REF_10KW_3LBUCK_SIC400 user guide

3-level flying capacitor buck with CoolSiC™ MOSFET 400 V G2

About this document

Scope and purpose

This document describes the details of the REF_10KW_3LBUCK_SIC400 evaluation platform and serves as a user guide for its safe operation.

The topology used in this platform is a 3-level-flying capacitor Buck DC/DC converter, which can also be reconfigured to be used as a 2-level Buck DC/DC converter. The primary goal of the platform is to enable the evaluation of CoolSiC™ G2 400 V and 650 V MOSFETs in TOLL and D2PAK-7 packages, as well as the EiceDRIVER™ 1ED-series isolated gate-drivers, and XMC4400 MCUs for high-performance SMPS applications.

Intended audience

This document is intended for design engineers, technicians, and developers of power electronic systems.

Reference Board/Kit

This board is to be used during the design-in process for evaluating and measuring characteristic curves (e.g., switching waveforms), and for testing the performance of the CoolSiC™ MOSFETs 400 V/650 V in a 3-level and 2-level buck topology.

Note: PCB and auxiliary circuits are NOT optimized for final customer design.

Note: Boards do not necessarily meet safety, EMI, quality standards (for example UL, CE) requirements

CoolSiC™ MOSFET 400 V G2

Infineon's CoolSiC™ MOSFET 400 V G2 are designed to offer high efficiency and extended reliability, while enabling exceptional ease of use. It's industry leading high gate-threshold voltage ($V_{gs,th}$ = 4.5 V) and the ability to turn off the device with zero gate bias ($V_{gs,off}$ = 0 V) while fully supporting negative gate bias turn-off voltages, makes the CoolSiC™ MOSFET 400 V G2 a true "normally-off" device with highly controllable and reliable switching behavior.

Core applications that the CoolSiC™ MOSFET 400 V G2 family supports include:

- Server (AI) and telecom SMPS
- Energy Storage Systems and UPS
- Renewables
- Motor control and drives
- Class-D Audio
- High voltage solid state power distribution

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Safety precautions

Note: Please note the following warnings regarding the hazards associated with development systems

Table 1 Safety precautions

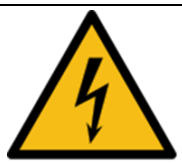
	**Warning:** *The DC link potential of this board is up to 400 VDC. When measuring voltage waveforms by oscilloscope, high voltage passive/differential probes must be used. Failure to do so may result in equipment damage, personal injury or death.*
	**Warning**: *The evaluation or reference board contains DC bus capacitors which take time to discharge after removal of the main supply. Before working on the drive system, ensure that capacitors are discharged to safe voltage levels. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Warning:** *Remove or disconnect power from the board before you disconnect or reconnect wires or perform maintenance work. Ensure that capacitors are discharged to safe voltage levels. Do not attempt to service the board until the bus capacitors have discharged to zero. Failure to do so may result in personal injury or death.*
	**Caution:** *The heat sink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.*
	**Caution:** *Only personnel familiar with the power electronics and associated machinery should plan, install, commission and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage. The cooling fan may operate at high speeds and is a potential injury hazard. Ensure personnel and object safety by maintaining sufficient clearance to the fan.*
	**Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	**Caution:** *A board that is incorrectly applied or installed can lead to component damage or reduction in product lifetime. Wiring or application errors such as undersizing the cabling, supplying an incorrect or excessive DC supply, or excessive ambient temperatures may result in system malfunction.*
	**Caution:** *The evaluation or reference board is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials that are unnecessary for system installation may result in overheating or abnormal operating conditions.*

Table of contents

1 Introduction: the board at a glance

The reference board REF_10KW_3LBUCK_SIC400 uses a 3-level-flying capacitor Buck DC/DC converter, which can also be reconfigured to be used as a 2-level Buck DC/DC converter. The primary goal of the platform is to enable evaluation of CoolSiC™ MOSFET 400 V and 650 V G2 in TOLL and D2PAK-7 packages. The reference design also aims to provide layout guidelines to optimize the commutation and gate loops and provide solutions for auxiliary supply for floating gate-drive, startup, pre-charging and voltage balancing of the flying capacitor in multi-level topologies. By enabling a fair benchmarking between 3-level (3L) and 2-level (2L) topologies, you can evaluate the following benefits of adopting a 3-level topology:

- Lower voltage swing across the inductor (factor 0.5 x) combined with the benefits of “series interleaving”, where the inductor ripple frequency is double that of the MOSFET switching frequency, allows for a significant reduction (factor 0.25 x) in required inductance value.
- For a given size, the inductor can be optimized to reduce conduction and core losses for higher efficiency. Alternatively, a smaller inductor can be used to increase power density.
- Lower blocking voltage across the MOSFETs enable the use of lower-voltage rated switches with better switching Figures of Merit (FoM) – effectively lowering the switching losses significantly.

Figure 1 shows the important functional blocks in the REF_10KW_3LBUCK_SiC400 platform. The design utilizes the following key components from Infineon:

- Power stage with CoolSiC™ MOSFET 400 V and 650 V G2, IMT40R011M2H and IMT65R010M2H
- EiceDRIVER™ compact fast single channel isolated gate driver 6.5 A, 1ED3141MU12F
- XENSIV™ high precision magnetic current sensor for AC and DC measurements, TLI4971 A050

1.1 Scope of supply

The board consists of the following components and items:

- REF_10KW_3LBUCK_SiC400 – main board with 3-level-flying capacitor Buck DC/DC converter, with CoolSiC™ MOSFET 400 V G2 IMT40R011M2H
- CoolSiC™ MOSFET 650 V G2 IMT65R010M2H (included)
- XMC™ control card using XMC4400F100F512BA (included)
- XMC™ Link Segger debugger/programmer (not included)
- Würth Elektronik inductors 760801122 (assembled) for 3-level and 760801102 (not assembled) for 2-level Buck DC/DC converter operation
- TDK stacked MLCCs CKG57NX7T2W225M500JH for flying capacitors (assembled)
- Bando TS103 100 x 100 mm T = 1.0 mm HeatEX thermal interface material (assembled)
- Assembly test report and safety guidelines

Introduction: the board at a glance

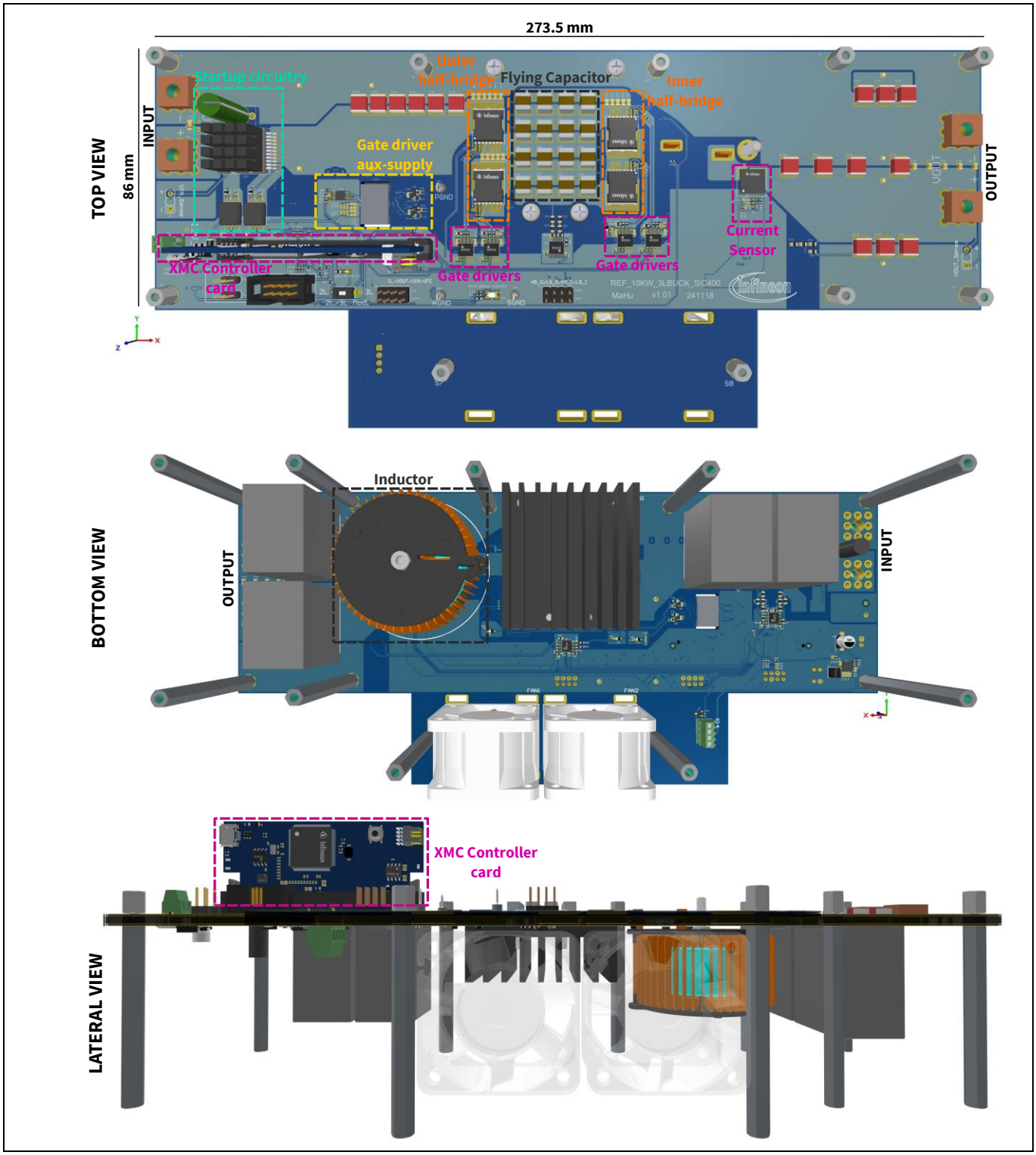


Figure 1 Description of the board

1.2 Description of the platform and block diagram

The following figure shows the topology and main functional blocks used in the REF_10KW_3LBUCK_SIC400 platform. The detailed description of the individual blocks is covered in Section 2.

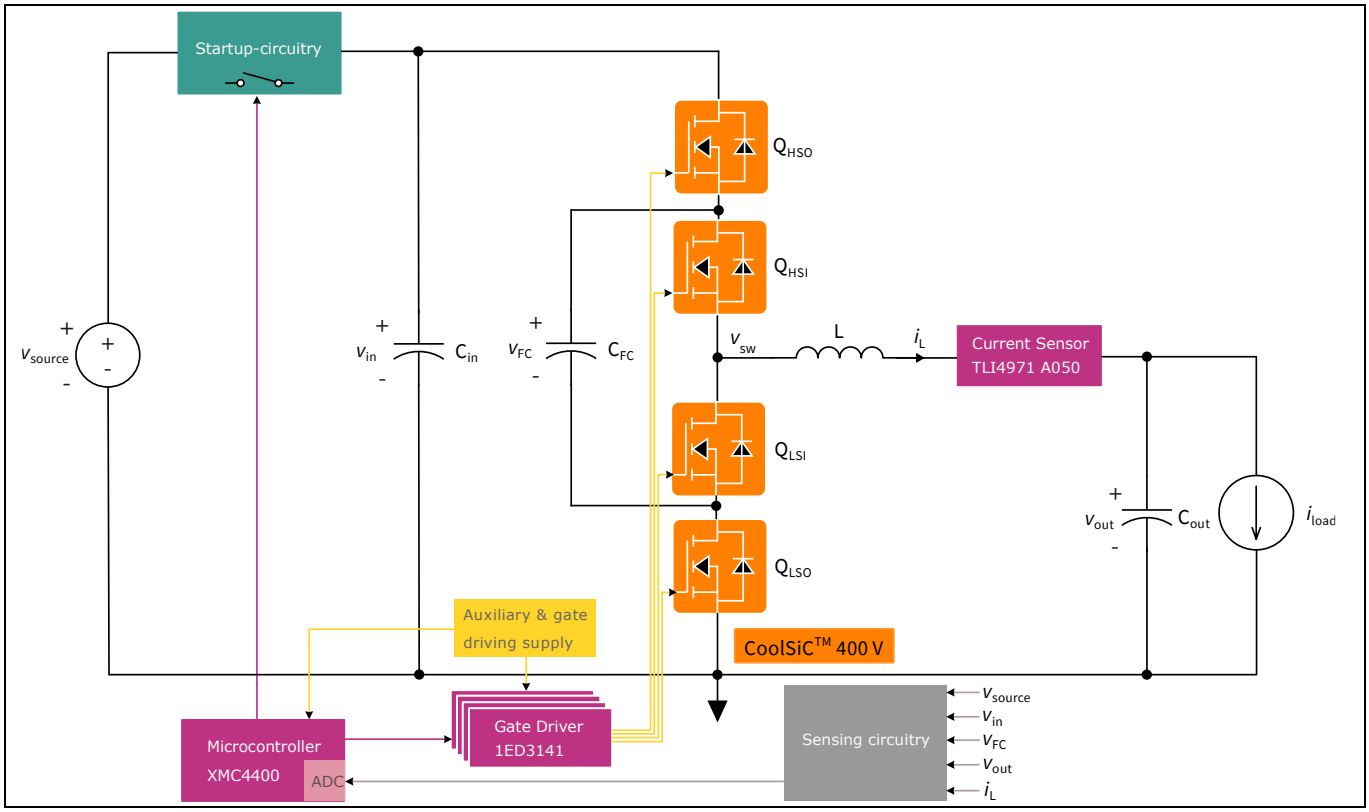


Figure 2 Block diagram of the REF_10KW_3LBUCK_SIC400 platform

1.3 Main features

- Platform to evaluate **CoolSiC™ 400 V or 650 V MOSFETs G2**, benchmarking 3L vs 2L topologies by shorting outer leg MOSFETs Q_{HSO} and Q_{LSO} for 2L operation
- **Flying capacitor balancing** algorithm
- **Low-cost and low-space** discrete planar-transformer based **isolated auxiliary gate drive supply** for 4 x HF leg MOSFETs
- Support for testing **bipolar vs. unipolar** gate drive with adjustable driving voltage
- Gate drive is selectable with respect to Kelvin-Source (KS 4-terminal drive) or Power-Source (PS 3-terminal drive)
- **Low commutation and gate-loop inductance** in a high-power design with a **heatsink** for cooling

1.4 Board specifications and test setup

Table 1 Key specifications of the board

Parameter	Symbol	Conditions	Value	Unit
Input voltage	VIN	Max. DC input voltage, Recommended current limit, IIN = 34 A.	400	V
Output current	IOUT	Max. DC output current in 3L mode Tsemi < 100°C with heatsink mounted and cooling FAN turned-on. *Note: Max. DC output current in 2L Mode = 24 A, refer to datasheet of 760801102 for details.*	34	A
Rated output power	POUT	Max. DC output power, VOUT = 300 V, IOUT = 33 A, Tsemi < 100°C with heatsink mounted and cooling FAN turned-on.	10	kW
Auxiliary supply voltage	VAUX	Max. DC aux. supply voltage, Recommended current limit, Iaux = 300 mA (MCU only) and Iaux = 2 A (fan included).	12	V
Mode	Switch1 (hardware flip switch)	Mode 1: 3L-FC-BUCK, Mode 2: 2L-BUCK, Selecting to 2L mode disables start-up and FC balancing but keeps the four PWMs switching. Refer Sections 2.1 and 2.5 for more details.	--	--
Default switching frequency	Fsw	Default value at start. To modify Fsw, enable the buck operation and then change the Fsw input via GUI. Recommended Fsw >= 32.5 kHz, with Tsemi < 100°C.	32500	Hz
Dead-time	Dead time (DT)	Default value at start, with Rg,ext,on = 1R, Rg,ext,off = 0R. Recommended DT >= 50 ns, with possibly higher DT needed if higher Rg,ext is used.	50	ns
Duty-cycle	Duty	Default value at start. VOUT = ~Duty x VIN. Limited by firmware, 0.05 <= Duty <= 0.95.	0.05	--
Gate driving voltage	VDR_nom	Default value at start uses unipolar driving. Alternative: Bipolar driving Vdrv = 18V/-3 V. Set Vdrv to 21V in GUI and solder Zener diodes D16, D17, D18, D19, R108, R109, R110, R111. Refer Sections 2.1 and 2.5 for more details.	18	V

Parameter	Symbol	Conditions	Value	Unit
		Note: GDS_fsw [Hz] is regulated automatically to ensure G2_VDR is regulated to the set VDR_nom value.		
External gate resistors	Rg,ext,on and Rg,ext,off	Rg,ext,on = R10, R18, R29, R38 Rg,ext,off = R12, R20, R31, R40	1 0	Ω Ω
Gate driving configuration	3-terminal and 4-terminal	For 4-terminal driving: solder R13, R21, R32, R41 For 3-terminal driving: solder R15, R23, R34, R43	--	--
FAN speed	Fan speed [%]	*Note: "Fan auto mode" = 1 (enabled) sets fan speed automatically as a function of measured load current.*	0-100	--
Enable	Buck enabled	Set flag = 1 to start operation.	0/1	--

Table 2 Headers, connectors and test-points

Symbol/Name	Description	Comment
X1	Auxiliary supply voltage, VAUX	12 V/2 A
X2	Positive rail VIN+	+400 V
X7	Negative rail VIN-	PGND/0 V
X4	Sense connector VIN	HV potential!
X5	Positive rail VOUT+	Up to 380 V
X6	Sense connector VOUT	HV potential!
X3	Negative rail VOUT-	PGND/0 V
X8	PWM signal probing points	
X9	Analog sense probing points for VFC, VIN, VOUT, IL	
X10	XMC debug connector	
X11	XMC control card plug-in socket	
X12	Iaux sense connector for gate drive aux. supply current	
X13	Vaux sense connector for gate drive aux. supply voltage	
X14	Supply for cooling fans	

Table 3 Required equipment

Equipment	Signal & Header	Comments
Electronic high-voltage DC power supply	VIN, X2, X7	Capable to supply up to 400 V/34 A.
Electronic high-voltage DC load or High power resistive load bank	VOUT/IOUT X5, X3	Capable of handling loads up to 400 V/34 A.
Electronic low-voltage DC power supply	VAUX X1	Capable of supply up to 12 V/2 A.
Personal computer (PC) with USB-cable		To connect to the REF_10KW_3LBUCK_SIC400 using the XMCLink.
Multimeter	VIN, VOUT X4, X6	For HV signals VIN, VOUT
Datalogger/multimeter		For LV signals – IOUT, IIN connected to shunts placed on the “low-side” low-voltage return path.
Oscilloscope (recommended)		Power HV signals (e.g., Vsw, Vds, Vgs) were measured using optically isolated high-voltage high-bandwidth probes (e.g., IsoVu, Firefly). PWM signals (e.g., PWM_HSO and PWM_HSI) were measured using LV passive probes to trigger waveforms.
Thermal imaging camera (recommended)		

Attention: The board including the XMC link is at a high-voltage potential. Isolation to PC is ensured via the XMC-link.

2 System and functional description

2.1 Getting started

The following steps are needed to set up the platform for operation:

1. To initially flash the controller, DAVE IDE and Segger J-Link driver are needed. For installation, follow the recommended procedure of the installers
   a) Download the latest firmware for the REF_10KW_3LBUCK_SiC400 from the webpage after registering the purchased board with the serial number. This needs to be flashed to unlock all the functionalities of the board (e.g., variable dead-time control).
   b) Plug in the XMC™ control card to the socket X11 on the main power board. Connect the PC to the XMC control card using the XMC link and a USB cable capable of data transfer.

   Precautionary notes:

   - Galvanic isolation between the control/power board and the PC is provided through the XMC™ link.
   - Ensure that the USB cable is sufficiently far away from the switching stage and the buck inductor to avoid any potential unwanted coupling of noise.
2. Connect an auxiliary power supply V_{aux} = 12 V with $I_{aux,limit}$ = 2 A at X1. Ensure that the power consumption is not exceeding approx. 2 W (<200 mA). The test setup is shown in the following figure.

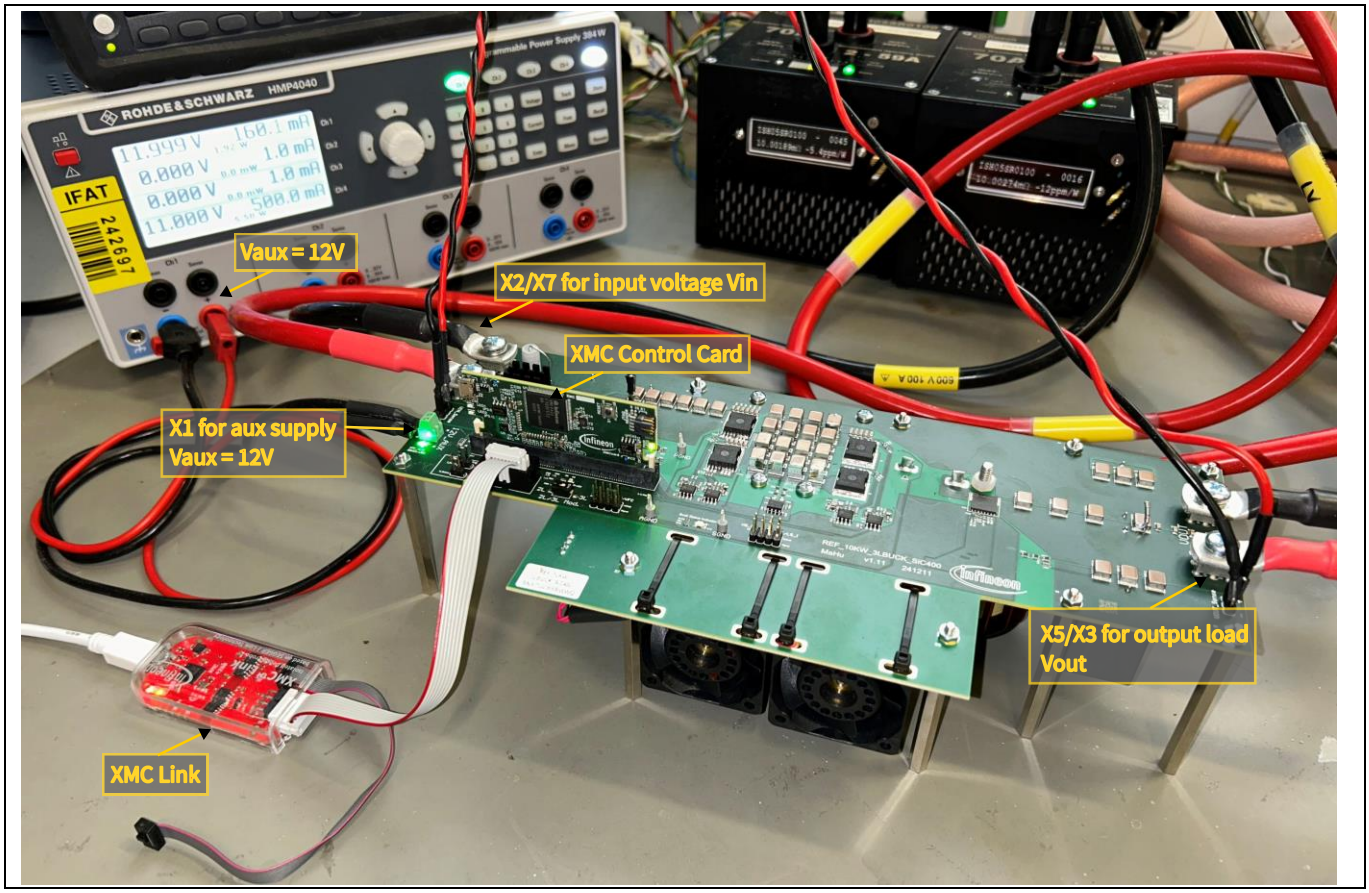


Figure 3 Test setup used for measurements

3. Open DAVE IDE, navigate to **File** > **Import** > **Select Directory / Archive File** > **Import Project** and import the project
4. Click Build Active Project (1)

The console presents a **Build Finished** message.

a) Click **Debug**

b) Choose **GDB SEGGER J-LINK Debugger** (3) under Debug Configurations (3)

c) Press Debug (4)

The Debug window opens.

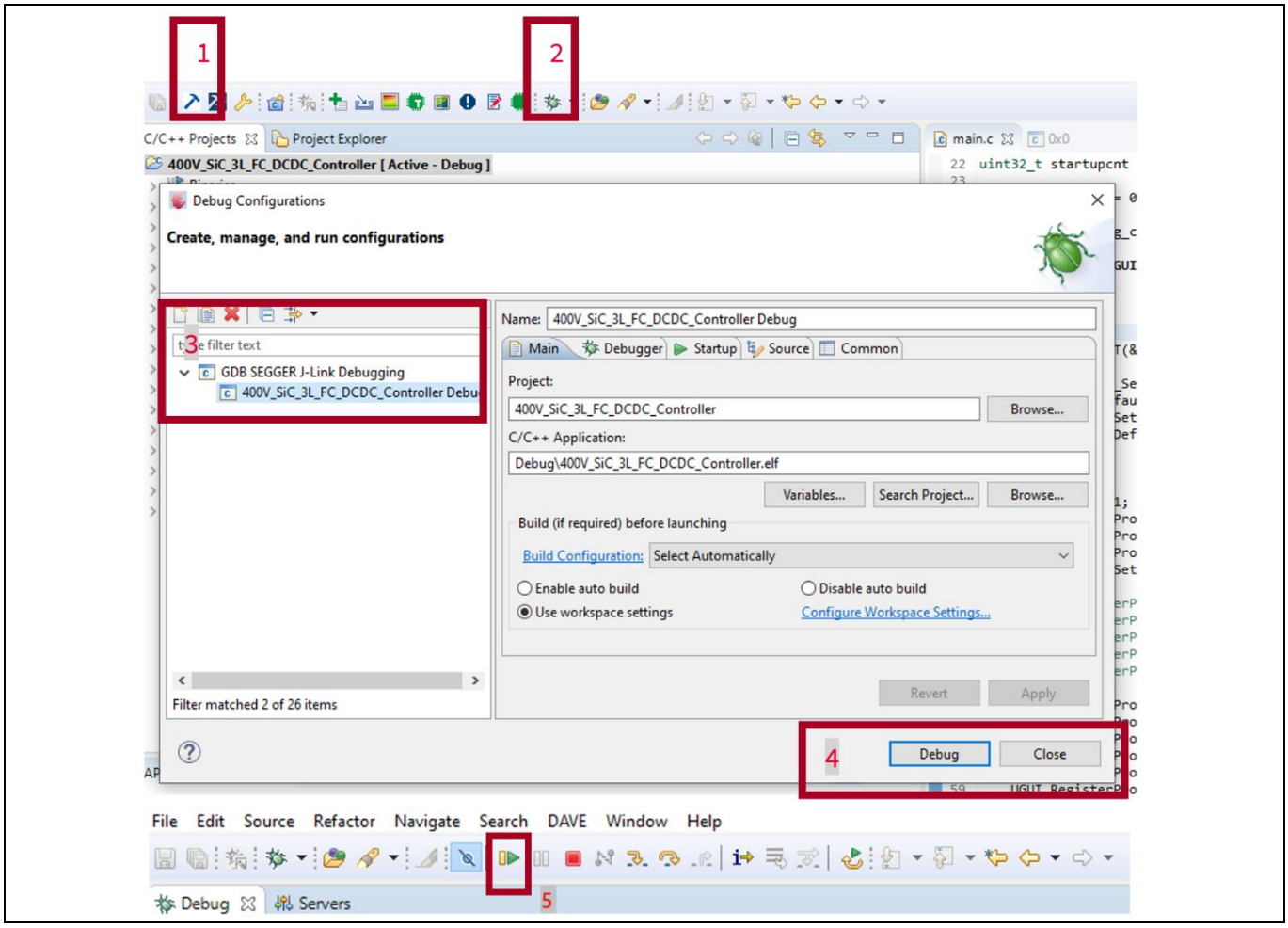


Figure 4 Flashing the latest firmware using DAVE

5. Click **Resume** (4) to finish flashing the controller. The firmware is now actively running on the controller. You can close the DAVE IDE
6. Open **UGUI_UniversalApp** from the *UniversalApp* folder and perform the following steps to configure the app to the latest functionalities provided in the latest firmware downloaded from the website

   a) In the **Interface Settings** section, click **Connect** (1)

   b) Navigate to **Commands** tab and click **Auto-Configure All** (2)

   The command information is downloaded (3) and updated (4) and (5).

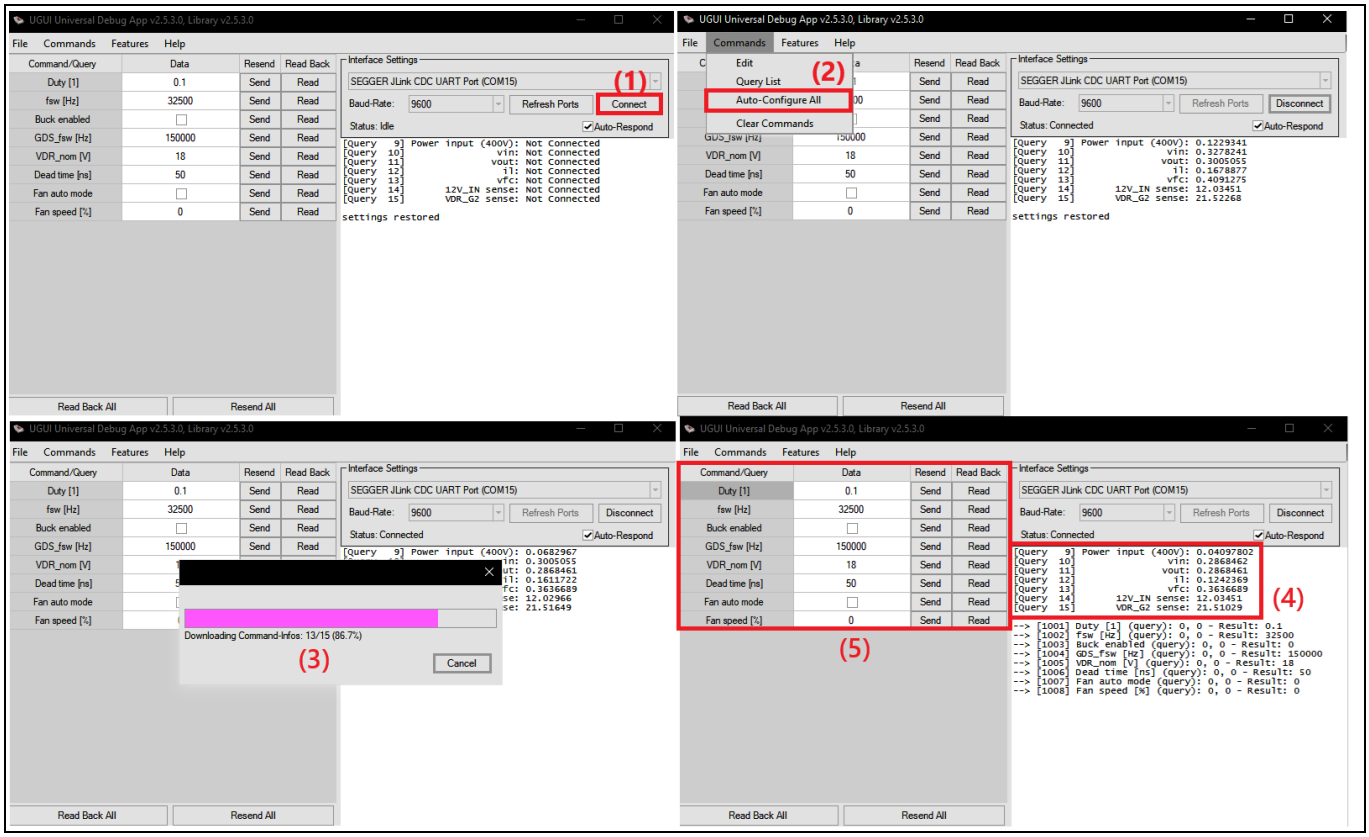


Figure 5 Setting up UGUI_UniversalApp to control the buck-mode operation

7. Connect the input power supply for VIN at X2/X7, and output load for VOUT at X5/X3

   Supply at least 55 V at the input to enable the board operation.

8. Use Switch1 to define the operation mode
   a) For 3-level buck move switch position to the right
   b) For 2-level buck move switch position to the left

   Ensure that 650 V MOSFETs are soldered for HSI and LSI (inner-leg MOSFETs) and 2L-buck inductor 760801102 is used. Additionally, short HSO and LSO drain-source and add a resistor between gate-kelvin source (4-terminal drive) or gate-power source (3-terminal drive) of HSO and LSO to emulate a load equaling the gate driver power of the used DUT for the aux-supply winding of HSO and LSO drivers. This is needed because the VDRV_LSO = (G2_VDR+) – (G2_VDR-) is sensed to regulate the VDR_nom voltage of the gate driver aux supply. As an example, with IMT65R010M2H with gate charge Q_g = 113 nC, for a switching frequency f_{sw} = 32.5 kHz and V_{drv} = 18 V/0 V, the gate drive power P_{drv} = 66 mW. This can be emulated by a 4.9 kΩ resistor connected between the gate-source of the HSO and LSO MOSFETs.

9. Turn on the converter by pressing “Buck enabled” button in the UGUI UniversalApp

2.2 Basic operation in 3L-FC-BUCK mode

The topology consists of four MOSFETs connected in series. At any point in time, only two MOSFETs conduct, and a flying capacitor is used as a “reservoir” to ensure balanced voltage sharing between the two blocking MOSFETs such that each MOSFET blocks $V_{in} – V_{FC}$. The steady-state voltage of the flying capacitor should be maintained at around $V_{in}/2$, so that the blocking voltage of each MOSFET is ~$V_{in}/2$. The four MOSFETs can be simplified into two half-bridges – outer (Q_{HSO}, Q_{LSO}) and inner (Q_{HSI}, Q_{LSI}) – which operate in a “series interleaved” fashion with a phase shift of 180° between the PWM signals of the outer and inner half-bridges.

Figure 6 and Figure 7 show the operation modes of a 3L-FC-BUCK in D < 0.5 and D > 0.5 conditions respectively. Note that all the non-black color coded MOSFETs represent their ON state.

For D < 0.5, the switching node voltage V_{sw} swings between $V_{in}/2$ and 0 V. For D > 0.5, V_{sw} swings between V_{in} and $V_{in} – V_{FC}$. For D = 0.5, V_{sw} will alternate between $V_{in} – V_{FC}$ and V_{FC}.

The D = 0.5 mode is the worst-case condition with the highest voltage ripple on the flying capacitor. As the V_{sw} can swing between three-levels, i.e. V_{in}, $V_{in} – V_{FC}$ and 0 V, this topology is called a 3-level Buck. It can also be noted that in a switching cycle, the flying capacitor has a charging and discharging state of operation. By controlling the duration of these two periods and ensuring a steady-state balance of $Q_{charge} = Q_{discharge}$, the voltage of the flying capacitor can be regulated as discussed in Section 2.2.2.

It is also important to note that the ripple period, T_{ripple}, of the inductor is half that of the switching period, T_{sw}, of the MOSFETs. This indicates the “frequency doubling” effect due to the series interleaving operation, where the ripple frequency of the inductor is twice the switching frequency of the MOSFETs.

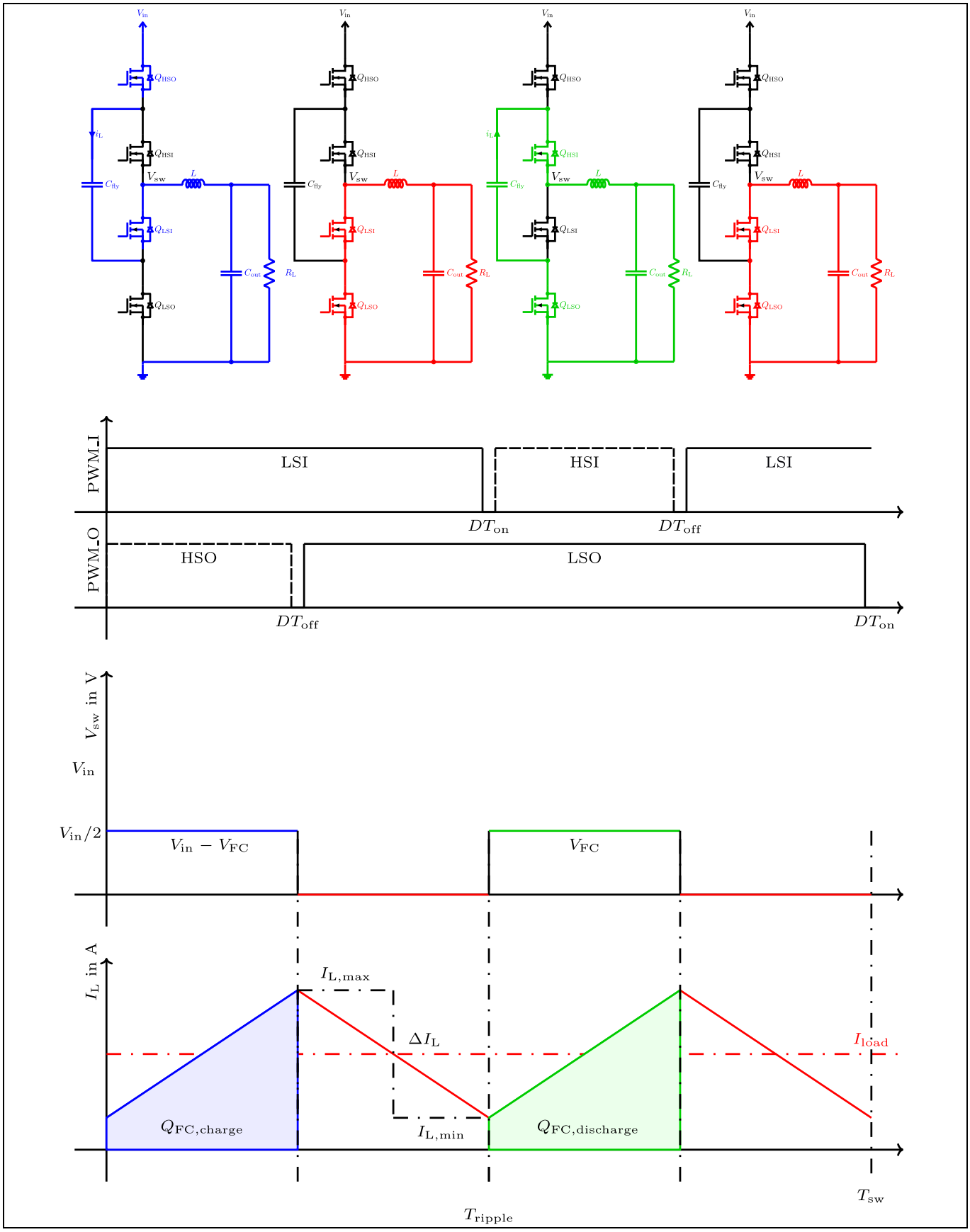


Figure 6 Conduction modes for D < 0.5 in 3L-FC-Buck mode

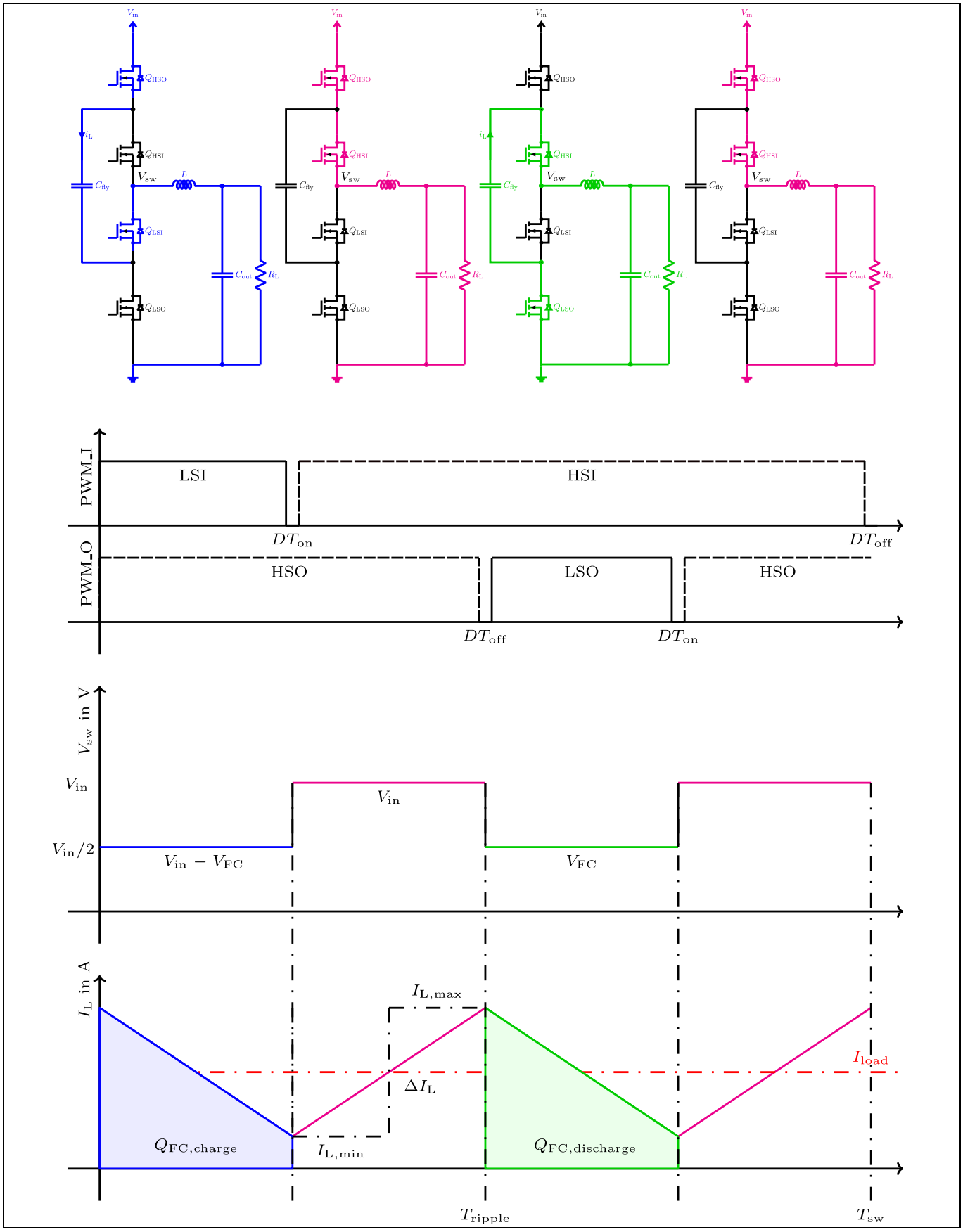


Figure 7 Conduction modes for D > 0.5 in 3L-FC-Buck mode

2.2.1 Dimensioning of the flying capacitor

The dimensioning of the flying capacitor depends on the following parameters:

- Switching frequency (f_{sw}): higher f_{sw} → lower C_{FC}.
- Maximum allowed voltage ripple (ΔV_{FC}): higher ΔV_{FC} → lower C_{FC}. Typically, ΔV_{FC} = 10 – 20% of $V_{FC,typ}$.
- Maximum load dependent inductor current (i_L): higher i_L → higher C_{FC}.

The following equations describe the impact of these parameters on the dimensioning of the flying capacitor.

$$\Delta Q_{FC} = i_L * \Delta t$$

$$\Delta t = (0.5 - |D - 0.5|) * T_{sw}$$

$$\Delta Q_{FC} = C_{FC} * \Delta V_{FC}$$

$$C_{FC} \geq \frac{i_L}{\Delta V_{FC} * 2 * f_{sw}} \; at \; D = 0.5$$

Equation 1 Equations for dimensioning of the flying capacitor

For high power density designs (e.g., AI server PSUs and BBUs) that also require high reliability, MLCC capacitors with soft-edge termination or metal-cap termination, along with a good PCB design to minimize solder-stress can be a good solution [2]. Typically, MLCCs with X7T or similar material also have a drop of capacitance under DC and temperature bias. Therefore, 450 V rated stacked metal-cap MLCC capacitors (CKG57NX7T2W225M500JH) were used in this design to mitigate the drop in capacitance, as well as enable experimenting with various switching frequencies and operation in the 2-level buck mode by simply shorting the outer-leg MOSFETs. Due to the necessity to provide flexibility to the user, the flying capacitor bank in this design has been over-dimensioned, with significant room for optimization in designs for mass-production.

2.2.2 Voltage balancing of the flying capacitors

The voltage of the flying capacitor needs to be maintained around $V_{FC} = V_{in}/2$ during the operation of the converter. However, there are many factors that can result in a deviation from its nominal value:

- Source impedance (ESL and ESR of capacitors and other commutation loop stray impedances) resulting in an input voltage ripple ΔV_{in}
- Mismatch in MOSFET parameters like $R_{ds,on}$, C_{iss}, C_{oss}, C_{rss}
- Mismatch in gate driver parameters, gate drive voltages and gate loop impedances

The control strategy to regulate the V_{FC} voltage uses the phase-shift between the inner and outer half-bridges as the control variable, as shown in Figure 8. A high-level control block diagram is shown in Figure 9.

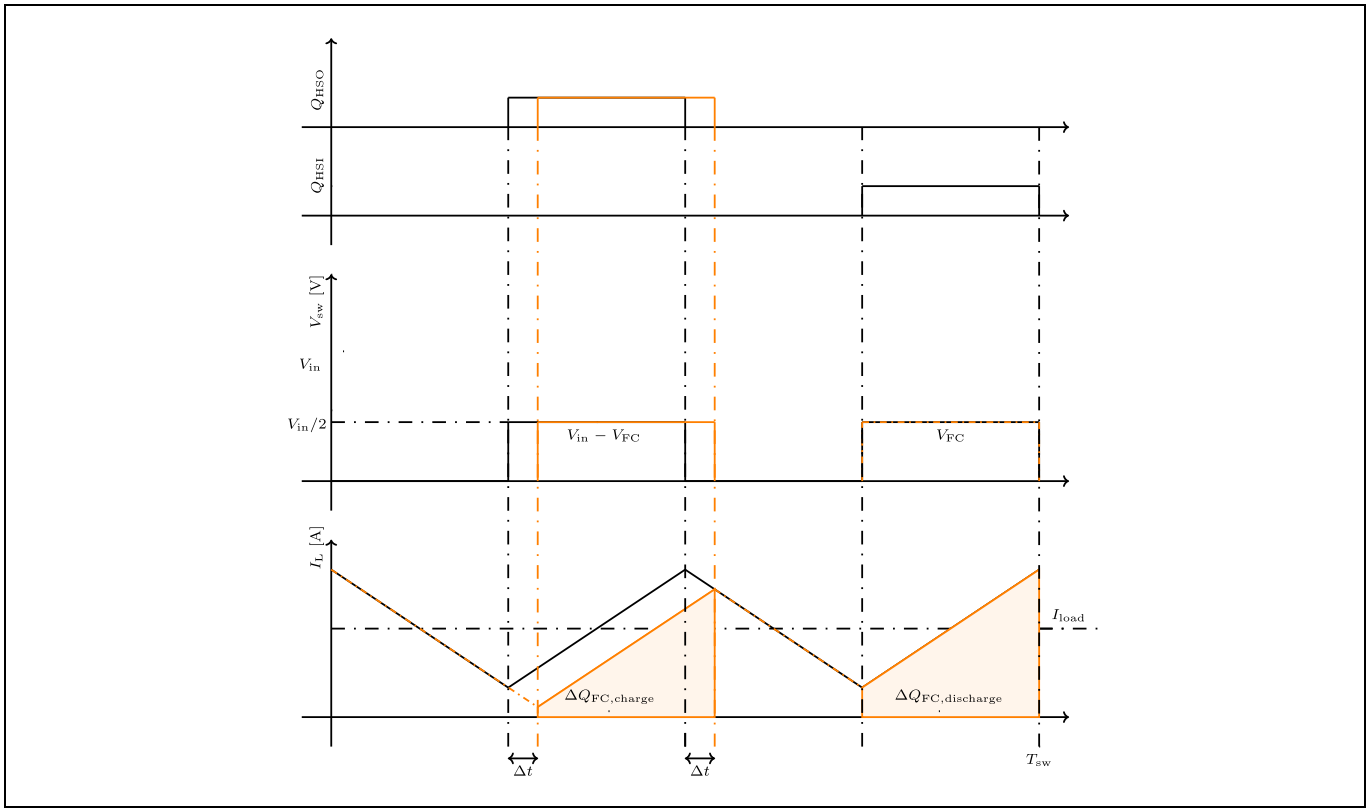


Figure 8 **Idealized exaggerated waveforms showing phase shift control and the resulting manipulation of effective charge delivered to the flying capacitor**

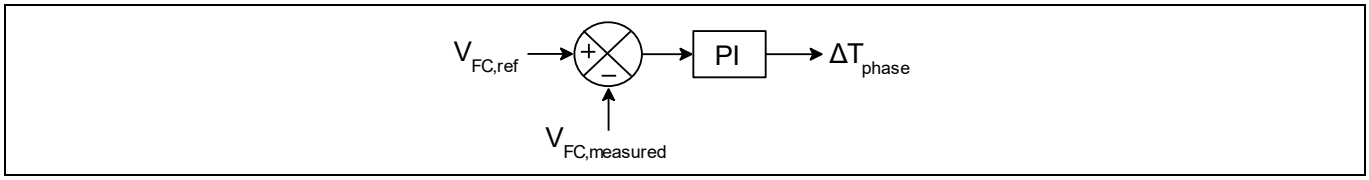


Figure 9 **Flying capacitor voltage balancing control loop**

2.2.3 Startup and pre-charging of the flying capacitor

The startup and pre-charging of the flying capacitor is implemented in hardware using the circuitry shown in **Figure 10**.

Before the start-up process can begin, the V_{AUX} = 12V supply must be connected and a PC must be connected using XMC-link to run the control GUI. The start-up and pre-charge is started when the START = 1 signal (“Buck enabled” button) is triggered using the control GUI. The high-ohmic small-signal MOSFET $Q_{startup}$, which is connected in series with the high-ohmic $R_{startup}$, is turned ON along with Q_{HSO} and Q_{LSO}. This provides a controlled RC charging circuit for both C_{in} and C_{fly}, which are effectively connected and charging in parallel. The controller measures the flying capacitor voltage V_{FC} during the start-up and turns-OFF Q_{HSO} and Q_{LSO} when V_{FC} = 0.5 x V_{SOURCE}.

When the input capacitor voltage V_{Cin} reaches the V_{SOURCE}, the start-up small-signal MOSFET $Q_{startup}$ is turned-off and the low-ohmic MOSFET Q_{normal} is turned-ON. The PWM operation is then started with soft-start, with the duty-cycle D slowly ramped up to the target duty-cycle value set using the GUI. The start-up waveforms are shown on Figure 11 for the 3L-Buck mode of operation, with high-voltage differential probes used to measure floating potential waveforms (e.g., V_{FC}). For the 2L-Buck mode, Q_{HSO} and Q_{LSO} must be physically shorted and

Switch1 set to the left position to enter 2L-Buck mode. The start-up process will be handled as described for the 3L-Buck mode.

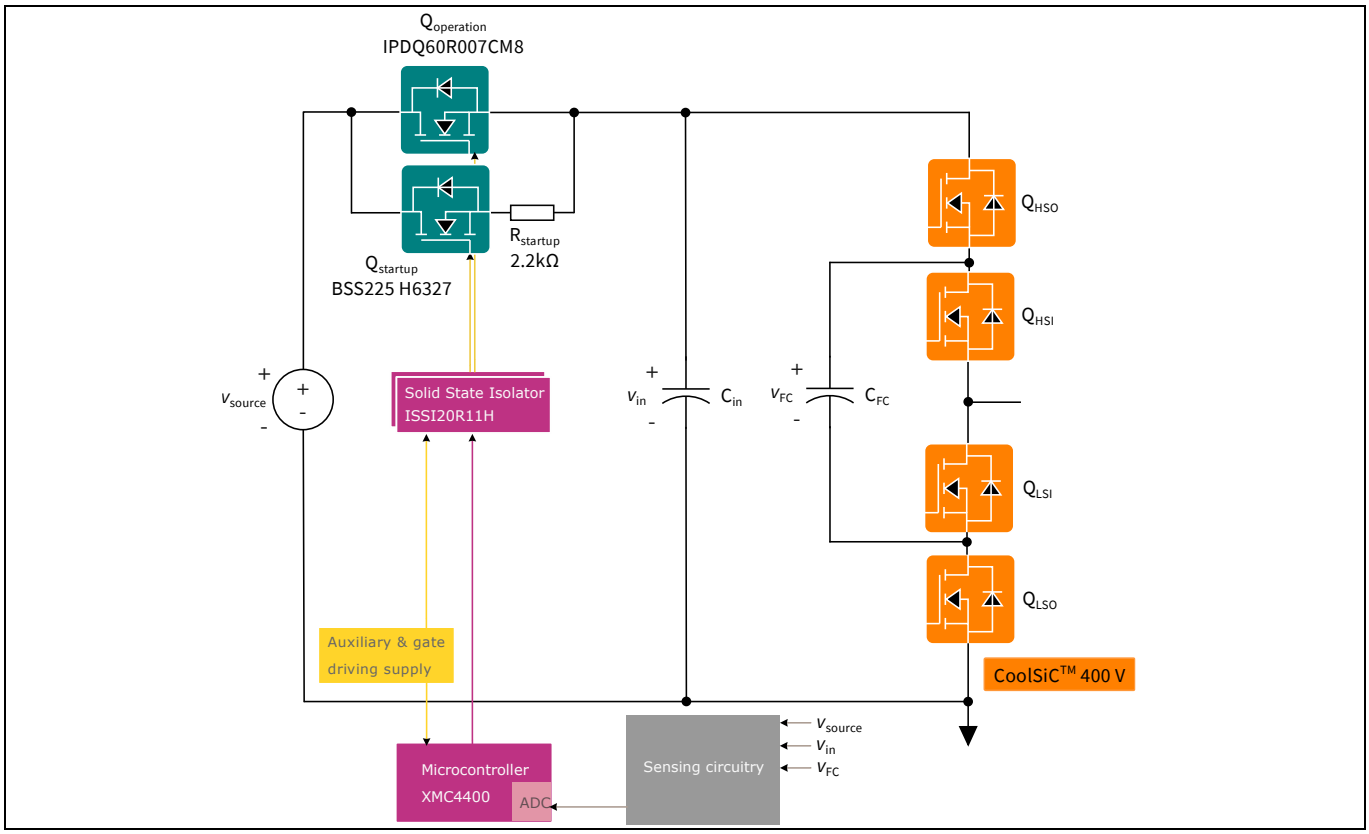


Figure 10 Simplified start-up and pre-charging circuitry

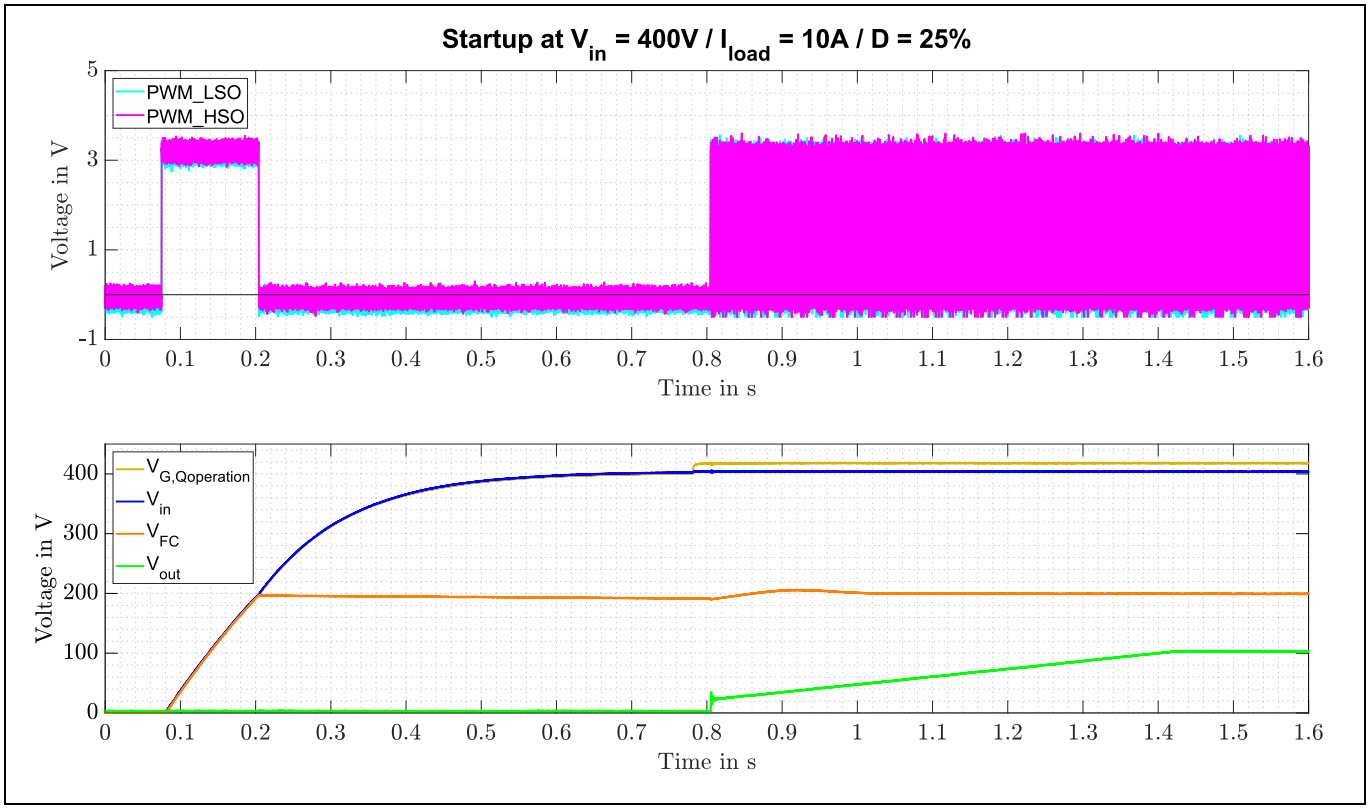


Figure 11 Measured start-up and pre-charging waveforms

2.3 Basic operation in 2L-BUCK mode

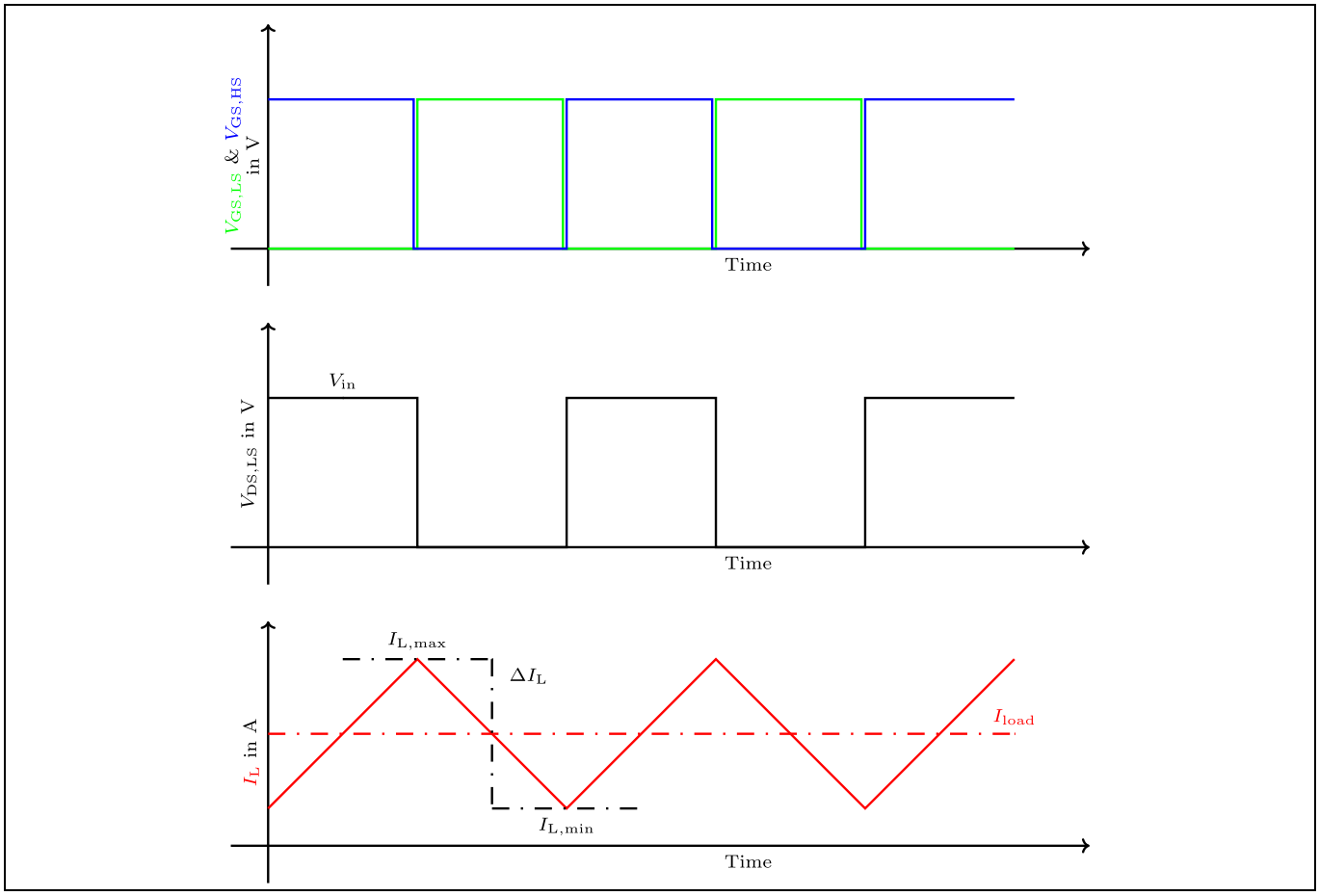


Figure 12 Typical waveforms of a 2-level Buck converter operated in CCM mode (idealized)

2.4 Comparison: 3L vs. 2L mode

In the 3L mode, the following advantages apply compared to the 2L mode, as illustrated in Figure 13.

- Reduced voltage applied across the inductor during all the modes of operation
- Effective frequency at the switching node is double that of the device switching frequency
- This results in an effective volt-seconds applied to the inductor reduced by a factor ¼ compared to the 3L mode, for a given switching frequency and inductance

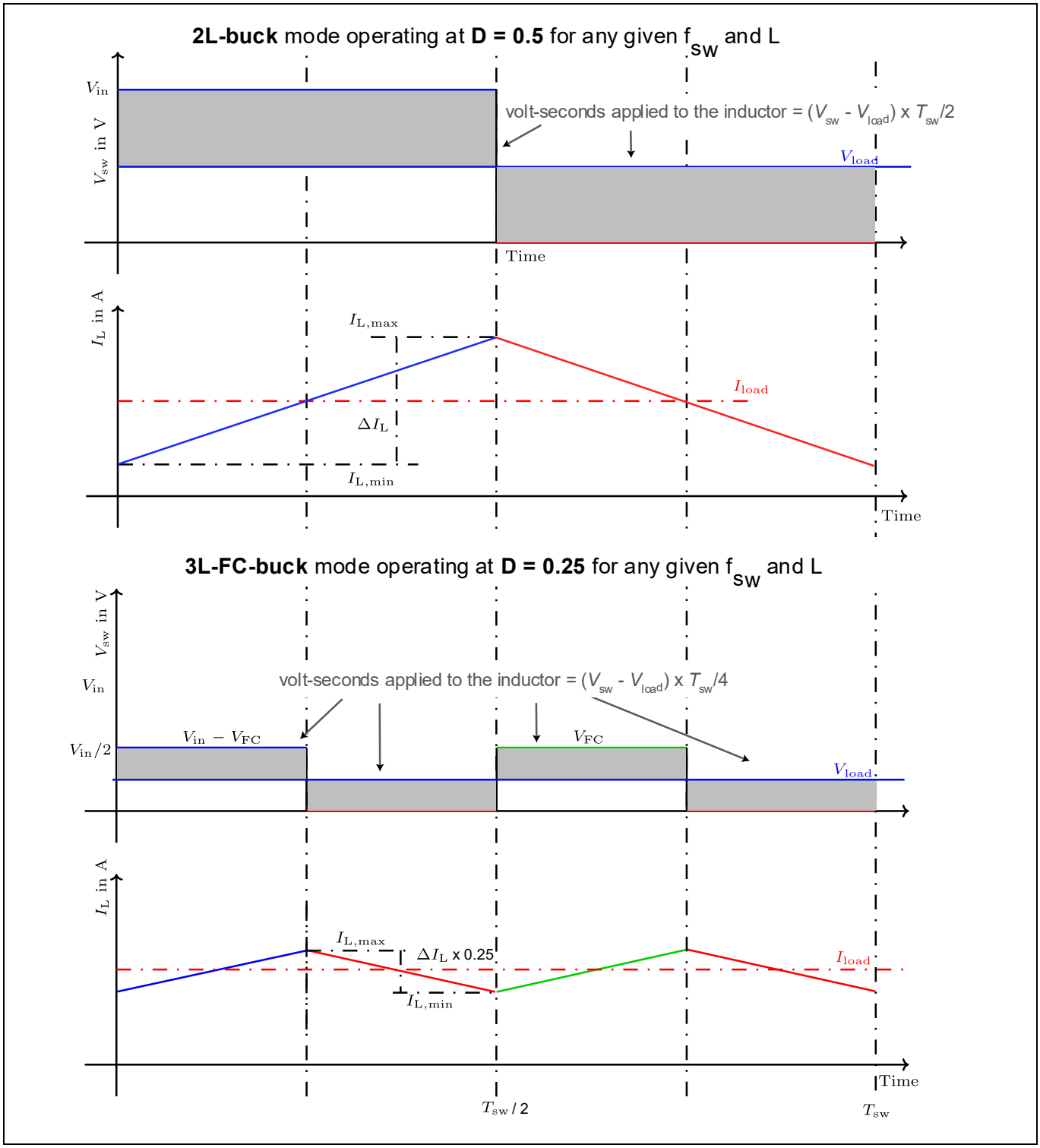


Figure 13 Comparison of volt-seconds applied to the inductor and the impact on the worst-case ripple current in 2-level and 3-level modes

Figure 14 shows the normalized ripple currents as a function of duty cycle for a given switching frequency and inductance value. This provides further insights into the degrees of freedom in designing the 3-level flying capacitor buck: (1) potential to reduce inductance and (2) choice of switching frequency as a lever to balance the reduction of inductance and the converter efficiency. This is illustrated in **Table 4**.

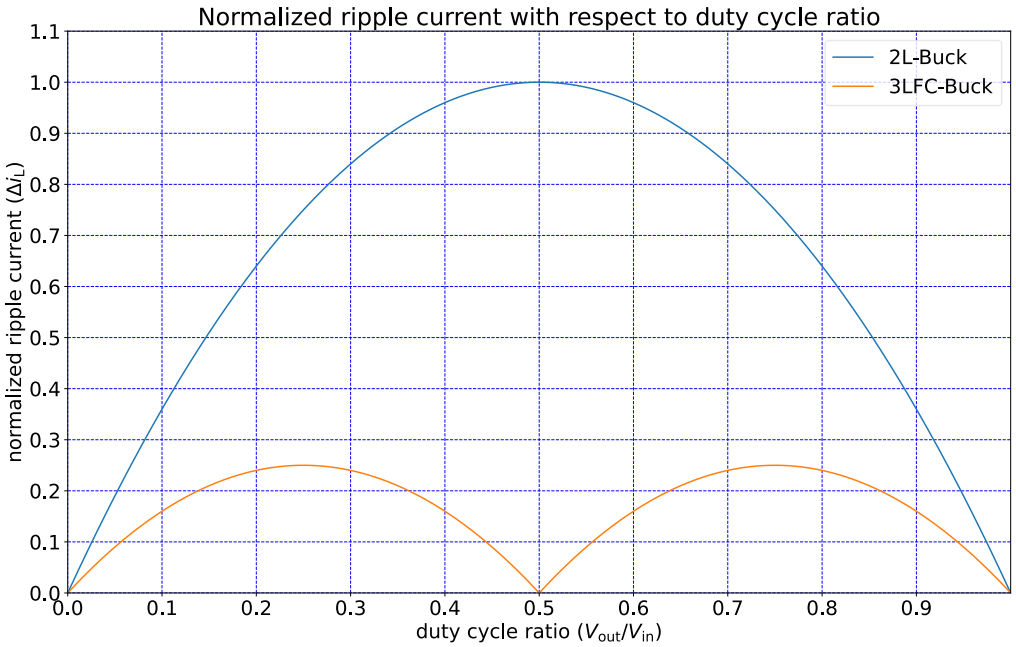


Figure 14 **Normalized ripple current for a given switching frequency and inductance value as a function of duty cycle of operation in 2-level and 3-level modes**

Table 4 **Degrees of freedom in designing a 3-level flying capacitor topology**

Topology		**Case 1:** f_{sw} (3L) = f_{sw} (2L)	**Case 2:** f_{sw} (3L) = f_{sw} (2L)/2
Conduction losses	2-level	$P_{cond} = I_{rms}^2 R_{on}$	$P_{cond} = I_{rms}^2 R_{on}$
	3-level	$P_{cond} = 2\ I_{rms}^2 R_{on}$	$P_{cond} = 2\ I_{rms}^2 R_{on}$
Switching losses	2-level	$P_{sw} = f_{sw} E_{sw}$	$P_{sw} = f_{sw} E_{sw}$
	3-level	$P_{sw} = 2\ f_{sw} (E_{sw}/2)$	$P_{sw} = 2\ (f_{sw}/2)\ (E_{sw}/2)$
Inductance and ESR for same Δi_L	2-level	L and ESR	L and ESR
	3-level	L/4, much lower ESR and smallest inductor	L/2, lower ESR and smaller inductor
Design outcome		Optimized for highest power density	Optimized for highest efficiency

2.5 Isolated auxiliary supply for the gate-drive

The gate driving scheme uses four isolated auxiliary supply voltages for driving each of the four MOSFETs. The four isolated auxiliary gate driver supply voltages are implemented using an isolated resonant multi-winding DC/DC converter using a planar transformer, as shown in **Figure 15**. The design target is as follows:

- Convert input V_{aux} = 12 V to an output V_{drive} = 18 V +/- 0.5 V for all four outputs
- Provide flexibility to use unipolar (18 V/0 V) or bipolar gate driving (18 V/-3 V)
- Minimize the idle power consumption and power loss during operation
- Minimize the coupling capacitances between the secondary windings to enable high CMTI and suppress parasitic coupling
- Provide functional isolation between input and output
- When operated in 2L mode, mount a resistor between gate and PS/KS of LSO (where the voltage is sensed) to emulate the gate drive power of the mounted HSI and LSI MOSFETs

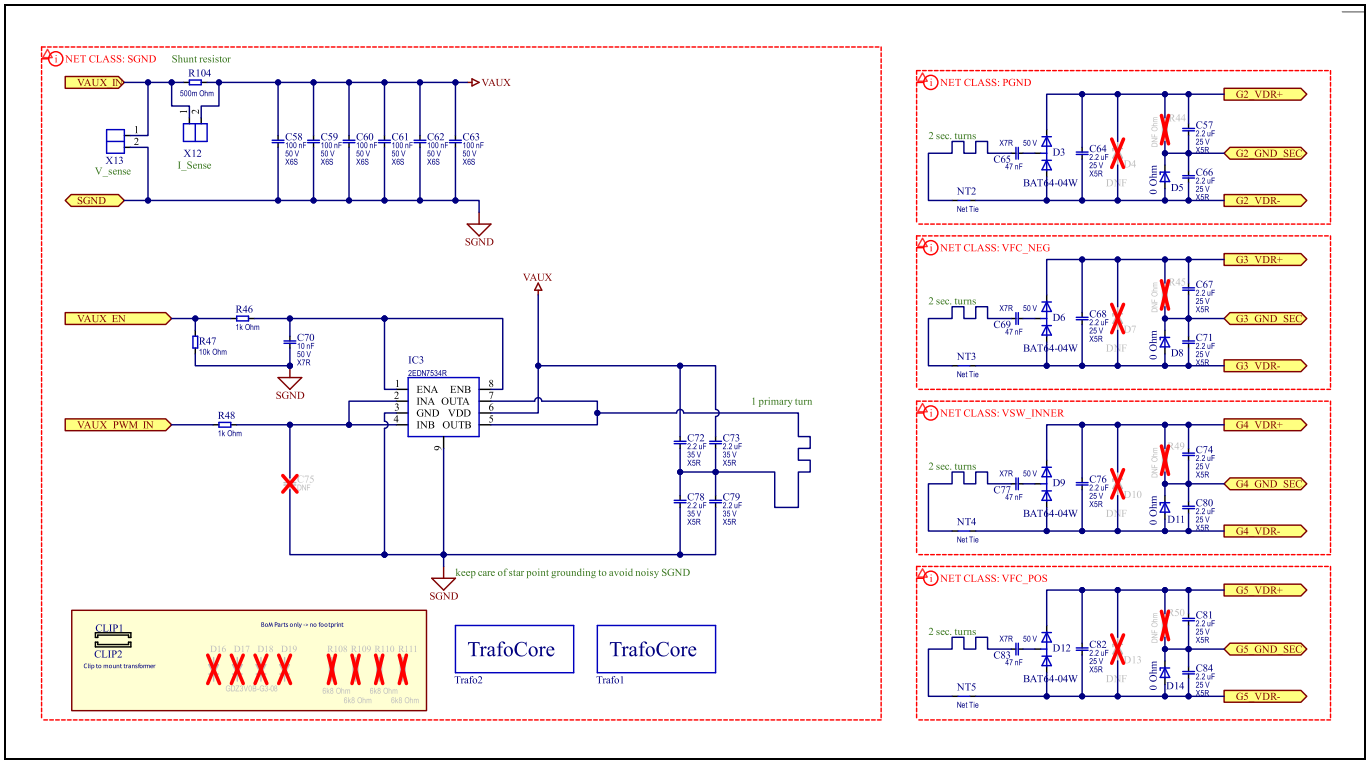


Figure 15 Schematic of the isolated aux. power supply for gate driving

- By default, the board is configured to operate in unipolar gate driving mode
  - R44, R45, R49, and R50 are not assembled
  - D5, D8, D11, and D14 are replaced by zero-ohm resistors
- To configure the isolated auxiliary power supply for bipolar driving, the following hardware changes must be carried out:
  - Assemble 6k8 ohm resistors for R44, R45, R49, R50
  - Assemble GDZ3V0B-G3-08 Zener diodes for D5, D8, D11, D14
- Set the proper gate driving voltage in the control GUI
  - The control value defines the total voltage at the secondary side of the drivers, such that VDR_nom = $V_{DR,on}$ – $V_{DR,off}$, with $V_{DR,off}$ = 0 V for unipolar and V_{Zener} (= -3 V) for bipolar driving
  - For unipolar driving with 18 V/0 V, $V_{DR,off}$ = 0 V and thus VDR_nom = 18 V

– For bipolar driving with 18 V/-3 V, $V_{DR,off} = V_{Zener}$ = -3 V and thus VDR_nom = 21 V

The following figure shows the power dissipation in the auxiliary supply as a function of switching frequency for various driving voltages in the 3L-mode with IMT40R011M2H.

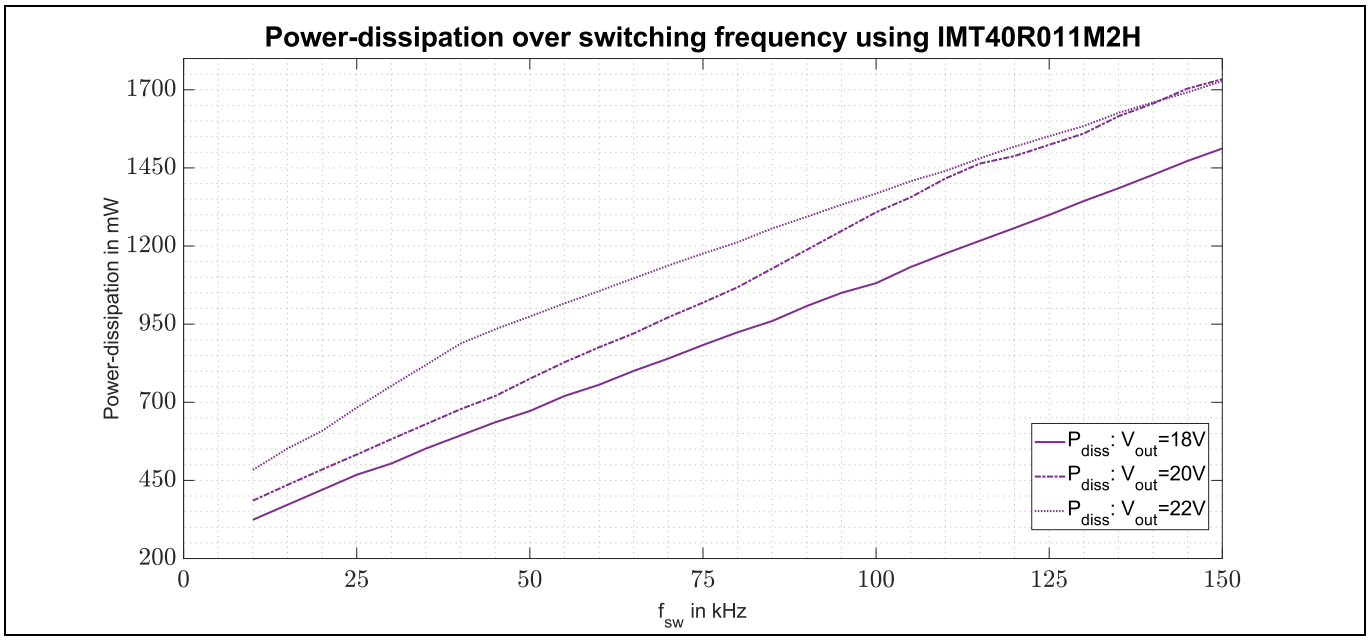


Figure 16 Aux. supply power consumption as a function of switching frequency in 3L-operation

3 System design

3.1 Schematics

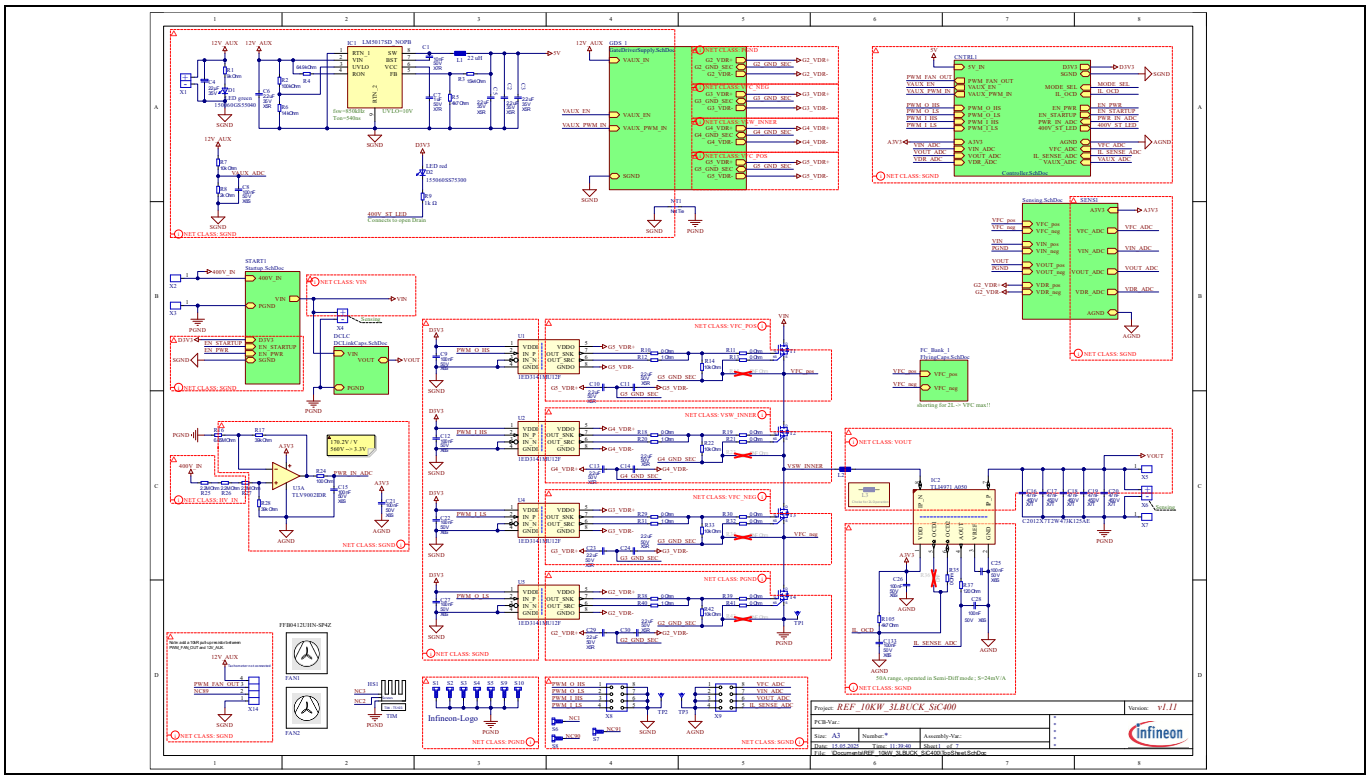


Figure 17 Schematic of the power stage (top-sheet)

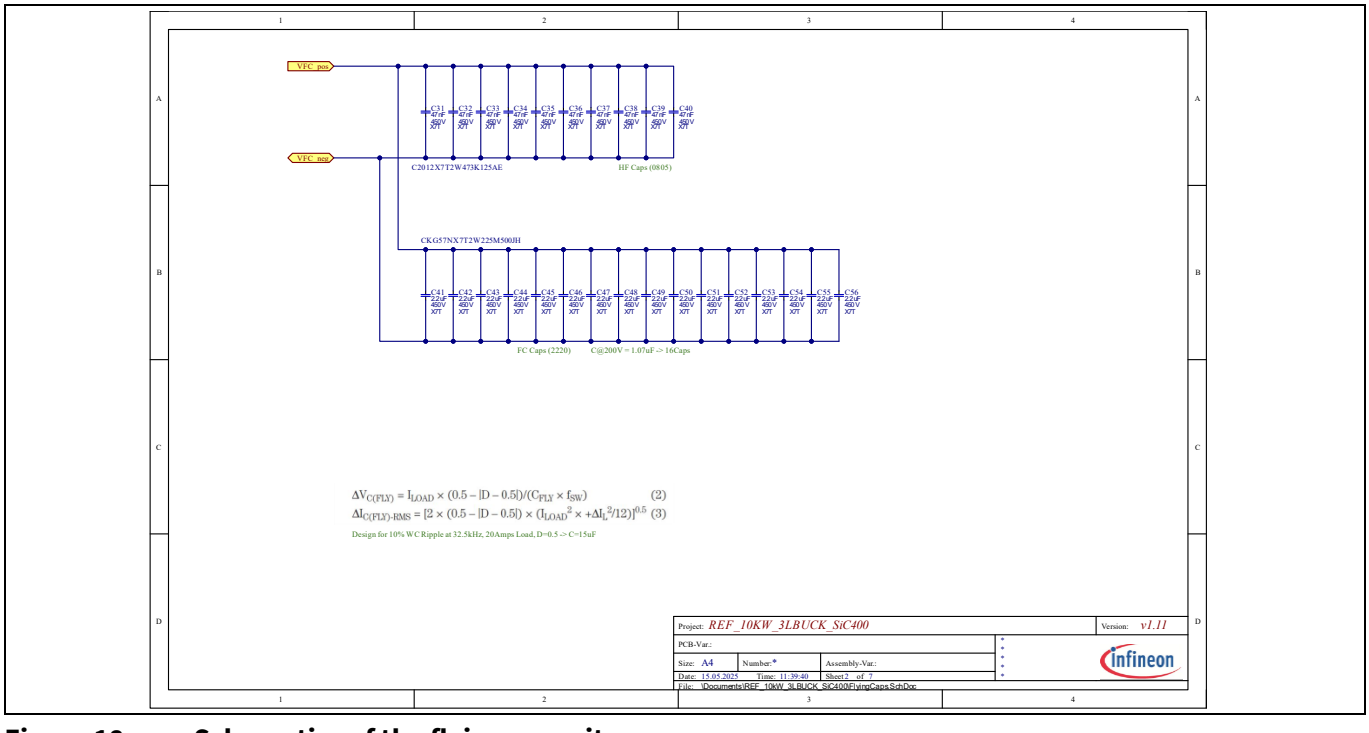


Figure 18 Schematics of the flying capacitor

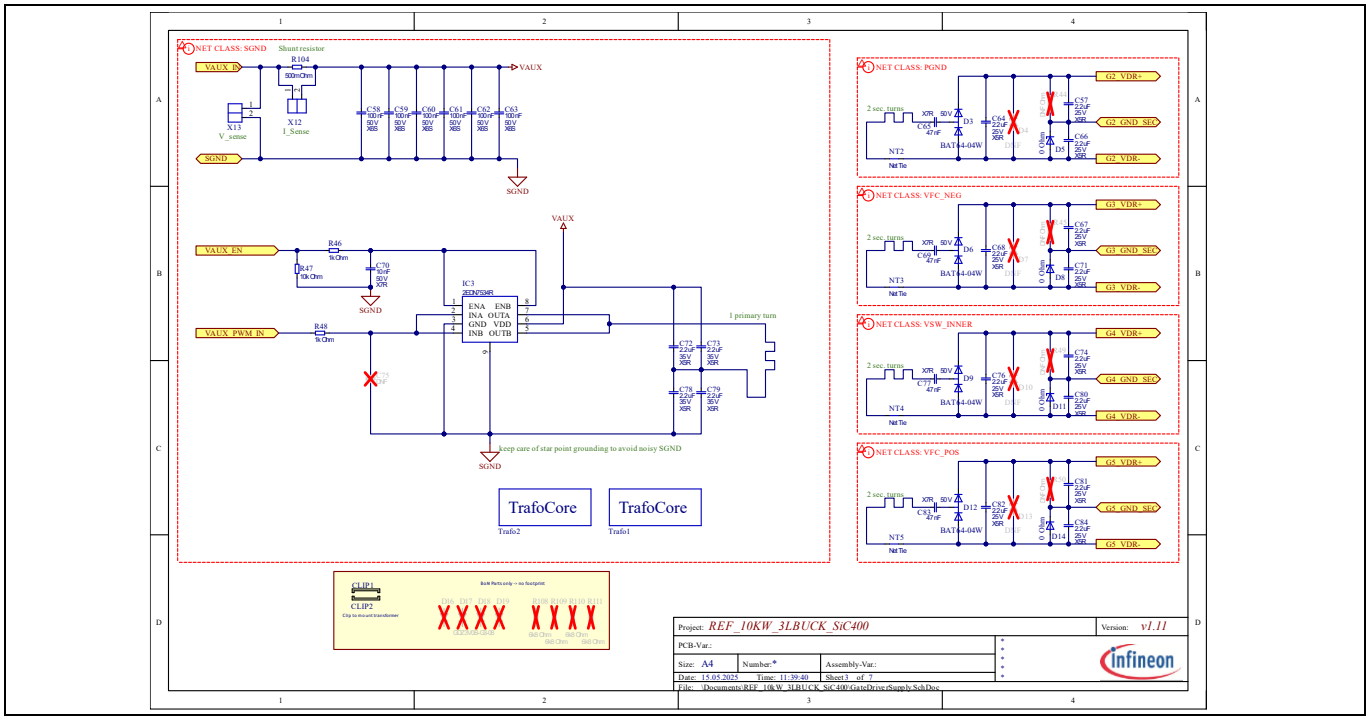


Figure 19 Schematics of gate driver auxiliary power supply

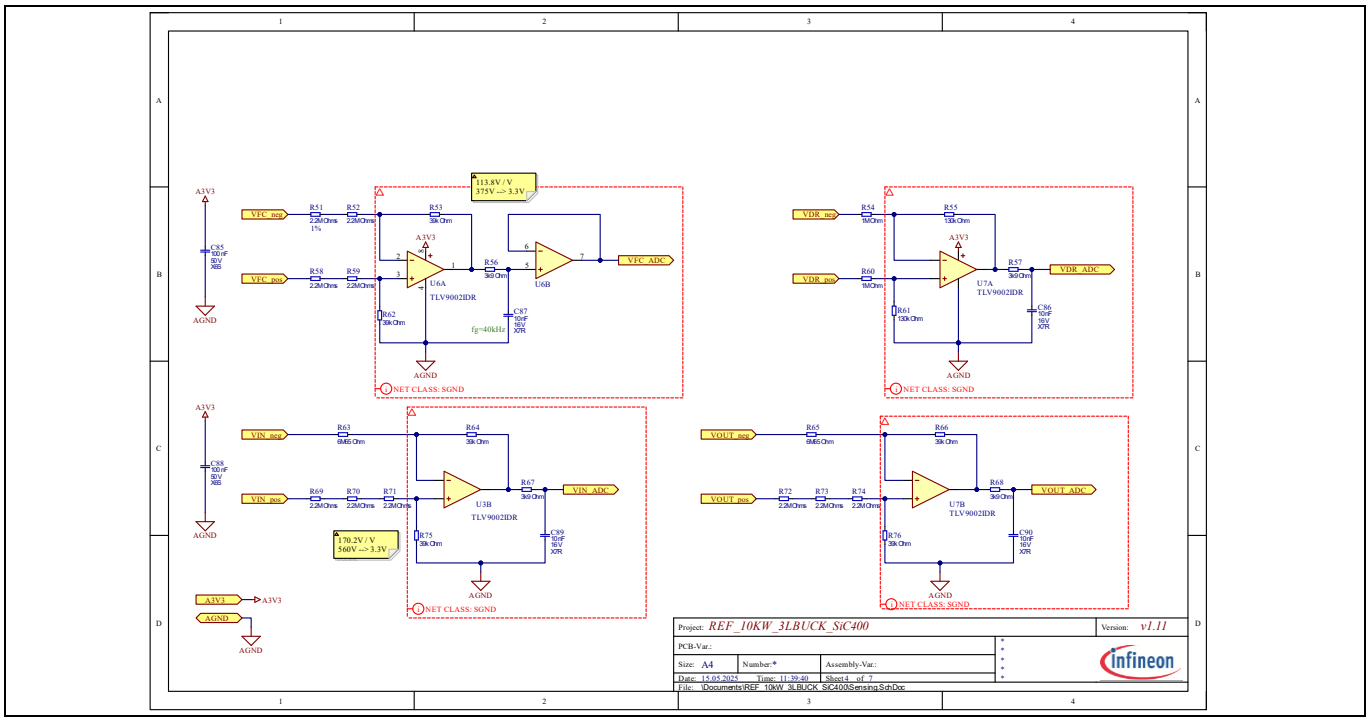


Figure 20 Schematics of the sensing circuitry

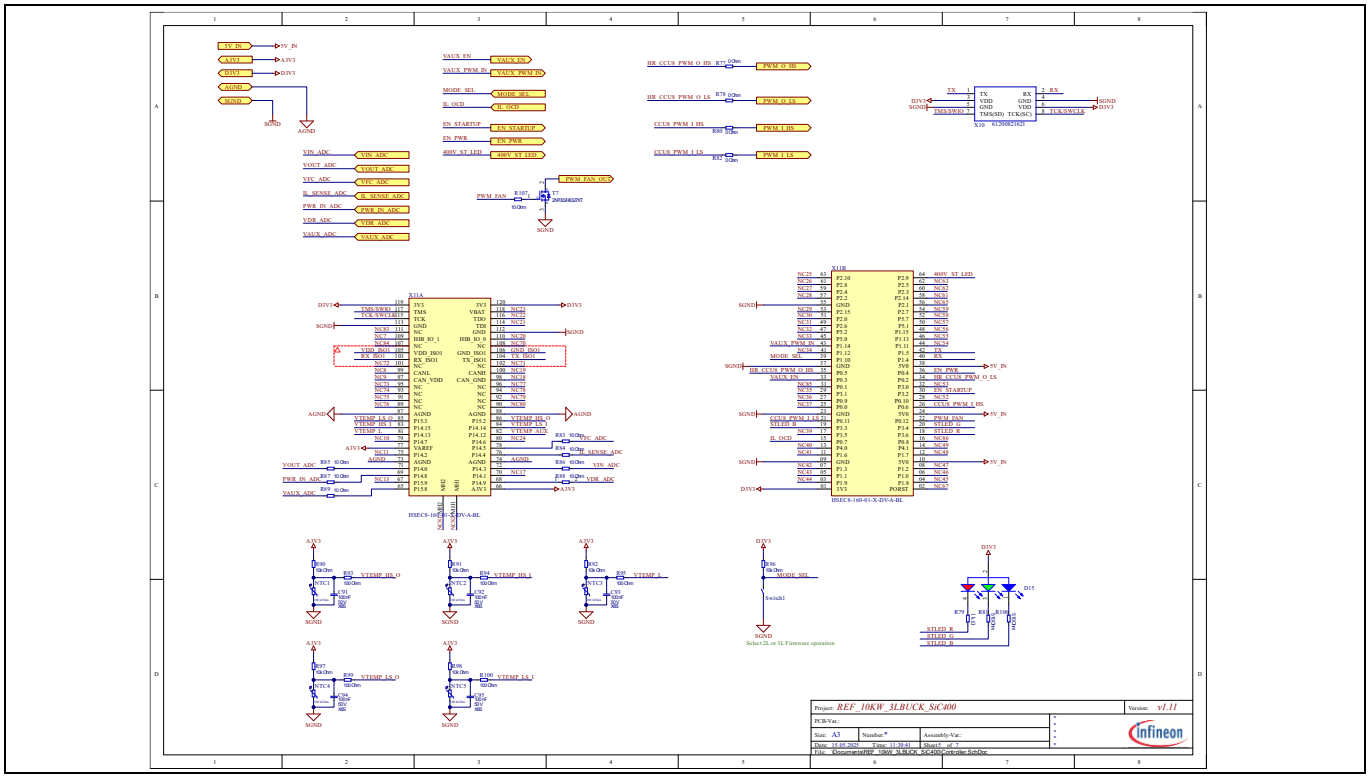


Figure 21 Schematics of the interface to the controller card

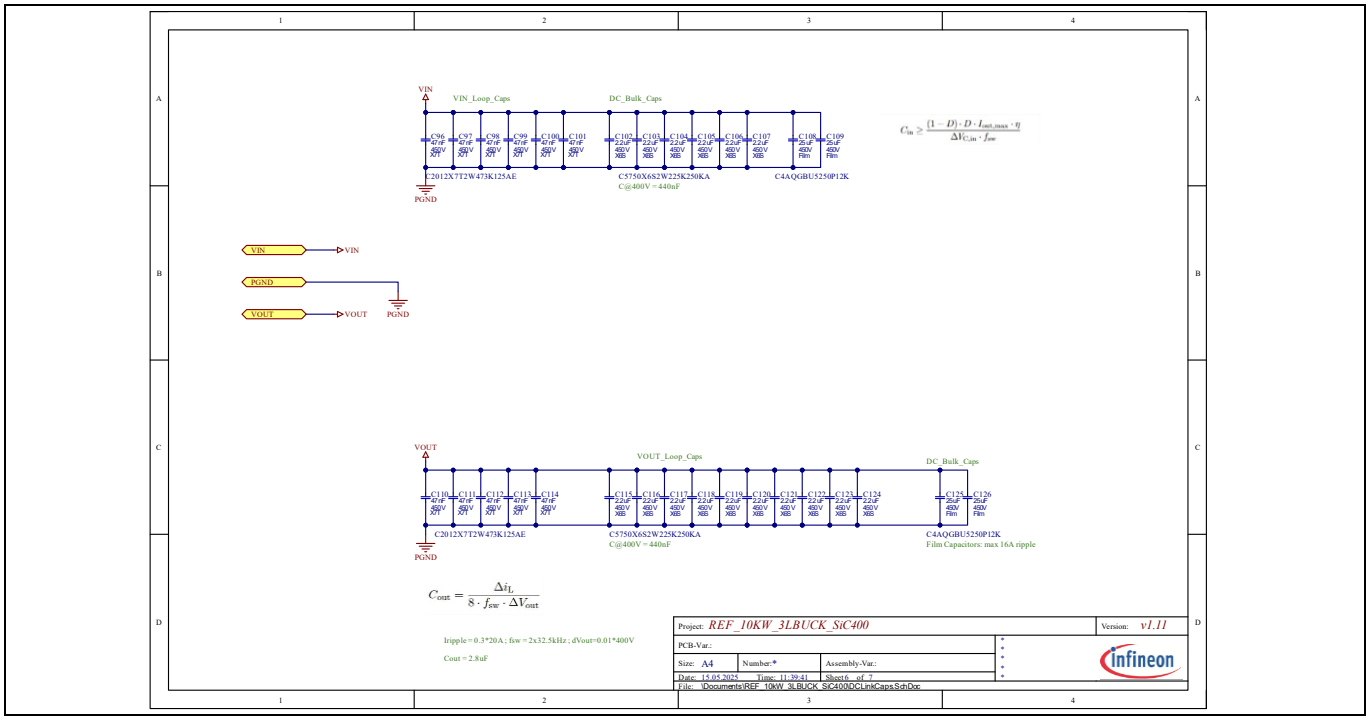


Figure 22 Schematics of the input and output capacitor bank

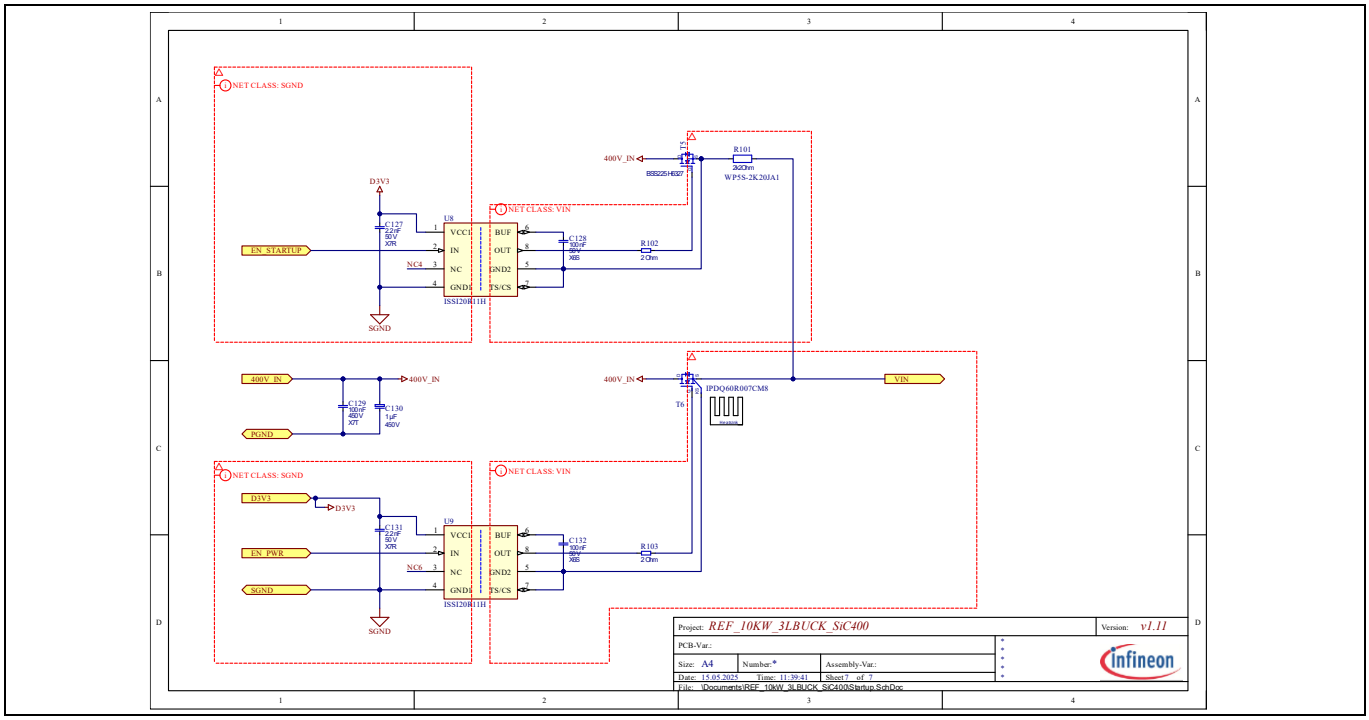


Figure 23 Schematics of the start-up circuit

3.2 Layout

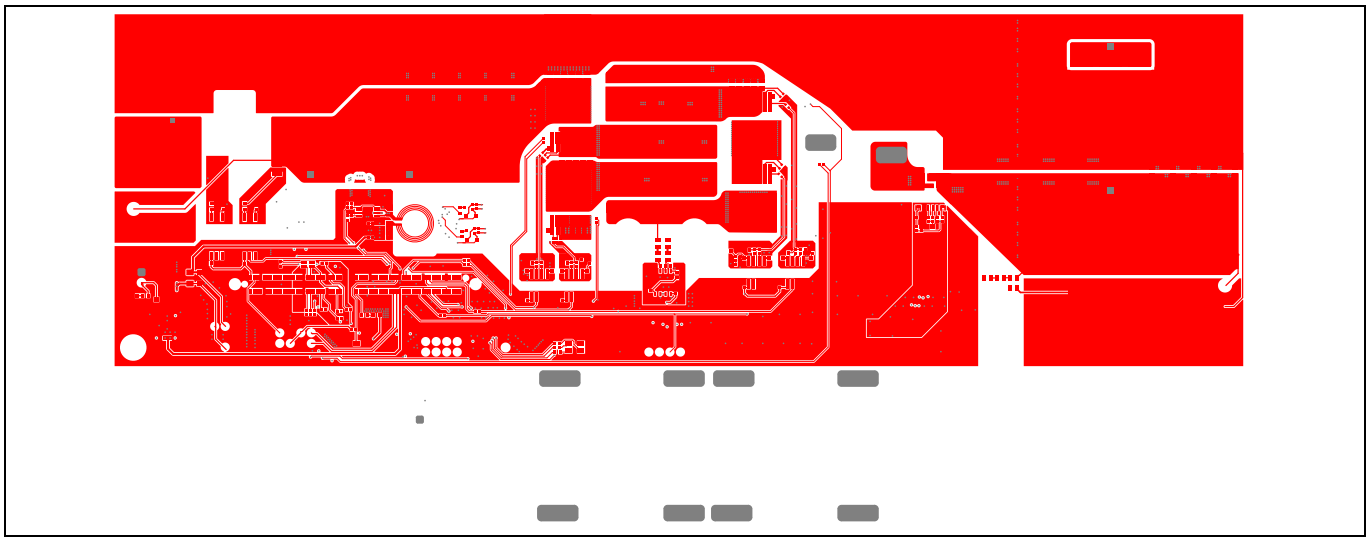


Figure 24 PCB layer 1 (TOP)

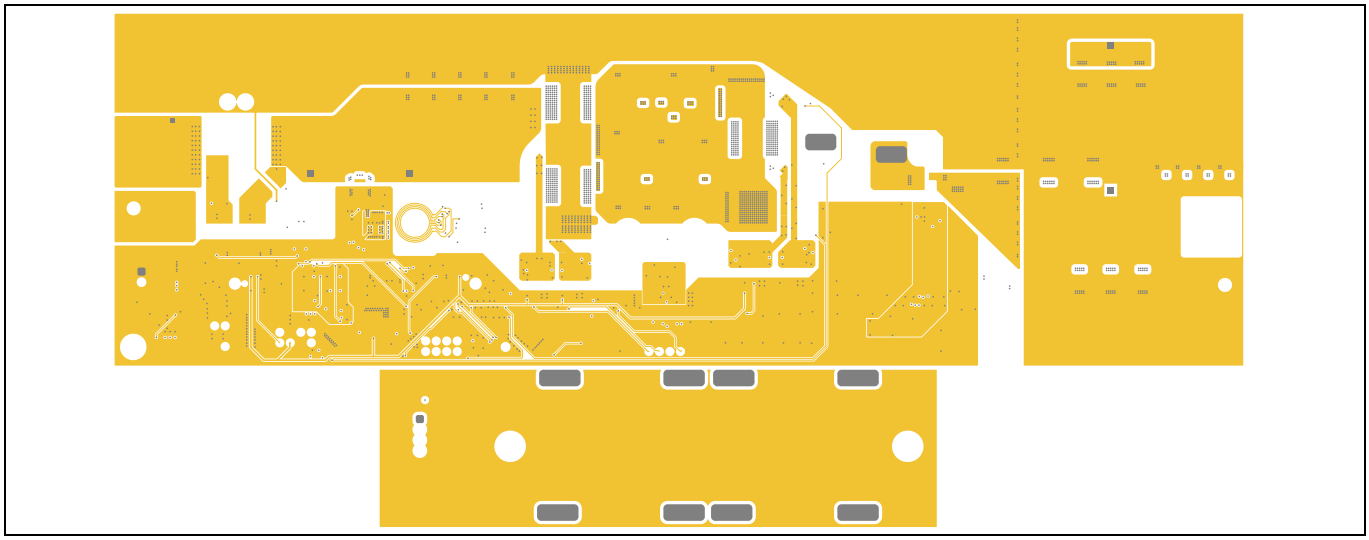


Figure 25 PCB layer 2 (inner)

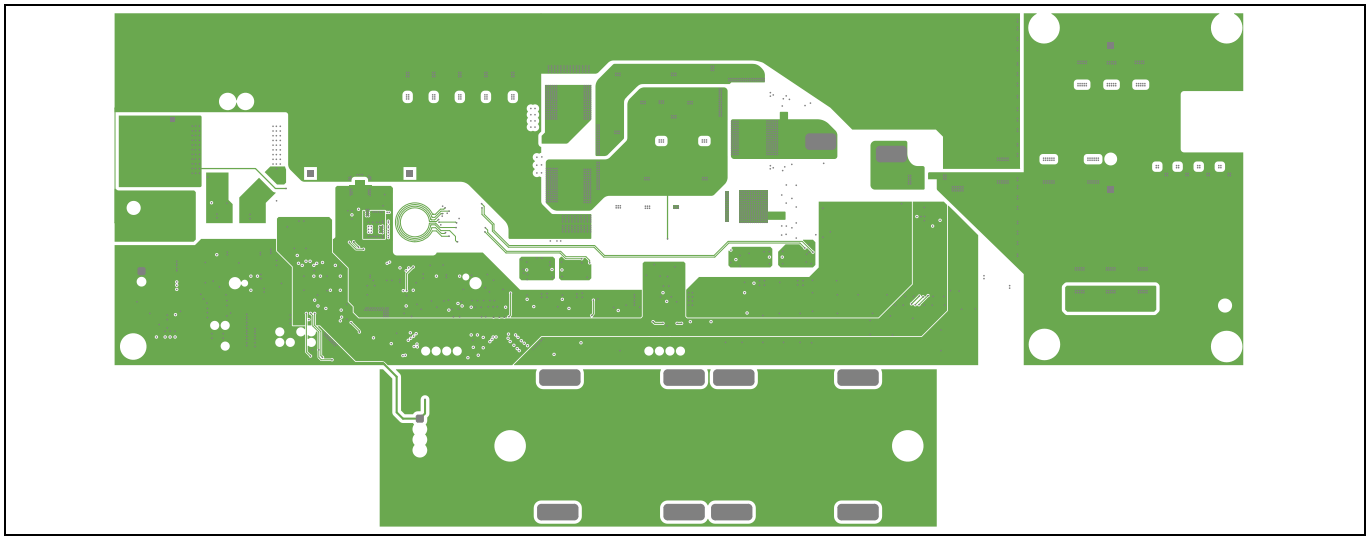


Figure 26 PCB layer 3 (inner)

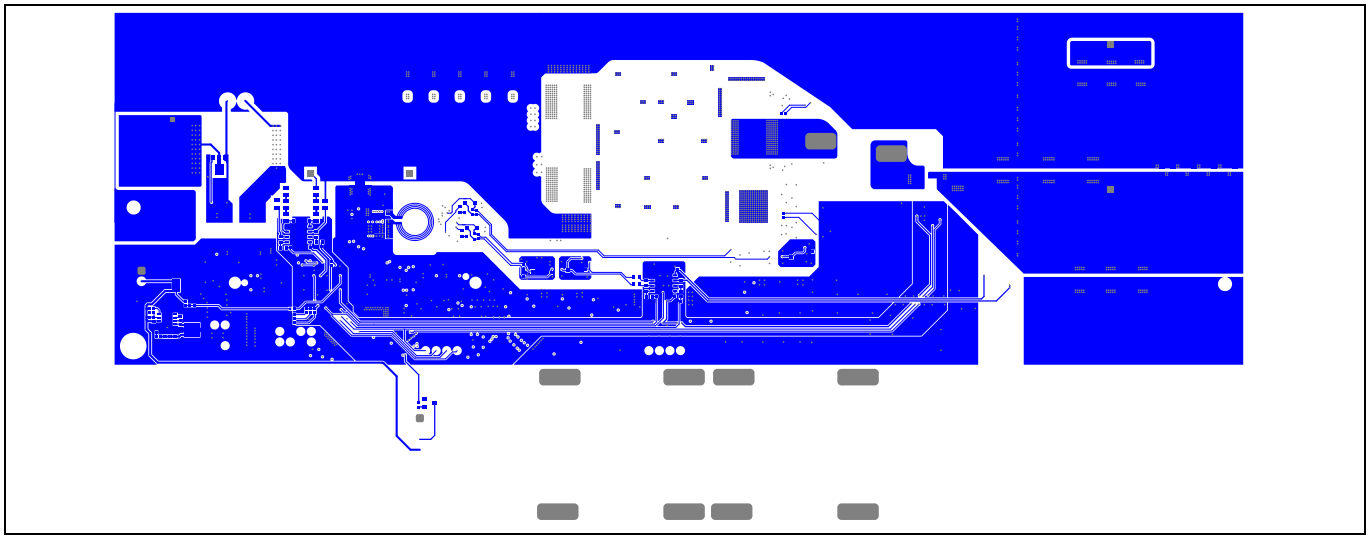


Figure 27 PCB layer 4 (BOT)

Board Stack Report

Stack Up		Layer Stack			
Layer	Board Layer Stack	Name	Material	Thickness	Constant
1		Top Paste			
2		Top Overlay			
3		Top Solder	Solder Resist	0.010mm	3.5
4		Top Layer	Copper	0.070mm	
5		Dielectric 1	FR4	0.150mm	4.2
6		Mid-Layer 1	Copper	0.070mm	
7		Dielectric 3	FR4	1.000mm	4.2
8		Mid-Layer 2	Copper	0.070mm	
9		Dielectric 2	FR4	0.150mm	4.2
10		Bottom Layer	Copper	0.070mm	
11		Bottom Solder	Solder Resist	0.010mm	3.5
12		Bottom Overlay			
13		Bottom Paste			
	Height : 1.600mm				

Note: Plugged vias of type VII (plug with nonconductive paste + capped vias) are used.

Figure 28 Layer stack-up of the four-layer PCB

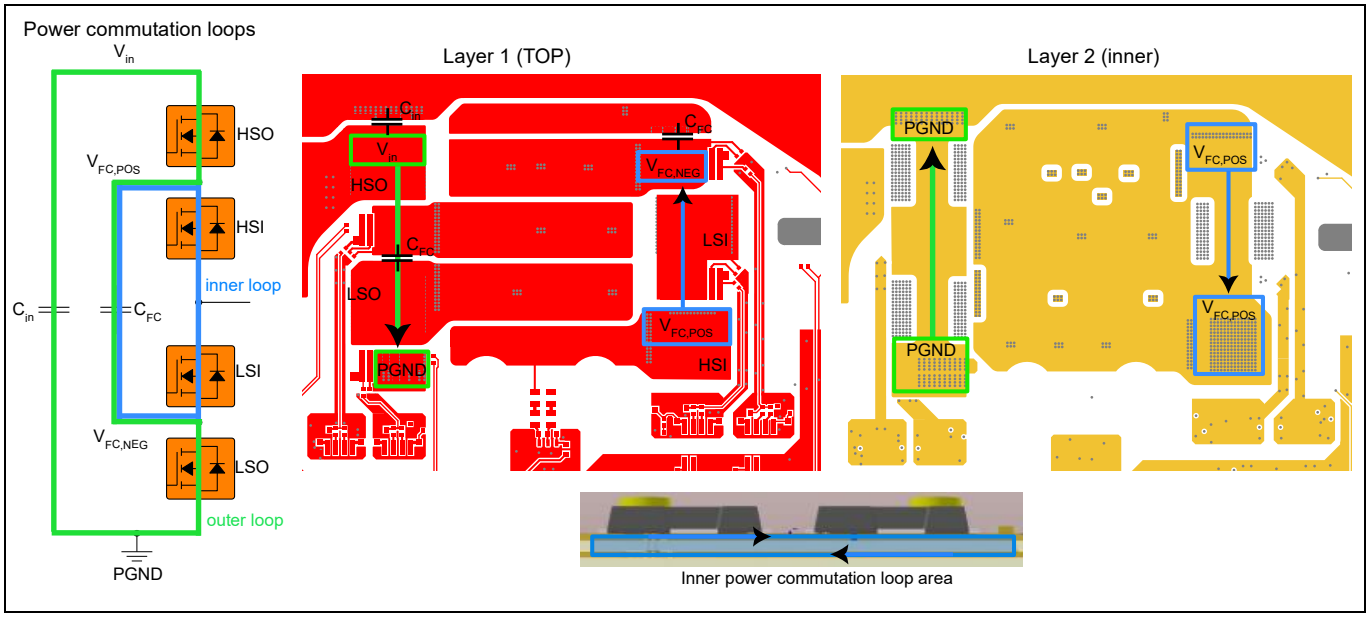


Figure 29 Optimization of commutation loops using an “I” layout

The previous figure shows the inner and outer leg commutation loops in the 3L-FC-buck. The “I” layout with a return-path directly in layer 2 (inner), underneath the half-bridge minimizes the commutation loop inductance with field-cancellation. The thermal vias have been placed towards the sides of the footprints to facilitate a tighter commutation loop at the expense of having slightly higher thermal resistance through the PCB ($R_{th,pcb}$). In early prototyping, the effect of such a higher $R_{th,pcb}$ compared to using an uninterrupted grid of thermal vias was negligible, leading to the decision to adopt this design.

3.3 Bill of material for key components of REF_10KW_3LBUCK_SIC400

The complete bill of material is available on the reference board webpage.

Table 5 BOM of the most important/critical parts of REF_10KW_3LBUCK_SIC400

Sl. No.	Ref Designator	Description	Manufacturer	Manufacturer P/N	Populated
1	T1, T2, T3, T4	CoolSiC™ MOSFET 400 V G2 CoolSiC™ MOSFET 650 V G2	Infineon	IMT40R011M2H IMT65R010M2H	Yes No
2	U1, U2, U3, U4	EiceDRIVER™ 6.5 A, 3 kV (rms) 1-ch. isolated gate driver w. separate o/p	Infineon	1ED3141MU12F	Yes
3	U8, U9	EiceDRIVER™ Coreless-transformer solid-state isolator	Infineon	ISSI20R11	Yes
4	T6	600 V CoolMOS™ 8 SJ MOSFET	Infineon	IPDQ60R007CM8	Yes
5	IC3	EiceDRIVER™ Fast dual-channel 5 A gate driver	Infineon	2EDN7534R	Yes
6	IC2	XENSIV™ - TLI4971-A050T5-E0001 high precision coreless current sensor	Infineon	TLI4971 A050	Yes
7	C41, C42, C43, C44, C45, C46, C47, C48, C49, C50, C51, C52, C53, C54, C55, C56	Flying capacitors. Stacked MLCCs, 2220 450 V 2.2 uF X7T 20% T: 5 mm	TDK	CKG57NX7T2W225M500JH	Yes
8	L3	Inductors	Würth Elektronik	760801122 760801102	Yes No
9	TIM	Thermal interface material	BANDO	HEATEX TS 103 T=1.0 mm	Yes

4 System performance

4.1 3L-FC Buck mode

4.1.1 Efficiency and thermal measurement

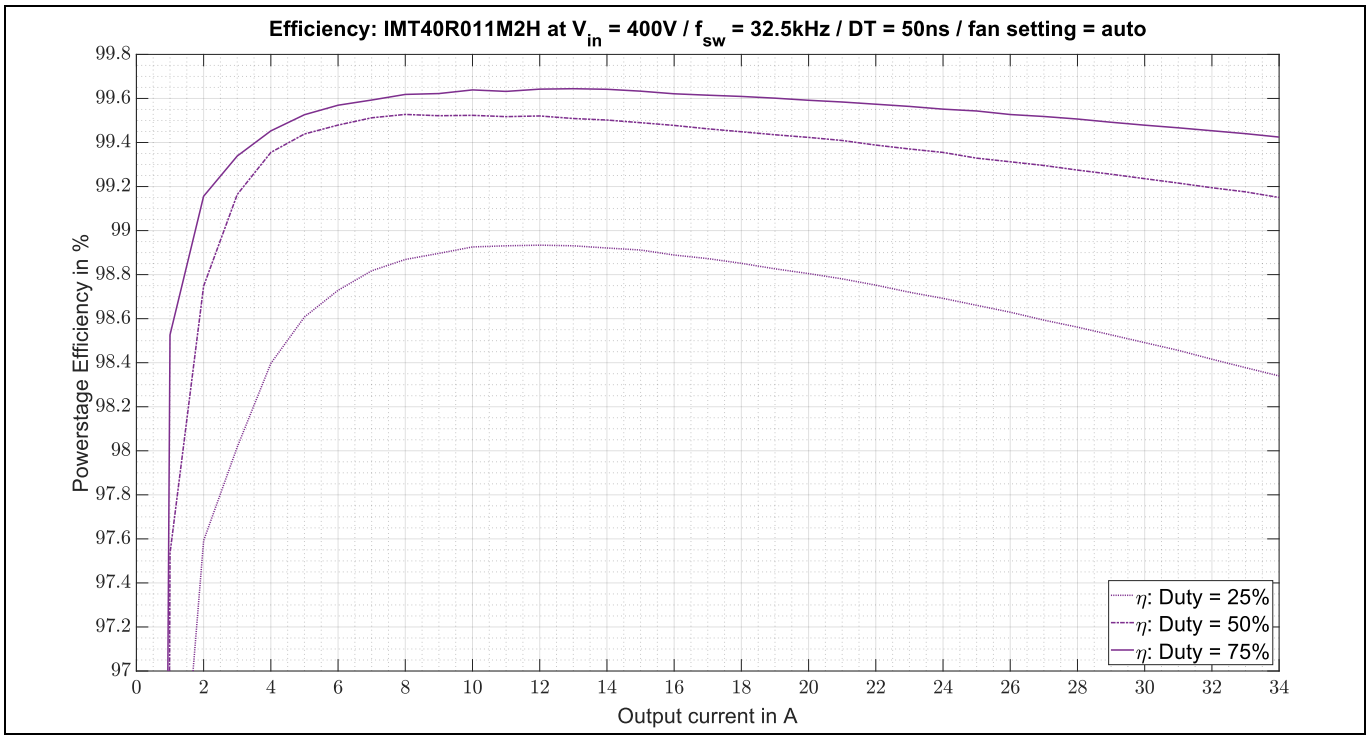


Figure 30 Efficiency measurements in 3L-FC-Buck mode for various duty-cycles

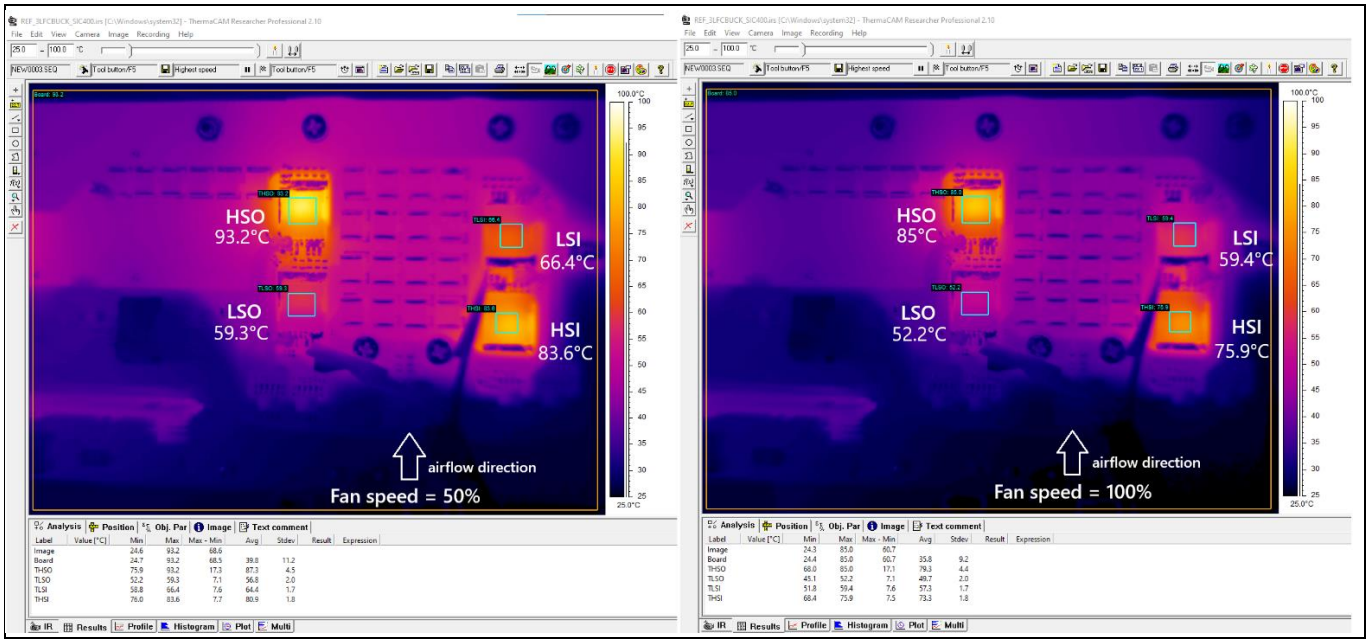


Figure 31 Thermal steady state measurements in 3L-FC-Buck mode at D = 0.75 and IOUT = 34 A

4.1.2 Waveform measurement

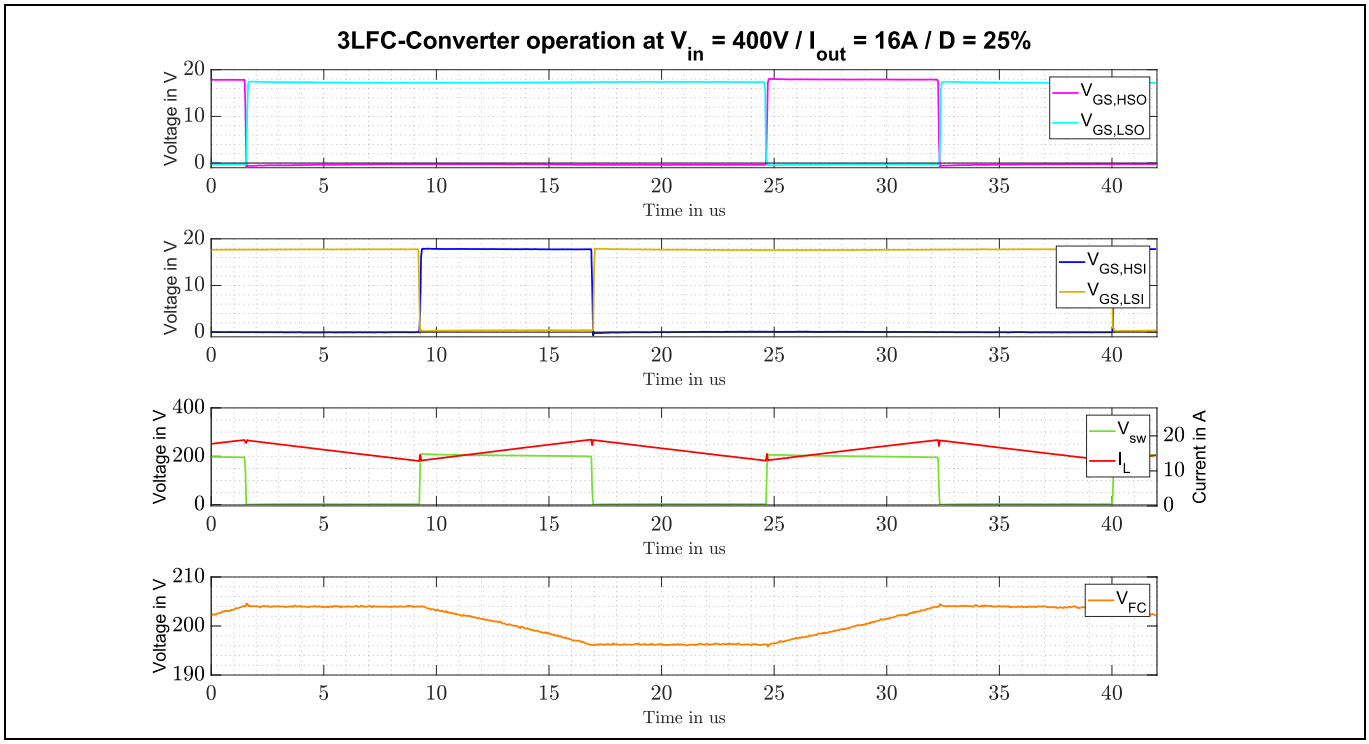


Figure 32 Switching waveforms at D = 0.25

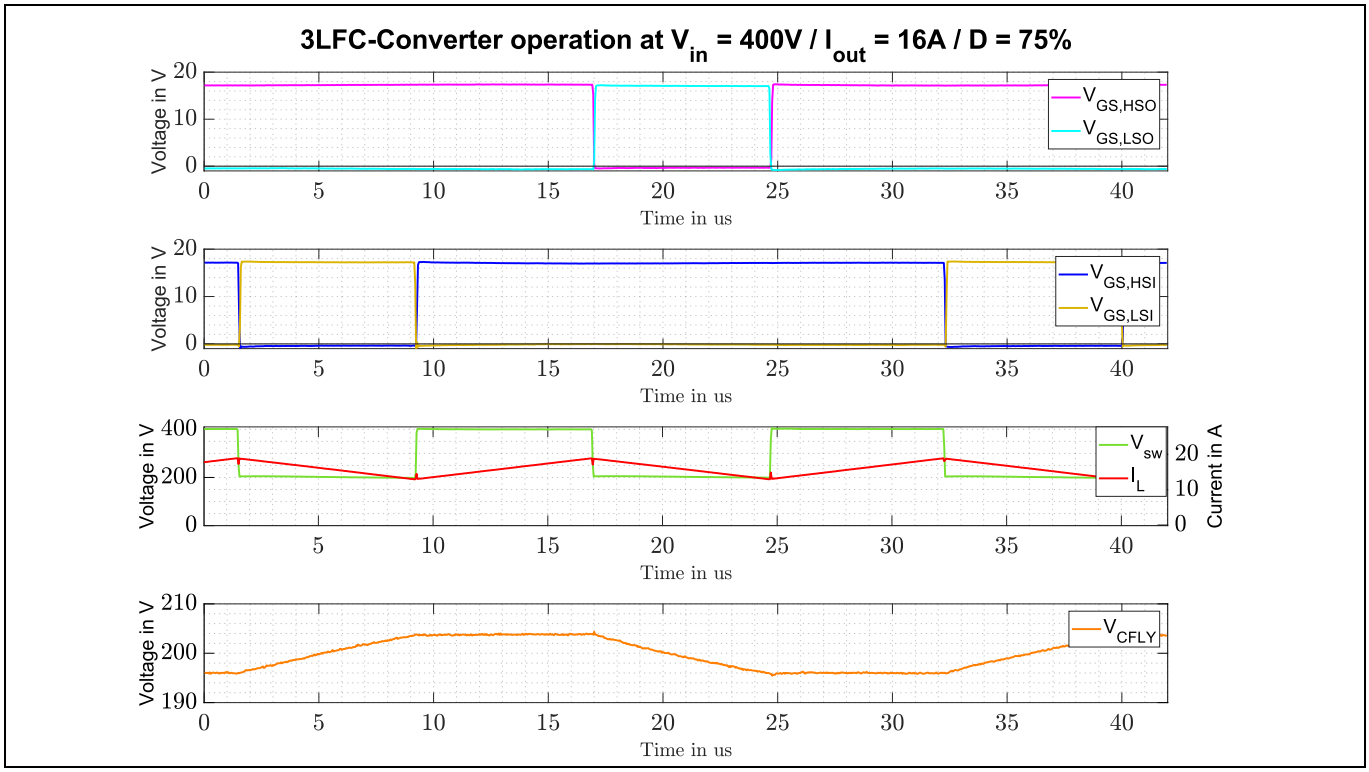


Figure 33 Switching waveforms at D = 0.75

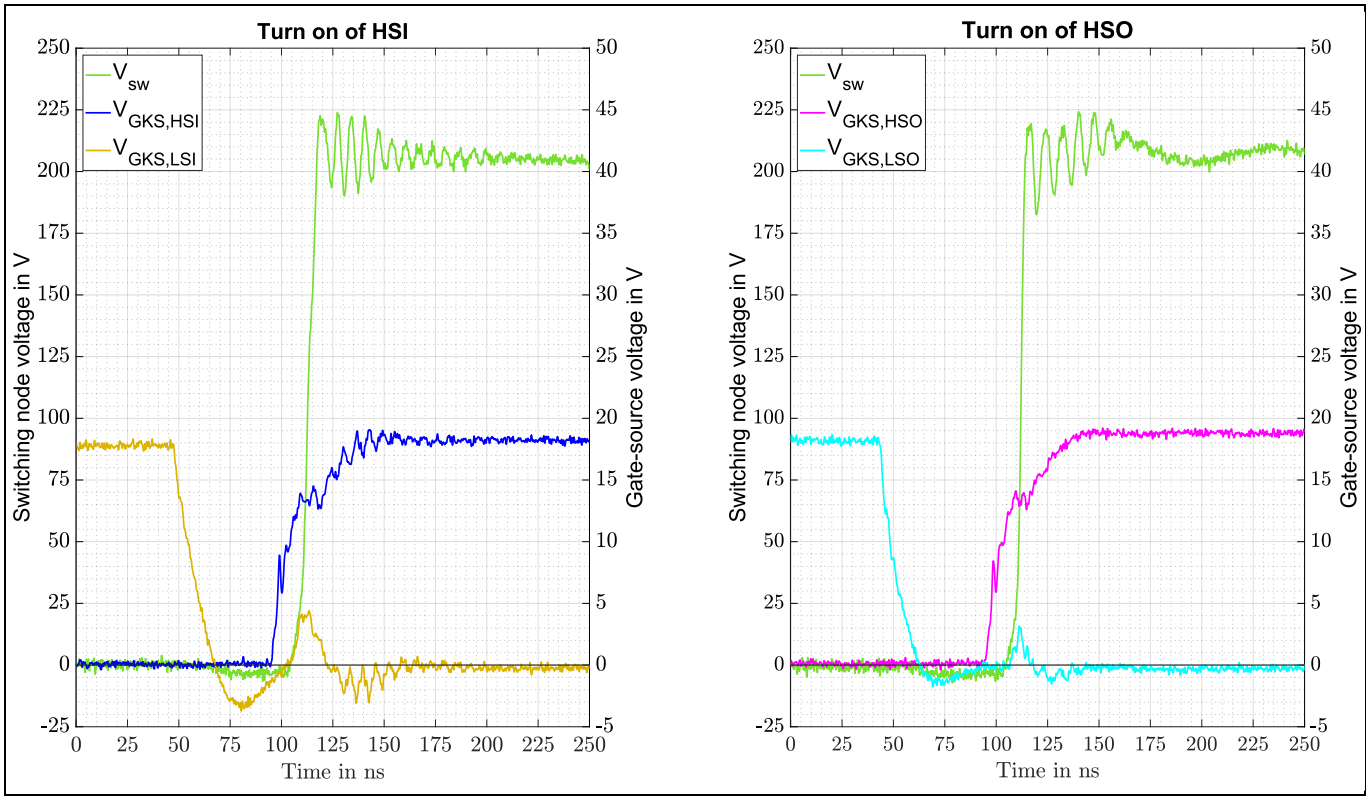


Figure 34 **Switching waveforms at D = 0.25 and IOUT = 20 A showing switching behavior**

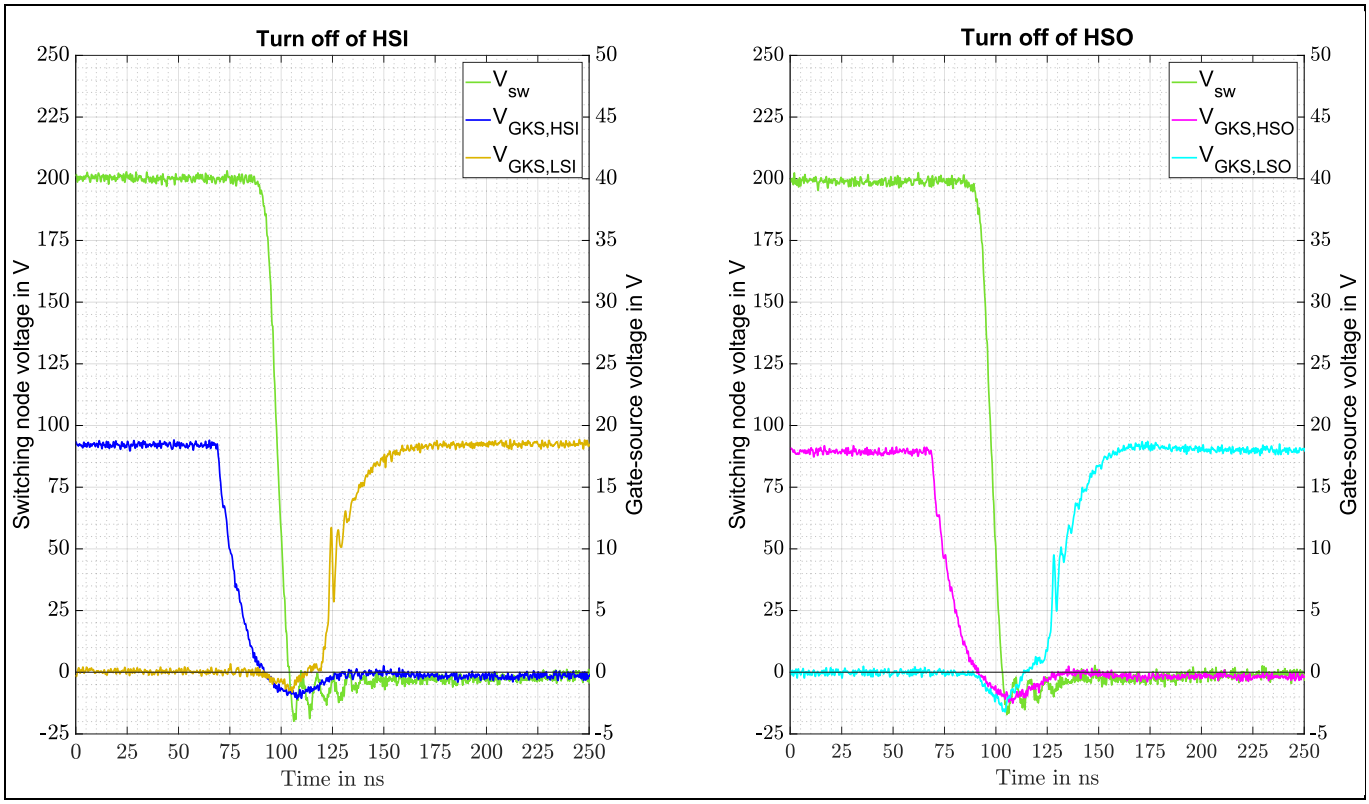


Figure 35 **Switching waveforms at D = 0.25 and IOUT = 20 A showing switching behavior**

4.1.3 Flying capacitor voltage balancing under load and line transients

The flying capacitor voltage balancing was validated at transients in output voltage and load conditions. **Figure 36** shows the key waveforms for a step change in duty-cycle (D = 0.25 to 0.75) to emulate a step change in output voltage for a given load current (I_{OUT} = 10 A). The rate of change in the duty cycle is limited by firmware to achieve a smooth $\Delta V_{OUT}/\Delta t$ = 0.4 V/ms. This is not only done to ensure FC balancing, but also to prevent a large transient volt-second product from being applied to the choke due to a sudden step-change in duty-cycle, which could cause core saturation and lead to larger inductor transient currents.

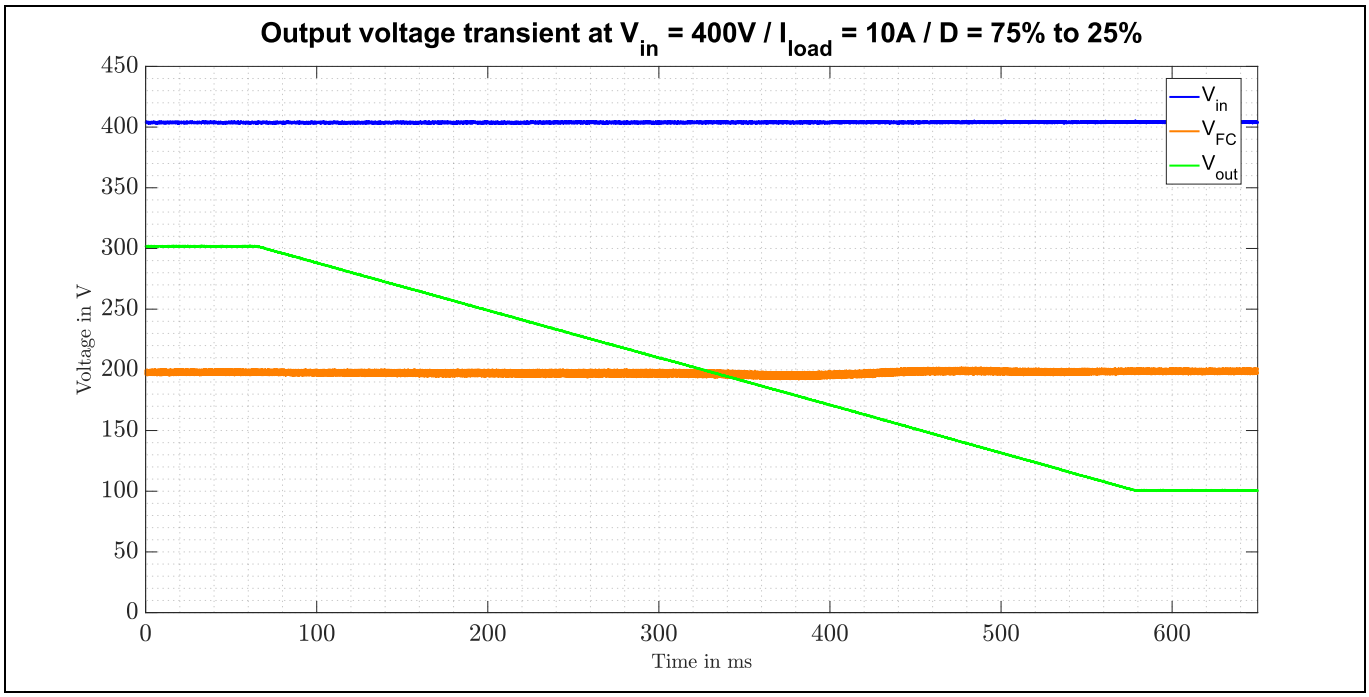


Figure 36 Output voltage transient measurement

4.2 2L Buck mode

4.2.1 Efficiency and thermal measurement

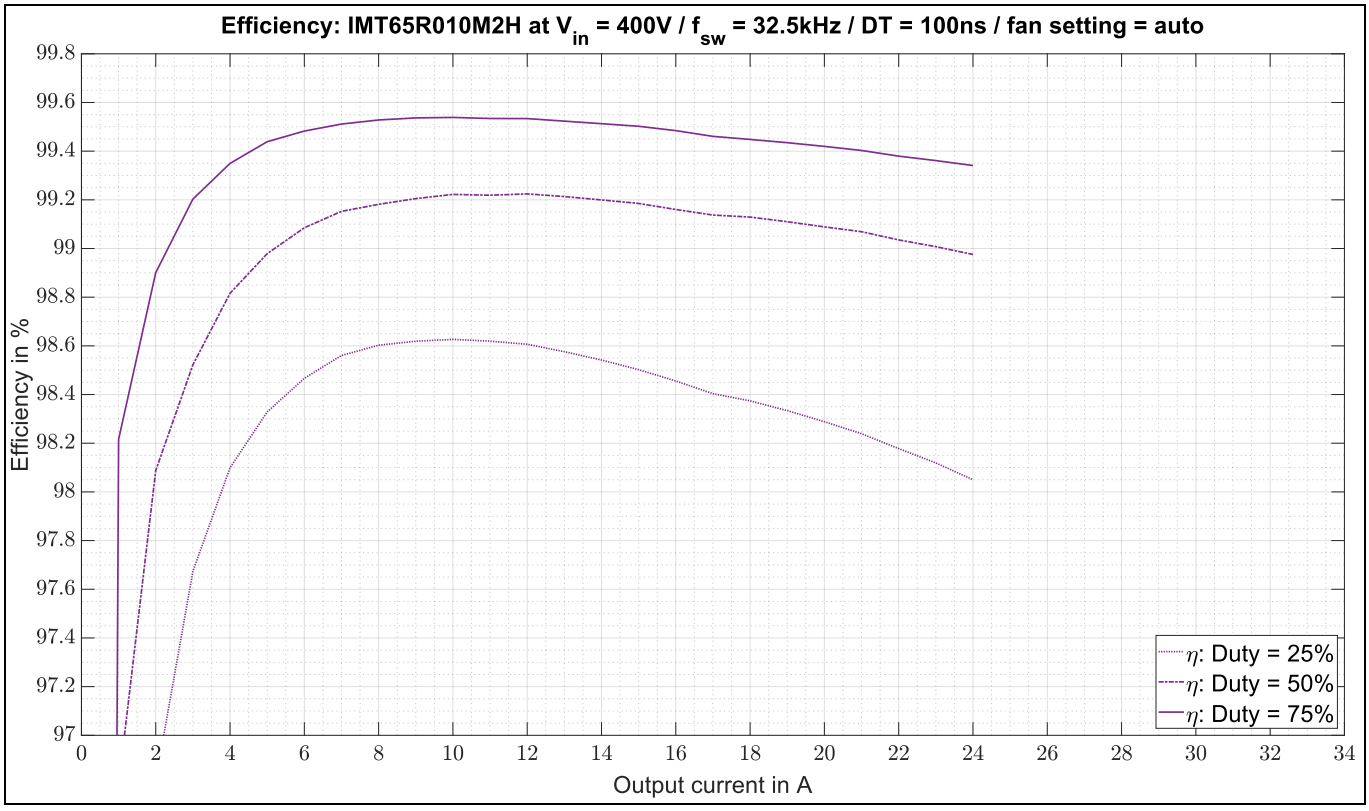


Figure 37 Efficiency measurements in 2L-Buck mode for various duty-cycles

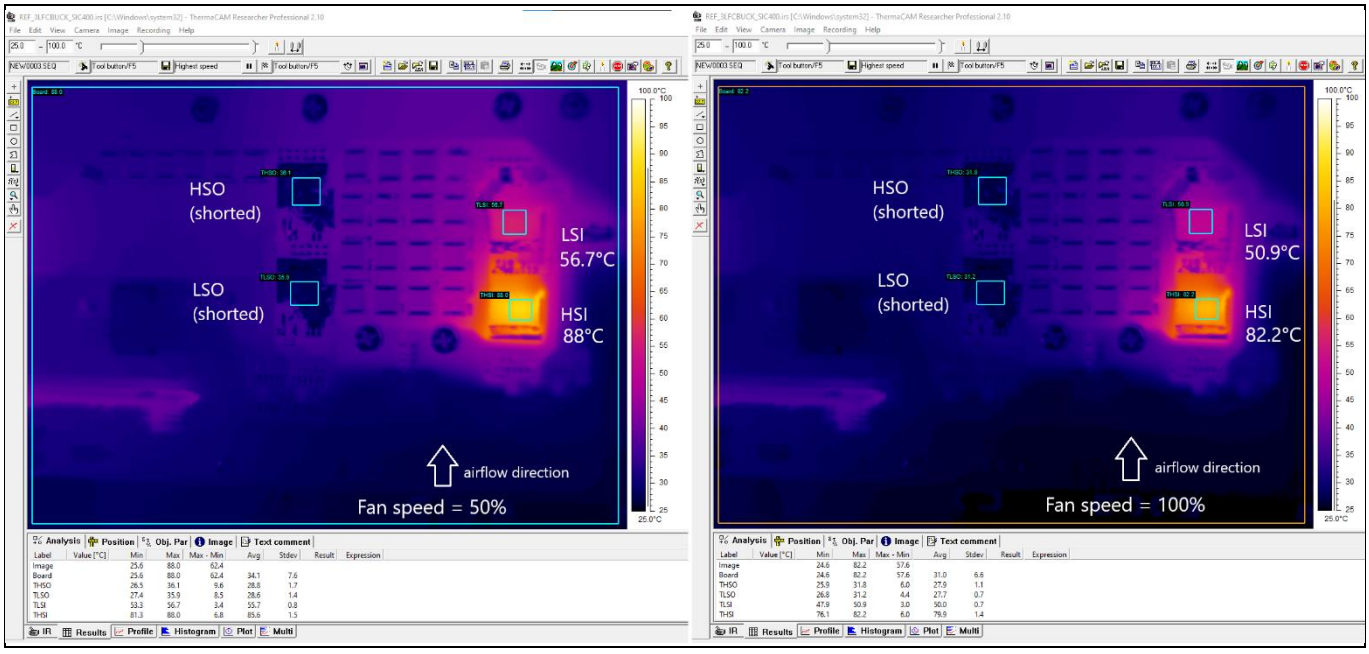


Figure 38 Thermal steady state measurements in 2L-Buck mode at D = 0.75 and IOUT = 24 A

4.2.2 Waveform measurement

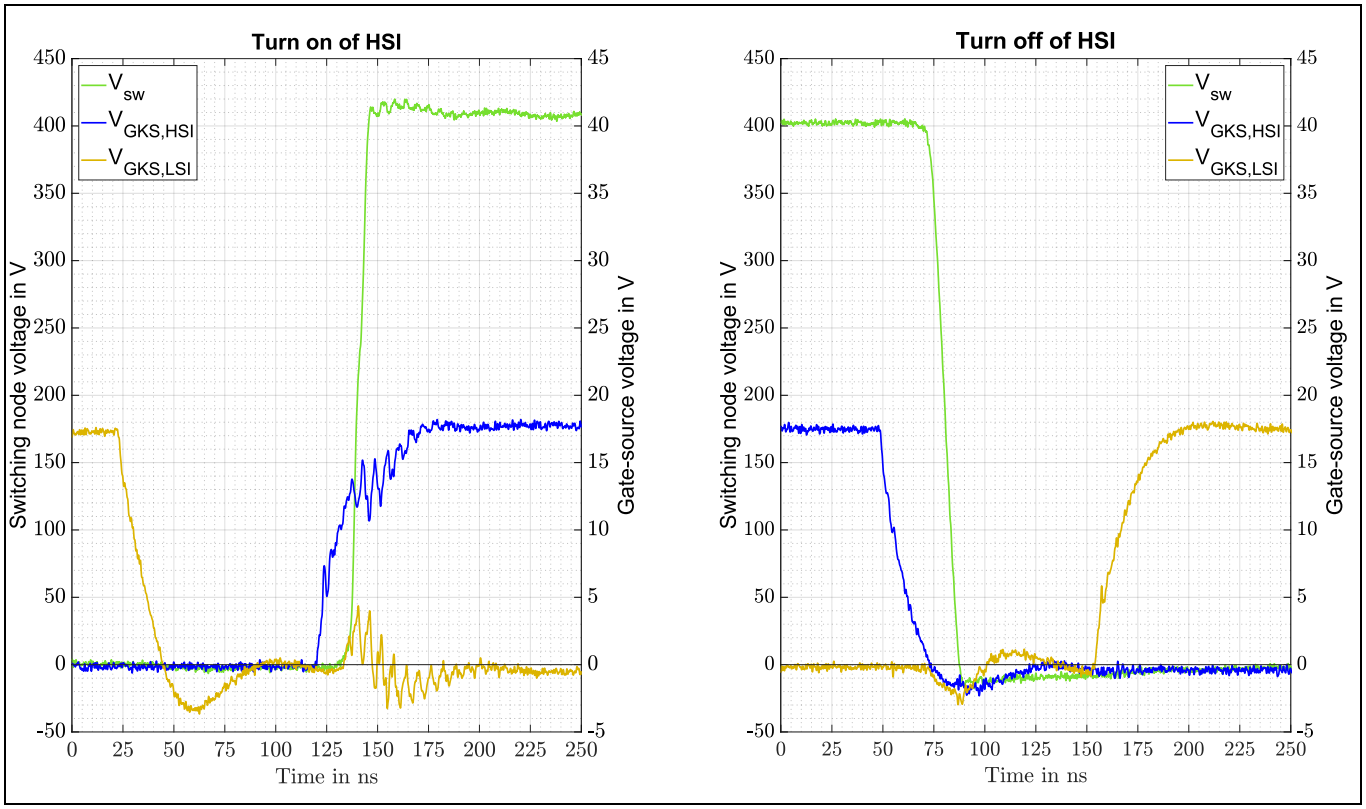


Figure 39 Switching waveforms at D = 0.25 and IOUT = 24 A showing switching behavior

4.3 Comparison: 3L vs. 2L mode

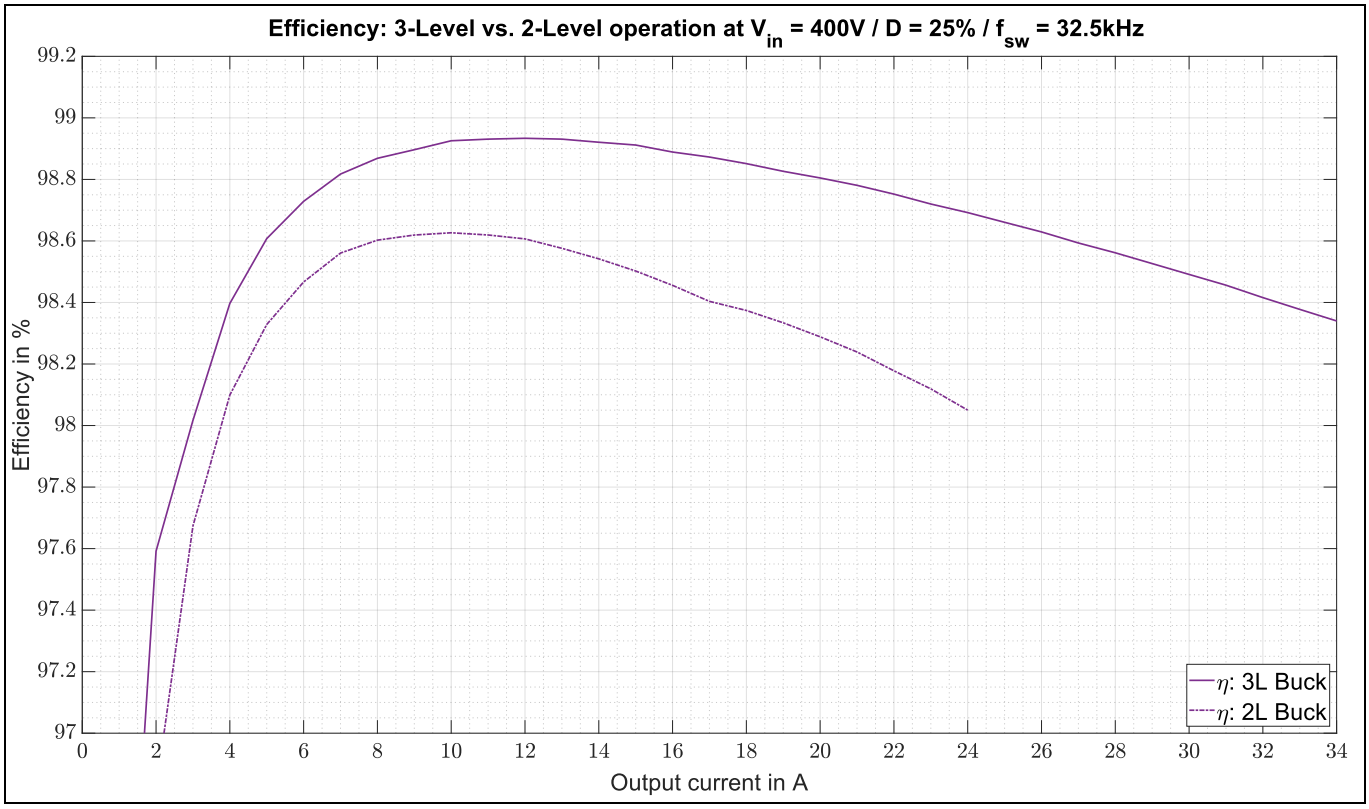


Figure 40 Comparison of efficiency curves between 2-level and 3-level operation

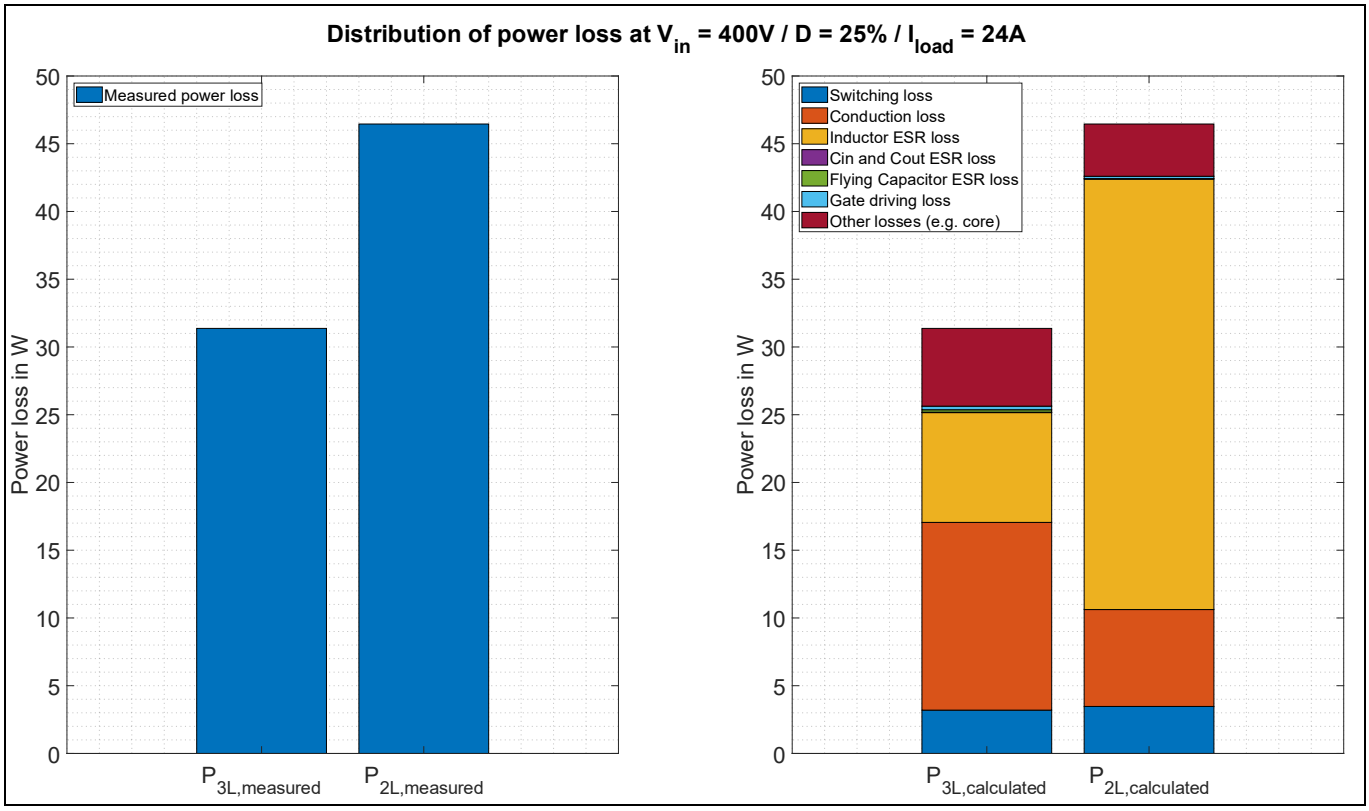


Figure 41 Power loss breakdown for 3-level and 2-level operation with f_{sw} = 32.5 kHz

References

[1] Maximilian Huber. Master Thesis “Evaluation of 400V SiC-MOSFETs in a 3-Level Flying Capacitor DC/DC Converter”; Graz; TU Graz; October 2024; Available online

[2] TDK Corporation. Solder Crack Countermeasures in MLCC Solution Guide; Available online

[3] Infineon Technologies AG. REF_10KW_3LBUCK_SIC400 reference board; Available online

Revision history

Document revision	Date	Description of changes
V 1.0	2025-06-02	Initial release

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