EZ-PD™ PAG1S-1P based 100 W single-stage power factor correction (PFC) USB PD dual-C charger and adapter solution (REF_100W_2C_SSFB_PAG1) user guide

About this document

Scope and purpose

This document provides instructions and a quick start guide for EZ-PD™ PAG1S-1P controller-based dual-C charger and adapter solution (REF_100W_2C_SSFB_PAG1).

Intended audience

This document is primarily intended for EZ-PD™ PAG1S-1P multiport charger and adapter solution developers.

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1 Introduction

As portable electronic devices such as smartphones, tablets, and laptops require faster charging, the Power Delivery (PD) technology is designed to provide the fastest charging possible through a USB Type-C (USB-C) cable. The USB PD Standard Power Range (SPR) standard defines the maximum power to deliver over a USB-C cable up to 100 W. This allows for providing multiple USB-C ports (Figure 1) on universal AC-DC adapters that can charge a wide range of devices such as smartphones, gaming laptops, power tools, and e-bikes.

However, these new requirements for higher power and multi-port have challenges for the converter topologies used till now. Considering a few factors such as electromagnetic compatibility, power factor correction, standby power, and average efficiency ensures that the chargers and adapters are effective and efficient. The size (power density), load sharing, and scaling up multiple ports became critical factors for design engineers and end-users. The power efficiency of USB-C chargers and adapters is a crucial in determining their power density. Therefore, converter topology, usage model, integration, and flexibility of controller functionalities are all key factors to consider when selecting the right adapter architecture for the needs.

Figure 1 shows a typical block diagram of a multi-port adapter. The front-end AC-DC converter produces the requested output voltage while ensuring PFC at the front end for up to 100 W of power. On the other hand, the buck converter (connected at the output of the AC-DC converter) ensures that the defined USB-C PD specifications and performance are achieved for multi-port adapter applications.
Figure 1 shows a high-level block diagram of the EZ-PD™ PAG1P-PAG1S-CCG7DC-based adapter and charger solution.

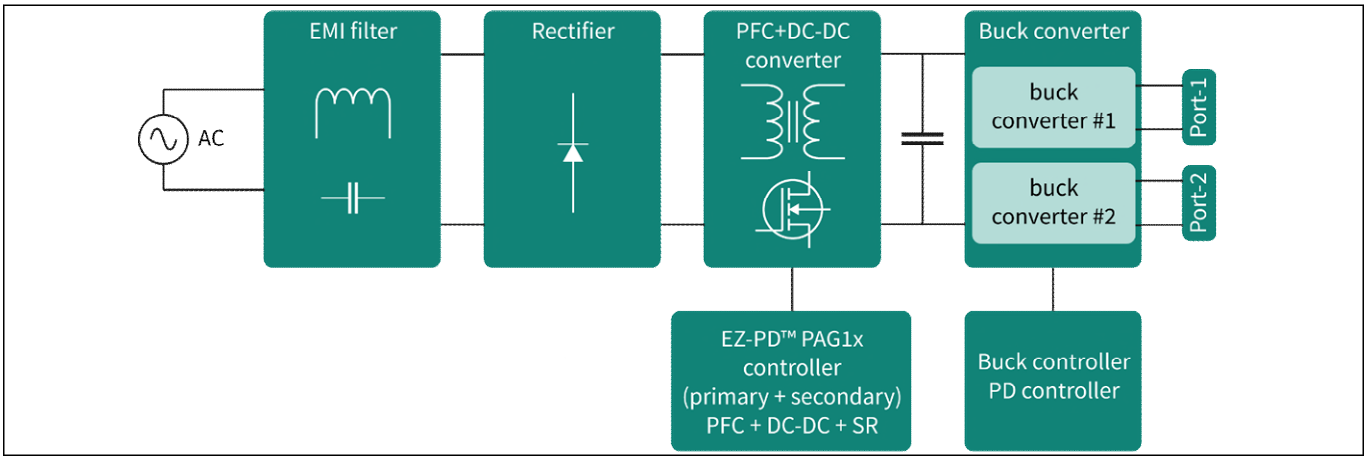

Figure 1 High-level block diagram of a dual-port adapter

Infineon provides a comprehensive solution for both sections of adapters, i.e., AC-DC and buck converters. Specifically, for AC-DC conversion, Infineon's EZ-PD™ PAG1x-based solution offers a single-stage PFC design, along with the EZ-PD™ CCG7DC-based buck converter, ensuring compatibility with USB PD/Programmable Power Supply (PPS) standards. The EZ-PD™ CCG7DC supports a dual PD/PPS port, capable of controlling two buck controllers with integrated drivers, which makes it an ideal choice for dual or multiports (multiples of 2) applications.

Table 1 Critical components bill of materials (BOM)

Designator	Description	Part number	Manufacturer
U1	EZ-PD™ PAG1P primary side startup controller	CYPAP112A3-10SXQ	Infineon Technologies
U2	EZ-PD™ PAG1S USB PD power adapter secondary side controller	CYPAS111A1-24LQXQ	Infineon Technologies
U6	EZ-PD™ CCG7DC dual-port USB Type-C with PD and buck-boost controller	CYPD7271-68LQXQES	Infineon Technologies
Q1	MOSFET N-CH 800 V 17 A TO220-3F	IPA80R280P7XKSA1	Infineon Technologies
Q3	MOSFET N-CH 150 V 56 A 8TDSON for SR	BSC160N15NS5ATMA1	Infineon Technologies
U4, U5	MOSFET array 2 N-channel (half bridge)	IAUC45N04S6N070H	Infineon Technologies
Q4, Q5	MOSFET N-CH 40 V 40 A 8TSDSON	IPZ40N04S53R1ATMA1	Infineon Technologies
T1	150 uH RM10 power transformer	–	–
T2	Pulse edge transformer	CYPET131	Infineon Technologies
C7, C8, C9, C12, C13, C14	CAP ALUM POLY 1200 UF 20% 25 V	A750MW128M1EAAE014	KEMET
L2, L3	4.7 µH shielded drum core	78439369047	Würth Elektronik

2 Specification

Table 2 Test specifications

Parameter	Value
Input voltage and frequency	100 to 240 V AC, 47 to 63 Hz
ATHD	<10% at 230 V AC and 100 W
Max output power	100 W system power with dual-C and a max load current of 5.0 A 100 W on each port with a max load current of 5.0 A
Output voltage	Fixed PDOs: 5.0 V / 5.0 A, 9.0 V / 5.0 A, 15.0 V / 5.0 A, 20.0 V / 5.0 A PPS: 3.3 V to 11.0 V, 5.0 A; 3.3 V to 16.0 V, 5.0 A; 3.3 V to 21.0 V, 5.0 A with PPS power limit
Peak efficiency	> 88%
Protections	1. Input overvoltage protection 2. Input undervoltage protection 3. V_{BUS_C} overvoltage protection (OVP) 4. V_{BUS_C} undervoltage protection (UVP) 5. Overcurrent protection (OCP) 6. Short-circuit protection (SCP) 7. Over-temperature protection (OTP) 8. VBUS_C to CC short protection
Charging standards supported	1. USB-C PD v3.1 including programmable power supply (PPS) mode 2. Apple Charging 2.4 A 3. Qualcomm QC 2.0, 3.0, 4.0, 5.0 4. Samsung AFC 5. USB BC 1.2
EMI/EMC	1. CE, CISPR32 CLASS B 2. ESD, IEC61000-4-2 3. Surge, IEC61000-4-5 4. Harmonics, IEC61000-3-2

3 Board overview

The EZ-PD™ PAG1S-1P-based 100 W single-stage PFC USB PD dual-C charger and adapter solution (REF_100W_2C_SSFB_PAG1) shown in Figure 2 solution board is designed to meet the specifications shown in Table 2. Baseboard with dual-C operates up to 100 W and each port operates up to 100 W.

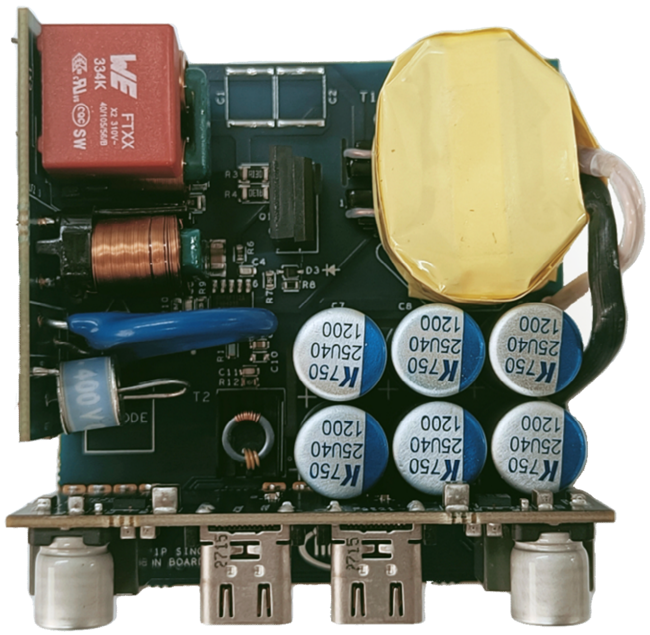

Figure 2 REF_100W_2C_SSFB_PAG1 solution board

Figure 3 shows the schematic diagram for the EZ-PD™ PAG1x-based single-stage PFC with dual-port output. In this solution, the EZ-PD™ PAG1x operates with a fixed frequency of 80-kHz and functions as a secondary-side flyback and PFC controller, and SR controller. Additionally, the EZ-PD™ CCG7DC functions as a buck controller, regulating the output voltage to a lower level than the input voltage, and a PD controller, negotiating with the connected device to provide the required power and voltage levels. The communication link between EZ-PD™ PAG1S and EZ-PD™ CCG7DC ensure optimal operation and efficiency by enabling a seamless optimization of the system's performance.

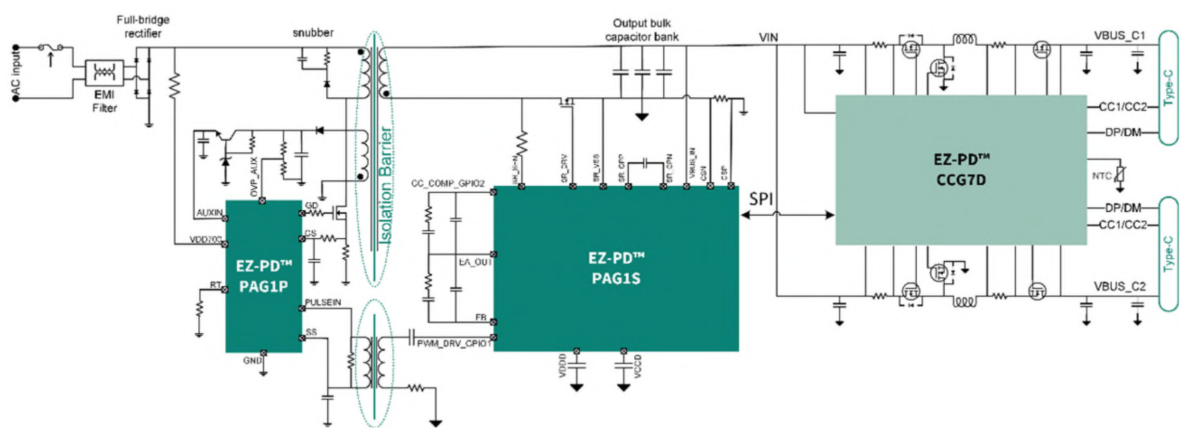

Figure 3 Schematic diagram of EZ-PD™ PAG1x-based single-stage PFC design

The waveform depicted in Figure 4 illustrates the input voltage and current characteristics of the 100 W PFC converter. This solution attains a power factor exceeding 0.9 for the entire input voltage range at a 100 W load while surpassing 0.98 for an input voltage of 115 V_{AC} and a 100 W load.

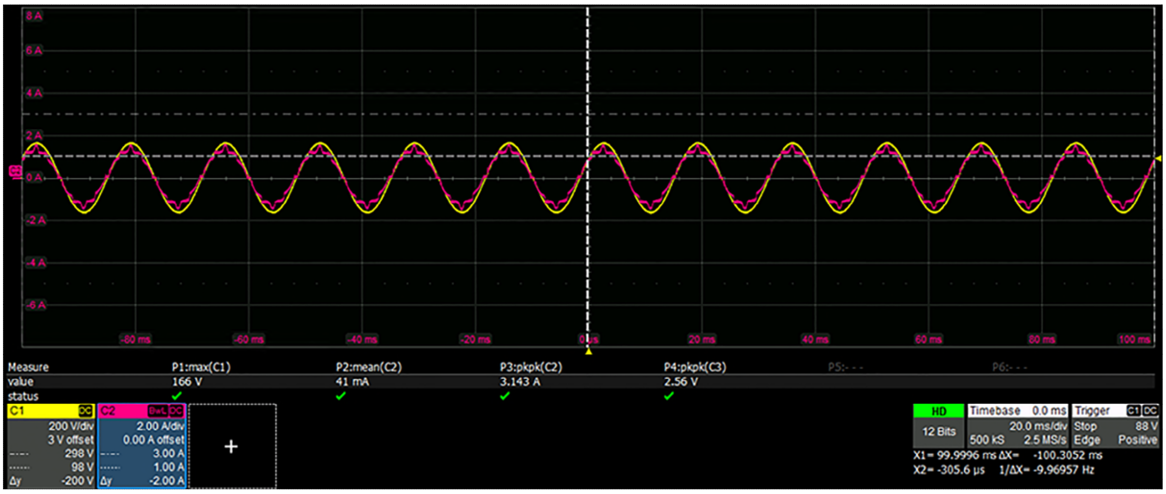

Figure 4 **Channel one shows the input voltage (yellow trace) and channel two shows the input current (magenta trace)**

4 Procedure to program EZ-PD™ CCG7DC-based daughter board

EZ-PD™ PAG1S and EZ-PD™ CCG7DC support PSoC™ MiniProg4 (CY8CKIT-005) as a programmer to program the EZ-PD™ controllers. The EZ-PD™ PAG1S-based main board and EZ-PD™ CCG7DC-based daughter board can be programmed using a PSoC™ MiniProg4 five-pin connection.

Figure 5 PSoC™ MiniProg4 (CY8CKIT-005) Programmer Kit

Programming interface and settings

The CYPRESS™ Programmer software is used as a programming interface to program the firmware (*.hex* file) in an EZ-PD™ PAG1S-based main board and EZ-PD™ CCG7DC-based daughter board. For programming, select the "CCGx" platform and make other settings, as shown in Figure 6.

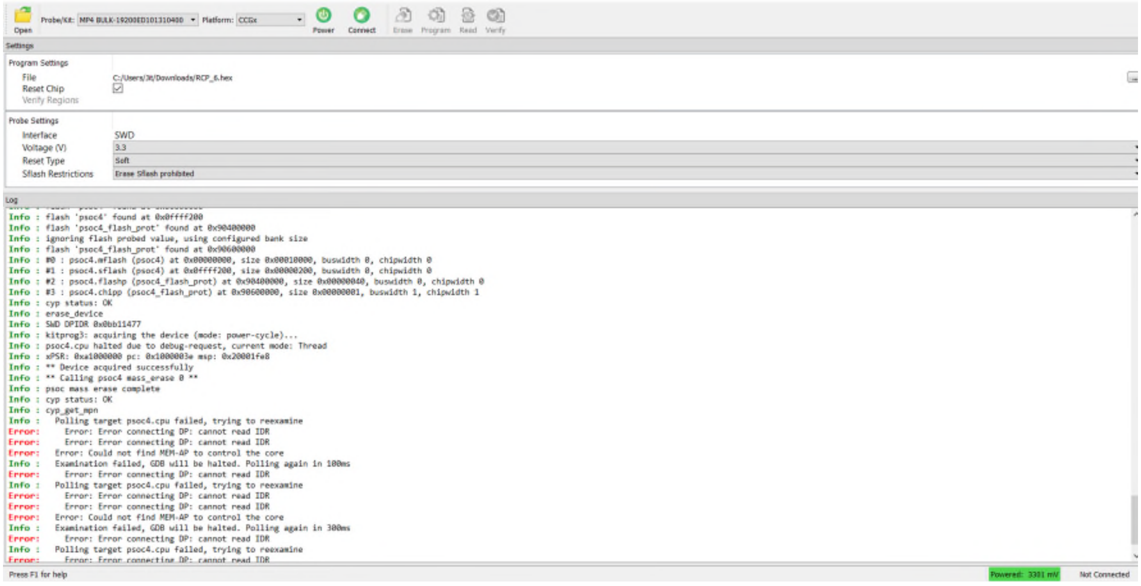

Figure 6 Programming interface to program EZ-PD™ CCG7DC 100-W daughter board

5 Test setup

Figure 7 shows the test setup to capture the electrical data of the DUT. The following setup is the optimal one to capture efficiency by capturing:

- Input power using a power meter
- Output power using high-resolution output multimeters

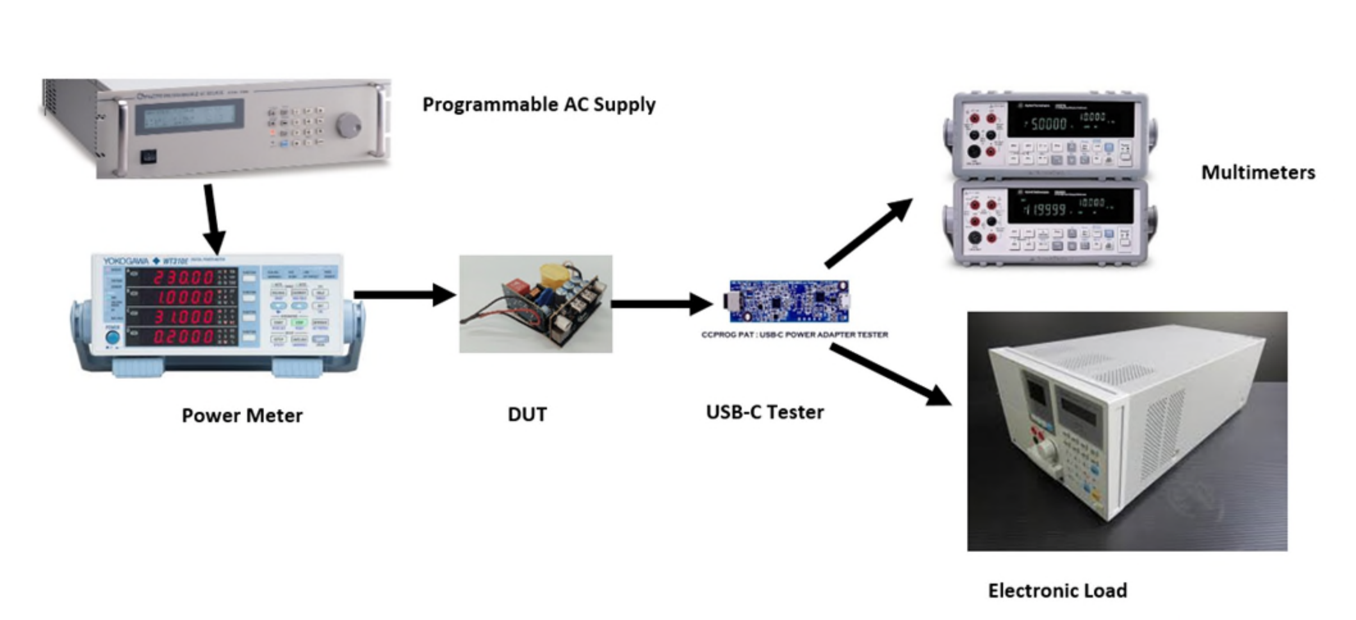

Figure 7 **Test equipment connected to the standalone REF_100W_2C_SSFB_PAG1 solution board**

5.1 Test equipment

Table 3 shows the test equipment to measure performance parameters such as efficiency, ripple, regulation, and transient response.

Table 3 **Test equipment details**

Test setup	Description
Programmable AC source	Chroma 61501
AC power meter	Yokogawa WT310E
PAT tester	USBCEE PAT
Electronic load	Chroma 63102A
Multimeters	Keysight 34465A

5.2 Power adapter tester (PAT)

Connect the DUT to a USB-C power adapter tester (PAT) using a USB Type-C cable. After the connection is established, the PAT UI does a PDO discovery and displays the results.

The EZ-PD™ PAG1S-1P based 100 W single-stage PFC USB PD dual-C charger and adapter solution is pre-configured with seven PDOs:

- **Fixed PDOs**: 5.0 V / 5.0 A; 9.0 V / 5.0 A; 15.0 V / 5.0 A; 20.0 V / 5.0 A
- **PPS**: 3.3 V to 11.0 V, 5.0 A; 3.3 V to 16.0 V, 5.0 A; 3.3 V to 21.0 V, 5.0 A (PPS power limited)

Choose a suitable pre-configured PDO or configure a new one using the EZ-PD™ Configuration Utility. Tests in the following sections use pre-configured PDOs.

To know more about the PAT tester, see USBCEE.

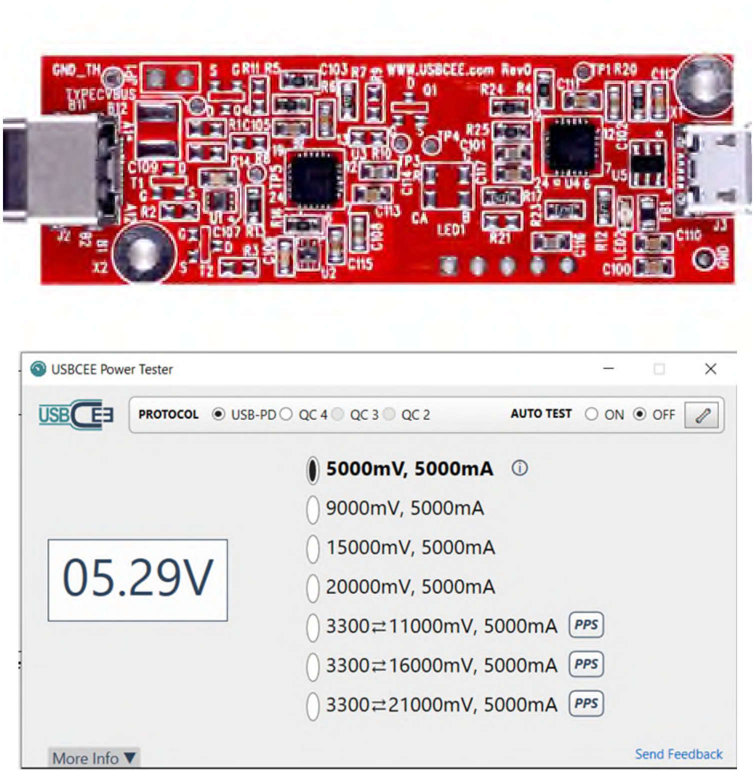

Figure 8 PAT tester and user interface

6 Quick steps for demo

1. Connect the 100 W solution board to the power meter AC terminal (which is already connected to the programmable AC supply) as in Figure 7.
2. Connect a USB PD tester or a power adapter tester (PAT) to the port and ensure the USB PD tester gets a successful Power Delivery contract as shown in Figure 8.
3. Connect the electronic load at the PAT tester load terminal as in Figure 7.
4. Select the desired voltage on PAT UI and ramp up the load on the electronic load.

References

Datasheets

[1] EZ-PD™ PAG1P, Primary side startup controller

[2] EZ-PD™ PAG1S - CYPAS111, USB PD power adapter secondary side controller

[3] CYPD7271, EZ-PD™ CCG7DC dual-port USB-C Power Delivery and DC-DC controller

Revision history

Document revision	Date	Description of changes
**	2023-03-31	Initial release
*A	2023-04-21	Post to web

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