IMC300A

iMOTION Controller with additional microcontroller

IMC300 Family
iMOTION™ Platform
Fully Integrated High Performance Motor Control System

About this document

Scope and purpose

The IMC300A motor controller series contains two distinct parts, the Motion Control Engine (MCE) for control of a motor and/or power factor correction (PFC) and an additional microcontroller (MCU) based on an Arm® Cortex®-M0 core.

This Reference Manual describes the functionality of the super-set of the embedded microcontroller and the related peripherals. For the available functionality (features) of a specific IMC300A derivative (derivative device) and package, please refer to the respective Data Sheet. For simplicity, the various device types are referenced by the collective term IMC300A throughout this manual.

Description of the functionality and configuration of the Motion Control Engine (MCE) is beyond the scope of this document and can be found in the document "iMOTION™Motion Control Engine Software Reference Manual".

Intended audience

This Reference Manual is targeting embedded hardware and software developers. It provides the reader with detailed descriptions about the behavior of the MCU and related peripheral modules embedded in the IMC300A series.

Description

The figure below shows the IMC300A in a typical application environment.

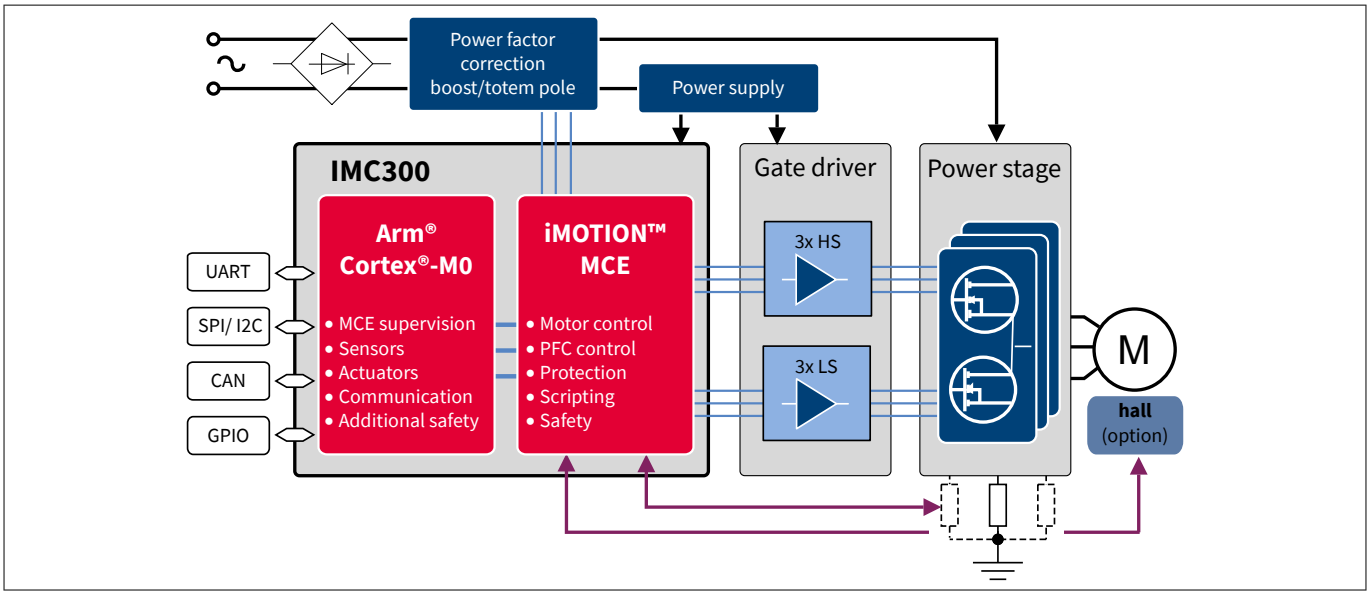

Figure 1 IMC300A application block diagram

iMOTION™ IMC300A is a family of highly integrated ICs for the control of variable speed drives. It integrates the Motion Control Engine (MCE) for control of a motor and/or power factor correction (PFC) with an additional microcontroller (MCU) based on an Arm® Cortex®-M0 core.

About this document

By integrating both the required hardware and software to perform control of a permanent magnet synchronous motor (PMSM) the MCE provides the shortest time to market for any motor system at the lowest system and development cost.

The embedded microcontroller combines an Arm® Cortex®-M0 core with Flash and SRAM memory and a comprehensive set of peripheral modules. This allows the implementation of almost any system function or communication independent from the actual motor control done by the MCE.

The interface between MCE and MCU is based on a high speed serial link allowing real time configuration and monitoring of the drive.

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1 Introduction

The IMC300A series belongs to the iMOTION Controller family of the iMOTION™ Platform based on an ARM Cortex-M0 processor core and the iMOTION™ MCE motor control core. The IMC300A series devices are the optimized solution for motor control applications featuring the Motion Control Engine (MCE) that was especially designed for highly optimized sensorless field oriented control algorithms.

Increasing complexity and demand for computing power of motor control applications and power factor correction topologies requires optimized controllers which provide a significant CPU performance, integrated peripheral functionality and rapid development environment enabling short time-to-market, without compromising cost efficiency. Nonetheless the architecture of the IMC300A controller pursues successful hardware and software concepts, which have been established in Infineon's iMOTION™ Platform portfolio.

1.1 Overview

The IMC300A series devices combine the extended functionality and performance of the ARM Cortex-M0 core including the following:

- Powerful on-chip peripheral subsystems
- On-chip memory units

The following key features are available within the range of IMC300A series devices:

CPU Subsystem

- One 32-bit ARM Cortex-M0 CPU Core
- Math Coprocessor (MATH)
  - 24-bit trigonometric calculation (CORDIC)
  - 32-bit division unit
- Nested Vectored Interrupt Controller (NVIC)
- Prefetch Unit (PFU) for code fetch access, to reduce flash latency
- Event Request Unit (ERU) for event interconnections

On-Chip Memories

- 8 Kbyte on-chip ROM
- 16 Kbyte SRAM (with parity)
- 128 Kbyte Flash (with ECC)

Supply, Reset, Clock

- 3.0 V to 5.5 V supply with power on reset and brownout detector
- External crystal oscillator support (32 kHz and 4 to 20 MHz)
- Two independent internal oscillators (32 kHz and 96 MHz)
- On-chip clock monitor supporting safety requirements (e.g. IEC 60730-1 Class B)

Timer Peripherals

- Timers and Capture/Compare Units:
  - CCU40 for signal monitoring and PWM
  - CCU41 for signal monitoring and PWM
- Position Interfaces (POSIF) for hall and quadrature encoders, motor positioning

Analog Frontend Peripherals

- Analog to Digital Converter (ADC) with up to 7 analog input channels and a fast 12-bit converter with adjustable gain
- 4 channels of out of range comparators (ORC)
- 2 fast analog comparators (ACMP)
- Temperature Sensor (DTS)
- DAC with one-bit sigma-delta generator, external low-pass filter and up to 9 outputs

Communication Peripherals

- 3 Universal Serial Interface Channels (USIC), usable as UART, SPI and I2C interfaces
- Controller Area Network interface (MultiCAN+), Full-CAN/Basic-CAN with 2 nodes and 32 message objects (MO)

System Control

- Window Watchdog Timer (WDT) for safety sensitive applications with pre-warning mechanism
- Real Time Clock (RTC) module with alarm support
- System Control Unit (SCU) for system configuration and control
- Pseudo Random Number Generator (PRNG), provides random data with fast generation times

General Purpose Input/Output Lines with Individual Bit Controllability

- Tri-stated in input mode
- Push/pull or open drain output mode
- Configurable pad hysteresis

Debug System

- Access through the standard ARM serial wire debug (SWD) or the single pin debug (SPD) interface
- A breakpoint unit (BPU) supporting up to 4 hardware breakpoints
- A watchpoint unit (DWT) supporting up to 2 watchpoints

Package Information

- PG-LQFP-64
- PG-LQFP-48

1.1.1 Block Diagram

The figures below show the toplevel block diagram and the functional blocks as well as their basic connectivity within the IMC300A system.

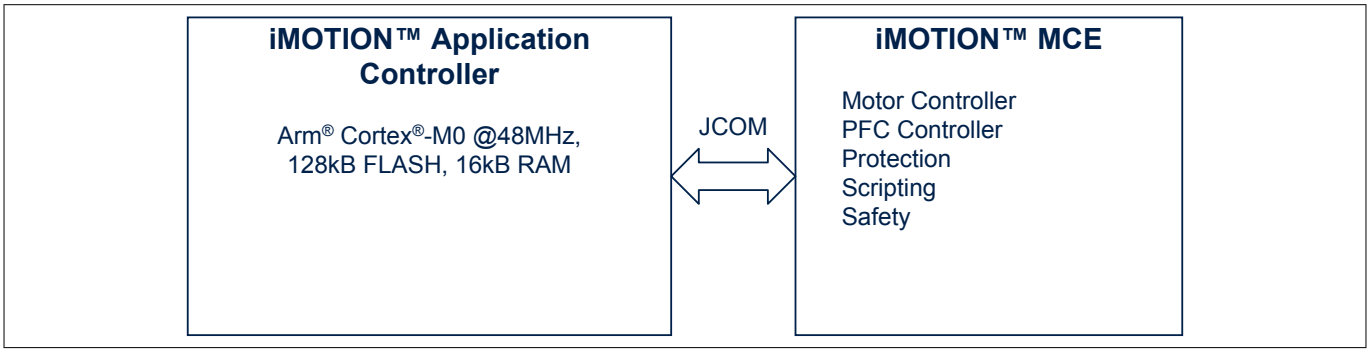

Figure 2 IMC300A Toplevel Block Diagram

1 Introduction

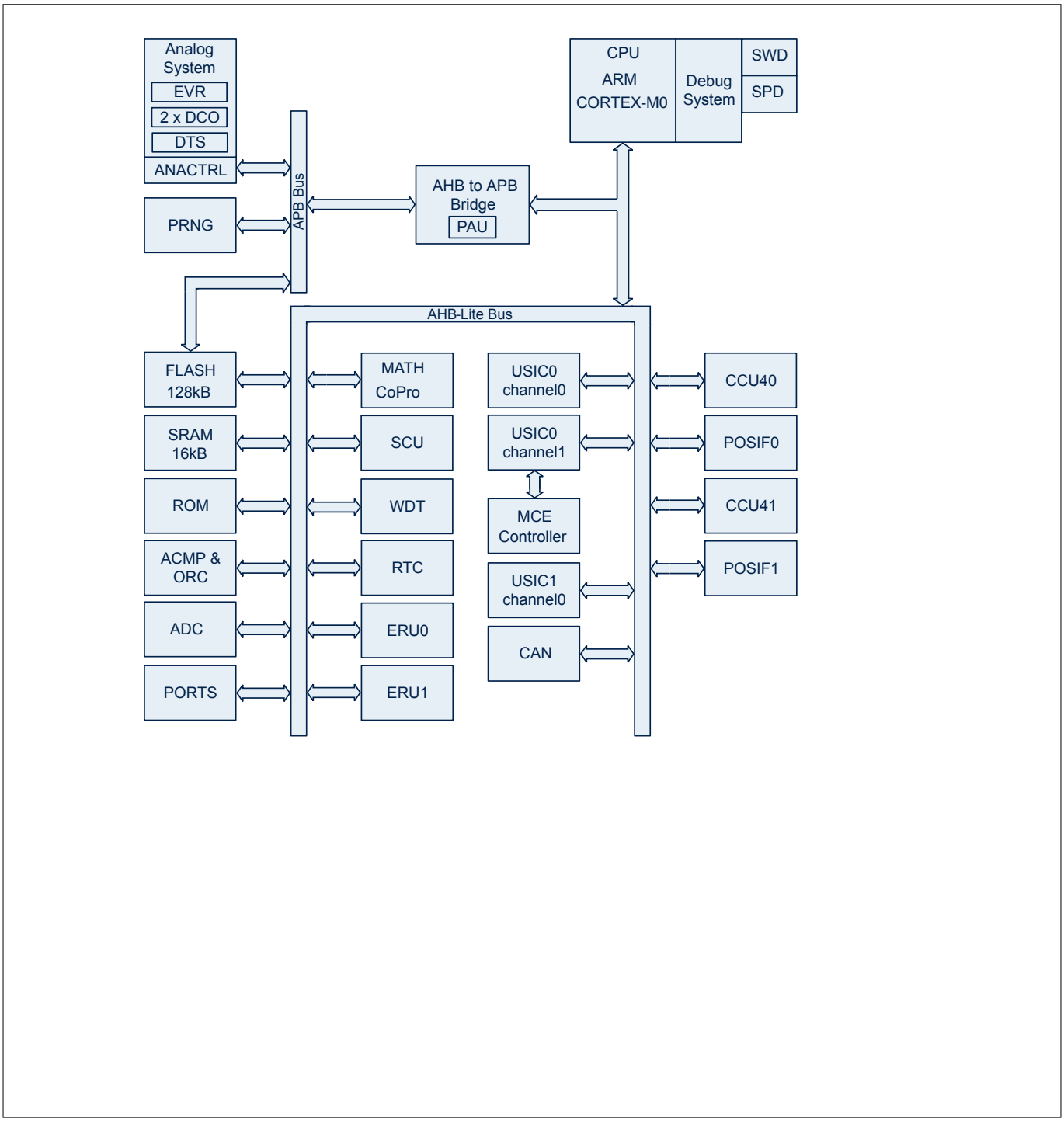

Figure 3 Block Diagram iMOTION Controller

1.1.2 Device Overview

The following table lists the available features per device type for the IMC300A series.

Table 1 Features of IMC300A Device Types[1)]

Features		IMC301A-F064	IMC302A-F064	IMC301A-F048	IMC302A-F048	
CPU frequency		48 MHz				
Operating temperature		Ambient temperature -40 to 105 °C				
Operating voltage		3.0 V to 5.5 V				
iMOTION™ Controller						
Motor Control		yes	yes	yes	yes	
Power Factor Correction (PFC)		-	yes	-	yes	
Scripting Engine		yes	yes	yes	yes	
...						
Application Controller						
Flash options (Kbytes)		128	128	128	128	
SRAM (Kbytes)		16	16	16	16	
MATH		1	1	1	1	
Timer Peripherals	CCU4, 16bit timer	8 slices	8 slices	8 slices	8 slices	
	PWM outputs / Capture Inputs	8 / 8	8 / 8	7 / 4	7 / 4	
	POSIF	1	1	1	1	
Communication Peripherals	UART	2	2	1	1	
	I2C	2	2	1	1	
	SPI (master / slave)	2 / 2	2 / 2	1 / 1	1 / 1	
	dual SPI (master / slave)	1 / 1	1 / 1	- / -	- / -	
	MultiCAN+ nodes	2	2	2	2	
Analog Peripherals	ADC (analog inputs)	7	7	5	5	
	analog comparators	2	2	2	2	
	DAC channels	7	7	4	4	
GPIO outputs		22	22	14	14	
GPIO inputs		25	25	16	16	
Packages		LQFP64	LQFP64	LQFP48	LQFP48	

1 Features that are not included in this table are available in all the derivatives

1.2 CPU Subsystem

The CPU subsystem contains the ARM Cortex-M0 processor with its 32bit bus system, the Math Coprocessor, the processing of service requests either as event requests or interrupt requests and a powerful event request unit.

1.2.1 Central Processing Unit (CPU)

The ARM Cortex-M0 processor is built on a highly area and power optimized 32-bit processor core, with a 3-stage pipeline von Neumann architecture. The processor delivers exceptional energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single cycle multiplier.

The instruction set is based on the 16-bit Thumb instrcution set and includes Thumb-2 technology. This provides the exceptional perfomance expected of a modern 32-bit architecture, with a higher code density than other 8-bit and 16-bit microcontrollers.

1.2.2 Math Coprocessor (MATH)

The MATH Coprocessor (MATH) module comprises of two independent sub-blocks to support the CPU in math-intensive computations: a Divider Unit (DIV) for signed and unsigned 32-bit division operations and a CORDIC (COrdinate Rotation DIgital Computer) Coprocessor for computation of trigonometric, linear or hyperbolic functions.

1.2.3 Programmable Multiple Priority Interrupt System (NVIC)

The IMC300A provides separate interrupt nodes that may be assigned to 4 interrupt priority levels. Most interrupt sources are connected to a dedicated interrupt node. In some cases, multi-source interrupt nodes are incorporated for efficient use of system resources. These nodes can be activated by several source requests and are controlled via interrupt subnode control registers.

1.3 On-chip Memories

Various types of dedicated memories are available on-chip. The suggested use of the memories aims to improve performance and system stability in most typical application cases. However, the user has the flexibility to use the memories in any other way in order to fulfill application specific requirements.

Boot ROM (BROM)

8 Kbyte of ROM memory for boot code execution and exception vector table. The ROM contains system basic initialization sequence code and is executed immediately after reset release. The Bootstrap Loaders (BSL) and User Routines are also stored in the ROM.

Flash memory

128 Kbyte of on-chip Flash memory store code or constant data. Dynamic error correction and parity error checks provide high read data safety for all read accesses.

Prefetch Unit (PFU)

A Prefetch unit reduces the Flash latency gap at higher system frequencies to increase the instruction per cycle performance.

SRAM memory

16 Kbyte of on-chip code RAM (SRAM) are provided to store user code or data, as well as system variables such as system stack. The SRAM is accessed via the AHB and provides zero-waitstate access for CPU code execution.

1.4 Communication Peripherals

Communication features are key requirements in today's industrial systems. The IMC300A offers a set of peripherals supporting advanced communication protocols. Dedicated hardware peripherals are available for CAN, UART, SPI and I2C.

1.4.1 Universal Serial Interface Channel (USIC)

The USIC is a flexible interface module covering several serial communication protocols such as UART, SPI and I2C. A USIC module contains two independent communication channels which can be used in parallel. A FIFO allows transmit and result buffering for relaxing real-time conditions. Multiple chip select signals are available for communication with multiple devices on the same channel.

1.4.2 Controller Area Network (MultiCAN)

The MultiCAN module contains 2 independently operating CAN nodes with Full-CAN functionality that are able to exchange Data and Remote Frames via a gateway function. Transmission and reception of CAN frames is handled in accordance to CAN specification ISO11898-1. Each CAN node can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

All 2 CAN nodes share a common set of message objects. Each message object can be individually allocated to one of the CAN nodes. Besides serving as a storage container for incoming and outgoing frames, message objects can be combined to build gateways between the CAN nodes or to set up a FIFO buffer.

1.5 Analog Frontend Peripherals

The IMC300A hosts a number of interfaces to connect to the analog world.

1.5.1 Analog to Digital Converter (ADC)

The Analog-to-Digital Converter operates according to the successive approximation principle (SAR) and provides up to 7input channels. The resolution is programmable from 8 to 12bit.

1.5.2 Analog Comparator (ACMP) and Out of Range Comparator (ORC)

The Analog Comparator is used to compare the voltage of two analog inputs and a digital output indicating which input voltage is higher. One of the input can either be the internal reference voltage or from external pin. A low power mode is available to help to reduce the total power comsumption.

A number of out-of-range on-chip comparators serve the purpose of over-voltage monitoring for analog input pins of the ADC.

1.5.3 Digital to Analog Converter (DAC)

The IMC300A supports a DAC with 7 channles. Each channel independantly generates a sigma delta bitstream which requires an external analog filter, e.g. a single capacitor or an RC-network. The DAC output signals can be configured to share the comparator input pins. As a result, the DAC generates the reference voltage for the comparators.

1.5.4 Temperature Sensor (DTS)

The Temperature Sensor generates a measurement result that indicates directly the die temperature. It is also capable of generating interrupt requests when the temperature measurement crosses the selectable upper/ lower threshold value.

1.6 Timer Peripherals

Core components needed for time based applications.

1.6.1 Capture/Compare Unit 4 (CCU4)

The CCU4 peripheral is a major component for systems that need general purpose timers for signal monitoring/ conditioning and Pulse Width Modulation (PWM) signal generation. Power electronic control systems like switched mode power supplies or uninterruptible power supplies can easily be implemented with the functions inside the CCU4 peripheral.

The internal modularity of CCU4 translates into a software friendly system for fast code development and portability between applications.

1.6.2 Position Interface Unit (POSIF)

The POSIF unit is a flexible and powerful component for motor control systems that use Rotary Encoders or Hall Sensors as feedback loop. The configuration schemes of the module target a very large number of motor control application requirements.

This enables the build of simple and complex control feedback loops for industrial motor applications, targeting high performance motion and position monitoring.

1.7 On-chip Debug Support

The on-chip debug system based on the ARM Cortex-M0® debug system provides a broad range of debug and emulation features built into the IMC300A. The user software running on the IMC300A can thus be debugged within the target system environment.

The Debug unit is controlled by an external debugging tool via the debug interface. The debugger controls the Debug unit via a set of dedicated registers accessible via the debug interface. Additionally, the Debug unit can be controlled by the CPU, e.g. by a monitor program.

Multiple breakpoints can be triggered by on-chip hardware or by software. Single stepping is supported as well as the injection of arbitrary instructions and read/write access to the complete internal address space. A breakpoint trigger can be answered with a CPU-halt, a monitor call or a data transfer.

The iMOTION™ MCE core provides a tuning and debug support on separate pins. Please refer to the MCE Software Reference Manual for details ***[10]***.

2 Conventions

2.1 iMOTION Controller User Documentation

The set of user documentation includes:

Reference Manual

The Reference Manual decribes the functionality of the superset device.

Data Sheets

Data Sheets list the complete ordering information, available features and electrical characteristics of derivative devices.

Errata Sheets

Errata Sheets list deviations from the specifications given in the related Reference Manual or Data Sheets. Errata Sheets are provided for the superset of devices.

Attention**: **Please consult all parts of the documentation set to attain consolidated knowledge about your device.

Application related guidance is provided by Users Guides and Application Notes.

Please refer to ***http://www.infineon.com/iMOTION*** to get access to the latest versions of those documents.

2.2 Copyright Notice

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2.3 Text Conventions

This document uses the following naming conventions:

- Functional units of the IMC300A are given in plain UPPER CASE. For example: “The USIC0 unit supports…”.
- Pins using negative logic are indicated by an overline. For example: “The $\overline{\text{WAIT}}$ input has…”.
- Bit fields and bits in registers are in general referenced as “Module_RegisterName.BitField” or “Module_RegisterName.Bit”. For example: “The USIC0_PCR.MCLK bit enables the…”. Most of the register names contain a module name prefix, separated by an underscore character “_” from the actual register name (for example, “USIC0_PCR”, where “USIC0” is the module name prefix, and “PCR” is the kernel register name). In chapters describing the kernels of the peripheral modules, the registers are mainly referenced with their kernel register names. The peripheral module implementation sections mainly refer to the actual register names with module prefixes.
- Variables used to describe sets of processing units or registers appear in mixed upper and lower cases. For example, register name “MOFCRn” refers to multiple “MOFCR” registers with variable n. The bounds of the variables are always given where the register expression is first used (for example, “n = 0-31”), and are repeated as needed in the rest of the text.
- The default radix is decimal. Hexadecimal constants are suffixed with a subscript letter “H”, as in 100_H. Binary constants are suffixed with a subscript letter “B”, as in: 111_B.
- When the extent of register fields, groups register bits, or groups of pins are collectively named in the body of the document, they are represented as “NAME[A:B]”, which defines a range for the named group from B to A. Individual bits, signals, or pins are given as “NAME[C]” where the range of the variable C is given in the text. For example: CFG[2:0] and SRPN[0].

- Units are abbreviated as follows:
  - MHz = Megahertz
  - µs = Microseconds
  - kBaud, kbit = 1000 characters/bits per second
  - MBaud, Mbit = 1,000,000 characters/bits per second
  - Kbyte, KB = 1024 bytes of memory
  - Mbyte, MB= 1048576 bytes of memory

  In general, the k prefix scales a unit by 1000 whereas the K prefix scales a unit by 1024. Hence, the Kbyte unit scales the expression preceding it by 1024. The kBaud unit scales the expression preceding it by 1000. The M prefix scales by 1,000,000 or 1048576. For example, 1 Kbyte is 1024 bytes, 1 Mbyte is 1024 × 1024 bytes, 1 kBaud/kbit are 1000 characters/bits per second, 1 MBaud/Mbit are 1000000 characters/bits per second, and 1 MHz is 1,000,000 Hz.
- Data format quantities are defined as follows:
  - Byte = 8-bit quantity
  - Half-word = 16-bit quantity
  - Word = 32-bit quantity
  - Double-word = 64-bit quantity

2.4 Bit Function Terminology

In tables where register bits or bit fields are defined, the following conventions are used to indicate the access types.

Table 2 Bit Function Terminology

Bit Function	Description
rw	The bit or bit field can be read and written.
rwh	As rw, but bit or bit field can be also set or reset by hardware. If not otherwise documented the software takes priority in case of a write conflict between software and hardware.
r	The bit or bit field can only be read (read-only).
w	The bit or bit field can only be written (write-only). A read to this register will always give a default value back.
rh	This bit or bit field can be modified by hardware (read-hardware, typical example: status flags). A read of this bit or bit field give the actual status of this bit or bit field back. Writing to this bit or bit field has no effect to the setting of this bit or bit field.

2.5 Register Access Modes

Read and write access to registers and memory locations are sometimes restricted. In memory and register access tables, the following terms are used.

Table 3 Register Access Modes

Symbol	Description
PV (SV), U	Access permitted in Privileged (Supervisor) Mode. *Note: ARM® Cortex M0 processor does not support different privilege levels. Only Privileged (Supervisor) Mode is supported in iMOTION Controller. Symbol "U" and Symbol "PV" can be used to represent the access permitted in this mode.*
BP	Indicates that this register can only be access when the bit protection is disabled. See detailed description of Bit Protection Scheme in the Memory Organisation chapter.
32	Only 32-bit word accesses are permitted to this register/address range.
NC	No change, indicated register is not changed.
BE	Indicates that an access to this address range generates a Bus Error.
nBE	Indicates that no Bus Error is generated when accessing this address range.

2.6 Reserved Bits

Register bit fields named **Reserved** or **0** indicate unimplemented functions with the following behavior.

- Reading these bit fields returns 0.
- These bit fields should be written with 0 if the bit field is defined as r or rh.
- These bit fields have to be written with 0 if the bit field is defined as rw.

These bit fields are reserved. The detailed description of these bit fields can be found in the register descriptions.

2.7 Abbreviations and Acronyms

ACMP	Analog Comparator
ADC	Analog-to Digital Converter
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
ANACTRL	Analog Control Unit
APB	Advanced Peripheral Bus
ASC	Asynchronous Serial Channel
BMI	Boot Mode Index
CMSIS	Cortex Microcontroller Software Interface Standard
CPU	Central Processing Unit
CCU4	Capture Compare Unit 4
CRC	Cyclic Redundancy Code
DAC	Digital to Analog Converter
DCO	Digitally Controlled Oscillator

2 Conventions

ECC	Error Correction Code
ERU	Event Request Unit
EVR	Embedded Voltage Regulator
FSM	Flash State Machine
GPIO	General Purpose Input/Output
IIC, I2C	Inter Integrated Circuit (also known as I2C)
IPM	Intelligent Power Module
iMOTION	A family of highly integrated products for the control of a variable speed drive
I/O	Input / Output
MATH	Math Coprocessor
MCE	Motion Control Engine
MSB	Most Significant Bit
NC	Not Connected
NMI	Non-Maskable Interrupt
NVIC	Nested Vectored Interrupt Controller
ORC	Out of Range Comparator
PAU	Peripheral Access Unit
PFU	Prefetch Unit
POSIF	Position Interface
PRNG	Pseudo Random Number Generator
ROM	Read-Only Memory
RAM	Random Access Memory
RTC	Real Time Clock
SCU	System Control Unit
SFR	Special Function Register
SHS	Sample and Hold Sequencer
SPI	Serial Peripheral Interface
SPD	Single Pin Debug Interface (defined by Infineon)
SRAM	Static RAM
SR	Service Request
SSC	Synchronous Serial Channel
SSW	Start-up Software
SWD	Serial Wire Debug Interface (defined by ARM)
TSE	Temperature Sensor
UART	Universal Asynchronous Receiver Transmitter
USIC	Universal Serial Interface Channel

WDT	Watchdog Timer

3 Motion Control Engine Interface

The interface to the Motion Control Engine (MCE) is based on a high speed serial link. Using the application MCU as the master and the MCE as the slave this JCOM interface allows access to the parameter configuration and data streaming between the application MCU and MCE.

The iMOTION™ Motion Control Engine (MCE) is a ready-to-use solution for variable speed drives. It contains all required hardware and software modules to perform the motor control and an optional power factor correction (PFC) in parallel. The MCE can be configured for almost any power stage and motor. A detailed description is beyond the scope of this document, please refer to the respective software reference manual.

The IMC300A provide an internal interface between the application MCU and the MCE called JCOM. The physical layer is based on a serial channel. The communication protocol is documented in detail within the MCE software reference manual.

The table below states the interface as used in the IMC300A.

Table 4 JCOM interface

JCOM function	Application MCU Pin	Description
JCOM channel	USIC0 CH1	USIC module and channel
JCOM transmit	P1.2	data from MCU to MCE
JCOM receive	P1.3	data from MCE to MCU
JCOM sync	P1.5	sync pin (function defined by software)
JCOM clock default	1.0 Mbps	default on startup

The speed of the JCOM interface can be configured over a wide range in order to meet the requirements of the concrete application. If the MCE experiences a number of frame errors it will automatically fall back to the default baud rate.

In order to ease the implementation of the JCOM communication protocol Infineon provides the respective software driver for this JCOM interface.

4 Central Processing Unit (CPU)

IMC300A features one ARM Cortex-M0 processor. An entry-level 32-bit ARM Cortex processor designed for a broad range of embedded applications. These CPUs offer significant benefits to users, including:

- a simple architecture that is easy to learn and program
- ultra-low power, energy efficient operation
- excellent code density
- deterministic, high-performance interrupt handling
- upward compatibility with Cortex-M processor family

4.1 Overview

The Cortex-M0 processor is built on a highly area and power optimized 32-bit processor core, with a 3-stage pipeline von Neumann architecture. The processor delivers exceptional energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier.

The Cortex-M0 processor implements the ARMv6-M architecture, which is based on the 16-bit Thumb® instruction set and includes Thumb-2 technology. The Cortex-M0 instruction set provides exceptional performance expected of a modern 32-bit architecture, with a higher code density than other 8-bit and 16-bit microcontrollers.

The Cortex-M0 processor closely integrates a configurable NVIC, to deliver industry leading interrupt performance. The NVIC provides 4 interrupt priority levels. The tight integration of the processor core and NVIC provides fast execution of interrupt service routines (ISRs), dramatically reducing the interrupt latency. This is achieved through the hardware stacking of registers, and the ability to abandon and restart load-multiple and store-multiple operations. Interrupt handlers do not require any assembler wrapper code, removing any code overhead from the ISRs. Tail-chaining optimization also significantly reduces the overhead when switching from one ISR to another.

To optimize low-power designs, the NVIC integrates with the sleep modes, that include a deep sleep function that enables the entire device to be rapidly powered down.

4.1.1 Features

The CPU provides the following functionality:

- Thumb instruction set combines high code density with 32-bit performance
- integrated sleep modes for low power consumption
- fast code execution permits slower processor clock or increases sleep mode time
- single cycle 32-bit hardware multiplier
- high-performance interrupt handling for time-critical applications
- extensive debug capabilities:
  - Serial Wire Debug and Single Pin Debug reduce the number of pins required for debugging.

4.1.2 Block Diagram

The Cortex-M0 core components comprise of:

Processor Core

The CPU provides most 16-bit Thumb instruction set and subset of 32-bit Thumb2 instruction set.

Nested Vectored Interrupt Controller

The NVIC is an embedded interrupt controller that supports low latency interrupt processing.

Debug Solution

The IMC300A implements a complete hardware debug solution.

- Single Pin Debug (SPD) or 2-pin Serial Wire Debug (SWD)
- Extensive hardware breakpoint and watchpoint options

This provides high system control and visibility of the processor and memory even in small package devices.

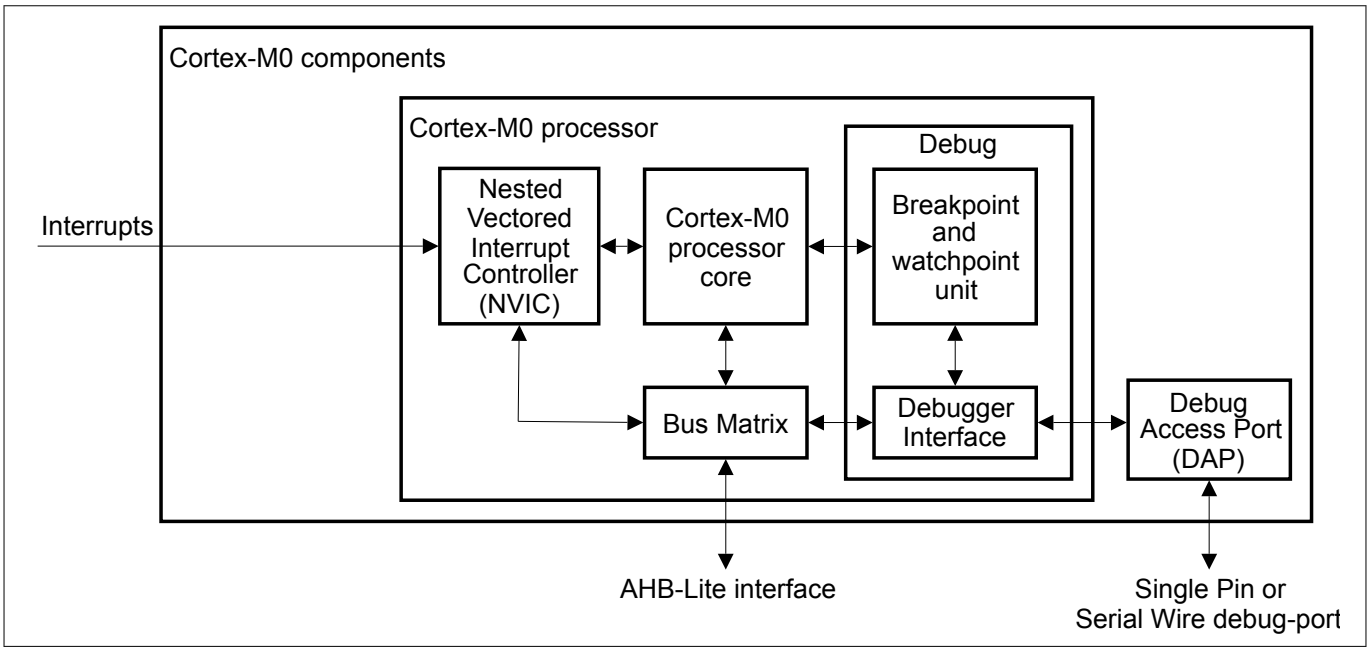


Figure 4 Cortex-M0 Block Diagram

System Level Interface

The Cortex-M0 processor provides a single system-level interface using AMBA® technology to provide high speed, low latency memory accesses.

4.2 Programmers Model

This section describes the Cortex-M0 programmers model. In addition to the individual core register descriptions, it contains information about the processor modes and stacks.

4.2.1 Processor Modes

Thread mode

Used to execute application software. The processor enters Thread mode when it comes out of reset.

Handler mode

Used to handle exceptions. The processor returns to Thread mode when it has finished all exception processing.

4.2.2 Stacks

The processor uses a full descending stack. This means the stack pointer holds the address of the last stacked item in memory. When the processor pushes a new item onto the stack, it decrements the stack pointer and then writes the item to the new memory location. The processor implements two stacks, the main stack and the process stack, with a pointer for each held in independent registers, see ***Stack Pointer***.

In Thread mode, the CONTROL register controls whether the processor uses the main stack or the process stack, see ***CONTROL Register***. In Handler mode, the processor always uses the main stack. The options for processor operations are:

Table 5 Summary of processor mode, execution, and stack use options

Processor mode	Used to execute	Stack used
Thread	Applications	Main stack or process stack[2)]
Handler	Exception handlers	Main stack

4.2.3 Core Registers

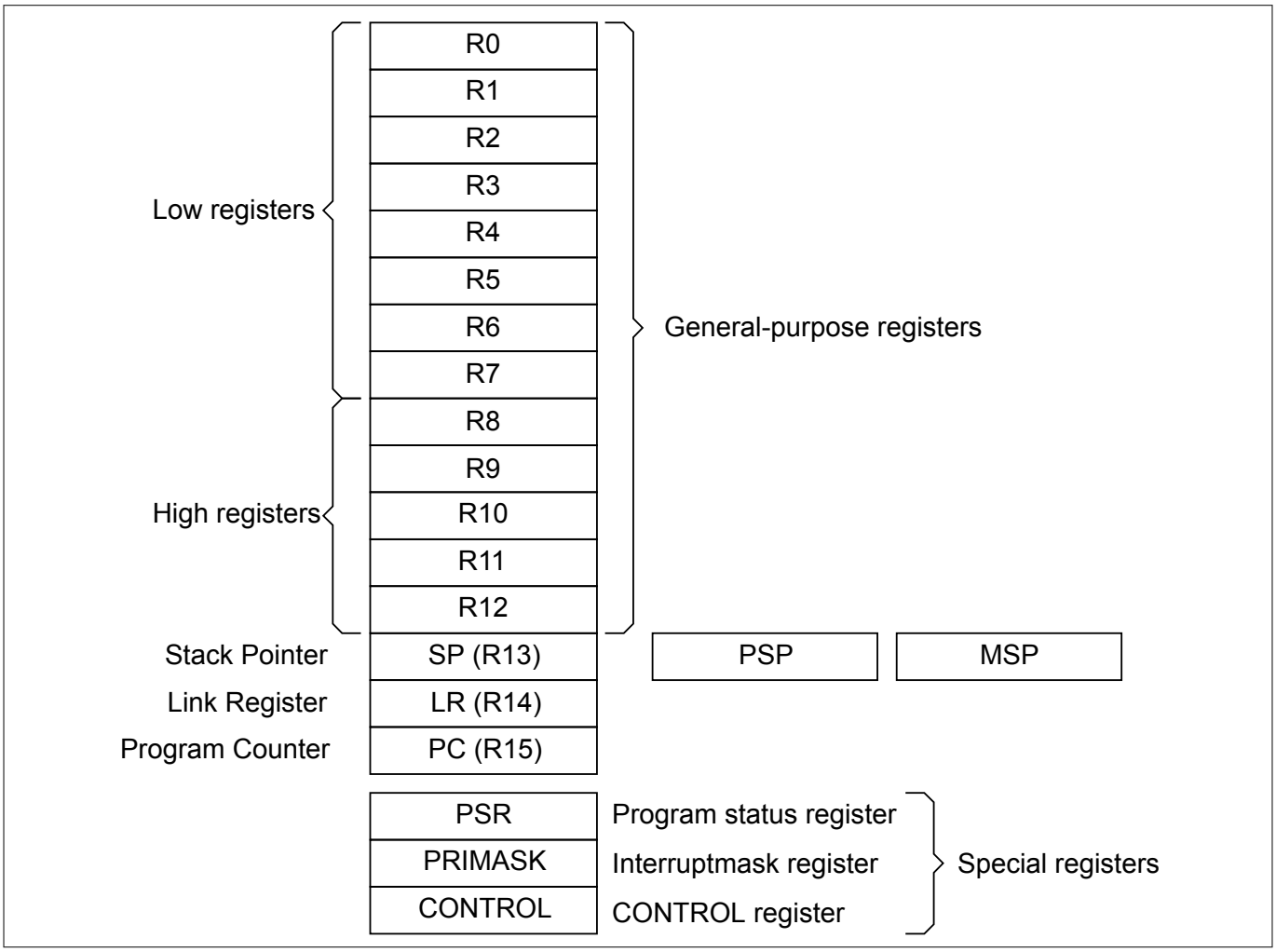


Figure 5 Core registers

The processor core registers are:

Table 6 Core register set summary

Name	Type[3)]	Reset value	Description
R0-R12	rw	Unknown	***General-purpose registers*** on page 52
MSP	rw	See description	***Stack Pointer*** on page 52

2 See ***CONTROL Register***.
3 Describes access type during program execution in thread mode and handler mode. Debug access can differ.

Table 6 Core register set summary (continued)

Name	Type[3)]	Reset value	Description
PSP	rw	Unknown	***Stack Pointer*** on page 52
LR	rw	Unknown	***Link Register*** on page 53
PC	rw	See description	***Program Counter*** on page 53
PSR	rw	Unknown	***Program Status Register*** on page 54
APSR	rw	Unknown	***Application Program Status Register*** on page 54
IPSR	r	00000000_H	***Interrupt Program Status Register*** on page 55
EPSR	r	Unknown	***Execution Program Status Register*** on page 56
PRIMASK	rw	00000000_H	***Priority Mask Register*** on page 57
CONTROL	rw	00000000_H	***CONTROL Register*** on page 58

4.2.3.1 General-purpose registers

R0-R12 are 32-bit general-purpose registers for data operations.

*Note: For information on how to program the core registers, please refer to **[2]**.*

Rx (x=0-12)

General-purpose register Rx Reset Value: XXXXXXXX_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Value															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value															
rw															

Field	Bits	Type	Description
Value	31:0	rw	**Content of Register**

4.2.3.2 Stack Pointer

The Stack Pointer (SP) is register R13. In Thread mode, bit[1] of the CONTROL register indicates the stack pointer to use:

- 0 = Main Stack Pointer (MSP). This is the reset value.
- 1 = Process Stack Pointer (PSP).

On reset, the processor loads the MSP with the value from address 00000000_H.

*Note: For information on how to program the core registers, please refer to **[2]**.*

3 Describes access type during program execution in thread mode and handler mode. Debug access can differ.

SP

Stack Pointer Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Value															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value															
rw															

Field	Bits	Type	Description
Value	31:0	rw	**Content of Register**

4.2.3.3 Link Register

The Link Register (LR) is register R14. It stores the return information for subroutines, function calls, and exceptions. On reset, the LR value is unknown.

*Note: For information on how to program the core registers, please refer to **[2]**.*

LR

Link Register Reset Value: XXXXXXXX_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Value															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value															
rw															

Field	Bits	Type	Description
Value	31:0	rw	**Content of Register**

4.2.3.4 Program Counter

The Program Counter (PC) is register R15. It contains the current program address. On reset, the processor loads the PC with the value of the reset vector, which is at address 00000004_H. Bit [0] of the value is loaded into the EPSR T-bit at reset and must be 1.

*Note: For information on how to program the core registers, please refer to **[2]**.*

PC

Program Counter Reset Value: 00000004_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Value															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value															
rw															

Field	Bits	Type	Description
Value	31:0	rw	**Content of Register**

4.2.3.5 Program Status Register

The Program Status Register (PSR) combines:

- Application Program Status Register (APSR)
- Interrupt Program Status Register (IPSR)
- Execution Program Status Register (EPSR)

These registers are mutually exclusive bit fields in the 32-bit PSR.

Access these registers individually or as a combination of any two or all three registers, using the register name as an argument to the MSR or MRS instructions. For example:

- read all of the registers using PSR with the MRS instruction
- write to the APSR N, Z, C, and V bits using APSR with the MSR instruction

The PSR combinations and attributes are:

Table 7 PSR register combinations

Register	Type	Combination
PSR	rw[4)5)]	APSR, EPSR, and IPSR
IEPSR	r	EPSR and IPSR
IAPSR	rw[4)]	APSR and IPSR
EAPSR	rw[5)]	APSR and EPSR

4.2.3.5.1 Application Program Status Register

The APSR contains the current state of the condition flags from previous instruction executions. See the register summary in ***Table 6*** for its attributes.

APSR

Application Program Status Register Reset Value: XXXXXXXX_H

4 The processor ignores writes to the IPSR bits.
5 Reads of the EPSR bits return zero, and the processor ignores writes to the these bits

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
N	**Z**	**C**	**V**	**0**											
rw	rw	rw	rw	r											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0															
r															

Field	Bits	Type	Description
N	31	rw	**Negative flag**
Z	30	rw	**Zero flag**
C	29	rw	**Carry or borrow flag**
V	28	rw	**Overflow flag**
0	27:0	r	**Reserved**

4.2.3.5.2 Interrupt Program Status Register

The IPSR contains the exception type number of the current Interrupt Service Routine (ISR). See the register summary in ***Table 6*** for its attributes.

IPSR

Interrupt Program Status Register Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0										**ISR_NUMBER**					
r										r					

Field	Bits	Type	Description
0	31:6	r	**Reserved**

(continued)

Field	Bits	Type	Description
ISR_NUMBER	5:0	r	**Number of the current exception** 0_D Thread mode 1_D Reserved 2_D Reserved 3_D HardFault 4_D Reserved 5_D Reserved 6_D Reserved 7_D Reserved 8_D Reserved 9_D Reserved 10_D Reserved 11_D SVCall 12_D Reserved 13_D Reserved 14_D PendSV 15_D SysTick 16_D IRQ0 ... 48_D-63_D Reserved See Exception types in ***Chapter 4.5.2*** for more information.

4.2.3.5.3 Execution Program Status Register

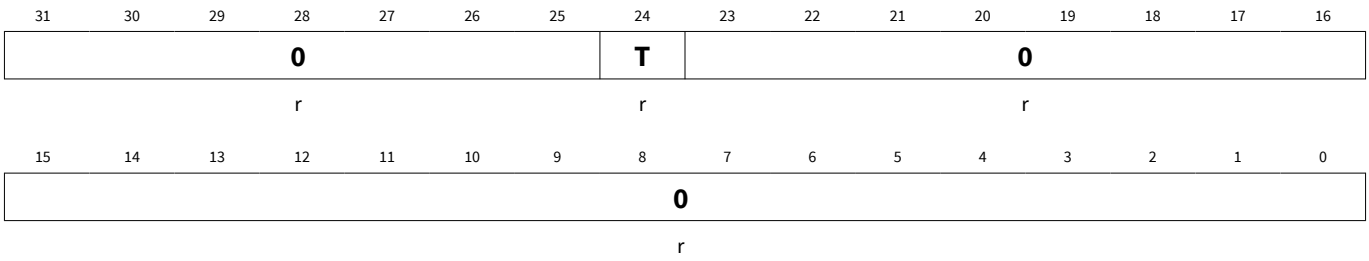
The EPSR contains the Thumb state bit.

See the register summary in ***Table 6*** for the EPSR attributes.

Attempts to read the EPSR directly through application software using the MSR instruction always return zero. Attempts to write the EPSR using the MSR instruction in application software are ignored. Fault handlers can examine the EPSR value in the stacked PSR to determine the cause of the fault. See Exception Entry and Return in ***Chapter 4.5.6***.

EPSR

Execution Program Status Register Reset Value: XXXXXXXX_H



Field	Bits	Type	Description
0	31:25	r	**Reserved**

(continued)

Field	Bits	Type	Description
T	24	r	**Thumb state bit** See Thumb state.
0	23:0	r	**Reserved**

4.2.3.5.4 Interruptible-restartable instructions

When an interrupt occurs during the execution of an LDM, STM, PUSH, POP instruction, the processor abandons execution of the instruction.

After servicing the interrupt, the processor restarts execution of the instruction from the beginning.

4.2.3.5.5 Thumb state

The Cortex-M0 processor only supports execution of instructions in Thumb state. The following can clear the T bit to 0:

- instructions BLX, BX and POP{PC}
- restoration from the stacked xPSR value on an exception return
- bit[0] of the vector value on an exception entry.

Attempting to execute instructions when the T bit is 0 results in a HardFault or lockup. See Lockup in ***Chapter 4.6.1*** for more information.

4.2.3.6 Exception mask registers

The exception mask registers disable the handling of exceptions by the processor. Disable exceptions where they might impact on timing critical tasks or code sequences requiring atomicity.

Exceptions can be disabled or re-enabled by the MSR and MRS instructions, or the CPS instruction, to change the value of PRIMASK or FAULTMASK.

4.2.3.6.1 Priority Mask Register

The PRIMASK register prevents activation of all exceptions with configurable priority. See the register summary in ***Table 6*** for its attributes.

PRIMASK

Priority Mask Register — Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0															PRIMASK
r															rw

Field	Bits	Type	Description
0	31:1	r	**Reserved**
PRIMASK	0	rw	**Priority Mask** 0_B No effect. 1_B Prevents the activation of all exceptions with configurable priority.

4.2.3.7 CONTROL Register

The CONTROL register controls the stack used when the processor is in Thread mode. See the register summary in ***Table 6*** for its attributes.

CONTROL

CONTROL Register Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0														**SPSEL**	**0**
r														rw	r

Field	Bits	Type	Description
0	31:2	r	**Reserved**
SPSEL	1	rw	**Active stack pointer** This bit defines the current stack. In Handler mode, this bit reads as zero and ignores writes. 0_B MSP is the current stack pointer 1_B PSP is the current stack pointer
0	0	r	**Reserved**

Handler mode always uses the MSP, so the processor ignores explicit writes to the active stack pointer bit of the CONTROL register when in Handler mode. The exception entry and return mechanisms automatically update the CONTROL register.

In an OS environment, it is recommended that threads running in Thread mode use the process stack and the kernel and exception handlers use the main stack.

By default, Thread mode uses the MSP. To switch the stack pointer used in Thread mode to the PSP, use the MSR instruction to set the Active stack pointer bit to 1.

Note: When changing the stack pointer, software must use an ISB instruction immediately after the MSR instruction. This ensures that instructions after the ISB instruction execute using the new stack pointer.

4.2.4 Exceptions and Interrupts

The Cortex-M0 processor supports interrupts and system exceptions. The processor and the NVIC prioritize and handle all exceptions. An interrupt or exception changes the normal flow of software control. The processor uses handler mode to handle all exceptions except for reset. See Exception entry on ***Chapter 4.5.6.1*** and Exception return on ***Chapter 4.5.6.2*** for more information.

The NVIC registers control interrupt handling. See Interrupt System chapter for more information.

4.2.5 Data Types

The processor:

- supports the following data types:
  - 32-bit words
  - 16-bit halfwords
  - 8-bit bytes
- manages all data memory accesses as little-endian. See Memory regions, types and attributes in ***Chapter 4.3.1*** for more information.

4.2.6 The Cortex Microcontroller Software Interface Standard

For a Cortex-M0 microcontroller system, the Cortex Microcontroller Software Interface Standard (CMSIS) ***[7]*** defines:

- a common way to:
  - access peripheral registers
  - define exception vectors
- the names of:
  - the registers of the core peripherals
  - the core exception vectors
- a device-independent interface for RTOS kernels.

The CMSIS includes address definitions and data structures for the core peripherals in the Cortex-M0 processor.

CMSIS simplifies software development by enabling the reuse of template code and the combination of CMSIS-compliant software components from various middleware vendors. Software vendors can expand the CMSIS to include their peripheral definitions and access functions for those peripherals.

This document includes the register names defined by the CMSIS, and gives short descriptions of the CMSIS functions that address the processor core and the core peripherals.

Note: This document uses the register short names defined by the CMSIS. In a few cases these differ from the architectural short names that might be used in other documents.

The following sections give more information about the CMSIS:

- Power Management Programming Hints in ***Chapter 4.7.3***
- CMSIS Functions in ***Chapter 4.2.7***
- Accessing CPU Registers using CMSIS in Interrupt System chapter
- NVIC programming hints in Interrupt System chapter

For additional information please refer to ***http://www.onarm.com/cmsis***

4.2.7 CMSIS Functions

ISO/IEC C code cannot directly access some Cortex-M0 instructions. This section describes intrinsic functions that can generate these instructions, provided by the CMSIS and that might be provided by a C compiler. If a C compiler does not support an appropriate intrinsic function, an inline assembler may be used to access the relevant instruction.

The CMSIS provides the following intrinsic functions to generate instructions that ISO/IEC C code cannot directly access:

Table 8 CMSIS functions to generate some Cortex-M0 instructions

Instruction	CMSIS intrinsic function
CPSIE i	void __enable_irq (void)
CPSID i	void __disable_irq (void)
ISB	void __ISB (void)
DSB	void __DSB (void)
DMB	void __DMB (void)
NOP	void __NOP (void)
REV	uint32_t __REV (uint32_t int value)
REV16	uint32_t __REV16 (uint32_t int value)
REVSH	uint32_t __REVSH (uint32_t int value)
WFE	void __WFE (void)
WFI	void __WFI (void)

The CMSIS also provides a number of functions for accessing the special registers using MRS and MSR instructions:

Table 9 CMSIS functions to access the special registers

Special register	Access	CMSIS function
PRIMASK	Read	uint32_t __get_PRIMASK (void)
	Write	void __set_PRIMASK (uint32_t value)
CONTROL	Read	uint32_t __get_CONTROL (void)
	Write	void __set_CONTROL (uint32_t value)
MSP	Read	uint32_t __get_MSP (void)
	Write	void __set_MSP (uint32_t TopOfMainStack)
PSP	Read	uint32_t __get_PSP (void)
	Write	void __set_PSP (uint32_t TopOfMainStack)

4.3 Memory Model

This section describes the processor memory map and the behavior of memory accesses. The processor has a fixed default memory map that provides up to 4GB of addressable memory. The memory map is:

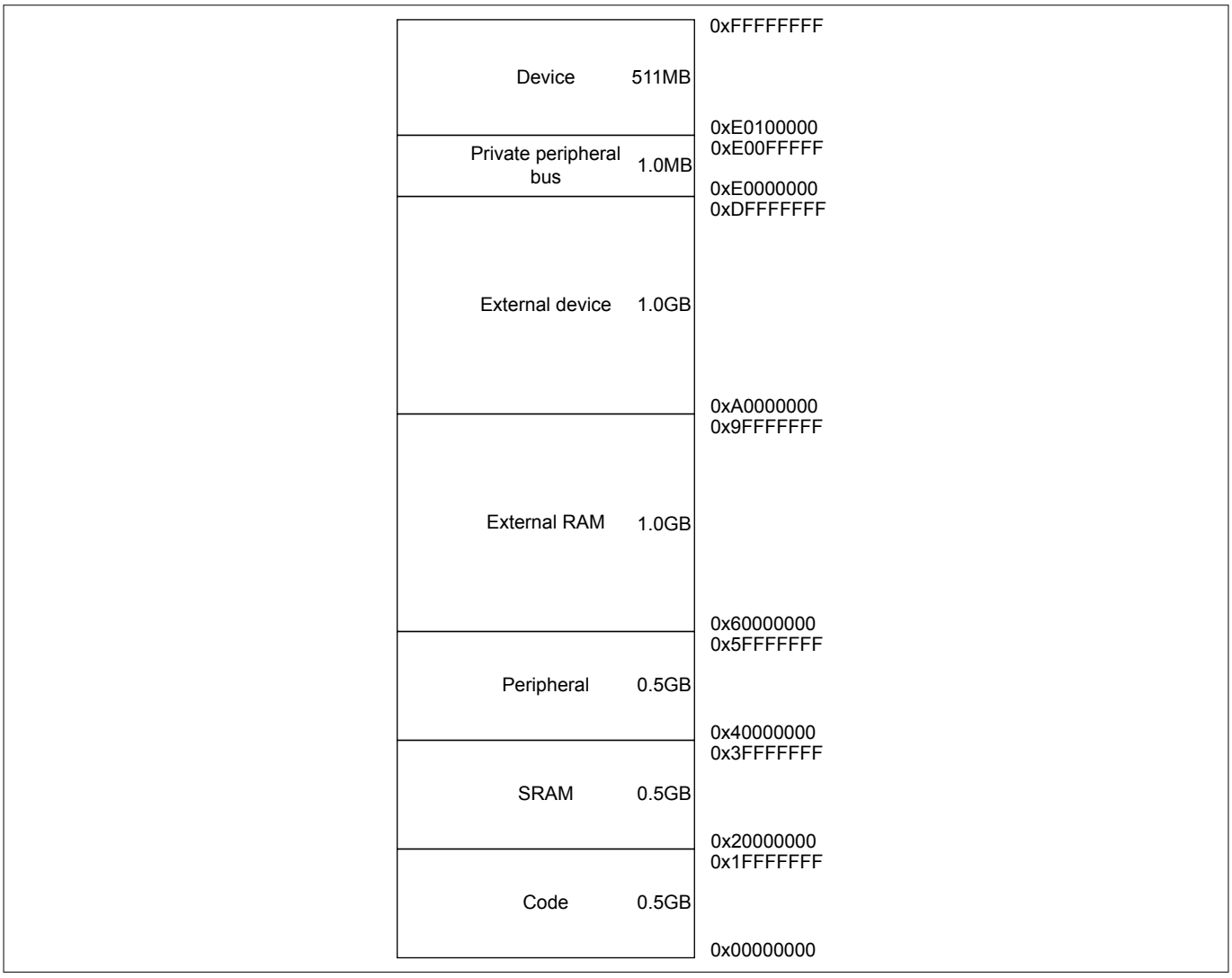


Figure 6 Memory map

The processor reserves regions of the Private peripheral bus (PPB) address range for core peripheral registers, see About the Private Peripherals in ***Chapter 4.8.1***.

4.3.1 Memory Regions, Types and Attributes

The memory map is split into regions. Each region has a defined memory type, and some regions have additional memory attributes. The memory type and attributes determine the behavior of accesses to the region.

The memory types are:

Normal

The processor can re-order transactions for efficiency, or perform speculative reads.

Device

The processor preserves transaction order relative to other transactions to Device or Strongly-ordered memory.

Strongly-ordered

The processor preserves transaction order relative to all other transactions.

The different ordering requirements for Device and Strongly-ordered memory mean that the memory system can buffer a write to Device memory, but must not buffer a write to Strongly-ordered memory.

The additional memory attributes include:

Execute Never (XN)

Means the processor prevents instruction accesses. A HardFault exception is generated on execution of an instruction fetched from an XN region of memory.

4.3.2 Memory System Ordering of Memory Accesses

For most memory accesses caused by explicit memory access instructions, the memory system does not guarantee that the order in which the accesses complete matches the program order of the instructions, providing any re-ordering does not affect the behavior of the instruction sequence. Normally, if correct program execution depends on two memory accesses completing in program order, software must insert a memory barrier instruction between the memory access instructions, see Software ordering of memory accesses in ***Chapter 4.3.4***.

However, the memory system does guarantee some ordering of accesses to Device and Strongly-ordered memory. For two memory access instructions A1 and A2, if A1 occurs before A2 in program order, the ordering of the memory accesses caused by two instructions is described in ***Figure 7***.

A1 \ A2	Normal access	Device access	Strongly-ordered access
Normal access	-	-	-
Device access	-	<	<
Strongly-ordered access	-	<	<

Figure 7 Memory system ordering

Where:

- "-" Means that the memory system does not guarentee the ordering of the accesses.
- "<" Means that accesses are observed in program order, that is, A1 is always observed before A2.

4.3.3 Behavior of Memory Accesses

The behavior of accesses to each region in the memory map is:

Table 10 Memory access behavior

Address range	Memory region	Memory type[6]	XN[6]	Description
0x00000000-0x1FFFFFFF	Code	Normal	-	Executable region for program code. Data can be placed here.
0x20000000-0x3FFFFFFF	SRAM	Normal	-	Executable region for data. Code can be placed here.
0x40000000-0x5FFFFFFF	Peripheral	Device	XN	Peripherals region.
0x60000000-0x9FFFFFFF	External RAM	Normal	-	Executable region for data.

6 See Memory regions, types and attributes in ***Chapter 4.3.1*** for more information.

Table 10 Memory access behavior (continued)

Address range	Memory region	Memory type[6]	XN[6]	Description
0xA0000000-0xDFFFFFFF	External device	Device	XN	External device memory.
0xE0000000-0xE00FFFFF	Private Peripheral Bus	Strongly- ordered	XN	This region includes the NVIC, system timer, and system control block. Only word accesses can be used in this region.
0xE0100000-0xFFFFFFFF	Device	Device	XN	Vendor specific

The Code, SRAM, and external RAM regions can hold programs.

4.3.4 Software Ordering of Memory Accesses

The order of instructions in the program flow does not always guarantee the order of the corresponding memory transactions. This is because:

- the processor can reorder some memory accesses to improve efficiency, providing this does not affect the behavior of the instruction sequence.
- memory or devices in the memory map have different wait states
- some memory accesses are buffered or speculative.

Memory system ordering of memory accesses in ***Chapter 4.3.2*** describes the cases where the memory system guarantees the order of memory accesses. Otherwise, if the order of memory accesses is critical, software must include memory barrier instructions to force that ordering. The processor provides the following memory barrier instructions:

DMB

The Data Memory Barrier (DMB) instruction ensures that outstanding memory transactions complete before subsequent memory transactions.

DSB

The Data Synchronization Barrier (DSB) instruction ensures that outstanding memory transactions complete before subsequent instructions execute.

ISB

The Instruction Synchronization Barrier (ISB) ensures that the effect of all completed memory transactions is recognizable by subsequent instructions.

4.3.5 Memory Endianness

The processor views memory as a linear collection of bytes numbered in ascending order from zero. For example, bytes 0-3 hold the first stored word, and bytes 4-7 hold the second stored word. ***Chapter 4.3.5.1*** describes how words of data are stored in memory.

4.3.5.1 Little-endian format

In little-endian format, the processor stores the least significant byte (lsbyte) of a word at the lowest-numbered byte, and the most significant byte (msbyte) at the highest-numbered byte. An example of the little-endian format is described in ***Figure 8***.

6 See Memory regions, types and attributes in ***Chapter 4.3.1*** for more information.

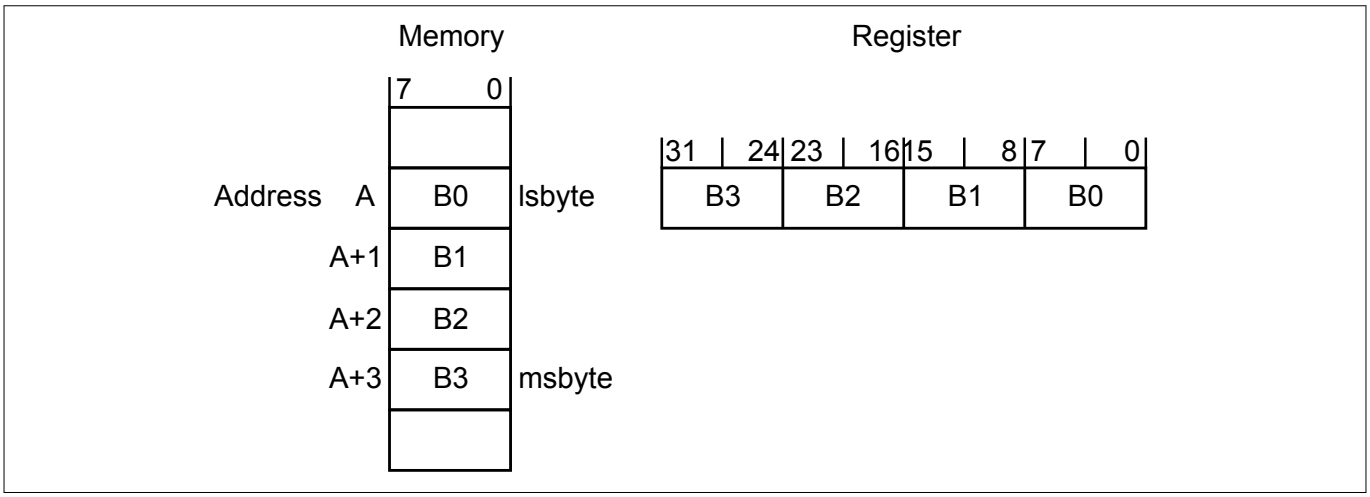


Figure 8 Little-endian format (Example)

4.4 Instruction Set

Table 11 lists the supported Cortex-M0 instructions. For more information on the instructions and operands, please refer to *[1]*.

Table 11 Cortex-M0 instructions

Mnemonic	Operands	Brief description	Flags
ADCS	{Rd,} Rn, Rm	Add with carry	N,Z,C,V
ADD{S}	{Rd,} Rn, <Rm|#imm>	Add	N,Z,C,V
ADR	Rd, label	PC-relative Address to Register	-
ANDS	{Rd,} Rn, Rm	Bitwise AND	N,Z
ASRS	{Rd,} Rm, <Rs|#imm>	Arithmetic Shift Right	N,Z,C
B{cc}	label	Branch {conditionally}	-
BICS	{Rd,} Rn, Rm	Bit Clear	N,Z
BKPT	#imm	Breakpoint	-
BL	label	Branch with Link	-
BLX	Rm	Branch indirect with Link	-
BX	Rm	Branch indirect	-
CMN	Rn, Rm	Compare Negative	N,Z,C,V
CMP	Rn, <Rm|#imm>	Compare	N,Z,C,V
CPSID	i	Change Processor State, Disable Interrupts	-
CPSIE	i	Change Processor State, Enable Interrupts	-
DMB	-	Data Memory Barrier	-
DSB	-	Data Synchronization Barrier	-
EORS	{Rd,} Rn, Rm	Exclusive OR	N,Z

Table 11 Cortex-M0 instructions (continued)

Mnemonic	Operands	Brief description	Flags
ISB	-	Instruction Synchronization Barrier	-
LDM	Rn{!}, reglist	Load Multiple registers, increment after	-
LDR	Rt, label	Load Register from PC-relative address	-
LDR	Rt, [Rn, <Rm|#imm>]	Load Register with word	-
LDRB	Rt, [Rn, <Rm|#imm>]	Load Reigster with byte	-
LDRH	Rt, [Rn, <Rm|#imm>]	Load Reigster with halfword	-
LDRSB	Rt, [Rn, <Rm|#imm>]	Load Reigster with signed byte	-
LDRSH	Rt, [Rn, <Rm|#imm>]	Load Reigster with signed halfword	-
LSLS	{Rd,} Rn, <Rs|#imm>	Logical Shift Left	N,Z,C
LSRS	{Rd,} Rn, <Rs|#imm>	Logical Shift Right	N,Z,C
MOV{S}	Rd, Rm	Move	N,Z
MRS	Rd, spec_reg	Move to general register from special register	-
MSR	spec_reg, Rm	Move to special register from general register	N,Z,C,V
MULS	Rd, Rn, Rm	Multiply, 32-bit result	N,Z
MVNS	Rd, Rm	Bitwise NOT	N,Z
NOP	-	No Operation	-
ORRS	{Rd,} Rn, Rm	Logical OR	N,Z
POP	reglist	Pop registers from stack	-
PUSH	reglist	Push registers onto stack	-
REV	Rd, Rm	Byte-Reverse word	-
REV16	Rd, Rm	Byte-Reverse packed halfwords	-
REVSH	Rd, Rm	Byte-Reverse signed halfword	-
RORS	{Rd,} Rn, Rs	Rotate Right	N,Z,C
RSBS	{Rd,} Rn, #0	Reverse Subtract	N,Z,C,V
SBCS	{Rd,} Rn, Rm	Subtract with Carry	N,Z,C,V
STM	Rn!, reglist	Store Multiple registers, increment after	-
STR	Rt, [Rn, <Rm|#imm>]	Store Register as word	-
STRB	Rt, [Rn, <Rm|#imm>]	Store Register as byte	-
STRH	Rt, [Rn, <Rm|#imm>]	Store Register as halfword	-
SUB{S}	{Rd,} Rn, <Rm|#imm>	Subtract	N,Z,C,V
SVC	#imm	Supervisor Call	-

Table 11 Cortex-M0 instructions (continued)

Mnemonic	Operands	Brief description	Flags
SXTB	Rd, Rm	Sign extend byte	-
SXTH	Rd, Rm	Sign extend halfword	-
TST	Rn, Rm	Logical AND based test	N,Z
UXTB	Rd, Rm	Zero extend a byte	-
UXTH	Rd, Rm	Zero extend a halfword	-
WFE	-	Wait for Event	-
WFI	-	Wait for Interrupt	-

4.4.1 Intrinsic Functions

ISO/IEC C code cannot directly access some Cortex-M0 instructions. The intrinsic functions that can generate these instructions, provided by the CMSIS and might be provided by a C compiler are described in ***Chapter 4.2.7***.

4.5 Exception Model

This section describes the exception model. It describes:

- Exception states (***Chapter 4.5.1***)
- Exception types (***Chapter 4.5.2***)
- Exception handlers (***Chapter 4.5.3***)
- Vector table (***Chapter 4.5.4***)
- Exception priorities (***Chapter 4.5.5***)
- Exception entry and return (***Chapter 4.5.6***)

4.5.1 Exception States

Each exception is in one of the following states:

Inactive

The exception is not active and not pending.

Pending

The exception is waiting to be serviced by the processor. An interrupt request from a peripheral or from software can change the state of the corresponding interrupt to pending.

Active

An exception that is being serviced by the processor but has not completed.

Note: An exception handler can interrupt the execution of another exception handler. In this case both exceptions are in the active state.

Active and pending

The exception is being serviced by the processor and there is a pending exception from the same source.

4.5.2 Exception Types

The exception types are described in ***Table 12***.

Table 12 Exception types

Exception Types	Descriptions
Reset	Reset is invoked on power up or a warm reset. The exception model treats reset as a special form of exception. When reset is asserted, the operation of the processor stops, potentially at any point in an instruction. When reset is deasserted, execution restarts from the address provided by the reset entry in the vector table. Execution restarts in Thread mode.
HardFault	A HardFault is an exception that occurs because of an error during normal or exception processing. HardFaults have a fixed priority of -1, meaning they have higher priority than any exception with configurable priority.
SVCall	A supervisor call (SVC) is an exception that is triggered by the SVC instruction. In an OS environment, applications can use SVC instructions to access OS kernel functions and device drivers.
PendSV	PendSV is an interrupt-driven request for system-level service. In an OS environment, use PendSV for context switching when no other exception is active.
SysTick	A SysTick exception is an exception the system timer generates when it reaches zero. Software can also generate a SysTick exception. In an OS environment, the processor can use this exception as system tick.
Interrupt (IRQ)	A interrupt, or IRQ, is an exception signalled by a peripheral, or generated by a software request. All interrupts are asynchronous to instruction execution. In the system, peripherals use interrupts to communicate with the processor.

Table 13 Properties of the different exception types

Exception number[7)]	IRQ number[7)]	Exception type	Priority	Vector address or offset[8)]	Activation
1	-	Reset	-3, the highest	0x00000004	Asynchronous
2	-	Reserved	-	-	-
3	-13	HardFault	-1	0x0000000C	Synchronous
4-10	-	Reserved	-	-	-
11	-5	SVCall	Configurable[9)]	0x0000002C	Synchronous
12-13	-	Reserved	-	-	-
14	-2	PendSV	Configurable[9)]	0x00000038	Asynchronous
15	-1	SysTick	Configurable[9)]	0x0000003C	Asynchronous
16 and above	0 and above	Interrupt (IRQ)	Configurable[9)]	0x00000040 and above[10)]	Asynchronous

7 To simplify the software layer, the CMSIS only uses IRQ numbers and therefore uses negative values for exceptions other than interrupts. The IPSR returns the Exception number, see ***Interrupt Program Status Register***.

8 See Vector table in ***Chapter 4.5.4*** for more information.

9 See Interrupt Priority Registers in Interrupt System chapter.

For an asynchronous exception, other than reset, the processor can execute additional instructions between when the exception is triggered and when the processor enters the exception handler.

Software can disable the exceptions in ***Table 13*** which have configurable priority, see Interrupt Clear-enable Register in Interrupt System chapter.

For more information about HardFaults, see Fault handling in ***Chapter 4.6***.

4.5.3 Exception Handlers

The processor handles exceptions using:

Interrupt Service Routines (ISRs)

Interrupts IRQ0 to IRQ31 are the exceptions handled by ISRs.

Fault handlers

HardFault is the only exception handled by the fault handler.

System handlers

PendSV, SVCall, SysTick, and the HardFault are all system exceptions that are handled by system handlers.

4.5.4 Vector Table

The vector table contains the reset value of the stack pointer, and the start addresses, also called exception vectors, for all exception handlers. ***Figure 9*** shows the order of the exception vectors in the vector table. The least-significant bit of each vector must be 1, indicating that the exception handler is written in Thumb code.

[10] Increasing in steps of 4.

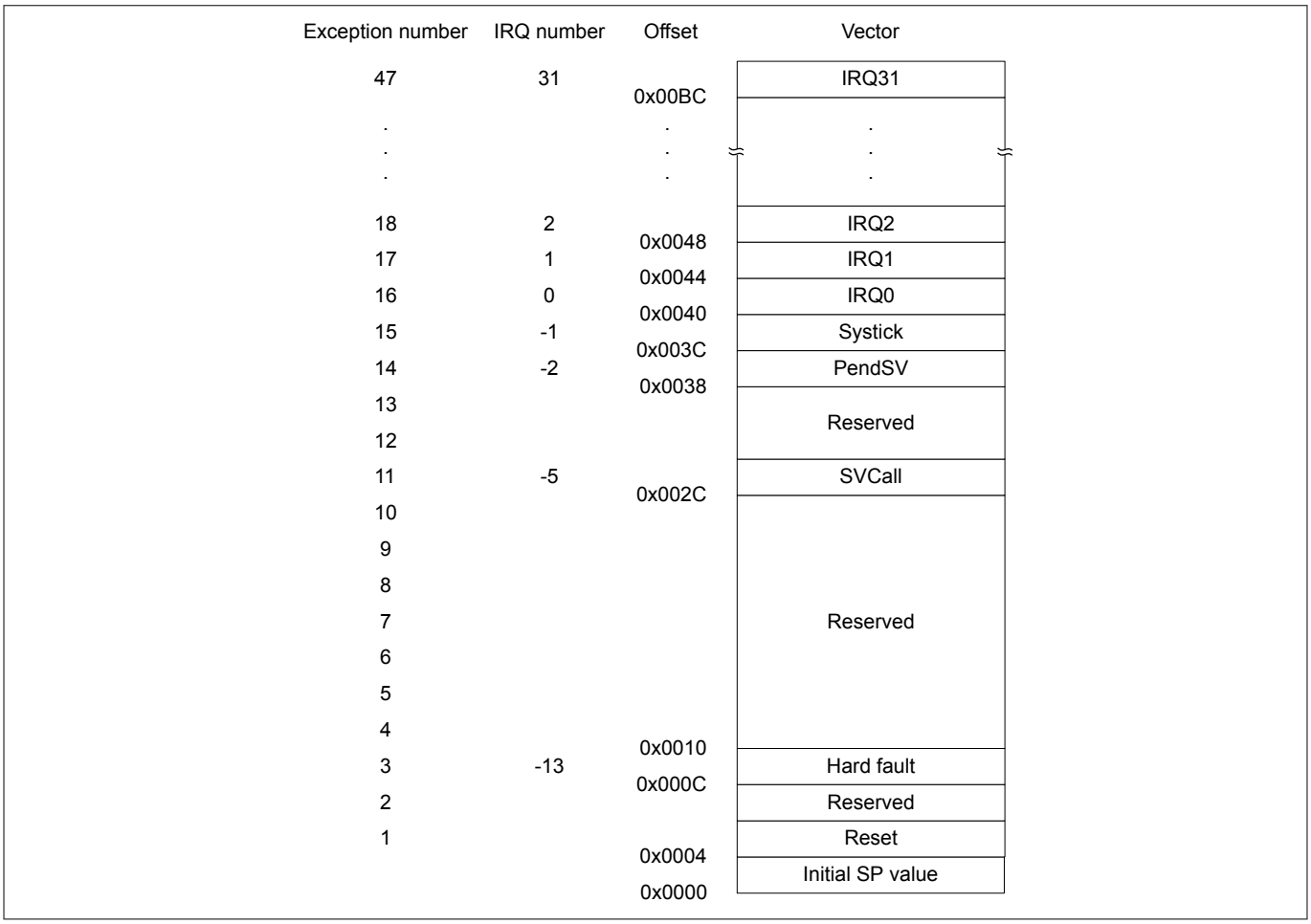


Figure 9 Vector table

The vector table is fixed at address 0x00000000.

4.5.4.1 Vector Table Remap

In IMC300A, the vector table is located inside the ROM. Therefore, the vector table is remapped to the SRAM based on the mapping shown in ***Table 14***. The user application uses these locations as entry points for the actual exception and interrupt handlers. This is done by placing the code for these handlers or having the branch instruction to the handlers there.

For example, upon an exception entry due to IRQ0, the processor reads the intermediate handler start address $2000'0040_H$ (fixed in ROM) from the vector table and starts execution from there. If the actual handler is located in another address location due to size contraints, the address $2000'0040_H$ should trigger a load and a branch instruction to jump to this new location.

Note: The user application needs to reserve the SRAM addresses $2000'000C_H$ - $2000'00BF_H$ for the remapped vector table if all vectors are used.

Table 14 Remapped Vector Table

Exception Number	IRQ Number	Vector	Default Vector Address	Remapped Vector Address
-	-	Initial SP Value	$0000'0000_H$	$1000'1000_H$

Table 14 Remapped Vector Table (continued)

Exception Number	IRQ Number	Vector	Default Vector Address	Remapped Vector Address
1	-	Reset	$0000'0004_H$	$1000'1004_H$ [11]
3	-13	HardFault	$0000'000C_H$	$2000'000C_H$
11	-5	SVCall	$0000'002C_H$	$2000'002C_H$
14	-2	PendSV	$0000'0038_H$	$2000'0038_H$
15	-1	SysTick	$0000'003C_H$	$2000'003C_H$
16-47	0-31	IRQn (n=0-31)	$0000'0040_H$ + (n*4)	$2000'0040_H$ + (n*4)

4.5.5 Exception Priorities

Table 13 shows that all exceptions have an associated priority, with:

- a lower priority value indicating a higher priority
- configurable priorities for all exceptions except Reset and HardFault.

If software does not configure any priorities, then all exceptions with a configurable priority have a priority of 0. For information about configuring exception priorities see

- System Handler Priority Registers ***SHPR2***, ***SHPR3***.
- Interrupt Priority Registers in Interrupt System chapter.

Note: Configurable priority values are in the range 0-192, in steps of 64. This means that the Reset and HardFault exceptions, with fixed negative priority values, always have higher priority than any other exception.

For example, assigning a higher priority value to IRQ[0] and a lower priority value to IRQ[1] means that IRQ[1] has higher priority than IRQ[0]. If both IRQ[1] and IRQ[0] are asserted, IRQ[1] is processed before IRQ[0].

If multiple pending exceptions have the same priority, the pending exception with the lowest exception number takes precedence. For example, if both IRQ[0] and IRQ[1] are pending and have the same priority, then IRQ[0] is processed before IRQ[1].

When the processor is executing an exception handler, the exception handler is preempted if a higher priority exception occurs. If an exception occurs with the same priority as the exception being handled, the handler is not preempted, irrespective of the exception number. However, the status of the new interrupt changes to pending.

4.5.6 Exception Entry and Return

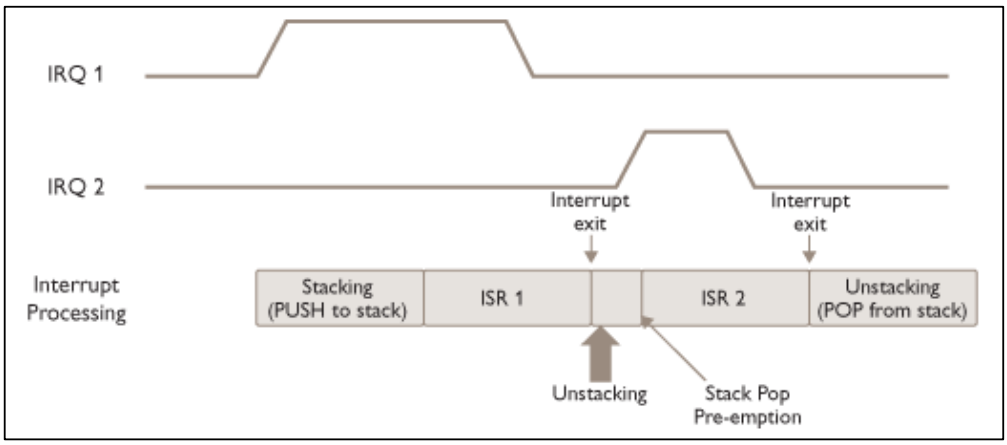
Exception handling can be described using the following terms:

Preemption

When the processor is executing an exception handler, an exception can preempt the exception handler if its priority is higher than the priority of the exception being handled.

When one exception preempts another, the exceptions are called nested exceptions. See Exception entry in ***Chapter 4.5.6.1*** for more information.

11 The remapped reset vector address refers to the location (start of the Flash memory) that the startup software jumps to upon exiting the startup sequence in user mode.



Source of figure *[8]*.

Return

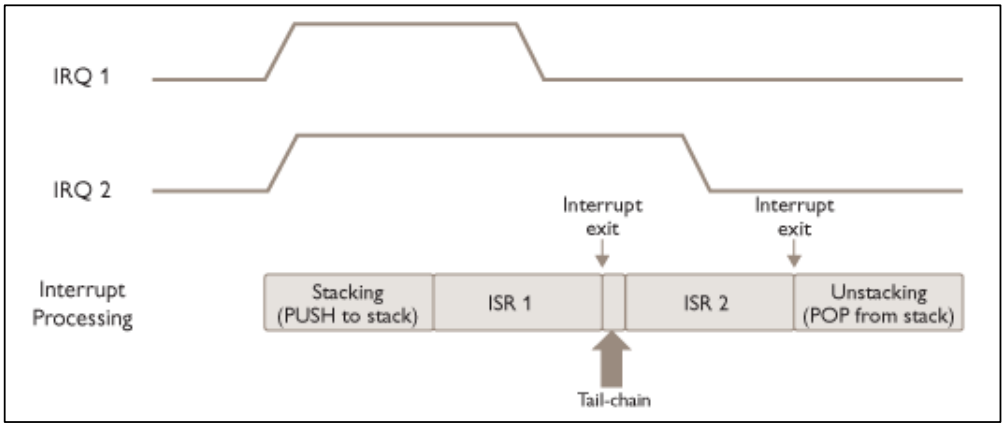
This occurs when the exception handler is completed, and:

- there is no pending exception with sufficient priority to be serviced
- the completed exception handler was not handling a late-arriving exception.

The processor pops the stack and restores the processor state to the state it had before the interrupt occurred. See Exception return in ***Chapter 4.5.6.2*** for more information.

Tail-chaining

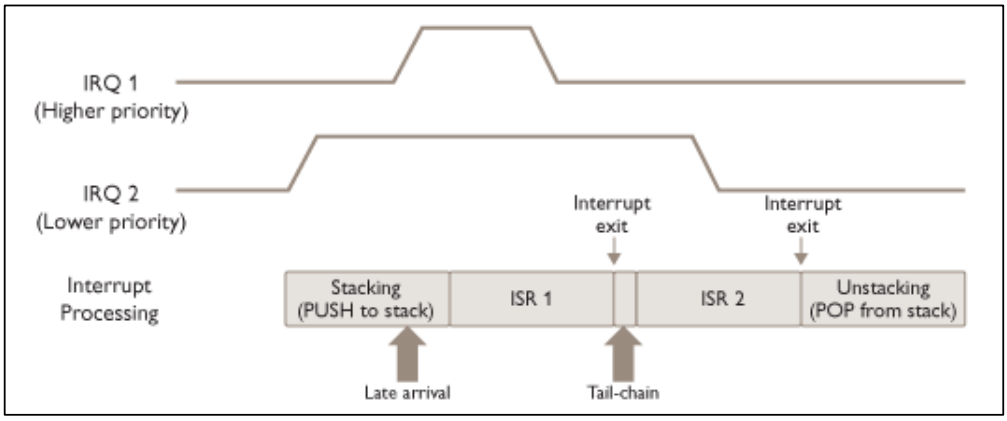
This mechanism speeds up exception servicing. On completion of an exception handler, if there is a pending exception that meets the requirements for exception entry, the stack pop is skipped and control transfers to the new exception handler.



Source of figure *[8]*.

Late-arriving

This mechanism speeds up preemption. If a higher priority exception occurs during state saving for a previous exception, the processor switches to handle the higher priority exception and initiates the vector fetch for that exception. State saving is not affected by late arrival because the state saved is the same for both exceptions. On return from the exception handler of the late-arriving exception, the normal tail-chaining rules apply.



Source of figure *[8]*.

4.5.6.1 Exception entry

Exception entry occurs when there is a pending exception with sufficient priority and either:

- the processor is in Thread mode
- the new exception is of higher priority than the exception being handled, in which case the new exception preempts the original exception.

When one exception preempts another, the exceptions are nested.

Sufficient priority means the exception has greater priority than any limits set by the mask register, see ***Exception mask registers***. An exception with less priority than this is pending but is not handled by the processor.

When the processor takes an exception, unless the exception is a tail-chained or a late-arriving exception, the processor pushes information onto the current stack. This operation is referred to as stacking and the structure of eight data words is referred as a stack frame. The stack frame contains the following information, as illustrated in ***Figure 10***.

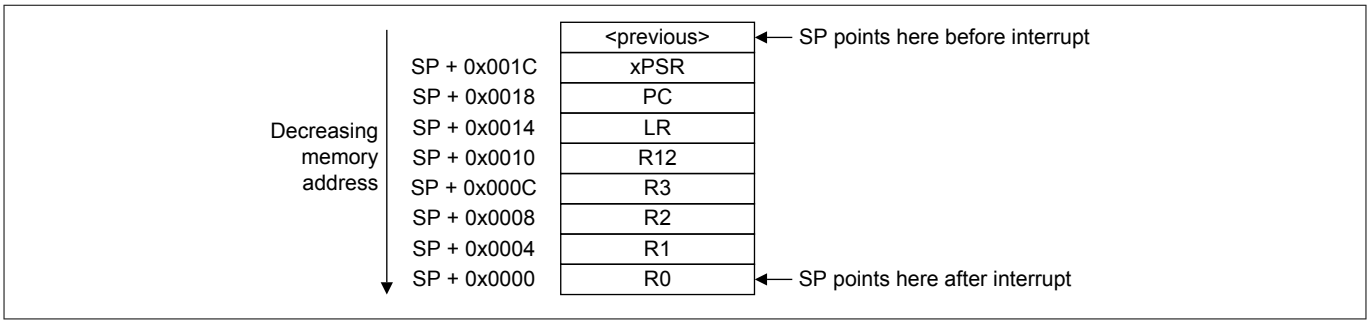


Figure 10 Exception stack frame

Immediately after stacking, the stack pointer indicates the lowest address in the stack frame. The stack frame is aligned to a double-word address.

The stack frame includes the return address. This is the address of the next instruction in the interrupted program. This value is restored to the PC at exception return so that the interrupted program resumes.

The processor performs a vector fetch that reads the exception handler start address from the vector table. When stacking is complete, the processor starts executing the exception handler. At the same time, the processor writes an EXC_RETURN value to the LR. This indicates which stack pointer corresponds to the stack frame and what operation mode the processor was in before the entry occurred.

If no higher priority exception occurs during exception entry, the processor starts executing the exception handler and automatically changes the status of the corresponding pending interrupt to active.

If another higher priority exception occurs during exception entry, the processor starts executing the exception handler for this exception and does not change the pending status of the earlier exception. This is the late arrival case.

4.5.6.2 Exception return

Exception return occurs when the processor is in Handler mode and execution of one of the following instructions attempts to set the PC to an EXC_RETURN value:

- a POP instruction that loads the PC
- a BX instruction using any register.

The processor saves an EXC_RETURN value to the LR on exception entry. The exception mechanism relies on this value to detect when the processor has completed an exception handler. Bits [31:4] of an EXC_RETURN value are set to 1. When this value is loaded into the PC, the processor detects that the exception is complete, and starts the exception return sequence. Bits [3:0] of the EXC_RETURN value indicate the required return stack and processor mode. ***Table 15*** shows the EXC_RETURN values with description of the exception return behavior.

Table 15 Exception return behavior

EXC_RETURN[31:0]	Description
0xFFFFFFF1	Return to Handler mode. Exception return gets state from the main stack. Execution uses MSP after return.
0xFFFFFFF9	Return to Thread mode. Exception return gets state from MSP. Execution uses MSP after return.
0xFFFFFFFD	Return to Thread mode. Exception return gets state from the PSP. Execution uses PSP after return.
All other values	Reserved.

4.6 Fault Handling

Faults are a subset of the exceptions, see Exception model in ***Chapter 4.5***. All faults result in the HardFault exception being taken or cause lockup if they occur in the HardFault handler. The faults are:

- execution of an SVC instruction at a priority equal or higher than SVCall
- execution of a BKPT instruction without a debugger attached
- a system-generated bus error on a load or store
- execution of an instruction from an XN memory address
- execution of an instruction from a location for which the system generates a bus fault
- a system-generated bus error on a vector fetch
- execution of an undefined instruction
- execution of an instruction when not in Thumb-State as a result of the T-bit being previously cleared to 0
- an attempted load or store to an unaligned address

Note: Only Reset can preempt the fixed priority HardFault handler. A HardFault can preempt any exception other than Reset, or another hard fault.

4.6.1 Lockup

The processor enters a lockup state if a fault occurs when executing the HardFault handlers, or if the system generates a bus error when unstacking the PSR on an exception return using the MSP. When the processor is in lockup state it does not execute any instructions. The processor remains in lockup state until one of the following occurs:

- it is reset
- it is halted by a debugger

4.7 Power Management

The Cortex-M0 processor sleep modes reduce power consumption:

- Sleep mode
- Deep sleep mode

The SLEEPDEEP bit of the SCR selects which sleep mode is used, see System Control Register ***SCR***.

This section describes the mechanisms for entering sleep mode, and the conditions for waking up from sleep mode.

4.7.1 Entering Sleep Mode

This section describes the mechanisms software can use to put the processor into sleep mode.

The system can generate spurious wakeup events, for example a debug operation wakes up the processor. Therefore software must be able to put the processor back into sleep mode after such an event. A program might have an idle loop to put the processor back to sleep mode.

Wait for interrupt

The wait for interrupt instruction, WFI, causes immediate entry to sleep mode. When the processor executes a WFI instruction it stops executing instructions and enters sleep mode.

Wait for event

The wait for event instruction, WFE, causes entry to sleep mode depending on the value of a one-bit event register. When the processor executes a WFE instruction, it checks the value of the event register:

0: The processor stops executing instructions and enters sleep mode.

1: The processor clears the register to 0 and continues executing instructions without entering sleep mode.

If the event register is 1, this indicate that the processor must not enter sleep mode on execution of a WFE instruction. Typically, this is because an external event is asserted. Software cannot access this register directly.

Sleep-on-exit

If the SLEEPONEXIT bit of the SCR is set to 1, when the processor completes the execution of an exception handler and returns to Thread mode, it immediately enters sleep mode. This mechanism is used in applications that only require the processor to run when an interrupt occurs.

4.7.2 Wakeup from Sleep Mode

The conditions for the processor to wakeup depend on the mechanism that caused it to enter sleep mode.

Wakeup from WFI or Sleep-on-exit

The following events are WFI wake-up events:

- reset event

- debug event, if debug is enabled
- exception at a priority that would preempt any currently active exceptions, if PRIMASK was set to 0

*Note: If PRIMASK is set to 1, an interrupt or exception that has a higher priority than the current exception priority will cause the processor to wake up. Interrupt handler is not executed until the processor sets PRIMASK to 0. For more information about PRIMASK, see **Exception mask registers**.*

Wakeup from WFE

The following events are WFE wake-up events:

- reset event
- exception or interrupt with sufficient priority to cause exception entry
- exception or interrupt entering pending state, if SEVONPEND is set to 1 (See ***SCR***)
- debug event, if debug is enabled

*Note: Wakeup by Event Register (see The Event Register in **[2]**) is not possible in IMC300A. Nevertheless, SEV instruction will set the event register.*

4.7.3 Power Management Programming Hints

ISO/IEC C cannot directly generate the WFI and WFE instructions. The CMSIS provides the following functions for these instructions:

```
void __WFE(void) // Wait for Event
void __WFI(void) // Wait for Interrupt
```

4.8 Private Peripherals

The following sections are the reference material for the ARM Cortex-M0 core peripherals.

4.8.1 About the Private Peripherals

The address map of the Private Peripheral Bus (PPB) is:

Table 16 Core peripheral register regions

Address	Core peripheral	Description
0xE000E008-0xE000E00F	System Control Block	See ***Chapter 4.8.2*** and ***Chapter 4.9.1.6***
0xE000E010-0xE000E01F	System timer	See ***Chapter 4.8.3*** and ***Chapter 4.9.2***
0xE000E100-0xE000E4EF	Nested Vectored Interrupt Controller	See Interrupt System chapter
0xE000ED00-0xE000ED3F	System Control Block	See ***Chapter 4.8.2*** and ***Chapter 4.9.1.6***
0xE000EF00-0xE000EF03	Nested Vectored Interrupt Controller	See Interrupt System chapter

4.8.2 System control block

The System Control Block (SCB) provides system implementation information, and system control. This includes configuration, control, and reporting of the system exceptions.

4.8.2.1 System control block usage hints and tips

Ensure software uses aligned 32-bit word size transactions to access all the system control block registers.

4.8.3 System timer, SysTick

The processor has a 24-bit system timer, SysTick, that counts down from the reload value to zero, reloads, that is wraps to, the value in the SYST_RVR register on the next clock cycle, then counts down on subsequent clock cycles.

Note: When the processor is halted for debugging the counter does not decrement.

4.8.3.1 SysTick usage hints and tips

The interrupt controller clock updates the SysTick count. When processor clock is selected and the clock signal is stopped for low power mode, the SysTick counter stops. When external clock is selected, the clock continues to run in low power mode and SysTick can be used as a wakeup source.

Ensure software uses aligned word accesses to access the SysTick registers.

If the SysTick counter reload and current value are undefined at reset, the correct initialization sequence for the SysTick counter is:

1. Program reload value.
2. Clear current value.
3. Program Control and Status register.

4.9 PPB Registers

The CPU private peripherals registers base address is $E000E000_H$.

Table 17 Register Overview

Short Name	Description	Offset Address	Access Mode		Description see
			Read	Write	
System Control Space (SCS)					
CPUID	CPUID Base Register	$D00_H$	PV, 32	PV, 32	Page 77
ICSR	Interrupt Control and State Register	$D04_H$	PV, 32	PV, 32	Page 78
AIRCR	Application Interrupt and Reset Control Register	$D0C_H$	PV, 32	PV, 32	Page 79
SCR	System Control Register	$D10_H$	PV, 32	PV, 32	Page 80
CCR	Configuration and Control Register	$D14_H$	PV, 32	PV, 32	Page 81
SHPR2	System Handler Priority Register 2	$D1C_H$	PV, 32	PV, 32	Page 83

Table 17 Register Overview (continued)

Short Name	Description	Offset Address	Access Mode		Description see
			Read	Write	
SHPR3	System Handler Priority Register 3	$D20_H$	PV, 32	PV, 32	Page 83
SHCSR	System Handler Control and State Register	$D24_H$	PV, 32	PV, 32	Page 84
System Timer (SysTick)					
SYST_CSR	SysTick Control and Status Register	010_H	PV, 32	PV, 32	Page 84
SYST_RVR	SysTick Reload Value Register	014_H	PV, 32	PV, 32	Page 85
SYST_CVR	SysTick Current Value Register	018_H	PV, 32	PV, 32	Page 86
SYST_CALIB	SysTick Calibration Value Register	$01C_H$	PV, 32	-	Page 87

4.9.1 SCS Registers

4.9.1.1 Register CPUID

The CPUID register contains the processor part number, version, and implementation information.

CPUID Address: $E000ED00_H$

CPUID Base Register Reset Value: $410CC200_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Implementer								**Variant**				**Architecture**			
r								r				r			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PartNo												**Revision**			
r												r			

Field	Bits	Type	Description
Revision	3:0	r	**Revision Number**
PartNo	15:4	r	**Part Number of the Processor**
Architecture	19:16	r	**Architecture**
Variant	23:20	r	**Variant Number**
Implementer	31:24	r	**Implementer Code**

4.9.1.2 Register ICSR

The ICSR:

- provides:
  - set-pending and clear-pending bits for the PendSV and SysTick exceptions
- indicates:
  - the exception number of the exception being processed
  - whether there are preempted active exceptions
  - the exception number of the highest priority pending exception
  - whether any interrupts are pending.

ICSR Address: $E000ED04_H$

Interrupt Control and State Register Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0			PENDSVSET	PENDSVCLR	PENDSTSET	PENDSTCLR	0		ISRPENDING	0				VECTPENDING	
r			rw	w	rw	w	r		r	r				r	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VECTPENDING				0						VECTACTIVE[12)]					
r				r						r					

Field	Bits	Type	Description
VECTACTIVE[13)]	5:0	r	**Active Exception Number** Non-zero value The exception number of the currently active exception. *Note: Subtract 16 from this value to obtain the CMSIS IRQ number required to index into the Interrupt Clear-Enable, Set-Enable, Clear-Pending, Set-Pending, or Priority Registers, see **Interrupt Program Status Register**.*
0	11:6	r	**Reserved** Read as 0; should be written with 0.
VECTPENDING	17:12	r	**Pending Exception Number** Indicates the exception number of the highest priority pending enabled exception. Non-zero value: The exception number of the highest priority pending enabled exception.

12 This is the same value as IPSR bits[5:0], see ***Interrupt Program Status Register***

13 This is the same value as IPSR bits[5:0], see ***Interrupt Program Status Register***

(continued)

Field	Bits	Type	Description
0	21:18	r	**Reserved** Read as 0; should be written with 0.
ISRPENDING	22	r	**Interrupt Pending Flag** This bit sets the interrupt pending flag, excluding faults. 0_B Interrupt not pending 1_B Interrupt pending.
0	24:23	r	**Reserved** Read as 0; should be written with 0.
PENDSTCLR	25	w	**SysTick Exception Clear-pending** 0_B No effect 1_B removes the pending state from the SysTick exception. This bit is write-only. On a register read, this value is unknown.
PENDSTSET	26	rw	**SysTick Exception Set-pending** 0_D SysTick exception is not pending 1_D SysTick exception is pending. A write of 0 to the bit has no effect.
PENDSVCLR	27	w	**PendSV Clear Pending** This bit clears a pending PendSV exception. 0_B Do not clear. 1_B Removes pending state from PendSV exception.
PENDSVSET	28	rw	**PendSV Set Pending** This bit sets a pending PendSV exception or reads back the current state. 0_B PendSV exception is not pending. 1_B PendSV excepton is pending. *Note: Writing 1 to this bit is the only way to set the PendSV exception state to pending.* A software write of 0 to the bit has no effect.
0	31:29	r	**Reserved** Read as 0; should be written with 0.

Notes:
The result is unpredictable if:

1. *Both PENDSVSET and PENDSVCLR bits are set to 1.*
2. *Both PENDSTSET and PENDSTCLR bits are set to 1.*

4.9.1.3 Register AIRCR

The AIRCR register provides endian status for data accesses and reset control of the system. To write to this register, you must write 0x5FA to the VECTKEY field, otherwise the processor ignores the write.

AIRCR Address: $E000ED0C_H$

Application Interrupt and Reset Control Register Reset Value: $FA050000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VECTKEY															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENDIANNESS	**0**												**SYSRESETREQ**	**0**	**0**
r	r												w	w	r

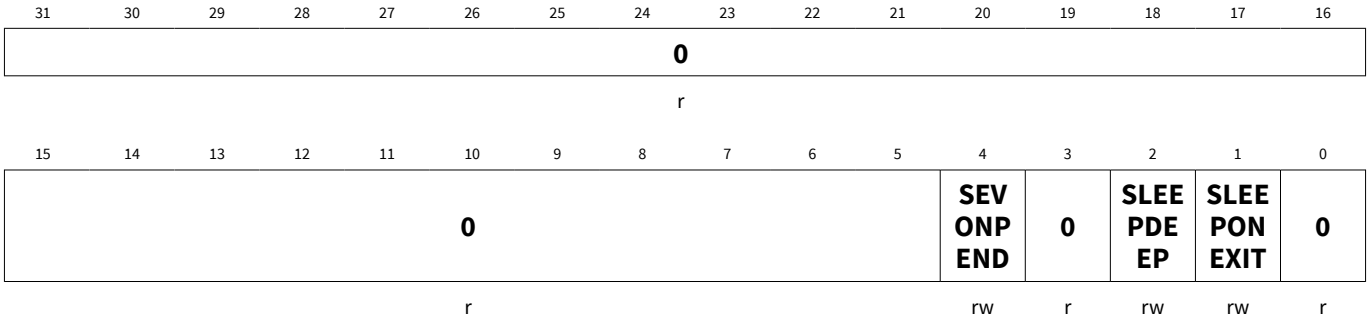
Field	Bits	Type	Description
0	0	r	**Reserved** Read as 0; should be written with 0.
0	1	w	**Reserved** Must be written with 0.
SYSRESETREQ	2	w	**System Reset Request** 0_B No effect. 1_B Requests a system level reset. This bit is read as 0.
0	14:3	r	**Reserved** Read as 0; should be written with 0.
ENDIANNESS	15	r	**Data Endianness**
VECTKEY	31:16	rw	**Register Key** Reads as unknown. On writes, write 0x5FA to VECTKEY, otherwise the write is ignored.

4.9.1.4 Register SCR

The SCR controls features of entry to and exit from low power state.

SCR Address: $E000ED10_H$

System Control Register Reset Value: 00000000_H



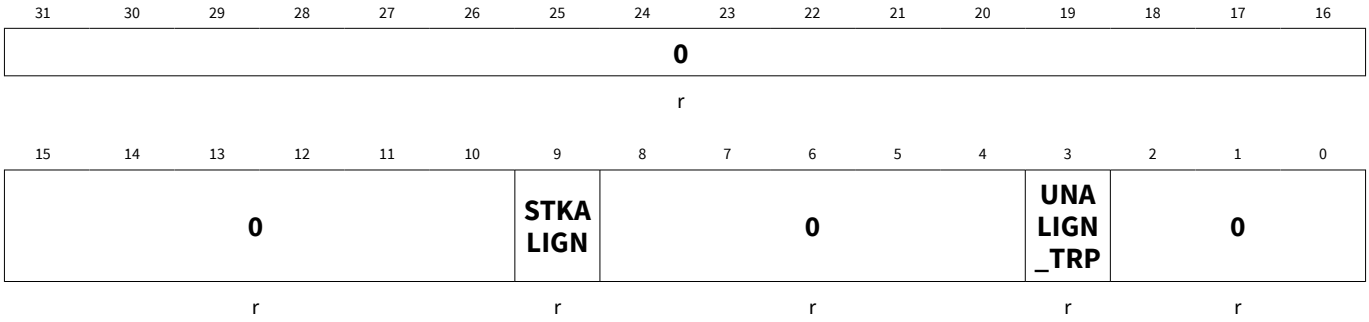
Field	Bits	Type	Description
0	0	r	**Reserved** Read as 0; should be written with 0.
SLEEPONEXIT	1	rw	**Sleep-on-exit** This bit indicates sleep-on-exit when returning from Handler mode to Thread mode. 0_B Do not sleep when returning to Thread mode. 1_B Enter sleep, or deep sleep, on return from an ISR to Thread mode. Setting this bit to 1 enables an interrupt driven application to avoid returning to an empty main application.
SLEEPDEEP	2	rw	**Low Power Sleep Mode** This bit controls whether the processor uses sleep or deep sleep as its low power mode. 0_B Sleep 1_B Deep sleep
0	3	r	**Reserved** Read as 0; should be written with 0.
SEVONPEND	4	rw	**Send Event on Pending bit** 0_B Only enabled interrupts or events can wakeup the processor, disabled interrupts are excluded. 1_B Enabled events and all interrupts, including disabled interrupts, can wakeup the processor. When an event or interrupt enters pending state, the event signal wakes up the processor from WFE. If the processor is not waiting for an event, the event is registered and affects the next WFE.
0	31:5	r	**Reserved** Read as 0; should be written with 0.

4.9.1.5 Register CCR

The CCR is a read-only register and it indicates some aspects of the behavior of the Cortex-M0 processor.

CCR Address: $E000ED14_H$

Configuration and Control Register Reset Value: 00000208_H



Field	Bits	Type	Description
0	2:0	r	**Reserved** Read as 0; should be written with 0.
UNALIGN_TRP	3	r	**Unaligned Access Traps** This bit always reads as 1, indicates that all unaligned accesses generate a HardFault.
0	8:4	r	**Reserved** Read as 0; should be written with 0.
STKALIGN	9	r	**Stack Alignment** This bit always reads as 1, indicates 8-byte stack alignment on exception entry. On exception entry, the processor uses bit [9] of the stacked PSR to indicate the stack alignment. On return from the exception, it uses this stacked bit to restore the correct stack alignment.
0	31:10	r	**Reserved** Read as 0; should be written with 0.

4.9.1.6 System Handler Priority Registers

The SHPR2-SHPR3 registers set the priority level, 0 to 192, of the exception handlers that have configurable priority.

SHPR2-SHPR3 are word accessible. To access to the system exception priority level using CMSIS, the following CMSIS functions are used:

- `uint32_t NVIC_GetPriority(IRQn_Type IRQn)`
- `void NVIC_SetPriority(IRQn_Type IRQn, uint32_t priority)`

The system fault handlers, the priority field and register for each handler are:

Table 18 System fault handler priority fields

Handler	Field	Register description
SVCall	PRI_11	System Handler Priority Register 2 on page *83*
PendSV	PRI_14	System Handler Priority Register 3 on page *83*
SysTick	PRI_15	

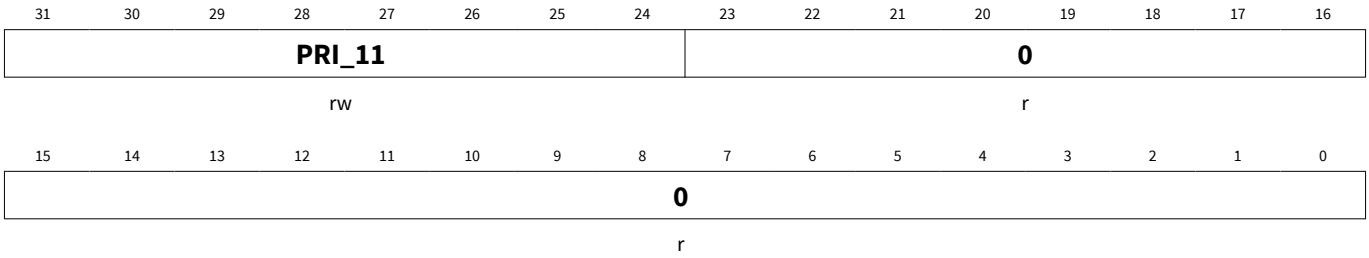
Each PRI_N field is 8 bits wide, but the IMC300A implements only bits [7:6] of each field, and bits [5:0] read as zero and ignore writes.

4.9.1.6.1 Register SHPR2

The SHPR2 register sets the priority level for the SVCall handler.

SHPR2 Address: $E000ED1C_H$

System Handler Priority Register 2 Reset Value: 00000000_H



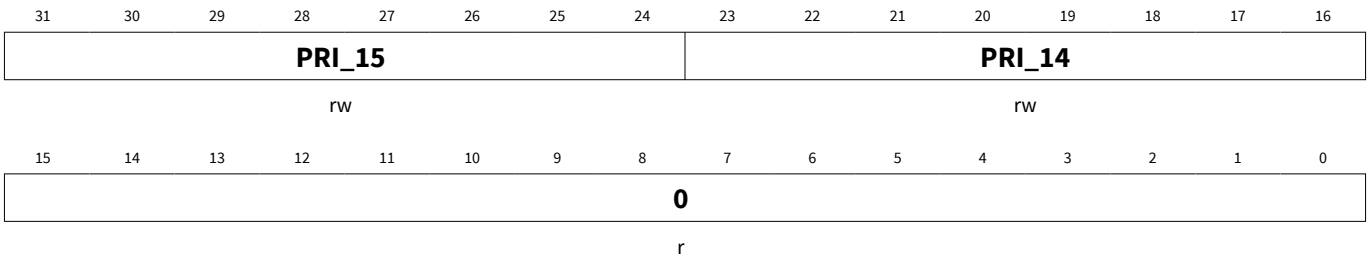
Field	Bits	Type	Description
0	23:0	r	**Reserved** Read as 0; should be written with 0.
PRI_11	31:24	rw	**Priority of System Handler 11** SVCall.

4.9.1.6.2 Register SHPR3

The SHPR3 register sets the priority level for the PendSV and SysTick handlers.

SHPR3 Address: $E000ED20_H$

System Handler Priority Register 3 Reset Value: 00000000_H



Field	Bits	Type	Description
0	15:0	r	**Reserved** Read as 0; should be written with 0.
PRI_14	23:16	rw	**Priority of System Handler 14** PendSV.
PRI_15	31:24	rw	**Priority of System Handler 15** SysTick exception.

4.9.1.7 Register SHCSR

The SHCSR register controls and provides the status of system handlers.

SHCSR Address: $E000ED24_H$

System Handler Control and State Register Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SVCALLPENDED	0														
rw	r														

Field	Bits	Type	Description
0	14:0	r	**Reserved** Read as 0; should be written with 0.
SVCALLPENDED	15	rw	**SVCall Pending bit** This bit reflects the pending state on a read, and updates the pending state, to the value written, on a write. 0_B SVCall is not pending. 1_B SVCall is pending[14].
0	31:16	r	**Reserved** Read as 0; should be written with 0.

4.9.2 SysTick Registers

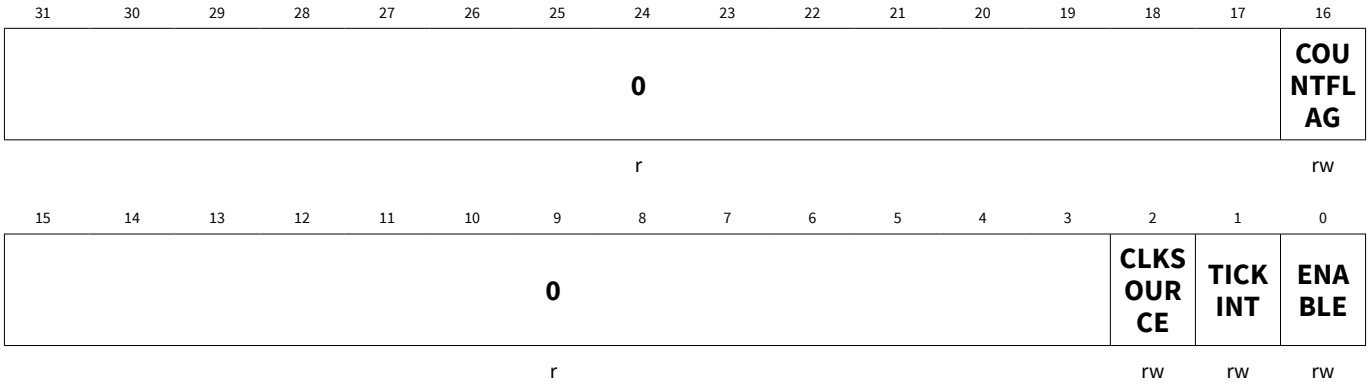
4.9.2.1 Register SYST_CSR

The SYST_CSR register enables the SysTick features.
Reading SYST_CSR clears the COUNTFLAG bit to 0.

SYST_CSR Address: $E000E010_H$

SysTick Control and Status Register Reset Value: 00000000_H

14 Pending state bits are set to 1 when an exception occurs, and are cleared to 0 when an exception becomes active.



Field	Bits	Type	Description
ENABLE	0	rw	**Counter Enable** This bit enables the counter. 0_B Counter disabled. 1_B Counter enabled.
TICKINT	1	rw	**SysTick Exception Request** This bit enables the SysTick exception request. 0_B Counting down to zero does not assert the SysTick exception request. 1_B Counting down to zero to assert the SysTick exception request. In software, COUNTFLAG bit can be used to determine if SysTick has counted to zero.
CLKSOURCE	2	rw	**Clock Source** This bit selects the SysTick timer clock source. 0_B External clock[15]. 1_B Processor clock.
0	15:3	r	**Reserved** Read as 0; should be written with 0.
COUNTFLAG	16	rw	**Counter Flag** This bit returns 1 if timer counted to 0 since the last read of this register.
0	31:17	r	**Reserved** Read as 0; should be written with 0.

When ENABLE is set to 1, the counter loads the RELOAD value from the SYST_RVR register and then counts down. On reaching 0, it sets the COUNTFLAG to 1 and optionally asserts the SysTick depending on the value of TICKINT. It then loads the RELOAD value again, and begins counting.

4.9.2.2 Register SYST_RVR

The SYST_RVR register specifies the start value to load into the SYST_CVR register.

15 In IMC300A, the external clock refers to the on-chip 32 kHz standby clock.

SYST_RVR Address: $E000E014_H$

SysTick Reload Value Register Reset Value: XXXXXXXX_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0								**RELOAD**							
r								rw							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RELOAD															
rw															

Field	Bits	Type	Description
RELOAD	23:0	rw	**Reload Value** This field sets the value to load into the SYST_CVR register when the counter is enabled and when it reaches 0.
0	31:24	r	**Reserved** Read as 0; should be written with 0.

Notes:
Calculating the RELOAD value:

1. *The RELOAD value can be any value in the range 0x00000001-0x00FFFFFF. A start value of 0 is possible, but this has no effect because the SysTick exception request and COUNTFLAG are activated when counting from 1 to 0.*
2. *The RELOAD value is calculated according to its use. For example, to generate a multi-shot timer with a period of N processor clock cycles, use a RELOAD value of N-1. If the SysTick interrupt is required every 100 clock pulses, set RELOAD to 99.*

4.9.2.3 Register SYST_CVR

The SYST_CVR register contains the current value of the SysTick counter.

Writing to the SYST_CVR clears the register and the COUNTFLAG status bit to 0. The write does not trigger the SysTick exception logic. Reading the register returns its value at the time it is accessed.

SYST_CVR Address: $E000E018_H$

SysTick Current Value Register Reset Value: XXXXXXXX_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0								**CURRENT**							
r								rw							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CURRENT															
rw															

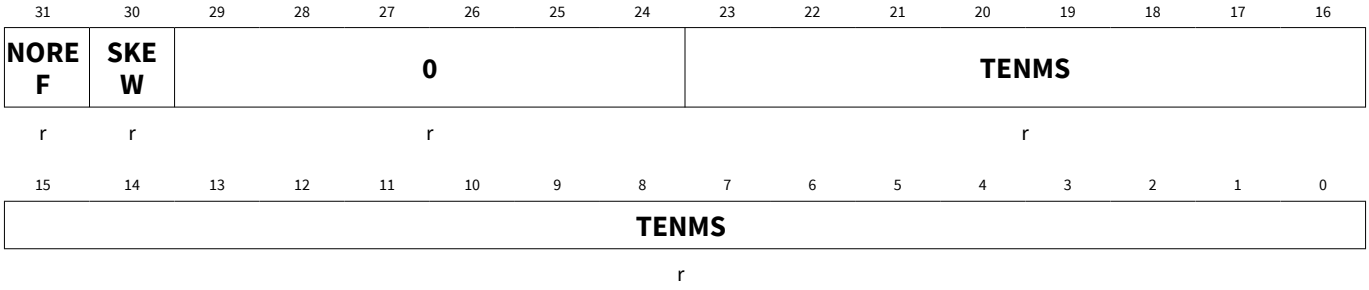
Field	Bits	Type	Description
CURRENT	23:0	rw	**SysTick Counter Current Value** When read, it returns the current value of the SysTick counter. A write of any value clears the field to 0, and also clears the SYST_CSR.COUNTFLAG bit to 0.
0	31:24	r	**Reserved** Read as 0; should be written with 0.

4.9.2.4 Register SYST_CALIB

The SYST_CALIB register indicates the SysTick calibration properties.

SYST_CALIB Address: $E000E01C_H$

SysTick Calibration Value Register Reset Value: 40000147_H



Field	Bits	Type	Description
TENMS	23:0	r	**10 Milliseconds** The reload value for 10ms timing is subject to system clock skew errors. The default value of TENMS is 0x000147.
0	29:24	r	**Reserved** Read as 0; should be written with 0.
SKEW	30	r	**Clock Skew** This bit is read as 1. It indicates that 10ms calibration value is inexact, because of the clock frequency.
NOREF	31	r	**Reference Clock** This bit is read as 0. It indicates that external reference clock is provided.

5 MATH Coprocessor (MATH)

5.1 Overview

The Math Coprocessor (MATH) module comprises of two independent sub-blocks to support the CPU in math-intensive computations: a Divider Unit (DIV) for signed and unsigned 32-bit division operations and a CORDIC (COrdinate Rotation DIgital Computer) Coprocessor for computation of trigonometric, linear or hyperbolic functions.

5.1.1 Features

The Math Coprocessor includes the following features:

- Divide function with operand pre-processing and result post-processing
- CORDIC Coprocessor for computation of trigonometric, hyperbolic and linear functions
- Supports kernel clock to interface clock ratio of 2:1 for faster execution
- Supports result chaining between the Divider Unit and CORDIC Coprocessor

5.1.2 Block Diagram

Figure 11 shows a block diagram of the Math Coprocessor.

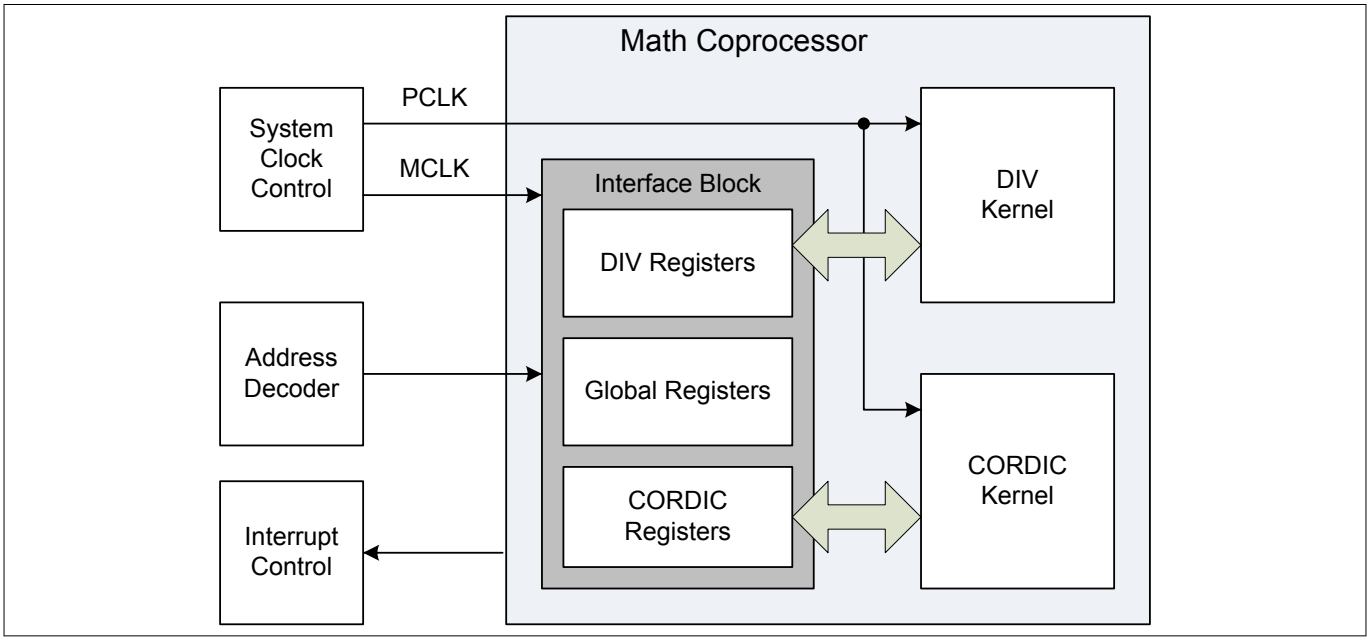


Figure 11 Math Coprocessor Block Diagram

5.2 Divider Unit (DIV)

5.2.1 Features

The DIV supports the following features:

- Signed/unsigned division operation in 35 kernel clock cycles
- Three division modes:
  - 32-bit divide by 32-bit

  - 32-bit divide by 16-bit
  - 16-bit divide by 16-bit
- Operands pre-processing with configurable number of:
  - Left shifts for dividend
  - Right shifts for divisor
- Result post-processing with configurable number of shifts and shift direction

Note: The execution time of 35 kernel clock cycles for a division operation does not include the time to access the operand and result registers, which takes an additional part of the time for a division function in the application software.

5.2.2 Division Operation

The DIV supports the truncated division operation, which is also the ISO C99 standard and the popular choice among modern processors. The division and modulus functions of the truncated division are related in the following way:

If q = D div d

and r = D mod d

then D = q * d + r

and | r | < | d |

where “D” is the dividend, “d” is the divisor, “q” is the quotient and “r” is the remainder. The truncated division rounds the quotient towards zero and the sign of its remainder is always the same as that of its dividend, i.e., sign (r) = sign (D).

To execute a divider operation with the DIV, it is first required to configure the division as follows:

- Signed or unsigned through the DIVCON.USIGN bit
- Division mode through the DIVCON.DIVMODE bits
- Start mode through the DIVCON.STMODE bit

The dividend and divisor values are then written into the DVD and DVS registers. The division is started with the write to DVS register or by setting the start bit DIVCON.ST, depending on the start mode. If the ST bit is used, the bit is automatically cleared in the next kernel clock cycle. The start of the division operation sets the busy flag, DIVST.BSY.

The division operation always takes 35 kernel clock cycles, and upon completion, the quotient and remainder values will be available at the QUOT and RMD registers, and the BSY flag will be cleared. The end of calculation event sets the Divider event flag EVFR.DIVEOC and can trigger an interrupt request to NVIC if enabled through the EVIER.DIVEOCIEN bit. The flag is cleared only by a software write to the EVFCR.DIVEOCC bit.

Figure 12 shows the timing diagram for a division operation.

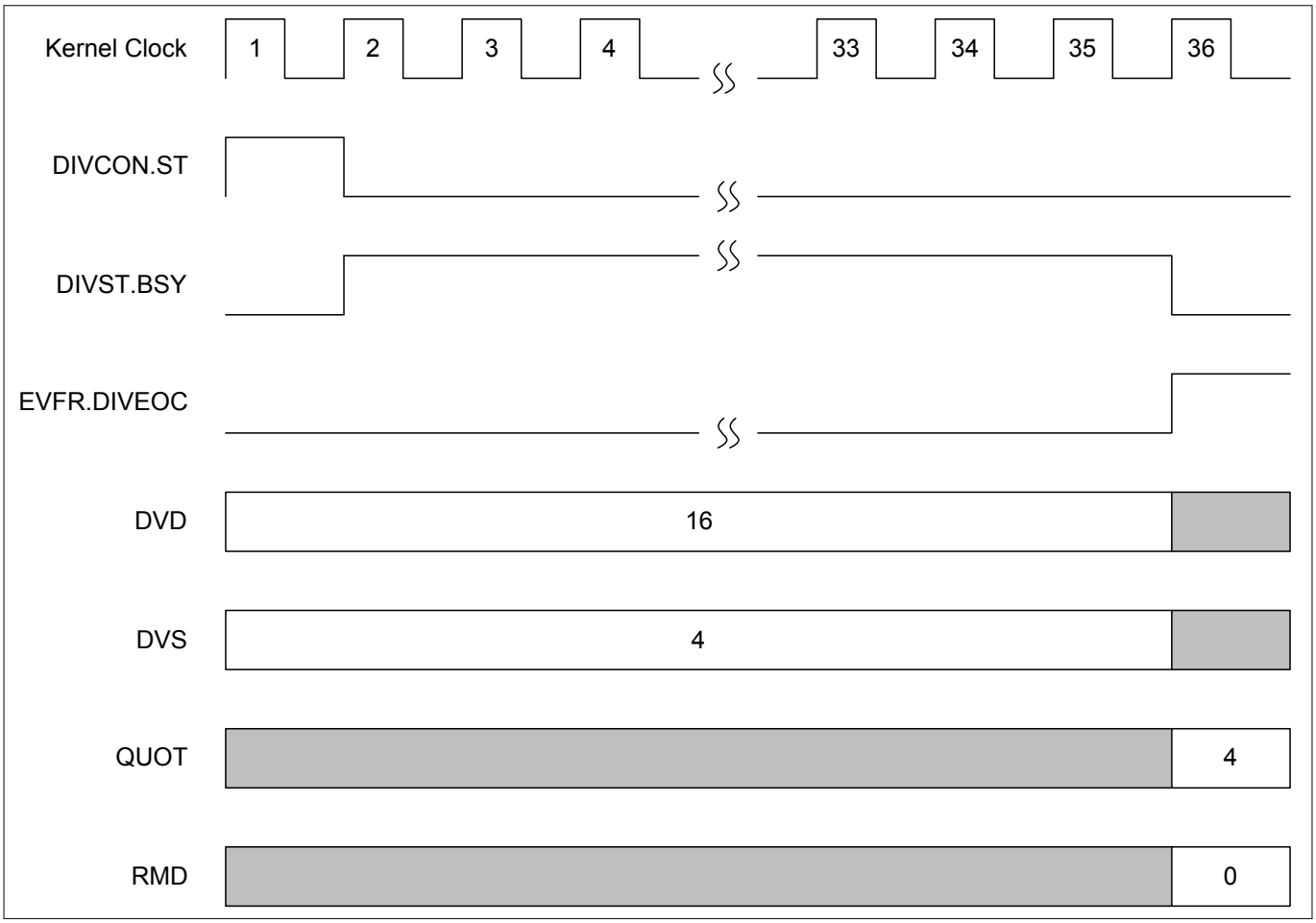


Figure 12 Timing Diagram for a Division Operation

Note: Reading the QUOT and RMD registers while BSY=1 will cause the DIV to insert wait states onto the bus until the active calculation is completed (BSY=0). This ensures that any read access on the result registers QUOT or RMD returns a valid result. However, the interrupt latency will be increased as the bus may be locked up for a number of kernel clock cycles.

5.2.2.1 Start Mode Selection

The condition to start a division operation is selectable through the DIVCON.STMODE bit:

- When STMODE = 0, a division operation is started with a write to the DVS register. In this case, no further software set of the ST bit is necessary.
- When STMODE = 1, a division is started by setting the ST bit.

For both start modes, it must be ensured that the DIV is not performing any active calculation and the DIVST.BSY flag is 0 before starting the operation, else the start request is discarded though DVS will still be updated with the write value. Write access to DIVCON register is ignored while BSY = 1. It is recommended for the application to poll for this condition before starting the divider operation with a write to ST bit or DVS register.

5.2.2.2 Error Handling

The DIV supports two types of error detection:

- Divide by zero error
- Overflow error

In both cases, the error will be indicated by the EVFR.DIVERR flag. An interrupt request to NVIC can be generated if it is enabled through EVIER.DIVERRIEN.

The division operation will still proceed as normal and complete in 35 kernel clock cycles. The error flag becomes set at the same clock cycle as DIVEOC.

Divide by Zero Error

A divide by zero error occurs when a division operation is started with the divisor value in DVS register equal to 0.

An example of a divide by zero error is shown in ***Figure 13***.

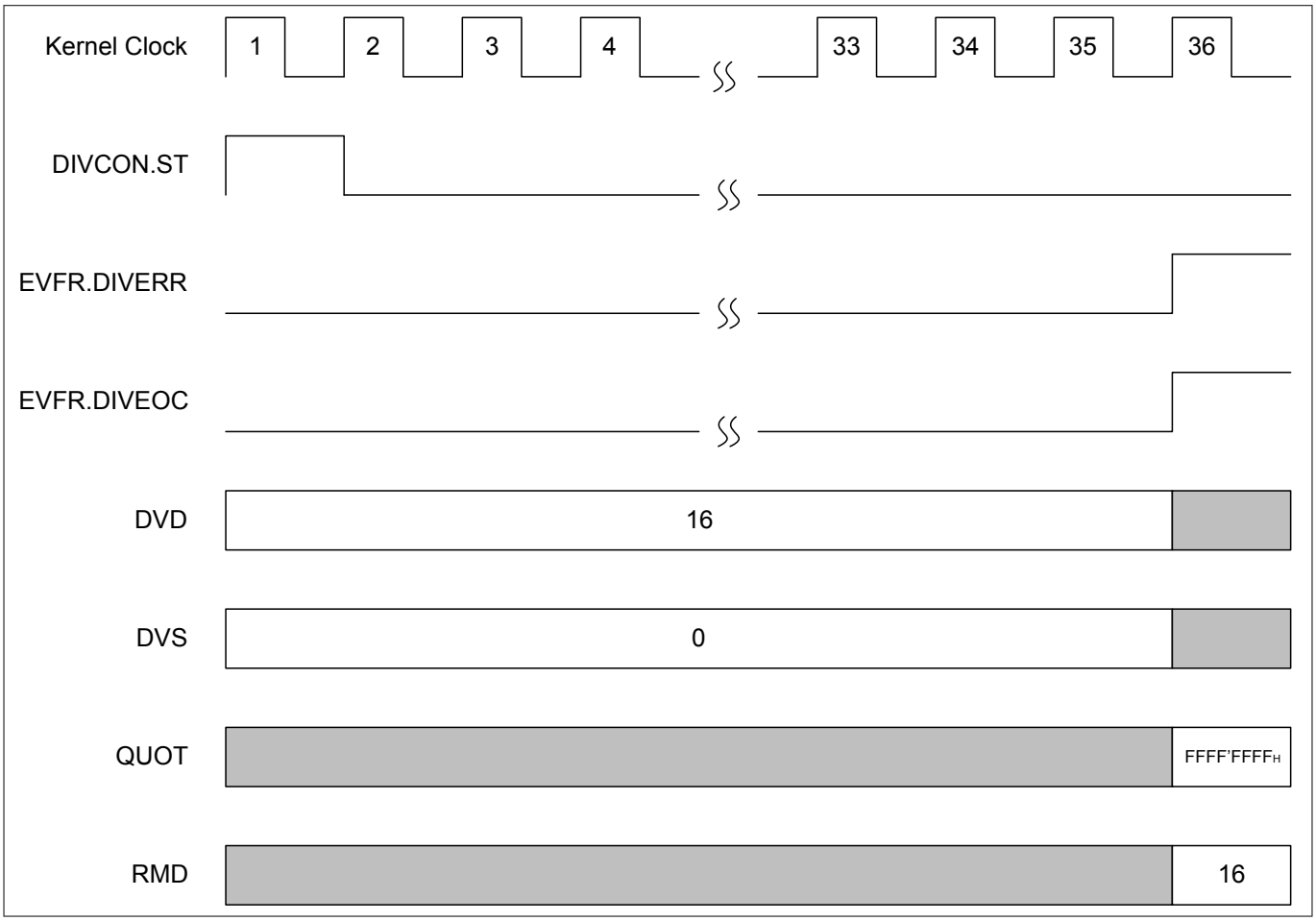


Figure 13 Timing Diagram with Divide by Zero Error

If DIVCON.USIGN is 0 (signed operation) and DVD is a negative value, the QUOT register will contain all zeros, else it will contain all ones. In either case, the RMD register will contain the value of the dividend. The flag is cleared only by a software write to the EVFCR.DIVERRC bit.

*Note: If result post-processing (see **Chapter 5.2.3**) is enabled, the value of the quotient (all zeros or all ones) will still be shifted according to DIVCON.QSCNT.*

Overflow Error

An overflow error occurs when one of the three conditions listed in ***Table 19*** is detected.

Table 19 Overflow Error Conditions

DIVCON.DIVMODE	Dividend (Hex)	Dividend (Dec)	Divisor (Hex)	Divisor (Dec)
00_B	$8000'0000_H$	-2^{31}	$FFFF'FFFF_H$	-1
01_B	$8000'0000_H$	-2^{31}	$FFFF_H$	-1
10_B	8000_H	-32768	$FFFF_H$	-1

The DIV does not detect for overflow errors that is due to result post-processing. In this case, user must always ensure that the result after post-processing is still within the boundaries of DIV.

5.2.3 Operand/Result Pre-/Post-Processing

The DIV supports operand pre-processing and result post-processing by allowing the following:

- Left shift of the dividend value before the start of division
- Right shift of the divisor value before the start of division
- Left or right shift of the quotient value after the end of division

The number of shifts is determined by the respective 5-bit shift count bit fields in DIVCON register. Additionally for the quotient, the shift direction is defined by the bit DIVCON.QSDIR.

All shifts are arithmetic shifts. This means if shift left, zeros will be inserted at LSB, while if shift right, zeros (in unsigned mode) or the signed bit (in signed mode) will be inserted at MSB.

Note: For the case where left shifting of the operand causes the signed bit to change from 0 to 1, the divider handles the signed bit as the MSB of the data value and ignores the signed effect.

If selected to be enabled by writing a non-zero value to the shift count bit fields, the shift operations will be triggered at the start and end of the division operation and do not consume any additional kernel clock cycles. The DIV event flag will be generated at the end of the 35-clock execution cycle.

During operand pre-processing, the shifts are performed only on the output of the DVD and DVS registers and not on the registers themselves. Therefore, the contents of these registers remain unchanged.

5.3 CORDIC Coprocessor

The CORDIC Coprocessor computes trigonometric, linear, hyperbolic and related functions.

5.3.1 Overview

The CORDIC algorithm is a useful convergence method for computing trigonometric, linear, hyperbolic and related functions. It allows performance of vector rotation not only in the Euclidian plane, but also in the Linear and Hyperbolic planes.

The CORDIC algorithm is an iterative process where truncation errors are inherent. Higher accuracy is achieved in the MATH with 27 iterations per calculation and kernel data width of at least 32 bits. The main advantage of using this algorithm is the fast calculation speed compared to software and high accuracy.

For clarity, the document uses the following terms for referencing CORDIC data:

- Result Data: Final result data at the end of CORDIC calculation (Bit BSY no longer active).
- Calculated Data: Intermediate or last data resulting from CORDIC iterations.
- Initial Data: Data used for the very first CORDIC iteration, is usually user-initialized data.

5.3.1.1 Features

The key features of the MATH are listed below:

- Modes of operation
  - Supports all CORDIC operating modes for solving circular (trigonometric), linear (multiply-add, divide-add) and hyperbolic functions
  - Integrated look-up tables (LUTs) for all operating modes
- Circular vectoring mode: Extended support for values of initial X and Y data up to full range of $[-2^{23},(2^{23}-1)]$ for solving angle and magnitude
- Circular rotation mode: Extended support for values of initial Z data up to full range of $[-2^{23},(2^{23}-1)]$, representing angles in the range $[-\pi,((2^{23}-1)/2^{23})\pi]$ for solving trigonometry
- 24-bit accessible data width
  - 32-bit kernel data width plus 2 sign extension bits and 1 overflow bit for X and Y each
  - 29-bit kernel data width plus 1 sign extension bit and 1 overflow bit for Z
  - With KEEP bit to retain the last value in the kernel register for a new calculation
- 27 iterations per calculation: 62 kernel clock cycles or less, from set of start (ST) bit to set of end-of-calculation flag, excluding time taken for write and read access of data bytes.
- Twos complement data processing
  - Only exception: X result data with user selectable option for unsigned result
- X and Y data generally accepted as integer or rational number; X and Y must be of the same data form
- Truncation Error
  - The result of a CORDIC calculation may return an approximation due to truncation of LSBs
  - Good accuracy of the CORDIC calculated result data, especially in circular mode
- Interrupt
  - On completion of a calculation
  - Interrupt enabling and corresponding flag

Table 20 CORDIC Applications

Use Case	Application
Angle computation	EPS, Motor control
Park transformation	Motor control
Y +XZ	Digital filtering, PI control loop

5.3.2 Functional Overview

The following sections describe the function of the MATH.

5.3.2.1 Operation of the MATH

The MATH can be used for the circular (trigonometric), linear (multiply-add, divide-add) or hyperbolic function, in either rotation or vectoring mode. The modes are selectable by software via the ***CON*** control register.

Initialization of the kernel data register is enabled by clearing respective ***STATC***.KEEPx bits of the register ***STATC***. If ***CON***.ST_MODE = 1, writing 1 to bit ***CON***.ST starts a new calculation. Otherwise, by default where ***CON***.ST_MODE = 0, a new calculation starts after a write access to register ***CORDX***. Each calculation involves a fixed number of 27 iterations. Bit ***STATC***.BSY is set while a calculation is in progress to indicate busy status. It is cleared by hardware at the end of a calculation.

As the first step on starting a CORDIC calculation (provided the corresponding KEEP bits are not set), the initial data is loaded from the data registers CORDx to the internal kernel data registers. During the calculation, the kernel data registers always hold the latest intermediate data. On completion of the calculation, the result data will be loaded to the result registers CORRx.

The data registers CORDx function as shadow registers which can be written to without affecting an ongoing calculation. Values are transferred to the kernel data registers only on valid setting of bit ***CON***.ST, or if ***CON***.ST_MODE = 0, after write access to X data register ***CORDX*** (provided KEEP bit of corresponding data is not set). The result data can be read from the result registers CORRx at the end of calculation (BSY no longer active). The result data needs to be read before the start of the next calculation. Any read access on the result registers CORRx while ***STATC***.BSY is set (kernel is still running a calculation) will cause the kernel to issue a bus wait until ***STATC***.BSY is reset. This will ensure that any read access on the result registers CORRx returns a valid result.

At the end of each calculation, ***STATC***.BSY returns to 0. The EVFR.CDEOC bit, which denotes the CORDIC end-of-calculation, is set. The interrupt request signal will be activated if interrupt is enabled by EVIER.CDEOCIEN = 1. The EVFR.CDEOC flag will have to be cleared manually via software by setting EVFCR.CDEOCC = 1. The result data in X, Y and Z are internally checked, and in case of data overflow, the EVFR.CDERR bit is set. An interrupt request signal will be activated if interrupt is enabled by EVIER.CDERRIEN = 1. The EVFR.CDERR flag will have to be cleared manually via software by setting EVFCR.CDERRC = 1.

Setting the bit ***CON***.ST during an ongoing calculation (if ***CON***.ST_MODE = 1) while ***STATC***.BSY is set has no effect. In order to start a new calculation, bit ***CON***.ST must be set again at a later time when ***STATC***.BSY is no longer active. In the same manner, changing the operating mode during a running calculation (as indicated by ***STATC***.BSY) has no effect.

In automatic start mode (***CON***.ST_MODE = 0), if write access to ***CORDX*** occurs while ***STATC***.BSY is set, the new calculation will not be started, similar to the case with ***CON***.ST_MODE = 1.

5.3.2.2 Normalized Result Data

In all operating modes, the MATH returns a normalized result data for X and Y, as shown in the following equation:

$$\text{X or Y Result Data} = \frac{\text{CORDIC Calculated Data}}{\text{MPS}}$$

Equation 1

On the other hand, the interpretation for Z result data differs, which is also dependent on the CORDIC function used:

For **linear** function, there is no additional processing of the CORDIC calculated Z data, as such it is taken directly as the result data. The accessible Z result data is a real number expressed as signed 4Q19.

For **circular** and **hyperbolic** functions, the accessible Z result data is a normalized integer value, angles in the range $[-\pi,((2^{23}-1)/2^{23})\pi]$ are represented by $[-2^{23},(2^{23}-1)]$. The MATH expects Z data to be interpreted with this scaling:

$$\text{Input Z Initial Data} = \text{Real Z Initial Value (in radians)} \times \frac{8388608}{\pi}$$

Equation 2

$$\text{Real Z Result Value (in radians)} = \text{Z Result Data} \times \frac{\pi}{8388608}$$

Equation 3

The CORDIC calculated data includes an inherent gain factor *K* resulting from the rotation or vectoring. The value *K* is different for each CORDIC function, as shown in ***Table 21***.

Table 21 CORDIC Function Inherent Gain Factor for Result Data

Function	Approximated Gain K
Circular	1.646760258121
Hyperbolic	0.828159360960
Linear	1

5.3.3 MATH Operating Modes

Table 22 gives an overview of the MATH operating modes. In this table, *X*, *Y* and *Z* represent the initial data, while X_{final}, Y_{final} and Z_{final} represent the final result data when all processing is complete and BSY is no longer active.

Table 22 MATH Operating Modes and Corresponding Result Data

Function	Rotation Mode	Vectoring Mode
Circular $m = 1$	$X_{final} = K[X \cos(Z) - Y \sin(Z)]$ / MPS $Y_{final} = K[Y \cos(Z) + X \sin(Z)]$ / MPS $Z_{final} = 0$ where K ≈ 1.646760258121	$X_{final} = K \sqrt{(X^2+Y^2)}$ / MPS $Y_{final} = 0$ $Z_{final} = Z + \text{atan}(Y / X)$ where K ≈ 1.646760258121
	For solving cos(*Z*) and sin(*Z*), set *X* = 1 / K, *Y* = 0. Useful domain: Full range of *X*, *Y* and *Z* supported due to pre-processing logic.	For solving magnitude of vector ($\sqrt{(x^2+y^2)}$), set *X* = x / K, *Y* = y / K. Useful domain: Full range of *X* and *Y* supported due to pre- and post-processing logic. For solving atan(*Y* / *X*), set *Z* = 0. Useful domain: Full range of *X* and *Y*, except *X* = 0.
	Relationships: tan(v) = sin(v) / cos(v)	Relationships: acos(w) = atan[$\sqrt{(1-w^2)}$ / w] asin(w) = atan[w / $\sqrt{(1-w^2)}$]
Linear $m = 0$	$X_{final} = X$ / MPS $Y_{final} = [Y + XZ]$ / MPS $Z_{final} = 0$	$X_{final} = X$ / MPS $Y_{final} = 0$ $Z_{final} = Z + Y / X$
	For solving $X \cdot Z$, set *Y* = 0. Useful domain: $\lvert Z \rvert \le 2$.	For solving ratio *Y* / *X*, set *Z* = 0. Useful domain: $\lvert Y / X \rvert \le 2$, $X > 0$.
Hyperbolic $m = -1$	$X_{final} = k[X \cosh(Z) + Y \sinh(Z)]$ / MPS $Y_{final} = k[Y \cosh(Z) + X \sinh(Z)]$ / MPS $Z_{final} = 0$ where k ≈ 0.828159360960	$X_{final} = k \sqrt{(X^2-Y^2)}$ / MPS $Y_{final} = 0$ $Z_{final} = Z + \text{atanh}(Y / X)$ where k ≈ 0.828159360960

Table 22 MATH Operating Modes and Corresponding Result Data (continued)

Function	Rotation Mode	Vectoring Mode
	For solving cosh(Z) and sinh(Z) and e^Z, set $X = 1 / k$, $Y = 0$. Useful domain: $\|Z\| \le 1.11$rad, $Y = 0$.	For solving sqrt(x^2-y^2), set $X = x / k$, $Y = y / k$. Useful domain: $\|y\| < \|x\|$, $X > 0$. For solving atanh(Y / X), set $Z = 0$. Useful domain: $\|\text{atanh}(Y / X)\| \le 1.11$rad, $X > 0$.
	Relationships: tanh(v) = sinh(v) / cosh(v) e^v = sinh(v) + cosh(v) $w^t = e^{t\ \ln(w)}$	Relationships: ln(w) = 2 atanh[(w-1) / (w+1)] sqrt(w) = sqrt($(w+0.25)^2$-$(w-0.25)^2$) acosh(w) = ln[w+sqrt(1-w^2)] asinh(w) = ln[w+sqrt(1+w^2)]

Usage Notes

- For solving the respective functions, user must initialize the CORDIC data (X, Y and Z) with valid initial values within the domain of convergence to ensure result convergence. The 'useful domain' listed in ***Table 22*** covers the supported domain of convergence for the CORDIC algorithm and excludes the invalid range(s) for the function.
- All data inputs are processed and handled as twos complement. Only exception is user-option for X result data (only) to be read as unsigned value.
- The only case where the result data is always positive and larger than the initial data is X result data (only) in circular vectoring mode; therefore, the user may want to use the MSB bit as data bit instead of sign bit. By setting X_USIGN = 1, X result data will be processed as unsigned data.
- For circular and hyperbolic functions the Z data is always handled as signed integer S28 (accessible as S23). Z data is limited (not considering domain of convergence) to represent angles $[-\pi,((2^{23}-1)/2^{23})\pi]$ for these CORDIC functions. Any calculated value of Z outside of this range will result in overflow error.
- For linear function, the Z data is always handled as signed fraction S4.24 (accessible as S4.19 in the form signed 4Q19). The emulated LUT is actually a shift register that holds data in the form 1.23 which gives the real value of 2^{-i}. Therefore, regardless of the domain of convergence, Z data is logically only useful for values whose magnitude is smaller than 16. Overflow error is indicated by the EVFR.CDERR bit.
- The MPS setting has no effect on Z data. User must ensure proper initialization of Z initial data to prevent overflow and incorrect result data.
- The MATH is designed such that with correct user setting of MPS > 1, there is no internal overflow of the X and Y data and the read result data is complete. However, note that in these cases, the higher the MPS setting, the lower the resolution of the result data due to loss of LSB bit(s).
- The hyperbolic rotation mode is limited, in terms of result accuracy, in that initial Y data must be set to zero. In other words, the MATH is not able to return accurate result for cosh(Z)+/-sinh(Z) in a single calculation.

5.3.3.1 Domains of Convergence

It is not intended for this document to cover the theory of the inherent limits of CORDIC convergence, which varies with different CORDIC function in rotation or vectoring mode.

For convergence of result data, there are limitations to the magnitude or value of initial data and corresponding useful data form, depending on the operating mode used. The following are generally applicable regarding convergence of CORDIC result data.

Rotation Mode

Z data must converge towards 0. In circular function, this means |Z| ≤ integer value representing 1.74 radians. For linear function, |Z| ≤ 2. In hyperbolic function, |Z| ≤ integer value representing 1.11 radians.

Vectoring Mode

Y data must converge towards 0. For circular function, this means |atan(Y / X)| ≤ 1.74 radians. For linear function, |Y / X| ≤ 2. For hyperbolic function, |atanh(Y / X)| ≤ 1.11 radians. In vectoring mode, the additional requirement is that X > 0.

While the operating modes of the MATH are generally bounded by these convergence limits, there are exceptions for the circular rotation and circular vectoring modes which use additional pre- (and post-)processing logic to support wider range of inputs.

Circular Rotation Mode

The full range of Z input $[-2^{23},(2^{23}-1)]$ representing angles $[-\pi,((2^{23}-1)/2^{23})\pi]$ is supported. No limitations on initial X and Y inputs, except for overflow considerations which can be overcome with MPS setting.

Circular Vectoring Mode

The full range of X and Y inputs $[-2^{23},(2^{23}-1)]$ are supported, while Z initial value should satisfy $|Z| \leq \pi / 2$ to prevent possible Z result data overflow.

*Note: Considerations should also be given to function limitations such as the meaning of the result data, e.g. divide by zero is not meaningful. The 'useful domain' included within **Table 22** for each of the main functions, attempts to cover both for CORDIC convergence and useful range of the function.*

*Note: Input values may be within the domain of convergence, however, this does not guarantee a fixed level of accuracy of the CORDIC result data. Refer to **Chapter 5.3.5** for details on accuracy of the MATH.*

5.3.3.2 Overflow Considerations

Besides considerations for domain of convergence, the limitations on the magnitude of input data must also be considered to prevent result data overflow.

Data overflow is handled by the MATH in the same way in all operating modes. Overflow for X and Y data can be prevented by correct setting by the user of the MPS bit, whose value is partly based on the MATH operating mode and the application data.

The MPS setting has no effect on the Z data. For circular and hyperbolic functions, any value of Z outside of the range $[-\pi,((2^{23}-1)/2^{23})\pi]$ cannot be represented and will result in Z data overflow error. Note that kernel data Z has values in the range $[-\pi,((2^{23}-1)/2^{23})\pi]$ scaled to the range $[-2^{23},(2^{23}-1)]$, so the written and read values of Z data are always normalized as such. For linear function, where Z is a real value, magnitude of Z must not exceed 4 integer bits.

5.3.4 MATH Data Format

The MATH accepts (initial) data X, Y and Z inputs in twos complement format. The result data are also in twos complement format.

The only exception is for the X result data in circular vectoring mode. The X result data has a default data format of twos complement, but the user can select via bit ***CON***.X_USIGN = 1 for the X result data to be read as unsigned value. This option prevents a potential overflow of the X result data (taken together with the MPS setting), as the MSB bit is now a data bit. Note that setting bit ***CON***.X_USIGN = 1 is only effective when operating in the circular vectoring mode, which always yields result data that is positive and larger than the initial data.

Generally, the input data for X and Y can be integer or rational number (fraction). However, in any calculation, the data form must be the same for both X and Y. Also, in case of fraction, X and Y must have the same number of bits for decimal place.

The Z data is always handled as integer, based on the normalization factor for circular or hyperbolic function. In case of linear function, accessible Z data is a real number with fixed input and result data form of S4.19 (signed 4Q19) which is a fraction with 19 decimal places.

Refer to ***Chapter 5.3.2.2*** for details on data normalization.

Table 23 summarizes the initial and result data format.

Table 23 Summary of X,Y and Z data format

Function	Data		Mode	
			Rotation	**Vectoring**
Circular	X	Initial	24-bit 2's complement	
		Result	24-bit 2's complement	24-bit 2's complement / 24-bit unsigned data (***CON***.X_USIGN = 1)
	Y	Initial	24-bit 2's complement	
		Result		
	Z	Initial		
		Result		
Linear	X	Initial		
		Result		
	Y	Initial		
		Result		
	Z	Initial	S4.19	
		Result		
Hyperbolic	X	Initial	24-bit 2's complement	
		Result		
	Y	Initial		
		Result		
	Z	Initial		
		Result		

5.3.5 Accuracy of MATH

Each CORDIC calculation involves a fixed number of 27 CORDIC iterations starting from iteration 0. The hyperbolic function is special in this respect in that it starts from iteration 1 with repeat iterations at defined steps. The addressable data registers are 24 bits wide, while the internal kernel X and Y data registers used for calculation are each 35 bits wide (32 data bits plus 2 sign extension bits and 1 overflow bit) and internal kernel Z data register is 31 bits wide (29 data bits plus 1 sign extension bit and 1 overflow bit).

For input data values within the specified useful domain (see ***Table 22***), the result of each calculation of the MATH is guaranteed to converge, although the accuracy is not fixed per data form in each operating mode. The accuracy is a measure of the magnitude of the difference between the result data and the expected data from a high-accuracy calculator. "Normalized Deviation" (ND) is a generic term used to refer to the magnitude of deviation of the result data from the expected result. The deviation is calculated as if the input/result data is

integer. In case the data is a rational number, the magnitude of deviation has to be interpreted. For example, Z for linear vectoring mode of the data form S4.19 - ND = 1 (01_B) means the difference from expected real data has magnitude of no more than $|2^{-19} + 2^{-19}|$; ND = 2 (10_B) means the difference is no more than $|2^{-18}+2^{-19}|$; ND = 3 (11_B) means the difference is no more than $|2^{-19}+2^{-18}+2^{-19}|$; ND = 4 ($100_B$) means the difference is no more than $|2^{-17}+2^{-19}|$, and so on. The value of 2^{-19} is always added to account for possible truncation error.

Table 24 lists the probability of Normalized Deviation in a single calculation, with approximately one million different input sets for each respective MATH operating mode, based on the input conditions specified (always within useful domain, possibly with additional conditions).

The accuracy of each mode can be easily increased, by working with rational numbers (fraction) instead of integers. This refers to X and Y data only (X and Y must always be of same data form), while the data form of Z is fixed per the respective LUT's definition. It is obvious to expect that for a given input of X and Y (and Z), the calculated result will always return a constant value—regardless of whether X and Y are integers or rational numbers. The only difference is with regards to interpreting the input and result data, i.e., with no decimal place or how many decimal places. The deviation of the CORDIC result from the expected data is never smaller if X and Y are integers instead of rational numbers. Therefore, wherever possible, assign X and Y as rational numbers with carefully selected decimal place point, which could be based on the maximum ND of that mode.

Table 24 Normalized Deviation of a Calculation

Mode	X Normalized Deviation	Y or Z Normalized Deviation
Circular Vectoring	Input conditions: Useful Domain and [(1.64676/2)·sqrt(X^2+Y^2) ≥ 600]	
	0 : 97.8830% 1 : 2.1150% 2 : 0.0010% 3 : 0.0010% ND for X ≤ 3	0 : 69.6738% 1 : 29.8307% 2 : 0.4919% 3 : 0.0036% ND for Z ≤ 3
Circular Rotation	Input conditions: Useful Domain (Full range of X, Y and Z)	
	0 : 47.8958% 1 : 50.3470% 2 : 1.7561% 3 : 0.0006% 4 : 0.0003% 5 : 0.0002% ND for X ≤ 5	0 : 47.8773% 1 : 50.3626% 2 : 1.7438% 3 : 0.0103% 4 : 0.0052% 5 : 0.0008% ND for Y ≤ 5
Linear Vectoring	Input conditions: Useful Domain (|Y / X| ≤ 2, X > 0)	
	0 : 99.5869% 1 : 0.4131% ND for X ≤ 1	0 : 47.6909% 1 : 52.2723% 2 : 0.0239% 3 : 0.0129% ND for Z ≤ 3

Table 24 Normalized Deviation of a Calculation (continued)

Mode	X Normalized Deviation	Y or Z Normalized Deviation
Linear Rotation	Input conditions: Useful Domain (|Z| ≤ 2)	
	0 : 100% ND for X ≤ 0	0 : 48.2181% 1 : 50.7801% 2 : 0.9996% 3 : 0.0022% ND for Y ≤ 3
Hyperbolic Vectoring	Input conditions: Useful Domain (|Y| < |X|, X > 0, |atanh(Y / X)| ≤ 1.11rad)	
	0 : 98.1092% 1 : 1.8855% 2 : 0.0017% 3 : 0.0019% 4 : 0.0017% ND for X ≤ 4	0 : 47.7010% 1 : 51.2954% 2 : 0.9938% 3 : 0.0098% ND for Z ≤ 3
Hyperbolic Rotation	Input conditions: Useful Domain (|Z| ≤ 1.11rad, Y = 0)	
	0 : 47.6358% 1 : 51.1029% 2 : 1.2578% 3 : 0.0012% 4 : 0.0007% 5 : 0.0006% 6 : 0.0005% 7 : 0.0002% 8 : 0.0003% ND for X ≤ 8	0 : 47.5419% 1 : 51.2064% 2 : 1.2478% 3 : 0.0013% 4 : 0.0010% 5 : 0.0007% 6 : 0.0006% 7 : 0.0003% ND for Y ≤ 7

Note: The accuracy/deviation as stated above for each mode is not guaranteed for the final result of multi-step calculations, e.g. if an operation involves two CORDIC calculations, the second calculation uses the result data from the first calculation (enabled with corresponding KEEP bit set). This is due to accumulated approximations and errors.

5.3.6 Performance of MATH

The CORDIC calculation time from the start of calculation to the instant the EVFR.CDEOC flag is set is approximately 62 kernel clock cycles. It should be noted that the EVFR.CDERR flag is valid only one kernel clock cycle after the onset of EVFR.CDEOC. This timing for one complete calculation is applicable also to those modes which involve additional data processing, and also to the hyperbolic modes which involve repeat iterations and an extra cycle for mode setup.

Note: The above timing exclude time taken for software loading of initial data and reading of the final result data, to and from the six data registers.

5.4 Global Functions

Since the DIV and CORDIC have their own set of control and data registers, they can work independently from one another.

However, they share a common bus interface and some global functions.

5.4.1 Result Chaining

The Math Coprocessor supports result chaining between the DIV and CORDIC.

For the DIV, this means that each of the operand registers, DVD and DVS, can be updated with the value from any one of the result registers (QUOT and RMD in DIV; CORR[Z:X] in CORDIC).

For the CORDIC, this means that each of the operand registers, CORD[Z:X], can be updated with the value from either of the DIV result registers, QUOT and RMD.

In both cases, the selection is done with the operand register result chaining bit fields (xRC) in GLBCON register.

Note: To update the CORDIC CORD[Z:X] registers with the value from the corresponding CORR[Z:X] registers, a separate control based on the KEEP[Z:X] bits in STATC register, has to be used.

The update is done once the preceding DIV or CORDIC operation is completed, together with the update to the actual result register. ***Figure 14*** shows an example of chaining the DIV quotient result to the CORDIC X-operand.

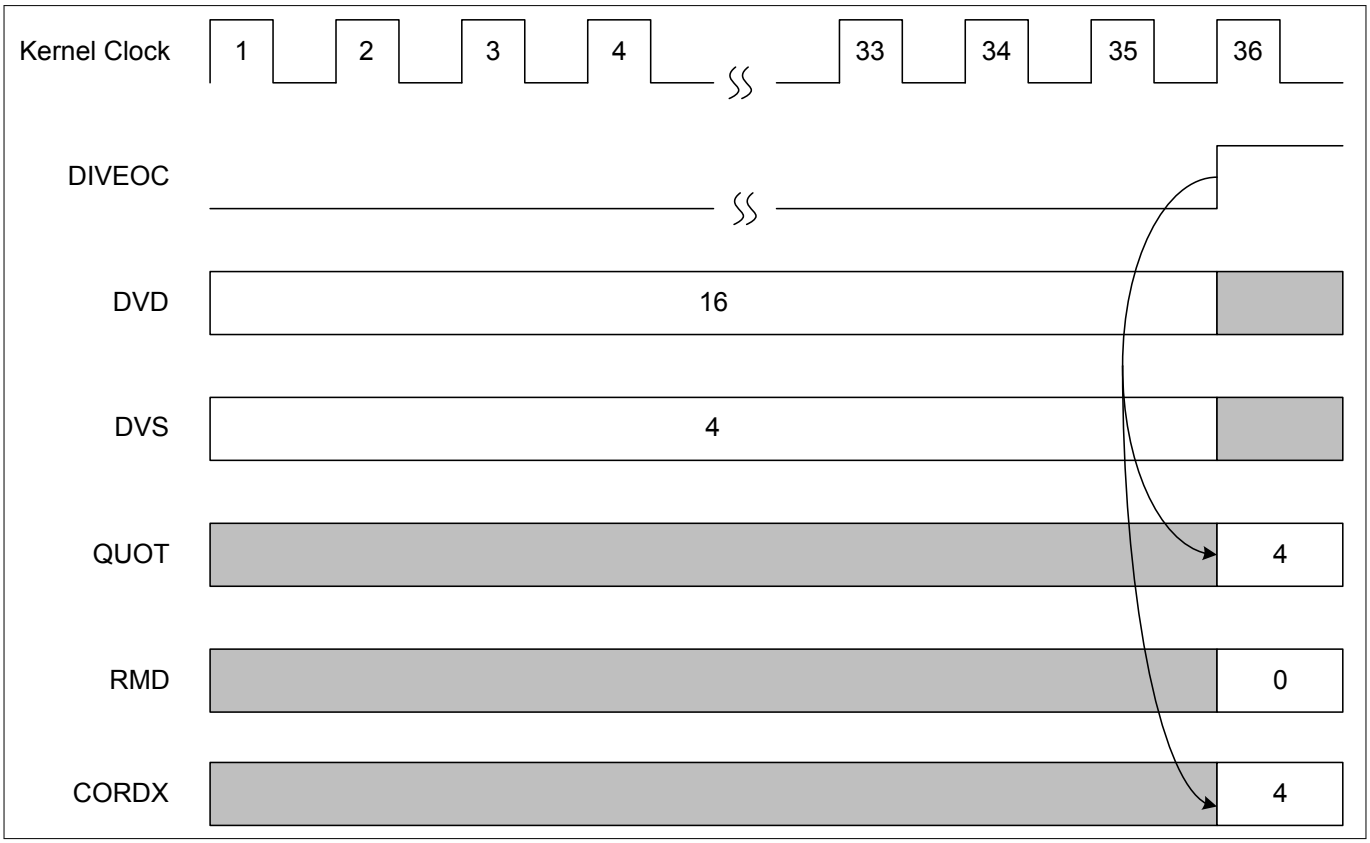


Figure 14 Division Operation with CORDXRC = 01

5.4.1.1 Result Chaining when Start Mode = 0

When the respective start mode is 0, a DIV and CORDIC operation can be started by having the application software write to the DVS and CORDX operand registers (see ***Chapter 5.2.2.1*** and ***Chapter 5.3.2***). An update of these registers due to result chaining is equivalent to a hardware write and therefore, has the same effect.

To avoid any potential deadlock situation, application must take care to avoid the following two scenarios when using the result chaining feature:

1. DVS is chained to QUOT or RMD while DIVCON.STMODE = 0
2. DVS is chained to CORRx and CORDX is chained to QUOT or RMD, and at the same time both DIVCON.STMODE and CON.ST_MODE = 0

5.4.1.2 Handling Busy Flags when Result Chaining is Enabled

Using the example given in ***Figure 14***, where a DIV result is chained to the CORDIC operand CORDX, if CON.ST_MODE = 0, starting the DIV calculation will set not just the DIV busy flag, but also that of the CORDIC. This is the case even though the CORDIC is initially not active, i.e. CORDIC calculation will start only after the DIV calculation is completed and either the QUOT or RMD value is written into CORDX. Similarly, the DIV, which becomes inactive after the DIV calculation is completed, does not clear its busy flag immediately. Instead, the busy flags of both DIV and CORDIC are cleared only after the CORDIC calculation is also completed.

The above applies also in the other direction, i.e. if a CORDIC result is chained to DIV DVS operand register and DIVCON.STMODE = 0.

While the busy flags are set:

- Reading the DIV or CORDIC result registers will cause wait states to be inserted onto the bus.
- While the DIV or CORDIC is active, starting a new DIV or CORDIC calculation or writing to their respective control registers DIVCON and CON will have no effect.
- However, if the DIV or CORDIC is still inactive or has just returned from an active state, starting a new DIV or CORDIC calculation or writing to their respective control registers will take effect.

A new calculation start or write to control register must be avoided while the DIV's or CORDIC's busy flag is set, otherwise calculation results might get corrupted.

5.5 Service Request Generation

If enabled by the respective interrupt enable bits in EVIER register, the DIV and CORDIC error and end of calculation events will trigger the interrupt service request to NVIC. The event is indicated by the event flag in EVFR register. The event flag can be cleared only by writing a 1 to the event flag clear bit in EVFCR register.

Writing a 1 to the event flag set bit in EVFSR register has the same effect of an end of calculation event.

Figure 15 shows the interrupt structure in the Math Coprocessor.

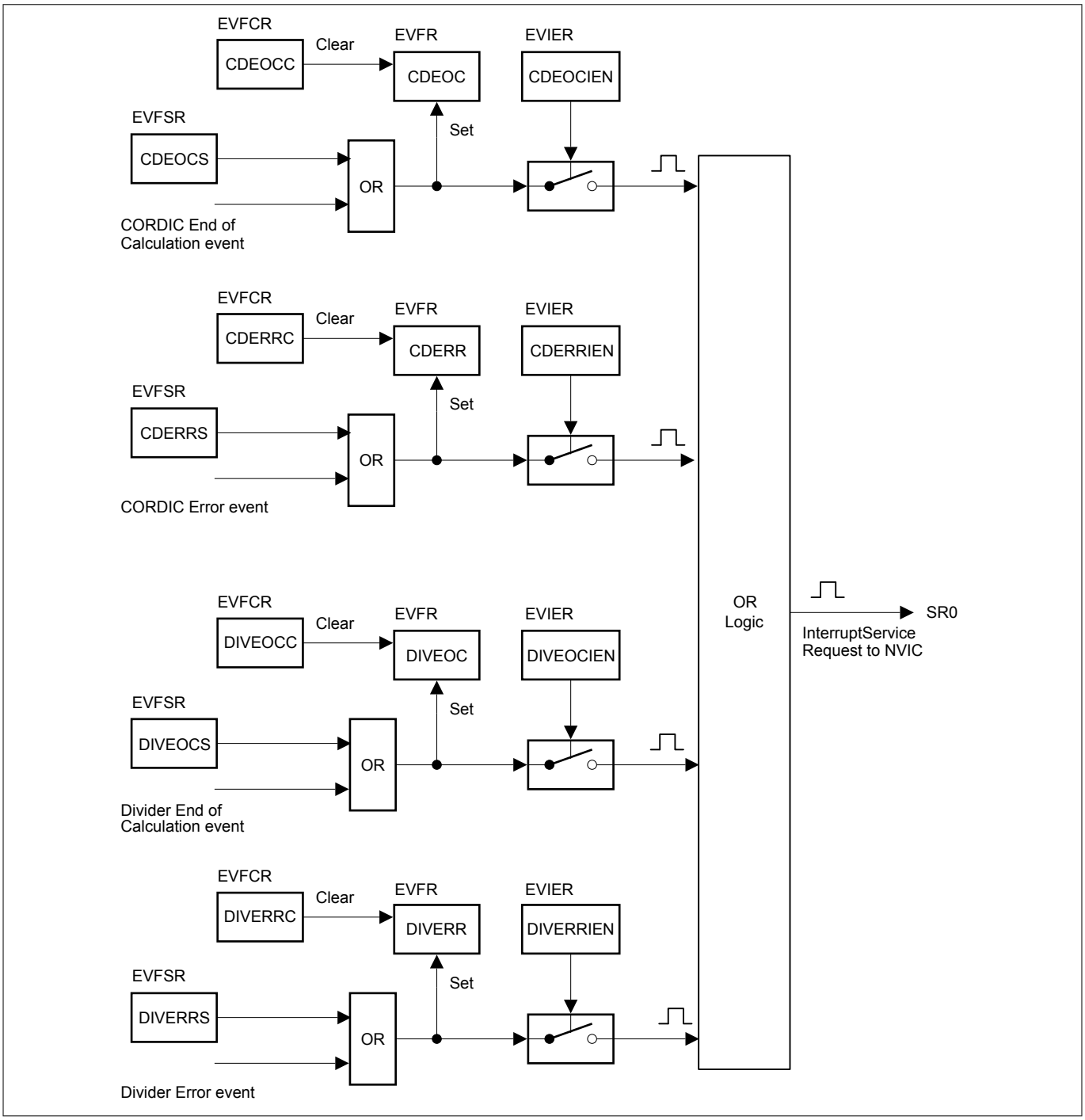


Figure 15 Interrupt Structure

5.6 Debug Behaviour

The Math Coprocessor can be configured to enter a suspend mode when the program execution of the CPU is halted by the debugger (indicated by the assertion of the suspend signal).

Two suspend modes are supported and can be selected through the control bit field GLBCON.SUSCFG:

- Hard Suspend Mode
  - The kernel clock is immediately switched off, thereby stopping all calculations
- Soft Suspend Mode
  - Any active calculation is allowed to continue and only after it is completed, will the kernel clock be switched off

After the kernel clock is switched off, all registers become read-only. Writing to registers in this state has no effect. Suspend mode is exited and normal operations resumed when the suspend signal becomes deasserted.

The suspend mode is non-intrusive concerning the register bits. This means register bits are not modified by hardware when entering or leaving the suspend mode.

Note: In IMC300A, bit field GLBCON.SUSCFG is reset to its default value by any reset. If the suspend function is required during debugging, it is recommended that it is enabled in the user initialization code. Before programming the bit field, the interface clock has to be enabled and special care needs to be taken while enabling the interface clock as described in the CCU (Clock Gating Control) section of the SCU chapter.

5.7 Power, Reset and Clock

The Math Coprocessor is located in the core power domain. The module, including all registers, will be reset to its default state by a system reset.

The Math Coprocessor requires two input clock signals, one for the kernel clock and one for the interface clock.The ratio of the kernel clock to the interface can be 2:1 or 1:1 but they must be at all times synchronous to each other.

Both clocks are disabled by default and can be enabled via the SCU_CGATCLR0 register. Enabling and disabling the two clocks could cause a load change and clock blanking could occur as described in the CCU (Clock Gating Control) section of the SCU chapter. It is strongly recommended to set up the two clocks in the user initialization code to avoid clock blanking during runtime.

5.8 Registers

Registers Overview

The absolute register address is calculated by adding:
Module Base Address + Offset Address

*Note: The DIV registers shown in **Table 26** supports both 16-bit and 32-bit bus access. All other registers (Global and CORDIC) supports only 32-bit access.*

Table 25 Registers Address Space

Module	Base Address	End Address	Note
MATH	$4003\ 0000_H$	$4003\ FFFF_H$	

Table 26 Register Overview

Short Name	Description	Offset Addr.	Access Mode		Description see
			Read	Write	
Global Registers					
Reserved	Reserved	0000_H	BE	BE	

Table 26 Register Overview (continued)

Short Name	Description	Offset Addr.	Access Mode		Description see
			Read	Write	
GLBCON	Global Control Register	0004_H	U, PV	U, PV	Page 105
ID	Module Identification Register	0008_H	U, PV	BE	Page 107
EVIER	Event Interrupt Enable Register	$000C_H$	U, PV	U, PV	Page 108
EVFR	Event Flag Register	0010_H	U, PV	U, PV	Page 109
EVFSR	Event Flag Set Register	0014_H	U, PV	U, PV	Page 109
EVFCR	Event Flag Clear Register	0018_H	U, PV	U, PV	Page 110
Reserved	Reserved	$001C_H$	BE	BE	
Divider Registers					
DVD	Dividend Register	0020_H	U, PV	U, PV	Page 111
DVS	Divisor Register	0024_H	U, PV	U, PV	Page 112
QUOT	Quotient Register	0028_H	U, PV	BE	Page 112
RMD	Dividend Register	$002C_H$	U, PV	BE	Page 113
DIVST	Divider Status Register	0030_H	U, PV	BE	Page 113
DIVCON	Divider Control Register	0034_H	U, PV	U, PV	Page 113
Reserved	Reserved	0038_H - $003F_H$	BE	BE	
CORDIC Registers					
STATC	Status and Data Control Register	0040_H	U, PV	U, PV	Page 115
CON	Control Register	0044_H	U, PV	U, PV	Page 116
CORDX	X Data Register	0048_H	U, PV	U, PV	Page 118
CORDY	Y Data Register	$004C_H$	U, PV	U, PV	Page 118
CORDZ	Z Data Register	0050_H	U, PV	U, PV	Page 118
CORRX	X Result Register	0054_H	U, PV	BE	Page 119
CORRY	Y Result Register	0058_H	U, PV	BE	Page 119
CORRZ	Z Result Register	$005C_H$	U, PV	BE	Page 120

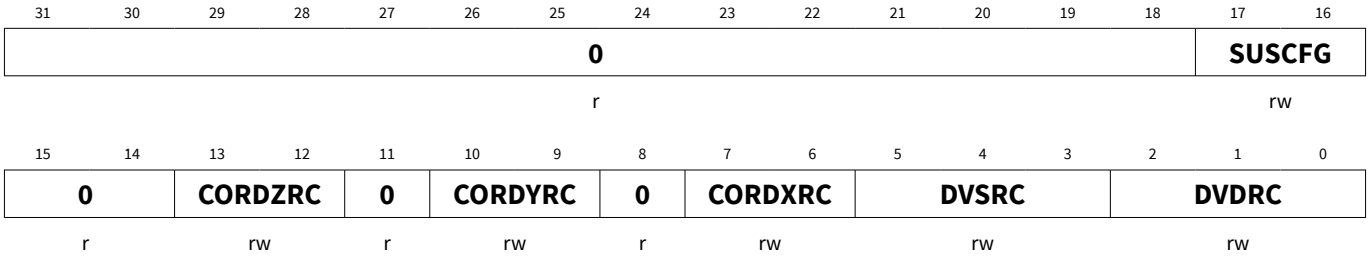
5.8.1 Global Registers Description

5.8.1.1 Register GLBCON

The GLBCON register contains the global control bits for the MATH Coprocessor.

GLBCON Address: 0004_H

Global Control Register Reset Value: $0000\ 0000_H$



Field	Bits	Type	Description
DVDRC	2:0	rw	**Dividend Register Result Chaining** The DVD register in DIV will be updated with the selected result register value when the result chaining trigger event occurs. 000_B No result chaining is selected 001_B QUOT register is the selected source 010_B RMD register is the selected source 011_B CORRX is the selected source 100_B CORRY is the selected source 101_B CORRZ is the selected source 110_B Reserved 111_B Reserved
DVSRC	5:3	rw	**Divisor Register Result Chaining** The DVS register in DIV will be updated with the selected result register value when the result chaining trigger event occurs. 000_B No result chaining is selected 001_B QUOT register is the selected source 010_B RMD register is the selected source 011_B CORRX is the selected source 100_B CORRY is the selected source 101_B CORRZ is the selected source 110_B Reserved 111_B Reserved
CORDXRC	7:6	rw	**CORDX Register Result Chaining** The CORDX register in CORDIC will be updated with the selected result register value when the result chaining trigger event occurs. 00_B No result chaining is selected 01_B QUOT register is the selected source 10_B RMD register is the selected source 11_B Reserved

(continued)

Field	Bits	Type	Description
CORDYRC	10:9	rw	**CORDY Register Result Chaining** The CORDY register in CORDIC will be updated with the selected result register value when the result chaining trigger event occurs. 00_B No result chaining is selected 01_B QUOT register is the selected source 10_B RMD register is the selected source 11_B Reserved
CORDZRC	13:12	rw	**CORDZ Register Result Chaining** The CORDZ register in CORDIC will be updated with the selected result register value when the result chaining trigger event occurs. 00_B No result chaining is selected 01_B QUOT register is the selected source 10_B RMD register is the selected source 11_B Reserved
SUSCFG	17:16	rw	**Suspend Mode Configuration** This bit determines if a suspend mode is entered by the Math Coprocessor when the CPU is halted. 00_B Suspend mode is never entered. 01_B Hard suspend mode will be entered when CPU is halted. 10_B Soft suspend mode will be entered when CPU is halted. 11_B Reserved
0	31:18, 15:14, 11, 8	r	**Reserved** Read as 0; should be written with 0.

5.8.1.2 Register MATH_ID

The MATH_ID register indicate the function and the design step of the Math Coprocessor.

MATH_ID Address: 0008_H

Module Identification Register Reset Value: $00F2\ C0XX_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MOD_NUMBER															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOD_TYPE								MOD_REV							
r								r							

Field	Bits	Type	Description
MOD_REV	7:0	r	**Module Revision Number** MOD_REV defines the revision number. The value of a module revision starts with 01_H (first revision).
MOD_TYPE	15:8	r	**Module Type** This bit field is $C0_H$. It defines the module as a 32-bit module.
MOD_NUMBER	31:16	r	**Module Number Value** This bit field defines the module identification number.

5.8.1.3 Register EVIER

This register enables interrupt generation for each event. If enabled, the detection of the event will generate the interrupt pulse through the service request output.

EVIER Address: $000C_H$

Event Interrupt Enable Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0												CDERRIEN	CDEOCIEN	DIVERRIEN	DIVEOCIEN
r												rw	rw	rw	rw

Field	Bits	Type	Description
DIVEOCIEN	0	rw	**Divider End of Calculation Interrupt Enable** 0_B Divider end of calculation interrupt generation is disabled. 1_B Divider end of calculation interrupt generation is enabled.
DIVERRIEN	1	rw	**Divider Error Interrupt Enable** 0_B Divider error interrupt generation is disabled 1_B Divider error interrupt generation is enabled
CDEOCIEN	2	rw	**CORDIC End of Calculation Interrupt Enable** 0_B CORDIC end of calculation interrupt generation is disabled. 1_B CORDIC end of calculation interrupt generation is enabled.
CDERRIEN	3	rw	**CORDIC Error Interrupt Enable** 0_B CORDIC error interrupt generation is disabled 1_B CORDIC error interrupt generation is enabled
0	31:4	r	**Reserved** Read as 0; should be written with 0.

5.8.1.4 Register EVFR

This register contains the status flags for each event. If set, it indicates that the event has been detected.

EVFR Address: 0010_H

Event Flag Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0												CDERR	CDEOC	DIVERR	DIVEOC
r												rh	rh	rh	rh

Field	Bits	Type	Description
DIVEOC	0	rh	**Divider End of Calculation Event Flag** 0_B Divider end of calculation event has not been detected. 1_B Divider end of calculation event has been detected.
DIVERR	1	rh	**Divider Error Event Flag** 0_B Divider error event has not been detected 1_B Divider error event has been detected
CDEOC	2	rh	**CORDIC End of Calculation Event Flag** 0_B CORDIC end of calculation event has not been detected. 1_B CORDIC end of calculation event has been detected.
CDERR	3	rh	**CORDIC Error Event Flag** 0_B CORDIC error event has not been detected 1_B CORDIC error event has been detected
0	31:4	r	**Reserved** Read as 0; should be written with 0.

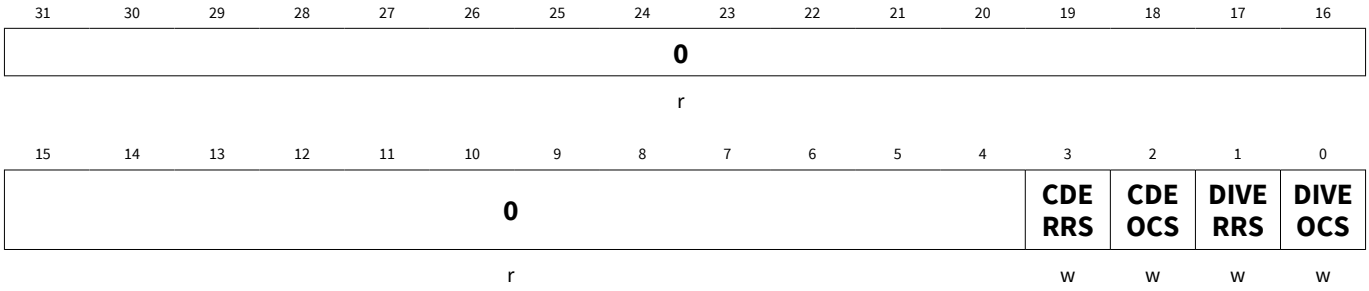
5.8.1.5 Register EVFSR

This register allows the application to set the status flags of each event in EVFR register, as if the event has been detected. If interrupt generation for that event is enabled previously in EVIER register, an interrupt service request will generated to the NVIC.

Writing 0 to these bits has no effect while reading always returns 0.

EVFSR Address: 0014_H

Event Flag Set Register Reset Value: $0000\ 0000_H$



Field	Bits	Type	Description
DIVEOCS	0	w	**Divider End of Calculation Event Flag Set** 0_B No effect. 1_B Sets the Divider end of calculation event flag in EVFR register. Interrupt will be generated if enabled in EVIER register.
DIVERRS	1	w	**Divider Error Event Flag Set** 0_B No effect. 1_B Sets the Divider error event flag in EVFR register. Interrupt will be generated if enabled in EVIER register.
CDEOCS	2	w	**CORDIC Event Flag Set** 0_B No effect. 1_B Sets the CORDIC end of calculation event flag in EVFR register. Interrupt will be generated if enabled in EVIER register.
CDERRS	3	w	**CORDIC Error Event Flag Set** 0_B No effect. 1_B Sets the CORDIC error event flag in EVFR register. Interrupt will be generated if enabled in EVIER register.
0	31:4	r	**Reserved** Read as 0; should be written with 0.

5.8.1.6 Register EVFCR

The event flags in EVFR register is cleared by writing a 1 to the corresponding bits in this register.
Writing 0 to these bits has no effect while reading always returns 0.

EVFCR Address: 0018_H

Event Flag Clear Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0												CDERRC	CDEOCC	DIVERRC	DIVEOCC
r												w	w	w	w

Field	Bits	Type	Description
DIVEOCC	0	w	**Divider End of Calculation Event Flag Clear** 0_B No effect. 1_B Clears the Divider end of calculation event flag in EVFR register.
DIVERRC	1	w	**Divider Error Event Flag Clear** 0_B No effect. 1_B Clears the Divider error event flag in EVFR register.
CDEOCC	2	w	**CORDIC End of Calculation Event Flag Clear** 0_B No effect. 1_B Clears the CORDIC end of calculation event flag in EVFR register.
CDERRC	3	w	**CORDIC Error Event Flag Clear** 0_B No effect. 1_B Clears the CORDIC error event flag in EVFR register.
0	31:4	r	**Reserved** Read as 0; should be written with 0.

5.8.2 Divider Registers Description

5.8.2.1 Register DVD

The DVD register is used to store the dividend operand of the division. It can be written by software and if result chaining is enabled, also by hardware.

DVD Address: 0020_H

Dividend Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VAL															
rwh															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL															
rwh															

Field	Bits	Type	Description
VAL	31:0	rwh	**Dividend Value**

5.8.2.2 Register DVS

The DVS register is used to store the divisor operand of the division. It can be written by software and if result chaining is enabled, also by hardware.

Note: A division operation can be started by a write to DVS while DIVCON.STMODE = 0.

DVS Address: 0024_H

Divisor Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VAL															
rwh															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL															
rwh															

Field	Bits	Type	Description
VAL	31:0	rwh	**Divisor Value**

5.8.2.3 Register QUOT

The QUOT register is used to store the quotient result of the division. It will be automatically updated by hardware upon each completion of a division operation.

Note: Wait states will be inserted on the bus if the QUOT register is read while BSY = 1. The bus read transaction will be completed only when the new QUOT value becomes available at the end of the active calculation/

QUOT Address: 0028_H

Quotient Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VAL															
rh															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL															
rh															

Field	Bits	Type	Description
VAL	31:0	rh	**Quotient Value**

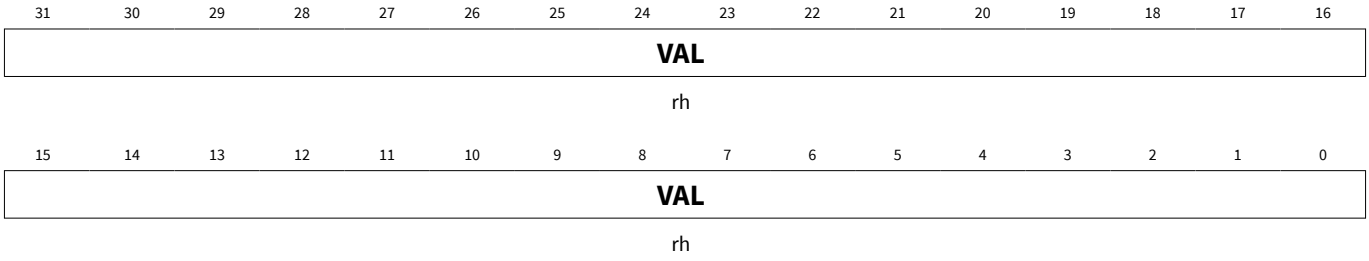
5.8.2.4 Register RMD

The RMD register is used to store the remainder result of the division. It will be automatically updated by hardware upon each completion of a division operation.

Note: Wait states will be inserted on the bus if the RMD register is read while BSY = 1. The bus read transaction will be completed only when the new RMD value becomes available at the end of the active calculation/

RMD Address: $002C_H$

Remainder Register Reset Value: $0000\ 0000_H$



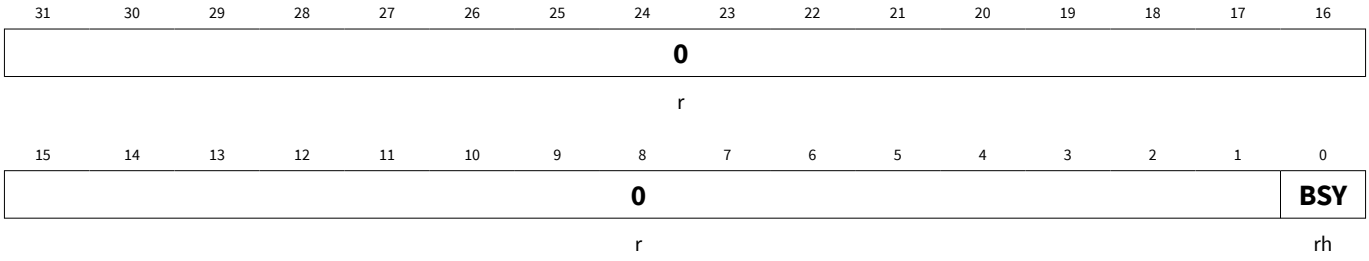
Field	Bits	Type	Description
VAL	31:0	rh	**Remainder Value**

5.8.2.5 Register DIVST

The DIVST register contains the status flags for the DIV.

DIVST Address: 0030_H

Divider Status Register Reset Value: $0000\ 0000_H$



Field	Bits	Type	Description
BSY	0	rh	**Busy Indication** 0_B Divider is not running any division operation. 1_B Divider is still running a division operation.
0	31:1	r	**Reserved** Read as 0; should be written with 0.

5.8.2.6 Register DIVCON

The DIVCON register contains the control bits for the DIV.

Write access to DIVCON register is ignored while BSY=1. No bus error will be generated in this case.

*Note: If result-chaining is enabled, refer also to **Chapter 5.4.1.2** for description on handling of the busy flag.*

DIVCON Address: 0034_H

Divider Control Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0			**DVSSRC**					**0**			**DVDSLC**				
r			rw					r			rw				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QSDIR	**0**		**QSCNT**					**0**			**DIVMODE**		**USIGN**	**STMODE**	**ST**
rw	r		rw					r			rw		rw	rw	rwh

Field	Bits	Type	Description
ST	0	rwh	**Start Bit** 0_B No effect 1_B Start the division operation when STMODE=1 The bit is automatically cleared by hardware after one kernel clock cycle.
STMODE	1	rw	**Start Mode** Selects the start mode for the division operation: 0_B Calculation is automatically started with a write to DVS register 1_B Calculation is started by setting the ST bit to 1 *Note: The start request for a new division operation will be ignored if BSY = 1.*
USIGN	2	rw	**Unsigned Division Enable** 0_B Signed division is selected 1_B Unsigned division is selected
DIVMODE	4:3	rw	**Division Mode** 00_B 32-bit divide by 32-bit 01_B 32-bit divide by 16-bit 10_B 16-bit divide by 16-bit 11_B Reserved
QSDIR	15	rw	**Quotient Shift Direction** This bit is used to select the shift direction for the quotient after a division: 0_B Left shift 1_B Right shift

(continued)

Field	Bits	Type	Description
QSCNT	12:8	rw	**Quotient Shift Count** If QSCNT is not equal to 0, it indicates the number of bits the quotient will be shifted by, after the division. If QSCNT=0, no shift operation will take place.
DVDSLC	20:16	rw	**Dividend Shift Left Count** If DVDSLC is not equal to 0, it indicates the number of bits the dividend will be shifted left by, prior to the division. If DVDSLC=0, no shift operation will take place.
DVSSRC	28:24	rw	**Divisor Shift Right Count** If DVSSRC is not equal to 0, it indicates the number of bits the divisor will be shifted right by, prior to the division. If DVSSRC=0, no shift operation will take place.
0	31:29, 23:21, 14:13, 7:5	r	**Reserved** Read as 0; should be written with 0.

5.8.3 CORDIC Registers Description

5.8.3.1 Register STATC

The STATC register generally reflects the status of the MATH. The register also contain bits for data control.

STATC Address: 0040_H

CORDIC Status and Data Control Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								KEEPZ	KEEPY	KEEPX	0				BSY
r								rw	rw	rw	r				rh

Field	Bits	Type	Description
BSY	0	rh	**Busy Indication** Indicates a running calculation when set. The flag is asserted one clock cycle after bit ST was set. It is deasserted at the end of a calculation.
0	4:1	r	**Reserved**

(continued)

Field	Bits	Type	Description
KEEPX	5	rw	**Last X Result as Initial Data for New Calculation** If set, a new calculation will use the value of the result from the previous calculation as the initial data. In other words, the respective kernel data register will not be overwritten by the contents of the shadow data register at the beginning of the new calculation. This bit should always be cleared for the very first calculation to load the initial X data. Independent of the KEEPx bit, the shadow data registers will continue to hold the last written initial data value until the next software write. If KEEPx bit is set for a multi-step calculation, the accuracy of the corresponding final x result data may be reduced and is not guaranteed as shown in ***Chapter 5.3.5***.
KEEPY	6	rw	**Last Y Result as Initial Data for New Calculation** <See description for KEEPX> Additionally, it may not be meaningful to set this bit in Vectoring modes as the last Y result converges to 0.
KEEPZ	7	rw	**Last Z Result as Initial Data for New Calculation** <See description for KEEPX> Additionally, it may not be meaningful to set this bit in Rotation modes as the last Z result converges to 0.
0	31:8	r	**Reserved**

5.8.3.2 Register CON

The CON register allows for the general control of the MATH. Write action to this register while ***STATC***.BSY is set has no effect.

*Note: If result-chaining is enabled, refer also to **Chapter 5.4.1.2** for description on handling of the busy flag.*

CON Address: 0044_H

CORDIC Control Register Reset Value: $0000\ 0062_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								**MPS**		**X_USIGN**	**ST_MODE**	**ROTVEC**	**MODE**		**ST**
r								rw		rw	rw	rw	rw		rwh

Field	Bits	Type	Description
ST	0	rwh	**Start Calculation** If ST_MODE = 1, set ST to start a CORDIC calculation. Is effective only while BSY is not set. This bit may be set with the other bits of this register in one write access. Cleared by hardware at the beginning of calculation.
MODE	2:1	rw	**Operating Mode** 00_B Linear Mode 01_B Circular Mode (default) 10_B Reserved 11_B Hyperbolic Mode
ROTVEC	3	rw	**Rotation Vectoring Selection** 0_B Vectoring Mode (default) 1_B Rotation Mode
ST_MODE	4	rw	**Start Method** 0_B Auto start of calculation after write access to X parameter data register ***CORDX*** (default). 1_B Start calculation only after bit ST is set
X_USIGN	5	rw	**Result Data Format for X in Circular Vectoring Mode** When reading the X result data, X data has a data format of: 0_B Signed, twos complement 1_B Unsigned (default) With this bit set, the MSB bit of the X result data is processed as a data bit instead of a sign bit. This bit is only effective when operating in circular vectoring mode. In all other modes, X is always processed as twos complement data. X_USIGN = 1 is meaningful in circular vectoring mode because the result data is always positive and always larger than the initial data.
MPS	7:6	rw	**X and Y Magnitude Prescaler** After the last iteration of a calculation, the calculated value of X and Y are each divided by this factor to yield the result. Proper setting of these bits is important to avoid an overflow of the result in the respective kernel data registers. 00_B Divide by 1 01_B Divide by 2 (default) 10_B Divide by 4 11_B Reserved, retain the last MPS setting
0	31:8	r	**Reserved**

5.8.3.3 CORDx

The Data registers are used to initialize the X, Y and Z parameters.

5.8.3.3.1 Register CORDX

CORDX Address: 0048_H

CORDIC X Data Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								0							
rw								r							

Field	Bits	Type	Description
0	7:0	r	**Reserved**
DATA	31:8	rw	**Initial X Parameter Data** Writing to this register with ***CON***.ST_MODE = 0 starts an operation.

5.8.3.3.2 Register CORDY

CORDY Address: $004C_H$

CORDIC Y Data Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
rw															

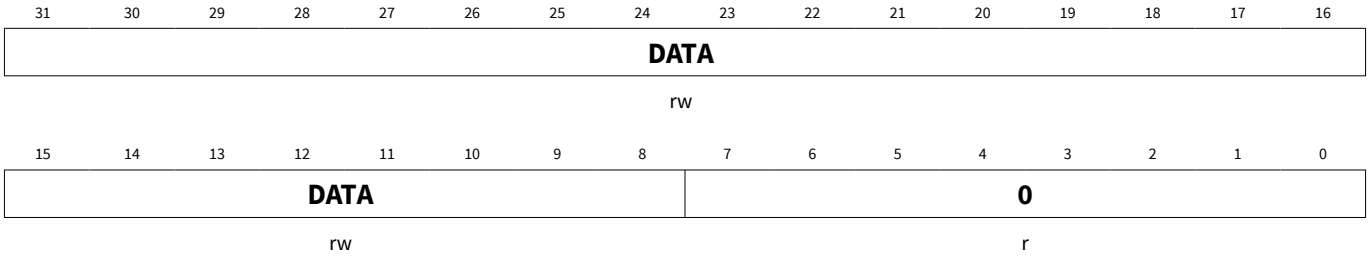
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								0							
rw								r							

Field	Bits	Type	Description
0	7:0	r	**Reserved**
DATA	31:8	rw	**Initial Y Parameter Data**

5.8.3.3.3 Register CORDZ

CORDZ Address: 0050_H

CORDIC Z Data Register Reset Value: $0000\ 0000_H$



Field	Bits	Type	Description
0	7:0	r	**Reserved**
DATA	31:8	rw	**Initial Z Parameter Data**

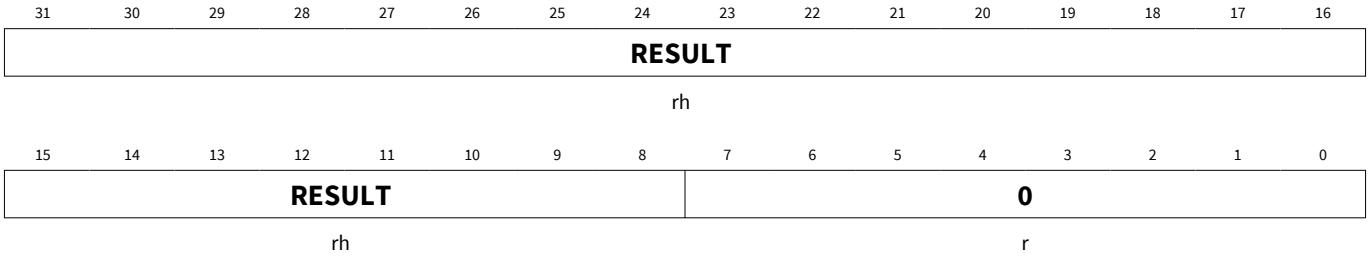
5.8.3.4 CORRx

The result data from CORDIC calculation will be written to the respective result registers. Any read access on these registers while ***STATC***.BSY is set (a calculation is still running) will cause the kernel to issue a bus wait until BSY is reset.

5.8.3.4.1 Register CORRX

CORRX Address: 0054_H

CORDIC X Result Register Reset Value: $0000\ 0000_H$



Field	Bits	Type	Description
0	7:0	r	**Reserved**
RESULT	31:8	rh	**X Calculation Result**

5.8.3.4.2 Register CORRY

CORRY Address: 0058_H

CORDIC Y Result Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESULT															
rh															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESULT								0							
rh								r							

Field	Bits	Type	Description
0	7:0	r	**Reserved**
RESULT	31:8	rh	**Y Calculation Result**

5.8.3.4.3 Register CORRZ

CORRZ Address: $005C_H$

CORDIC Z Result Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESULT															
rh															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESULT								0							
rh								r							

Field	Bits	Type	Description
0	7:0	r	**Reserved**
RESULT	31:8	rh	**Z Calculation Result**

5.9 Interconnects

Table 27 shows the module interconnects:

Table 27 Module Interconnects

Input/Output	I/O	Connected To	Description
SR0	O	NVIC	Interrupt service request output.

6 Service Request Processing

A hardware pulse is called Service Request (SR) in an IMC300A system. Service Requests are the fastest way to send trigger “messages” between connected on-chip resources.

An SR can generate any of the following requests

- Interrupt
- Peripheral action

This chapter describes the available Service Requests and the different ways to select and process them.

Table 28 Abbreviations

ERU	Event Request Unit
NVIC	Nested Vectored Interrupt Controller
SR	Service Request

6.1 Overview

Efficient Service Request Processing is based on the interconnect between the request sources and the request processing units. IMC300A provides both fixed and programmable interconnect.

6.1.1 Features

The following features are provided for Service Request processing:

- Connectivity matrix between Service Requests and request processing units
  - Fixed connections
  - Programmable connections using ERU

6.1.2 Block Diagram

Figure 16 shows a representation of the interaction between the request sources and the request processing units.

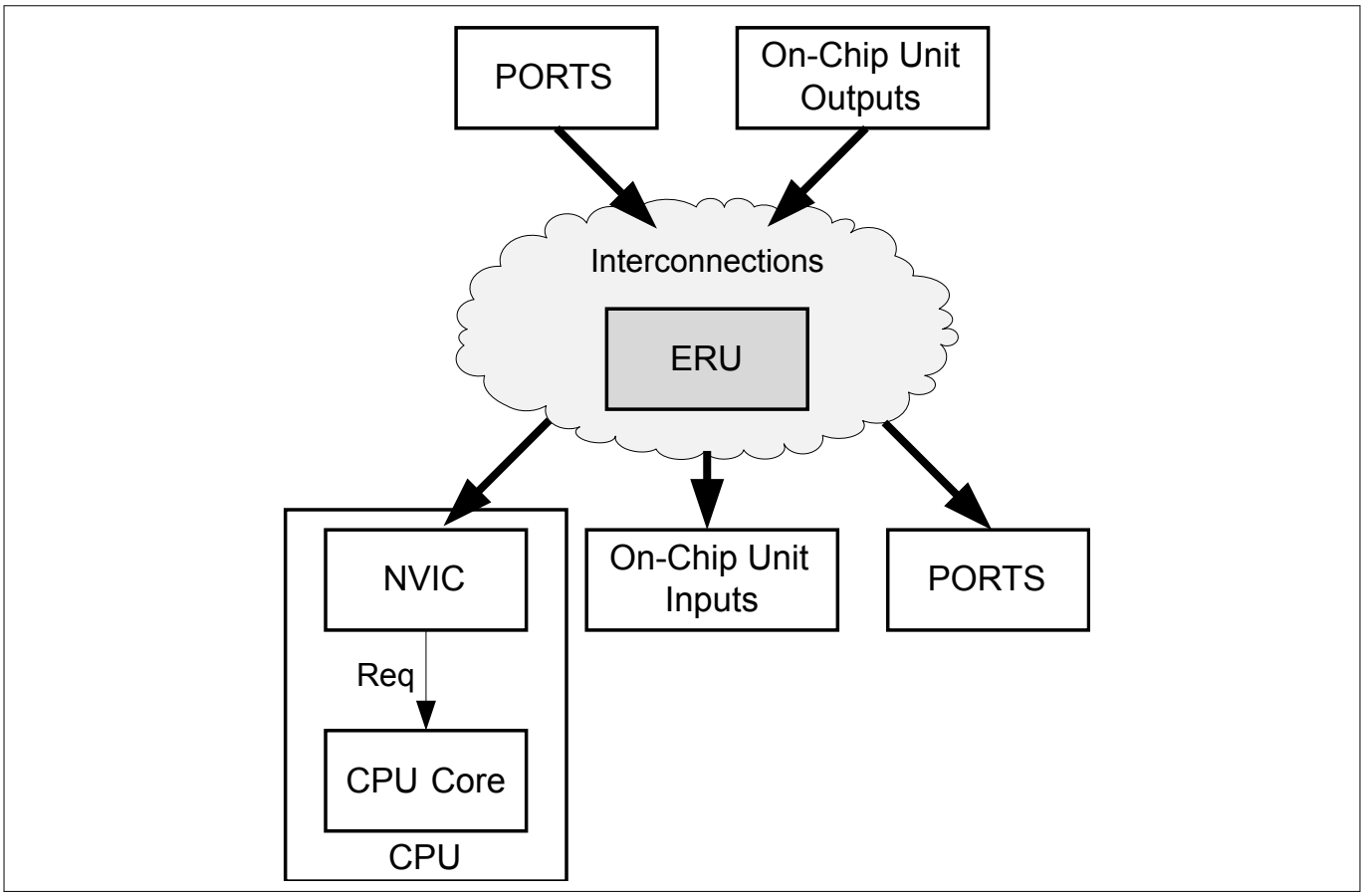


Figure 16 Block Diagram on Service Request Processing

6.2 Service Request Distribution

Figure 17 shows an example of how a service request can be distributed concurrently. To support the concurrent distribution to multiple receivers, the receiving modules are capable to enable/disable incoming requests.

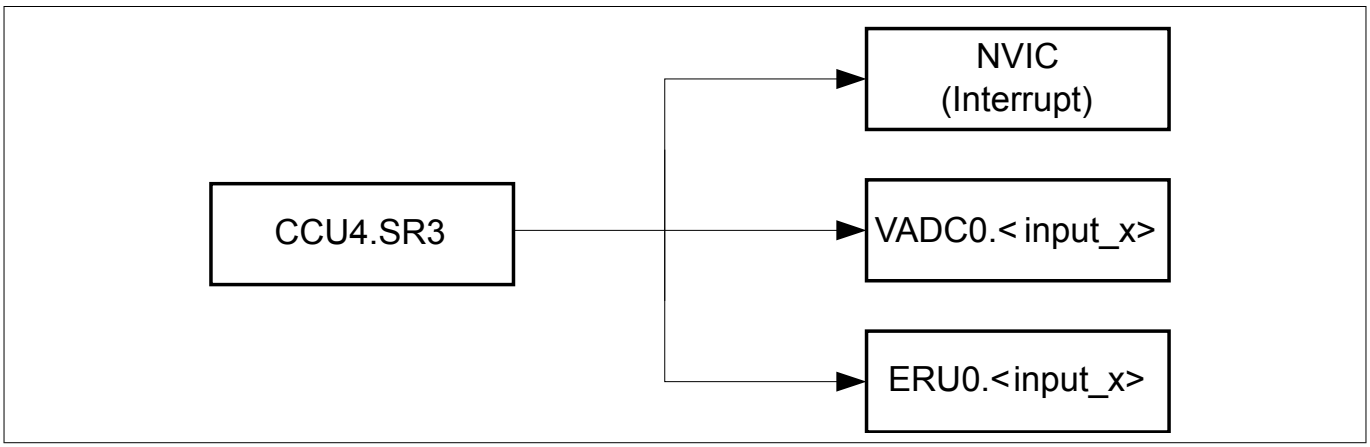


Figure 17 Example for Service Request Distribution

The units involved in Service Request distribution can be subdivided into

- Embedded real time services
- Interrupt services

Embedded real time services

Connectivity between On-Chip Units and PORTS is real time application and also chip package dependant. Related connectivity and availability of pins can be looked up in the

- “Interconnects” Section of the respective module(s) chapters
- “Parallel Ports” chapter and Data Sheet for PORTS
- “Event Request Unit” chapter

Interrupt services

The following table gives an overview on the number of service requests per module and the number that can be assigned to the NVIC Interrupt service provider.

As there are more service requests than available NVIC nodes, a combination of OR logic and multiplexors are implemented for each NVIC node to allow flexible assignment of service requests. Refer to the Interrupt Node Assignment section in the Interrupt Subsystem chapter for details.

Service Requests are always of of type “Pulse” in IMC300A.

Table 29 Interrupt services per module

Modules	Request Sources	NVIC	Type
VADC	12	6	Pulse
CCU40	4	4	Pulse
CCU41	4	4	Pulse
CCU80	4	2	Pulse
CCU81	4	2	Pulse
POSIF0	2	2	Pulse
POSIF1	2	2	Pulse
USIC0	6	6	Pulse
USIC1	6	6	Pulse
MATH	1	1	Pulse
SCU	3	3	Pulse
ERU0	4	4	Pulse
ERU1	4	4	Pulse
MultiCAN+	8	4	Pulse

7 Interrupt Subsystem (NVIC)

The interrupt Subsystem in IMC300A consists of the Nested Vectored Interrupt Controller (NVIC) and the respective modules' interrupt generation blocks.

Note: The CPU exception model is described in the CPU chapter.

7.1 Nested Vectored Interrupt Controller (NVIC)

The NVIC is an integral part of the Cortex M0 processor unit. Due to a tight coupling with the CPU, it provides the lowest interrupt latency and efficient processing of late arriving interrupts.

7.1.1 Features

The NVIC supports the following features:

- 32 interrupt nodes
- 4 programmable priority levels for each interrupt node
- Support for interrupt tail-chaining and late-arrival
- Software interrupt generation

7.1.2 Interrupt Node Assignment

Table 30 lists the service request sources per peripheral and their assignment to NVIC interrupt nodes. For calculation of the vector routine address, please refer to the section on Vector Table in the CPU chapter.

Each node can be assigned one of the following, as shown in ***Figure 18***:

- Service Request Source A
- Service Request Source B
- Service Request Source C
- Service Request Source A OR B

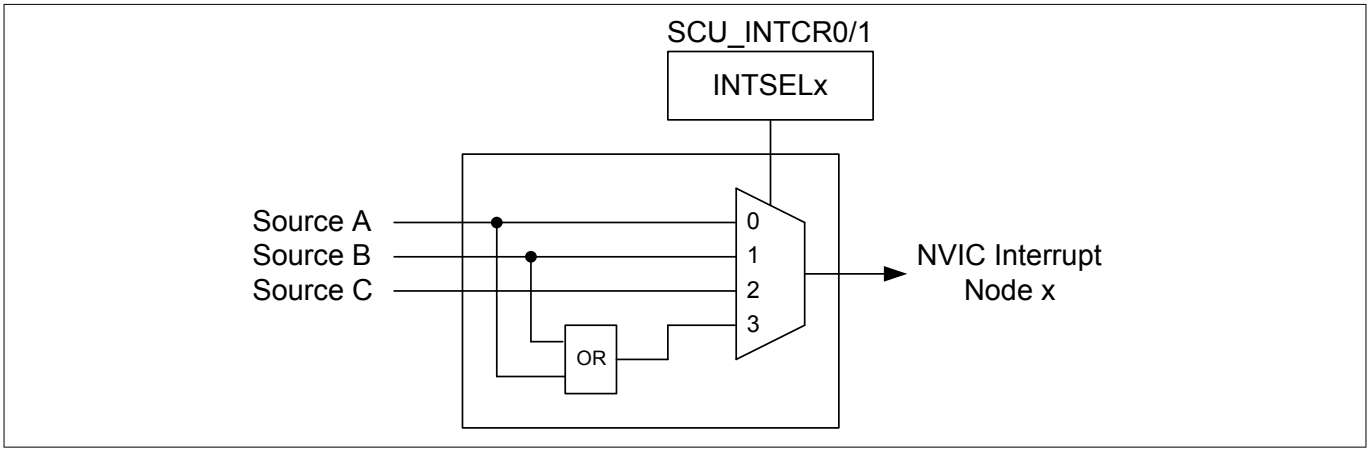


Figure 18 Source Selection per Interrupt Node

The selection is done through the bit field INTSELx (x=0-31) corresponding to the interrupt node in the SCU registers INTCR0 and INTCR1. Refer to ***Chapter 7.3.2*** for the register description.

Table 30 Interrupt Node assignment

Node ID	Service Request Source A	Service Request Source B	Service Request Source C
0	SCU.SR0	CAN0.SR0	CCU40.SR0
1	SCU.SR1	CAN0.SR1	CCU80.SR0
2	SCU.SR2	CAN0.SR2	CCU80.SR1
3	ERU0.SR0	ERU1.SR0	CAN0.SR0
4	ERU0.SR1	ERU1.SR1	CAN0.SR1
5	ERU0.SR2	ERU1.SR2	CAN0.SR2
6	ERU0.SR3	ERU1.SR3	CAN0.SR3
7	MATH.SR0	CAN0.SR3	CCU40.SR1
8	-	CCU40.SR0	CCU80.SR0
9	USIC0.SR0	USIC1.SR0	ERU0.SR0
10	USIC0.SR1	USIC1.SR1	ERU0.SR1
11	USIC0.SR2	USIC1.SR2	ERU0.SR2
12	USIC0.SR3	USIC1.SR3	ERU0.SR3
13	USIC0.SR4	USIC1.SR4	CCU80.SR1
14	USIC0.SR5	USIC1.SR5	POSIF0.SR0
15	VADC0.C0SR0	USIC0.SR0	POSIF0.SR1
16	VADC0.C0SR1	USIC0.SR1	CCU40.SR2
17	VADC0.G0SR0	USIC0.SR2	CAN0.SR0
18	VADC0.G0SR1	USIC0.SR3	CAN0.SR1
19	VADC0.G1SR0	USIC0.SR4	CAN0.SR2
20	VADC0.G1SR1	USIC0.SR5	CAN0.SR3
21	CCU40.SR0	CCU41.SR0	USIC0.SR0
22	CCU40.SR1	CCU41.SR1	USIC0.SR1
23	CCU40.SR2	CCU41.SR2	USIC0.SR2
24	CCU40.SR3	CCU41.SR3	USIC0.SR3
25	CCU80.SR0	CCU81.SR0	USIC0.SR4
26	CCU80.SR1	CCU81.SR1	USIC0.SR5
27	POSIF0.SR0	POSIF1.SR0	CCU40.SR3
28	POSIF0.SR1	POSIF1.SR1	ERU0.SR0
29	-	CCU40.SR1	ERU0.SR1
30	-	CCU40.SR2	ERU0.SR2
31	-	CCU40.SR3	ERU0.SR3

7.1.3 Interrupt Signal Generation

In IMC300A, all peripherals support only the generation of pulse interrupts. Pulse interrupts are also described as edge-triggered interrupts.

A pulse interrupt is an interrupt signal sampled synchronously on the rising edge of the processor clock (MCLK). To ensure the NVIC detects the interrupt, the peripheral asserts the interrupt signal for at least one MCLK clock cycle, during which the NVIC detects the pulse and latches the interrupt.

When the processor enters the ISR, it automatically removes the pending state from the interrupt, see ***Hardware and software control of interrupts***.

The processor automatically stacks its state on exception entry and unstacks this state on exception exit, with no instruction overhead. This provides low latency exception handling.

Hardware and software control of interrupts

The Cortex-M0 latches all interrupts. A peripheral interrupt becomes pending for one of the following reasons:

- the NVIC detects that the interrupt signal is active and the interrupt is not active
- the NVIC detects a rising edge on the interrupt signal
- software writes to the corresponding interrupt set-pending register bit, see Interrupt Set-pending Register NVIC_ISPR.

A pending interrupt remains pending until one of the following:

- The processor enters the ISR for the interrupt. This changes the state of the interrupt from pending to active. Then:
  - The NVIC continues to monitor the interrupt signal, and If this is pulsed the state of the interrupt changes to pending and active. In this case, when the processor returns from the ISR the state of the interrupt changes to pending, which might cause the processor to immediately re-enter the ISR.

    If the interrupt signal is not pulsed while the processor is in the ISR, the state of the interrupt changes to inactive when the processor returns from the ISR.
- Software writes to the corresponding interrupt clear-pending register bit.
  - The state of the interrupt changes to inactive, if the state was pending; or active, if the state was active and pending.

7.1.4 NVIC design hints and tips

An interrupt node can enter pending state even if it is disabled. Disabling an interrupt node only prevents the processor from taking interrupts from that node.

NVIC programming hints

Software uses the CPSIE i and CPSID i instructions to enable and disable interrupts. The CMSIS provides the following intrinsic functions for these instructions:

```
void __disable_irq(void) // Disable Interrupts
void __enable_irq(void) // Enable Interrupts
```

In addition, the CMSIS provides a number of functions for NVIC control, including:

Table 31 CMSIS functions for NVIC control

CMSIS interrupt control function	Description
void NVIC_EnableIRQ (IRQn_t IRQn)	Enable IRQn
void NVIC_DisableIRQ (IRQn_t IRQn)	Disable IRQn
uint32_t NVIC_GetPendingIRQ (IRQn_t IRQn)	Return true (1) if IRQn is pending
void NVIC_SetPendingIRQ (IRQn_t IRQn)	Set IRQn pending

Table 31 CMSIS functions for NVIC control (continued)

CMSIS interrupt control function	Description
void NVIC_ClearPendingIRQ (IRQn_t IRQn)	Clear IRQn pending status
void NVIC_SetPriority (IRQn_t IRQn, uint32_t priority)	Set priority for IRQn
uint32_t NVIC_GetPriority (IRQn_t IRQn)	Read priority of IRQn
void NVIC_SystemReset (void)	Reset the system

The input parameter IRQn is the IRQ number. For more information about these functions, please refer to the CMSIS documentation.

7.1.5 Accessing CPU Registers using CMSIS

CMSIS functions enable software portability between different Cortex-M profile processors. To access the NVIC registers when using CMSIS, use the following functions:

Table 32 CMSIS access NVIC functions

CMSIS function	Description
void NVIC_EnableIRQ (IRQn_Type IRQn)[16]	Enables an interrupt or exception.
void NVIC_DisableIRQ (IRQn_Type IRQn)[16]	Disables an interrupt or exception.
void NVIC_SetPendingIRQ (IRQn_Type IRQn)[16]	Sets the pending status of interrupt or exception to 1.
void NVIC_ClearPendingIRQ (IRQn_Type IRQn)[16]	Clears the pending status of interrupt or exception to 0.
uint32_t NVIC_GetPendingIRQ (IRQn_Type IRQn)[16]	Reads the pending status of interrupt or exception. This function returns non-zero value if the pending status is set to 1.
void NVIC_SetPriority(IRQn_Type IRQn, uint32_t priority)[16]	Sets the priority of an interrupt or exception with configurable priority level to 1.
uint32_t NVIC_GetPriority(IRQn_Type IRQn)[16]	Reads the priority of an interrupt or exception with configurable priority level. This function return the current priority level.

7.1.6 Interrupt Priority

An interrupt node can be assigned one of four priority levels. The levels are in steps of 64, from 0 to 192, and defined in an 8-bit priority field in the Interrupt Priority Register x (IPRx). A higher level corresponds to a lower priority, so level 0 is the highest interrupt priority.

Since there are four priority fields in each IPRx register and each field corresponds to one interrupt node, altogether 8 IPRx registers (IPR0...IPR7) are needed as shown in ***Figure 19***.

16 The input parameter IRQn is the IRQ number.

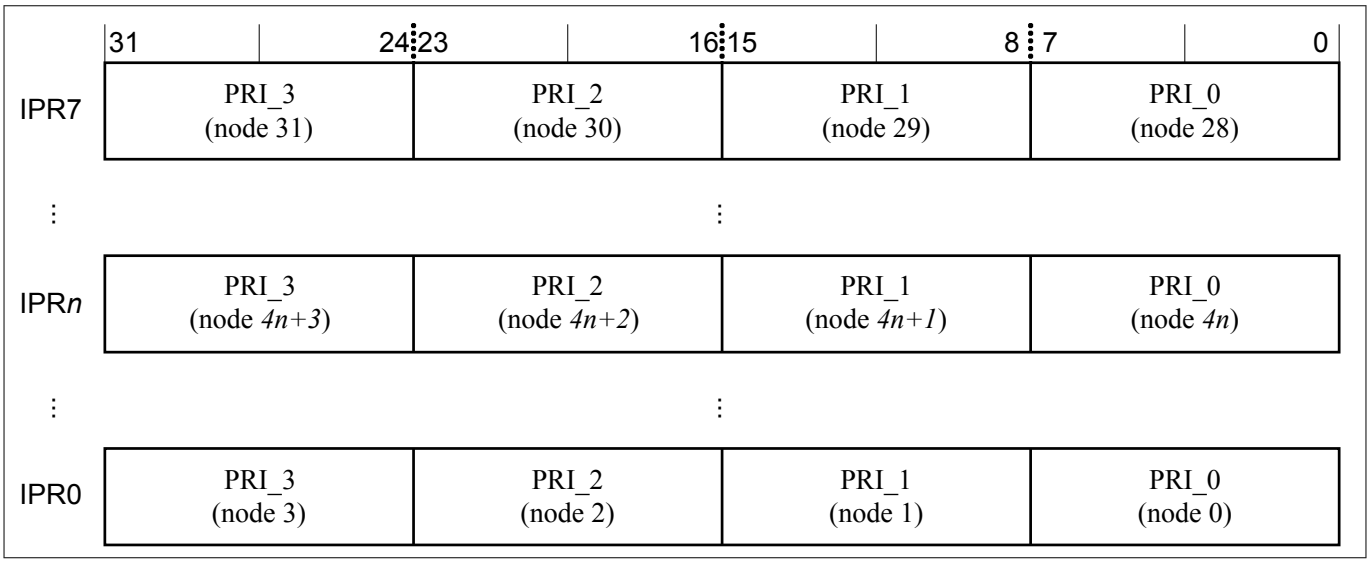


Figure 19 Interrupt Priority Register

The IPR number and byte offset for interrupt node m (0...31) can be found as follows:

- the corresponding IPR number n is given by
  - n = m DIV 4
- the byte offset of the required Priority field in this register is m MOD 4, where:
  - byte offset 0 refers to register bits [7:0]
  - byte offset 1 refers to register bits [15:8]
  - byte offset 2 refers to register bits [23:16]
  - byte offset 3 refers to register bits [31:24]
- for example, Priority field of interrupt node 21 is located at IPR5.[15:8], since
  - n = 21 DIV 4 = 5
  - byte offset = 21 MOD 4 = 1

Note: IPRx registers are only word-accessible.

Refer to ***Table 31*** for more information on the access to the interrupt node priority array, which provides the software view of the interrupt node priorities.

7.1.7 Interrupt Latency

The IMC300A interrupt latency, defined as the time from detection of the generated pulse and latching of the interrupt by NVIC to execution of the first instruction at the interrupt handler, is typically 21 MCLK cycles as shown in ***Figure 20***.

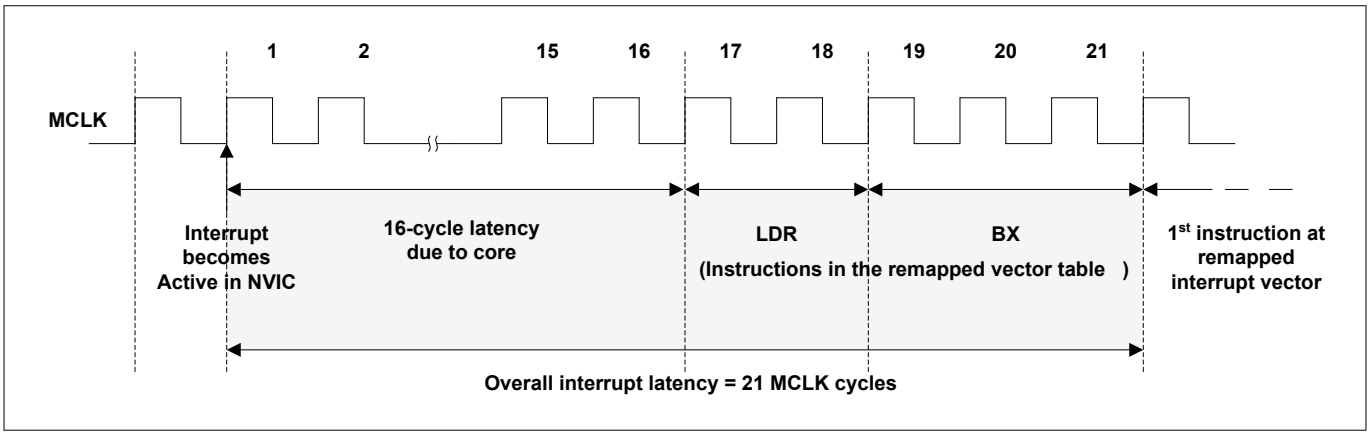


Figure 20 Typical IMC300A Interrupt Latency

This assumes the following conditions:

- Interrupt generation is enabled
- No occurrence of interrupt pre-emption, late-arrival or tail-chaining
- Delays due to memory wait states are not taken into account

7.2 General Module Interrupt Structure

A module might have multiple interrupt sources. Each interrupt source has typically the following structure (see ***Figure 21***):

- An interrupt source status flag
- A set bit to allow software to set the flag to 1
- A clear bit to allow software to reset the flag to 0
- An enable bit to trigger interrupt when the hardware event occurs or status flag set bit is set (i.e. software triggered interrupt)

Note: If a flag set event (due to a peripheral HW event) occurs in the same clock cycle as a flag clear event (due to SW Setting of the Clear bit), the set has higher priority over the clear.

Note: Setting of the status flag by a hardware event or software writing to status flag set bit, is independent of interrupt generation enabled/disabled. Similarly, interrupt generation is independent of the level of the status flag.

Additionally, some modules might have more interrupt sources than interrupt lines. Therefore, they include an interrupt routing management block, which maps the interrupt sources to the interrupt lines.

For further details and exceptions to the above general structure, refer to the respective module chapters.

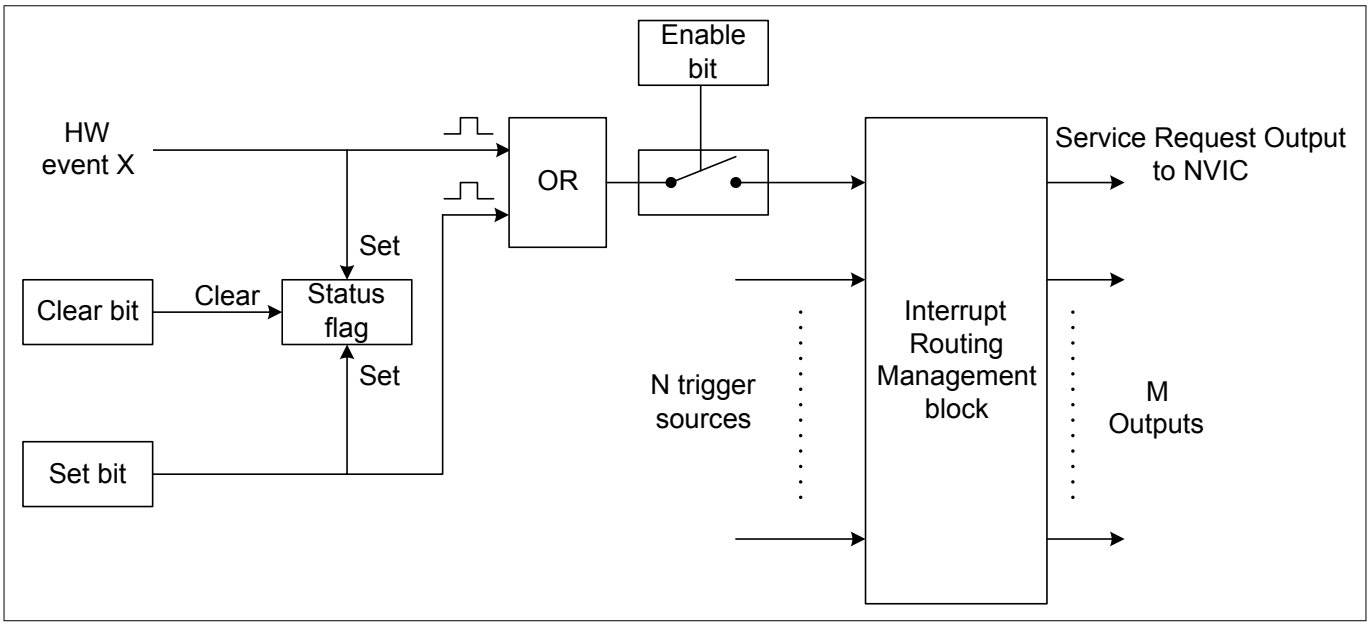


Figure 21 Typical Module Interrupt Structure

To enable a module HW event for interrupt generation, SW has to:

- Select the required module service request source for the interrupt node, through the SCU_INTCRx registers.
- Enable the interrupt node through the NVIC_ISER register.
- If the module has an interrupt routing management block, select an available service request output through which the interrupt will be generated to the NVIC. This is usually done by configuring a interrupt node pointer register in the module.
- Finally, set the interrupt enable bit of the module HW event for interrupt generation.

7.3 Registers

Table 33 Registers Address Space

Module	Base Address	End Address	Note
CPU PPB: System Control Space (SCS)	$E000E000_H$	$E000EFFF_H$	
SCU General Control Unit Registers	40010000_H	$40011FFF_H$	

Registers Overview

The absolute register address is calculated by adding:
Module Base Address + Offset Address

Table 34 Register Overview

Short Name	Description	Offset Address	Access Mode		Description See
			Read	Write	
Nested Vectored Interrupt Controller (NVIC)					
NVIC_ISER	Interrupt Set-enable Registers	100_H	U, PV	U, PV	Page 131

Table 34 Register Overview (continued)

Short Name	Description	Offset Address	Access Mode		Description See
			Read	Write	
NVIC_ICER	Interrupt Clear-enable Registers	180_H	U, PV	U, PV	Page 131
NVIC_ISPR	Interrupt Set-pending Registers	200_H	U, PV	U, PV	Page 132
NVIC_ICPR	Interrupt Clear-pending Registers	280_H	U, PV	U, PV	Page 132
NVIC_IPR0 - NVIC_IPR7	Interrupt Priority Registers	400_H-$41C_H$	U, PV	U, PV	Page 133
SCU Interrupt Related Registers					
SCU_INTCR0	Interrupt Control Register 0	$6C_H$	U, PV	U, PV	Page 134
SCU_INTCR1	Interrupt Control Register 1	70_H	U, PV	U, PV	Page 134

7.3.1 NVIC Registers

7.3.1.1 Register NVIC_ISER

The ISER register enables interrupt nodes, and shows which interrupt nodes are enabled.

NVIC_ISER Address: $E000E100_H$

Interrupt Set-enable Register Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SETENA															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETENA															
rw															

Field	Bits	Type	Description
SETENA	31:0	rw	**Interrupt Node Set-enable** 0_B Read: Interrupt node disabled. Write: No effect. 1_B Read: Interrupt node enabled. Write: Enable interrupt node

If a pending interrupt is enabled, the NVIC activates the interrupt based on its priority. If an interrupt is not enabled, asserting its interrupt signal changes the interrupt state to pending, but the NVIC never activates the interrupt, regardless of its priority.

7.3.1.2 Register NVIC_ICER

The ICER register disables interrupt nodes, and shows which interrupt nodes are enabled.

NVIC_ICER Address: $E000E180_H$

IInterrupt Clear-enable Register Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLRENA															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLRENA															
rw															

Field	Bits	Type	Description
CLRENA	31:0	rw	**Interrupt Node Clear-enable** 0_B Read: Interrupt node disabled. Write: No effect 1_B Read: Interrupt node enabled. Write: Disable interrupt node.

7.3.1.3 Register NVIC_ISPR

The ISPR register forces interrupt nodes into the pending state, and shows which interrupt nodes are pending.

NVIC_ISPR Address: $E000E200_H$

Interrupt Set-pending Register Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SETPEND															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETPEND															
rw															

Field	Bits	Type	Description
SETPEND	31:0	rw	**Interrupt Node Set-pending** 0_B Read: Interrupt node is not pending. Write: No effect 1_B Read: Interrupt node is pending. Write: Change interrupt state to pending.

Note: Writing 1 to the ISPR bit corresponding to:

- *an interrupt node that is pending has no effect*
- *a disabled interrupt node sets the state of that interrupt node to pending*

7.3.1.4 Register NVIC_ICPR

The ICPR register removes the pending state from interrupt nodes, and shows which interrupt nodes are pending.

NVIC_ICPR Address: $E000E280_H$

Interrupt Clear-pending Register Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLRPEND															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLRPEND															
rw															

Field	Bits	Type	Description
CLRPEND	31:0	rw	**Interrupt Node Clear-pending** 0_B Read: Interrupt node is not pending. Write: No effect. 1_B Read: Interrupt node is pending. Write: Remove interrupt state from pending.

Note: Writing 1 to an ICPR bit does not affect the active state of the corresponding interrupt node.

7.3.1.5 Register NVIC_IPRx (x=0-7)

The IPR0-IPR7 registers provide a 8-bit priority field for each interrupt node. Each register holds four priority fields.

Each priority field holds a priority value, 0-192. The lower the value, the greater the priority of the corresponding interrupt node. The processor implements only bits [7:6] of each field, bits [5:0] reads as 0 and ignores writes. This means writing 255 to a priority register saves value 192 to the register.

NVIC_IPRx (x=0-7) Address: $E000E400_H + 4*x$

Interrupt Priority Register x Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRI_3								**PRI_2**							
rw								rw							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI_1								**PRI_0**							
rw								rw							

Field	Bits	Type	Description
PRI_3	31:24	rw	**Priority, Byte Offset 3**
PRI_2	23:16	rw	**Priority, Byte Offset 2**
PRI_1	15:8	rw	**Priority, Byte Offset 1**
PRI_0	7:0	rw	**Priority, Byte Offset 0**

7.3.2 SCU Interrupt Related Registers

This section describes the SCU registers INTCR0 and INTCR1, which are used to select the interrupt source for each interrupt node.

These registers are also described in the SCU chapter.

7.3.2.1 Register SCU_INTCR0

This register selects the interrupt source for interrupt node 0 to 15.

SCU_INTCR0 Address: $4001006C_H$

Interrupt Control Register 0 Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTSEL15		**INTSEL14**		**INTSEL13**		**INTSEL12**		**INTSEL11**		**INTSEL10**		**INTSEL9**		**INTSEL8**	
rw		rw		rw		rw		rw		rw		rw		rw	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTSEL7		**INTSEL6**		**INTSEL5**		**INTSEL4**		**INTSEL3**		**INTSEL2**		**INTSEL1**		**INTSEL0**	
rw		rw		rw		rw		rw		rw		rw		rw	

Field	Bits	Type	Description
INTSELx (x=0-15)	2*x+1:2*x	rw	**Interrupt Source Select for Node x** 00_B Select source A. 01_B Select source B 10_B Select source C 11_B Select source A or B

7.3.2.2 Register SCU_INTCR1

This register selects the interrupt source for interrupt node 16 to 31.

SCU_INTCR1 Address: 40010070_H

Interrupt Control Register 1 Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTSEL31		**INTSEL30**		**INTSEL29**		**INTSEL28**		**INTSEL27**		**INTSEL26**		**INTSEL25**		**INTSEL24**	
rw		rw		rw		rw		rw		rw		rw		rw	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTSEL23		**INTSEL22**		**INTSEL21**		**INTSEL20**		**INTSEL19**		**INTSEL18**		**INTSEL17**		**INTSEL16**	
rw		rw		rw		rw		rw		rw		rw		rw	

Field	Bits	Type	Description
INTSELx (x=16-31)	2*x-31:2*x-32	rw	**Interrupt Source Select for Node x** 00_B Select source A. 01_B Select source B 10_B Select source C 11_B Select source A or B

7.4 Interrupt Request Source Overview

An overview of all IMC300A interrupt sources and related register bits are shown in the next few pages.

7.4.1 Interrupt source: SCU.SR0

7.4.1.1 Flash double bit ECC event

Table 35 SCU.SR0 - Flash double bit ECC event

Flash ECC double bit error has two status flags, each having its own clear bit. It is sufficient to use only one of the status flags and ignore the other.

Type	Register	Bits
Interrupt enable	SCU_SRMSK	FLECC2I
	-	-
Status flag	SCU_SRRAW	FLECC2I
	NVM_NVMSTATUS	ECC2READ
Set flag	SCU_SRSET	FLECC2I
	-	-
Clear flag	SCU_SRCLR	FLECC2I
	NVM_NVMPROG	RSTECC
Node pointer	-	-
	-	-

7.4.1.2 Flash operation complete event

Table 36 SCU.SR0 - Flash operation complete event

Type	Register	Bits
Interrupt enable	NVM_NVMCONF	INT_ON
Status flag	SCU_SRRAW	FLCMPLTI
Set flag	SCU_SRSET	FLCMPLTI
Clear flag	SCU_SRCLR	FLCMPLTI
Node pointer	-	-

7.4.1.3 SRAM parity error event

Table 37 SCU.SR0 - SRAM parity error event

Type	Register	Bits
Interrupt enable	SCU_SRMSK	PESRAMI
Status flag	SCU_SRRAW	PESRAMI

Table 37 SCU.SR0 - SRAM parity error event (continued)

Type	Register	Bits
Set flag	SCU_SRSET	PESRAMI
Clear flag	SCU_SRCLR	PESRAMI
Node pointer	-	-

7.4.1.4 USIC RAM parity error event

Table 38 SCU.SR0 - USIC RAM parity error event

Type	Register	Bits
Interrupt enable	SCU_SRMSK	PEU0I
Status flag	SCU_SRRAW	PEU0I
Set flag	SCU_SRSET	PEU0I
Clear flag	SCU_SRCLR	PEU0I
Node pointer	-	-

7.4.1.5 Loss of clock event

Table 39 SCU.SR0 - Loss of clock event

Type	Register	Bits
Interrupt enable	SCU_SRMSK	LOCI
Status flag	SCU_SRRAW	LOCI
Set flag	SCU_SRSET	LOCI
Clear flag	SCU_SRCLR	LOCI
Node pointer	-	-

7.4.2 Interrupt source: SCU.SR1

7.4.2.1 Standby clock failure event

Table 40 SCU.SR1 - Standby clock failure event

Type	Register	Bits
Interrupt enable	SCU_SRMSK	SBYCLKFI
Status flag	SCU_SRRAW	SBYCLKFI
Set flag	SCU_SRSET	SBYCLKFI
Clear flag	SCU_SRCLR	SBYCLKFI

Table 40 SCU.SR1 - Standby clock failure event (continued)

Type	Register	Bits
Node pointer	-	-

7.4.2.2 VDDP pre-warning event

Table 41 SCU.SR1 - VDDP pre-warning event

Type	Register	Bits
Interrupt enable	SCU_SRMSK	VDDPI
Status flag	SCU_SRRAW	VDDPI
Set flag	SCU_SRSET	VDDPI
Clear flag	SCU_SRCLR	VDDPI
Node pointer	-	-

7.4.2.3 VDDC drops below VDROP event

Table 42 SCU.SR1 - VDDC drops below VDROP event

Type	Register	Bits
Interrupt enable	SCU_SRMSK	VDROPI
Status flag	SCU_SRRAW	VDROPI
Set flag	SCU_SRSET	VDROPI
Clear flag	SCU_SRCLR	VDROPI
Node pointer	-	-

7.4.2.4 VDDC rises above VCLIP event

Table 43 SCU.SR1 - VDDC rises above VCLIP event

Type	Register	Bits
Interrupt enable	SCU_SRMSK	VCLIPI
Status flag	SCU_SRRAW	VCLIPI
Set flag	SCU_SRSET	VCLIPI
Clear flag	SCU_SRCLR	VCLIPI
Node pointer	-	-

7.4.2.5 DTS done event

Table 44 SCU.SR1 - DTS done event

Type	Register	Bits
Interrupt enable	SCU_SRMSK	TSE_DONE
Status flag	SCU_SRRAW	TSE_DONE
Set flag	SCU_SRSET	TSE_DONE
Clear flag	SCU_SRCLR	TSE_DONE
Node pointer	-	-

7.4.2.6 DTS compare high event

Table 45 SCU.SR1 - DTS compare high event

Type	Register	Bits
Interrupt enable	SCU_SRMSK	TSE_HIGH
Status flag	SCU_SRRAW	TSE_HIGH
Set flag	SCU_SRSET	TSE_HIGH
Clear flag	SCU_SRCLR	TSE_HIGH
Node pointer	-	-

7.4.2.7 DTS compare low event

Table 46 SCU.SR1 - DTS compare low event

Type	Register	Bits
Interrupt enable	SCU_SRMSK	TSE_LOW
Status flag	SCU_SRRAW	TSE_LOW
Set flag	SCU_SRSET	TSE_LOW
Clear flag	SCU_SRCLR	TSE_LOW
Node pointer	-	-

7.4.2.8 WDT pre-warning event

Table 47 SCU.SR1 - WDT pre-warning event

Type	Register	Bits
Interrupt enable	SCU_SRMSK	PRWARN
Status flag	SCU_SRRAW	PRWARN
Set flag	SCU_SRSET	PRWARN

Table 47 SCU.SR1 - WDT pre-warning event (continued)

Type	Register	Bits
Clear flag	SCU_SRCLR	PRWARN
Node pointer	-	-

7.4.2.9 RTC periodic event

Table 48 SCU.SR1 - RTC periodic event

Type	Register	Bits
Interrupt enable	-	-
Status flag	SCU_SRRAW	PI
Set flag	SCU_SRSET	PI
Clear flag	SCU_SRCLR	PI
Node pointer	-	-

7.4.2.10 RTC alarm event

Table 49 SCU.SR1 - RTC alarm event

Type	Register	Bits
Interrupt enable	-	-
Status flag	SCU_SRRAW	AI
Set flag	SCU_SRSET	AI
Clear flag	SCU_SRCLR	AI
Node pointer	-	-

7.4.2.11 RTC CTR Mirror Register updated event

Table 50 SCU.SR1 - RTC CTR Mirror Register updated event

Type	Register	Bits
Interrupt enable	SCU_SRMSK	RTC_CTR
Status flag	SCU_SRRAW	RTC_CTR
Set flag	SCU_SRSET	RTC_CTR
Clear flag	SCU_SRCLR	RTC_CTR
Node pointer	-	-

7.4.2.12 RTC ATIM0 Mirror Register updated event

Table 51 SCU.SR1 - RTC ATIM0 Mirror Register updated event

Type	Register	Bits
Interrupt enable	SCU_SRMSK	RTC_ATIM0
Status flag	SCU_SRRAW	RTC_ATIM0
Set flag	SCU_SRSET	RTC_ATIM0
Clear flag	SCU_SRCLR	RTC_ATIM0
Node pointer	-	-

7.4.2.13 RTC ATIM1 Mirror Register updated event

Table 52 SCU.SR1 - RTC ATIM1 Mirror Register updated event

Type	Register	Bits
Interrupt enable	SCU_SRMSK	RTC_ATIM1
Status flag	SCU_SRRAW	RTC_ATIM1
Set flag	SCU_SRSET	RTC_ATIM1
Clear flag	SCU_SRCLR	RTC_ATIM1
Node pointer	-	-

7.4.2.14 RTC TIM0 Mirror Register updated event

Table 53 SCU.SR1 - RTC TIM0 Mirror Register updated event

Type	Register	Bits
Interrupt enable	SCU_SRMSK	RTC_TIM0
Status flag	SCU_SRRAW	RTC_TIM0
Set flag	SCU_SRSET	RTC_TIM0
Clear flag	SCU_SRCLR	RTC_TIM0
Node pointer	-	-

7.4.2.15 RTC TIM1 Mirror Register updated event

Table 54 SCU.SR1 - RTC TIM1 Mirror Register updated event

Type	Register	Bits
Interrupt enable	SCU_SRMSK	RTC_TIM1
Status flag	SCU_SRRAW	RTC_TIM1
Set flag	SCU_SRSET	RTC_TIM1

Table 54 SCU.SR1 - RTC TIM1 Mirror Register updated event (continued)

Type	Register	Bits
Clear flag	SCU_SRCLR	RTC_TIM1
Node pointer	-	-

7.4.3 Interrupt source: SCU.SR2

7.4.3.1 Out of range comparator x event (x=0,4,6,7)

Table 55 SCU.SR2 - Out of range comparator x event (x=0,4,6,7)

Type	Register	Bits
Interrupt enable	SCU_SRMSK	ORCxI
Status flag	SCU_SRRAW	ORCxI
Set flag	SCU_SRSET	ORCxI
Clear flag	SCU_SRCLR	ORCxI
Node pointer	-	-

7.4.3.2 Analog comparator x event (x=0-2)

Table 56 SCU.SR2 - Analog comparator x event (x=0-2)

Type	Register	Bits
Interrupt enable	SCU_SRMSK	ACMPxI
Status flag	SCU_SRRAW	ACMPxI
Set flag	SCU_SRSET	ACMPxI
Clear flag	SCU_SRCLR	ACMPxI
Node pointer	-	-

7.4.4 Interrupt source: ERUx.SR[3:0] (x=0-1)

7.4.4.1 ERUx_IOUTy (y=0-3)

See chapter on ERUx for details.

7.4.5 Interrupt source: MATH.SR0

7.4.5.1 CORDIC end of calculation event

Table 57 MATH.SR0 - CORDIC end of calculation event

Type	Register	Bits
Interrupt enable	MATH_EVIER	CDEOCIEN
Status flag	MATH_EVFR	CDEOC
Set flag	MATH_EVFSR	CDEOCS
Clear flag	MATH_EVFCR	CDEOCC
Node pointer	-	-

7.4.5.2 CORDIC error event

Table 58 MATH.SR0 - CORDIC error event

Type	Register	Bits
Interrupt enable	MATH_EVIER	CDERRIEN
Status flag	MATH_EVFR	CDERR
Set flag	MATH_EVFSR	CDERRS
Clear flag	MATH_EVFCR	CDERRS
Node pointer	-	-

7.4.5.3 DIV end of calculation event

Table 59 MATH.SR0 - DIV end of calculation event

Type	Register	Bits
Interrupt enable	MATH_EVIER	DIVEOCIEN
Status flag	MATH_EVFR	DIVEOC
Set flag	MATH_EVFSR	DIVEOCS
Clear flag	MATH_EVFCR	DIVEOCC
Node pointer	-	-

7.4.5.4 DIV error event

Table 60 MATH.SR0 - DIV error event

Type	Register	Bits
Interrupt enable	MATH_EVIER	DIVERRIEN
Status flag	MATH_EVFR	DIVERR
Set flag	MATH_EVFSR	DIVERRS
Clear flag	MATH_EVFCR	DIVERRC
Node pointer	-	-

7.4.6 Interrupt source: USICx_SR[5:0] (x=0-1)

7.4.6.1 USIC: Standard receive event

Table 61 USICx_SR[5:0] (x=0-1) - USIC: Standard receive event

Type	Register	Bits
Interrupt enable	USICx_CHy_CCR	RIEN
Status flag	USICx_CHy_PSR	RIF
Set flag	-	-
Clear flag	USICx_CHy_PSCR	CRIF
Node pointer	USICx_CHy_INPR	RINP

7.4.6.2 USIC: Receive start event

Table 62 USICx_SR[5:0] (x=0-1) - USIC: Receive start event

Type	Register	Bits
Interrupt enable	USICx_CHy_CCR	RSIEN
Status flag	USICx_CHy_PSR	RSIF
Set flag	-	-
Clear flag	USICx_CHy_PSCR	CRSIF
Node pointer	USICx_CHy_INPR	TBINP

7.4.6.3 USIC: Alternate receive event

Table 63 USICx_SR[5:0] (x=0-1) - USIC: Alternate receive event

Type	Register	Bits
Interrupt enable	USICx_CHy_CCR	AIEN

Table 63 USICx_SR[5:0] (x=0-1) - USIC: Alternate receive event (continued)

Type	Register	Bits
Status flag	USICx_CHy_PSR	AIF
Set flag	-	-
Clear flag	USICx_CHy_PSCR	CAIF
Node pointer	USICx_CHy_INPR	AINP

7.4.6.4 USIC: Transmit shift event

Table 64 USICx_SR[5:0] (x=0-1) - USIC: Transmit shift event

Type	Register	Bits
Interrupt enable	USICx_CHy_CCR	TSIEN
Status flag	USICx_CHy_PSR	TSIF
Set flag	-	-
Clear flag	USICx_CHy_PSCR	CTSIF
Node pointer	USICx_CHy_INPR	TSINP

7.4.6.5 USIC: Transmit buffer event

Table 65 USICx_SR[5:0] (x=0-1) - USIC: Transmit buffer event

Type	Register	Bits
Interrupt enable	USICx_CHy_CCR	TBIEN
Status flag	USICx_CHy_PSR	TBIF
Set flag	-	-
Clear flag	USICx_CHy_PSCR	CTBIF
Node pointer	USICx_CHy_INPR	TBINP

7.4.6.6 USIC: Data lost event

Table 66 USICx_SR[5:0] (x=0-1) - USIC: Data lost event

Type	Register	Bits
Interrupt enable	USICx_CHy_CCR	DLIEN
Status flag	USICx_CHy_PSR	DLIF
Set flag	-	-
Clear flag	USICx_CHy_PSCR	CDLIF
Node pointer	USICx_CHy_INPR	PINP

7.4.6.7 USIC: BRG event

Table 67 USICx_SR[5:0] (x=0-1) - USIC: BRG event

Type	Register	Bits
Interrupt enable	USICx_CHy_CCR	BRGIEN
Status flag	USICx_CHy_PSR	BRGIF
Set flag	-	-
Clear flag	USICx_CHy_PSCR	CBRGIF
Node pointer	USICx_CHy_INPR	PINP

7.4.6.8 USIC: Standard transmit buffer event

Table 68 USICx_SR[5:0] (x=0-1) - USIC: Standard transmit buffer event

Type	Register	Bits
Interrupt enable	USICx_CHy_TBCTR	STBIEN
Status flag	USICx_CHy_TRBSR	STBI
Set flag	-	-
Clear flag	USICx_CHy_TRBSCR	CSTBI
Node pointer	USICx_CHy_TBCTR	STBINP

Table 69 USICx_SR[5:0] (x=0-1) - USIC: Standard transmit buffer event

Type	Register	Bits
Interrupt enable	USICx_CHy_TBCTR	STBIEN
Status flag	USICx_CHy_TRBSR	STBT
Set flag	-	-
Clear flag	-	-
Node pointer	USICx_CHy_TBCTR	STBINP

7.4.6.9 USIC: Transmit Buffer error event

Table 70 USICx_SR[5:0] (x=0-1) - USIC: Transmit Buffer error event

Type	Register	Bits
Interrupt enable	USICx_CHy_TBCTR	TBERIEN
Status flag	USICx_CHy_TRBSR	TBERI
Set flag	-	-
Clear flag	USICx_CHy_TRBSCR	CTBERI
Node pointer	USICx_CHy_TBCTR	ATBINP

7.4.6.10 USIC: Standard receive buffer event

Table 71 USICx_SR[5:0] (x=0-1) - USIC: Standard receive buffer event

Type	Register	Bits
Interrupt enable	USICx_CHy_RBCTR	SRBIEN
Status flag	USICx_CHy_TRBSR	SRBI
Set flag	-	-
Clear flag	USICx_CHy_TRBSCR	CSRBI
Node pointer	USICx_CHy_RBCTR	SRBINP

Table 72 USICx_SR[5:0] (x=0-1) - USIC: Standard receive buffer event

Type	Register	Bits
Interrupt enable	USICx_CHy_RBCTR	SRBIEN
Status flag	USICx_CHy_TRBSR	SRBT
Set flag	-	-
Clear flag	-	-
Node pointer	USICx_CHy_RBCTR	SRBINP

7.4.6.11 USIC: Alternate receive buffer event

Table 73 USICx_SR[5:0] (x=0-1) - USIC: Alternate receive buffer event

Type	Register	Bits
Interrupt enable	USICx_CHy_RBCTR	ARBIEN
Status flag	USICx_CHy_TRBSR	ARBI
Set flag	-	-
Clear flag	USICx_Chy_TRBSCR	CARBI
Node pointer	USICx_CHy_RBCTR	ARBINP

7.4.6.12 USIC: Receive buffer error event

Table 74 USICx_SR[5:0] (x=0-1) - USIC: Receive buffer error event

Type	Register	Bits
Interrupt enable	USICx_CHy_RBCTR	RBERIEN
Status flag	USICx_CHy_TRBSR	RBERI
Set flag	-	-
Clear flag	USICx_Chy_TRBSCR	CRBERI
Node pointer	USICx_CHy_RBCTR	ARBINP

7.4.6.13 ASC: Synchronisation break detected event

Table 75 USICx_SR[5:0] (x=0-1) - ASC: Synchronisation break detected event

Type	Register	Bits
Interrupt enable	USICx_CHy_PCR	SBDIEN
Status flag	USICx_CHy_PSR	SBD
Set flag	-	-
Clear flag	USICx_CHy_PSCR	CSBD
Node pointer	USICx_CHy_INPR	PINP

7.4.6.14 ASC: Collision detected event

Table 76 USICx_SR[5:0] (x=0-1) - ASC: Collision detected event

Type	Register	Bits
Interrupt enable	USICx_CHy_PCR	CDIEN
Status flag	USICx_CHy_PSR	COL
Set flag	-	-
Clear flag	USICx_CHy_PSCR	CCOL
Node pointer	USICx_CHy_INPR	PINP

7.4.6.15 ASC: Receiver noise detected event

Table 77 USICx_SR[5:0] (x=0-1) - ASC: Receiver noise detected event

Type	Register	Bits
Interrupt enable	USICx_CHy_PCR	RNIEN
Status flag	USICx_CHy_PSR	RNS
Set flag	-	-
Clear flag	USICx_CHy_PSCR	CRNS
Node pointer	USICx_CHy_INPR	PINP

7.4.6.16 ASC: Format error in stop bit 0 event

Table 78 USICx_SR[5:0] (x=0-1) - ASC: Format error in stop bit 0 event

Type	Register	Bits
Interrupt enable	USICx_CHy_PCR	FEIEN
Status flag	USICx_CHy_PSR	FER0
Set flag	-	-

Table 78 USICx_SR[5:0] (x=0-1) - ASC: Format error in stop bit 0 event (continued)

Type	Register	Bits
Clear flag	USICx_CHy_PSCR	CFER0
Node pointer	USICx_CHy_INPR	PINP

7.4.6.17 ASC: Format error in stop bit 1 event

Table 79 USICx_SR[5:0] (x=0-1) - ASC: Format error in stop bit 1 event

Type	Register	Bits
Interrupt enable	USICx_CHy_PCR	FEIEN
Status flag	USICx_CHy_PSR	FER1
Set flag	-	-
Clear flag	USICx_CHy_PSCR	CFER1
Node pointer	USICx_CHy_INPR	PINP

7.4.6.18 ASC: Receive frame finished event

Table 80 USICx_SR[5:0] (x=0-1) - ASC: Receive frame finished event

Type	Register	Bits
Interrupt enable	USICx_CHy_PCR	FFIEN
Status flag	USICx_CHy_PSR	RFF
Set flag	-	-
Clear flag	USICx_CHy_PSCR	CRFF
Node pointer	USICx_CHy_INPR	PINP

7.4.6.19 ASC: Transmit frame finished event

Table 81 USICx_SR[5:0] (x=0-1) - ASC: Transmit frame finished event

Type	Register	Bits
Interrupt enable	USICx_CHy_PCR	FFIEN
Status flag	USICx_CHy_PSR	TFF
Set flag	-	-
Clear flag	USICx_CHy_PSCR	CTFF
Node pointer	USICx_CHy_INPR	PINP

7.4.6.20 SSC: MSLS event detected event

Table 82 USICx_SR[5:0] (x=0-1) - SSC: MSLS event detected event

Type	Register	Bits
Interrupt enable	USICx_CHy_PCR	MSLSIEN
Status flag	USICx_CHy_PSR	MSLSEV
Set flag	-	-
Clear flag	USICx_CHy_PSCR	CMSLSEV
Node pointer	USICx_CHy_INPR	PINP

7.4.6.21 SSC: Parity error detected event

Table 83 USICx_SR[5:0] (x=0-1) - SSC: Parity error detected event

Type	Register	Bits
Interrupt enable	USICx_CHy_PCR	PARIEN
Status flag	USICx_CHy_PSR	PAERR
Set flag	-	-
Clear flag	USICx_CHy_PSCR	CPAERR
Node pointer	USICx_CHy_INPR	PINP

7.4.6.22 SSC: DX2T event detected event

Table 84 USICx_SR[5:0] (x=0-1) - SSC: DX2T event detected event

Type	Register	Bits
Interrupt enable	USICx_CHy_PCR	DX2TIEN
Status flag	USICx_CHy_PSR	DX2TEV
Set flag	-	-
Clear flag	USICx_CHy_PSCR	CDX2TEV
Node pointer	USICx_CHy_INPR	PINP

7.4.6.23 IIC: Wrong TDF code detected event

Table 85 USICx_SR[5:0] (x=0-1) - IIC: Wrong TDF code detected event

Type	Register	Bits
Interrupt enable	USICx_CHy_PCR	ERRIEN
Status flag	USICx_CHy_PSR	WTDF
Set flag	-	-

Table 85 USICx_SR[5:0] (x=0-1) - IIC: Wrong TDF code detected event (continued)

Type	Register	Bits
Clear flag	USICx_CHy_PSCR	CWTDF
Node pointer	USICx_CHy_INPR	PINP

7.4.6.24 IIC: Start condition received event

Table 86 USICx_SR[5:0] (x=0-1) - IIC: Start condition received event

Type	Register	Bits
Interrupt enable	USICx_CHy_PCR	SCRIEN
Status flag	USICx_CHy_PSR	SCR
Set flag	-	-
Clear flag	USICx_CHy_PSCR	CSCR
Node pointer	USICx_CHy_INPR	PINP

7.4.6.25 IIC: Repeated start condition received event

Table 87 USICx_SR[5:0] (x=0-1) - IIC: Repeated start condition received event

Type	Register	Bits
Interrupt enable	USICx_CHy_PCR	RSCRIEN
Status flag	USICx_CHy_PSR	RSCR
Set flag	-	-
Clear flag	USICx_CHy_PSCR	CRSCR
Node pointer	USICx_CHy_INPR	PINP

7.4.6.26 IIC: Stop condition received event

Table 88 USICx_SR[5:0] (x=0-1) - IIC: Stop condition received event

Type	Register	Bits
Interrupt enable	USICx_CHy_PCR	PCRIEN
Status flag	USICx_CHy_PSR	PCR
Set flag	-	-
Clear flag	USICx_CHy_PSCR	CPCR
Node pointer	USICx_CHy_INPR	PINP

7.4.6.27 IIC: NACK received event

Table 89 USICx_SR[5:0] (x=0-1) - IIC: NACK received event

Type	Register	Bits
Interrupt enable	USICx_CHy_PCR	NACKIEN
Status flag	USICx_CHy_PSR	NACK
Set flag	-	-
Clear flag	USICx_CHy_PSCR	CNACK
Node pointer	USICx_CHy_INPR	PINP

7.4.6.28 IIC: Arbitration lost event

Table 90 USICx_SR[5:0] (x=0-1) - IIC: Arbitration lost event

Type	Register	Bits
Interrupt enable	USICx_CHy_PCR	ARLIEN
Status flag	USICx_CHy_PSR	ARL
Set flag	-	-
Clear flag	USICx_CHy_PSCR	CARL
Node pointer	USICx_CHy_INPR	PINP

7.4.6.29 IIC: Slave read request event

Table 91 USICx_SR[5:0] (x=0-1) - IIC: Slave read request event

Type	Register	Bits
Interrupt enable	USICx_CHy_PCR	SRRIEN
Status flag	USICx_CHy_PSR	SRR
Set flag	-	-
Clear flag	USICx_CHy_PSCR	CSRR
Node pointer	USICx_CHy_INPR	PINP

7.4.6.30 IIC: Error detected event

Table 92 USICx_SR[5:0] (x=0-1) - IIC: Error detected event

Type	Register	Bits
Interrupt enable	USICx_CHy_PCR	ERRIEN
Status flag	USICx_CHy_PSR	ERR
Set flag	-	-

Table 92 USICx_SR[5:0] (x=0-1) - IIC: Error detected event (continued)

Type	Register	Bits
Clear flag	USICx_CHy_PSCR	CERR
Node pointer	USICx_CHy_INPR	PINP

7.4.6.31 IIC: ACK received event

Table 93 USICx_SR[5:0] (x=0-1) - IIC: ACK received event

Type	Register	Bits
Interrupt enable	USICx_CHy_PCR	ACKIEN
Status flag	USICx_CHy_PSR	ACK
Set flag	-	-
Clear flag	USICx_CHy_PSCR	CACK
Node pointer	USICx_CHy_INPR	PINP

7.4.6.32 IIS: DX2T event detected event

Table 94 USICx_SR[5:0] (x=0-1) - IIS: DX2T event detected event

Type	Register	Bits
Interrupt enable	USICx_CHy_PCR	DX2TIEN
Status flag	USICx_CHy_PSR	DX2TEV
Set flag	-	-
Clear flag	USICx_CHy_PSCR	CDX2TEV
Node pointer	USICx_CHy_INPR	PINP

7.4.6.33 IIS: WA falling edge event

Table 95 USICx_SR[5:0] (x=0-1) - IIS: WA falling edge event

Type	Register	Bits
Interrupt enable	USICx_CHy_PCR	WAFEIEN
Status flag	USICx_CHy_PSR	WAFE
Set flag	-	-
Clear flag	USICx_CHy_PSCR	CWAFE
Node pointer	USICx_CHy_INPR	PINP

7.4.6.34 IIS: WA rising edge event

Table 96 USICx_SR[5:0] (x=0-1) - IIS: WA rising edge event

Type	Register	Bits
Interrupt enable	USICx_CHy_PCR	WAREIEN
Status flag	USICx_CHy_PSR	WARE
Set flag	-	-
Clear flag	USICx_CHy_PSCR	CWARE
Node pointer	USICx_CHy_INPR	PINP

7.4.6.35 IIS: WA generation end event

Table 97 USICx_SR[5:0] (x=0-1) - IIS: WA generation end event

Type	Register	Bits
Interrupt enable	USICx_CHy_PCR	ENDIEN
Status flag	USICx_CHy_PSR	END
Set flag	-	-
Clear flag	USICx_CHy_PSCR	CEND
Node pointer	USICx_CHy_INPR	PINP

7.4.7 Interrupt source: VADC0_C0SR[1:0] and VADC0_GxSR[1:0] (x=0-1)

7.4.7.1 Source Event 0 event

Table 98 VADC0_C0SR[1:0] and VADC0_GxSR[1:0] (x=0-1) - Source Event 0 event

Type	Register	Bits
Interrupt enable	VADC0_GxQINR0	ENSI
Status flag	VADC0_GxSEFLAG	SEV0
Set flag	VADC0_GxSEFLAG	SEV0
Clear flag	VADC0_GxSEFCLR	SEV0
Node pointer	VADC0_GxSEVNP	SEV0NP

7.4.7.2 Source Event 1 event

Table 99 VADC0_C0SR[1:0] and VADC0_GxSR[1:0] (x=0-1) - Source Event 1 event

Type	Register	Bits
Interrupt enable	VADC0_GxASMR	ENSI

Table 99 VADC0_C0SR[1:0] and VADC0_GxSR[1:0] (x=0-1) - Source Event 1 event (continued)

Type	Register	Bits
Status flag	VADC0_GxSEFLAG	SEV1
Set flag	VADC0_GxSEFLAG	SEV1
Clear flag	VADC0_GxSEFCLR	SEV1
Node pointer	VADC0_GxSEVNP	SEV1NP

7.4.7.3 Channel Event y (y=0-7) event

Table 100 VADC0_C0SR[1:0] and VADC0_GxSR[1:0] (x=0-1) - Channel Event y (y=0-7) event

Type	Register	Bits
Interrupt enable	VADC0_GxCHCTRy	CHEVMODE
Status flag	VADC0_GxCEFLAG	CEVy
Set flag	VADC0_GxCEFLAG	CEVy
Clear flag	VADC0_GxCEFCLR	CEVy
Node pointer	VADC0_GxCEVNP	CEVyINP

7.4.7.4 Result Event y (y=0-7) event

Table 101 VADC0_C0SR[1:0] and VADC0_GxSR[1:0] (x=0-1) - Result Event y (y=0-7) event

Type	Register	Bits
Interrupt enable	VADC0_GxRCRy	SRGEN
Status flag	VADC0_GxREFLAG	REVy
Set flag	VADC0_GxREFLAG	REVy
Clear flag	VADC0_GxREFCLR	REVy
Node pointer	VADC0_GxREVNP0	REVyNP

7.4.7.5 Result Event y (y=8-15) event

Table 102 VADC0_C0SR[1:0] and VADC0_GxSR[1:0] (x=0-1) - Result Event y (y=8-15) event

Type	Register	Bits
Interrupt enable	VADC0_GxRCRy	SRGEN
Status flag	VADC0_GxREFLAG	REVy
Set flag	VADC0_GxREFLAG	REVy
Clear flag	VADC0_GxREFCLR	REVy
Node pointer	VADC0_GxREVNP1	REVyNP

7.4.7.6 Global Source Event

Table 103 VADC0_C0SR[1:0] and VADC0_GxSR[1:0] (x=0-1) - Global Source Event

Type	Register	Bits
Interrupt enable	VADC0_BRSMR	ENSI
Status flag	VADC0_GLOBEFLAG	SEVGLB
Set flag	VADC0_GLOBEFLAG	SEVGLB
Clear flag	VADC0_GLOBEFLAG	SEVGLBCLR
Node pointer	VADC0_GLOBEVNP	REV0NP

7.4.7.7 Global Result Event

Table 104 VADC0_C0SR[1:0] and VADC0_GxSR[1:0] (x=0-1) - Global Result Event

Type	Register	Bits
Interrupt enable	VADC0_GLOBERCR	SRGEN
Status flag	VADC0_GLOBEFLAG	REVGLB
Set flag	VADC0_GLOBEFLAG	REVGLB
Clear flag	VADC0_GLOBEFLAG	REVGLBCLR
Node pointer	VADC0_GLOBEVNP	SEV0NP

7.4.8 Interrupt source: CCU4x_SR[3:0] (x=0-1)

7.4.8.1 Event 0 edge(s) information from event selector

Table 105 CCU4x_SR[3:0] (x=0-1) - Event 0 edge(s) information from event selector

Type	Register	Bits
Interrupt enable	CCU4x_CC4yINTE	E0AE
Status flag	CCU4x_CC4yINTS	E0AS
Set flag	CCU4x_CC4ySWS	SE0A
Clear flag	CCU4x_CC4ySWR	RE0A
Node pointer	CCU4x_CC4ySRS	E0SR

7.4.8.2 Event 1 edge(s) information from event selector

Table 106 CCU4x_SR[3:0] (x=0-1) - Event 1 edge(s) information from event selector

Type	Register	Bits
Interrupt enable	CCU4x_CC4yINTE	E1AE

Table 106 CCU4x_SR[3:0] (x=0-1) - Event 1 edge(s) information from event selector (continued)

Type	Register	Bits
Status flag	CCU4x_CC4yINTS	E1AS
Set flag	CCU4x_CC4ySWS	SE1A
Clear flag	CCU4x_CC4ySWR	RE1A
Node pointer	CCU4x_CC4ySRS	E1SR

7.4.8.3 Event 2 edge(s) information from event selector

Table 107 CCU4x_SR[3:0] (x=0-1) - Event 2 edge(s) information from event selector

Type	Register	Bits
Interrupt enable	CCU4x_CC4yINTE	E2AE
Status flag	CCU4x_CC4yINTS	E2AS
Set flag	CCU4x_CC4ySWS	SE2A
Clear flag	CCU4x_CC4ySWR	RE2A
Node pointer	CCU4x_CC4ySRS	E2SR

7.4.8.4 Period Match while counting up event

Table 108 CCU4x_SR[3:0] (x=0-1) - Period Match while counting up event

Type	Register	Bits
Interrupt enable	CCU4x_CC4yINTE	PME
Status flag	CCU4x_CC4yINTS	PMUS
Set flag	CCU4x_CC4ySWS	SPM
Clear flag	CCU4x_CC4ySWR	RPM
Node pointer	CCU4x_CC4ySRS	POSR

7.4.8.5 Compare Match while counting up event

Table 109 CCU4x_SR[3:0] (x=0-1) - Compare Match while counting up event

Type	Register	Bits
Interrupt enable	CCU4x_CC4yINTE	CMUE
Status flag	CCU4x_CC4yINTS	CMUS
Set flag	CCU4x_CC4ySWS	SCMU
Clear flag	CCU4x_CC4ySWR	RCMU
Node pointer	CCU4x_CC4ySRS	CMSR

7.4.8.6 Compare Match while counting down event

Table 110 CCU4x_SR[3:0] (x=0-1) - Compare Match while counting down event

Type	Register	Bits
Interrupt enable	CCU4x_CC4yINTE	CMDE
Status flag	CCU4x_CC4yINTS	CMDS
Set flag	CCU4x_CC4ySWS	SCMD
Clear flag	CCU4x_CC4ySWR	RCMD
Node pointer	CCU4x_CC4ySRS	CMSR

7.4.8.7 One Match while counting down event

Table 111 CCU4x_SR[3:0] (x=0-1) - One Match while counting down event

Type	Register	Bits
Interrupt enable	CCU4x_CC4yINTE	OME
Status flag	CCU4x_CC4yINTS	OMDS
Set flag	CCU4x_CC4ySWS	SOM
Clear flag	CCU4x_CC4ySWR	ROM
Node pointer	CCU4x_CC4ySRS	POSR

7.4.8.8 Entering Trap State event

Table 112 CCU4x_SR[3:0] (x=0-1) - Entering Trap State event

Type	Register	Bits
Interrupt enable	CCU4x_CC4yINTE	E2AE
Status flag	CCU4x_CC4yINTS	TRPF
Set flag	CCU4x_CC4ySWS	STRPF
Clear flag	CCU4x_CC4ySWR	RTRPF
Node pointer	CCU4x_CC4ySRS	E2SR

7.4.9 Interrupt source: CCU8x_SR[1:0] (x=0-1)

7.4.9.1 Event 0 edge(s) information from event selector

Table 113 CCU8x_SR[1:0] (x=0-1) - Event 0 edge(s) information from event selector

Type	Register	Bits
Interrupt enable	CCU8x_CC8yINTE	E0AE

Table 113 CCU8x_SR[1:0] (x=0-1) - Event 0 edge(s) information from event selector (continued)

Type	Register	Bits
Status flag	CCU8x_CC8yINTS	E0AS
Set flag	CCU8x_CC8ySWS	SE0A
Clear flag	CCU8x_CC8ySWR	RE0A
Node pointer	CCU8x_CC8ySRS	E0SR

7.4.9.2 Event 1 edge(s) information from event selector

Table 114 CCU8x_SR[1:0] (x=0-1) - Event 1 edge(s) information from event selector

Type	Register	Bits
Interrupt enable	CCU8x_CC8yINTE	E1AE
Status flag	CCU8x_CC8yINTS	E1AS
Set flag	CCU8x_CC8ySWS	SE1A
Clear flag	CCU8x_CC8ySWR	RE1A
Node pointer	CCU8x_CC8ySRS	E1SR

7.4.9.3 Event 2 edge(s) information from event selector

Table 115 CCU8x_SR[1:0] (x=0-1) - Event 2 edge(s) information from event selector

Type	Register	Bits
Interrupt enable	CCU8x_CC8yINTE	E2AE
Status flag	CCU8x_CC8yINTS	E2AS
Set flag	CCU8x_CC8ySWS	SE2A
Clear flag	CCU8x_CC8ySWR	RE2A
Node pointer	CCU8x_CC8ySRS	E2SR

7.4.9.4 Period Match while counting up event

Table 116 CCU8x_SR[1:0] (x=0-1) - Period Match while counting up event

Type	Register	Bits
Interrupt enable	CCU8x_CC8yINTE	PME
Status flag	CCU8x_CC8yINTS	PMUS
Set flag	CCU8x_CC8ySWS	SPM
Clear flag	CCU8x_CC8ySWR	RPM
Node pointer	CCU8x_CC8ySRS	POSR

7.4.9.5 Compare Match while counting up from compare channel 1 event

Table 117 CCU8x_SR[1:0] (x=0-1) - Compare Match while counting up from compare channel 1 event

Type	Register	Bits
Interrupt enable	CCU8x_CC8yINTE	CMU1E
Status flag	CCU8x_CC8yINTS	CMU1S
Set flag	CCU8x_CC8ySWS	SCM1U
Clear flag	CCU8x_CC8ySWR	RCM1U
Node pointer	CCU8x_CC8ySRS	CM1SR

7.4.9.6 Compare Match while counting down from compare channel 1 event

Table 118 CCU8x_SR[1:0] (x=0-1) - Compare Match while counting down from compare channel 1 event

Type	Register	Bits
Interrupt enable	CCU8x_CC8yINTE	CMD1E
Status flag	CCU8x_CC8yINTS	CMD1S
Set flag	CCU8x_CC8ySWS	SCM1D
Clear flag	CCU8x_CC8ySWR	RCM1D
Node pointer	CCU8x_CC8ySRS	CM1SR

7.4.9.7 Compare Match while counting up from compare channel 2 event

Table 119 CCU8x_SR[1:0] (x=0-1) - Compare Match while counting up from compare channel 2 event

Type	Register	Bits
Interrupt enable	CCU8x_CC8yINTE	CMU2E
Status flag	CCU8x_CC8yINTS	CMU2S
Set flag	CCU8x_CC8ySWS	SCM2U
Clear flag	CCU8x_CC8ySWR	RCM2U
Node pointer	CCU8x_CC8ySRS	CM2SR

7.4.9.8 Compare Match while counting down from compare channel 2 event

Table 120 CCU8x_SR[1:0] (x=0-1) - Compare Match while counting down from compare channel 2 event

Type	Register	Bits
Interrupt enable	CCU8x_CC8yINTE	CMD2E
Status flag	CCU8x_CC8yINTS	CMD2S
Set flag	CCU8x_CC8ySWS	SCM2D
Clear flag	CCU8x_CC8ySWR	RCM2D
Node pointer	CCU8x_CC8ySRS	CM2SR

7.4.9.9 One Match while counting down event

Table 121 CCU8x_SR[1:0] (x=0-1) - One Match while counting down event

Type	Register	Bits
Interrupt enable	CCU8x_CC8yINTE	OME
Status flag	CCU8x_CC8yINTS	OMDS
Set flag	CCU8x_CC8ySWS	SOM
Clear flag	CCU8x_CC8ySWR	ROM
Node pointer	CCU8x_CC8ySRS	POSR

7.4.9.10 Entering Trap State event

Table 122 CCU8x_SR[1:0] (x=0-1) - Entering Trap State event

Type	Register	Bits
Interrupt enable	CCU8x_CC8yINTE	E2AE
Status flag	CCU8x_CC8yINTS	TRPF
Set flag	CCU8x_CC8ySWS	STRPF
Clear flag	CCU8x_CC8ySWR	RTRPF
Node pointer	CCU8x_CC8ySRS	E2SR

7.4.10 Interrupt source: POSIFx.SR[1:0] (x=0-1)

7.4.10.1 Transition at Hall inputs events

Table 123 POSIFx.SR[1:0] (x=0-1) - Transition at Hall inputs events

Type	Register	Bits
Interrupt enable	POSIFx_PFLGE	EHIE

Table 123 POSIFx.SR[1:0] (x=0-1) - Transition at Hall inputs events (continued)

Type	Register	Bits
Status flag	POSIFx_PFLG	HIES
Set flag	POSIFx_SPFLG	SHIE
Clear flag	POSIFx_RPFLG	RHIE
Node pointer	POSIFx_PFLGE	HIESEL

7.4.10.2 Occurrence of correct Hall event

Table 124 POSIFx.SR[1:0] (x=0-1) - Occurrence of correct Hall event

Type	Register	Bits
Interrupt enable	POSIFx_PFLGE	ECHE
Status flag	POSIFx_PFLG	CHES
Set flag	POSIFx_SPFLG	SCHE
Clear flag	POSIFx_RPFLG	RCHE
Node pointer	POSIFx_PFLGE	CHESEL

7.4.10.3 Occurrence of wrong Hall event

Table 125 POSIFx.SR[1:0] (x=0-1) - Occurrence of wrong Hall event

Type	Register	Bits
Interrupt enable	POSIFx_PFLGE	EWHE
Status flag	POSIFx_PFLG	WHES
Set flag	POSIFx_SPFLG	SWHE
Clear flag	POSIFx_RPFLG	RWHE
Node pointer	POSIFx_PFLGE	WHESEL

7.4.10.4 Shadow transfer of MCM pattern event

Table 126 POSIFx.SR[1:0] (x=0-1) - Shadow transfer of MCM pattern event

Type	Register	Bits
Interrupt enable	POSIFx_PFLGE	EMST
Status flag	POSIFx_PFLG	MSTS
Set flag	POSIFx_SPFLG	SMST
Clear flag	POSIFx_RPFLG	RMST
Node pointer	POSIFx_PFLGE	MSTSEL

7.4.10.5 Index event detection event

Table 127 POSIFx.SR[1:0] (x=0-1) - Index event detection event

Type	Register	Bits
Interrupt enable	POSIFx_PFLGE	EINDX
Status flag	POSIFx_PFLG	INDXS
Set flag	POSIFx_SPFLG	SINDX
Clear flag	POSIFx_RPFLG	RINDX
Node pointer	POSIFx_PFLGE	INDSEL

7.4.10.6 Phase detection error event

Table 128 POSIFx.SR[1:0] (x=0-1) - Phase detection error event

Type	Register	Bits
Interrupt enable	POSIFx_PFLGE	EERR
Status flag	POSIFx_PFLG	ERRS
Set flag	POSIFx_SPFLG	SERR
Clear flag	POSIFx_RPFLG	RERR
Node pointer	POSIFx_PFLGE	ERRSEL

7.4.10.7 Quadrature clock generation event

Table 129 POSIFx.SR[1:0] (x=0-1) - Quadrature clock generation event

Type	Register	Bits
Interrupt enable	POSIFx_PFLGE	ECNT
Status flag	POSIFx_PFLG	CNTS
Set flag	POSIFx_SPFLG	SCNT
Clear flag	POSIFx_RPFLG	RCNT
Node pointer	POSIFx_PFLGE	CNTSEL

7.4.10.8 Period clock generation event

Table 130 POSIFx.SR[1:0] (x=0-1) - Period clock generation event

Type	Register	Bits
Interrupt enable	POSIFx_PFLGE	EPCLK
Status flag	POSIFx_PFLG	PCLKS
Set flag	POSIFx_SPFLG	SPCLK

Table 130 POSIFx.SR[1:0] (x=0-1) - Period clock generation event (continued)

Type	Register	Bits
Clear flag	POSIFx_RPFLG	RPCLK
Node pointer	POSIFx_PFLGE	PCLSEL

7.4.10.9 Direction change event

Table 131 POSIFx.SR[1:0] (x=0-1) - Direction change event

Type	Register	Bits
Interrupt enable	POSIFx_PFLGE	EDIR
Status flag	POSIFx_PFLG	DIRS
Set flag	POSIFx_SPFLG	SDIR
Clear flag	POSIFx_RPFLG	RDIR
Node pointer	POSIFx_PFLGE	DIRSEL

7.4.11 Interrupt source: CAN0.SR[3:0]

7.4.11.1 Message Transmitted event

Table 132 CAN0.SR[3:0] - Message Transmitted event

Type	Register	Bits
Interrupt enable	CAN0_NCRx	TRIE
Status flag	CAN0_NSRx	TXOK
Set flag	-	-
Clear flag	-	-
Node pointer	CAN0_NIPRx	TRINP

7.4.11.2 Message Received event

Table 133 CAN0.SR[3:0] - Message Received event

Type	Register	Bits
Interrupt enable	CAN0_NCRx	TRIE
Status flag	CAN0_NSRx	RXOK
Set flag	-	-
Clear flag	-	-
Node pointer	CAN0_NIPRx	TRINP

7.4.11.3 Last Error Code event

Table 134 CAN0.SR[3:0] - Last Error Code event

Type	Register	Bits
Interrupt enable	CAN0_NCRx	LECIE
Status flag	CAN0_NSRx	LEC
Set flag	-	-
Clear flag	-	-
Node pointer	CAN0_NIPRx	LECINP

7.4.11.4 Fast Last Error Code event

Table 135 CAN0.SR[3:0] - Fast Last Error Code event

Type	Register	Bits
Interrupt enable	CAN0_NCRx	LECIE
Status flag	CAN0_NSRx	FLEC
Set flag	-	-
Clear flag	-	-
Node pointer	CAN0_NIPRx	LECINP

7.4.11.5 Alert Warning event

Table 136 CAN0.SR[3:0] - Alert Warning event

Type	Register	Bits
Interrupt enable	CAN0_NCRx	ALIE
Status flag	CAN0_NSRx	ALERT
Set flag	-	-
Clear flag	-	-
Node pointer	CAN0_NIPRx	ALINP

7.4.11.6 Receive Pending event

Table 137 CAN0.SR[3:0] - Receive Pending event

Type	Register	Bits
Interrupt enable	CAN0_MOFCRn	RXIE
Status flag	CAN0_MOSTATn	RXPND
Set flag	-	-

Table 137 CAN0.SR[3:0] - Receive Pending event (continued)

Type	Register	Bits
Clear flag	CAN0_MOCTRn	RESRXPND
Node pointer	CAN0_MOIPRn	RXINP

7.4.11.7 Transmit Pending event

Table 138 CAN0.SR[3:0] - Transmit Pending event

Type	Register	Bits
Interrupt enable	CAN0_MOFCRn	TXIE
Status flag	CAN0_MOSTATn	TXPND
Set flag	-	-
Clear flag	CAN0_MOCTRn	RESTXPND
Node pointer	CAN0_MOIPRn	TXINP

7.4.11.8 FIFO Full event

Table 139 CAN0.SR[3:0] - FIFO Full event

Type	Register	Bits
Interrupt enable	CAN0_MOFCRn	OVIE
Status flag	-	-
Set flag	-	-
Clear flag	-	-
Node pointer	CAN0_MOIPRn	TXINP/RXINP

8 Event Request Unit (ERU)

As described in the Service Request Processing chapter, IMC300A uses the Event Request Unit (ERU) to support the programmable interconnection for the processing of service requests. There are 2 instances of ERU in IMC300A, ERU0 and ERU1.

8.1 Features

The ERU supports these features:

- Flexible processing of external and internal service requests
- Programmable for edge and/or level triggering
- Multiple inputs per channel
- Triggers combinable from multiple inputs
- Input and output gating

8.2 Overview

The Event Request Unit (ERU) is a versatile multiple input event detection and processing unit.

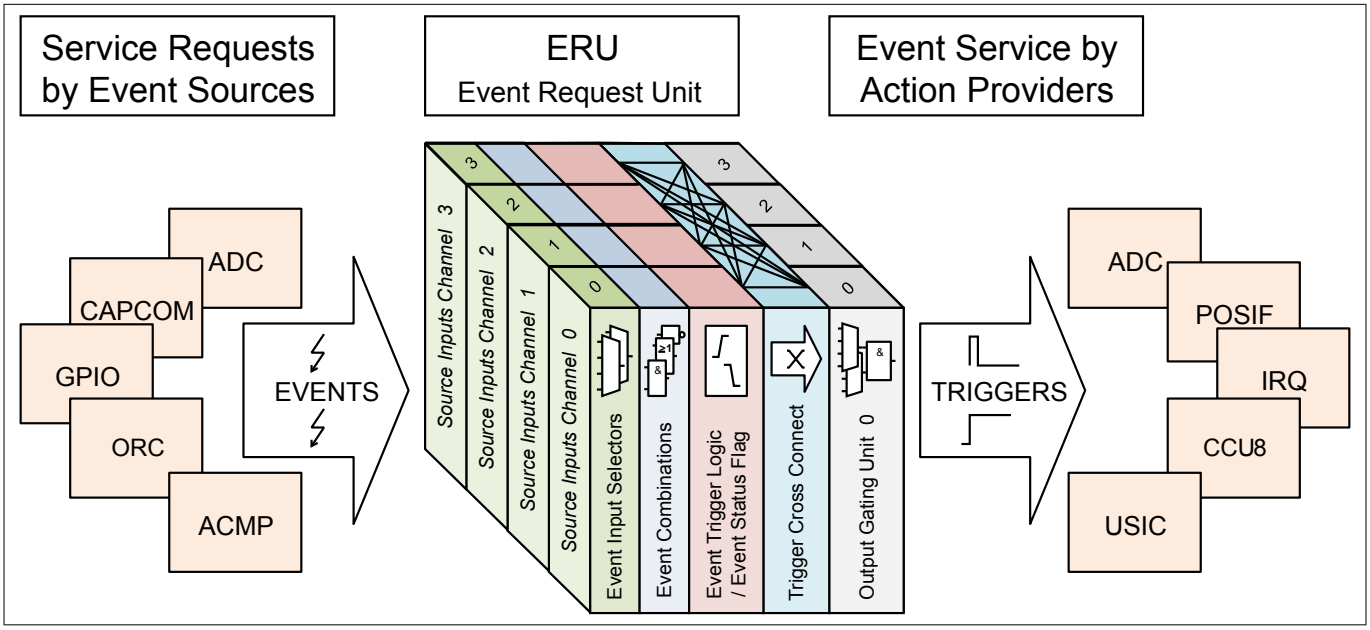


Figure 22 Event Request Unit Overview

Each ERU unit consists of the following blocks:

- An **Event Request Select (ERS)** unit.
  - Event Input Selectors allow the selection of one out of two inputs. For each of these two inputs, an vector of 4 possible signals is available.
  - Event Combinations allow a logical combination of two input signals to a common trigger.
- An **Event Trigger Logic (ETL)** per Input Channel allows the definition of the transition (edge selection, or by software) that lead to a trigger event and can also store this status. Here, the input levels of the selected signals are translated into events.

- The Trigger **Cross Connect Matrix** distributes the events and status flags to the Output Channels. Additionally, trigger signals from other modules are made available and can be combined with the local triggers.
- An **Output Gating Unit (OGU)** combines the trigger events and status information and gates the Output depending on a gating signal.

Note: An event of one Input can lead to reactions on several Outputs, or also events on several Inputs can be combined to a reaction on one Output.

8.3 Event Request Select Unit (ERS)

For each Input Channel x (x = 0-3), an ERSx unit handles the input selection for the associated ETLx unit. Each ERSx performs a logical combination of two signals (Ax, Bx) to provide one combined output signal ERSxO to the associated ETLx. Input Ax can be selected from 4 options of the input vector ERU_xA[3:0] and can be optionally inverted. A similar structure exists for input Bx (selection from ERU_xB[3:0]).

In addition to the direct choice of either input Ax or Bx or their inverted values, the possible logical combinations for two selected inputs are a logical AND or a logical OR.

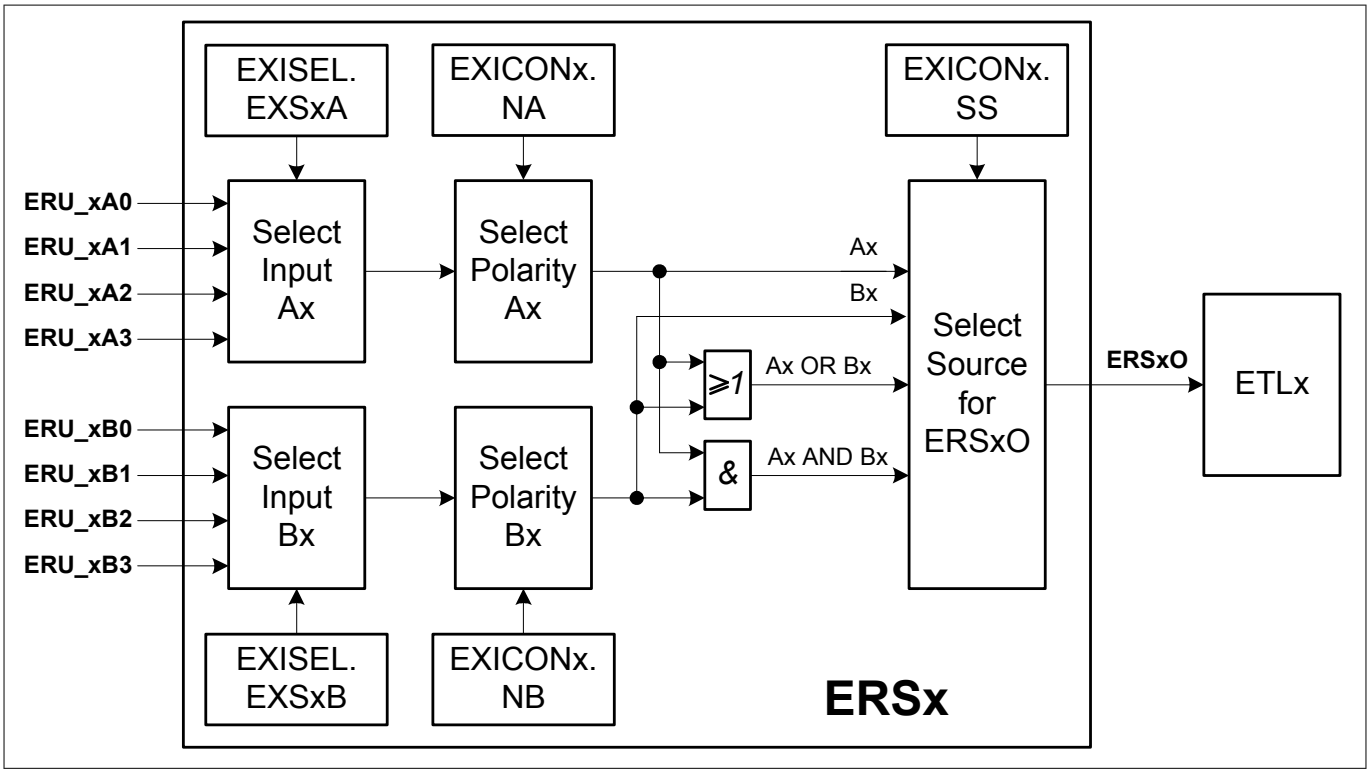


Figure 23 Event Request Select Unit Overview

The ERS units are controlled via register ***EXISEL*** (one register for all four ERSx units) and registers EXICONx (one register for each ERSx and associated ETLx unit, e.g. ***EXICONx (x=0-3)*** for Input Channel 0).

8.4 Event Trigger Logic (ETLx)

For each Input Channel x (x = 0-3), an event trigger logic ETLx derives a trigger event and related status information from the input ERSxO. Each ETLx is based on an edge detection block, where the detection of a rising or a falling edge can be individually enabled. Both edges lead to a trigger event if both enable bits are set (e.g. to handle a toggling input).

Each of the four ETLx units has an associated EXICONx register, that controls all options of an ETLx (the register also holds control bits for the associated ERSx unit, e.g. ***EXICONx (x=0-3)*** to control ERS0 and ETL0).

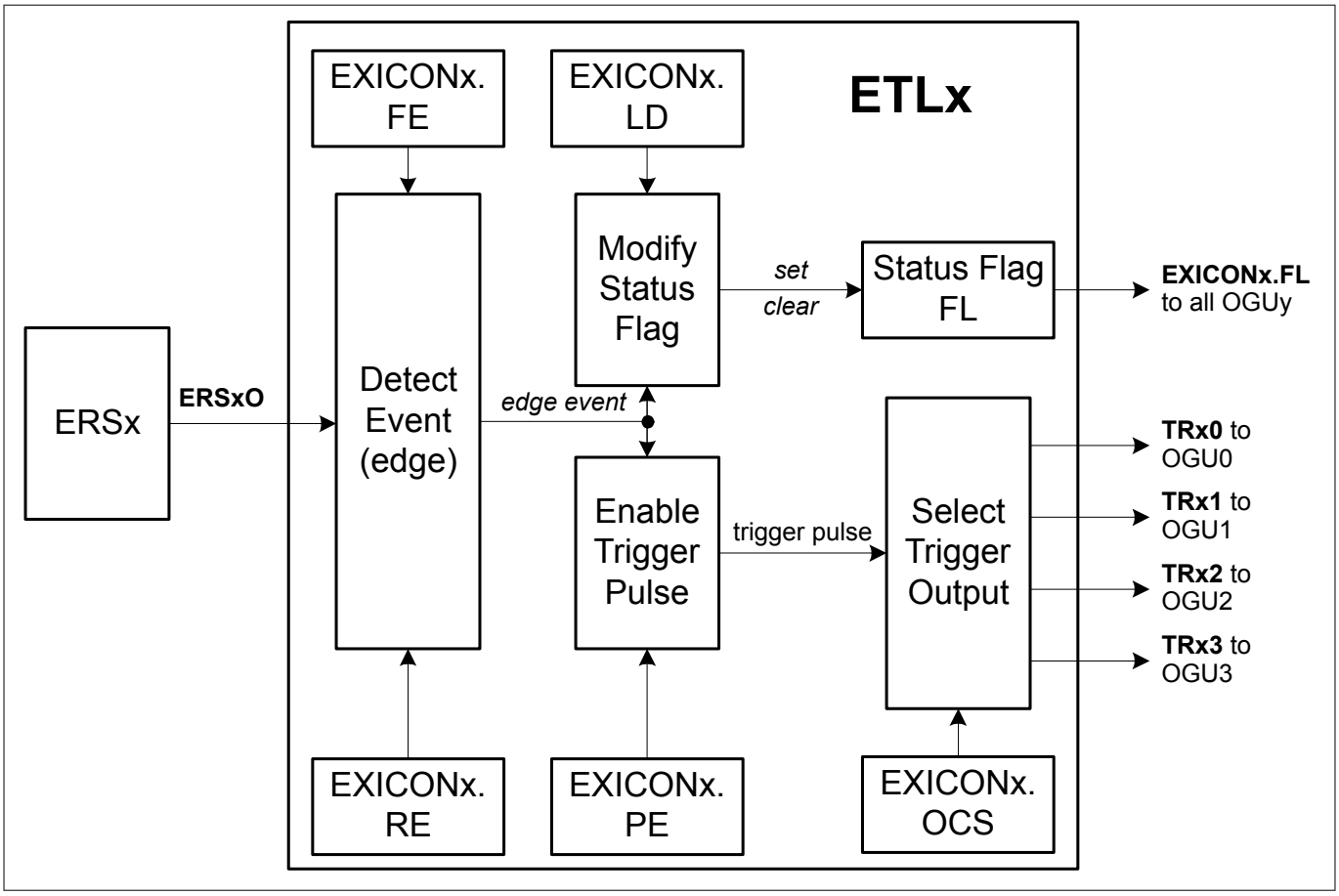


Figure 24 Event Trigger Logic Overview

When the selected event (edge) is detected, the status flag EXICONx.FL becomes set. This flag can also be modified by software. Two different operating modes are supported by this status flag.

It can be used as “sticky” flag, which is set by hardware when the desired event has been detected and has to be cleared by software. In this operating mode, it indicates that the event has taken place, but without indicating the actual status of the input.

In the second operating mode, it is cleared automatically if the “opposite” event is detected. For example, if only the falling edge detection is enabled to set the status flag, it is cleared when the rising edge is detected. In this mode, it can be used for pattern detection where the actual status of the input is important (enabling both edge detections is not useful in this mode).

The output of the status flag is connected to all following Output Gating Units (OGUy) in parallel (see ***Figure 25***) to provide **pattern detection capability of all OGUy** units based on different or the same status flags.

In addition to the modification of the status flag, a trigger pulse output TRxy of ETLx can be enabled (by bit EXICONx.PE) and selected to **trigger actions in one of the OGUy** units. The target OGUy for the trigger is selected by bit field EXICON.OCS.

The trigger becomes active when the selected edge event is detected, independently from the status flag EXICONx.FL.

8.5 Cross Connect Matrix

The matrix shown in ***Figure 25*** distributes the trigger signals (TRxy) and status signals (EXICONx.FL) from the different ETLx units between the OGUy units. In addition, it receives peripheral trigger signals that can be OR-combined with the ETLx trigger signals in the OGUy units.

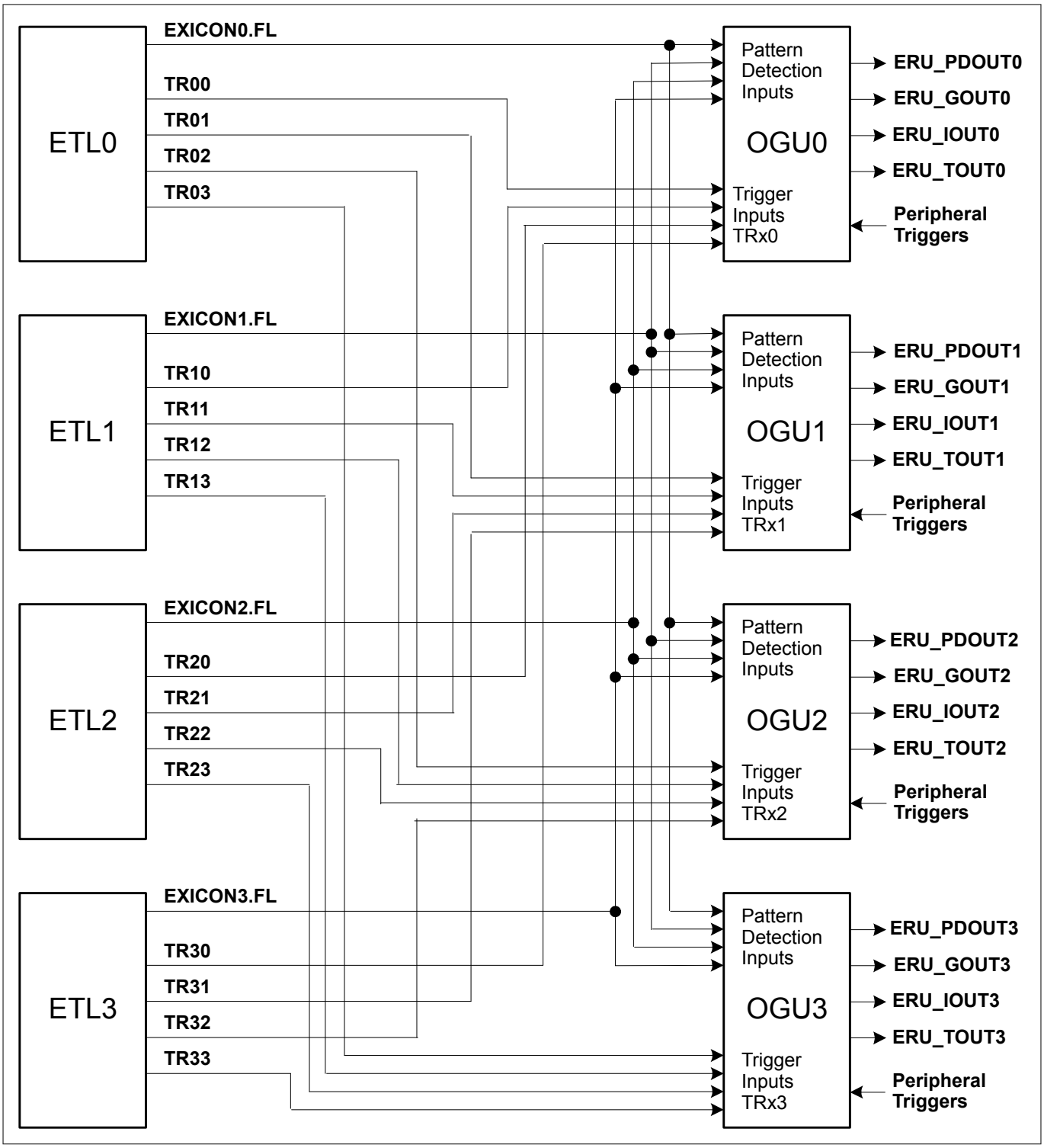


Figure 25 ERU Cross Connect Matrix

8.6 Output Gating Unit (OGUy)

Each OGUy (y = 0-3) unit combines the available trigger events and status flags from the Input Channels and distributes the results to the system. ***Figure 26*** illustrates the logic blocks within an OGUy unit. All functions of an OGUy unit are controlled by its associated EXOCONy register, e.g. ***EXOCONx (x=0-3)*** for OGU0. The function of an OGUy unit can be split into two parts:

Trigger Combination

All trigger signals TRxy from the Input Channels that are enabled and directed to OGUy, a selected peripheral-related trigger event, and a pattern change event (if enabled) are logically OR-combined.

Pattern Detection

The status flags EXICONx.FL of the Input Channels can be enabled to take part in the pattern detection. A pattern match is detected while all enabled status flags are set.

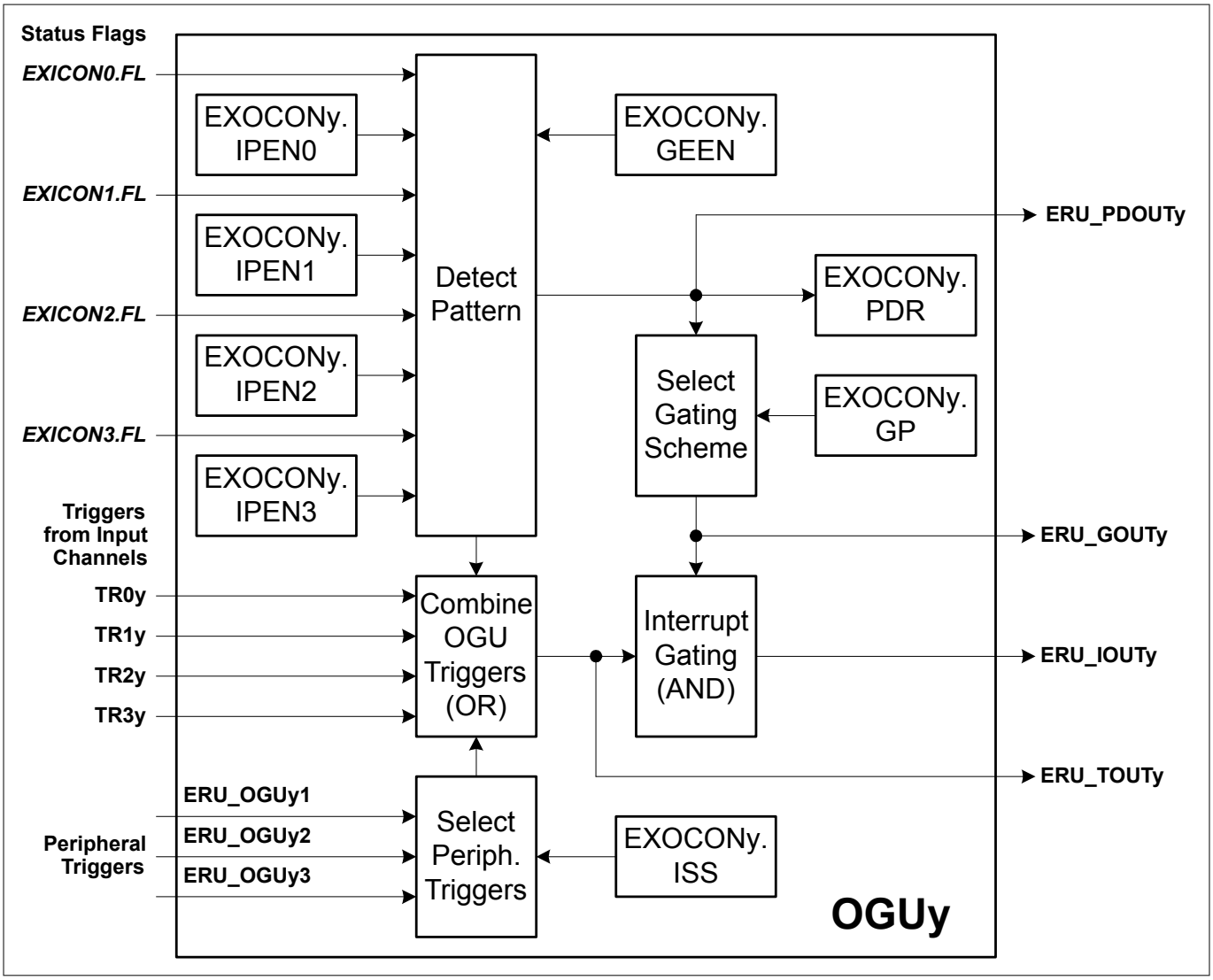


Figure 26 Output Gating Unit for Output Channel y

Each OGUy unit generates 4 output signals that are distributed to the system (not all of them are necessarily used):

- **ERU_PDOUTy** to directly output the pattern match information for gating purposes in other modules (pattern match = 1).

- **ERU_GOUTy** to output the pattern match or pattern miss information (inverted pattern match), or a permanent 0 or 1 under software control for gating purposes in other modules.
- **ERU_TOUTy** as combination of a peripheral trigger, a pattern detection result change event, or the ETLx trigger outputs TRxy to trigger actions in other modules.
- **ERU_IOUTy** as gated trigger output (ERU_GOUTy logical AND-combined with ERU_TOUTy) to trigger service requests (e.g. the service request generation can be gated to allow service request activation during a certain time window).

Trigger Combination

The trigger combination logically OR-combines different trigger inputs to form a common trigger ERU_TOUTy. Possible trigger inputs are:

- In each ETLx unit of the **Input Channels**, the trigger output TRxy can be enabled and the trigger event can be directed to one of the OGUy units.
- One out of three **peripheral trigger** signals per OGUy can be selected as additional trigger source. These peripheral triggers are generated by on-chip peripheral modules, such as capture/compare or timer units. The selection is done by bit field EXOCONy.ISS.
- In the case that at least one **pattern detection** input is enabled (EXOCONy.IPENx) and a change of the pattern detection result from pattern match to pattern miss (or vice-versa) is detected, a trigger event is generated to indicate a pattern detection result event (if enabled by ECOCONy.GEEN).

The trigger combination offers the possibility to program different trigger criteria for several input signals (independently for each Input Channel) or peripheral signals, and to combine their effects to a single output, e.g. to generate an service request or to start an ADC conversion. This combination capability allows the generation of a service request per OGU that can be triggered by several inputs (multitude of request sources results in one reaction).

The selection is defined by the bit fields ISS in registers ***EXOCONx (x=0-3)***.

Pattern Detection

The pattern detection logic allows the combination of the status flags of all ETLx units. Each status flag can be individually included or excluded from the pattern detection for each OGUy, via control bits EXOCONy.IPENx. The pattern detection block outputs the following pattern detection results:

- **Pattern match** (EXOCONy.PDR = 1 and ERU_PDOUTy = 1):

  A pattern match is indicated while all status flags FL that are included in the pattern detection are 1.
- **Pattern miss** (EXOCONy.PDR = 0 and ERU_PDOUTy = 0):

  A pattern miss is indicated while at least one of the status flags FL that are included in the pattern detection is 0.

In addition, the pattern detection can deliver a trigger event if the pattern detection result changes from match to miss or vice-versa (if enabled by EXOCONy.GEEN = 1). The pattern result change event is logically OR-combined with the other enabled trigger events to support service request generation or to trigger other module functions (e.g. in the ADC). The event is indicated when the pattern detection result changes and EXOCONy.PDR becomes updated.

The service request generation in the OGUy is based on the trigger ERU_TOUTy that can be gated (masked) with the pattern detection result ERU_PDOUTy. This allows an automatic and reproducible generation of service requests during a certain time window, where the request event is elaborated by the trigger combination block and the time window information (gating) is given by the pattern detection. For example, service requests can be issued on a regular time base (peripheral trigger input from capture/compare unit is selected) while a combination of input signals occurs (pattern detection based on ETLx status bits).

A programmable gating scheme introduces flexibility to adapt to application requirements and allows the generation of service requests ERU_IOUTy under different conditions:

- **Pattern match** (EXOCONy.GP = 10_B):

  A service request is issued when a trigger event occurs while the pattern detection shows a pattern match.
- **Pattern miss** (EXOCONy.GP = 11_B):

A service request is issued when the trigger event occurs while the pattern detection shows a pattern miss.

- **Independent** of pattern detection (EXOCONy.GP = 01_B):
  In this mode, each occurring trigger event leads to a service request. The pattern detection output can be used independently from the trigger combination for gating purposes of other peripherals (independent use of ERU_TOUTy and ERU_PDOUTy with service requests on trigger events).
- **No service requests** (EXOCONy.GP = 00_B, default setting):
  In this mode, an occurring trigger event does not lead to a service request. The pattern detection output can be used independently from the trigger combination for gating purposes of other peripherals (independent use of ERU_TOUTy and ERU_PDOUTy without service requests on trigger events).

8.7 Power, Reset and Clock

ERU is running on the main clock, MCLK. It is consuming power in all operating modes as long as the MCLK continues to run.

8.8 Initialization and System Dependencies

Service Requests must always be enabled at the source and at the destination. Additionally it must be checked whether it is necessary to program the ERUx process and route a request.

Enabling Peripheral SRx Outputs

- Peripherals' SRx outputs must be selectively enabled. This procedure depends on the individual peripheral. Please look up the section "Service Request Generation" within a peripheral chapter for details.
- Optionally ERUx must be programmed to process and route the request

Enabling External Requests

- Selected PORTS must be programmed for input
- ERUx must be programmed to process and route the external request

Note: The number of external service request inputs may be limited by the package used.

8.9 Registers

Table 140 Registers Address Space

Module	Base Address	End Address	Note
ERU0	$4001\ 0600_H$	$4001\ 062F_H$	
ERU1	$4001\ 0630_H$	$4001\ 06FF_H$	

Registers Overview

The absolute register address is calculated by adding:
Module Base Address + Offset Address

Table 141 Register Overview

Short Name	Description	Offset Address	Access Mode		Description see
			Read	Write	
EXISEL	ERU External Input Control Selection	0000_H	U, PV	U, PV	Page 173

Table 141 Register Overview (continued)

Short Name	Description	Offset Address	Access Mode		Description see
			Read	Write	
EXICON0	ERU External Input Control Selection	0010_H	U, PV	U, PV	Page 174
EXICON1	ERU External Input Control Selection	0014_H	U, PV	U, PV	Page 174
EXICON2	ERU External Input Control Selection	0018_H	U, PV	U, PV	Page 174
EXICON3	ERU External Input Control Selection	$001C_H$	U, PV	U, PV	Page 174
EXOCON0	ERU Output Control Register	0020_H	U, PV	U, PV	Page 176
EXOCON1	ERU Output Control Register	0024_H	U, PV	U, PV	Page 176
EXOCON2	ERU Output Control Register	0028_H	U, PV	U, PV	Page 176
EXOCON3	ERU Output Control Register	$002C_H$	U, PV	U, PV	Page 176

8.9.1 ERU Registers

8.9.1.1 Register EXISEL

EXISEL Address: 00_H

Event Input Select Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXS3B		EXS3A		EXS2B		EXS2A		EXS1B		EXS1A		EXS0B		EXS0A	
rw		rw		rw		rw		rw		rw		rw		rw	

Field	Bits	Type	Description
EXS0A	1:0	rw	**Event Source Select for A0 (ERS0)** This bit field defines which input is selected for A0. 00_B Input ERU_0A0 is selected 01_B Input ERU_0A1 is selected 10_B Input ERU_0A2 is selected 11_B Input ERU_0A3 is selected
EXS0B	3:2	rw	**Event Source Select for B0 (ERS0)** This bit field defines which input is selected for B0. 00_B Input ERU_0B0 is selected 01_B Input ERU_0B1 is selected 10_B Input ERU_0B2 is selected 11_B Input ERU_0B3 is selected

(continued)

Field	Bits	Type	Description
EXS1A	5:4	rw	**Event Source Select for A1 (ERS1)** This bit field defines which input is selected for A1. 00_B Input ERU_1A0 is selected 01_B Input ERU_1A1 is selected 10_B Input ERU_1A2 is selected 11_B Input ERU_1A3 is selected
EXS1B	7:6	rw	**Event Source Select for B1 (ERS1)** This bit field defines which input is selected for B1. 00_B Input ERU_1B0 is selected 01_B Input ERU_1B1 is selected 10_B Input ERU_1B2 is selected 11_B Input ERU_1B3 is selected
EXS2A	9:8	rw	**Event Source Select for A2 (ERS2)** This bit field defines which input is selected for A2. 00_B Input ERU_2A0 is selected 01_B Input ERU_2A1 is selected 10_B Input ERU_2A2 is selected 11_B Input ERU_2A3 is selected
EXS2B	11:10	rw	**Event Source Select for B2 (ERS2)** This bit field defines which input is selected for B2. 00_B Input ERU_2B0 is selected 01_B Input ERU_2B1 is selected 10_B Input ERU_2B2 is selected 11_B Input ERU_2B3 is selected
EXS3A	13:12	rw	**Event Source Select for A3 (ERS3)** This bit field defines which input is selected for A3. 00_B Input ERU_3A0 is selected 01_B Input ERU_3A1 is selected 10_B Input ERU_3A2 is selected 11_B Input ERU_3A3 is selected
EXS3B	15:14	rw	**Event Source Select for B3 (ERS3)** This bit field defines which input is selected for B3. 00_B Input ERU_3B0 is selected 01_B Input ERU_3B1 is selected 10_B Input ERU_3B2 is selected 11_B Input ERU_3B3 is selected
0	31:16	r	**Reserved** Read as 0; should be written with 0.

8.9.1.2 Register EXICONx

EXICONx (x=0-3) Address: $10_H + 4*x$

Event Input Control x Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				**NB**	**NA**	**SS**		**FL**	**OCS**			**FE**	**RE**	**LD**	**PE**
r				rw	rw	rw		rwh	rw			rw	rw	rw	rw

Field	Bits	Type	Description
PE	0	rw	**Output Trigger Pulse Enable for ETLx** This bit enables the generation of an output trigger pulse at TRxy when the selected edge is detected (set condition for the status flag FL). 0_B The trigger pulse generation is disabled 1_B The trigger pulse generation is enabled
LD	1	rw	**Rebuild Level Detection for Status Flag for ETLx** This bit selects if the status flag FL is used as “sticky” bit or if it rebuilds the result of a level detection. 0_B The status flag FL is not cleared by hardware and is used as “sticky” bit. Once set, it is not influenced by any edge until it becomes cleared by software. 1_B The status flag FL rebuilds a level detection of the desired event. It becomes automatically set with a rising edge if RE = 1 or with a falling edge if FE = 1. It becomes automatically cleared with a rising edge if RE = 0 or with a falling edge if FE = 0.
RE	2	rw	**Rising Edge Detection Enable ETLx** This bit enables/disables the rising edge event as edge event as set condition for the status flag FL or as possible trigger pulse for TRxy. 0_B A rising edge is not considered as edge event 1_B A rising edge is considered as edge event
FE	3	rw	**Falling Edge Detection Enable ETLx** This bit enables/disables the falling edge event as edge event as set condition for the status flag FL or as possible trigger pulse for TRxy. 0_B A falling edge is not considered as edge event 1_B A falling edge is considered as edge event

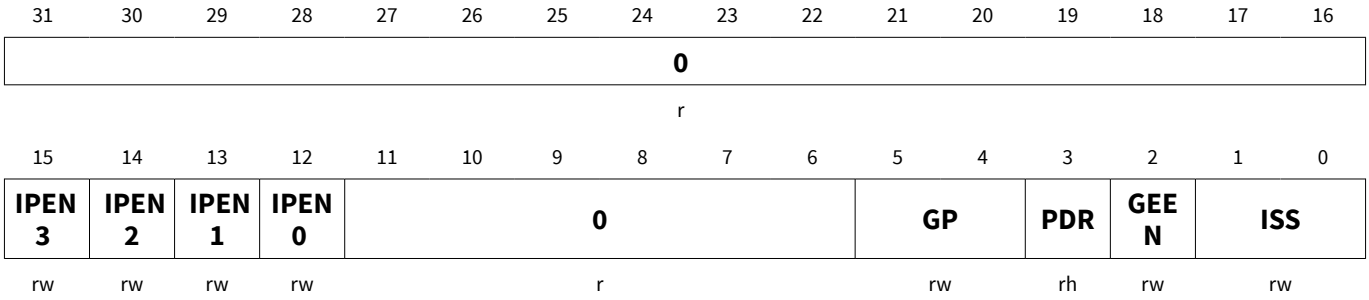
(continued)

Field	Bits	Type	Description
OCS	6:4	rw	**Output Channel Select for ETLx Output Trigger Pulse** This bit field defines which Output Channel OGUy is targeted by an enabled trigger pulse TRxy. 000_B Trigger pulses are sent to OGU0 001_B Trigger pulses are sent to OGU1 010_B Trigger pulses are sent to OGU2 011_B Trigger pulses are sent to OGU3 Others: Reserved, do not use this combination
FL	7	rwh	**Status Flag for ETLx** This bit represents the status flag that becomes set or cleared by the edge detection. 0_B The enabled edge event has not been detected 1_B The enabled edge event has been detected
SS	9:8	rw	**Input Source Select for ERSx** This bit field defines which logical combination is taken into account as ERSxO. 00_B Input A without additional combination 01_B Input B without additional combination 10_B Input A OR input B 11_B Input A AND input B
NA	10	rw	**Input A Negation Select for ERSx** This bit selects the polarity for the input A. 0_B Input A is used directly 1_B Input A is inverted
NB	11	rw	**Input B Negation Select for ERSx** This bit selects the polarity for the input B. 0_B Input B is used directly 1_B Input B is inverted
0	31:12	r	**Reserved** Read as 0; should be written with 0.

8.9.1.3 Register EXOCONx

EXOCONx (x=0-3) Address: $20_H + 4*x$

Event Output Trigger Control x Reset Value: $0000\ 0008_H$



Field	Bits	Type	Description
ISS	1:0	rw	**Internal Trigger Source Selection** This bit field defines which input is selected as peripheral trigger input for OGUy. 00_B The peripheral trigger function is disabled 01_B Input ERU_OGUy1 is selected 10_B Input ERU_OGUy2 is selected 11_B Input ERU_OGUy3 is selected
GEEN	2	rw	**Gating Event Enable** Bit GEEN enables the generation of a trigger event when the result of the pattern detection changes from match to miss or vice-versa. 0_B The event detection is disabled 1_B The event detection is enabled
PDR	3	rh	**Pattern Detection Result Flag** This bit represents the pattern detection result. 0_B A pattern miss is detected 1_B A pattern match is detected
GP	5:4	rw	**Gating Selection for Pattern Detection Result** This bit field defines the gating scheme for the service request generation (relation between the OGU output ERU_PDOUTy and ERU_GOUTy). 00_B ERU_GOUTy is always disabled and ERU_IOUTy can not be activated 01_B ERU_GOUTy is always enabled and ERU_IOUTy becomes activated with each activation of ERU_TOUTy 10_B ERU_GOUTy is equal to ERU_PDOUTy and ERU_IOUTy becomes activated with an activation of ERU_TOUTy while the desired pattern is detected (pattern match PDR = 1) 11_B ERU_GOUTy is inverted to ERU_PDOUTy and ERU_IOUTy becomes activated with an activation of ERU_TOUTy while the desired pattern is not detected (pattern miss PDR = 0)
IPENx (x=0-3)	12+x	rw	**Pattern Detection Enable for ETLx** Bit IPENx defines whether the trigger event status flag EXICONx.FL of ETLx takes part in the pattern detection of OGUy. 0_B Flag EXICONx.FL is excluded from the pattern detection 1_B Flag EXICONx.FL is included in the pattern detection

(continued)

Field	Bits	Type	Description
0	31:16, 11:6	r	**Reserved** Read as 0; should be written with 0.

8.10 Interconnects

This section describes how the ERU0 and ERU1 module is connected within the IMC300A system.

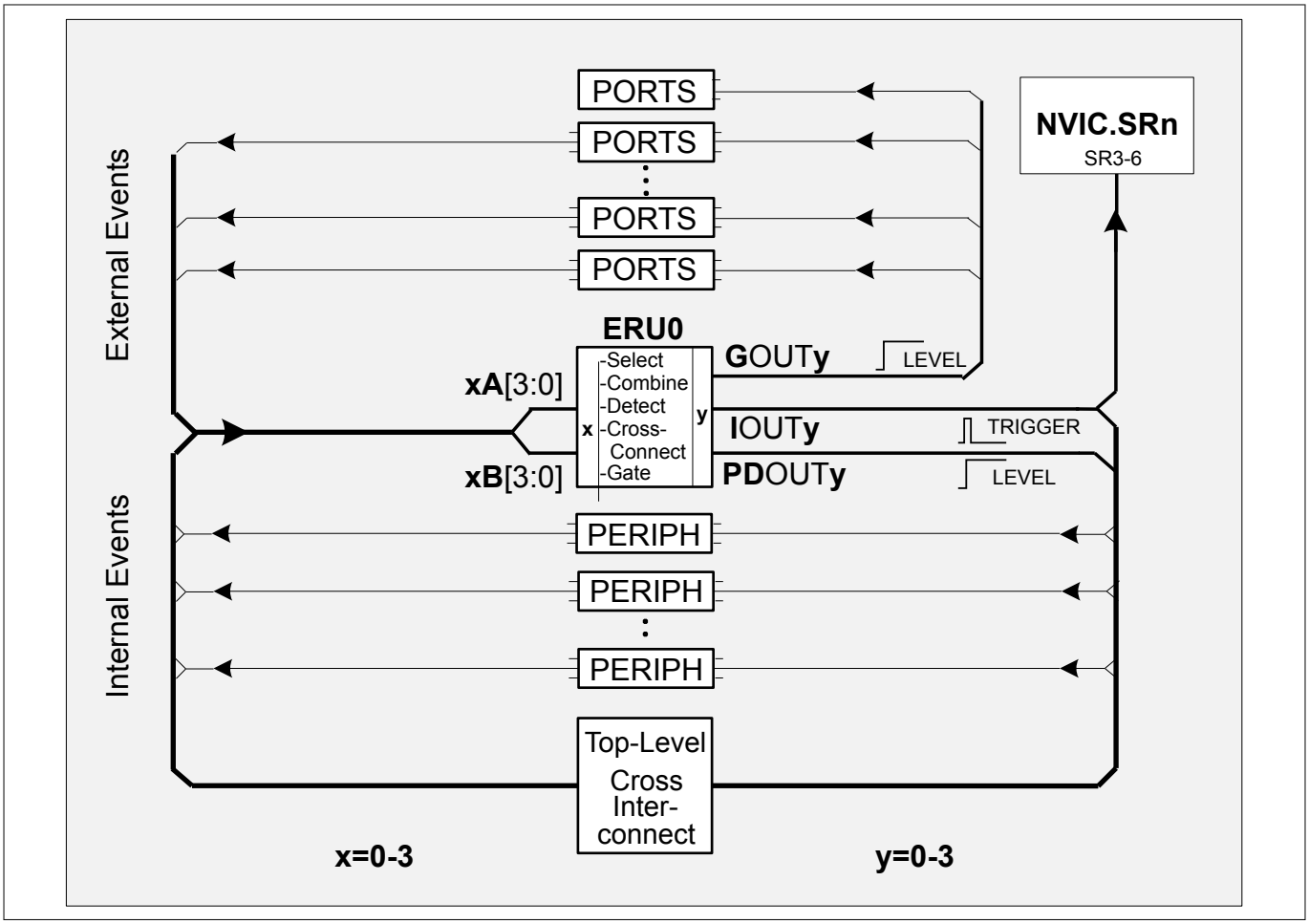


Figure 27 ERU Interconnects Overview

8.10.1 ERU0 Connections

The following table shows the ERU0 connections.

Table 142 ERU0 Pin Connections

Global Input/Output	I/O	Connected To	Description
ERU0.0A0	I	ACMP0.OUT	
ERU0.0A1	I		
ERU0.0A2	I		
ERU0.0A3	I		

Table 142 ERU0 Pin Connections (continued)

Global Input/Output	I/O	Connected To	Description
ERU0.0B0	I	P2.0	
ERU0.0B1	I	P2.2	
ERU0.0B2	I	ORC0.OUT	
ERU0.0B3	I		
ERU0.1A0	I	ACMP1.OUT	
ERU0.1A1	I		
ERU0.1A2	I		
ERU0.1A3	I		
ERU0.1B0	I	P2.1	
ERU0.1B1	I		
ERU0.1B2	I		
ERU0.1B3	I		
ERU0.2A0	I	ACMP2.OUT	
ERU0.2A1	I	P2.6	
ERU0.2A2	I	ORC4.OUT	
ERU0.2A3	I		
ERU0.2B0	I	P2.10	
ERU0.2B1	I	P2.11	
ERU0.2B2	I		
ERU0.2B3	I		
ERU0.3A0	I		
ERU0.3A1	I		
ERU0.3A2	I		
ERU0.3A3	I		
ERU0.3B0	I		
ERU0.3B1	I	P2.8	
ERU0.3B2	I	ORC6.OUT	
ERU0.3B3	I		
ERU0.OGU01	I	CCU40.SR0	
ERU0.OGU02	I		
ERU0.OGU03	I		
ERU0.OGU11	I	CCU40.SR1	
ERU0.OGU12	I	VADC0.C0SR2	
ERU0.OGU13	I		

Table 142 ERU0 Pin Connections (continued)

Global Input/Output	I/O	Connected To	Description
ERU0.OGU21	I	CCU40.SR2	
ERU0.OGU22	I		
ERU0.OGU23	I		
ERU0.OGU31	I	CCU40.SR3	
ERU0.OGU32	I		
ERU0.OGU33	I		
ERU0.PDOUT0	O	CCU40.IN0AJ; CCU40.IN1AD; CCU41.IN0AJ; CCU41.IN1AD; USIC0_CH1.HWIN0; P2.11;	
ERU0.GOUT0	O	P2.11;	
ERU0.TOUT0	O	not connected	
ERU0.IOUT0	O	NVIC; SCU.RTC_extclkin; CCU40.CLKB; CCU40.IN0AK; CCU41.CLKA; CCU41.IN0AK;	
ERU0.PDOUT1	O	CCU40.IN0AD; CCU40.IN1AJ; CCU41.IN0AD; CCU41.IN1AJ; USIC0_CH1.HWIN2; P2.10;	
ERU0.GOUT1	O	P2.10;	
ERU0.TOUT1	O	not connected	
ERU0.IOUT1	O	NVIC; CCU40.CLKC; CCU40.IN1AK; CCU41.IN1AK;	
ERU0.PDOUT2	O	CCU40.IN3AD; CCU40.IN2AJ; CCU41.IN3AD; CCU41.IN2AJ; P2.1;	

Table 142 ERU0 Pin Connections (continued)

Global Input/Output	I/O	Connected To	Description
ERU0.GOUT2	O	P2.1;	
ERU0.TOUT2	O	not connected	
ERU0.IOUT2	O	NVIC; CCU40.IN2AK; CCU41.IN2AK;	
ERU0.PDOUT3	O	CCU40.IN2AD; CCU40.IN3AJ; CCU41.IN2AD; CCU41.IN3AJ; P2.0;	
ERU0.GOUT3	O	P2.0;	
ERU0.TOUT3	O	not connected	
ERU0.IOUT3	O	NVIC; CCU40.IN3AK; CCU41.IN3AK; POSIF1.EWHED;	

8.10.2 ERU1 Connections

The following table shows the ERU1 connections.

Table 143 ERU1 Pin Connections

Global Input/Output	I/O	Connected To	Description
ERU1.0A0	I	ACMP1.OUT	
ERU1.0A1	I		
ERU1.0A2	I	P4.4	
ERU1.0A3	I	P4.7	
ERU1.0B0	I	CCU40.ST0	
ERU1.0B1	I	CCU41.ST0	
ERU1.0B2	I	CCU80.ST0	
ERU1.0B3	I	CCU81.ST0	
ERU1.1A0	I	ACMP3.OUT;	
ERU1.1A1	I		
ERU1.1A2	I	P4.5	
ERU1.1A3	I		
ERU1.1B0	I	CCU40.ST1	
ERU1.1B1	I	CCU41.ST1	

Table 143 ERU1 Pin Connections (continued)

Global Input/Output	I/O	Connected To	Description
ERU1.1B2	I	CCU80.ST3	
ERU1.1B3	I	CCU81.ST3	
ERU1.2A0	I	ACMP2.OUT	
ERU1.2A1	I		
ERU1.2A2	I	P4.6	
ERU1.2A3	I		
ERU1.2B0	I	CCU40.ST2	
ERU1.2B1	I	CCU41.ST2	
ERU1.2B2	I	CCU80.ST1	
ERU1.2B3	I	CCU81.ST1	
ERU1.3A0	I	ACMP0.OUT	
ERU1.3A1	I	POSIF1.SR1	
ERU1.3A2	I		
ERU1.3A3	I		
ERU1.3B0	I	CCU40.ST3	
ERU1.3B1	I	CCU41.ST3	
ERU1.3B2	I	CCU80.ST2	
ERU1.3B3	I	CCU81.ST2	
ERU1.OGU01	I	CCU41.SR0	
ERU1.OGU02	I	CAN0.SR4;	
ERU1.OGU03	I	CCU81.SR2	
ERU1.OGU11	I	CCU41.SR1	
ERU1.OGU12	I	CAN0.SR5;	
ERU1.OGU13	I	CCU81.SR2	
ERU1.OGU21	I	CCU41.SR2	
ERU1.OGU22	I	CAN0.SR6;	
ERU1.OGU23	I	CCU81.SR3	
ERU1.OGU31	I	CCU41.SR3	
ERU1.OGU32	I	CAN0.SR7;	
ERU1.OGU33	I	CCU81.SR3	

Table 143 ERU1 Pin Connections (continued)

Global Input/Output	I/O	Connected To	Description
ERU1.PDOUT0	O	CCU40.IN0AW; CCU40.IN1AY; CCU41.IN0AW; CCU41.IN1AY; POSIF1.IN0D; P4.0;	
ERU1.GOUT0	O	P4.0	
ERU1.TOUT0	O	not connected	
ERU1.IOUT0	O	NVIC; CCU40.CLKA; CCU40.IN0AX; CCU41.IN0AX; CCU41.CLKB; POSIF1.EWHEB;	
ERU1.PDOUT1	O	CCU40.IN0AY; CCU40.IN1AW; CCU41.IN0AY; CCU41.IN1AW; POSIF1.IN1D; P1.1; P4.1;	
ERU1.GOUT1	O	P4.1	
ERU1.TOUT1	O	not connected	
ERU1.IOUT1	O	NVIC; CCU41.CLKC; CCU40.IN1AX; CCU41.IN1AX;	
ERU1.PDOUT2	O	CCU40.IN2AW; CCU40.IN3AY; CCU41.IN2AW; CCU41.IN3AY; POSIF1.IN2D; P4.2;	
ERU1.GOUT2	O	P4.2	
ERU1.TOUT2	O	not connected	

Table 143 ERU1 Pin Connections (continued)

Global Input/Output	I/O	Connected To	Description
ERU1.IOUT2	O	NVIC; CCU40.IN2AX; CCU41.IN2AX; POSIF1.MSETF;	
ERU1.PDOUT3	O	CCU40.IN3AW; CCU40.IN2AY; CCU41.IN2AY; CCU41.IN3AW; P4.3;	
ERU1.GOUT3	O	P4.3	
ERU1.TOUT3	O	not connected	
ERU1.IOUT3	O	NVIC; CCU40.IN3AX; CCU41.IN3AX; POSIF1.EWHEC; POSIF1.MSETG;	

9 Bus System

The single master bus system in IMC300A consists of a high-performance system bus based on the industry AMBA 3 AHB-Lite Protocol standard for memories and high-bandwidth on-chip peripherals and a narrower APB for low-bandwidth on-chip peripherals.

9.1 Bus Interfaces

This chapter describes the features for the two kinds of interfaces.

- Memory Interface
- Peripheral Interface

All on-chip modules implement Little Endian data organization.

Memory Interface

The on-chip memories are capable to accept a transfer request with each bus clock cycle.

The memory interface data bus width is 32-bit. Flash memory supports only 32-bit accesses while SRAM allows 32-bit, 16-bit and 8-bit write accesses. Read accesses to SRAM is always 32-bit wide.

Peripheral Interface

Each slave on the AHB-Lite supports 32-bit accesses. Additionally:

- USIC0 supports 8-bit and 16-bit accesses
- MATH coprocessor supports 16-bit accesses for the Divider registers

Each slave on the APB supports only 16-bit accesses.

Note: Unaligned memory accesses to memory or peripheral slaves result in a HardFault exception.

10 Memory Organization

This chapter provides description of the system memory organization, memory accesses and memory protection strategy.

10.1 Overview

The memory map in IMC300A is based on standard ARM™ Cortex-M0 system memory map.

10.1.1 Features

The memory map implements the following features:

- Compatibility with standard ARM Cortex-M0 CPU *[1]*
- Full compatibility across entire iMOTION Controller

10.1.2 Cortex-M0 Address Space

The system memory map defines several regions. Address boundaries of each of the regions are determined by the Cortex-M0 core architecture.

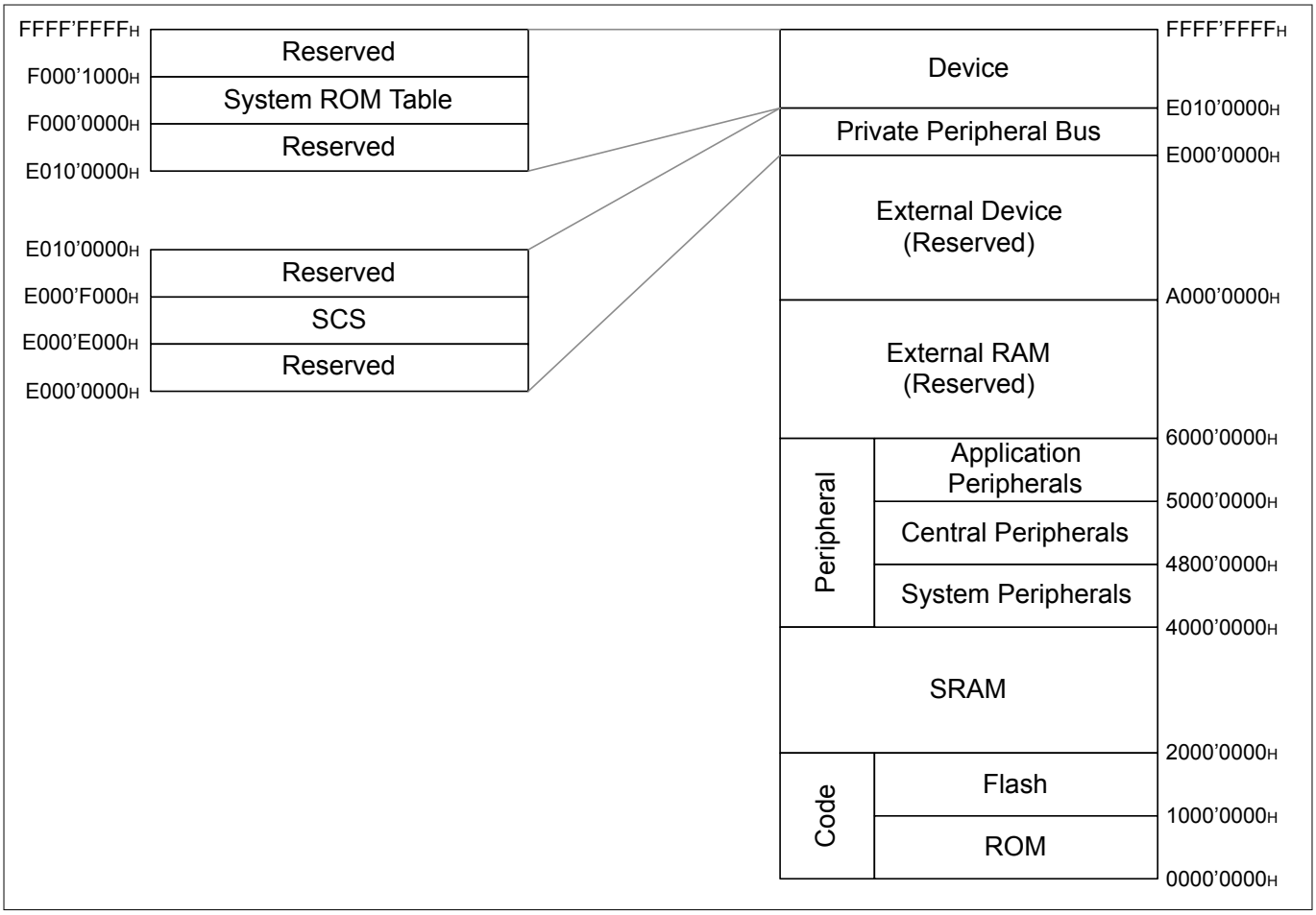


Figure 28 IMC300A Address Space

10.2 Memory Regions

The IMC300A device-specific address map contains on-chip memories and peripherals. The memory regions for IMC300A are described in ***Table 144***.

Table 144 Memory Regions

Start (hex)	End (hex)	Size (hex)	Space name	Usage
00000000	1FFFFFFF	20000000	Code	ROM Firmware, Flash
20000000	3FFFFFFF	20000000	SRAM	Fast internal SRAM
40000000	47FFFFFF	08000000	Peripheral	System Peripherals group
48000000	4FFFFFFF	08000000	Peripheral	Central Peripherals group
50000000	57FFFFFF	08000000	Peripheral	Application Peripherals group
58000000	5FFFFFFF	08000000	Peripheral	reserved
60000000	9FFFFFFF	40000000	External SRAM	reserved
A0000000	DFFFFFFF	40000000	External Device	reserved
E0000000	E00FFFFF	00100000	Private Peripheral Bus	CPU
E0100000	EFFFFFFF	0FF00000	Vendor specific 1	reserved
F0000000	FFFFFFFF	10000000	Vendor specific 2	System ROM Table

10.3 Memory Map

The tables in the following sections define detailed system memory map of IMC300A where each individual peripheral or memory instance implement its own address spaces. For detailed register description of the system components and peripherals, please refer to respective chapters of this document.

Note: Depending on the device variant, not all peripherals and memory address ranges may be available.

Address space: Code

Table 145 Address space: Code

Address range	Description	Access Type [17]	
		Read	Write
00000000_H - $00000CFF_H$	ROM (user-readable)	U, PV	nBE
$00000D00_H$ - $00001FFF_H$	ROM (non-user-readable)	BE	BE
00002000_H - $0FFFFFFF_H$	reserved	BE	BE

17 For address ranges taken up by peripherals, the access type for each address in the range may differ from that shown in the table. Refer to respective chapters for details.

Table 145 Address space: Code (continued)

Address range	Description	Access Type [17]	
		Read	Write
10000000_H - $10000DFF_H$	Flash Sector 0 (non-user-readable)	nBE	nBE
$10000E00_H$ - $10000FFF_H$	Flash Sector 0 (user-readable)	U, PV	nBE
10001000_H - $10020FFF_H$	Flash (128 Kbytes)	U, PV	U, PV
10021000_H - $1FFFFFFF_H$	reserved	BE	BE

Address space: SRAM

Table 146 Address space: SRAM

Address range [18]	Description	Access Type [17]	
		Read	Write
20000000_H - $20000FFF_H$	SRAM Block 0	U, PV	U, PV
20001000_H - $20001FFF_H$	SRAM Block 1	U, PV	U, PV
20002000_H - $20002FFF_H$	SRAM Block 2	U, PV	U, PV
20003000_H - $20003FFF_H$	SRAM Block 3	U, PV	U, PV
20004000_H - $3FFFFFFF_H$	reserved	BE	BE

Address space: System peripherals

Table 147 Address space: System peripherals

Address range	Description	Access Type [17]	
		Read	Write
40000000_H - $400007FF_H$	Memory Control	U, PV	U, PV
40000800_H - $4000FFFF_H$	reserved	BE	BE
40010000_H - $40010FFF_H$	SCU (including RTC)	U, PV	U, PV
40011000_H - $400110FF_H$	ANACTRL	U, PV	U, PV
40011100_H - $4001FFFF_H$	reserved	BE	BE
40020000_H - $4002001F_H$	WDT	U, PV	U, PV
40020020_H - $4002FFFF_H$	reserved	BE	BE
40030000_H - $4003003F_H$	MATH Global Registers and DIV	U, PV	U, PV
40030040_H - $4003007F_H$	MATH CORDIC	U, PV	U, PV
40030080_H - $4003FFFF_H$	reserved	BE	BE

17 For address ranges taken up by peripherals, the access type for each address in the range may differ from that shown in the table. Refer to respective chapters for details.

Table 147 Address space: System peripherals (continued)

Address range	Description	Access Type [17]	
		Read	Write
40040000_H - $4004007F_H$	Port 0	U, PV	U, PV
40040080_H - $400400FF_H$	reserved	BE	BE
40040100_H - $4004017F_H$	Port 1	U, PV	U, PV
40040180_H - $400401FF_H$	reserved	BE	BE
40040200_H - $4004027F_H$	Port 2	U, PV	U, PV
40040280_H - $400402FF_H$	reserved	BE	BE
40040300_H - $4004037F_H$	Port 3	U, PV	U, PV
40040380_H - $400403FF_H$	reserved	BE	BE
40040400_H - $4004047F_H$	Port 4	U, PV	U, PV
40040480_H - $4004FFFF_H$	reserved	BE	BE
40050000_H - $400500DF_H$	Flash Registers	U, PV	U, PV
$400500E0_H$ - $47FFFFFF_H$	reserved	BE	BE

Address space: Central peripherals

Table 148 Address space: Central peripherals

Address range	Description	Access Type [17]	
		Read	Write
48000000_H - $480001FF_H$	USIC0 Channel 0	U, PV	U, PV
48000200_H - $480003FF_H$	USIC0 Channel 1	U, PV	U, PV
48000400_H - $480007FF_H$	USIC0 RAM	nBE	BE
48000800_H - $48003FFF_H$	reserved	BE	BE
48004000_H - $480041FF_H$	USIC1 Channel 0	U, PV	U, PV
48004200_H - $480043FF_H$	USIC1 Channel 1	U, PV	U, PV
48004400_H - $480047FF_H$	USIC1 RAM	nBE	BE
48004800_H - $4801FFFF_H$	reserved	BE	BE
48020000_H - $4802000F_H$	PRNG	U, PV	U, PV
48020010_H - $4802FFFF_H$	reserved	BE	BE
48030000_H - $480303FF_H$	VADC0 General and Global Registers	U, PV	U, PV
48030400_H - $480307FF_H$	VADC0 Group 0	U, PV	U, PV
48030800_H - $48030BFF_H$	VADC0 Group 1	U, PV	U, PV
$48030C00_H$ - $48033FFF_H$	reserved	BE	BE

17 For address ranges taken up by peripherals, the access type for each address in the range may differ from that shown in the table. Refer to respective chapters for details.

Table 148 Address space: Central peripherals (continued)

Address range	Description	Access Type [17]	
		Read	Write
48034000_H - $480341FF_H$	SHS0	U, PV	U, PV
48034200_H - $4803FFFF_H$	reserved	BE	BE
48040000_H - $480401FF_H$	CCU40 CC40 and Kernel Registers	U, PV	U, PV
48040200_H - $480402FF_H$	CCU40 CC41	U, PV	U, PV
48040300_H - $480403FF_H$	CCU40 CC42	U, PV	U, PV
48040400_H - $480404FF_H$	CCU40 CC43	U, PV	U, PV
48040500_H - $48043FFF_H$	reserved	BE	BE
48044000_H - $480441FF_H$	CCU41 CC40 and Kernel Registers	U, PV	U, PV
48044200_H - $480442FF_H$	CCU41 CC41	U, PV	U, PV
48044300_H - $480443FF_H$	CCU41 CC42	U, PV	U, PV
48044400_H - $480444FF_H$	CCU41 CC43	U, PV	U, PV
48044500_H - $4FFFFFFF_H$	reserved	BE	BE

Address space: Application peripherals

Table 149 Address space: Application peripherals

Address range	Description	Access Type [17]	
		Read	Write
50000000_H - $500001FF_H$	CCU80 CC80 and Kernel Registers	U, PV	U, PV
50000200_H - $500002FF_H$	CCU80 CC81	U, PV	U, PV
50000300_H - $500003FF_H$	CCU80 CC81	U, PV	U, PV
50000400_H - $500004FF_H$	CCU80 CC83	U, PV	U, PV
50000500_H - $50003FFF_H$	reserved	BE	BE
50004000_H - $500041FF_H$	CCU81 CC80 and Kernel Registers	U, PV	U, PV
50004200_H - $500042FF_H$	CCU81 CC81	U, PV	U, PV
50004300_H - $500043FF_H$	CCU81 CC81	U, PV	U, PV
50004400_H - $500044FF_H$	CCU81 CC83	U, PV	U, PV
50004500_H - $5000FFFF_H$	reserved	BE	BE
50010000_H - $500101FF_H$	POSIF0	U, PV	U, PV
50010200_H - $50013FFF_H$	reserved	BE	BE

17 For address ranges taken up by peripherals, the access type for each address in the range may differ from that shown in the table. Refer to respective chapters for details.

Table 149 Address space: Application peripherals (continued)

Address range	Description	Access Type [17]	
		Read	Write
50014000_H - $500141FF_H$	POSIF1	U, PV	U, PV
50014200_H - $5001FFFF_H$	reserved	BE	BE
50020000_H - $5003FFFF_H$	reserved	BE	BE
50040000_H - $500402FF_H$	MultiCAN Node 0 and Global Registers	U, PV	U, PV
50040300_H - $500403FF_H$	MultiCAN Node 1	U, PV	U, PV
50040400_H - $50040FFF_H$	reserved	BE	BE
50041000_H - $50043FFF_H$	MultiCAN Message Object Registers	U, PV	U, PV
50044000_H - $5FFFFFFF_H$	reserved	BE	BE

Address space: External SRAM

Table 150 Address space: External SRAM

Address range	Description	Access Type [17]	
		Read	Write
60000000_H - $9FFFFFFF_H$	reserved	BE	BE

Address space: External device

Table 151 Address space: External device

Address range	Description	Access Type [17]	
		Read	Write
$A0000000_H$ - $DFFFFFFF_H$	reserved	BE	BE

Address space: Private peripheral bus

Table 152 Address space: Private peripheral bus

Address range	Description	Access Type [17]	
		Read	Write
$E0000000_H$ - $E00FFFFF_H$	NVIC, System timer, System Control Block	U, PV	U, PV

17 For address ranges taken up by peripherals, the access type for each address in the range may differ from that shown in the table. Refer to respective chapters for details.

18 The address range $2000'0000_H$ to $2000'01FF_H$ will be overwritten by start-up software during device start-up

Address space: Vendor specific 1

Table 153 Address space: Vendor specific 1

Address range	Description	Access Type [17]	
		Read	Write
$E0100000_H$ - $EFFFFFFF_H$	reserved	BE	BE

Address space: Vendor specific 2

Table 154 Address space: Vendor specific 2

Address range	Description	Access Type [17]	
		Read	Write
$F0000000_H$ - $F0000FFF_H$	System ROM Table	U, PV	nBE
$F0001000_H$ - $FFFFFFFF_H$	reserved	BE	BE

10.4 Memory Access

This section describes the memory accesses to the different type of memories in IMC300A.

10.4.1 Flash Memory Access

The IMC300A provides up to 128 Kbytes of Flash memory for instruction code or constant data, starting at address $1000'1000_H$. This excludes Flash sector 0, which is used to store system information and is always read only.

The Flash memory will insert waitstates during memory read automatically if needed.

For details of Flash memory access, refer to the Flash Architecture chapter.

10.4.2 SRAM Access

The IMC300A provides 16 Kbytes of SRAM for instruction code or constant data, as well as system variables such as the system stack, starting at address $2000'0000_H$.

The SRAM supports 8-bit, 16-bit and 32-bit writes, and generates one parity bit for each 8 bits of written data. A read operation will check for parity errors on the 32-bit read data. Accesses to the SRAM require no wait states.

The 16 Kbytes of SRAM is logically divided into four blocks of 4 Kbytes each. Accesses to blocks 1, 2 and 3 can be disabled and enabled again during run-time with the peripheral privilege access scheme. See PAU chapter for details.

Note: The address range $2000'0000_H$ to $2000'01FF_H$ will be overwritten by the start-up software during device start-up. Therefore, these addresses should not be targeted during the download of code/data by the bootstrap loader into the SRAM nor should they store critical data that are still needed by the application after a system reset or SW master reset.

17 For address ranges taken up by peripherals, the access type for each address in the range may differ from that shown in the table. Refer to respective chapters for details.

10.4.3 ROM Access

The IMC300A provides 8 Kbytes of ROM, which contains the startup software, vector table and user routines.

Read accesses to the ROM require no wait states.

10.5 Memory Protection Strategy

Two aspects of memory protection are considered:

1. Intellectual Property (IP) Protection
2. Memory Access Protection during Run-time

The memory protection measures available in IMC300A are listed in ***Table 155***.

Table 155 Memory Protection Measures

Protection Aspects	Protection Measures	Protection Target
IP protection	Blocking of unauthorized external access	Flash memory contents
Memory access protection	Bit protection scheme	Specific system-critical registers/bit fields
	Peripheral privilege access control	Specific address ranges; each range can be controlled independently

10.5.1 Intellectual Property (IP) Protection

IP protection refers to the prevention against unauthorized read out of critical data and user IP from Flash memory.

10.5.1.1 Blocking of Unauthorized External Access

In IMC300A, the Boot Mode Index (BMI) is used to control the boot options such that once the BMI is programmed to enter user mode (productive), it is not allowed to enter the other boot modes without an erase of the complete user Flash (including sector 0).

Therefore, boot options that load and execute external code, including unauthorized code that might read out the Flash memory contents, will be blocked and only user code originating from the Flash memory can be executed.

10.5.2 Memory Access Protection during Run-time

Memory access protection refers to the prevention against unintended write access on a memory address space during run-time.

10.5.2.1 Bit Protection Scheme

The bit protection scheme prevents direct software writing of selected register bits (i.e., protected bits) using the PASSWD register in the SCU module. When the bit field MODE is 11_B, writing 10011_B to the bit field PASS opens access to writing of all protected bits, and writing 10101_B to the bit field PASS closes access to writing of all protected bits. In both cases, the value of the bit field MODE is not changed even if PASSWD register is written with 98_H or $A8_H$. It can only be changed when bit field PASS is written with 11000_B, for example, writing $0000'00C0_H$ to PASSWD register disables the bit protection scheme.

Access is opened for maximum 32 MCLKs if the “close access” password is not written. If “open access” password is written again before the end of 32 MCLK cycles, there will be a recount of 32 MCLK cycles.

Table 156 shows the list of protected bit in IMC300A.

Table 156 List of Protected Register Bit Fields

Register	Bit Field
SCU_CLKCR, SCU_CLKCR1	FDIV, IDIV, PCLKSEL, RTCLKSEL, ADCCLKSEL, DCLKSEL
SCU_OSCCSR	DCO1PD
SCU_ANAOSCHPCTRL	All bits
SCU_ANASYNC1, SCU_ANASYNC2	All bits
SCU_ANAOFFSET	ADJL_OFFSET
SCU_CGATSET0	All bits
SCU_CGATCLR0	All bits
VADC0_ACCPROT0	All bits
VADC0_ACCPROT1	All bits

Write to all protected registers except VADC0_ACCPROT[1:0], without opening access through bit field PASS, will be ignored. No bus error will be generated. User should read back the register value to ensure the write has taken place.

Write to VADC0_ACCPROT[1:0], without opening access through bit field PASS, will trigger a hard fault. If an interrupt occurs immediately after the access is opened and the interrupt service routine requires more than 32 MCLK cycles, the write to the register will happen after the access is closed and thereby, triggering a hard fault. To avoid this, interrupts should be disabled before writing to these two registers.

The PASSWD register is also described in the SCU chapter.

10.5.2.1.1 Register SCU_PASSWD

SCU_PASSWD Address: $4001\ 0024_H$

Password Register Reset Value: $0000\ 0007_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								PASS					PROTS	MODE	
r								w					rh	rw	

Field	Bits	Type	Description
MODE	1:0	rw	**Bit Protection Scheme Control Bits** 00_B Scheme disabled - direct access to the protected bits is allowed. 11_B Scheme enabled - the bit field PASS has to be written with the passwords to open and close the access to the protected bits. (Default) Others: Scheme enabled, similar to the setting for MODE = 11_B. These two bits cannot be written directly. To change the value between 11_B and 00_B, the bit field PASS must be written with 11000_B. Only then will the MODE bit field be registered.
PROTS	2	rh	**Bit Protection Signal Status Bit** This bit shows the status of the protection. 0_B Software is able to write to all protected bits. 1_B Software is unable to write to any of the protected bits.
PASS	7:3	w	**Password Bits** This bit protection scheme only recognizes the following three passwords: 11000_B Enables writing of the bit field MODE. 10011_B Opens access to writing of all protected bits. 10101_B Closes access to writing of all protected bits.
0	31:8	r	**Reserved**

10.5.2.2 Peripheral Privilege Access Control

All CPU accesses are privileged accesses. In IMC300A, a separate scheme called Peripheral Privilege Access Control, which allows a peripheral's memory address space to be disabled to block any unintended write or read access, is provided. The address space can be re-enabled when necessary.

Refer to the PAU chapter for details.

10.6 Service Request Generation

Memory modules and other system components are capable of generating error responses indicated to the CPU as bus error exceptions or interrupts.

Types of Error Causes

- Unsupported Access Mode
- Access to Invalid Address
- Data integrity Error (memories only)

Errors that cannot be indicated with bus errors get indicated with service requests that get propagated to the CPU as interrupts.

Unsupported Access Modes

Unsupported access modes can be classified in various ways and are usually specific to the module that access is performed to. Typical examples of unsupported access modes are write access to read-only type of address mapped resources, protected memory regions. For module specific limitations please refer to individual module chapters.

Invalid Address

Accesses to invalid addresses result in error responses. Invalid addresses are defined as those that do not mapped to any valid resources. This applies to single addresses and to wider address ranges. Some invalid addresses within valid module address ranges may not produce error responses and this is specific to individual modules.

Data Integrity Error

Accesses to corrupted data in the memories result in either ECC (Error Correction Code) (ECC) or parity errors. The occurrence of such errors get signalized to the system through an SCU interrupt.

10.7 Debug Behaviour

The bus system in debug mode allows debug probe access to all system resources. No special handling of HALT mode is implemented and all interfaces respond with a valid bus response upon accesses.

10.8 Power, Reset and Clock

The bus system clocking scheme enables stable system operation and accesses to system resources for all valid system clock rates.

10.9 Initialization and System Dependencies

No initialization is required for the memory system from user point of view. All valid memories are available after reset. Some peripherals may need to be initialized (e.g. disable clock gating) before they can be accessed. For details please refer to individual peripheral chapters.

11 Peripheral Access Unit (PAU)

This chapter describes Peripheral Access Unit (PAU) in IMC300A.

11.1 Overview

The PAU supports access control of memories and peripherals in a central place.

11.1.1 Features

The PAU provides the following features:

- Allows user application to enable/disable the access to the registers of a peripheral
- Generates a HardFault exception when there is an access to a disabled or unassigned address location
- Provides information on availability of peripherals and size of memories

11.2 Peripheral Privilege Access Control

The user application can use the Peripheral Privilege Access Registers, PRIVDISn, to disable access to a peripheral. When the PDISx bit corresponding to the peripheral is set, the memory address space mapped to the peripheral is rendered invalid. An access to such an invalid address causes a HardFault exception.

The application can clear the same bit to enable accesses to the peripheral again.

Table 157 shows the peripherals and their assigned PDISx bits. Peripherals without a PDISx bit are accessible at all times.

Table 157 Peripherals Availability and Privilege Access Control

Peripheral	Address Grouping	AVAILn.AVAILx bit	PRIVDIS.PDISx bit
Flash	Flash SFRs	-	PRIVDIS0.2
SRAM	RAM Block 1	AVAIL0.5	PRIVDIS0.5
	RAM Block 2	AVAIL0.6	PRIVDIS0.6
	RAM Block 3	AVAIL0.7	PRIVDIS0.7
WDT	WDT	-	PRIVDIS0.19
MATH	MATH Global SFRs and DIV	AVAIL0.20	PRIVDIS0.20
	MATH CORDIC	AVAIL0.21	PRIVDIS0.21
Ports	Port 0	AVAIL0.22	PRIVDIS0.22
	Port 1	AVAIL0.23	PRIVDIS0.23
	Port 2	AVAIL0.24	PRIVDIS0.24
	Port 3	AVAIL0.25	PRIVDIS0.25
	Port 4	AVAIL0.26	PRIVDIS0.26
USIC0	USIC0_CH0	AVAIL1.0	PRIVDIS1.0
	USIC0_CH1	AVAIL1.1	PRIVDIS1.1
PRNG	PRNG	AVAIL1.4	-
VADC0	VADC0 Basic SFRs	AVAIL1.5	PRIVDIS1.5
	VADC0 Group 0 SFRs	AVAIL1.6	PRIVDIS1.6

Table 157 Peripherals Availability and Privilege Access Control (continued)

Peripheral	Address Grouping	AVAILn.AVAILx bit	PRIVDIS.PDISx bit
	VADC0 Group 1 SFRs	AVAIL1.7	PRIVDIS1.7
SHS0	SHS0	AVAIL1.8	PRIVDIS1.8
CCU40	CCU40_CC40 and CCU40 Kernel SFRs	AVAIL1.9	PRIVDIS1.9
	CCU40_CC41	AVAIL1.10	PRIVDIS1.10
	CCU40_CC42	AVAIL1.11	PRIVDIS1.11
	CCU40_CC43	AVAIL1.12	PRIVDIS1.12
USIC1	USIC1_CH0	AVAIL1.16	PRIVDIS1.16
	USIC1_CH1	AVAIL1.17	PRIVDIS1.17
CCU41	CCU41_CC40 and CCU41 Kernel SFRs	AVAIL1.25	PRIVDIS1.25
	CCU41_CC41	AVAIL1.26	PRIVDIS1.26
	CCU41_CC42	AVAIL1.27	PRIVDIS1.27
	CCU41_CC43	AVAIL1.28	PRIVDIS1.28
CCU80	CCU80_CC80 and CCU80 Kernel SFRs	AVAIL2.0	PRIVDIS2.0
	CCU80_CC81	AVAIL2.1	PRIVDIS2.1
	CCU80_CC82	AVAIL2.2	PRIVDIS2.2
	CCU80_CC83	AVAIL2.3	PRIVDIS2.3
POSIF0	POSIF0	AVAIL2.12	PRIVDIS2.12
DAC0	DAC0	AVAIL2.15	PRIVDIS2.15
CCU81	CCU81_CC81 and CCU80 Kernel SFRs	AVAIL2.16	PRIVDIS2.16
	CCU81_CC81	AVAIL2.17	PRIVDIS2.17
	CCU81_CC82	AVAIL2.18	PRIVDIS2.18
	CCU81_CC83	AVAIL2.19	PRIVDIS2.19
CAN0	MultiCAN Global and Node 0 SFRs	AVAIL2.20	PRIVDIS2.20
	MultiCAN Node 1 SFRs	AVAIL2.21	PRIVDIS2.21
	MultiCAN Message Objects	AVAIL2.23	PRIVDIS2.23
POSIF1	POSIF1	AVAIL2.28	PRIVDIS2.28

11.3 Peripheral Availability and Memory Size

The availability of peripherals and memory sizes varies according to product variants. The user application can read the Peripheral Availability Registers, AVAILn, to check for the availability of peripherals in a product variant. Refer to ***Table 157*** for the bit assignment. Similarly, the Memory Size Registers (e.g. FLSIZE for Flash memory) can be used to check for the size of the available memories.

11.4 Service Request Generation

The PAU generates a hard fault exception when there is an access to an invalid address.

11.5 Debug Behaviour

The PAU does not support a suspend mode while the system is halted by the debugger. That means that the PAU continues its operation during debug halt.

11.6 Power, Reset and Clock

The PAU is located in the core power domain.

The module can be reset to its default state by a system reset. The PAU module is clocked by the main clock, MCLK, from SCU.

11.7 Initialization and System Dependencies

The PAU is always available after reset.

11.8 PAU Registers

Registers Overview

The absolute register address is calculated by adding:
Module Base Address + Offset Address

Table 158 Registers Address Space

Module	Base Address	End Address	Note
PAU	4000 0000$_H$	4000 FFFF$_H$	

Table 159 Register Overview

Short Name	Description	Offset Addr.	Access Mode		Description See
			Read	Write	
Reserved	Reserved	0000$_H$ - 003C$_H$	nBE	nBE	
AVAIL0	Peripheral Availability Register 0	0040$_H$	U, PV	BE	Page 205
AVAIL1	Peripheral Availability Register 1	0044$_H$	U, PV	BE	Page 206
AVAIL2	Peripheral Availability Register 2	0048$_H$	U, PV	BE	Page 208
Reserved	Reserved	004C$_H$ - 007C$_H$	nBE	nBE	
PRIVDIS0	Peripheral Privilege Access Register 0	0080$_H$	U, PV	U, PV	Page 200
PRIVDIS1	Peripheral Privilege Access Register 1	0084$_H$	U, PV	U, PV	Page 201
PRIVDIS2	Peripheral Privilege Access Register 2	0088$_H$	U, PV	U, PV	Page 203
Reserved	Reserved	008C$_H$ - 03FC$_H$	nBE	nBE	
ROMSIZE	ROM Size Register	0400$_H$	U, PV	BE	Page 209

Table 159 Register Overview (continued)

Short Name	Description	Offset Addr.	Access Mode		Description See
			Read	Write	
FLSIZE	Flash Size Register	0404_H	U, PV	BE	Page 210
RAM0SIZE	RAM0 Size Register	0410_H	U, PV	BE	Page 210
Reserved	Reserved	0414_H - $07FF_H$	nBE	nBE	

11.8.1 Peripheral Privilege Access Registers (PRIVDISn)

The PRIVDISn registers provide the bit to enable and disable access to a peripheral during runtime. When disabled, an access to the peripheral throws a BusFault.

11.8.1.1 Register PRIVDIS0

PRIVDIS0 Address: 0080_H

Peripheral Privilege Access Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0					PDIS 26	PDIS 25	PDIS 24	PDIS 23	PDIS 22	PDIS 21	PDIS 20	PDIS 19	0		
r					rw	rw	rw	rw	rw	rw	rw	rw	r		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								PDIS 7	PDIS 6	PDIS 5	0		PDIS 2	0	
r								rw	rw	rw	r		rw	r	

Field	Bits	Type	Description
PDIS2	2	rw	**Flash SFRs Privilege Disable Flag** 0_B Flash SFRs are accessible. 1_B Flash SFRs are not accessible.
PDIS5	5	rw	**RAM Block 1 Privilege Disable Flag** 0_B RAM Block 1 is accessible. 1_B RAM Block 1 is not accessible.
PDIS6	6	rw	**RAM Block 2 Privilege Disable Flag** 0_B RAM Block 2 is accessible. 1_B RAM Block 2 is not accessible.
PDIS7	7	rw	**RAM Block 3 Privilege Disable Flag** 0_B RAM Block 3 is accessible. 1_B RAM Block 3 is not accessible.

(continued)

Field	Bits	Type	Description
PDIS19	19	rw	**WDT Privilege Disable Flag** 0_B WDT is accessible. 1_B WDT is not accessible.
PDIS20	20	rw	**MATH Global SFRs and Divider Privilege Disable Flag** 0_B MATH Global SFRs and Divider are accessible. 1_B MATH Global SFRs and Divider are not accessible.
PDIS21	21	rw	**MATH CORDIC Privilege Disable Flag** 0_B MATH CORDIC is accessible. 1_B MATH CORDIC is not accessible.
PDIS22	22	rw	**Port 0 Privilege Disable Flag** 0_B Port 0 is accessible. 1_B Port 0 is not accessible.
PDIS23	23	rw	**Port 1 Privilege Disable Flag** 0_B Port 1 is accessible. 1_B Port 1 is not accessible.
PDIS24	24	rw	**Port 2 Privilege Disable Flag** 0_B Port 2 is accessible. 1_B Port 2 is not accessible.
PDIS25	25	rw	**Port 3 Privilege Disable Flag** 0_B Port 3 is accessible. 1_B Port 3 is not accessible.
PDIS26	26	rw	**Port 4 Privilege Disable Flag** 0_B Port 4 is accessible. 1_B Port 4 is not accessible.
0	31:27, 18:8, 4:3, 1:0	r	**Reserved**

11.8.1.2 Register PRIVDIS1

PRIVDIS1 Address: 0084_H

Peripheral Privilege Access Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0			PDIS 28	PDIS 27	PDIS 26	PDIS 25	0							PDIS 17	PDIS 16
r			rw	rw	rw	rw	r							rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0			PDIS 12	PDIS 11	PDIS 10	PDIS 9	PDIS 8	PDIS 7	PDIS 6	PDIS 5	0			PDIS 1	PDIS 0
r			rw	rw	rw	rw	rw	rw	rw	rw	r			rw	rw

Field	Bits	Type	Description
PDIS0	0	rw	**USIC0 Channel 0 Privilege Disable Flag** 0_B USIC0 Channel 0 is accessible. 1_B USIC0 Channel 0 is not accessible.
PDIS1	1	rw	**USIC0 Channel 1 Privilege Disable Flag** 0_B USIC0 Channel 1 is accessible. 1_B USIC0 Channel 1 is not accessible.
PDIS5	5	rw	**VADC0 Basic SFRs Privilege Disable Flag** 0_B VADC0 Basic SFRs are accessible. 1_B VADC0 Basic SFRs are not accessible.
PDIS6	6	rw	**VADC0 Group 0 SFRs Privilege Disable Flag** 0_B VADC0 Group 0 SFRs are accessible. 1_B VADC0 Group 0 SFRs are not accessible.
PDIS7	7	rw	**VADC0 Group 1 SFRs Privilege Disable Flag** 0_B VADC0 Group 1 SFRs are accessible. 1_B VADC0 Group 1 SFRs are not accessible.
PDIS8	8	rw	**SHS0 Privilege Disable Flag** 0_B SHS0 is accessible. 1_B SHS0 is not accessible.
PDIS9	9	rw	**CCU40 Kernel SFRs and CC40 Privilege Disable Flag** 0_B CCU40 Kernel SFRs and CC40 are accessible. 1_B CCU40 Kernel SFRs and CC40 are not accessible.
PDIS10	10	rw	**CCU40 CC41 Privilege Disable Flag** 0_B CCU40 CC41 is accessible. 1_B CCU40 CC41 is not accessible.
PDIS11	11	rw	**CCU40 CC42 Privilege Disable Flag** 0_B CCU40 CC42 is accessible. 1_B CCU40 CC42 is not accessible.
PDIS12	12	rw	**CCU40 CC43 Privilege Disable Flag** 0_B CCU40 CC43 is accessible. 1_B CCU40 CC43 is not accessible.
PDIS16	16	rw	**USIC1 Channel 0 Privilege Disable Flag** 0_B USIC1 Channel 0 is accessible. 1_B USIC1 Channel 0 is not accessible.
PDIS17	17	rw	**USIC1 Channel 1 Privilege Disable Flag** 0_B USIC1 Channel 1 is accessible. 1_B USIC1 Channel 1 is not accessible.
PDIS25	25	rw	**CCU41 Kernel SFRs and CC40 Privilege Disable Flag** 0_B CCU41 Kernel SFRs and CC40 are accessible. 1_B CCU41 Kernel SFRs and CC40 are not accessible.

(continued)

Field	Bits	Type	Description
PDIS26	26	rw	**CCU41 CC41 Privilege Disable Flag** 0_B CCU41 CC41 is accessible. 1_B CCU41 CC41 is not accessible.
PDIS27	27	rw	**CCU41 CC42 Privilege Disable Flag** 0_B CCU41 CC42 is accessible. 1_B CCU41 CC42 is not accessible.
PDIS28	28	rw	**CCU41 CC43 Privilege Disable Flag** 0_B CCU41 CC43 is accessible. 1_B CCU41 CC43 is not accessible.
0	31:29, 24:18, 15:13, 4:2	r	**Reserved**

11.8.1.3 Register PRIVDIS2

PRIVDIS2 Address: 0088_H

Peripheral Privilege Access Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0			PDIS 28	0				PDIS 23	0	PDIS 21	PDIS 20	PDIS 19	PDIS 18	PDIS 17	PDIS 16
r			rw	r				rw	r	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PDIS 15	0		PDIS 12	0								PDIS 3	PDIS 2	PDIS 1	PDIS 0
rw	r		rw	r								rw	rw	rw	rw

Field	Bits	Type	Description
PDIS0	0	rw	**CCU80 Kernel SFRs and CC80 Privilege Disable Flag** 0_B CCU80 Kernel SFRs and CC80 are accessible. 1_B CCU80 Kernel SFRs and CC80 are not accessible.
PDIS1	1	rw	**CCU80 CC81 Privilege Disable Flag** 0_B CCU80 CC81 is accessible. 1_B CCU80 CC81 is not accessible.
PDIS2	2	rw	**CCU80 CC82 Privilege Disable Flag** 0_B CCU80 CC82 is accessible. 1_B CCU80 CC82 is not accessible.
PDIS3	3	rw	**CCU80 CC83 Privilege Disable Flag** 0_B CCU80 CC83 is accessible. 1_B CCU80 CC83 is not accessible.

(continued)

Field	Bits	Type	Description
PDIS12	12	rw	**POSIF0 Privilege Disable Flag** 0_B POSIF0 is accessible. 1_B POSIF0 is not accessible.
PDIS15	15	rw	**DAC0 Privilege Disable Flag** 0_B DAC0 is accessible. 1_B DAC0 is not accessible.
PDIS16	16	rw	**CCU81 Kernel SFRs and CC80 Privilege Disable Flag** 0_B CCU81 Kernel SFRs and CC80 are accessible. 1_B CCU81 Kernel SFRs and CC80 are not accessible.
PDIS17	17	rw	**CCU81 CC81 Privilege Disable Flag** 0_B CCU81 CC81 is accessible. 1_B CCU81 CC81 is not accessible.
PDIS18	18	rw	**CCU81 CC82 Privilege Disable Flag** 0_B CCU81 CC82 is accessible. 1_B CCU81 CC82 is not accessible.
PDIS19	19	rw	**CCU81 CC83 Privilege Disable Flag** 0_B CCU81 CC83 is accessible. 1_B CCU81 CC83 is not accessible.
PDIS20	20	rw	**MultiCAN Node 0 and Global SFRs Privilege Disable Flag** 0_B MultiCAN node 0 and global SFRs are accessible. 1_B MultiCAN node 0 and global SFRs are not accessible.
PDIS21	21	rw	**MultiCAN Node 1 Privilege Disable Flag** 0_B MultiCAN node 1 is accessible. 1_B MultiCAN node 1 is not accessible.
PDIS23	23	rw	**MultiCAN Message Object SFRs Privilege Disable Flag** 0_B MultiCAN message object SFRs are accessible. 1_B MultiCAN message object SFRs are not accessible.
PDIS28	28	rw	**POSIF1 Privilege Disable Flag** 0_B POSIF1 is accessible. 1_B POSIF1 is not accessible.
0	31:29, 27:24, 22, 14:13, 11:4	r	**Reserved**

11.8.2 Peripheral Availability Registers (AVAILn)

The AVAILn registers indicate the available peripherals for the particular device variant.

Note: The reset values of AVAILn registers show the configuration with all peripherals available. Actual values might differ depending on the product variant.

11.8.2.1 Register AVAIL0

AVAIL0 Address: 0040_H

Peripheral Availability Register 0 Reset Value: $07FF\ 00FF_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0					AVAIL26	AVAIL25	AVAIL24	AVAIL23	AVAIL22	AVAIL21	AVAIL20	1			
r					r	r	r	r	r	r	r	r			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								AVAIL7	AVAIL6	AVAIL5	1				
r								r	r	r	r				

Field	Bits	Type	Description
AVAIL5	5	r	**RAM Block 1 Availability Flag** 0_B RAM block 1 is not available. 1_B RAM block 1 is available.
AVAIL6	6	r	**RAM Block 2 Availability Flag** 0_B RAM block 2 is not available. 1_B RAM block 2 is available.
AVAIL7	7	r	**RAM Block 3 Availability Flag** 0_B RAM block 3 is not available. 1_B RAM block 3 is available.
AVAIL20	20	r	**MATH Global SFRs and Divider Availability Flag** 0_B MATH Global SFRs and Divider are not available. 1_B MATH Global SFRs and Divider are available.
AVAIL21	21	r	**MATH CORDIC Availability Flag** 0_B MATH CORDIC is not available. 1_B MATH CORDIC is available.
AVAIL22	22	r	**Port 0 Availability Flag** 0_B Port 0 is not available. 1_B Port 0 is available.
AVAIL23	23	r	**Port 1 Availability Flag** 0_B Port 1 is not available. 1_B Port 1 is available.
AVAIL24	24	r	**Port 2 Availability Flag** 0_B Port 2 is not available. 1_B Port 2 is available.
AVAIL25	25	r	**Port 3 Availability Flag** 0_B Port 3 is not available. 1_B Port 3 is available.

(continued)

Field	Bits	Type	Description
AVAIL26	26	r	**Port 4 Availability Flag** 0_B Port 4 is not available. 1_B Port 4 is available.
1	19:16, 4:0	r	**Reserved**
0	31:27, 15:8	r	**Reserved**

11.8.2.2 Register AVAIL1

AVAIL1 Address: 0044_H

Peripheral Availability Register 1 Reset Value: $1E07\ 1FF7_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0			AVAIL28	AVAIL27	AVAIL26	AVAIL25	0						1	AVAIL17	AVAIL16
r			r	r	r	r	r						r	r	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0			AVAIL12	AVAIL11	AVAIL10	AVAIL9	AVAIL8	AVAIL7	AVAIL6	AVAIL5	AVAIL4	0	1	AVAIL1	AVAIL0
r			r	r	r	r	r	r	r	r	r	r	r	r	r

Field	Bits	Type	Description
AVAIL0	0	r	**USIC0 Channel 0 Availability Flag** 0_B USIC0 Channel 0 is not available. 1_B USIC0 Channel 0 is available.
AVAIL1	1	r	**USIC0 Channel 1 Availability Flag** 0_B USIC0 Channel 1 is not available. 1_B USIC0 Channel 1 is available.
AVAIL4	4	r	**PRNG Availability Flag** 0_B PRNG is not available. 1_B PRNG is available.
AVAIL5	5	r	**VADC0 Basic SFRs Availability Flag** 0_B VADC0 Basic SFRs are not available. 1_B VADC0 Basic SFRs are available.
AVAIL6	6	r	**VADC0 Group 0 SFRs Availability Flag** 0_B VADC0 Group 0 SFRs are not available. 1_B VADC0 Group 0 SFRs are available.
AVAIL7	7	r	**VADC0 Group 1 SFRs Availability Flag** 0_B VADC0 Group 1 SFRs are not available. 1_B VADC0 Group 1 SFRs are available.

(continued)

Field	Bits	Type	Description
AVAIL8	8	r	**SHS0 Availability Flag** 0_B SHS0 is not available. 1_B SHS0 is available.
AVAIL9	9	r	**CCU40 kernel SFRs and CC40 Availability Flag** 0_B CCU40 kernel SFRs and CC40 is not available. 1_B CCU40 kernel SFRs and CC40 is available.
AVAIL10	10	r	**CCU40 CC41 Availability Flag** 0_B CCU40 CC41 is not available. 1_B CCU40 CC41 is available.
AVAIL11	11	r	**CCU40 CC42 Availability Flag** 0_B CCU40 CC42 is not available. 1_B CCU40 CC42 is available.
AVAIL12	12	r	**CCU40 CC43 Availability Flag** 0_B CCU40 CC43 is not available. 1_B CCU40 CC43 is available.
AVAIL16	16	r	**USIC1 Channel 0 Availability Flag** 0_B USIC1 Channel 0 is not available. 1_B USIC1 Channel 0 is available.
AVAIL17	17	r	**USIC1 Channel 1 Availability Flag** 0_B USIC1 Channel 1 is not available. 1_B USIC1 Channel 1 is available.
AVAIL25	25	r	**CCU41 kernel SFRs and CC40 Availability Flag** 0_B CCU41 kernel SFRs and CC40 is not available. 1_B CCU41 kernel SFRs and CC40 is available.
AVAIL26	26	r	**CCU41 CC41 Availability Flag** 0_B CCU41 CC41 is not available. 1_B CCU41 CC41 is available.
AVAIL27	27	r	**CCU41 CC42 Availability Flag** 0_B CCU41 CC42 is not available. 1_B CCU41 CC42 is available.
AVAIL28	28	r	**CCU41 CC43 Availability Flag** 0_B CCU41 CC43 is not available. 1_B CCU41 CC43 is available.
1	2, 18	r	**Reserved**
0	31:29, 24:19, 15:13, 3	r	**Reserved**

11.8.2.3 Register AVAIL2

AVAIL2 Address: 0048_H

Peripheral Availability Register 2 Reset Value: $30BFF00F_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0			AVAIL28	0				AVAIL23	0	AVAIL21	AVAIL20	AVAIL19	AVAIL18	AVAIL17	AVAIL16
r			r	r				r	r	r	r	r	r	r	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AVAIL15	0		AVAIL12	0								AVAIL3	AVAIL2	AVAIL1	AVAIL0
r	r		r	r								r	r	r	r

Field	Bits	Type	Description
AVAIL0	0	r	**CCU80 kernel SFRs and CC80 Availability Flag** 0_B CCU80 kernel SFRs and CC80 are not available. 1_B CCU80 kernel SFRs and CC80 are available.
AVAIL1	1	r	**CCU80 CC81 Availability Flag** 0_B CCU80 CC81 is not available. 1_B CCU80 CC81 is available.
AVAIL2	2	r	**CCU80 CC82 Availability Flag** 0_B CCU80 CC82 is not available. 1_B CCU80 CC82 is available.
AVAIL3	3	r	**CCU80 CC83 Availability Flag** 0_B CCU80 CC83 is not available. 1_B CCU80 CC83 is available.
AVAIL12	12	r	**POSIF0 Availability Flag** 0_B POSIF0 is not available. 1_B POSIF0 is available.
AVAIL15	15	r	**DAC0 Availability Flag** 0_B DAC0 is not available. 1_B DAC0 is available.
AVAIL16	16	r	**CCU81 kernel SFRs and CC80 Availability Flag** 0_B CCU81 kernel SFRs and CC80 are not available. 1_B CCU81 kernel SFRs and CC80 are available.
AVAIL17	17	r	**CCU81 CC81 Availability Flag** 0_B CCU81 CC81 is not available. 1_B CCU81 CC81 is available.
AVAIL18	18	r	**CCU81 CC82 Availability Flag** 0_B CCU81 CC82 is not available. 1_B CCU81 CC82 is available.

(continued)

Field	Bits	Type	Description
AVAIL19	19	r	**CCU81 CC83 Availability Flag** 0_B CCU81 CC83 is not available. 1_B CCU81 CC83 is available.
AVAIL20	20	r	**MultiCAN Node 0 and Global SFRs Availability Flag** 0_B MultiCAN node 0 and Global SFRs are not available. 1_B MultiCAN node 0 and Global SFRs are available.
AVAIL21	21	r	**MultiCAN Node 1 Availability Flag** 0_B MultiCAN node 1 is not available. 1_B MultiCAN node 1 is available.
AVAIL23	23	r	**MultiCAN Message Object SFRs Availability Flag** 0_B MultiCAN message object SFRs are not available. 1_B MultiCAN message object SFRs are available.
AVAIL28	28	r	**POSIF1 Availability Flag** 0_B POSIF1 is not available. 1_B POSIF1 is available.
0	31:29, 27:24, 22, 14:13, 11:4	r	**Reserved**

11.8.3 Memory Size Registers

Memory size registers are available for the ROM, SRAM and Flash memories. They are used to indicate the available size of these memories in the device.

Note: The reset values of the size registers show the configuration of the superset device. Actual values might differ depending on the product variant.

11.8.3.1 Register ROMSIZE

ROMSIZE Address: 0400_H

ROM Size Register Reset Value: $0000\ 0B00_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

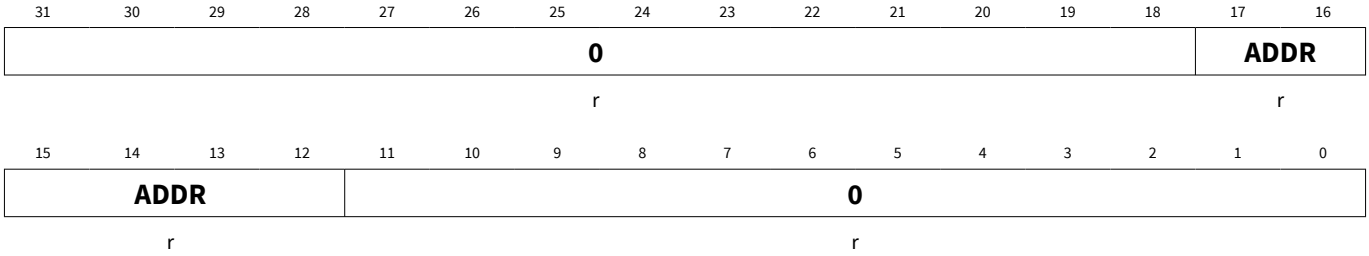
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		ADDR						0							
r		r						r							

Field	Bits	Type	Description
ADDR	13:8	r	**ROM Size** Size of user-readable ROM in bytes = ADDR * 256
0	31:14, 7:0	r	**Reserved**

11.8.3.2 Register FLSIZE

FLSIZE Address: 0404_H

Flash Size Register Reset Value: 000_H

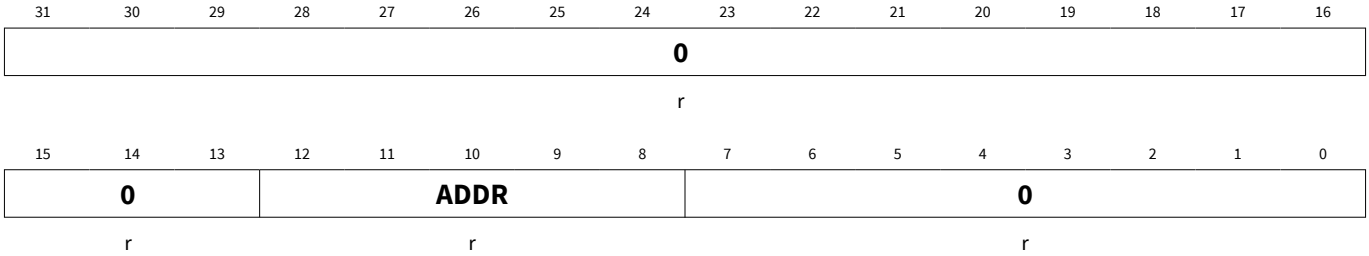


Field	Bits	Type	Description
ADDR	17:12	r	**Flash Size** Size of the Flash (excluding Flash sector 0) in Kbytes = (ADDR - 1) * 4
0	31:18, 11:0	r	**Reserved**

11.8.3.3 Register RAM0SIZE

RAM0SIZE Address: 0410_H

RAM0 Size Register Reset Value: $0000\ 1000_H$



Field	Bits	Type	Description
ADDR	12:8	r	**RAM0 Size** Size of RAM block 0 in bytes = ADDR * 256 For total RAM size, RAM blocks 1 to 3 have to be also taken into consideration.

(continued)

Field	Bits	Type	Description
0	31:13, 7:0	r	**Reserved**

12 Flash Architecture

This chapter describes the non volatile memory (NVM) module.

12.1 Overview

The IMC300A has an embedded user-programmable NVM for storage of user code and data.

12.1.1 Features

The NVM has the following features:

- Reading by word, writing by block (4 words) and erasing by page (256 bytes) or sector (4 Kbytes).
- Automatic verify support.
- Up to 50,000 erase cycles per page.
- Minimum data retention of 10 years in cells that were never previously programmed.
- Flash programming voltage generated on-chip.
- Configurable erase and write protection.
- Power saving sleep mode.
- Incremental write without erase for semaphores.

12.2 Definitions

Throughout the document the terms NVM (Non Volatile Memory) and Flash are used as synonyms, disregarding the fact that NVM describes a broader class of memories, where the described Flash is only a special case.

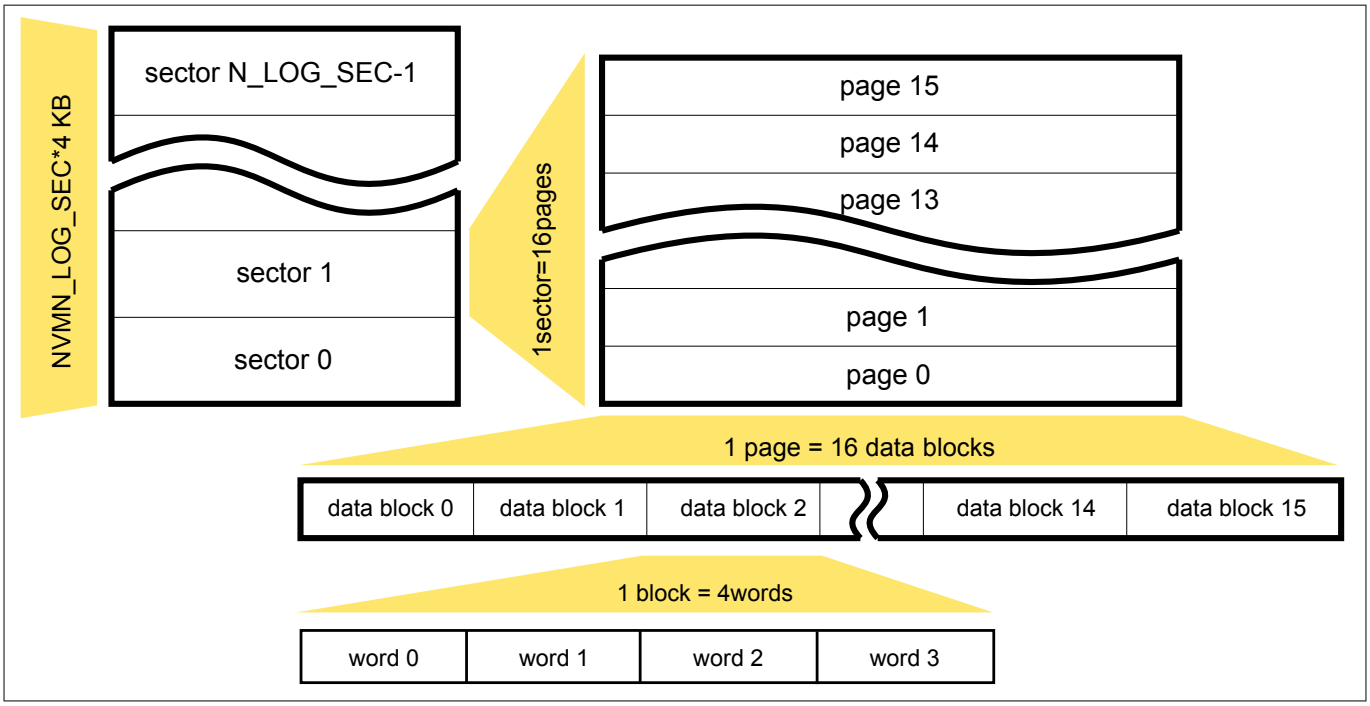


Figure 29 Logical structure of the NVM module

12.2.1 Logical and Physical States

Erasing

The erased state of a cell is ‘1’. Forcing an NVM cell to this state is called erasing. Erasing is possible with a granularity of a page (see below).

Writing

The written state of a cell is ‘0’. Changing an erased cell to this state is called writing. Writing is possible with a granularity of a block (see below).

Programming

The combination of erasing and writing is called programming. Programming often means also writing a previously erased page.

Note: The termini write and writing are also used for accessing special function registers. The meaning depends therefore on the context.

12.2.2 Data Portions

Word

A word consists of 32 bits. A word represents the data size which is read from or written to the NVM module within one access cycle.

Block

A block consists of 4 words (128 bit data, extended by 4 bit parity, and 6 bit ECC). A block represents the smallest data portion that can be written.

Page

A page consists of 16 blocks.

Sector

A sector consists of 16 pages.

12.2.3 Address Types

Physical Address

Address of the CPU system.

Base Address or Memory Base Address

Physical address of the lower boundary for memory accesses of an NVM module.

Logical Address

Memory address offset inside the NVM module: If the memory is addressed, the logical address is the physical address subtracted by the base address of the module.

Sector Address

Module specific part of the logical address specifying the sector, for calculation see ***Chapter 12.3.1***.

Page Address

Module specific part of the logical address, for calculation see ***Chapter 12.3.1***.

12.2.4 Module Specific Definitions

The following table defines NVM specific constants used throughout this chapter.

Table 160 Module Specific Definitions

Module size [KB]	128 + 4	
Constant name	**Value**	**Comment**
N_BLOCKS	16	Number of blocks per page
N_PAGES	16	Number of pages per sector
N_LOG_SEC	32 + 1	Number of sectors (RW + RO)

12.3 Module Components

12.3.1 Memory Cell Array

The non-volatile memory cells are organized in sectors, which consist of pages, which on their part are structured in blocks.

A logical memory address addr has the following structure:

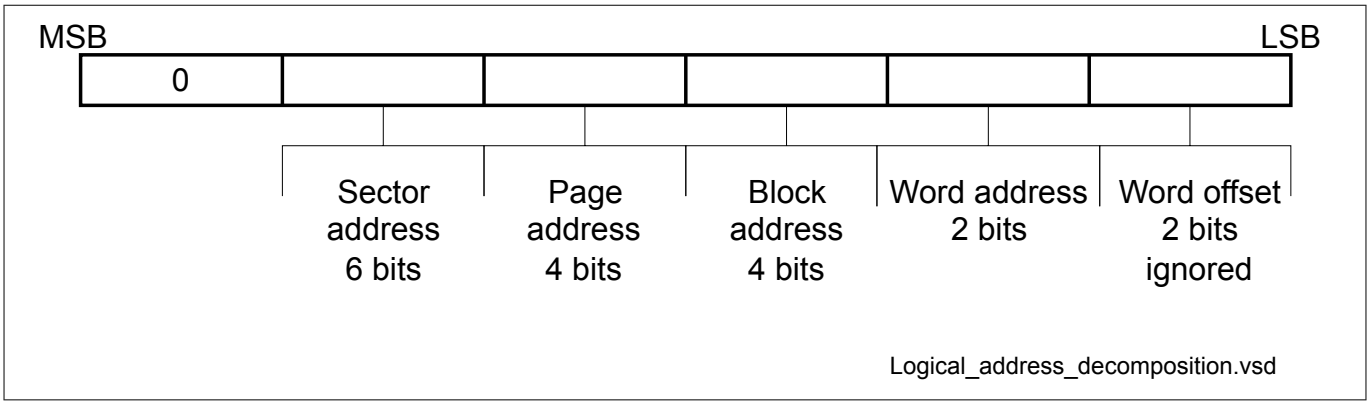


Figure 30 Decomposition of Logical Address

- addr[1:0] = word offset, for a memory address undefined and ignored
- addr[3:2] = word address
- addr[7:4] = block address
- addr[11:8] = page address
- addr[17:12] = sector address.

The memory subsystem always accesses whole words, therefore the word offset is ignored by the NVM module.

12.3.1.1 Page

Each page consists of 16 data blocks of 138 bits each (including parity bits and ECC bits).

A page is the granularity of data that can be erased in the cell array.

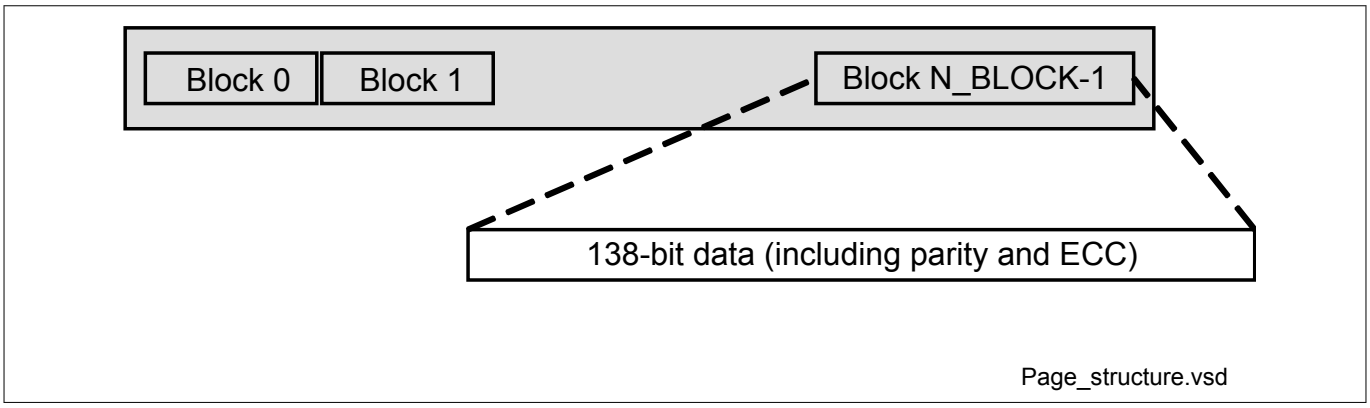


Figure 31 Structure of a Page

12.3.1.2 Sector

16 pages form a sector.

12.4 Functional Description

The NVM module supports read and write accesses to the memory and to the special function registers (SFRs). No read-modify-write mechanism is supported for SFRs.

The main tasks of the NVM module are reading and writing from/to the memory array.

12.4.1 SFR Accesses

Reading the special function registers is possible in every mode of the NVM module.

Register write is not possible while the state machine is busy. The write is stalled in this case. For other exceptions see ***Chapter 12.7.2.2***.

12.4.2 Memory Read

The NVM memory can be read with a minimum granularity of a word provided that the word is in the memory address range of the module.

If the word is not within the memory address range of the NVM module, the module does not react at all and a different memory module may handle the access.

Memory read accesses are only possible while no flash state machine (FSM) procedure (erase, write, verify, sleep or wake-up) is in progress. A memory read access while the FSM is busy is stalled until the FSM is idle again. Then the access is carried out. Such a stall will also stop the CPU from executing code.

The NVM will insert waitstates during memory read automatically if needed.

12.4.3 Memory Write

From the user's viewpoint data is written directly to the memory array. Module internally one block is buffered and the ECC bits are calculated. Then a finite state machine is started that writes the ECC and data bits to the memory field.

Writing does not support wrap-around, i.e. writing of a block has always to start with word 0 of the selected block and then automatically continues in ascending order up to word 3.

Since a block has to be written in four word writing steps, a special procedure has to be followed to transfer complete block data to the NVM: Writing of a block has always to start with word 0 of the addressed block. The following three writes need to address the other three words of the same block in ascending order. If this rule is

not observed, the already provided words are discarded. If in this case the last provided word is addressing a word 0, this word is already accepted as the first word of a new block write procedure. Intermediate read operations do not influence the write data transfer. Intermediate read operations targeting the same address as the interrupted write operation are served from the memory array, i.e. do not read back the already transferred write data.

To write to the memory array, the NVM module has to be set to one-shot or continuous write mode by setting the SFR ***NVMPROG*** to the corresponding value. Data to be written can now be written to the desired address. It is not checked, if the addressed block was erased before. Writing to a non erased block leads to corrupted data since writing can only clear bits but not set any bits. Reading such a block will lead most probably to an ECC fault.

A write access to the NVM when not in write mode does not trigger an exception or interrupt. The data is lost. Writes to the NVM are also used to trigger other operations which are described in the following subsections. Similarly, a write access to the NVM module has no effect and the data is lost when a protected sector is addressed (see ***Chapter 12.4.7***).

Depending on the settings of ***NVMPROG***, an automatic verify is performed (see ***Chapter 12.4.6***).

In case of a one-shot write, write mode is automatically left. In case of continuous write mode, further write operations to new addresses can follow, until the write mode is explicitly left. Continuous write operations can target blocks within the complete memory without any restriction regarding sector or page borders.

12.4.4 Memory Erase

Only whole pages can be physically erased, i.e. all bits of the addressed page are physically set to ‘1’.

To erase a page in the memory field, the NVM module has to be set to one-shot or continuous page erase mode by setting the SFR ***NVMPROG*** to the corresponding value. A write access to a memory location specifies the address of the page to be erased and triggers the erase.

A write access to the NVM when not in page erase mode does not trigger an exception or interrupt because they are also used to trigger other operations; as described in this section. Similarly, no erase is triggered when a protected sector is addressed (see ***Chapter 12.4.7***).

In case of a one-shot page erase, page erase mode is automatically left. In case of continuous page erase mode, further page erase operations can follow, until the page erase mode is explicitly left.

12.4.5 Sector Erase

Additionally, whole sectors consisting of 16 pages can be physically erased in parallel, i.e. all bits of the addressed sector are physically set to ‘1’.

To erase a sector in the memory array, the NVM module has to be set to one-shot or continuous sector erase mode by setting the SFR ***NVMPROG*** to the corresponding value. Writing arbitrary data to a memory location specifies the address of the sector to be erased.

A write access to the NVM when not in sector erase mode does not trigger an exception or interrupt because it is also used to trigger other operations; as described in this section. Similarly, no erase is triggered when a protected sector is addressed (see ***Chapter 12.4.7***).

In case of a one-shot sector erase, sector erase mode is automatically left. In case of continuous sector erase mode, further sector erase operations can follow, until the sector erase mode is explicitly left.

12.4.6 Verify

The data written as described in ***Chapter 12.4.3*** can be verified automatically. The written data in the cell array can be automatically compared to the data still available in the module internal buffer. This is automatically performed two times with hardread written and hardread erased. These hardread levels provide some margin

compared to the normal read level to ensure that the data is really programmed with suitably distinct levels for written and erased bits. The verification result can be read at SFR ***NVMSTATUS***.

Stand-alone verify operations can also be started by setting the SFR ***NVMPROG*** to the corresponding value. In this case, data written to a memory location is compared with the content of the memory field at the specified address. The comparison here is performed just once with a read level chosen before from normal read, hardread written and hardread erased.

A write access to the NVM when not in verification mode does not trigger an exception or interrupt because it is also used to trigger other operations; as described in this section. Similarly, a write access to the NVM module has no effect, when a protected sector is addressed (see ***Chapter 12.4.7***).

In case of a one-shot verify, verify mode is automatically left. In case of continuous verify mode, further verify operations can follow, until the verify mode is explicitly left.

Note: A continuous write operation without automatic verification, followed by two stand-alone verifications with 'hardread written' and 'hardread erased', is faster than a write operation with continuous automatic verification, since in the second case for every block write the hardread level has to be changed twice, whereas in the first case this change is performed only two times for the complete write data. On the other hand, for the continuous automatic verification the reference data for the verification is directly available within the NVM module, whereas for the stand-alone verification the reference data needs to be provided again by the CPU.

12.4.7 Erase-Protection and Write-Protection

By setting ***NVMCONF***.SECPROT, a configurable number of sectors can be selected to be protected from any modification, i.e. a range of sectors starting with sector 0 can be defined to be erase-protected and write-protected.

12.5 Properties and Implementation of Error Correcting Code (ECC)

The error correcting code (ECC) for the data blocks is a one-bit error correction and a (partial) double-bit error detection for every data block of 128 bit, which uses 4 parity bits and 6 ECC bits in addition to the protected 128 data bits. The correct ECC bits for every block are generated automatically when the data is written.

12.6 Service Request Generation

The NVM module supports immediate error and status information to the user by interrupt generation.

A NVM interrupt can be issued because of the following events:

- Completion of:
  - NVM operations started through NVMPROG.ACTION (except for verify-only sequence)
  - NVM wake-up sequence
- NVM ECC double-bit error

The NVM interrupt request is generated to the CPU through the SCU. Therefore, related interrupt control bits are located in the SCU but with the following exceptions:

- There are two sets of NVM ECC double-bit error status flag and clear status bit:
  - NVMSTATUS.ECC2READ and NVMPROG.RSTECC in NVM module
  - SCU_RAWSR.FLECC2I and SCU_SRCLR.FLECC2I in SCU module
- It is sufficient to use just one of the two sets and ignore the other.
- The interrupt enable bit for the NVM operation complete interrupt is located only in the NVMCONF register.

12.7 Power, Reset and Clock

The following sections describe the power, reset and clock sources of the NVM module.

12.7.1 Power Supply

The NVM module sources all voltages required for read, program and erase operations from the on-chip Embedded Voltage Regulator (EVR).

The standard V_{DDC} is used for all digital control functions.

12.7.2 Power Saving Modes

The NVM module supports the following power saving modes. The modes differ in power consumption and in the time to restart the memory.

12.7.2.1 NVM Idle Mode

Idle mode is entered after reset after charging the pumps. In idle mode the power consumption is less than during a memory read access or write access.

Any operation of the NVM module (SFR access or memory access) can be started from idle mode without time delay.

12.7.2.2 NVM Sleep Mode

Entering and leaving NVM sleep mode requires special state machine sequences, which need some time. Therefore, besides SFR accesses, the NVM module cannot be used immediately after wake-up from sleep mode, as indicated by ***NVMSTATUS***.BUSY.

NVM sleep mode is entered via WFE/WFI when Flash Power down is activated, see SCU chapter. Alternatively, sleep mode for the NVM module can be triggered by writing the respective bit in SFR ***NVMCONF***.

In NVM sleep mode only the SFR ***NVMCONF*** can be read and written, all other SFRs can only be read. No memory access is possible in sleep mode.

12.7.3 Reset

The NVM module is reset with the system reset.

12.7.4 Clock

The NVM module is operating at the same clock speed as main clock, MCLK.

12.8 Registers

Table 162 shows a complete list of the NVM special function registers.

Table 161 Registers Address Space

Module	Base Address	End Address	Note
NVM	$4005\ 0000_H$	$4005\ 00FF_H$	

Table 162 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
NVMSTATUS	NVM Status Register	0000_H	Page ***219***
NVMPROG	NVM Programming Control Register	0004_H	Page ***220***
NVMCONF	NVM Configuration Register	0008_H	Page ***223***

Registers Access

The registers are addressed wordwise

Reading an SFR is not blocked, while the NVM module is busy. If the SFR value depends on the completion of an NVM sequence, ***NVMSTATUS***.BUSY must be polled for 0_B, before the SFR is read. Otherwise, reading the SFR might yield a value that is not updated yet.

12.8.1 NVM Register

12.8.1.1 Register NVMSTATUS

NVMSTATUS Address: 0000_H

NVM Status Register Reset Value: 0002_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0									**WRPERR**	**ECC2READ**	**ECC1READ**	**VERR**		**SLEEP**	**BUSY**
r									r	r	r	r		r	r

Field	Bits	Type	Description
0	15:7	r	**Reserved** Read as 0.
WRPERR	6	r	**Write Protocol Error** The flag accumulates write protocol violations during the last 4-word write operations (for write or verify). It is also set when a triggered operation was ignored because of write protection. The correct protocol is defined in ***Chapter 12.4.3***. It is reset by hardware when ***NVMPROG***.RSTECC is written. 0_B WRPROTOK, No write protocol failure occurred. 1_B WRPROTFAIL, At least one write protocol failure was detected.
ECC2READ	5	r	**ECC2 Read**[19)] The flag accumulates ECC two bit failure during memory read operations. It is reset by hardware when ***NVMPROG***.RSTECC is written. 0_B ECC2RDOK, No ECC two bit failure during memory read operations. 1_B ECC2RDFAIL, At least one ECC two bit failure was detected.

(continued)

Field	Bits	Type	Description
ECC1READ	4	r	**ECC1 Read**[19)] The flag accumulates ECC single bit failure during the last memory read operations. It is reset by hardware when ***NVMPROG***.RSTECC is written. 0_B ECC1RDOK, No ECC single bit failure occurred. 1_B ECC1RDFAIL, At least one ECC single bit failure was detected and corrected.
VERR	3:2	r	**Verify Error** The flag is reset by hardware, when ***NVMPROG***.RSTVERR is written. The flag is also reset, when write mode or verify-only mode are entered, i.e. ***NVMPROG***.ACTION.OPTYPE = 0001_B or ***NVMPROG***.ACTION.VERIFY = 11_B. The flag accumulates, i.e. VERR is updated every time a value higher than the current value is required, until write mode or verify-only mode are left (automatically in case of a one-shot write operation). Information on number of fail bits during verify procedure(s): 00_B NOFAIL, No fail bit. 01_B ONEFAIL, One fail bit in one data block. 10_B TWOFAIL, Two fail bits in two different data blocks. 11_B MOREFAIL, Two or more fail bits in one data block, or three or more fail bits overall.
SLEEP	1	r	**Sleep Mode** 0_B READY, NVM not in sleep mode, and no sleep or wake up procedure in progress. 1_B SLEEP, NVM in sleep mode, or busy due to a sleep or wake up procedure.
BUSY	0	r	**Busy** 0_B READY, The NVM is not busy. Memory reads from the cell array and register write accesses are possible. 1_B BUSY, The NVM is busy. Memory reads and register write accesses are not possible.

12.8.1.2 Register NVMPROG

NVMPROG Address: 0004_H

NVM Programming Control Register Reset Value: 0000_H

19 If a block is read from the field that contains two or more parity errors ECC1 and ECC2 errors may be flagged simultaneously.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		**RSTECC**	**RSTVERR**	**0**				**ACTION**							
r		rw	rw	r				rw							

Field	Bits	Type	Description
0	15:14	r	**Reserved** Read as 0; should by written with 0.
RSTECC	13	rw	**Reset ECC** Can only be set by software, is reset automatically by hardware. 0_B NOP, No action. 1_B RESET, Reset of ***NVMSTATUS***.ECCxREAD and NVMSTATUS.WRPERR.
RSTVERR	12	rw	**Reset Verify Error** Can only be set by software, is reset automatically by hardware. 0_B NOP, No action. 1_B RESET, Reset of ***NVMSTATUS***.VERR.
0	11:8	r	**Reserved** Read as 0; should be written with 0.

(continued)

Field	Bits	Type	Description
ACTION	7:0	rw	**ACTION: [VERIFY, ONE_SHOT, OPTYPE]** This field selects an erase, write, or verify operation. See also ***More details on ACTION***. ACTION is a concatenation of three bit fields: ACTION[7:6] = VERIFY, ACTION[5:4] = ONE_SHOT and ACTION[3:0] = OPTYPE. OPTYPE defines the following operations: 0000_B: idle or verify-only, that depends on the setting of VERIFY; 0001_B: write; 0010_B: page erase. 0100_B: sector erase. ONE_SHOT is a parameter of OPTYPE with the following values: 01_B: once or 10_B: continuously. In case of 01_B, ACTION is automatically reset to idle mode after operation has been performed. VERIFY defines a second parameter of OPTYPE: 01_B: verification of written data with hardread levels after every write operation, 10_B: no verification, 11_B: verification of array content. The following operations are defined, other values are interpreted as 00_H 00_H Idle state, no action triggered. Writing 00_H exits current mode. 51_H Start one-shot write operation with automatic verify. 91_H Start one-shot write operation without verify. 61_H Start continuous write operation with automatic verify of every write. $A1_H$ Start continuous write operation without verify. 92_H Start one-shot page erase operation. 94_H Start one-shot sector erase operation. $A4_H$ Start continuous sector erase operation. $A2_H$ Start continuous page erase operation. $D0_H$ Start one-shot verify-only: Written data is compared to array content. $E0_H$ Start continuous verify-only: Written data is compared to array content.

More details on ACTION

The operation selected by ACTION is performed, when a write to the NVM address range is performed, which defines the address (and block data) for the operation. Afterwards, in case of a one-shot operation, ACTION is automatically reset.

Verification results can be read at ***NVMSTATUS***.VERR.

ACTION can only be changed when the current value of ACTION is 00_H, otherwise ACTION is set to 00_H. Once ACTION is not idle, ACTION can only be written again with its current value; any other value leads to a reset of ACTION.

Only write operations can be automatically verified. Page erase operations cannot use automatic verify, they must be started with ACTION.VERIFY = 10_B.

If the correct erasing of a page or sector is to be verified, a separate sequence using ACTION.VERIFY = 11_B has to be started.

A verify operation requires the provision of the data for a complete block and always includes the ECC bits. The ECC bits for every block are generated automatically when the data is written.

A verify operation started with ACTION.VERIFY = 01_B is automatically performed with both hardread written and hardread erased levels.

A verify operation started with ACTION.VERIFY = 11_B is performed with the single hardread level defined by ***NVMCONF***.HRLEV at this starting time.

A sequence started by setting ACTION will set ***NVMSTATUS***.BUSY only after the transfer of the address (and block data) is performed. The end of the sequence can be detected either by polling NVMSTATUS.BUSY or by waiting for an NVM interrupt (not for verify-only sequence).

Entering sleep mode resets ACTION.

NVM Configuration Register

NVMCONF is the only SFR that can be written while the module is in sleep mode. This is necessary to enable the use of NVM_ON = 0_B to go to sleep mode and of NVM_ON = 1_B to wake-up again.

12.8.1.3 Register NVMCONF

NVMCONF Address: 0008_H

NVM Configuration Register Reset Value: 9000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NVM_ON	**INT_ON**	**0**	**1**	**SECPROT**								**0**	**HRLEV**		**0**
rw	rw	rw	rw	rw								r	rw		rw

Field	Bits	Type	Description
NVM_ON	15	rw	**NVM On** When cleared, no software code can be executed anymore from the NVM, until it is set again. I.e., already the software code that initiates the change in NVM_ON itself may not reside in the NVM, otherwise the software is stalled forever. 0_B SLEEP, NVM is switched to or stays in sleep mode. 1_B NORM, NVM is switched to or stays in normal mode.
INT_ON	14	rw	**Interrupt On** When enabled the completion of a sequence started by setting ***NVMPROG***.ACTION (write or erase sequence) will be indicated by NVM interrupt. The same is true for the wake-up sequence. 0_B INTOFF, No NVM ready interrupts are generated. 1_B INTON, NVM ready interrupts are generated.
0	13	rw	**Reserved for Future Use** Must be written with 0 to allow correct operation.
1	12	rw	**Reserved for Future Use** Must be written with 1 to allow correct operation.

(continued)

Field	Bits	Type	Description
SECPROT	11:4	rw	**Sector Protection**[20] This field defines the number of write, erase, verify protected sectors, starting with physical sector 0.
0	3	r	**Reserved** Read as 0; should be written with 0.
HRLEV	2:1	rw	**Hardread Level**[21] Defines single hardread level for verification with ***NVMPROG***.ACTION.VERIFY = 11_B: 00_B NR, Normal read 01_B HRW, Hardread written 10_B HRE, Hardread erased 11_B RFU, Reserved for Future Use
0	0	rw	**Reserved for Future Use** Must be written with 0 to allow correct operation.

12.9 Example Sequences

This section presents some low-level programming examples.

In all following operations the protection defined by ***NVMCONF***.SECPROT needs to be taken into account.

12.9.1 Writing to Memory

12.9.1.1 Writing a Single Block

This sequence requires that the target block is already erased.

Additional assumption: ***NVMPROG***.ACTION = 00_H.

1. Start a one-shot write operation: Write ***NVMPROG***.ACTION = 51_H or 91_H, respectively, if an automatic verification of the written data is to be performed or not.
2. Write data for one block to the physical address.
3. Poll flag ***NVMSTATUS***.BUSY until write sequence has finished, or wait for NVMready interrupt (if enabled).
4. If an automatic verification of the written data was requested in the first step, read ***NVMSTATUS***.VERR for the verification result.

If no verification of the written data was requested in step 1, and thus no read access to the NVM SFR is required in step 4, step 3 may be omitted.

The next access to the NVM module or the next write access to an NVM SFR (which ever comes first) will be automatically stalled, until the operation started in step 2 is finished.

20 For SECPROT > 0, SECPROT defines the number of protected sectors. The sectors 0 to SECPROT-1 cannot be written, erased, or verified. All writes that target the protected sectors are accepted, but are internally ignored.

21 HRLEV defines the hardread level for a stand-alone verification sequence started with NVMPROG.ACTION.VERIFY = 11_B. This hardread level is used until the end of the verification sequence. HRLEV may not be changed in between.

12.9.1.2 Writing Blocks

This sequence requires the target blocks are already erased.

Additional assumption: ***NVMPROG***.ACTION = 00_H.

1. Start a continuous write operation: Write ***NVMPROG***.ACTION = 61_H or $A1_H$, respectively, if an automatic verification of the written data is to be performed or not.
2. Write data for one block to the physical address.
3. Poll flag ***NVMSTATUS***.BUSY until write sequence has finished, or wait for NVMready interrupt (if enabled). Optionally, step 3 may be omitted: The next access to the NVM module or the next write access to an NVM SFR (which ever comes first) will be automatically stalled, until the operation started in step 2 is finished.
4. Jump to step 2 unless all data is written.
5. Stop continuous write operation: Write ***NVMPROG***.ACTION = 00_H.
6. If an automatic verification of the written data was requested in the first step, read ***NVMSTATUS***.VERR for the verification result.

12.9.2 Erasing Memory

12.9.2.1 Erasing a Single Page

Assumption: ***NVMPROG***.ACTION = 00_H.

1. Start a one-shot page erase operation: Write ***NVMPROG***.ACTION = 92_H.
2. Write dummy data for one word to one arbitrary word-aligned physical address of the page to be erased.
3. Poll flag ***NVMSTATUS***.BUSY until page erase sequence has finished, or wait for NVMready interrupt (if enabled).

Optionally, step 3 may be omitted: The next access to the NVM module or the next write access to an NVM SFR (which ever comes first) will be automatically stalled, until the operation started in step 2 is finished.

12.9.2.2 Erasing Pages

Assumption: ***NVMPROG***.ACTION = 00_H.

1. Start a continuous page erase operation: Write ***NVMPROG***.ACTION = $A2_H$.
2. Write dummy data for one word to one arbitrary word-aligned physical address of the page to be erased.
3. Poll flag ***NVMSTATUS***.BUSY until page erase sequence has finished, or wait for NVMready interrupt (if enabled). Optionally, step 3 may be omitted: The next access to the NVM module or the next write access to an NVM SFR (which ever comes first) will be automatically stalled, until the operation started in step 2 is finished.
4. Jump to step 2 unless all pages are erased.
5. Stop continuous page erase operation: Write ***NVMPROG***.ACTION = 00_H.

12.9.2.3 Erasing a Single Sector

Assumption: ***NVMPROG***.ACTION = 00_H.

1. Start a one-shot sector erase operation: Write ***NVMPROG***.ACTION = 94_H.
2. Write dummy data for one word to one arbitrary word-aligned physical address of the sector to be erased.
3. Poll flag ***NVMSTATUS***.BUSY until sector erase sequence has finished, or wait for NVMready interrupt (if enabled). Optionally, step 3 may be omitted: The next access to the NVM module or the next write access to an NVM SFR (which ever comes first) will be automatically stalled, until the operation started in step 2 is finished.

12.9.2.4 Erasing Sectors

Assumption: ***NVMPROG***.ACTION = 00_H.

1. Start a continuous sector erase operation: Write ***NVMPROG***.ACTION = $A4_H$.
2. Write dummy data for one word to one arbitrary word-aligned physical address of the sector to be erased.
3. Poll flag ***NVMSTATUS***.BUSY until sector erase sequence has finished, or wait for NVMready interrupt (if enabled). Optionally, step 3 may be omitted: The next access to the NVM module or the next write access to an NVM SFR (which ever comes first) will be automatically stalled, until the operation started in step 2 is finished.
4. Jump to step 2 unless all sectors are erased.
5. Stop continuous sector erase operation: Write ***NVMPROG***.ACTION = 00_H.

12.9.3 Verifying Memory

12.9.3.1 Verifying a Single Block

Assumption: ***NVMPROG***.ACTION = 00_H.

1. Choose desired hardread level by setting NVMCONF.HRLEV.
2. Start a one-shot verify operation: Write ***NVMPROG***.ACTION = $D0_H$.
3. Write reference data for one block to the physical address.
4. Poll flag ***NVMSTATUS***.BUSY until verify sequence has finished.
5. Read ***NVMSTATUS***.VERR for the verification result.

12.9.3.2 Verifying Blocks

Assumption: ***NVMPROG***.ACTION = 00_H.

1. Choose desired hardread level by setting NVMCONF.HRLEV.
2. Start a continuous verify operation: Write ***NVMPROG***.ACTION = $E0_H$.
3. Write reference data for one block to the physical address.
4. Poll flag ***NVMSTATUS***.BUSY until verify sequence has finished. Optionally, step 4 may be omitted: The next access to the NVM module or the next write access to an NVM SFR (which ever comes first) will be automatically stalled, until the operation started in step 3 is finished.
5. Jump to step 3 unless all blocks are verified.
6. Stop continuous verify operation: Write ***NVMPROG***.ACTION = 00_H.
7. Read ***NVMSTATUS***.VERR for the verification result.

12.9.4 Writing to an Already Written Block

Normally, writing additional bits in an already written block is not feasible, since the already written ECC bits and the parity bits would need an update, too, which in most cases would require to erase some bits, which is not possible. The result would be an ECC-faulty block.

For special purposes a repeated update of specially constructed data is possible, e.g. to store some marker bits for use in a power loss recovery SW implementation.

Starting with an erased block, and making use of the special structure of the ECC, it is possible to repeatedly add two newly written bits in identical bit positions to two arbitrary words of the block. This principle is shown in the exemplary writing scheme of ***Table 163***, where a block is updated 32 times without corruption of the ECC, i.e. the data stays ECC protected throughout the procedure.

Table 163 Incremental Update of a Block with Specially Constructed Data

Operation	Block Write Data	Resulting Block Content[22]
Erase block		FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF
Add 1st value	FFFFFFFF FFFFFFFC FFFFFFFF FFFFFFFC	FFFFFFFF FFFFFFFC FFFFFFFF FFFFFFFC
Add 2nd value	FFFFFFFF FFFFFFF3 FFFFFFFF FFFFFFF3	FFFFFFFF FFFFFFF0 FFFFFFFF FFFFFFF0
Add 3rd value	FFFFFFFF FFFFFFCF FFFFFFFF FFFFFFCF	FFFFFFFF FFFFFFC0 FFFFFFFF FFFFFFC0
Add 4th value	FFFFFFFF FFFFF3F FFFFFFFF FFFFF3F	FFFFFFFF FFFFF00 FFFFFFFF FFFFF00
Add 5th value	FFFFFFFF FFFFCFF FFFFFFFF FFFFCFF	FFFFFFFF FFFFC00 FFFFFFFF FFFFC00
Add 6th value	FFFFFFFF FFFF3FF FFFFFFFF FFFF3FF	FFFFFFFF FFFF000 FFFFFFFF FFFF000
...	...	...
15th value	FFFFFFFF CFFFFFFF FFFFFFFF CFFFFFFF	FFFFFFFF C0000000 FFFFFFFF C0000000
16th value	FFFFFFFF 3FFFFFFF FFFFFFFF 3FFFFFFF	FFFFFFFF 00000000 FFFFFFFF 00000000
17th value	FFFFFFFC FFFFFFFF FFFFFFFC FFFFFFFF	FFFFFFFC 00000000 FFFFFFFC 00000000
...	...	...
30th value	F3FFFFFF FFFFFFFF F3FFFFFF FFFFFFFF	F0000000 00000000 F0000000 00000000
31st value	CFFFFFFF FFFFFFFF CFFFFFFF FFFFFFFF	C0000000 00000000 C0000000 00000000
32nd value	3FFFFFFF FFFFFFFF 3FFFFFFF FFFFFFFF	00000000 00000000 00000000 00000000
Add to invalidate written values[23]	FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFE	Same as before, but ECC2-faulty

Other combinations of write values are possible, too, as long as the basic “add two identical bits in each of two words” is adhered to. In ***Table 163*** it is also shown that an invalidation of the data by deliberately creating an ECC2 error is possible.

To minimize the write times and also to minimize the cycle load of the block, it is important to only write the new bits of the block as shown in ***Table 163***. In principle it is possible to repeatedly write also the already written bits again, but this would unnecessarily increase the writing times and would also increase the cycle load.

12.9.5 Sleep Mode

Assumption: Active mode (***NVMSTATUS***.SLEEP = 0_B) and ***NVMSTATUS***.BUSY = 0_B.

To Enter Sleep Mode

1. Execute WFE/WFI or ***NVMCONF***.NVM_ON = 0_B.

22 ECC-clean and parity-clean (ECC bits and parity bits all stay erased), except where indicated otherwise.
23 This write data can be written on any of the states above (except the completely erased state), always resulting in an unchanged data content, but now with an ECC2 error (three ECC bits and one parity bit are written).

2. NVMSTATUS.BUSY = 1_B and NVMSTATUS.SLEEP = 1_B until sleep mode is reached.
3. NVMSTATUS.BUSY = 0_B and NVMSTATUS.SLEEP = 1_B while in sleep mode.

To Wake-up from Sleep Mode

1. Any wake-up event and NVMCONF.NVM_ON = 1_B.
2. NVMSTATUS.BUSY = 1_B and NVMSTATUS.SLEEP = 1_B until active mode is reached.
3. Poll flag ***NVMSTATUS***.BUSY until wake-up sequence has finished, or wait for NVMready interrupt (if enabled).
4. NVMSTATUS.BUSY = 0_B and NVMSTATUS.SLEEP = 0_B while in active mode.

A wake-up event while the goto sleep sequence has not finished yet, does not shorten this sequence, but only directly starts the wake-up sequence afterwards.

12.9.6 Timing

This state diagram shows the transitions and timings of all possible sequences.

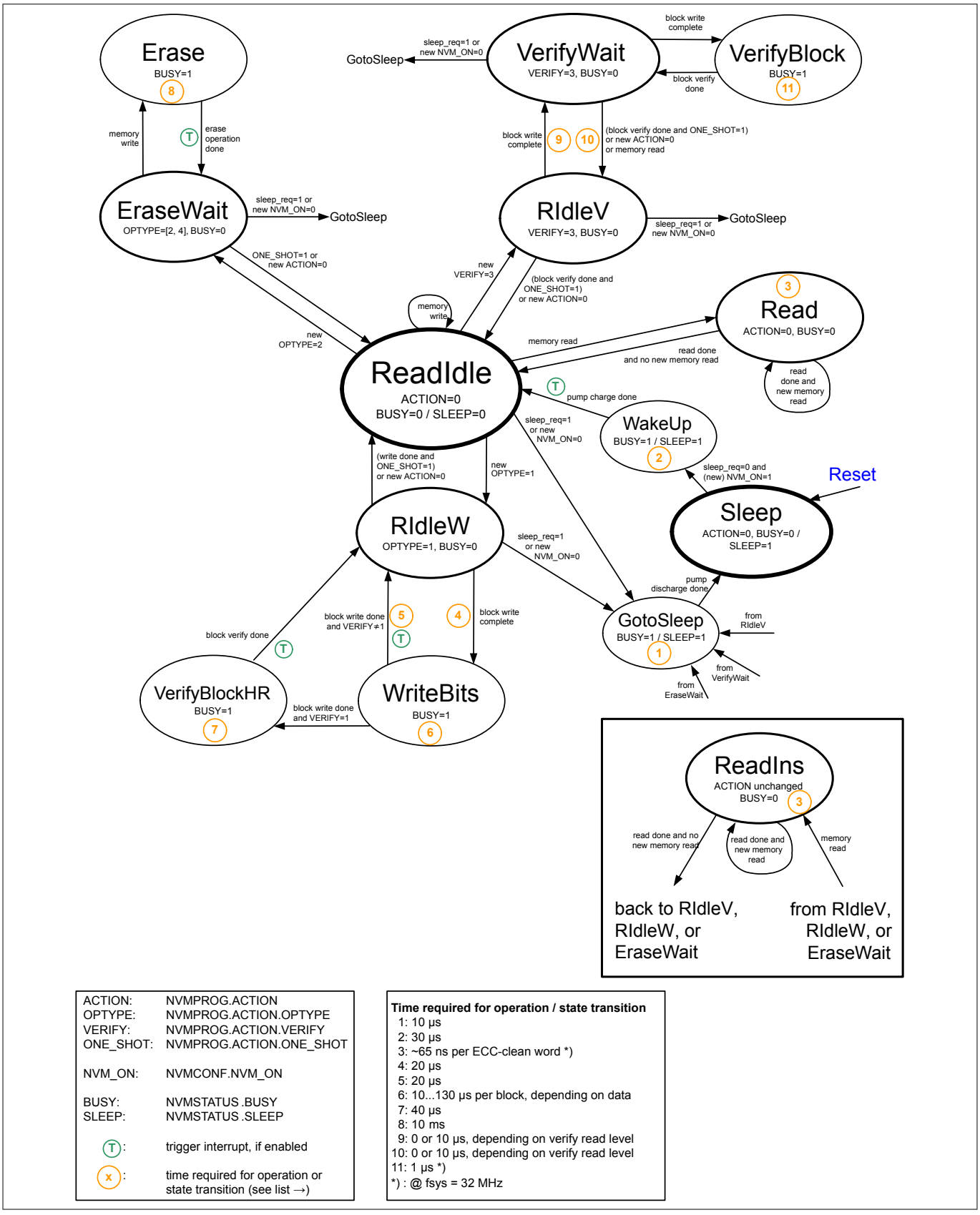


Figure 32 State Diagram of the NVM Module Timings are preliminary

13 Prefetch Unit (PFU)

The purpose of the Prefetch unit is to reduce the Flash latency gap at higher system frequencies to increase the instruction per cycle performance.

13.1 Overview

The PFU consists mainly of:

- A 1-word prefetch buffer to store the prefetched Flash contents.
- A prefetch controller, which triggers a prefetch to the Flash if necessary and determines if the contents of the prefetch buffer can be used for a CPU instruction fetch.

13.1.1 Block Diagram

Figure 33 shows the block diagram of the PFU.

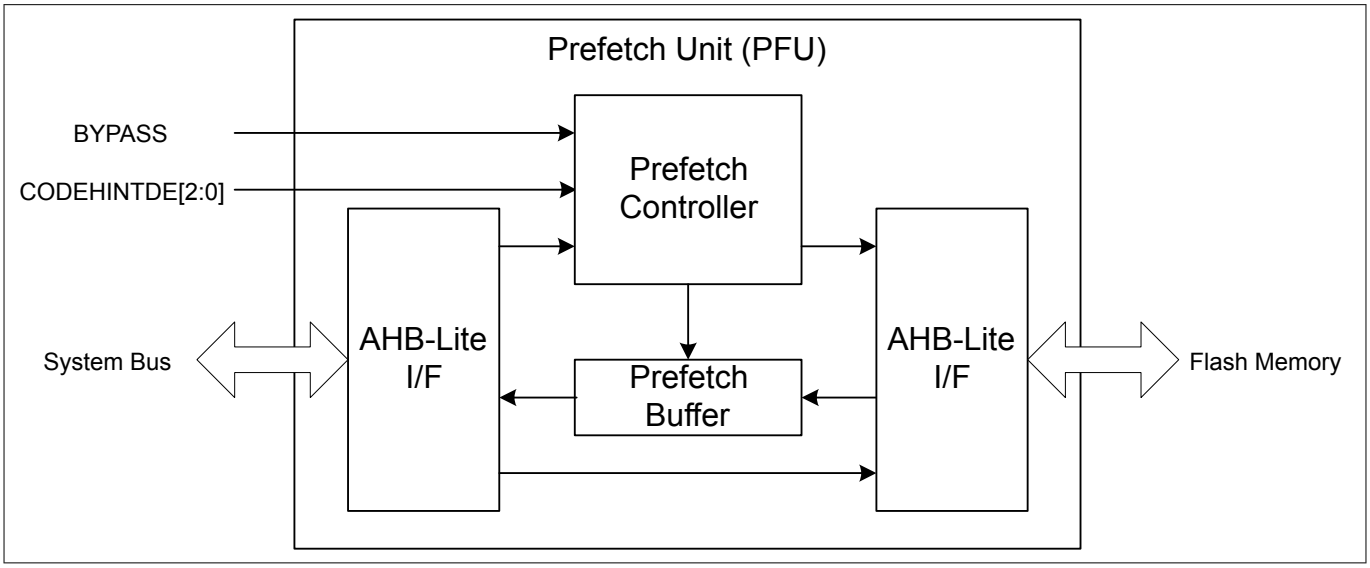


Figure 33 PFU Block Diagram

13.2 Operation Mode

The PFU is by default bypassed after a reset. The bit PFUBYP in SCU register PFUCR controls the bypass:

- Setting PFUBYP to 1 bypasses the PFU.
- Clearing PFUBYP to 0 removes the bypass and enables the PFU.

When the PFU is enabled, at the end of every instruction fetch by the CPU on the Flash, the PFU determines if a prefetch of the next address should be started based on the information from the CPU.

If yes, a read access to the next Flash address is immediately started, and the read data will be stored in the prefetch buffer when it becomes available.

Prefetch buffer hits are without any penalty i.e. single cycle access rate. This ensures a minimized latency.

Note: It is recommended to enable the PFU only when an application code consists of predominantly linear code. Otherwise, the performance penalty due to the execution of branch instructions may outweigh the performance gain of linear code execution.

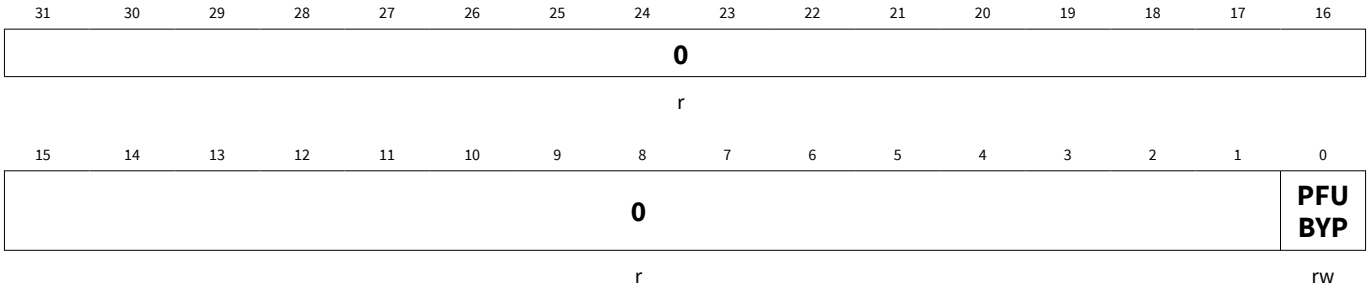
13.2.1 PFU Control Register

The PFU control register, PFUCR, is used to enable or disable the bypass to the PFU. This register is located in the SCU and is also described in the SCU chapter.

13.2.1.1 Register SCU_PFUCR

SCU_PFUCR Address: $4001\ 0068_H$

PFU Control Register Reset Value: $0000\ 0001_H$



Field	Bits	Type	Description
PFUBYP	0	rw	**Prefetch Unit Bypass** 0_B PFU is not bypassed. 1_B PFU is bypassed.
0	31:1	r	**Reserved** Should be written with 0.

14 System Control Unit (SCU)

The SCU is the SoC power, reset and a clock manager with additional responsibility of providing system stability protection and other auxiliary functions.

14.1 Overview

The functionality of the SCU described in this chapter is organized in the following sub-chapters, representing different aspects of system control:

- Miscellaneous control functions, GCU ***Chapter 14.2***
- Power control, PCU ***Chapter 14.3***
- Reset operation, RCU ***Chapter 14.4***
- Clock Control, CCU ***Chapter 14.5***

14.1.1 Features

The following features are provided for monitoring and controlling the system:

- General Control
  - Start-up Software (SSW) and Boot Mode Support
  - Memory Content Protection
  - Interrupt Handling
- Power control
  - On-chip core supply generation via EVR
  - Power Validation
  - Supply Watchdog
  - Voltage Monitoring
  - Load Change Handling
- Reset Control
  - Reset assertion on various reset request sources
  - System Reset Generation
  - Inspection of reset sources after reset
- Clock Control
  - Clock Generation
  - Clock Supervision
  - Individual Peripheral Clock Gating
  - Clock Blanking Support
  - On-chip Oscillator Calibration
  - External Oscillator Controls

14.1.2 Block Diagram

Figure 34 shows the following sub-units:

- Power Control Unit (PCU)
- Reset Control Unit (RCU)
- Clock Control Unit (CCU)
- General Control Unit (GCU)

All the SFRs in SCU module are accessible via the AHB and the 16-bit APB bus interface as shown in ***Figure 34***.The APB bus interface is used to access the group of SFR called ANACTRL register. These registers are used to configure the analog modules in the system, namely, the embedded voltage regulator (EVR) and the digitally controlled oscillators (DCO1 and DCO2). The other group of SFR called SCU register are accesible via the AHB bus interface.

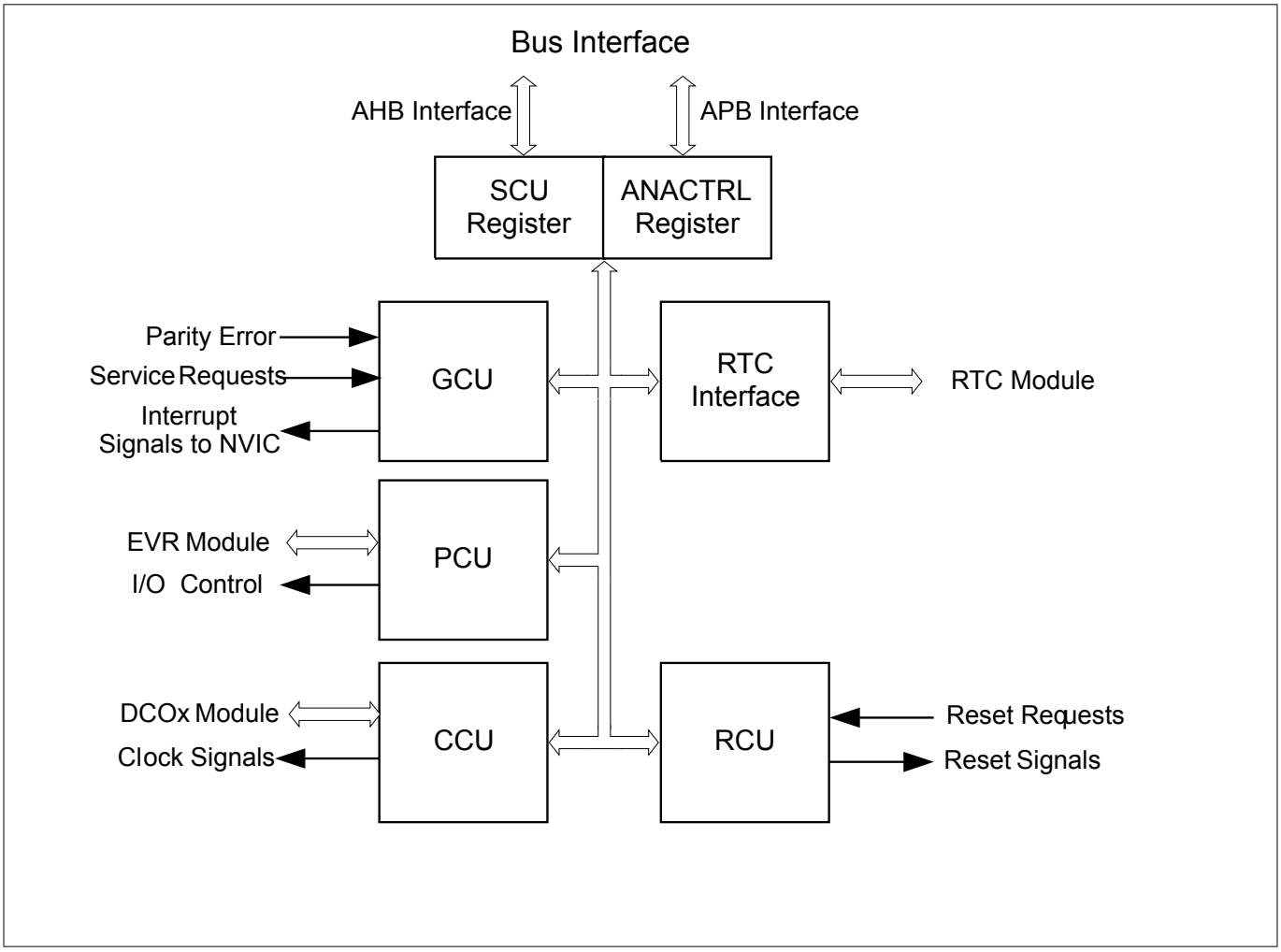


Figure 34 SCU Block Diagram

Interface of General Control Unit

The General Control Unit GCU has a memory fault interface to the memory validation logic of each on-chip SRAM and the Flash to receive memory fault events, as parity errors.

Interface of Power Control Unit

The Power Control Unit PCU has an interface to the Embedded Voltage Regulator (EVR) and an interface to the CCU module. The PCU related signals are described in more detail in ***Chapter 14.3***.

Interface of Reset Control Unit

The Reset Control Unit RCU has an interface to the Embedded Voltage Regulator (EVR). The RCU receives the power-on reset and the brownout reset information from the EVR. Reset requests are coming to the unit from the watchdog, the CPU, the GCU and the clock control unit (CCU). The RCU is providing the reset signals to all other units of the chip in the core power domain. The RCU related signals are described in more detail in ***Chapter 14.4***.

Interface of Clock Control Unit

The Clock Control Unit (CCU) receives the clock source from the on-chip Digitally Controlled Oscillator (DCO). The CCU provides the clock signals to all other units of the chip.

Interface of RTC

Access to the RTC module is served over a serial interface. The interface provides mirror registers updated via the serial interface to the RTC module registers. Update of the mirror registers over the serial is controlled using ***MIRRSTS*** registers. End of update can also trigger service requests via ***SRRAW*** register. Refresh of the registers in the register mirror are performed continuously, as fast as possible in order to instantly reflect any register state change on both sides.

The RTC module functionality is described in separate RTC chapter.

14.2 Miscellaneous Control Functions (GCU)

System Control implements system management functions accessible via GCU registers. General system control including various auxillary function is performed in the General Control Unit (GCU).

14.2.1 Service Requests Handling

Service request events listed in ***Table 164*** can result in assertion of an interrupt. Please refer to ***SRMSK***/ ***SRMSK1*** register description.

The interrupt structure is shown in ***Figure 35***. The interrupt request or the corresponding interrupt set bit (in register ***SRSET***/***SRSET1***) can trigger the interrupt generation at the selected interrupt node x. The service request pulse is generated independently from the interrupt flag in register ***SRRAW***/***SRRAW1***. The interrupt flag can be cleared by software by writing to the corresponding bit in register ***SRCLR***/***SRCLR1***.

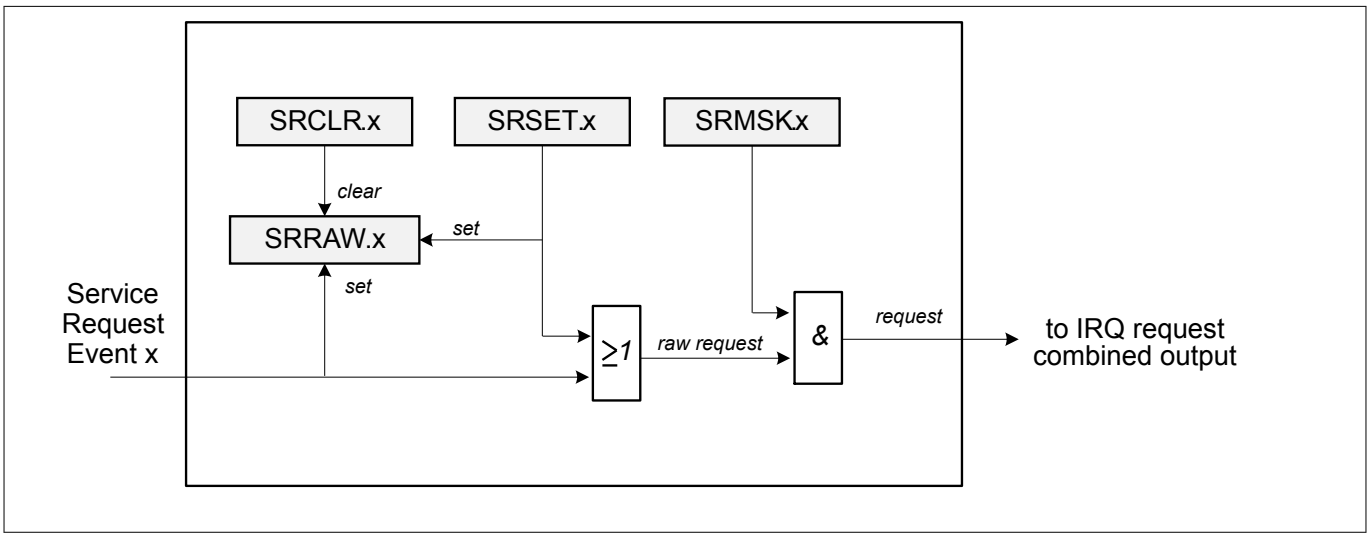


Figure 35 Service Request Handling

The flag in register ***SRRAW***/***SRRAW1*** can be cleared by software by writing to the corresponding bit in register ***SRCLR***/***SRCLR1***. All trap requests are combined to one common line and connected to a regular interrupt node of NVIC.

Note: When servicing an SCU service request, make sure that all related request flags are cleared after the identified request has been handled.

14.2.1.1 Service Request Sources

The SCU supports service request sources listed in ***Table 164*** and reflected in the ***SRRAW***/***SRRAW1***, ***SRMSK***/***SRMSK1***, ***SRCLR***/***SRCLR1*** and ***SRSET***/***SRSET1*** registers. The events that trigger these service requests are described in the respective module chapters or in the various sections within SCU.

Table 164 Service Requests

Modules	Service Request Name	Service Request Short Name	SCU.SRx
NVM	Flash Double Bit ECC Event	FLECC2I	SR0
	Flash Operation Complete Event	FLCMPLTI	SR0
RAM	16kbytes SRAM Parity Error Event	PESRAMI	SR0
USIC0	USIC0 SRAM Parity Error Event	PEU0I	SR0
USIC1	USIC1 SRAM Parity Error Event	PEU1I	SR0
MultiCAN	MultiCAN SRAM Parity Error Event	PEMCI	SR0
SCU:CCU	Loss of DCO1 Clock Event	LOCI	SR0
	Loss of External OSC_HP Clock Event	LOECI	SR0
	Standby Clock Failure Event	SBYCLKFI	SR1
	DCO1 out of syncronisation Event	DCO1OFSI	SR1
SCU:PCU	VDDP Pre-warning Event	VDDPI	SR1
	VDROP Event	VDROPI	SR1
	VCLIP Event	VCLIPI	SR1
SCU:GCU	Temperature Sensor Done Event	TSE_DONE	SR1
	Temperature Sensor Compare High Event	TSE_HIGH	SR1
	Temperature Sensor Compare Low Event	TSE_LOW	SR1
WDT	WDT pre-warning	PRWARN	SR1
RTC	RTC Periodic Event	PI	SR1
	RTC Alarm	AI	SR1
	RTC CTR Mirror Register Updated	RTC_CTR	SR1
	RTC ATIM0 Mirror Register Updated	RTC_ATIM0	SR1
	RTC ATIM1 Mirror Register Updated	RTC_ATIM1	SR1
	RTC TIM0 Mirror Register Updated	RTC_TIM0	SR1
	RTC TIM1 Mirror Register Updated	RTC_TIM1	SR1
ORC	Out of Range Comparator Event	ORCxI [x = 0,4,6,7]	SR2
ACMP	Analog Comparator Event	ACMPxI [x = 1 and 2]	SR2

14.2.2 SRAM Memory Content Protection

For supervising the content of the on-chip SRAM memories, the following mechanism is provided:

All on-chip SRAMs provide protection of content via parity checking. The parity logic generates additional parity bits which are stored along with each data word at a write operation. A read operation implies checking of the previous stored parity information.

An occurrence of a parity error is observable at the ***SRRAW***/***SRRAW1*** status register. It is configurable via ***SRMSK***/***SRMSK1*** whether a memory error should trigger an interrupt. It can also trigger a system reset when ***RSTCON***.SPERSTEN, ***RSTCON***.U0PERSTEN, ***RSTCON***.U1PERSTEN or ***RSTCON***.MPERSTEN is set to 1.

A parity control software test, such as to support in-system testing to fulfill Class B requirements, can be enabled with bit ***PMTSR***.MTENS for the 16 kbytes SRAM memory individually. Once this bit is set, an inverted parity bit is generated during a write operation. When a read operation is performed on this SRAM address, a parity error shall be detected.

Note: Test software should be located in a different memory space.

14.2.3 Summary of ID

This section describes the various ID in IMC300A.

Module Identification

The module identification register indicates the function and the design step of each peripherals. Register SCU_***ID*** is used for SCU module.

System ROM Table ID

The PID values in the system ROM table are defined in the ***Table 165***. The IMC300A system ROM table is located at F000 0000$_H$. Cortex-M0 ROM table is described in the debug chapter.

Table 165 PID Values of IMC300A System ROM Table

Name	Offset	Reference	Values
PID0	FE0$_H$	IMC300A Part Number [7:0]	04$_H$
PID1	FE4$_H$	bits [7:4] JEP106 ID code [3:0] bits [3:0] IMC300A Part Number [11:8]	12$_H$
PID2	FE8$_H$	bits [7:4] IMC300A Revision bit [3] == 1: JEDEC assigned ID fields bits [2:0] JEP106 ID code [6:4]	1C$_H$
PID3	FEC$_H$	bits [7:4] RevAnd, minor revision field bits [3:0] if non-zero indicate a customer-modified block	00$_H$
PID4	FD0$_H$	bits [7:4] 4KB count bits [3:0] JEP106 continuation code	00$_H$

Chip Identification Number

The chip identification number is a 8 word length number. It consists of the values in register DBGROMID, IDCHIP, register PAU_FLSIZE, register PAU_RAM0SIZE and register PAU_AVAILn(n=0-2) respectively. This number is for easy identification of product variants information of the device, example, package type, the temperature profile, flash size, RAM size and the peripheral availability.

14.2.4 Boot via Pins

In IMC300A, the following boot modes can be selected via pin configuration (P4.6 and P4.7):

- ASC BSL
- CAN BSL
- User productive mode
- User Boot mode

The input of boot pin are latched during the de-assertion of reset and stored in register bit STSTAT.HWCON. More details about the selection of this mode can be found in the “Boot and Startup” Chapter.

14.3 Power Management (PCU)

Power management control is performed in the Power Control Unit (PCU).

14.3.1 Functional Description

The IMC300A is running from a single external power supply of 3.0 - 5.5V (V_{DDP}). The main supply voltage is supervised by a supply watchdog.

The I/Os is running directly from the external supply voltage. The core voltage (V_{DDC}) is generated by an on-chip Embedded Voltage Regulator (EVR). The safe voltage range of the core voltage is supervised by a power validation circuit, which is part of the EVR.

14.3.2 System States

The system has the following general system states:

- Off
- Active
- Sleep
- Deep-Sleep

Figure 36 shows the state diagram and the transitions between the states.

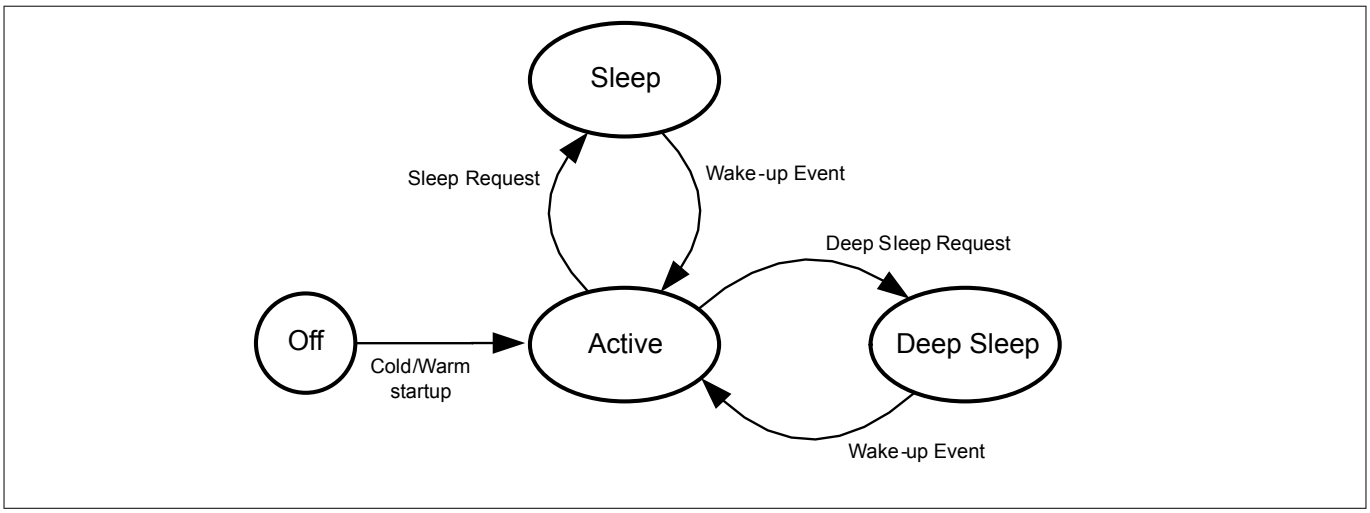


Figure 36 System States Diagram

Active State

The active state is the normal operation state. The system is fully powered. The CPU is usually running from a high-speed clock. Depending on the application, the system clock might be slowed down. Unused peripherals might be stopped by gating the clock to these peripherals.

Sleep State

The sleep state of the system corresponds to the sleep state of the CPU. The state is entered via WFI or WFE instruction of the CPU. In this state, the clock to the CPU is stopped. To save power, the clock of the peripherals that are not needed during sleep state can be gated by register ***CGATSET0*** before entering sleep state.

The Flash can be put into shutdown mode during active state to achieve a further power reduction before entering sleep state via bit NVMCONF.NVM_ON. However, user code would have to be executed in SRAM before entering sleep state and after waking up from sleep state.

To avoid the switching of code execution to SRAM due to the shutdown of flash, register ***PWRSVCR*** can be used. When FPD bit is set, flash is shutdown only when the device has entered sleep state. The shut down operation is performed after the core has executed WFI/WFE instruction. After a wake-up event is detected, the system will resumed to the previous state i.e. the flash is operable again before the CPU can continue to fetch and execute the code. In this case, user code can be executed in Flash and no switching to SRAM in needed. In his approach, the wake-up time is longer because of the time needed for flash to reach the active state.

Peripherals can continue to operate unaffected and eventually generate an event to wake-up the CPU. In User with Debug mode (UMD) or User with Debug mode and HAR (UMHAR), a Debug HALT request is also able to wake-up the CPU. Any accordingly configured interrupt will bring the CPU back to operation via the NVIC or the M0 debug system.

Deep-Sleep State

The deep-sleep state is entered on the same mechanism as the sleep state with the addition that user code has enabled the deep-sleep state in system control register. This state is similiar to sleep state, except that in deep-sleep state, the PCLK and MCLK will be switched to a slow standby clock and DCO1 will be put into power-down mode.

The analog comparator could also be kept active during deep-sleep state. It can be switched to low power mode to save power.

The shutting down of flash via NVMCONF.NVM_ON or PWRSVCR.FPD as explained in above section is applicable for deep-sleep mode.

Peripherals that continue to operate will run using the slow standby clock and can eventually generate an event to wake-up the CPU. In User with Debug mode (UMD) or User with Debug mode and HAR (UMHAR), a Debug HALT request is also able to wake-up the CPU. Any accordingly configured interrupt will bring the CPU back to operation via the NVIC or the M0 debug system. The clock system is restored to the previous configuration for active state upon wake-up. Peripherals that are active will run with restored clock configuration.

The SRAM content is preserved in the deep-sleep state.

Note: It is recommended to slow down the PCLK and MCLK before entering deep sleep mode to prevent a sudden load change that could cause a brownout reset.

Note: When DCO1 is used for the generation of MCLK/PCLK, it is recommended to disable the DCO1 calibration function before entering deep-sleep mode.

14.3.3 Embedded Voltage Regulator (EVR)

The EVR generates the core voltage V_{DDC} out of the external supplied voltage V_{DDP}. The EVR provides 2 supply monitoring detectors for the input voltage V_{DDP}. The generated core voltage V_{DDC} is monitored by a power validation circuit (PV).

14.3.4 Power-on Reset

The EVR starts operation as soon as V_{DDP} is above defined minimum level. It releases the reset, when the external voltage V_{DDP} and the generated voltage V_{DDC} are above the reset thresholds and reaching the nominal values.

14.3.5 Power Validation

A power validation circuit monitors the internal core supply voltage,V_{DDC}. It monitors that the core voltage is above the voltage threshold V_{DDCBO} which guarantees safe operation. Whenever the voltage falls below the threshold level, a brownout reset is generated.

14.3.6 Supply Voltage Monitoring

There are 2 detectors, namely, External voltage detector (VDEL) and External brownout detector (BDE) in the EVR that are used to monitor the V_{DDP}.

VDEL detector compares the supply voltage against a pre-warning threshold voltage. The threshold level is programmable via register ANAVDEL.VDEL_SELECT. An interrupt if enabled, will be triggered if a level below this threshold is detected and the flag, VDDPI, in SRRAW register bit is set. An indication bit, VDESR.VDDPPW, shows the output of the detector. During power-up, this indication bit can be polled to ensure that the external supply has reached the pre-warning voltage before starting the application code.

BDE detector is used to trigger a brownout reset when the V_{DDP} supply voltage drops below the defined threshold. Similiarly, it is also used to ensure a proper startup during the power-up phase.

The Data Sheet defines the nominal value and applied hysteresis

14.3.7 V_{DDC} Response During Load Change

In IMC300A, the core voltage level, V_{DDC}, drops below the typical threshold when there is an increase in the load and rises when there is a decrease in the load. 2 detectors, VDROP and VCLIP detectors are used to montior the lower limits and the upper limits of the core voltage level respectively (detectors details are described in the next section). A VDROP event happens when VDDC drops below the VDROP threshold voltage. A VCLIP event happens when VDDC rises above the VCLIP threshold voltage. Each of these events can triggered it's dedicated interrupt if enabled via SRMSK register and the event status can be monitior via SRRAW register.

In IMC300A, the following scenarios may trigger a VDROP/VCLIP event due to load change:

- Changing the MCLK and PCLK frequency via CLKCR register
- Enabling/Gating the peripheral clock via the CGATSET0/CGATCLR0 registers

When a sudden load change happens (> 4*baseload or < 0.25*baseload), irregardless of an increase or decrease in load, the EVR needs time (15 usec) to regulate the core voltage back to a stable nominal voltage. During this period of time, the system is expected to maintain in the current load and no load change is allowed. Status bit VDDC2LOW and VDDC2HIGH in CRCLK register are used to indicate whether the voltage is stable.

Note: It is not recommended to increase the load more than 4 times of the baseload or decrease the load to less than 0.25 times of the baseload. If a bigger than the specified load change is required, the recommendation is to change the load in steps that each steps are within the limits. For example, a final load of 16mA from the current baseload of 1mA needs at least 2 steps. A step from 1mA to 4mA followed by another step from 4mA to 16mA

The VDDC2LOW and VDDC2HIGH status bit is generated by a 10-bit counter using 48MHz clock as the clock input . It is implemented to count the 16 usec (default) that is needed to have a stable V_{DDC} after a VDROP or VCLIP event happens. The length of this counter can be changed depending on the amount of load change via bit CLKCR.CNTADJ. The larger is the load change, the more is the time that user need to wait for a stable clock. Refer to datasheet for a guideline of the current consumption of each modules.

Using the example above, after programming some configuration that causes a change in load from 1mA to 4mA, user can poll for VDDC2LOW (CNTADJ=300_H) to ensure the 16 usec(max) needed to regulate EVR. After VDDC2LOW is set to 0, another load change from 4mA to 16mA can be performed and the cycle repeats for each step of load change.

During a VDROP event, clock blanking happens and the detail description is documented in ***Clock Blanking*** on page ***244***. CPU clock and peripheral clocks continue to run during VCLIP event.

Note: When overflow event happens while the VDROP=1 (time to overflow based on the CNTADJ value is shorter than the time the device stays in a vdrop event), the 10-bit counter will automatically be restarted with the CNTADJ value.

Note: VDROP and VCLIP detectors are disabled during deep sleep mode.

14.3.8 Flash Power Control

The Flash module can be switched off to reduce static power. In sleep or deep-sleep state, it is dependent on the setting of register ***PWRSVCR*** whether the Flash module will be put to sleep or not in this state. The user has to evaluate the reduced leakage current against the longer startup time. In addition, the Flash can also be put to sleep using NVMCONF.NVM_ON before entering these power save modes.

14.4 Reset Control (RCU)

Reset Control Unit performs control of all reset related functionality including:

- Reset assertion on various reset request sources
- Inspection of reset sources after reset
- Selective reset of peripheral

14.4.1 Functional Description

The IMC300A has the following reset types for the system:

- Master Reset, $\overline{\text{MRESET}}$
- System Reset, $\overline{\text{SYSRESET}}$

Master Reset, $\overline{\text{MRESET}}$

Master reset is triggered by:

- Power-on reset (PORST)
- V_{DDP} or V_{DDC} undervoltage reset (also known as brownout reset)
- SW master reset via setting bit RSTCON.MRSTEN to 1

A complete reset to the device is executed by a master reset. Master reset is triggered by a power-on reset upon power-up. Whenever the supply V_{DDP} is ramped-up and crossing the V_{DDP} and V_{DDC} voltage threshold, the power-on reset is released. A power-on reset (also known as brown-out reset) is asserted again whenever the V_{DDP} voltage or the V_{DDC} voltage falls below reset thresholds. In additional, a master reset can be triggered by setting bit RSTCON.MRSTEN.

The sources that trigger a master reset also triggers a system reset $\overline{\text{SYSRESET}}$.

System Reset, $\overline{\text{SYSRESET}}$

System reset is triggered by:

- SW reset via Cortex M0 Application Interrupt and Reset Control Register (AIRCR)
- Lockup signal from Cortex M0 when enabled at RCU
- Watchdog reset
- Memory parity error when enabled
- Flash ECC double bit error when enabled

- Loss of DCO1 clock when enabled
- sources that trigger a master reset

A system reset affects almost all logics. The only exceptions are RCU registers and Debug system when debug probe is present. The reset gets extended to the length defined by implementation requirements.

The debug system is reset by System Reset in normal operation mode when debug probe is not present. When debug probe is present, System Reset must not affect the Debug system.

14.4.2 Reset Status

The EVR provides the cause of a power on reset to the RCU. The reset cause can be inspected after resuming operation by reading register ***RSTSTAT*** . This register also indicates the source of event that causes the triggering of a system reset.

All registers of the RCU undergo reset only by a master reset except for RSTSTAT and RSTCON register. RSTSTAT register is only reset by a power-on reset and RSTCON is reset by any reset type.

*Note: Clearing of the reset status via register bit **RSTCLR**.RSCLR is strongly recommended to ensure a clear indication of the cause of next reset.*

Table 166 shows an overview of the reset signals their source and effects on the various parts of the system.

Table 166 Reset Overview

Module/Function	Power-on Reset	Master Reset by SW bit	System Reset
CPU Core	yes	yes	yes
SCU	yes	yes	yes, except reset indication bit
Peripherals	yes	yes	yes
Debug System	yes	yes	see footnote[24)25)]
Port Control	yes	yes	yes
SRAM	Affected,unreliable	Not affected	Not affected
Flash	yes	yes	yes
EVR	yes	no[26)]	no
Clock System	yes	yes	yes

14.5 Clock Control (CCU)

14.5.1 Features

The clock control unit CCU has the following functionality:

- Dedicated RTC and standby clock

24 Debug system will be reset only if debug probe is not present.
25 Access to debug interface is disabled after every reset even when debug probe is present. See Warm Reset section of Debug System chapter for more details.
26 The supply to EVR will not be affected and hence a complete reset to EVR is not possible. However, it will be partially affected by the reset in the ANACTRL module.

- Clock Supervisory
  - Oscillator watchdog
- Wide range of frequency scaling of system frequencies
- Individual peripheral clock gating
- Calibration of DCO based on external reference clock or the temperature sensor
- Controls for the external oscillator, eg crystal oscillators

14.5.2 Clock System and Control

Figure 37 shows the block diagram of the clock system in IMC300A. It consists of two on-chip oscillators (DCO1[27)] with synchronisation unit and DCO2), 2 oscillators pad (OSC_HP and OSC_LP to drive external clock), a doubler and a clock control unit (CCU). DCO1 has a clock output (dco1_clk), running at 48MHz. DCO2 is used to generate the standby clock running at 32kHz.

The main clock, MCLK, and fast peripherial clock, PCLK, are generated from DCLK (output of the doubler clock). Input to DCLK can be selected using bit ***CLKCR1***.DCLKSEL to be either from the DCO1 clock source or the external clock source via the OSC_HP oscillator. After reset, DCLK is generated from DCO1 clock source. To select the external clock source, the sequence described in ***Chapter 14.5.2.7*** is required.

PCLK is running in either the same frequency as MCLK or double the frequency of MCLK. It is selectable via ***CLKCR***.PCLKSEL.

Figure 37 shows the list of peripherals that are running in the PCLK domain. The rest of the peripherals except RTC and WDT are clocked by MCLK which is the same as the core and bus system. WDT is running at a frequency of 32kHz from the standby clock which is asychronous to the MCLK and PCLK clock. RTC is running asynchronously from either the internal 32kHz standby clock or the external 32.768kHz XTAL (via ERU/ACMPx or the OSC_LP).

27 The accuracy of the DCO1 clock output can be improved by calibrating it based on the die temperatue given by the temperature sensor or based on an accurate external references. Refer to ***Chapter 14.5.4*** and ***Chapter 14.5.5*** respectively for detailed description.

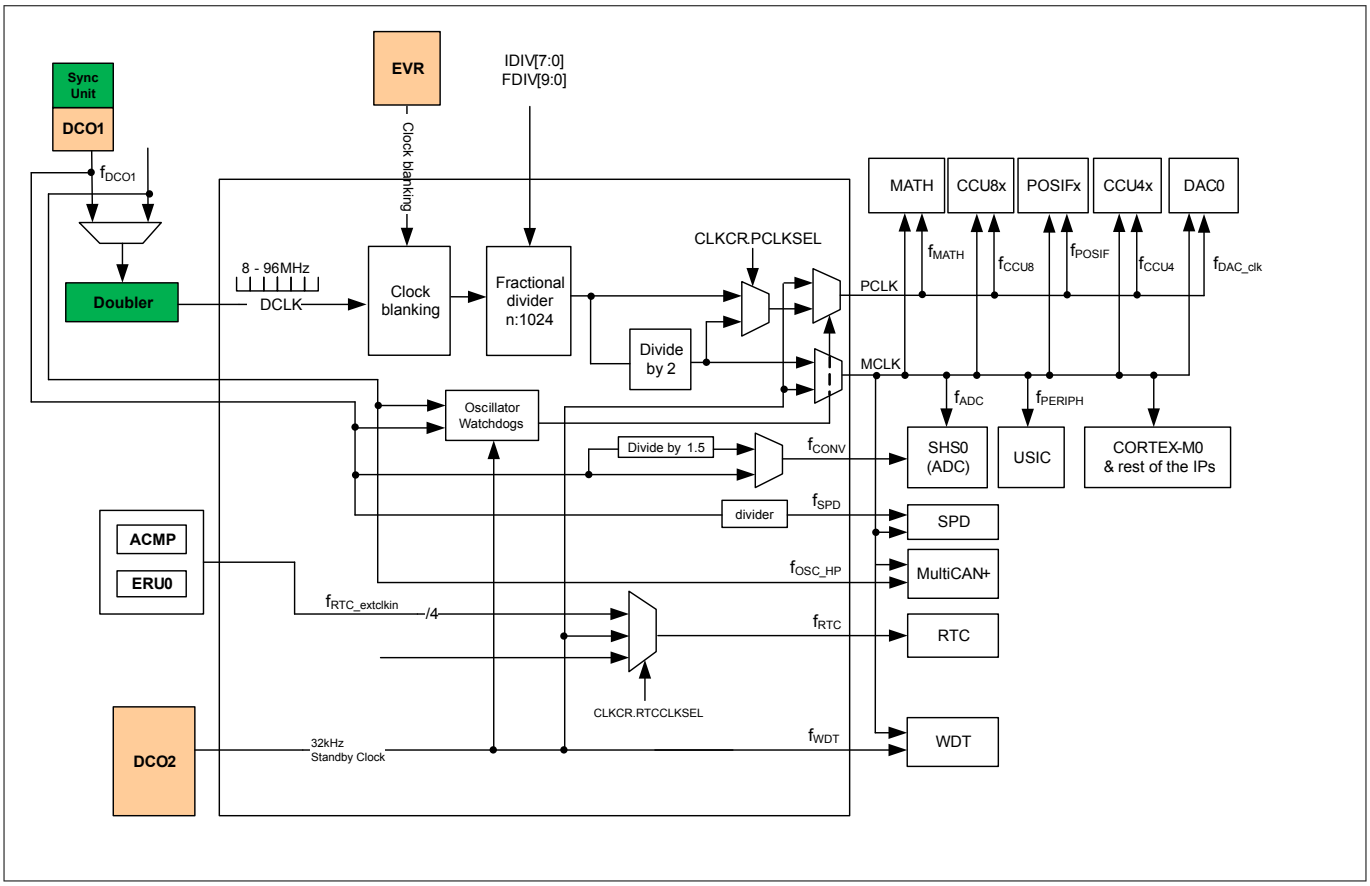


Figure 37 Clock System Block Diagram

Note: SHS(ADC) clock will not switched to standby clock source when there is a loss of DCO1 or external clock event.

Note: DCO1 must be enabled (OSCCSR.DCO1PD = 0_B) when debug system via SPD or ADC is enabled.

Note: RTC_extclkin are further described in RTC chapter.

*Note: MultiCAN+ clocks are further described in page **246** .*

The following clock configuration option can be used for maximum performance and clock accuracy:

- Select DCO1 for MCLK (max. 48MHz) and PCLK (max. 96 MHz)
- Select external crystal (20MHz) for accurate CAN baudrate generation
- Calibrate DCO1 based on external crystal to achieve accurate MCLK/PCLK (see ***Chapter 14.5.5***)

Fractional Divider

The frequency of MCLK and PCLK are programmable through a fractional divider. The range of PCLK and MCLK frequencies based on different clock source are shown in ***Table 167***.

Table 167 PCLK and MCLK frequency range

DCLK clock source	DCLK frequency	PCLK frequency	MCLK frequency
DCO1 (48MHz)	96MHz	188kHz - 96MHz	188kHz - 48MHz

Table 167 PCLK and MCLK frequency range (continued)

DCLK clock source	DCLK frequency	PCLK frequency	MCLK frequency
External oscillator via OSC_HP in osc mode (4 - 20MHz)	8MHz - 40MHz	15.6kHz - 40MHz	15.6kHz - 20MHz
External clock via OSC_HP in direct-in mode (4 - 48MHz)	8MHz - 96MHz	15.6kHz - 96MHz	15.6kHz - 48MHz

The following formula calculate the MCLK clock frequency.

$$\left(MCLK = \frac{DCLK}{(2) \times \left(IDIV + \frac{FDIV}{1024} \right)} \right) \text{ for IDIV > 0}$$

Equation 4

The following formula calculate the PCLK clock frequency when CLKCR.PCLKSEL is set to 1 and it is double the frequency of MCLK.

$$\left(PCLK = \frac{DCLK}{\left(IDIV + \frac{FDIV}{1024} \right)} \right) \text{ for IDIV > 0}$$

Equation 5

IDIV represents an unsigned 8-bit integer from the bit field CLKCR.IDIV and FDIV/1024 defines the fractional divider selection in CLKCR.FDIV. FDIV is an unsigned 10-bit integer from bit field CLKCR1[1:0] and CLKCR[7:0].

Table 168 Examples of MCLK frequency (FDIV=0)

DCLK frequency	IDIV = 1	IDIV = 2	IDIV = 4	IDIV = 8	IDIV = 128
96MHz via DCO1	48MHz	24MHz	12MHz	6MHz	375kHz
40MHz via 20MHz crystal oscillator	20MHz	10MHz	5MHz	2.5MHz	156kHz

Below is the sequence to program the MCLK and PCLK frequency :

- Enable the access of protected bit IDIV and FDIV via register PASSWD
- Program the IDIV, FDIV value
  - write value to CLKCR1.FDIV (optional, could be skipped if no update required)
  - write value to CLKCR.IDIV/FDIV (mandatory, IDIV/FDIV is valid only when register CLKCR is written)

Changing of the MCLK and PCLK can be done within 2 clock cycles .

*Note: Changing the MCLK and PCLK frequency may result in a load change that causes clock blanking to happen. Refer to **Clock Blanking** and **V_{DDC} Response During Load Change** for more details.*

Clock Blanking

To prevent a brown-out reset in case of a sudden positive load change, the clock blanking circuitry is used. It freezed the clock input to the fractional divider to regulate the load change. The clock blanking only causes a small jitter if it is considered over a longer time period.

The clock blanking is activated when V_{DDC} is detected to be below the VDROP threshold. Once the V_{DDC} is above this threshold, the enabled clocking is resume. This voltage drop detector is part of the EVR and it is activated by default upon any reset.

To monitor clock blanking activities, user can enable interrupt but can only enter ISR after the clock resume.

In addition to the use of clock blanking function to prevent a brown-out reset, the system is also expected to maintain in the current load and no further load change is allowed for 16 usec (max). Detail description of the core voltage behaviors during load change are described in ***V_{DDC} Response During Load Change*** on page ***239***.

As described in ***V_{DDC} Response During Load Change*** on page ***239***, the status bit CLKCR.VDDC2LOW is used to indicate to user that the core voltage, V_{DDC}, is below the nominal voltage and EVR is in the process of regulating it. During this period, the clock could be also not running in the selected speed and it is recommended to poll this bit before continuing with any large change to the current load.

Note: It is recommended to slow down the PCLK and MCLK before entering deep sleep mode to prevent a sudden load change that could cause a brownout reset when entering .

High Precision Oscillator Circuit (OSC_HP)

The high precision oscillator circuit can drive an external crystal or accepts an external clock source. It consists of an inverting amplifier with XTAL1 as input, and XTAL2 as output.

Figure 38 and ***Figure 39*** show the recommended external circuitries for both operating modes, External Crystal Mode and External Input Clock Mode.

In external input clock mode, an external clock signal is supplied directly not using an external crystal and bypassing the amplifier of the oscillator. The input frequency must be in the range from 4 to 48MHz.When using an external clock signal it must be connected to XTAL1. XTAL2 is left open i.e. unconnected.

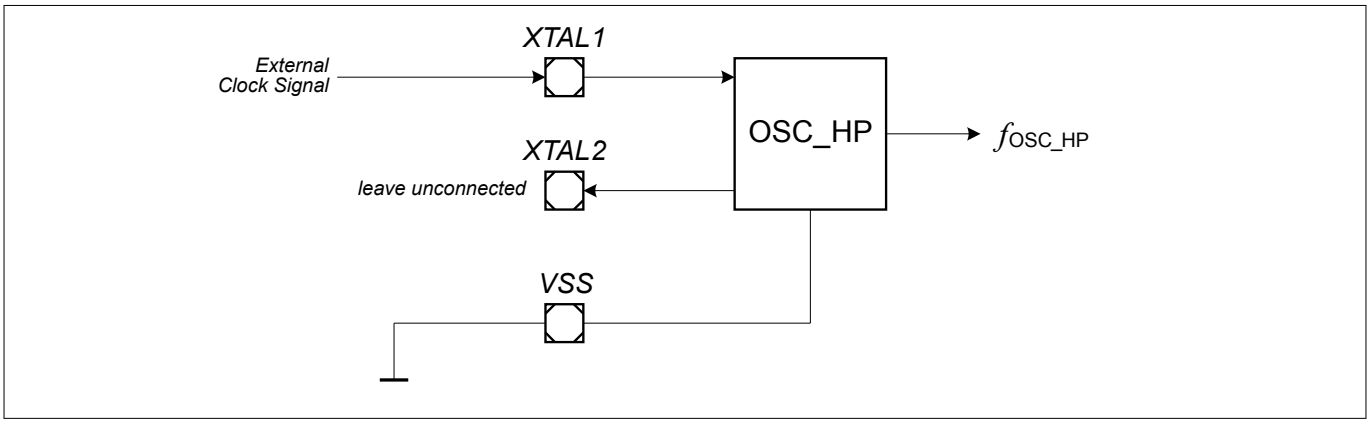


Figure 38 External Clock Input Mode for the High-Precision Oscillator

For the external crystal mode an external oscillator load circuitry is required. The circuitry must be connected to both pins, XTAL1 and XTAL2. It consists normally of the two load capacitances C1 and C2. For some crystals, a series damping resistor might be necessary. The exact values and related operating range depend on the crystal and have to be determined and optimized together with the crystal vendor using the negative resistance method.

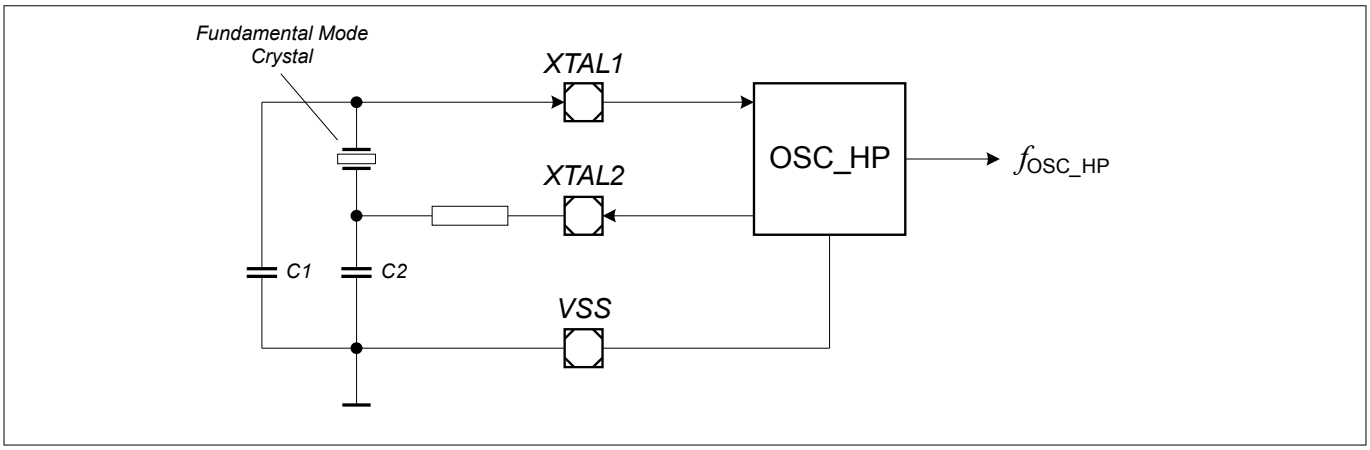


Figure 39 External Crystal Mode Circuitry for the High-Precision Oscillator

MultiCAN+ Clock

Figure 40 show the clock selection via the MultiCAN+ register bit CAN_MCR.CLKSEL. Refer to MultiCAN+ chapter for detailed description.

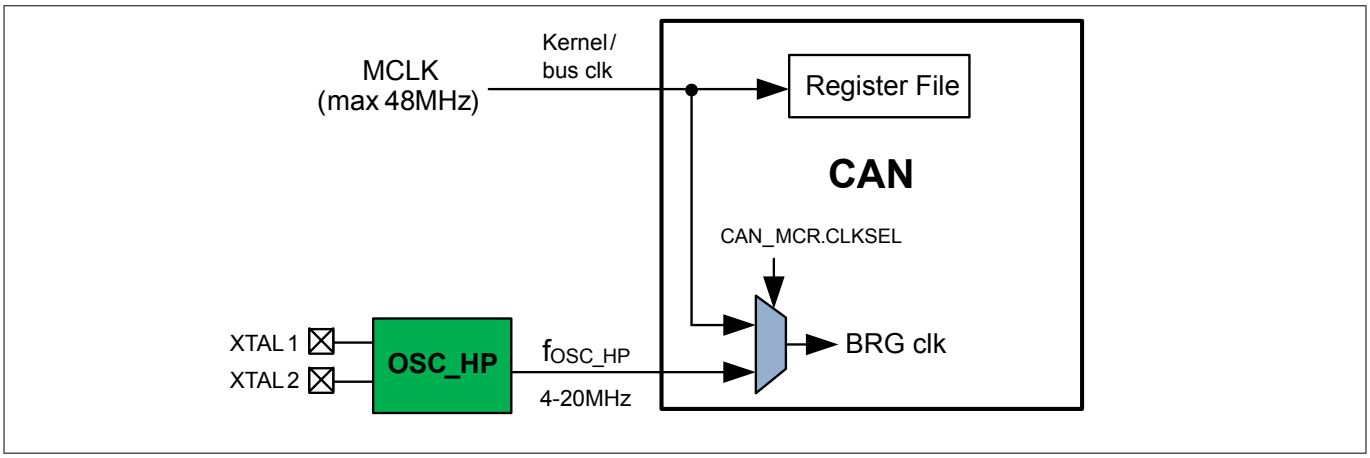


Figure 40 MultiCAN+ Clock

Note: Before changing MutliCAN+ clock source, the CAN clock must be gated using bit CGATSET0.MCAN0.

Note: OSC_HP must be enabled (ANAOSCHPCTR.MODE) before changing the MutliCAN+ clock source.

14.5.2.1 DCO1 Oscillator Watchdog

The oscillator watchdog (OWD) monitors the DCO1 clock frequency using the standby clock as the reference clock. It can be disabled via OSCCSR.OWDEN. By setting bit OSCCSR.OWDRES[28], the detection for DCO1 clock frequency can be restarted. The detection status output is only valid after some cycles of the standby clock frequency. When the OWD is disabled, the detection status will be reset and no detection is possible.

If the OWD is enabled before entering deep sleep mode, it will be disabled automatically by hardware when it enters deep sleep mode and re-enabled again after exiting deep sleep mode. The detection is reset and restarted after device wake-up from deep sleep mode.

28 It is recommended to clear the status bit SRRAW.LOCI and SRRAW.SBYCLKFI before restarting the detection.

14.5.2.2 Loss of DCO1 Clock Detection and Recovery

Loss of DCO1 clock happens when the oscillator watchdog (OWD) detects a DCO1 frequency that is less than 75MHz or more than 105MHz during normal operation. In this case, an interrupt will be generated if it is enabled. Concurrently, the oscillator status flag, OSCCSR.OSC2L or OSCCSR.OSC2H, is set to 1 and the system clock will be provided by the standby clock of 32kHz if DCO1 is selected for the generation of PCLK/MCLK. Emergency routines can be executed to safely shut down the system. Beside triggering an interrupt when the loss of DCO1 clock happens, a system reset can also be triggered if it is enabled by ***RSTCON***.LOCRSTEN.

*Note: Switching to standby clock during loss of DCO1 clock event happens only if DCO2 is still running (>0MHz). Bit **SRRAW**.SBYCLKFI indicates the fail status of the standby clock.*

The IMC300A remains in this loss of clock state until the next reset or after a successful clock recovery has been performed. A clock recovery could be carried out by restarting the detection by setting bit OSCCSR.OWDRES. Upon detecting a stable oscillator frequency of more than and lower than , OSC2L and OSC2H will be set to 0 and the MCLK/PCLK will switched automatically to the DCO1 clock source.

14.5.2.3 Standby Clock Failure

The standby clock failure event happens when the OWD detects a failure in standby clock where the clock stops running (~0kHz). Bit SRRAW.SBYCLKFI is set to 1 and trigger an interrupt via SCU_SR1 service request if the interrupt is enabled in register SRMSK.

14.5.2.4 XTAL Oscillator Watchdog

The XTAL oscillator watchdog (XOWD) monitors the external OSC_HP clock frequency using the standby clock as the reference clock. It can be disabled via OSCCSR.XOWDEN. By setting bit OSCCSR.XOWDRES[29], the detection for the external OSC_HP clock frequency can be restarted. The detection status output is only valid after some cycles of the standby clock frequency. When the XOWD is disabled, the detection status will be reset and no detection is possible.

If the XOWD is enabled before entering deep sleep mode, it will be disabled automatically by hardware when it enters deep sleep mode and re-enabled again after exiting deep sleep mode. The detection is reset and restarted after device wake-up from deep sleep mode.

Note: When OSC_HP is disabled in deep sleep mode, it is recommended to disable XOWD first before entering deep sleep to avoid a false detection after device wake-up.

14.5.2.5 Loss of external OSC_HP Clock Detection and Recovery

Loss of external (OSC_HP) clock happens when the XTAL oscillator watchdog (XOWD) detects a a failure in the external XTAL clock where the clock stops running (~0kHz). In this case, bit SRRAW1.LOECI is set to 1 and trigger an interrupt via SCU_SR1 service request if the interrupt is enabled in register SRMSK1. Concurrently, the system clock will be provided by the standby clock of 32kHz if external clock is used to generate the PCLK/MCLK. Emergency routines can be executed to safely shut down the system. Beside triggering an interrupt when the loss of external clock happens, a system reset can also be triggered if it is enabled by ***RSTCON***.LOECRSTEN.

*Note: Switching to standby clock during loss of external clock event happens only if DCO2 is still running (>0MHz). Bit **SRRAW**.SBYCLKFI indicates the fail status of the standby clock.*

29 It is recommended to clear the status bit SRRAW1.LOECI and SRRAW.SBYCLKFI before restarting the detection.

The IMM100 remains in this loss of clock state until the next reset or after a successful clock recovery has been performed. A clock recovery could be carried out by restarting the detection by setting bit OSCCSR.XOWDRES. Upon detecting a stable external clock frequency, MCLK/PCLK will switched automatically to the external clock source.

14.5.2.6 Startup Control for System Clock

When the IMC300A starts up after reset, system frequency is provided by the DCO1 oscillator. After reset, CPU runs in 8MHz, default frequency. User can change the clock frequency that is used to execute the SSW and the user application code by defining it in the flash memory location 1000 1010_H. This feature allows the fexibility of device performance e.g. speed vs power consumption optimisation during start-up. For details, please refer to the section “Clock system handling by SSW” in the “Boot and Startup” chapter.

14.5.2.7 DCLK input - External Clock via OSC_HP

The following sequence shall be used to select the external clock source via OSC_HP as the DCLK input.

- Enable OSC_HP with shaper not bypassed
  - set ANAOSCHPCTRL.MODE to 11_B
  - set ANAOSCHPCTRL.GAIN to
- Wait 10msec for the external clock to stablise
- Enable and reset XOWD
  - set OSCCSR.XOWDEN to 1_B
  - set OSCCSR.XOWDRES to 1_B
- Select external clock source as DCLK input (set bit CLKCR1.DCLKSEL)

14.5.3 Clock Gating Control

The clock to peripherals can be individually gated and parts of the system can be stopped by registers ***CGATSET0***. After a master reset, only core, memories, SCU and PORT peripheral are not clock gated. The rest of the peripherals are default clock gated. User can select the clock of individual modules to be enabled by SSW after reset by defining it in the flash memory location 1000 1014_H. Refer to Boot and Startup chapter for more details.

Load change during module clock enabling or gating

Enabling or gating the clock to peripherals could result in a load change that could cause clock blanking to happen. In addition, a load change of more than 4 times the current load would required the system to maintain in the current load and no further load change is allowed for 16 usec (max). See ***V_{DDC} Response During Load Change*** for more details.

Module clock gating in Sleep and Deep-Sleep modes

It is recommended to gate the clock using registers ***CGATSET0*** for module that is not needed during sleep mode or deep-sleep mode. These modules must be disabled before entering sleep or deep-sleep mode. In addition, the PCLK and MCLK will be switched to a slow standby clock and DCO1 will be put into power-down mode in deep-sleep mode.

14.5.4 Calibrating DCO1 based on Temperature

In IMC300A, DCO1 clock frequency can be calibrated during runtime to achieve a better accuracy. Based on the measured temperature using the on-chip temperature sensor(DTS), an offset value can be obtained using the formulae as shown below:

$$\text{OFFSET[steps]} = b + \frac{(a-b)(c-d)}{(e-d)}$$

Equation 6

where :

OFFSET value is range from 0 to 255

c is the measured temperature [°C]

a is constant DCO_ADJLO_T2

b is constant DCO_ADJLO_T1

d is constant ANA_TSE_T1

e is constant ANA_TSE_T2

The 4 constants in the formulae are stored in flash configuration page shown in ***Table 169***.

Table 169 DCO calibration data in Flash sector 0 (CS0)

Address	Length	Function
		DCO calibration data:
1000'0F30H	1 B	ANA_TSE_T1
1000'0F31H	1 B	ANA_TSE_T2
1000'0F32H	1 B	DCO_ADJLO_T1
1000'0F33H	1 B	DCO_ADJLO_T2

Input the offset value (rounded to the nearest integer) to register bit ***ANAOFFSET***.ADJL_OFFSET to start the DCO1 calibration. The offset value must be within the range of 0 to 255. This bit field is bit protected. DCO1 will take about 5 usec(max) for clock to be adjusted to the new frequency.

Note: Ensure bit ANASYNC1.SYNC_DCO_EN is set to 0 to disable the calibration via an external clock source so that the calibration via DTS can be carried out.

14.5.5 Automatic DCO1 Calibration based on External Reference

In IMC300A, DCO1 clock frequency can be calibrated automatically during runtime to achieve a better accuracy. To achieve an accuracy of < +/- 0.3%, calibration performed by a synchronisation unit using high-precision clock as reference is implemented. The high precision clock source for synchronisation would be either one of the following and is selectable via bit ANASYNC1.XTAL_SEL:

- OSC_HP via XTAL1 and XTAL2 (4 - 20MHz)
- OSC_LP via RTC_XTAL1 and RTC_XTAL2 (32.768kHz)

Figure 41 shows the overview of the calibration scheme in IMC300A. It is enabled via bit ***ANASYNC1***.SYNC_DCO_EN. ***ANAOFFSET***.ADJL_OFFSET is taken as the initial DCO1 adjust value once the synchronisation unit is enabled.

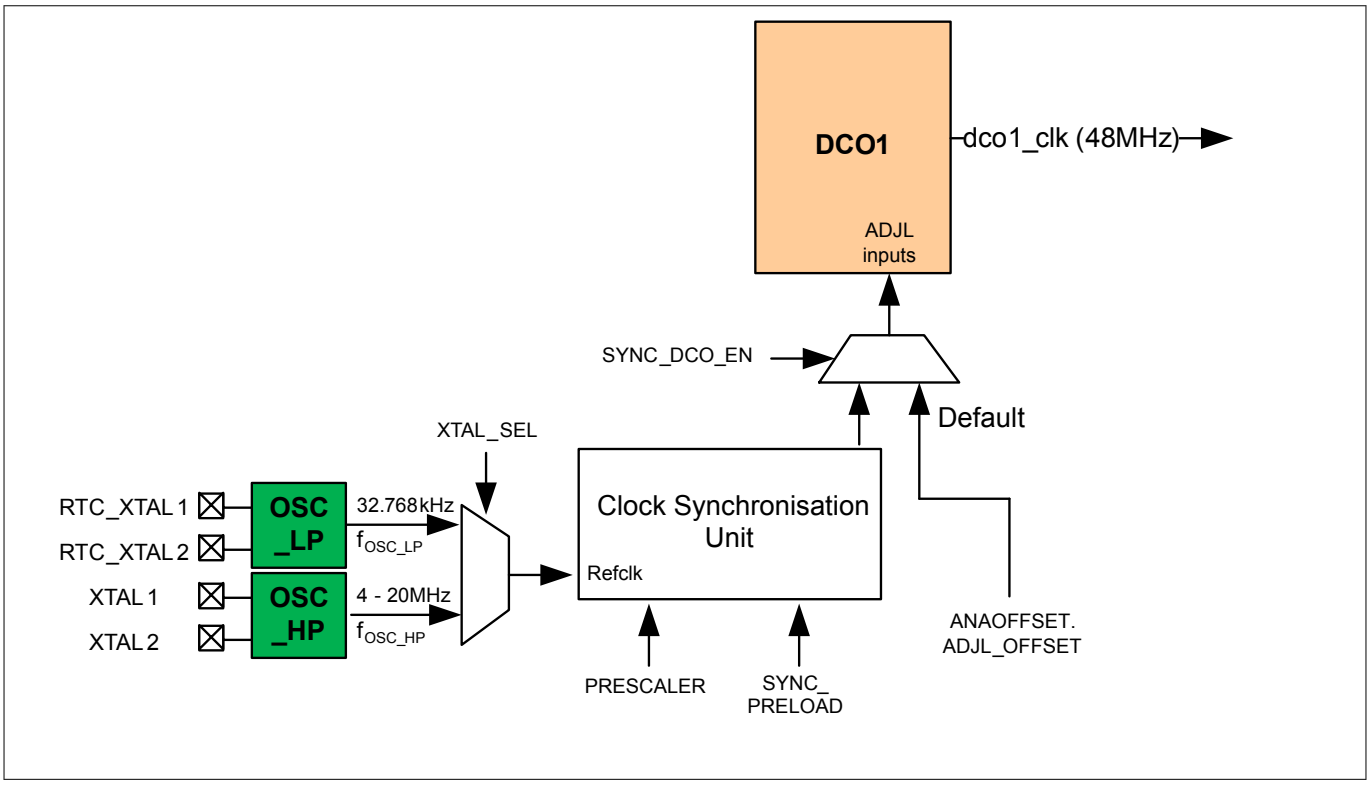


Figure 41 DCO1 Calibration

Note: The external clock must be enabled and stablised before selecting the automatic DCO1 calibration based on XTAL

Note: DCO1 is shut down when device enter Deep sleep mode. Hence, before entering Deep sleep mode, it is recommended to disable the automatic DCO1 calibration and shut down the XTAL function. If it is enabled, the DCO1 calibration will be disabled automatically during Deep sleep mode and resume after exiting this mode. Under this situation, the calibration values to ADJL inputs will be kept as the last values when the operation resume.

Before enabling the DCO1 calibration, 2 values are needed to be programmed into bit ANASYNC2.PRESCALER and ANASYNC1.SYN_PRELOAD in order to generate a MCLK/PCLK frequency which is close to its target frequency. These parameters need to be setup once depending on the selected type of external clock source.

To trigger a reload of ANASYNC1.SYNC_PRELOAD and ANASYNC2.PRESCALER to the synchronisation unit, write access to one of following:

- write access to register ANASYNC1
- write access to register ANASYNC2

Using OSC_LP as Reference for Calibration

Table 170 shows the recommended values if OSC_LP is used as the reference clock.

Table 170 Recommended values for a 32.768kHz clock via OSC_LP

Register name	HEX value
ANASYNC2.PRESCALER	6
ANASYNC1.SYNC_PRELOAD	2256

Using OSC_HP as Reference for Calibration

When OSC_HP is used, according to the wide range of selectable f_{OSC_HP} frequency (e.g 4 - 20MHz crystal oscillator), these two values have to be calculated once for a defined and constant crystal frequency based on the formula

.

$$PRESCALER = \text{integer}\left(\frac{3000 \times f_{OSC_HP}[MHz]}{48}\right)$$

Equation 7

$$SYN_PRELOAD = \text{integer}\left(\frac{48 \times PRESCALER}{f_{OSC_HP}[MHz]}\right)$$

Equation 8

Table 171 shows some examples of PRESCALER and SYNC_PRELOAD values based on the frequency of the selected oscillator, f_{OSC_HP}.

Table 171 Examples of PRESCALER and SYNC_PRELOAD values

f_{OSC_HP}	***ANASYNC2*.PRESCALER**	***ANASYNC1*.SYNC_PRELOAD**
4	250	3000
8	500	3000
16	1000	3000
20	1250	3000

DCO1 Out of Synchronisation

The status of synchronisation can be monitored via bit ANASYN2.SYNC_READY. When the DCO1 synchronisation is not within the defined range, a DCO1 out of synchronisation (DCO1OFS) event occurs. An interrupt can be triggered via SCU SR1 request source during this event when is it enabled via the enable bit, DCO1OFSI in the SRMSK1 register.

As a precondition, the DCO1 frequency has to be synchronized once (by polling bit syn_ready in ANASYNC2 until it gets set). After that, it is then recommend to enable this interrupt if needed to detect the DCO1 out of synchronisation event. Status bit has to be cleared by using a bit in SRCLR1 register.

14.6 Service Request Generation

The SCU module provides 3 service request outputs SR[2:0]. SR0 is for system critical request, such as loss of clock event. SR1 is for the common SCU request such as DTS request. SR2 is for ACMP and ORC requests. The service request outputs SR[2:0] are connected to interrupt nodes in the Nested Vectored Interrupt Controller (NVIC).

Refer to ***Chapter 14.2.1*** for more details.

14.7 Debug Behavior

The SCU module does not get affected with the HALTED signal from SCU upon debug activities performed using external debug probe.

14.8 Power, Reset and Clock

The SCU module implements functions that involve varoius types of modules controlled directly or via dedicated interfaces that are instantiated in different power, clock and reset domains. These modules are functionally considered parts of the SCU and therefore SCU is also considered a multi domain circuit in this sense.

Power domains:

Power domains get separated with appropriate power separation cells.

- Core domain supplied with V_{DDC} voltage
- Pad domain supplied with V_{DDP} voltage

Clock domains:

All cross-domain interfaces implement signal synchchronization.

- internal SCU clock is MCLK, always identical to the CPU clock
- RTC and register mirror interface clock is 32.786 kHz clock generated from DCO2 oscillator

Reset domains:

All resets get internally synchronized to respective clocks.

- System Reset ($\overline{\text{SYSRESET}}$) resets most of the logics in SCU and can be triggered from various sources (please refer to ***Reset Control (RCU)*** section for more details)
- Master Reset ($\overline{\text{MRESET}}$) contributes in generation of the System Reset and gets triggered upon power-up sequence of the Core domain

14.9 Registers

This section describes the registers of SCU which some of them resides in the ANACTRL module. Most of the registers are reset by $\overline{\text{SYSRESET}}$ reset signal but some of the registers can be reset only with power-on reset. SCU registers are accessible via the AHB-lite bus. ANACTRL registers are accessible via the APB bus. ANACTRL registers have name starting with “ANA”.

Table 172 Base Addresses of sub-sections of SCU registers

Short Name	Description	Offset Addr.[30)]
GCU Registers	Offset address of General Control Unit	0000_H
PCU Registers	Offset address of Power Control Unit	0200_H
CCU Registers	Offset address of Clock Control Unit	0300_H
RCU Registers	Offset address of Reset Control Unit	0400_H
RTC Registers	Offset address of Real Time Clock Module	$0A00_H$
ANACTRL Registers	Offset address of ANACTRL registers	1000_H

Following access to SCU/ANACTRL SFRs result in an AHB/APB error response:

- Read or write access to undefined address
- Write access to read-only registers
- Write access to startup protected registers

30 The absolute register address is calculated as follows: Module Base Address + Sub-Module Offset Address (shown in this column) + Register Offset Address

Table 173 Registers Address Space

Module	Base Address	End Address	Note
SCU	4001 0000$_H$	4001 FFFF$_H$	System Control Unit Registers

Table 174 Registers Overview

Short Name	Description	Offset Addr.[31]	Access Mode		Description See
			Read	Write	
PCU Registers (ANACTRL)					
ANAVDEL	Voltage Detector Control register	0050$_H$	U, PV	U, PV	Page 255
PCU Registers (SCU)					
VDESR	Voltage Detector Status Register	0000$_H$	U, PV	U, PV	Page 256
CCU Registers (SCU)					
CLKCR	Clock Control Register	0000$_H$	U, PV	U, PV, BP	Page 257
CLKCR1	Clock Control Register 1	001C$_H$	U, PV	U, PV, BP	Page 259
PWRSVCR	Power Save Control Register	0004$_H$	U, PV	U, PV	Page 260
CGATSTAT0	Clock Gating Status for Peripherals 0	0008$_H$	U, PV	U, PV	Page 260
CGATSET0	Clock Gating Set for Peripherals 0	000C$_H$	U, PV	U, PV, BP	Page 262
CGATCLR0	Clock Gating Clear for Peripherals 0	0010$_H$	U, PV	U, PV, BP	Page 264
OSCCSR	Oscillator Control and Status Register	0014$_H$	U, PV	U, PV	Page 265
CCU Registers (ANACTRL)					
ANAOFFSET	DCO1 Offset Register	106C$_H$	U, PV	U, PV, BP	Page 267
ANASYNC1	DCO1 Sync Control Register 1	1078$_H$	U, PV	U,PV	Page 269

31 The absolute register address is calculated as follows: Module Base Address + Sub-Module Offset Address + Offset Address (shown in this column)

Table 174 Registers Overview (continued)

Short Name	Description	Offset Addr.[31]	Access Mode		Description See
			Read	Write	
ANASYNC2	DCO1 Sync Control Register 2	$107C_H$	U, PV	U,PV	Page 270
ANAOSCLPCTRL	OSC_LP Control Register	$108C_H$	U, PV	U,PV	Page 267
ANAOSCHPCTRL	OSC_HP Control Register	1090_H	U, PV	U,PV.BP	Page 268
RCU Registers (SCU)					
RSTSTAT	Reset Status	0000_H	U, PV	BE	Page 271
RSTSET	Reset Set Register	0004_H	U, PV	U, PV	Page 272
RSTCLR	Reset Clear Register	0008_H	U, PV	U, PV	Page 272
RSTCON	Reset Control Register	$000C_H$	U, PV	U, PV	Page 273
GCU Registers (SCU)					
ID	Module Identification Register	0008_H	U, PV	BE	Page 274
IDCHIP	Chip ID	0004_H	U, PV	U, PV	Page 274
DBGROMID	DBGROMID	0000_H	U, PV	U, PV	Page 275
SSW0	SSW Support Register	0014_H	U, PV	U, PV	Page 276
CCUCON	CCUx Global Start Control Register	0030_H	U, PV	U, PV	Page 276
SRRAW	RAW Service Request Status	0038_H	U, PV	BE	Page 277
SRMSK	Service Request Mask	$003C_H$	U, PV	U, PV	Page 280
SRCLR	Service Request Clear	0040_H	U, PV	U, PV	Page 282
SRSET	Service Request Set	0044_H	U, PV	U, PV	Page 284
SRRAW1	RAW Service Request Status 1	0058_H	U, PV	BE	Page 286

31 The absolute register address is calculated as follows: Module Base Address + Sub-Module Offset Address + Offset Address (shown in this column)

Table 174 Registers Overview (continued)

Short Name	Description	Offset Addr.[31]	Access Mode		Description See
			Read	Write	
SRMSK1	Service Request Mask 1	$005C_H$	U, PV	U, PV	Page 287
SRCLR1	Service Request Clear 1	0060_H	U, PV	U, PV	Page 288
SRSET1	Service Request Set 1	0064_H	U, PV	U, PV	Page 289
PASSWD	Bit protection Register 1	0024_H	U, PV	U, PV	Page 290
MIRRSTS	Mirror Update Status Register	0048_H	U, PV	BE	Page 291
PMTSR	Parity Memory Test Select Register	0054_H	U, PV	U, PV	Page 291>
PFUCR	Prefetch Unit Control Register	0068_H	U, PV	U, PV	Page 292
INTCR0	Interrupt Control Register 0	$006C_H$	U, PV	U, PV	Page 292
INTCR1	Interrupt Control Register 1	0070_H	U, PV	U, PV	Page 293
STSTAT	Startup Status Register	0074_H	U, PV	U, PV	Page 293

14.9.1 PCU Registers (ANACTRL)

14.9.1.1 Register ANAVDEL

Voltage Detector Control register.

ANAVDEL Address: 1050_H

Voltage Detector Control Register Reset Value: $001C_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0											VDEL_EN	VDEL_TIM_ADJ		VDEL_SELECT	
r											rw	rw		rw	

31 The absolute register address is calculated as follows: Module Base Address + Sub-Module Offset Address + Offset Address (shown in this column)

Field	Bits	Type	Description
VDEL_SELECT	1:0	rw	**VDEL Range Select** With these bits the VDDP range is set. 00_B 2.25V 01_B 3.0V 10_B 4.4V
VDEL_TIM_ADJ	3:2	rw	**VDEL Timing Setting** These bits control the reaction speed of the VDEL. The value is determined by characterisation. 00_B typ 1µs - slowest response time 01_B typ 500n 10_B typ 250n 11_B no delay - fastest response time.
VDEL_EN	4	rw	**VDEL unit Enable** 0_B VDEL is disabled 1_B VDEL is active
0	15:5	r	**Reserved** Read as 0; should be written with 0.

14.9.2 PCU Registers (SCU)

14.9.2.1 Register VDESR

Voltage Detector status register.

VDESR Address: 0200_H

Voltage Detector Status Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0														**VDDPPW**	**VCLIP**
r														rh	rh

Field	Bits	Type	Description
VCLIP	0	rh	**VCLIP Indication** VCLIP monitoring bit. 0_B VCLIP is not active 1_B VCLIP is active

(continued)

Field	Bits	Type	Description
VDDPPW	1	rh	**VDDPPW Indication** 0_B VDDP is above pre-warning threshold 1_B VDDP is below pre-warningthreshold
0	31:2	r	**Reserved** Read as 0; should be written with 0.

14.9.3 CCU Registers (SCU)

14.9.3.1 Register CLKCR

Clock control register.

CLKCR Address: 0300_H

Clock Control Register Reset Value: $3000\ 0600_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VDDC2HIGH	**VDDC2LOW**	**CNTADJ**										**RTCCLKSEL**			**PCLKSEL**
rh	rh	rw										rw			rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IDIV								**FDIV**							
rw								rw							

Field	Bits	Type	Description
FDIV	7:0	rw	**Fractional Divider Selection, FDIV[7:0]** FDIV is a 10-bit value. CLKCR1[1:0] and CLKCR[7:0] are concatenated to form the FDIV[9:0]. Selects the fractional divider to be n/1024, where n is the value of FDIV and is in the range of 0 to 1023. For example, writing 001_H to FDIV selects the fractional divider to be 1/1024. This bit is protected by the bit protection scheme as described in Memory Organization chapter *Note: Fractional divider has no effect if IDIV = 00_H .*

(continued)

Field	Bits	Type	Description
IDIV	15:8	rw	**Divider Selection** 00_H Divider is bypassed. 01_H 1; 02_H 2; 03_H 3; 04_H 4; FE_H 254; FF_H 255; Refer to ***Table 168*** for some examples of MCLK frequency based on the value of IDIV. This bit is protected by the bit protection scheme as described in Memory Organization chapter
PCLKSEL	16	rw	**PCLK Clock Select** 0_B PCLK = MCLK 1_B PCLK = 2 x MCLK This bit is protected by the bit protection scheme as described in Memory Organization chapter *Note: Do not select option PCLK = 2 x MCLK when the clock source is in external direct-in mode clock mode (CLKCR1.DCLKSEL = 1_B and OSCHPCTRL.MODE = 10_B).*
RTCCLKSEL	19:17	rw	**RTC Clock Select** 000_B 32kHz standby clock 001_B 32.768kHz external clock from ERU0.IOUT0 010_B 32.768kHz external clock from ACMP0.OUT 011_B 32.768kHz external clock from ACMP1.OUT 100_B 32.768kHz external clock from ACMP2.OUT 101_B 32.768kHz XTAL clock via OSC_LP 110_B Reserved 111_B Reserved This bit is protected by the bit protection scheme as described in Memory Organization chapter.
CNTADJ	29:20	rw	**Counter Adjustment** 000_H 1 clock cycles of the DCO1, 48MHz clock 001_H 2 clock cycles of the DCO1, 48MHz clock 002_H 3 clock cycles of the DCO1, 48MHz clock 003_H 4 clock cycles of the DCO1, 48MHz clock 004_H 5 clock cycles of the DCO1, 48MHz clock 300_H 769 clock cycles of the DCO1, 48MHz clock $3FE_H$ 1023 clock cycles of the DCO1, 48MHz clock $3FF_H$ 1024 clock cycles of the DCO1, 48MHz clock Note: DCO1 must be enabled for counting the time that is needed to have a stable V_{DDC} after a VDROP or VCLIP event happens.

(continued)

Field	Bits	Type	Description
VDDC2LOW	30	rh	**VDDC too low** 0_B VDDC is not too low and the fractional divider input clock is running at the targeted frequency 1_B VDDC is too low and the fractional divider input clock is not running at the targeted frequency
VDDC2HIGH	31	rh	**VDDC too high** 0_B VDDC is not too high 1_B VDDC is too high

14.9.3.2 Register CLKCR1

Clock control register 1

CLKCR1 Address: $031C_H$

Clock Control Register 1 Reset Value: $0000\ 0100_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0						DCLKSEL	ADCCLKSEL	0						FDIV	
r						rw	rw	r						rw	

Field	Bits	Type	Description
FDIV	1:0	rw	**Fractional Divider Selection, FDIV[9:8]** FDIV is a 10-bit value. CLKCR1[1:0] and CLKCR[7:0] are concatenated to form the FDIV[9:0]. Selects the fractional divider to be n/1024, where n is the value of FDIV and is in the range of 0 to 1023. For example, writing 001_H to FDIV selects the fractional divider to be 1/1024. This bit is protected by the bit protection scheme as described in Memory Organization chapter *Note: Fractional divider has no effect if IDIV = 00_H .*
ADCCLKSEL	8	rw	**ADC Converter Clock Select** 0_B f_{CONV} = 48MHz 1_B f_{CONV} = 32MHz This bit is protected by the bit protection scheme as described in Memory Organization chapter

(continued)

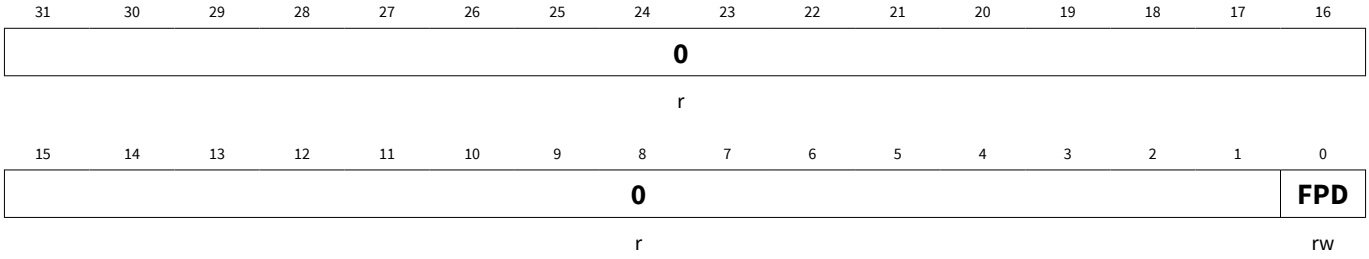
Field	Bits	Type	Description
DCLKSEL	9	rw	**Doubler Clock Source Select** 0_B DCO1 1_B External clock via OSC_HP This bit is protected by the bit protection scheme as described in Memory Organization chapter
0	7:2,31:10	r	**Reserved** Read as 0.

14.9.3.3 Register PWRSVCR

Configuration register that defines some system behaviour aspects while in deep-sleep mode or sleep mode. The original system state gets restored upon wakeup from sleep mode or deep-sleep mode.

PWRSVCR Address: 0304_H

Power Save Control Register Reset Value: $0000\ 0000_H$



Field	Bits	Type	Description
FPD	0	rw	**Flash Power Down** 0_B no effect 1_B Flash power down when entering power save mode. Upon wake-up, CPU is able to fetch code from flash.
0	31:1	r	**Reserved** Read as 0.

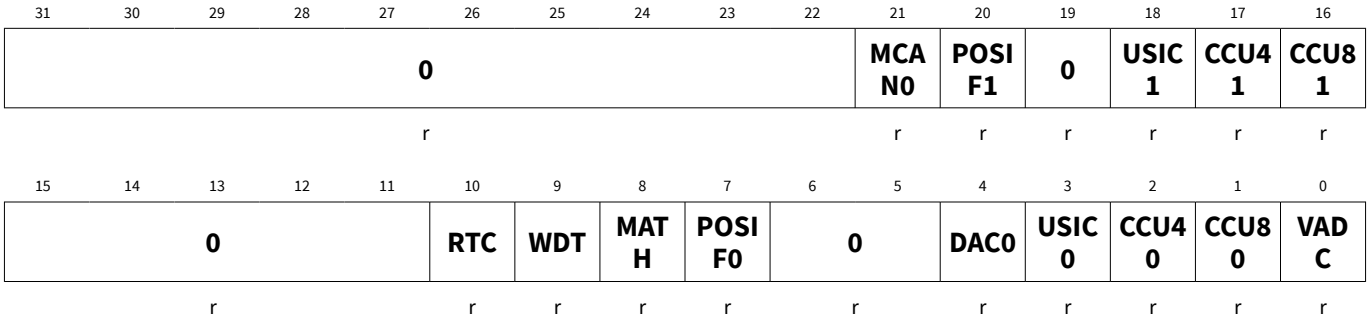
14.9.3.4 Register CGATSTAT0

Clock gating status for IMC300A peripherals. After reset, all peripherals as listed in the registers are not running. Their module clock are gated.

Every bit in this register is protected by the bit protection scheme as described in Memory Organization chapter.

CGATSTAT0 Address: 0308_H

Peripheral 0 Clock Gating Status Reset Value: $003F\ 07FF_H$



Field	Bits	Type	Description
VADC	0	r	**VADC and SHS Gating Status** 0_B gating de-asserted 1_B gating asserted
CCU80	1	r	**CCU80 Gating Status** 0_B gating de-asserted 1_B gating asserted
CCU40	2	r	**CCU40 Gating Status** 0_B gating de-asserted 1_B gating asserted
USIC0	3	r	**USIC0 Gating Status** 0_B gating de-asserted 1_B gating asserted
DAC0	4	r	**DAC0 Gating Status** 0_B gating de-asserted 1_B gating asserted
POSIF0	7	r	**POSIF0 Gating Status** 0_B gating de-asserted 1_B gating asserted
MATH	8	r	**MATH Gating Status** 0_B gating de-asserted 1_B gating asserted
WDT	9	r	**WDT Gating Status** 0_B gating de-asserted 1_B gating asserted
RTC	10	r	**RTC Gating Status** 0_B gating de-asserted 1_B gating asserted
CCU81	16	r	**CCU81 Gating Status** 0_B gating de-asserted 1_B gating asserted

(continued)

Field	Bits	Type	Description
CCU41	17	r	**CCU41 Gating Status** 0_B gating de-asserted 1_B gating asserted
USIC1	18	r	**USIC1 Gating Status** 0_B gating de-asserted 1_B gating asserted
POSIF1	20	r	**POSIF1 Gating Status** 0_B gating de-asserted 1_B gating asserted
MCAN0	21	r	**MultiCAN Gating Status** 0_B gating de-asserted 1_B gating asserted
0	6:5, 15:11, 19, 31:22	r	**Reserved**

14.9.3.5 Register CGATSET0

Clock gating enable for IMC300A peripherals. Write one to selected bit to enable gating of corresponding clock, writing zeros has no effect.

Every bit in this register is protected by the bit protection scheme as described in Memory Organization chapter.

CGATSET0 Address: $030C_H$

Peripheral 0 Clock Gating Set Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0										MCAN0	POSIF1	0	USIC1	CCU41	CCU81
r										w	w	r	w	w	w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0					RTC	WDT	MATH	POSIF0	0		DAC0	USIC0	CCU40	CCU80	VADC
r					w	w	w	w	r		w	w	w	w	w

Field	Bits	Type	Description
VADC	0	w	**VADC and SHS Gating Set** 0_B no effect 1_B enable gating
CCU80	1	w	**CCU80 Gating Set** 0_B no effect 1_B enable gating

(continued)

Field	Bits	Type	Description
CCU40	2	w	**CCU40 Gating Set** 0_B no effect 1_B enable gating
USIC0	3	w	**USIC0 Gating Set** 0_B no effect 1_B enable gating
DAC0	4	w	**DAC0 Gating Set** 0_B no effect 1_B enable gating
POSIF0	7	w	**POSIF0 Gating Set** 0_B no effect 1_B enable gating
MATH	8	w	**MATH Gating Set** 0_B no effect 1_B enable gating
WDT	9	w	**WDT Gating Set** 0_B no effect 1_B enable gating
RTC	10	w	**RTC Gating Set** 0_B no effect 1_B enable gating
CCU81	16	w	**CCU81 Gating Set** 0_B no effect 1_B enable gating
CCU41	17	w	**CCU41 Gating Set** 0_B no effect 1_B enable gating
USIC1	18	w	**USIC1 Gating Set** 0_B no effect 1_B enable gating
POSIF1	20	w	**POSIF1 Gating Set** 0_B no effect 1_B enable gating
MCAN0	21	w	**MutliCAN Gating Set** 0_B no effect 1_B enable gating
0	6:5, 15:11, 19, 31:22	r	**Reserved**

14.9.3.6 Register CGATCLR0

Clock gating disable for IMC300A peripherals. Write one to selected bit to disable gating of corresponding clock, writing zeros has no effect.

CGATCLR0 Address: 0310_H

Peripheral 0 Clock Gating Clear Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0										MCAN0	POSIF1	0	USIC1	CCU41	CCU81
r										w	w	r	w	w	w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0					RTC	WDT	MATH	POSIF0	0		DAC0	USIC0	CCU40	CCU80	VADC
r					w	w	w	w	r		w	w	w	w	w

Field	Bits	Type	Description
VADC	0	w	**VADC and SHS Gating Clear** 0_B no effect 1_B disable gating
CCU80	1	w	**CCU80 Gating Clear** 0_B no effect 1_B disble gating
CCU40	2	w	**CCU40 Gating Clear** 0_B no effect 1_B disable gating
USIC0	3	w	**USIC0 Gating Clear** 0_B no effect 1_B disable gating
DAC0	4	w	**DAC0 Gating Clear** 0_B no effect 1_B disable gating
POSIF0	7	w	**POSIF0 Gating Clear** 0_B no effect 1_B disable gating
MATH	8	w	**MATH Gating Clear** 0_B no effect 1_B disable gating
WDT	9	w	**WDT Gating Clear** 0_B no effect 1_B disable gating

(continued)

Field	Bits	Type	Description
RTC	10	w	**RTC Gating Clear** 0_B no effect 1_B disable gating
CCU81	16	w	**CCU81 Gating Clear** 0_B no effect 1_B disble gating
CCU41	17	w	**CCU41 Gating Clear** 0_B no effect 1_B disable gating
USIC1	18	w	**USIC1 Gating Clear** 0_B no effect 1_B disable gating
POSIF1	20	w	**POSIF1 Gating Clear** 0_B no effect 1_B disable gating
MCAN0	21	w	**MutliCAN Gating Clear** 0_B no effect 1_B disable gating
0	6:5, 15:11, 19, 31:22	r	**Reserved**

14.9.3.7 Register OSCCSR

Oscillator Control and Status Register.

OSCCSR Address: 0314_H

Oscillator Control and Status Register Reset Value: $0000\ 000X_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0						**XOWDEN**	**XOWDRES**	**0**						**OWDEN**	**OWDRES**
r						rw	rwh	r						rw	rwh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0							**DCO1PD**	**0**						**OSC2H**	**OSC2L**
r							rw	r						rh	rh

Field	Bits	Type	Description
OSC2L	0	rh	**Oscillator Valid Low Status Bit** This bit indicates if the frequency output of OSC is usable. This is checked by the Oscillator Watchdog 0_B The OSC frequency is usable 1_B The OSC frequency is not usable. Frequency is too low.
OSC2H	1	rh	**Oscillator Valid High Status Bit** This bit indicates if the frequency output of OSC is usable. This is checked by the Oscillator Watchdog. 0_B The OSC frequency is usable 1_B The OSC frequency is not usable. Frequency is too high.
DCO1PD	8	rw	**DCO1 Power down** This bit is protected by the bit protection scheme as described in Memory Organization chapter 0_B DCO1 is not power down 1_B DCO1 power down. *Note: This bit must be set to 0 when debug system via SPD or ADC is enabled.*
OWDRES	16	rwh	**Oscillator Watchdog Reset** Setting this bit will restart the oscillator detection. This bit will be automatically reset to 0 after OWD is reset which takes 2 standby clock cycles due to synchronisation. 0_B The Oscillator Watchdog is not cleared and remains active 1_B The Oscillator Watchdog is cleared and restarted. The OSC2L and OSC2H flag will be held in the last value until it is updated after 3 standby clock cycles.
OWDEN	17	rw	**Oscillator Watchdog Enable** 0_B The Oscillator Watchdog is disabled 1_B The Oscillator Watchdog is enabled *Note: OSC2H and OSC2L will be cleared to 0 when OWD is disabled.*
XOWDRES	24	rwh	**XTAL Oscillator Watchdog Reset** Setting this bit will restart the oscillator detection. This bit will be automatically reset to 0 after XOWD is reset which takes 2 standby clock cycles due to synchronisation. 0_B The Oscillator Watchdog is not cleared and remains active 1_B The Oscillator Watchdog is cleared and restarted.
XOWDEN	25	rw	**XTAL Oscillator Watchdog Enable** 0_B The XTAL Oscillator Watchdog is disabled 1_B The XTAL Oscillator Watchdog is enabled
0	7:2, 15:9,23:18, 31:26	r	**Reserved** Read as 0.

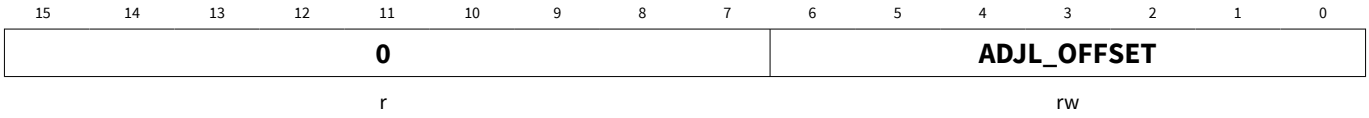
14.9.4 CCU Registers (ANACTRL)

14.9.4.1 Register ANAOFFSET

DCO1 Offset register.
User is able to use bit ADJL_OFFSET to calibrate the DCO1 based on the temperature.

ANAOFFSET Address: $106C_H$

DCO1 Offset Register Reset Value: 0040_H



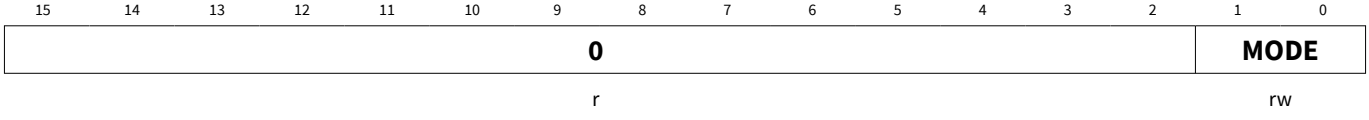
Field	Bits	Type	Description
ADJL_OFFSET	6:0	rw	**ADJL Offset register** The adjusted oscillator frequency can be varied according to the steps programmed. This bit is protected by the bit protection scheme as described in Memory Organization chapter ... $3F_H$ DCO1 calibration value is reduced by 1 step 40_H 0, default 41_H DCO1 calibration value is increased by 1 step ...
0	15:7	r	**Reserved** Read as 0; should be written with 0.

14.9.4.2 Register ANAOSCLPCTRL

OSC_LP oscillator control register.

ANAOSCLPCTRL Address: $108C_H$

OSC_LP Control Register Reset Value: 0003_H



Field	Bits	Type	Description
MODE	1:0	rw	**OSC_LP Oscillator Mode** 00_B Oscillator is enabled and in operation mode (OSC mode) 01_B Reserved 10_B Reserved 11_B Oscillator is in power down mode , Pad can be used in GPIO mode
0	15:2	r	**Reserved** Read as 0; should be written with 0.

14.9.4.3 Register ANAOSCHPCTRL

OSC_HP oscillator control register.
Every bit in this register is protected by the bit protection scheme as described in Memory Organization chapter

ANAOSCHPCTRL Address: 1090_H
OSC_HP Control Register Reset Value: 0038_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0									HYSCTRL	MODE		GAINSEL		SHBY	0
r									rw	rw		rw		rw	r

Field	Bits	Type	Description
SHBY	1	rw	**Shaper Bypass Mode** This bit is protected by the bit protection scheme as described in Memory Organization chapter 0_B The shaper is not bypassed 1_B The shaper is bypassed *Note: For the OSC_HP pad to function in GPIO mode , user must set SHBY = 0 and MODE = 11.* *Note: When shaper function is enable (MODE=0x), shaper should be in non-bypass mode (SHBY=0).*
GAINSEL	3:2	rw	**OSC_HP Oscillator Gain Selection** This bit is protected by the bit protection scheme as described in Memory Organization chapter 00_B Gain control is configured for frequencies from 4 MHz to y1 MHz 01_B Gain control is configured for frequencies from 4 MHz to y2 MHz 10_B Gain control is configured for frequencies from 4 MHz to 20 MHz 11_B Reserved

(continued)

Field	Bits	Type	Description
MODE	5:4	rw	**OSC_HP Oscillator Mode** This bit is protected by the bit protection scheme as described in Memory Organization chapter 00_B Oscillator is enabled and in active power mode with shaper enabled (OSC mode) 01_B Oscillator in power down mode with shaper enabled (External Clock Input Mode). 10_B Oscillator is enabled with shaper disabled. No clock output is available unless the shaper is bypass (SHBY=1) 11_B Oscillator is in power down mode with shaper disabled. Pad can be used in GPIO mode. *Note: For the OSC_HP pad to function in GPIO mode , user must set SHBY = 0 and MODE = 11.* *Note: When shaper function is enable (MODE=0x), shaper should be in non-bypass mode (SHBY=0)*
HYSCTRL	6	rw	**Shaper Hystersis Mode** This bit is protected by the bit protection scheme as described in Memory Organization chapter 0_B External clock frequency < 20MHz. 1_B External clock frequency > 20MHz
0	0, 15:7	r	**Reserved** Read as 0; should be written with 0.

14.9.4.4 Register ANASYNC1

DCO1 Sync Control register. DCO1 clock synchronization unit - prescaler section. All the bits in ANASYNC1 are protected by the bit protection scheme as described in Memory Organization chapter.

ANASYNC1 Address: 1078_H

DCO1 Sync Control Register 1 Reset Value: $0B72_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XTAL_SEL	**SYNC_DCO_EN**	**SYNC_PRELOAD**													
rw	rw	rw													

Field	Bits	Type	Description
SYNC_PRELOAD	13:0	rw	**Counter target value, which defines the update cycle** Together with the bit field PRESCALER, this SFR field defines the DCO1 target frequency. This counter value has to be calculated according to the external clock frequency and prescaler value. For the recommended value for a 32.768kHz OSC_LP oscillator please refer to ***Table 170***.
SYNC_DCO_EN	14	rw	**DCO1 synchronization feature enable** 0_B No DCO1 synchronization via an external clock source. This option is used for the DCO1 calibration using the temperature sensor. 1_B DCO1 gets synchronized via an external clock source.
XTAL_SEL	15	rw	**Oscillator Source select** Selects the oscillator as frequency source which gets routed to the prescaler 0_B OSC_LP is selected 1_B OSC_HP is selected

14.9.4.5 Register ANASYNC2

DCO1 Sync Control register 2. DCO1 clock synchronization unit - prescaler section. All the bits in ANASYNC2 are protected by the bit protection scheme as described in Memory Organization chapter.

ANASYNC2 Address: $107C_H$

DCO1 Sync Control Register 2 Reset Value: 0002_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0			**SYNC_READY**	**0**	**PRESCALER**										
r			r	r	rw										

Field	Bits	Type	Description
PRESCALER	10:0	rw	**Prescaler value** The selected external frequency gets divided by this prescaler level. For the recommended value for a 32.768kHz OSC_LP oscillator please refer to ***Table 170***. 000_H Bypass: Internal sync counter frequency = crystal frequency 001_H DIV1: Internal sync counter feed freq. = crystal frequency/1 002_H DIV2: Internal sync counter feed freq. = crystal frequency/2 $7FF_H$ Maximum divider value (for best accuracy, but slowest response)

(continued)

Field	Bits	Type	Description
SYNC_READY	12	r	**DCO1 frequency reached its target value** If the DCO1 frequency is close to its target frequency, this bit has to be set. 0_B Actual DCO1 frequency is out of targe 1_B DCO1 is synchronized to the XTAL frequency *Note: This bit is set to low after the synchronisation unit is enabled via (ANASYNC1.SYNC_DCO_EN=1). It is updated after each synchronisation cycle*
0	11,15:13	r	**Reserved** Read as 0; should be written with 0.

14.9.5 RCU Registers (SCU)

14.9.5.1 Register RSTSTAT

Reset status register. This register needs to be checked after system startup in order to determine last reset reason. User should clear this register after reading it to ensure a clear status when the next reset happen. This register is reset by a power-on reset.

RSTSTAT Address: 0400_H

RCU Reset Status Reset Value: $0000\ 0XXX_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0					LCKEN	RSTSTAT									
r					r	rh									

Field	Bits	Type	Description
RSTSTAT	9:0	rh	**Reset Status Information** Provides reason of last reset 0000000001_B Power on reset or Brownout reset $XXXXXXXX1X_B$ Master reset via bit RSTCON.MRSTEN $XXXXXXX1XX_B$ CPU system reset request $XXXXXX1XXX_B$ CPU lockup reset $XXXXX1XXXX_B$ Flash ECC reset $XXXX1XXXXX_B$ WDT reset $XXX1XXXXXX_B$ Loss of MCLK/PCLK clock reset $XX1XXXXXXX_B$ Parity Error reset

(continued)

Field	Bits	Type	Description
LCKEN	10	r	**Enable Lockup Status** 0_B Reset by Lockup disabled 1_B Reset by Lockup enabled
0	31:11	r	**Reserved**

14.9.5.2 Register RSTSET

Selective configuration of reset behaviour in the system. Write one to set selected bit, writing zeros has no effect.

RSTSET Address: 0404_H

RCU Reset Set Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0					LCKEN	0									
r					w	r									

Field	Bits	Type	Description
LCKEN	10	w	**Enable Lockup Reset** 0_B no effect 1_B Enable reset when Lockup gets asserted
0	9:0, 31:11	r	**Reserved**

14.9.5.3 Register RSTCLR

Selective configuration of reset behaviour in the system. Write one to clear selected bit, writing zeros has no effect.

RSTCLR Address: 0408_H

RCU Reset Clear Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0					LCKEN	0									RSCLR
r					w	r									w

Field	Bits	Type	Description
RSCLR	0	w	**Clear Reset Status** 0_B no effect 1_B Clears field ***RSTSTAT***.RSTSTAT
LCKEN	10	w	**Enable Lockup Reset** 0_B no effect 1_B Disable reset when Lockup gets asserted
0	9:1,31:11	r	**Reserved**

14.9.5.4 Register RSTCON

Enabling of reset triggered by critical events. It is reset by any reset type.

RSTCON Address: $040C_H$

RCU Reset Control Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															MRSTEN
r															w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0									LOECRSTEN	MPERSTEN	U1PERSTEN	U0PERSTEN	SPERSTEN	LOCRSTEN	ECCRSTEN
r									rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
ECCRSTEN	0	rw	**Enable ECC Error Reset** 0_B No reset when ECC double bit error occur 1_B Reset when ECC double bit error occur
LOCRSTEN	1	rw	**Enable Loss of DCO1 Clock Reset** 0_B No reset when loss of DCO1 clock occur 1_B Reset when loss of DCO1 clock occur
SPERSTEN	2	rw	**Enable 16kbytes SRAM Parity Error Reset** 0_B No reset when SRAM parity error occur 1_B Reset when SRAM parity error occur
U0PERSTEN	3	rw	**Enable USIC0 SRAM Parity Error Reset** 0_B No reset when USIC0 memory parity error occur 1_B Reset when USIC0 memory parity error occur
U1PERSTEN	4	rw	**Enable USIC01 SRAM Parity Error Reset** 0_B No reset when USIC1 memory parity error occur 1_B Reset when USIC1 memory parity error occur

(continued)

Field	Bits	Type	Description
MPERSTEN	5	rw	**Enable MultiCAN+SRAM Parity Error Reset** 0_B No reset when MultiCAN+ memory parity error occur 1_B Reset when MultiCAN+ memory parity error occur
LOECRSTEN	6	rw	**Enable Loss of External Clock Reset** 0_B No reset when loss of external clock occur 1_B Reset when loss of external clock occur
MRSTEN	16	w	**Enable Master Reset** 0_B No effect 1_B Triggered Master reset
0	15:7, 31:17	r	**Reserved**

14.9.6 GCU Registers (SCU)

14.9.6.1 Register ID

Register containing uniques ID of the module.

ID Address: 0008_H

SCU Module ID Register Reset Value: 00F4 C0XX$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MOD_NUMBER															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOD_TYPE								MOD_REV							
r								r							

Field	Bits	Type	Description
MOD_REV	7:0	r	**Module Revision Number** MOD_REV defines the revision number. The value of a module revision starts with 01_H (first revision).
MOD_TYPE	15:8	r	**Module Type** This bit field is $C0_H$. It defines the module as a 32-bit module.
MOD_NUMBER	31:16	r	**Module Number Value** This bit field defines the module identification number.

14.9.6.2 Register IDCHIP

Register containing a unique ID of the chip in the device family. The value of this register formed part of the chip identification number as described in ***Chip Identification Number***.

IDCHIP Address: 0004_H

Chip ID Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IDCHIP															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IDCHIP															
r															

Field	Bits	Type	Description
IDCHIP	31:0	r	**CHIP ID** 1XXX X00X_HIMC Family 1XXX X00X_HIMD Family 3XXX XXXX$_H$IMM Family 4XXX XXXX$_H$IMI Family X1NN XXXX$_H$ 100 Series X3NN XXXX$_H$ 300 Series XXXX 1XXX$_H$ API firmware XXXX 2XXX$_H$ Custom firmware 1XXX XXX5$_H$ TSSOP38 pin package 1XXX XXX6$_H$ QFP48 pin package 1XXX XXXA$_H$ QFN64 pin package 1XXX XXXB$_H$ QFP64 pin package 1XXX XXXD$_H$ QFP100 pin package 2XXX XXX7$_H$ QFP40 pin package 3XXX XXX0$_H$ PQFN package Others Reserved

14.9.6.3 Register DBGROMID

Register containing unique manufactory ID, part number and the design stepping code of the chip.

DBGROMID Address: 0000_H

Debug System ROM ID Register Reset Value: $1020\ 4083_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VERSION				**PARTNO**											
r				r											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PARTNO				**MANUFID**											**1**
r				r											r

Field	Bits	Type	Description
MANUFID	11:1	r	**Manufactory Identity**
PARTNO	27:12	r	**Part Number**
VERSION	31:28	r	**Product version**
1	0	r	**Reserved** Read as 1; should be written with 1.

14.9.6.4 Register SSW0

Software support registers.
SSW0 is used to change the BMI value.

SSW0 Address: 0014_H

SSW Register 0 Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DAT															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAT															
rw															

Field	Bits	Type	Description
DAT	31:0	rw	**SSW Data** *Note: SSW registers can be reset with master reset only*

14.9.6.5 Register CCUCON

CAPCOM module control register.

CCUCON Address: 0030_H

CCU Control Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0						**GSC81**	**GSC80**	**0**						**GSC41**	**GSC40**
r						rw	rw	r						rw	rw

Field	Bits	Type	Description
GSC40	0	rw	**Global Start Control CCU40** This register can be used to control a synchronous start of multiple timers of CCU40. It also can be used to control additional functions that are available in the timers, e.g. Count or Capture. For a complete description of the available set of functions, please address the specific section of the CCU4 chapters. Writing 1 or 0 into this field will not by itself trigger a synchronous start of multiple timers and one must before configure the specific peripheral function accordingly.
GSC41	1	rw	**Global Start Control CCU41** This register can be used to control a synchronous start of multiple timers of CCU41. It also can be used to control additional functions that are available in the timers, e.g. Count or Capture. For a complete description of the available set of functions, please address the specific section of the CCU4 chapters. Writing 1 or 0 into this field will not by itself trigger a synchronous start of multiple timers and one must before configure the specific peripheral function accordingly.
GSC80	8	rw	**Global Start Control CCU80** This register can be used to control a synchronous start of multiple timers of CCU80. It also can be used to control additional functions that are available in the timers, e.g. Count or Capture. For a complete description of the available set of functions, please address the specific section of the CCU8 chapters. Writing 1 or 0 into this field will not by itself trigger a synchronous start of multiple timers and one must before configure the specific peripheral function accordingly.
GSC81	9	rw	**Global Start Control CCU81** This register can be used to control a synchronous start of multiple timers of CCU81. It also can be used to control additional functions that are available in the timers, e.g. Count or Capture. For a complete description of the available set of functions, please address the specific section of the CCU8 chapters. Writing 1 or 0 into this field will not by itself trigger a synchronous start of multiple timers and one must before configure the specific peripheral function accordingly.
0	7:2,31:10	r	**Reserved** Read as 0; should be written with 0.

14.9.6.6 Register SRRAW

Service request status without masking. Write one to a bit in SRCLR register to clear a bit or SRSET to set a bit. Writing zero has no effect.

SRRAW Address: 0038_H

SCU Raw Service Request Status Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TSE_LOW	**TSE_HIGH**	**TSE_DONE**	**RTC_TIM1**	**RTC_TIM0**	**RTC_ATIM1**	**RTC_ATIM0**	**RTC_CTR**	**0**	**SBYCLKFI**	**VCLIPI**	**FLCMPLTI**	**FLEC2I**	**PEU0I**	**PESRAMI**	**LOCI**
rh	rh	rh	rh	rh	rh	rh	rh	r	rh	rh	rh	rh	rh	rh	rh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**ORC6I**	**0**	**ORC4I**	**0**	**0**	**0**	**ORC0I**	**VDROPI**	**ACMP2I**	**ACMP1I**	**ACMP0I**	**VDDPI**	**AI**	**PI**	**PRWARN**
r	rh	r	rh	r	r	r	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
PRWARN	0	rh	**WDT pre-warning Event Status Before Masking** 0_B Event has not occurred 1_B Event has occurred
PI	1	rh	**RTC Raw Periodic Event Status Before Masking** 0_B Event has not occurred 1_B Event has occurred
AI	2	rh	**RTC Raw Alarm Event Status Before Masking** 0_B Event has not occurred 1_B Event has occurred
VDDPI	3	rh	**VDDP pre-warning Event Status Before Masking** 0_B Event has not occurred 1_B Event has occurred
ACMP0I	4	rh	**Analog Comparator 0 Event Status Before Masking** 0_B Event has not occurred 1_B Event has occurred
ACMP1I	5	rh	**Analog Comparator 1 Event Status Before Masking** 0_B Event has not occurred 1_B Event has occurred
ACMP2I	6	rh	**Analog Comparator 2 Event Status Before Masking** 0_B Event has not occurred 1_B Event has occurred
VDROPI	7	rh	**VDROP Event Status Before Masking** 0_B Event has not occurred 1_B Event has occurred
ORCxI (x=0,4,6,7)	x+8	rh	**Out of Range Comparator X Event Status Before Masking** 0_B Event has not occurred 1_B Event has occurred

(continued)

Field	Bits	Type	Description
LOCI	16	rh	**Loss of DCO1 Clock Event Status Before Masking** 0_B Event has not occurred 1_B Event has occurred
PESRAMI	17	rh	**16kbytes SRAM Parity Error Event Status Before Masking** 0_B Event has not occurred 1_B Event has occurred
PEU0I	18	rh	**USIC0 SRAM Parity Error Event Status Before Masking** 0_B Event has not occurred 1_B Event has occurred
FLECC2I	19	rh	**Flash Double Bit ECC Event Status Before Masking** 0_B Event has not occurred 1_B Event has occurred
FLCMPLTI	20	rh	**Flash Operation Complete Event Status Before Masking** 0_B Event has not occurred 1_B Event has occurred
VCLIPI	21	rh	**VCLIP Event Status Before Masking** 0_B Event has not occurred 1_B Event has occurred
SBYCLKFI	22	rh	**Standby Clock Failure Event Status Before Masking** 0_B No standby clock failure has occurred 1_B Standby clock failure has occurred
RTC_CTR	24	rh	**RTC CTR Mirror Register Update Status Before Masking** 0_B not updated 1_B update completed
RTC_ATIM0	25	rh	**RTC ATIM0 Mirror Register Update Status Before Masking** 0_B not updated 1_B update completed
RTC_ATIM1	26	rh	**RTC ATIM1 Mirror Register Update Status Before Masking** 0_B not updated 1_B update completed
RTC_TIM0	27	rh	**RTC TIM0 Mirror Register Update Before Masking** 0_B not updated 1_B update completed
RTC_TIM1	28	rh	**RTC TIM1 Mirror Register Update Status Before Masking** 0_B not updated 1_B update completed
TSE_DONE	29	rh	**DTS Measurement Done Event Status Before Masking** 0_B Event has not occurred 1_B Event has occurred

(continued)

Field	Bits	Type	Description
TSE_HIGH	30	rh	**DTS Compare High Temperature Event Status Before Masking** 0_B Event has not occurred 1_B Event has occurred
TSE_LOW	31	rh	**DTS Compare Low Temperature Event Status Before Masking** 0_B Event has not occurred 1_B Event has occurred
0	23	r	**Reserved**

14.9.6.7 Register SRMSK

Service request mask used to mask outputs of SRRAW register. When the bit is set to 1, an interrupt or service request will be triggered when the event happens.

SRMSK Address: $003C_H$

SCU Service Request Mask Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TSE_LOW	**TSE_HIGH**	**TSE_DONE**	**RTC_TIM1**	**RTC_TIM0**	**RTC_ATIM1**	**RTC_ATIM0**	**RTC_CTR**	**0**	**SBYCLKFI**	**VCLIPI**	**0**	**FLECC2I**	**PEU0I**	**PESRAMI**	**LOCI**
rw	rw	rw	rw	rw	rw	rw	rw	r	rw	rw	r	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**ORC6I**	**0**	**ORC4I**	**0**	**0**	**0**	**ORC0I**	**VDROPI**	**ACMP2I**	**ACMP1I**	**ACMP0I**	**VDDPI**	**0**	**0**	**PRWARN**
0	rw	0	rw	0	0	0	rw	rw	rw	rw	rw	rw	r	r	rw

Field	Bits	Type	Description
PRWARN	0	rw	**WDT pre-warning Interrupt Mask** 0_B disable interrupt 1_B enable interrupt
VDDPI	3	rw	**VDDP pre-warning Interrupt Mask** 0_B disable interrupt 1_B enable interrupt
ACMP0I	4	rw	**Analog Comparator 0 Interrupt Mask** 0_B disable interrupt 1_B enable interrupt
ACMP1I	5	rw	**Analog Comparator 1 Interrupt Mask** 0_B disable interrupt 1_B enable interrupt
ACMP2I	6	rw	**Analog Comparator 2 Interrupt Mask** 0_B disable interrupt 1_B enable interrupt

(continued)

Field	Bits	Type	Description
VDROPI	7	rw	**VDROP Interrupt Mask** 0_B disable interrupt 1_B enable interrupt
ORCxI (x=0,4,6,7)	x+8	rw	**Out of Range Comparator X Interrupt Mask** 0_B disable interrupt 1_B enable interrupt
LOCI	16	rw	**Loss of DCO1 Clock Interrupt Mask** 0_B disable interrupt 1_B enable interrupt
PESRAMI	17	rw	**16kbytes SRAM Parity Error Interrupt Mask** 0_B disable interrupt 1_B enable interrupt
PEU0I	18	rw	**USIC0 SRAM Parity Error Interrupt Mask** 0_B disable interrupt 1_B enable interrupt
FLECC2I	19	rw	**Flash Double Bit ECC Interrupt Mask** 0_B disable interrupt 1_B enable interrupt
VCLIPI	21	rw	**VCLIP Interrupt Mask** 0_B disable interrupt 1_B enable interrupt
SBYCLKFI	22	rw	**Standby Clock Failure Interrupt Mask** 0_B disable interrupt 1_B enable interrupt
RTC_CTR	24	rw	**RTC CTR Mirror Register Update Mask** 0_B disable interrupt 1_B enable interrupt
RTC_ATIM0	25	rw	**RTC ATIM0 Mirror Register Update Mask** 0_B disable interrupt 1_B enable interrupt
RTC_ATIM1	26	rw	**RTC ATIM1 Mirror Register Update Mask** 0_B disable interrupt 1_B enable interrupt
RTC_TIM0	27	rw	**RTC TIM0 Mirror Register Update Mask** 0_B disable interrupt 1_B enable interrupt
RTC_TIM1	28	rw	**RTC TIM1 Mirror Register Update Mask** 0_B disable interrupt 1_B enable interrupt

(continued)

Field	Bits	Type	Description
TSE_DONE	29	rw	**DTS Measurement Done Interrupt Mask** 0_B disable interrupt 1_B enable interrupt
TSE_HIGH	30	rw	**DTS Compare High Temperature Interrupt Mask** 0_B disable interrupt 1_B enable interrupt
TSE_LOW	31	rw	**DTS Compare Low Temperature Interrupt Mask** 0_B disable interrupt 1_B enable interrupt
0	2:1, 20, 23	r	**Reserved**

14.9.6.8 Register SRCLR

Clear service request bits of register SRRAW. Write one to clear corresponding bits. Writing zeros has no effect.

SRCLR Address: 0040_H

SCU Service Request Clear Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TSE_LOW	**TSE_HIGH**	**TSE_DONE**	**RTC_TIM1**	**RTC_TIM0**	**RTC_ATIM1**	**RTC_ATIM0**	**RTC_CTR**	**0**	**SBYCLKFI**	**VCLIPI**	**FLCMPLTI**	**FLEC2I**	**PEU0I**	**PESRAMI**	**LOCI**
w	w	w	w	w	w	w	w	r	w	w	w	w	w	w	w
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**ORC6I**	**0**	**ORC4I**	**0**	**0**	**0**	**ORC0I**	**VDROPI**	**ACMP2I**	**ACMP1I**	**ACMP0I**	**VDDPI**	**AI**	**PI**	**PRWARN**
r	w	r	w	r	r	r	w	w	w	w	w	w	w	w	w

Field	Bits	Type	Description
PRWARN	0	w	**WDT pre-warning Interrupt Clear** 0_B no effect 1_B clear status bit in the raw status register
PI	1	w	**RTC Periodic Interrupt Clear** 0_B no effect 1_B clear status bit in the raw status register
AI	2	w	**RTC Alarm Interrupt Clear** 0_B no effect 1_B clear status bit in the raw status register
VDDPI	3	w	**VDDP pre-warning Interrupt Clear** 0_B no effect 1_B clear status bit in the raw status register

(continued)

Field	Bits	Type	Description
ACMP0I	4	w	**Analog Comparator 0 Interrupt Clear** 0_B no effect 1_B clear status bit in the raw status register
ACMP1I	5	w	**Analog Comparator 1 Interrupt Clear** 0_B no effect 1_B clear status bit in the raw status register
ACMP2I	6	w	**Analog Comparator 2 Interrupt Clear** 0_B no effect 1_B clear status bit in the raw status register
VDROPI	7	w	**VDROP Interrupt Clear** 0_B no effect 1_B clear status bit in the raw status register
ORCxI (x=0,4,6,7)	x+8	w	**Out of Range Comparator X Interrupt Clear** 0_B no effect 1_B clear status bit in the raw status register
LOCI	16	w	**Loss of DCO1 Clock Interrupt Clear** 0_B no effect 1_B clear status bit in the raw status register
PESRAMI	17	w	**16kbytes SRAM Parity Error Interrupt Clear** 0_B no effect 1_B clear status bit in the raw status register
PEU0I	18	w	**USIC0 SRAM Parity Error Interrupt Clear** 0_B no effect 1_B clear status bit in the raw status register
FLECC2I	19	w	**Flash Double Bit ECC Interrupt Clear** 0_B no effect 1_B clear status bit in the raw status register
FLCMPLTI	20	w	**Flash Operation Complete Interrupt Clear** 0_B no effect 1_B clear status bit in the raw status register
VCLIPI	21	w	**VCLIP Interrupt Clear** 0_B no effect 1_B clear status bit in the raw status register
SBYCLKFI	22	w	**Standby Clock Failure Interrupt Clear** 0_B no effect 1_B clear status bit in the raw status register
RTC_CTR	24	w	**RTC CTR Mirror Register Update Clear** 0_B no effect 1_B clear status bit in the raw status register

(continued)

Field	Bits	Type	Description
RTC_ATIM0	25	w	**RTC ATIM0 Mirror Register Update Clear** 0_B no effect 1_B clear status bit in the raw status register
RTC_ATIM1	26	w	**RTC ATIM1 Mirror Register Update Clear** 0_B no effect 1_B clear status bit in the raw status register
RTC_TIM0	27	w	**RTC TIM0 Mirror Register Update Clear** 0_B no effect 1_B clear status bit in the raw status register
RTC_TIM1	28	w	**RTC TIM1 Mirror Register Update Clear** 0_B no effect 1_B clear status bit in the raw status register
TSE_DONE	29	w	**DTS Measurement Done Interrupt Clear** 0_B no effect 1_B clear status bit in the raw status register
TSE_HIGH	30	w	**DTS Compare High Temperature Interrupt Clear** 0_B no effect 1_B clear status bit in the raw status register
TSE_LOW	31	w	**DTS Compare Low Temperature Interrupt Clear** 0_B no effect 1_B clear status bit in the raw status register
0	23	r	**Reserved**

14.9.6.9 Register SRSET

Set service request fits of register SRRAW. Write one to set corresponding bits. Writing zeros has no effect.

SRSET Address: 0044_H

SCU Service Request Set Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TSE_LOW	**TSE_HIGH**	**TSE_DONE**	**RTC_TIM1**	**RTC_TIM0**	**RTC_ATIM1**	**RTC_ATIM0**	**RTC_CTR**	**0**	**SBYCLKFI**	**VCLIPI**	**FLCMPLTI**	**FLEC2I**	**PEU0I**	**PESRAMI**	**LOCI**
w	w	w	w	w	w	w	w	r	w	w	w	w	w	w	w
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**ORC6I**	**0**	**ORC4I**	**0**	**0**	**0**	**ORC0I**	**VDROPI**	**ACMP2I**	**ACMP1I**	**ACMP0I**	**VDDPI**	**AI**	**PI**	**PRWARN**
r	w	r	w	r	r	r	w	w	w	w	w	w	w	w	w

Field	Bits	Type	Description
PRWARN	0	w	**WDT pre-warning Interrupt Set** 0_B no effect 1_B set status bit in the raw status register
PI	1	w	**RTC Periodic Interrupt Set** 0_B no effect 1_B set status bit in the raw status register
AI	2	w	**RTC Alarm Interrupt Set** 0_B no effect 1_B set status bit in the raw status register
VDDPI	3	w	**VDDP pre-warning Interrupt Set** 0_B no effect 1_B set status bit in the raw status register
ACMP0I	4	w	**Analog Comparator 0 Interrupt Set** 0_B no effect 1_B set status bit in the raw status register
ACMP1I	5	w	**Analog Comparator 1 Interrupt Set** 0_B no effect 1_B set status bit in the raw status register
ACMP2I	6	w	**Analog Comparator 2 Interrupt Set** 0_B no effect 1_B set status bit in the raw status register
VDROPI	7	w	**VDROP Interrupt Set** 0_B no effect 1_B set status bit in the raw status register
ORCxI (x=0,4,6,7)	x+8	w	**Out of Range Comparator X Interrupt Set** 0_B no effect 1_B set status bit in the raw status register
LOCI	16	w	**Loss of DCO1 Clock Interrupt Set** 0_B no effect 1_B set status bit in the raw status register
PESRAMI	17	w	**16kbytes SRAM Parity Error Interrupt Set** 0_B no effect 1_B set status bit in the raw status register
PEU0I	18	w	**USIC0 SRAM Parity Error Interrupt Set** 0_B no effect 1_B set status bit in the raw status register
FLECC2I	19	w	**Flash Double Bit ECC Interrupt Set** 0_B no effect 1_B set status bit in the raw status register

(continued)

Field	Bits	Type	Description
FLCMPLTI	20	w	**Flash Operation Complete Interrupt Set** 0_B no effect 1_B set status bit in the raw status register
VCLIPI	21	w	**VCLIP Interrupt Set** 0_B no effect 1_B set status bit in the raw status register
SBYCLKFI	22	w	**Standby Clock Failure Interrupt Set** 0_B no effect 1_B set status bit in the raw status register
RTC_CTR	24	w	**RTC CTR Mirror Register Update Set** 0_B no effect 1_B set status bit in the raw status register
RTC_ATIM0	25	w	**RTC ATIM0 Mirror Register Update Set** 0_B no effect 1_B set status bit in the raw status register
RTC_ATIM1	26	w	**RTC ATIM1 Mirror Register Update Set** 0_B no effect 1_B set status bit in the raw status register
RTC_TIM0	27	w	**RTC TIM0 Mirror Register Update Set** 0_B no effect 1_B set status bit in the raw status register
RTC_TIM1	28	w	**RTC TIM1 Mirror Register Update Set** 0_B no effect 1_B set status bit in the raw status register
TSE_DONE	29	w	**DTS Measurement Done Interrupt Set** 0_B no effect 1_B set status bit in the raw status register
TSE_HIGH	30	w	**DTS Compare High Temperature Interrupt Set** 0_B no effect 1_B set status bit in the raw status register
TSE_LOW	31	w	**DTS Compare Low Temperature Interrupt Set** 0_B no effect 1_B set status bit in the raw status register
0	23	r	**Reserved**

14.9.6.10 Register SRRAW1

Service request status without masking. Write one to a bit in SRCLR1 register to clear a bit or SRSET1 to set a bit. Writing zero has no effect.

SRRAW1 Address: 0058_H

SCU Raw Service Request Status 1 Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0											DCO1OFSI	PEMCI	PEU1I	LOECI	ACMP3I
r											rh	rh	rh	rh	rh

Field	Bits	Type	Description
ACMP3I	0	rh	**Analog Comparator 3 Event Status Before Masking** 0_B Event has not occurred 1_B Event has occurred
LOECI	1	rh	**Loss of External OSC_HP Clock Event Status Before Masking** 0_B Event has not occurred 1_B Event has occurred
PEU1I	2	rh	**USIC1 SRAM Parity Error Event Status Before Masking** 0_B Event has not occurred 1_B Event has occurred
PEMCI	3	rh	**MultiCAN SRAM Parity Error Event Status Before Masking** 0_B Event has not occurred 1_B Event has occurred
DCO1OFSI	4	rh	**DCO1 Out of SYNC Event Status Before Masking** 0_B Event has not occurred 1_B Event has occurred
0	31:5	r	**Reserved**

14.9.6.11 Register SRMSK1

Service request mask used to mask outputs of SRRAW1 register. When the bit is set to 1, an interrupt or service request will be triggered when the event happens.

SRMSK1 Address: $005C_H$

SCU Service Request Mask 1 Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0											DCO1OFSI	PEMCI	PEU1I	LOECI	ACMP3I
r											rw	rw	rw	rw	rw

Field	Bits	Type	Description
ACMP3I	0	rw	**Analog Comparator 3 Interrupt Mask** 0_B disable interrupt 1_B enable interrupt
LOECI	1	rw	**Loss of External OSC_HP Clock Interrupt Mask** 0_B disable interrupt 1_B enable interrupt
PEU1I	2	rw	**USIC1 SRAM Parity Error Interrupt Mask** 0_B disable interrupt 1_B enable interrupt
PEMCI	3	rw	**MultiCAN SRAM Parity Error Interrupt Mask** 0_B disable interrupt 1_B enable interrupt
DCO1OFSI	4	rw	**DCO1 Out of SYNC Interrupt Mask** 0_B disable interrupt 1_B enable interrupt
0	31:5	r	**Reserved**

14.9.6.12 Register SRCLR1

Clear service request bits of register SRRAW1. Write one to clear corresponding bits. Writing zeros has no effect.

SRCLR1 Address: 0060_H

SCU Service Request Clear 1 Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0											**DCO1OFSI**	**PEMCI**	**PEU1I**	**LOECI**	**ACMP3I**
r											w	w	w	w	w

Field	Bits	Type	Description
ACMP3I	0	w	**Analog Comparator 3 Interrupt Clear** 0_B no effect 1_B clear status bit in the raw status register
LOECI	1	w	**Loss of External OSC_HP Clock Interrupt Clear** 0_B no effect 1_B clear status bit in the raw status register

(continued)

Field	Bits	Type	Description
PEU1I	2	w	**USIC1 SRAM Parity Error Interrupt Clear** 0_B no effect 1_B clear status bit in the raw status register
PEMCI	3	w	**MultiCAN SRAM Parity Error Interrupt Clear** 0_B no effect 1_B clear status bit in the raw status register
DCO1OFSI	4	w	**DCO1 Out of SYNC Interrupt Clear** 0_B no effect 1_B clear status bit in the raw status register
0	31:5	r	**Reserved**

14.9.6.13 Register SRSET1

Set service request fits of register SRRAW1. Write one to set corresponding bits. Writing zeros has no effect.

SRSET1 Address: 0064_H

SCU Service Request Set 1 Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0											**DCO1OFSI**	**PEMCI**	**PEU1I**	**LOECI**	**ACMP3I**
r											w	w	w	w	w

Field	Bits	Type	Description
ACMP3I	0	w	**Analog Comparator 3 Interrupt Set** 0_B no effect 1_B set status bit in the raw status register
LOECI	1	w	**Loss of External OSC_HP Clock Interrupt Set** 0_B no effect 1_B set status bit in the raw status register
PEU1I	2	w	**USIC1 SRAM Parity Error Interrupt Set** 0_B no effect 1_B set status bit in the raw status register
PEMCI	3	w	**MultiCAN SRAM Parity Error Interrupt Set** 0_B no effect 1_B set status bit in the raw status register

(continued)

Field	Bits	Type	Description
DCO1OFSI	4	w	**DCO1 Out of SYNC Interrupt Set** 0_B no effect 1_B set status bit in the raw status register
0	31:5	r	**Reserved**

14.9.6.14 Register PASSWD

The PASSWD register is used to control the bit protection scheme.

PASSWD Address: 0024_H

Password Register Reset Value: $0000\ 0007_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								**PASS**					**PROTS**	**MODE**	
r								w					rh	rw	

Field	Bits	Type	Description
MODE	1:0	rw	**Bit Protection Scheme Control Bits** 00_B Scheme disabled - direct access to the protected bits is allowed. 11_B Scheme enabled - the bit field PASS has to be written with the passwords to open and close the access to the protected bits. (Default) Others: Scheme enabled, similar to the setting for MODE = 11. These two bits cannot be written directly. To change the value between 11 and 00, the bit field PASS must be written with 11000. Only then will the MODE bit field be registered.
PROTS	2	rh	**Bit Protection Signal Status Bit** This bit shows the status of the protection. 0_B Software is able to write to all protected bits. 1_B Software is unable to write to any of the protected bits.
PASS	7:3	w	**Password Bits** This bit protection scheme only recognizes the following three passwords: 11000_B Enables writing of the bit field MODE. 10011_B Opens access to writing of all protected bits. 10101_B Closes access to writing of all protected bits.
0	31:8	r	**Reserved**

14.9.6.15 Register MIRRSTS

Mirror status register for control of communication between SCU and RTC.

MIRRSTS Address: 0048_H

Mirror Update Status Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0											RTC_TIM1	RTC_TIM0	RTC_ATIM1	RTC_ATIM0	RTC_CTR
r											rh	rh	rh	rh	rh

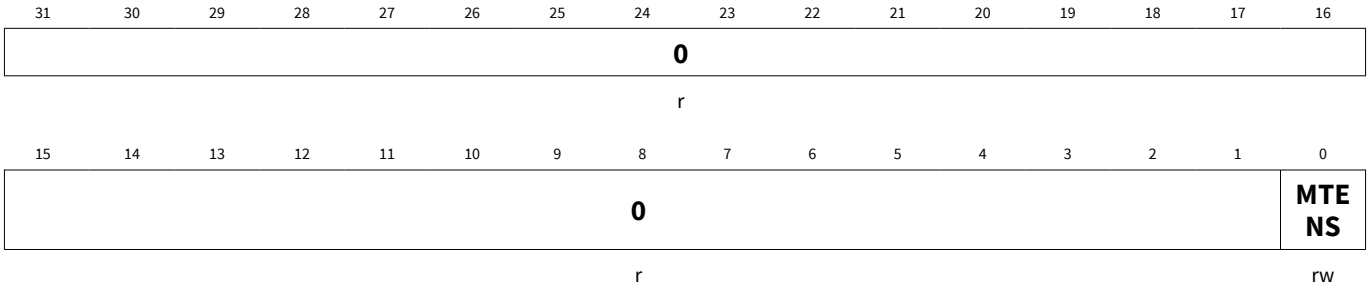
Field	Bits	Type	Description
RTC_CTR	0	rh	**RTC CTR Mirror Register Update Status** 0_B no update pending 1_B update pending
RTC_ATIM0	1	rh	**RTC ATIM0 Mirror Register Update Status** 0_B no update pending 1_B update pending
RTC_ATIM1	2	rh	**RTC ATIM1 Mirror Register Update Status** 0_B no update pending 1_B update pending
RTC_TIM0	3	rh	**RTC TIM0 Mirror Register Update Status** 0_B no update pending 1_B update pending
RTC_TIM1	4	rh	**RTC TIM1 Mirror Register Update Status** 0_B no update pending 1_B update pending
0	31:5	r	**Reserved** Read as 0; should be written with 0.

14.9.6.16 Register PMTSR

This register selects parity test output from a memory instance.

PMTSR Address: 0054_H

Parity Memory Test Select Register Reset Value: $0000\ 0000_H$



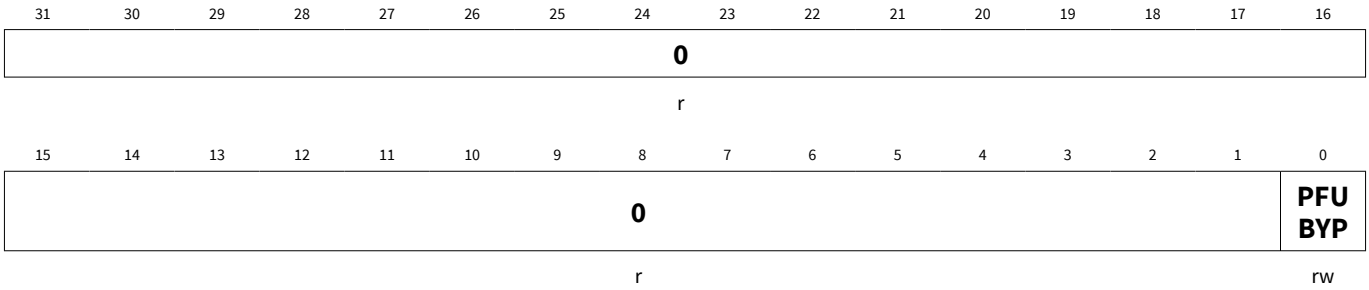
Field	Bits	Type	Description
MTENS	0	rw	**Parity Test Enable Control for 16kbytes SRAM** Controls the test multiplexer for the 16kbytes SRAM. 0_B standard operation 1_B generate an inverted parity bit during a write operation
0	31:1	r	**Reserved** Should be written with 0.

14.9.6.17 Register PFUCR

The Prefetch Unit (PFU) control register.

PFUCR Address: 0068_H

Prefetch Unit Control Register Reset Value: $0000\ 0001_H$



Field	Bits	Type	Description
PFUBYP	0	rw	**Prefetch Unit (PFU) Bypass** 0_B PFU not bypass 1_B PFU bypass
0	31:1	r	**Reserved** Should be written with 0.

14.9.6.18 Register INTCR0

This register selects the interrupt source for interrupt node 0 to 15.

INTCR0 Address: $006C_H$

Interrupt Control Register 0 Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTSEL15		**INTSEL14**		**INTSEL13**		**INTSEL12**		**INTSEL11**		**INTSEL10**		**INTSEL9**		**INTSEL8**	
rw		rw		rw		rw		rw		rw		rw		rw	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTSEL7		**INTSEL6**		**INTSEL5**		**INTSEL4**		**INTSEL3**		**INTSEL2**		**INTSEL1**		**INTSEL0**	
rw		rw		rw		rw		rw		rw		rw		rw	

Field	Bits	Type	Description
INTSELx (x=0-15)	2*x+1:2*x	rw	**Interrupt Source Select for Node x** 00_B Select source A 01_B Select source B 10_B Select source C 11_B Select source A or B

14.9.6.19 Register INTCR1

This register selects the interrupt source for interrupt node 16 to 31.

INTCR1 Address: 0070_H

Interrupt Control Register 1 Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTSEL31		**INTSEL30**		**INTSEL29**		**INTSEL28**		**INTSEL27**		**INTSEL26**		**INTSEL25**		**INTSEL24**	
rw		rw		rw		rw		rw		rw		rw		rw	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTSEL23		**INTSEL22**		**INTSEL21**		**INTSEL20**		**INTSEL19**		**INTSEL18**		**INTSEL17**		**INTSEL16**	
rw		rw		rw		rw		rw		rw		rw		rw	

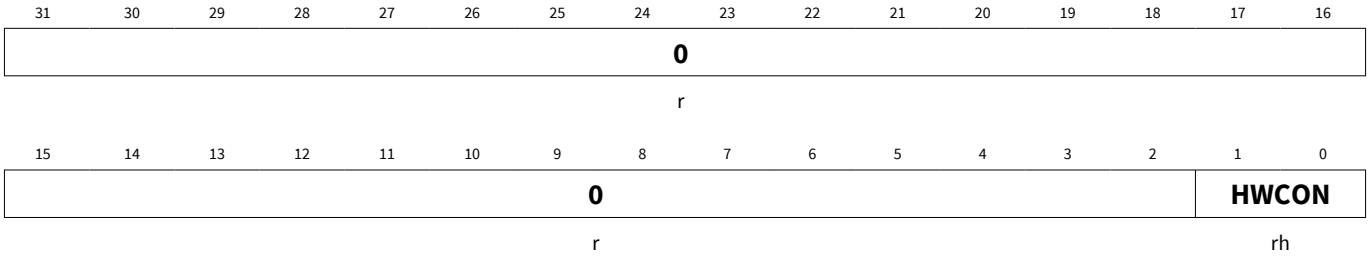
Field	Bits	Type	Description
INTSELx (x=16-31)	2*x-31:2*x-32	rw	**Interrupt Source Select for Node x** 00_B Select source A 01_B Select source B 10_B Select source C 11_B Select source A or B

14.9.6.20 Register STSTAT

Startup status register determines the boot process of the chip via pins.

STSTAT Address: 0074_H

Startup Status Register Reset Value: $0000\ 000X_H$



Field	Bits	Type	Description
HWCON	1:0	rh	**HW Configuration** At master reset, the following values are latched HWCON.0 = P4.6 HWCON.1 = P4.7 00_B User productive mode (UPM) 01_B ASC BSL 10_B Alternate Boot Mode (ABM) 11_B CAN BSL *Note: These values are not used when the BMI is used to bootup the device.*
0	31:2	r	**Reserved** Should be written with 0.

15 Window Watchdog Timer (WDT)

Purpose of the Window Watchdog Timer module is improvement of system integrity. WDT triggers the system reset or other corrective action like e.g. an interrupt if the main program, due to some fault condition, neglects to regularly service the watchdog (also referred to as “kicking the dog”, “petting the dog”, “feeding the watchdog” or “waking the watchdog”). The intention is to bring the system back from the unresponsive state into normal operation.

15.1 Overview

A successful servicing of the WDT results in a pulse on the signal wdt_service. The signal is offered also as an alternate function output can be used to show to an external watchdog that the system is alive.

The WDT timer is a 32-bit counter, which counts up from 0_H. It can be serviced while the counter value is within the window boundary, i.e. between the lower and the upper boundary value. Correct servicing results in a reset of the counter to 0_H. A so called “Bad Service” attempt results in the system reset request.

The timer block is running on the fWDT clock which is independent from the bus clock. The timer value is updated in the corresponding AHB register ***TIM***. This mechanism enables immediate response on a read access from the bus.

15.1.1 Features

The watchdog timer (WDT) is an independent window watchdog timer.

The features are:

- Triggers system reset when not serviced on time or serviced in a wrong way
- Servicing restricted to be within boundaries of refresh window
- Can run from an independent clock
- Provides service indication to an external pin
- Can be suspended in halting mode
- Provides optional pre-warning alarm before reset

Table 175 Application Features

Feature	Purpose/Application
System reset upon Bad Servicing	Triggered to restore system stable operation and ensure system integrity
Servicing restricted to be within defined boundaries of refresh window	Allows to consider minimum and maximum software timing
Independent clocks	To ensure that WDT counts even in case of the system clock failure
Service indication on external pin	For dual-channel watchdog solution, additional external control of system integrity
Suspending in HALT mode	Enables safe debugging with productive code
Pre-warning alarm	Software recovery to allow corrective action via software recovery routine bringing system back from the unresponsive state into normal operation

15.1.2 Block Diagram

The WDT block diagram is shown in ***Figure 42***.

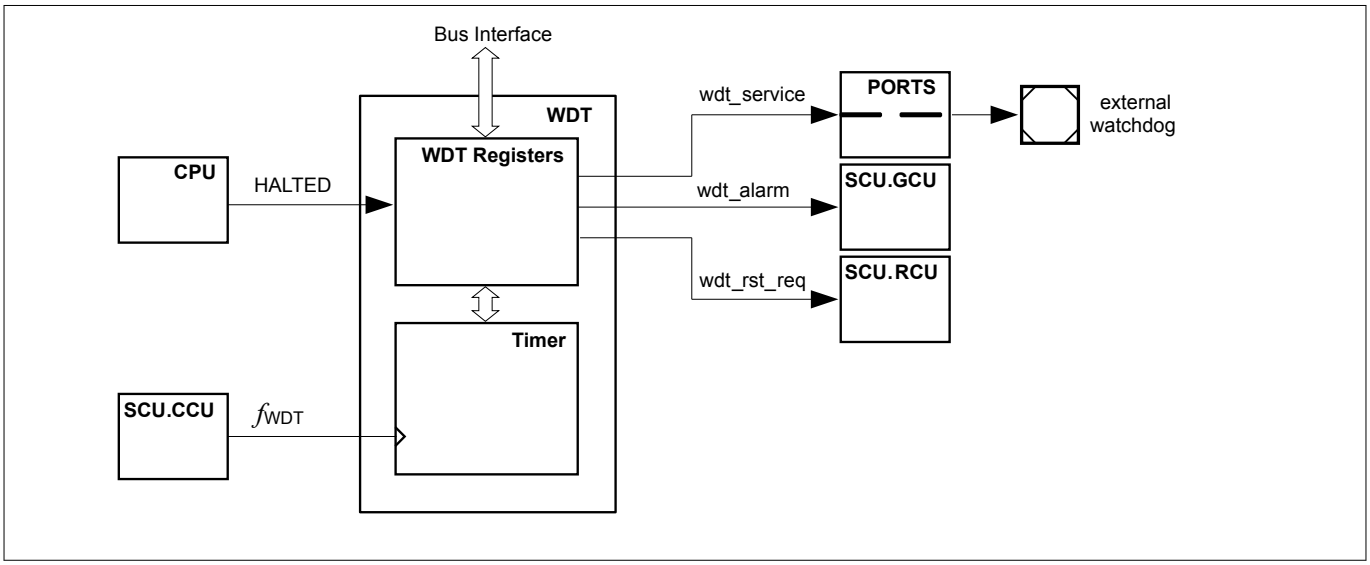


Figure 42 Watchdog Timer Block Diagram

15.2 Time-Out Mode

An overflow results in an immediate reset request going to the RCU of the SCU via the signal wdt_rst_req whenever the counter crosses the upper boundary it triggers an overflow event pre-warning is not enabled with ***CTR*** register. A successful servicing performed with writing a unique value, referred to as “Magic Word” to the ***SRV*** register of the WDT within the valid servicing window, results in a pulse on the signal wdt_service and reset of the timer counter.

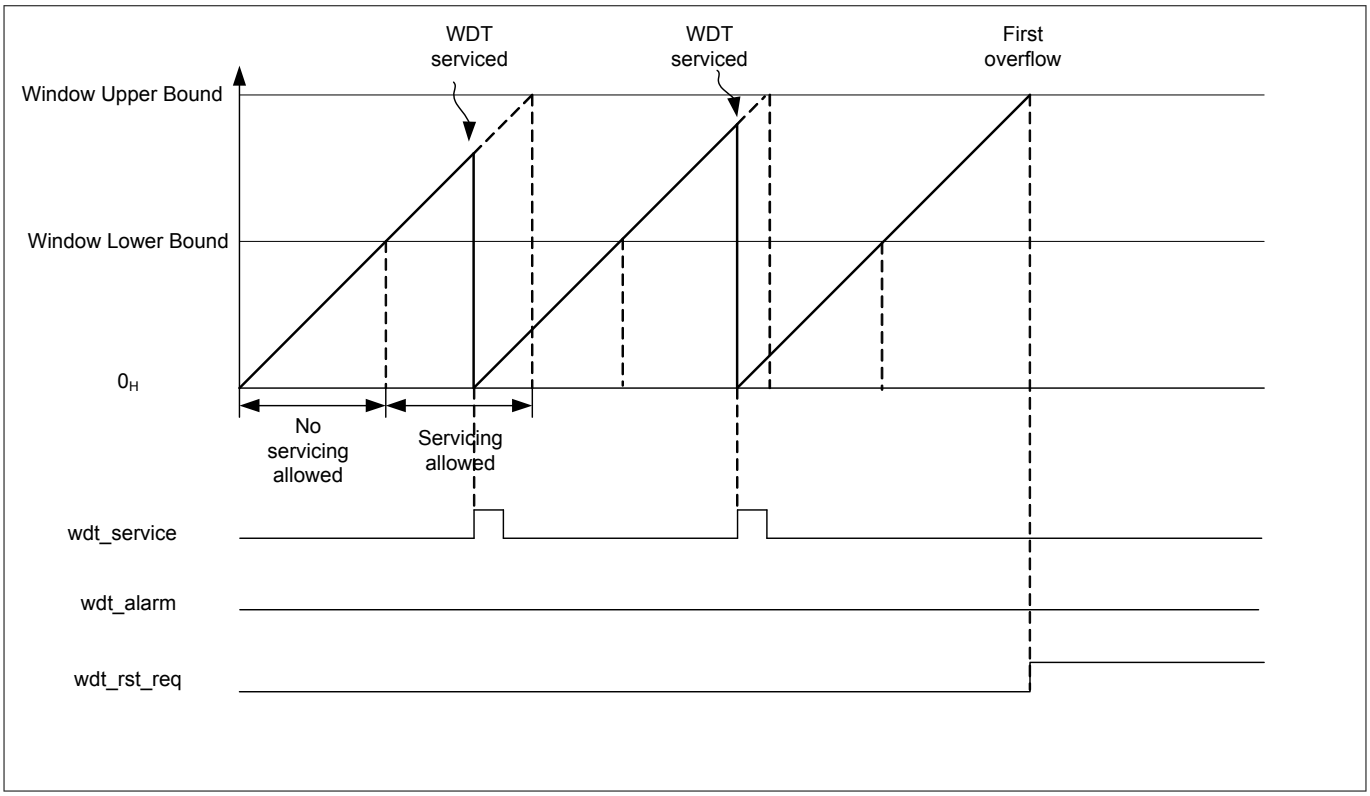


Figure 43 Reset without pre-warning

The example scenario depicted in ***Figure 43*** shows two consecutive service pulses generated from WDT module as the result of successful servicing within valid time windows. The situation where no service has been performed immediately triggers generation of reset request on the wdt_rst_req output after the counter value has exceeded window upper bound value.

15.3 Pre-warning Mode

While in pre-warning mode the effect of the overflow event is different with and without pre-warning enabled. The first crossing of the upper bound triggers the outgoing alarm signal wdt_alarm when pre-warning is enabled. Only the next overflow results a reset request. The alarm status is shown via register ***WDTSTS*** and can be cleared via register ***WDTCLR***. A clear of the alarm status will bring the WDT back to normal state.

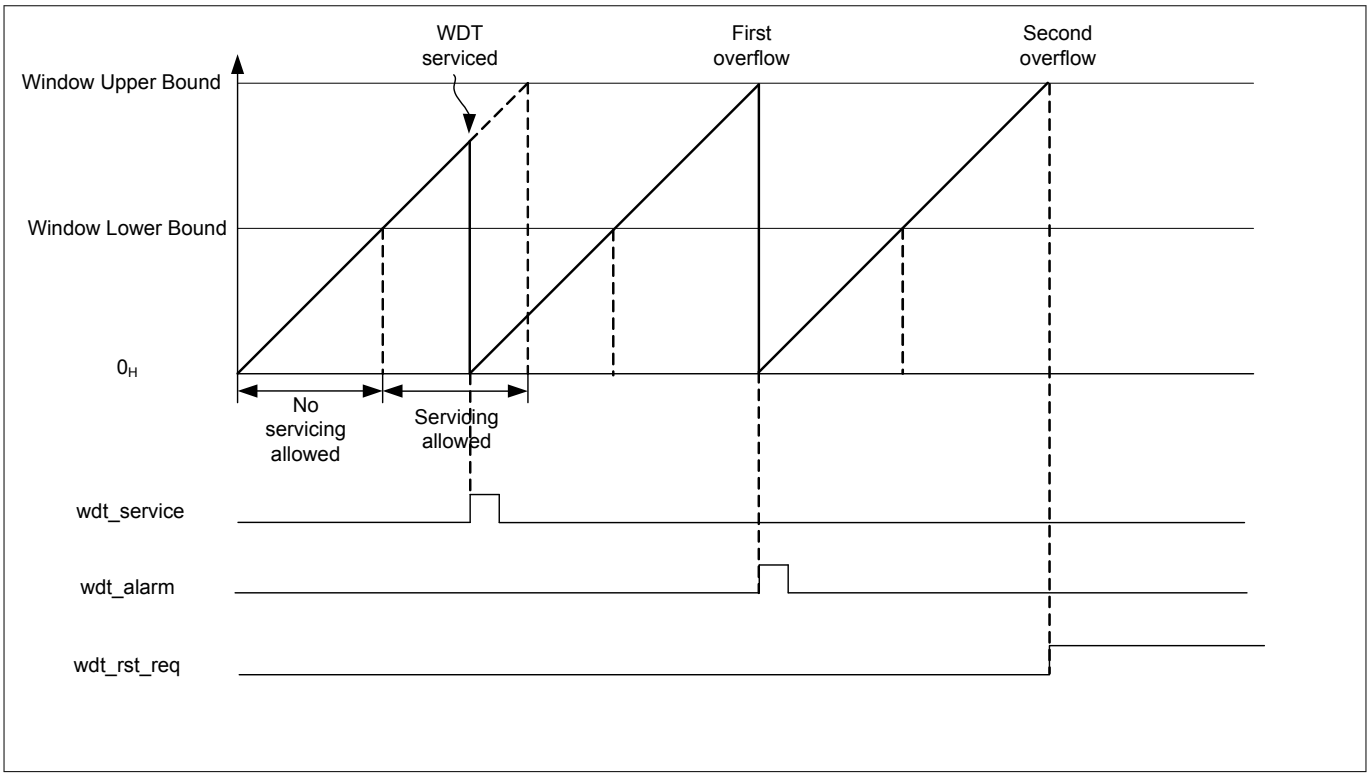


Figure 44 Reset after pre-warning

The example scenario depicted in ***Figure 44*** shows service pulse generated from WDT module as the result of successful servicing within valid time window. WDT generates alarm pulse on wdt_alarm upon first missing servicing. The alarm signal is routed as interrupt request to the SCU. Within this alarm service request the user can clear the WDT status bit and give a proper WDT service before it overflows next time. Otherwise WDT generates reset request on wdt_rstn upon the second missing service.

15.4 Bad Service Operation

A bad service attempt results in a reset request. A bad service attempt can be due to servicing outside the window boundaries or servicing with an invalid Magic Word.

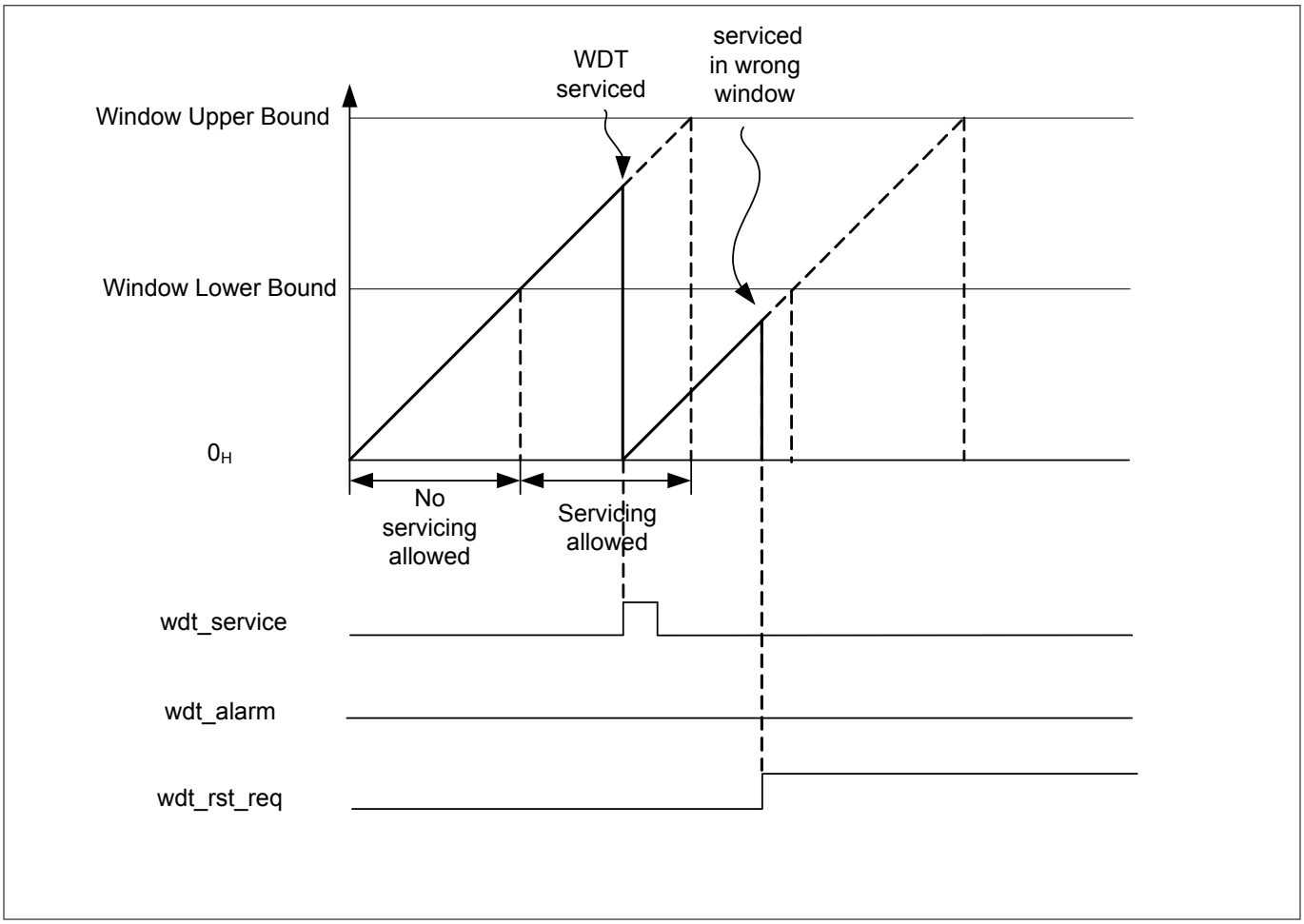


Figure 45 Reset upon servicing in a wrong window

The example in ***Figure 45*** shows servicing performed outside of valid servicing window. Attempt to service WDT while counter value remains below the window lower bound results in immediate reset request on wdt_rst_req signal.

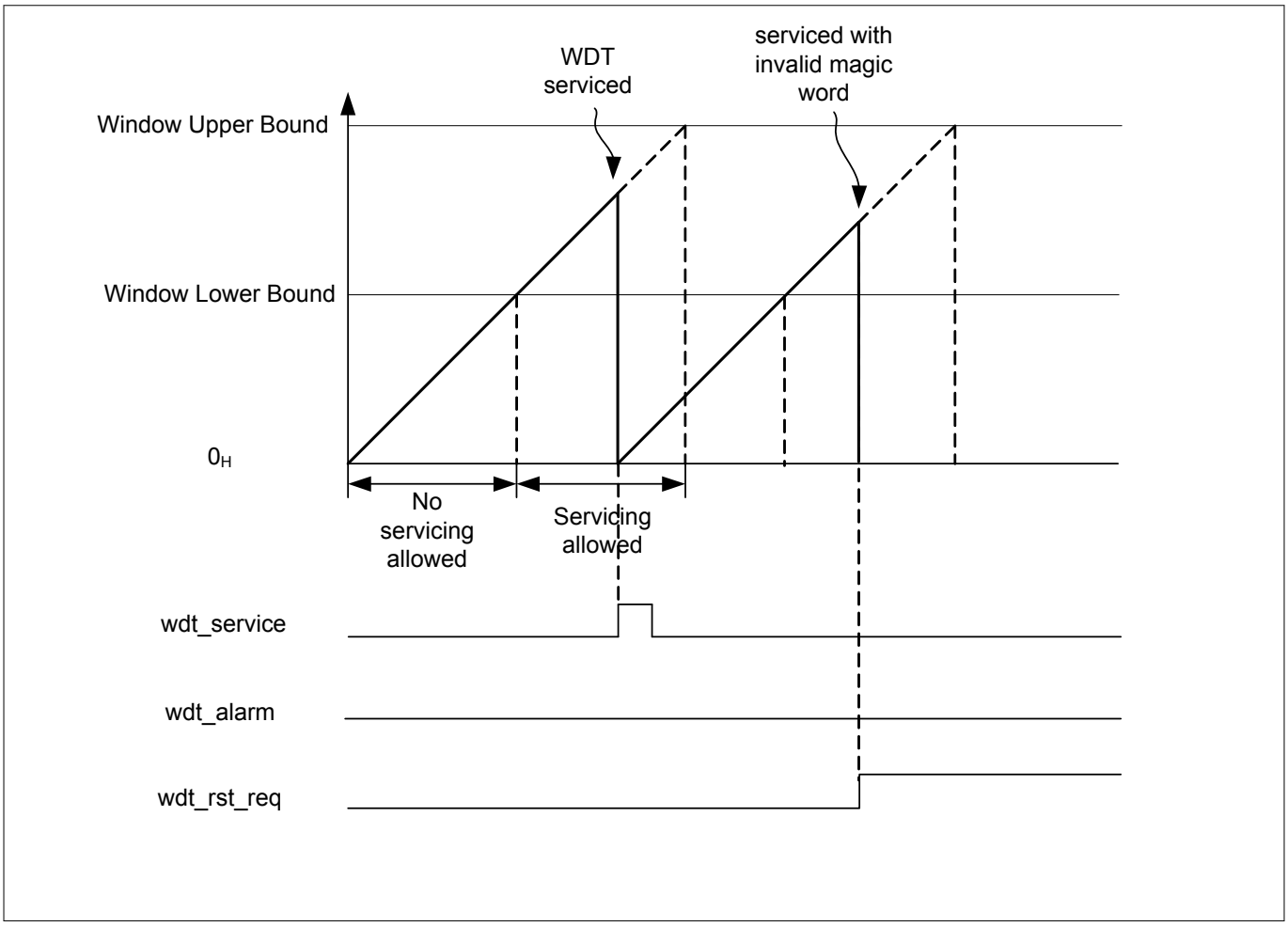


Figure 46 Reset upon servicing with a wrong magic word

The example in ***Figure 46*** shows servicing performed within a valid servicing window but with an invalid Magic Word. Attempt to write a wrong word to the ***SRV*** register results in immediate reset request on wdt_rst_req signal.

15.5 Service Request Processing

The WDT generates watchdog alarm service requests via wdt_alarm output signal upon first counter overflow over watchdog upper bound when pre-warning mode is enabled. The alarm service request is serviced in SCU.

Service requests can be disabled respectively by service request mask register in SCU.

15.6 Debug Behavior

The WDT function can be suspended when the CPU enters HALT mode. WDT debug function is controlled with DSP bit field in ***CTR*** register and it is set to be suspended by default.

15.7 Power, Reset and Clock

The WDT module is a part of the core domain and supplied with V_{DDC} voltage.

All WDT registers get reset with the system reset.

A sticky bit in the Reset Status Register, RSTSTAT, of SCU/RCU module indicates whether the last system reset has been triggered by the WDT module. This bit does not get reset with system reset.

The input clock of the WDT counter is provided by the internal 32kHz standby clock from SCU/CCU module, independently from the AHB interface clock.

The WDT module clock is default disabled and can be enabled via the SCU_CGATCLR0 register. Enabling and disabling the module clock could cause load change and clock blanking could happen as explained in the CCU (Clock Gating Control) section of the SCU chapter. It is strongly recommended to setup the module clock in the user initialisation code to avoid clock blanking during runtime.

15.8 Initialization and Control Sequence

Programming model of the WDT module assumes several scenarios where different control sequences apply.

Note: Some of the scenarios described in this chapter require operations on system level the that are not in the scope of the WDT module description, therefore for detailed information please refer to relevant chapters of this document.

15.8.1 Initialization & Start of Operation

Complete WDT module initialization is required upon system reset.

- check reason for last system reset in order to determine power state
  - read out SCU_RSTSTAT.RSTSTAT register bit field to determine last system reset cause and clear this bit using bit SCU_RSTCLR.RSCLR
  - perform appropriate operations dependent on the last system reset cause
- WDT software initialization sequence
  - enable WDT clock with SCU_CGATCLR0.WDT register bit field
  - set lower window bound with WDT_WLB register
  - set upper window bound with WDT_WUB register
  - configure external watchdog service indication (optional, please refer to PORT chapter)
  - enable interrupt for pre-warning alarm on system level with SCU_SRMSK register (optional, used in WDT pre-warning mode only)
- software start sequence
  - select mode (Time-Out or Pre-warning) and enable WDT module with WDT_CTR register
- service the watchdog
  - write magic word to WDT_SRV register within valid time window

15.8.2 Software Stop & Resume Operation

The WDT module can be stopped and re-started at any point of time for e.g. debug purpose using software sequence.

- software stop sequence
  - disable WDT module with WDT_CTR register
- perform any user operations
- software start (resume) sequence
  - enable WDT module with WDT_CTR register with WDT_CTR register
- service the watchdog
  - write magic word to WDT_SRV register within valid time window

15.8.3 Enter Sleep/Deep-Sleep & Resume Operation

The WDT counter clock can be configured to stop while in sleep or deep-sleep mode. No direct software interaction with the WDT is required in those modes and no watchdog time-out will fire if the WDT clock is configured to stop while CPU is sleeping.

- software configuration sequence for sleep/deep-sleep mode
  - configure WDT behavior with SCU_CGATx register
- enter sleep/deep-sleep mode software sequence
  - select sleep or deep-sleep mode in CPU (for details please refer to Cortex-M0 documentation *[1]*)
  - enter selected mode (for details please refer to Cortex-M0 documentation *[1]*)
- wait for a wake-up event (no software interaction, CPU stopped)
- resume operation (CPU clock restarted automatically on an event)
- service the watchdog
  - write magic word to WDT_SRV register within valid time window

15.8.4 Pre-warning Alarm Handling

The WDT will fire pre-warning alarm before requesting system reset while in pre-warning mode and not serviced within valid time window. The WDT status register indicating alarm must be cleared before the timer counter value crosses the upper bound for the second time after firing the alarm. After clearing of the alarm status regular watchdog servicing must be performed within valid time window.

- alarm event
  - exception routine (service request) clearing WDT_WDTSTAT register with WDT_WDTCLR register
- service the watchdog
  - write magic word to WDT_SRV register within valid time window

15.9 WDT Registers

Registers Overview

The absolute register address is calculated by adding:
Module Base Address + Offset Address

Table 176 Registers Address Space

Module	Base Address	End Address	Note
WDT	$4002\ 0000_H$	$4002\ FFFF_H$	Watchdog Timer Registers

Table 177 Register Overview

Short Name	Description	Offset Addr.	Access Mode		Description See
			Read	Write	
WDT Kernel Registers					
ID	Module ID Register	00_H	U, PV	PV	Page *303*
CTR	Control Register	04_H	U, PV	PV	Page *303*
SRV	Service Register	08_H	BE	PV	Page *304*
TIM	Timer Register	$0C_H$	U, PV	BE	Page *305*

Table 177 Register Overview (continued)

Short Name	Description	Offset Addr.	Access Mode		Description See
			Read	Write	
WLB	Window Lower Bound	10_H	U, PV	PV	Page 305
WUB	Window Upper Bound	14_H	U, PV	PV	Page 306
WDTSTS	Watchdog Status Register	18_H	U, PV	PV	Page 306
WDTCLR	Watchdog Status Clear Register	$1C_H$	U, PV	PV	Page 307

15.9.1 Register ID

The module unique ID register.

ID Address: 0000_H

WDT Module ID Register Reset Value: 00AD C0XX$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MOD_NUMBER															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOD_TYPE								MOD_REV							
r								r							

Field	Bits	Type	Description
MOD_REV	7:0	r	**Module Revision Number** Indicates the revision number of the implementation. The value of a module revision starts with 01_H (first revision).
MOD_TYPE	15:8	r	**Module Type** This bit field is fixed to $C0_H$.
MOD_NUMBER	31:16	r	**Module Number Value** This bit field defines the module identification number.

15.9.2 Register CTR

The operation mode control register.

CTR Address: 04_H

WDT Control Register Reset Value: 0000 0000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPW								0			DSP	0		PRE	ENB
rw								r			rw	r		rw	rw

Field	Bits	Type	Description
ENB	0	rw	**Enable** 0_B disables watchdog timer, 1_B enables watchdog timer
PRE	1	rw	**Pre-warning** 0_B disables pre-warning 1_B enables pre-warning,
DSP	4	rw	**Debug Suspend** 0_B watchdog timer is stopped during debug halting mode 1_B watchdog timer is not stopped during debug halting mode
SPW	15:8	rw	**Service Indication Pulse Width** Pulse width (SPW+1) of service indication in f_{WDT} cycles
0	3:2, 7:5, 31:16	r	**reserved**

15.9.3 Register SRV

The WDT service register. Software must write a magic word while the timer value is within the valid window boundary. Writing the magic word while the timer value is within the window boundary will service the watchdog and result a reload of the timer with 0H.

Upon writing data different than the magic word within valid time window or writing even correct Magic Word but outside of the valid time window no servicing will be performed. Instead will request an immediate system reset request.

SRV Address: 08_H

WDT Service Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SRV															
w															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRV															
w															

Field	Bits	Type	Description
SRV	31:0	w	**Service** Writing the magic word ABADCAFE$_H$ while the timer value is within the window boundary will service the watchdog.

15.9.4 Register TIM

The actual watchdog timer register count value. This register can be read by software in order to determine current position in the WDT time window.

TIM Address: 0C$_H$

WDT Timer Register Reset Value: 0000 0000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TIM															
rh															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIM															
rh															

Field	Bits	Type	Description
TIM	31:0	rh	**Timer Value** Actual value of watchdog timer value.

15.9.5 Register WLB

The Window Lower Bound register defines the lower bound for servicing window. Servicing of the watchdog has only effect within the window boundary

WLB Address: 10$_H$

WDT Window Lower Bound Register Reset Value: 0000 0000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WLB															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WLB															
rw															

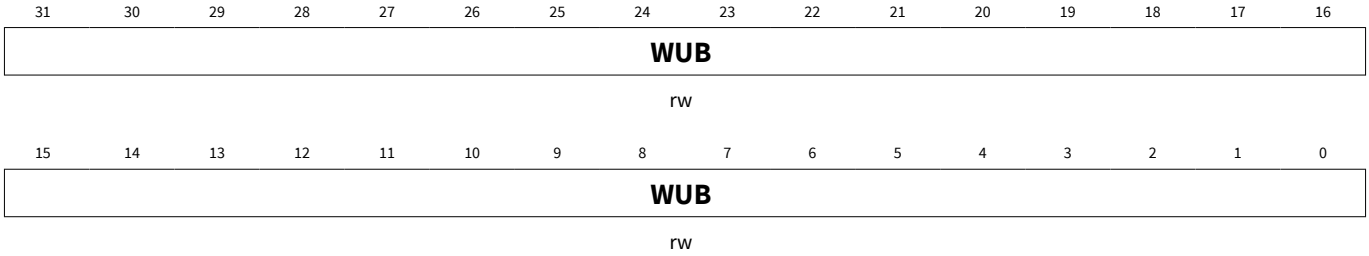
Field	Bits	Type	Description
WLB	31:0	rw	**Window Lower Bound** Lower bound for servicing window. Setting the lower bound to 0$_H$ disables the window mechanism.

15.9.6 Register WUB

The Window Upper Bound register defines the upper bound for servicing window. Servicing of the watchdog has only effect within the window boundary.

WUB Address: 14_H

WDT Window Upper Bound Register Reset Value: $FFFF\ FFFF_H$



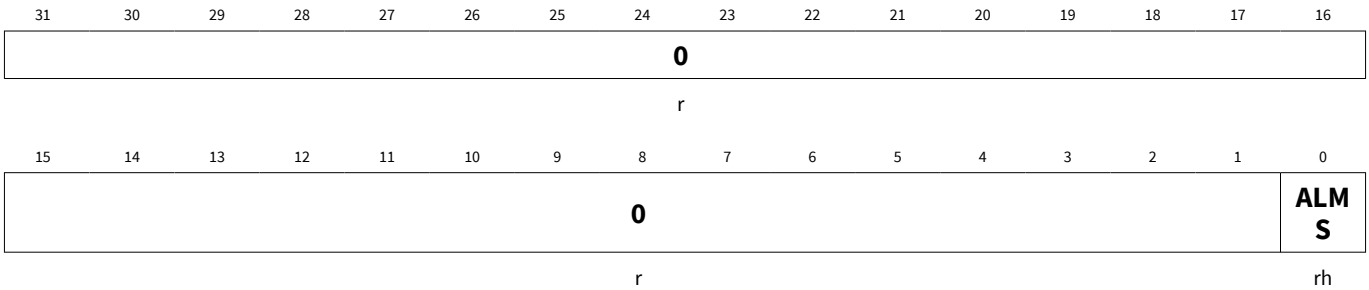
Field	Bits	Type	Description
WUB	31:0	rw	**Window Upper Bound** Upper Bound for servicing window. The WDT triggers an reset request when the timer is crossing the upper bound value without pre-warning enabled. With pre-warning enabled the first crossing triggers a watchdog alarm and the second crossing triggers a system reset.

15.9.7 Register WDTSTS

The status register contains sticky bit indicating occurrence of alarm condition.

WDTSTS Address: 0018_H

WDT Status Register Reset Value: 00000000_H



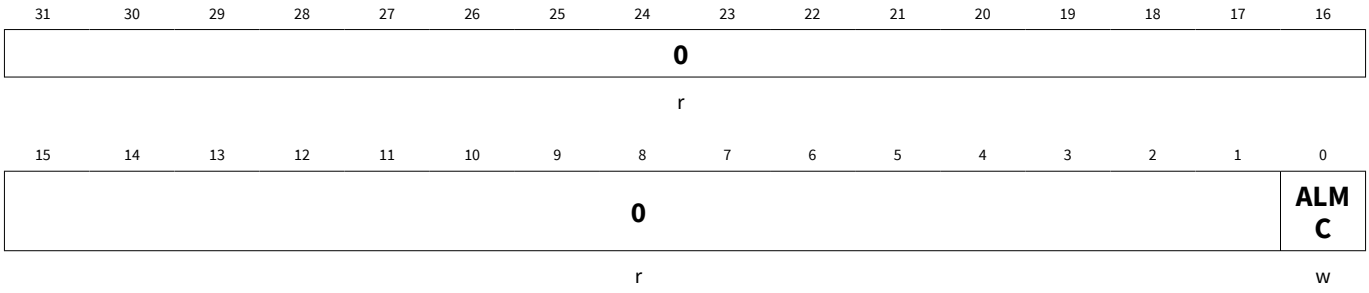
Field	Bits	Type	Description
ALMS	0	rh	**Pre-warning Alarm** 1_B pre-warning alarm occurred, 0_B no pre-warning alarm occurred
0	31:1	r	**reserved**

15.9.8 Register WDTCLR

The status register contains sticky bitfield indicating occurrence of alarm condition.

WDTCLR Address: $001C_H$

WDT Clear Register Reset Value: 00000000_H



Field	Bits	Type	Description
ALMC	0	w	**Pre-warning Alarm** 1_B clears pre-warning alarm 0_B no-action
0	31:1	r	**reserved**

15.10 Interconnects

Table 178 Pin Table

Input/Output	I/O	Connected To	Description
Clock and Reset Signals			
f_{WDT}	I	SCU.CCU	timer clock
Timer Signals			
wdt_service	O	PORTS	service indication to external watchdog
HALTED	I	CPU	In halting mode debug. HALTED remains asserted while the core is in debug.
Service Request Connectivity			
wdt_alarm	O	SCU.GCU	pre-warning alarm
wdt_rst_req	O	SCU.RCU	reset request

16 Real Time Clock (RTC)

Real-time clock (RTC) is a clock that keeps track of the current time. RTCs are present in almost any electronic device which needs to keep accurate time in a digital format for clock displays and computer systems.

16.1 Overview

The RTC module tracks time with separate registers for hours, minutes, and seconds. The calendar registers track date, day of the week, month and year with automatic leap year correction[32]. The clock of RTC is selectable via bit SCU_CLKCR.RTCCLKSEL.

The timer may remains operational during sleep or deep sleep mode.

16.1.1 Features

The features of the Real Time Clock (RTC) module are:

- Real time keeping with
  - 32.768 kHz external clock
  - 32.768 kHz internal clock
- Periodic time-based interrupt
- Programmable alarm interrupt on time match
- Supports wake-up mechanism from sleep or deep sleep mode

Table 179 Application Features

Feature	Purpose/Application
Precise real time keeping	Reduced need for time adjustments
Periodic time-based interrupt	Scheduling of operations performed on precisely defined intervals
Programmable alarm interrupt on time match	Scheduling of operations performed on precisely defined times
Supports wake-up mechanism from sleep or deep sleep mode	Autonomous wakeups from sleep or deep sleep mode for system state control and maintaintenance routine operations

16.1.2 Block Diagram

The RTC block diagram is shown in ***Figure 47***.

The main building blocks of the RTC is Time Counter implementing real time counter and RTC Registers containing multi-field registers for the time counter and alarm programming register where dedicated fields represent a separate values for elapsing second, minutes, hours, days, days of week, months and years.

The RTC module is controlled directly from SCU module and shares system bus interface with other sub-modulesof SCU.

Access to the RTC registers is performed via Register Mirror updated over serial interface .

32 The automatic leap year correction is performed when the year is divisible by 4.

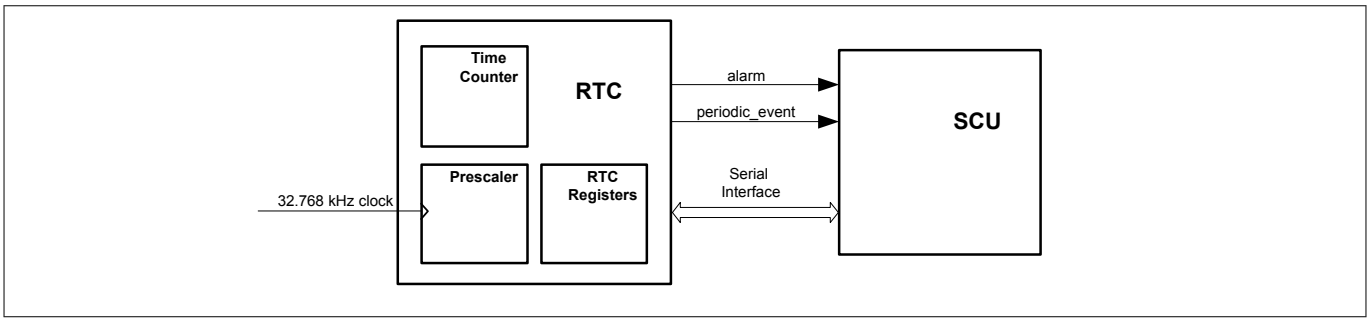


Figure 47 Real Time Clock Block Diagram Structure

16.2 RTC Operation

The RTC timer counts seconds, minutes, hours, days, days of week, months and years the time in separate fields (see ***Figure 48***). Individual bit fields of the RTC counter can be programmed and read with software over serial interface via mirror registers in SCU module.

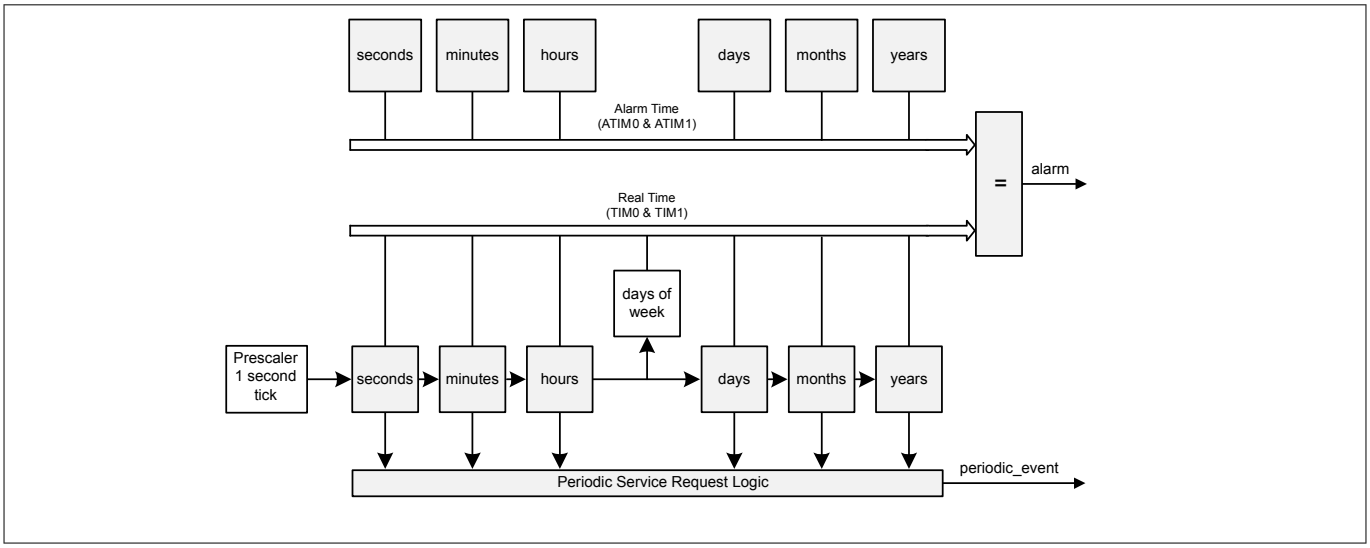


Figure 48 Block Diagram of RTC Time Counter

Occurrence of an internal timer event is stored in the service request raw status register ***RAWSTAT***. The values of the status register ***RAWSTAT*** drive the outgoing service request lines alarm and periodic_event.

16.3 Register Access Operations

The RTC module is a part of SCU from programmming model perepcetive and shares register address space for configuration with other sub-modules of SCU. RTC registers are instantiated in the RTC module and mirrored in SCU. The registers get updated in both clock domains over serial interface running at 32kHz clock rate.

Any update of the registers is performed with some delay required for data to propagate to and from the mirror registers over serial interface. Accesses to the RTC registers in core domain must not block the bus interface of SCU module. For details of the register mirror and serial communication handling please refer to SCU chapter.

For consistent write to the timer registers ***TIM0*** and ***TIM1***, the register ***TIM0*** has to be written before the register ***TIM1***. Transfer of the new values from the register mirror starts only after both registers have been written.

For consistent read-out of the timer registers ***TIM0*** and ***TIM1***, the register ***TIM0*** has to be read before the register ***TIM1***. The value of ***TIM1*** is stored in a shadow register upon each read of ***TIM0*** before they get copied to the mirror register in core domain.

16.4 Service Request Processing

The RTC generates service requests upon:

- periodic timer events
- configured alarm condition

The service requests can be processed in the core domain as regular service requests or as wake-up triggers from sleep or deep sleep mode.

16.4.1 Periodic Service Request

The periodic timer service request is raised whenever a non-masked field of the timer counter gets updated. Masking of the bits is performed using ***MSKSR*** register. Periodic Service requests can be disabled with ***MSKSR***.

16.4.2 Timer Alarm Service Request

The alarm interrupt is triggered when ***TIM0*** and ***TIM1*** bit fields values match all corresponding bit fields values of ***ATIM0***, ***ATIM1*** registers. The Timer Alarm Service requests can be enabled/disabled with the ***MSKSR*** register.

16.5 Debug Behavior

The RTC function can be suspended when the CPU enters HALT mode. RTC debug function is controlled with SUS bit field in ***CTR*** register.

Note: In IMC300A, bit CTR.SUS is reset to its default value by any reset. Hence, if suspend function is required during debugging, it is recommended to enable the debug suspend function in the user initialisation code. Before programming the register, the module clock has to be enabled and special care need to be handled while enabling the module clock as described in the CCU (Clock Gating Control) section of the SCU chapter.

16.6 Power, Reset and Clock

RTC can be programmed to remains powered up in sleep and deep sleep mode.

The RTC module remains in reset state after initial power up until reset released.

The RTC timer is running from an internal or external 32.768 kHz clock selectable with CLKCR.RTCCLKSEL control register of SCU/CCU module as shown in ***Figure 49***.The prescaler setting of $7FFF_H$ results in an once per second update of the RTC timer.

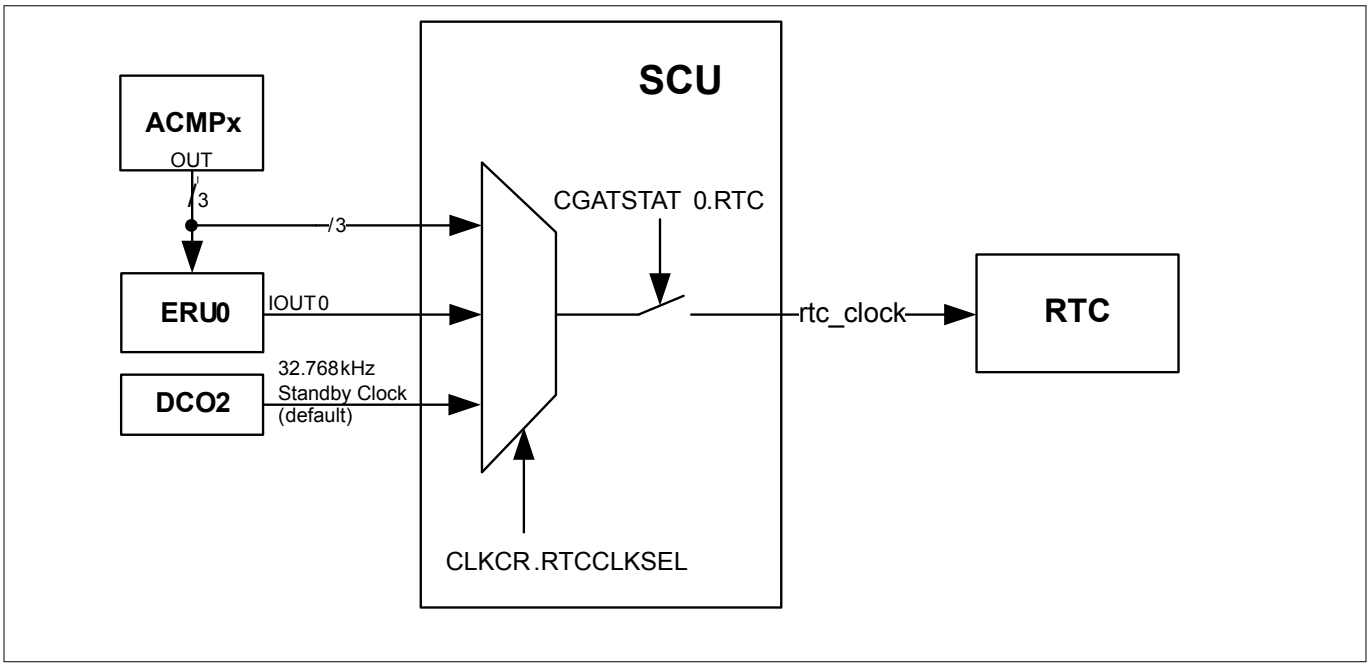


Figure 49 RTC Clock selection

The RTC module clock is default disabled and can be enabled via the SCU_CGATCLR0 register.

Note: Before changing RTC clock source via CLKCR.RTCCLKSEL, the RTC clock must be gated using bit CGATSET0.RTC.

16.7 Initialization and Control Sequence

Programming model of the RTC module assumes several scenarios where different control sequences apply.

Note: Some of the scenarios described in this chapter require operations on system level the that are not in the scope of the RTC module description, therefore for detailed information please refer to relevant chapters of this document.

16.7.1 Initialization & Start of Operation

Complete RTC module initialization is required upon reset. Accesses to RTC registers are performed via dedicated mirror registers (for more details please refer to SCU chapter)

- enable the clock to RTC module
  - write one to SCU_CGATCLR0.RTC
- program RTC_TIM0 and RTC_TIM1 registers with current time
  - check SCU_MIRRSTS to ensure that no transfer over serial interface is pending to the RTC_TIM0 and RTC_TIM1 registers
  - write a new value to the RTC_TIM0 and RTC_TIM1 registers
- enable RTC module to start counting time
  - write one to RTC_CTR.ENB

Note: To ensure a successful transfer over serial interface, RTC_TIM0 and RTC_TIM1 can only be written once for each transfer. In addition, these registers must be written in 32-bit data width. Individual bit access will not start the serial transfer operation.

16.7.2 Configure and Enable Periodic Event

The RTC periodic event configuration require programming in order to enable interrupt request generation out upon a change of value in the corresponding bit fields.

- enable service request for periodic timer events in RTC module
  - set respective bit field (MPSE, MPMI, MPHO, MPDA, MPMO, MPYE) in RTC_MSKSR register to enable the individual periodic timer events

16.7.3 Configure and Enable Timer Event

The RTC alarm event configuration require programming in order to enable interrupt request generation out upon compare match of values in the corresponding bit fields of TIM0 and TIM1 against ATIM0 and ATIM1 respectively.

- program compare values in individual bit fields of ATIM0 and ATIM1 in RTC module
  - check SCU_MIRRSTS to ensure that no transfer over serial interface is pending to the RTC_ATIM0 and RTC_ATIM1 registers
  - write to RTC_ATIM0 and RTC_ATIM1 registers
- enable service request for timer alarm events in RTC module
  - set MAI bit field of RTC_MSKSR register in order enable individual periodic timer events

Note: To ensure a successful transfer over serial interface, RTC_ATIM0 and RTC_ATIM1 can only be written once for each transfer. In addition, these registers must be written in 32-bit data width. Individual bit access will not start the serial transfer operation.

16.8 RTC Registers

Registers Overview

The absolute register address is calculated by adding:
Module Base Address + Offset Address

Table 180 Registers Address Space

Module	Base Address	End Address	Note
RTC	$4001\ 0A00_H$	$4001\ 0AFF_H$	

Table 181 Register Overview

Short Name	Description	Offset Addr.	Access Mode		Description See
			Read	Write	
RTC Kernel Registers					
ID	ID Register	0000_H	U, PV	BE	Page 313
CTR	Control Register	0004_H	U, PV	PV	Page 313
RAWSTAT	Raw Service Request Register	0008_H	U, PV	BE	Page 314
STSSR	Status Service Request Register	$000C_H$	U, PV	BE	Page 315
MSKSR	Mask Service Request Register	0010_H	U, PV	PV	Page 316
CLRSR	Clear Service Request Register	0014_H	U, PV	PV	Page 316

Table 181 Register Overview (continued)

Short Name	Description	Offset Addr.	Access Mode		Description See
			Read	Write	
ATIM0	Alarm Time Register 0	0018_H	U, PV	PV	Page 317
ATIM1	Alarm Time Register 1	$001C_H$	U, PV	PV	Page 318
TIM0	Time Register 0	0020_H	U, PV	PV	Page 319
TIM1	Time Register 1	0024_H	U, PV	PV	Page 320

16.8.1 Register ID

Read-only ID register of the RTC module containing unique identification code of the RTC module.

ID Address: 00_H

RTC Module ID Register Reset Value: $00A3\ C0XX_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MOD_NUMBER															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOD_TYPE								MOD_REV							
r								r							

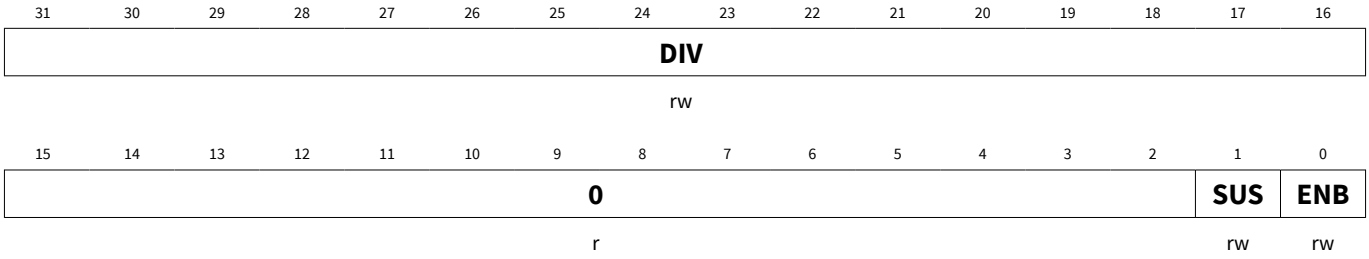
Field	Bits	Type	Description
MOD_REV	7:0	r	**Module Revision Number** Indicates the revision number of the implementation. The value of a module revision starts with 01_H (first revision).
MOD_TYPE	15:8	r	**Module Type** This bit field is fixed to $C0_H$.
MOD_NUMBER	31:16	r	**Module Number Value** This bit field defines the module identification number.

16.8.2 Register CTR

RTC Control Register providing control means of the operation mode of the module.

CTR Address: 04_H

RTC Control Register Reset Value: $7FFF\ 0000_H$



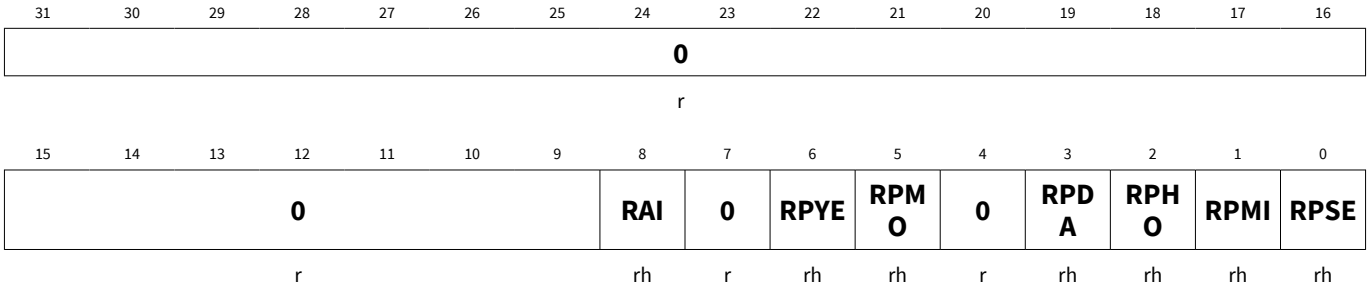
Field	Bits	Type	Description
ENB	0	rw	**RTC Module Enable** 0_B disables RTC module 1_B enables RTC module
SUS	1	rw	**Debug Suspend Control** 0_B RTC is not stopped during halting mode debug 1_B RTC is stopped during halting mode debug
DIV	31:16	rw	**Divider Value** reload value of RTC prescaler. Clock is divided by DIV+1. $7FFF_H$ is default value for RTC mode with 32.768 kHz crystal or external clock
0	15:2	r	**Reserved** Read as 0; should be written with 0

16.8.3 Register RAWSTAT

RTC Raw Service Request Register contains raw status info i.e. before status mask takes effect on generation of service requests or iterrupts. This register serves debug purpose but can be aslo used for polling of the status withou generating serice requests.

RAWSTAT Address: 08_H

RTC Raw Service Request Register Reset Value: $0000\ 0000_H$



Field	Bits	Type	Description
RPSE	0	rh	**Raw Periodic Seconds Service Request** Set whenever seconds count increments
RPMI	1	rh	**Raw Periodic Minutes Service Request** Set whenever minutes count increments

(continued)

Field	Bits	Type	Description
RPHO	2	rh	**Raw Periodic Hours Service Request** Set whenever hours count increments
RPDA	3	rh	**Raw Periodic Days Service Request** Set whenever days count increments
RPMO	5	rh	**Raw Periodic Months Service Request** Set whenever months count increments
RPYE	6	rh	**Raw Periodic Years Service Request** Set whenever years count increments
RAI	8	rh	**Alarm Service Request** Set whenever count value matches compare value
0	4, 7, 31:9	r	**Reserved**

16.8.4 Register STSSR

RTC Service Request Status Register contains status info reflecting status mask effect on generation of service requests or iterrupts. This register needs to be accessed by software in order to determine the actual cause of an event.

STSSR Address: $0C_H$

RTC Service Request Status Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0							**SAI**	**0**	**SPYE**	**SPMO**	**0**	**SPDA**	**SPHO**	**SPMI**	**SPSE**
r							rh	r	rh	rh	r	rh	rh	rh	rh

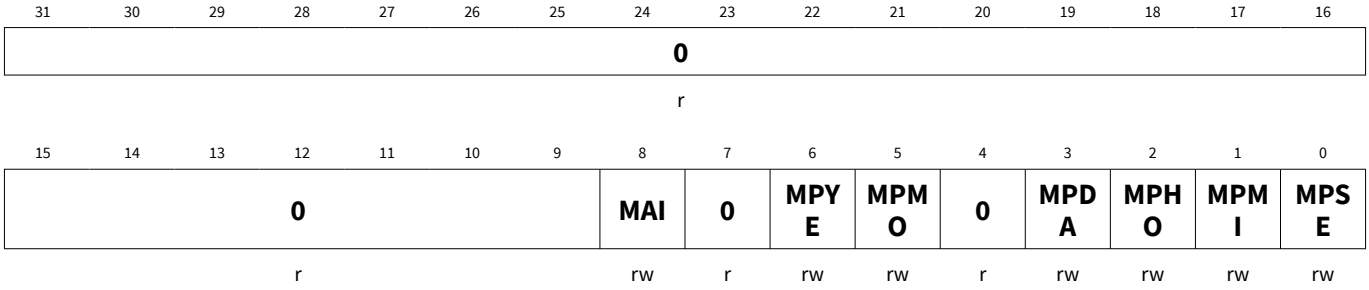
Field	Bits	Type	Description
SPSE	0	rh	**Periodic Seconds Service Request Status after masking**
SPMI	1	rh	**Periodic Minutes Service Request Status after masking**
SPHO	2	rh	**Periodic Hours Service Request Status after masking**
SPDA	3	rh	**Periodic Days Service Request Status after masking**
SPMO	5	rh	**Periodic Months Service Request Status after masking**
SPYE	6	rh	**Periodic Years Service Request Status after masking**
SAI	8	rh	**Alarm Service Request Status after masking**
0	4, 7, 31:9	r	**reserved**

16.8.5 Register MSKSR

RTC Service Request Mask Register contains masking value for generation control of service requests or iterrupts.

MSKSR Address: 10_H

RTC Service Request Mask Register Reset Value: $0000\ 0000_H$



Field	Bits	Type	Description
MPSE	0	rw	**Periodic Seconds Interrupt Mask** 0_B disable interrupt 1_B enable interrupt
MPMI	1	rw	**Periodic Minutes Interrupt Mask** 0_B disable interrupt 1_B enable interrupt
MPHO	2	rw	**Periodic Hours Interrupt Mask** 0_B disable interrupt 1_B enable interrupt
MPDA	3	rw	**Periodic Days Interrupt Mask** 0_B disable interrupt 1_B enable interrupt
MPMO	5	rw	**Periodic Months Interrupt Mask** 0_B disable interrupt 1_B enable interrupt
MPYE	6	rw	**Periodic Years Interrupt Mask** 0_B disable interrupt 1_B enable interrupt
MAI	8	rw	**Alarm Interrupt Mask** 0_B disable interrupt 1_B enable interrupt
0	4, 7, 31:9	r	**Reserved**

16.8.6 Register CLRSR

RTC Clear Service Request Register serves purpose of clearing sticky bits of ***RAWSTAT*** and ***STSSR*** registers. Write one to a bit in order to clear the status bit. Writing zero has no effect on the set nor reset bits.

CLRSR Address: 14_H

RTC Clear Service Request Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0							RAI	0	RPYE	RPMO	0	RPDA	RPHO	RPMI	RPSE
r							w	r	w	w	r	w	w	w	w

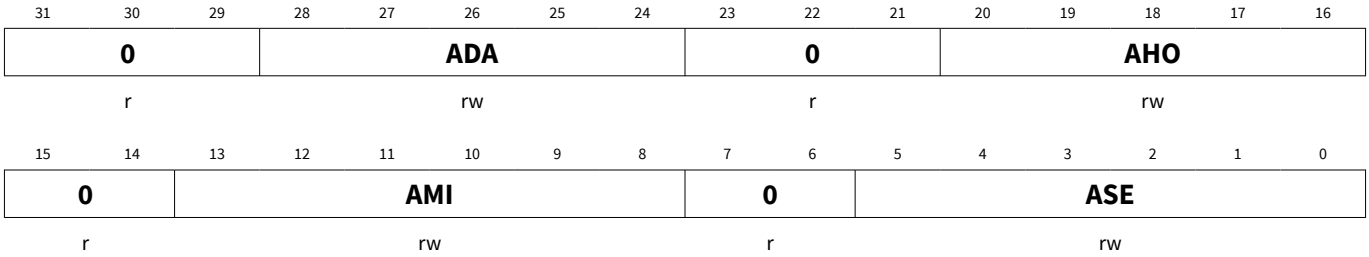
Field	Bits	Type	Description
RPSE	0	w	**Raw Periodic Seconds Interrupt Clear** 0_B no effect 1_B clear status bit
RPMI	1	w	**Raw Periodic Minutes Interrupt Clear** 0_B no effect 1_B clear status bit
RPHO	2	w	**Raw Periodic Hours Interrupt Clear** 0_B no effect 1_B clear status bit
RPDA	3	w	**Raw Periodic Days Interrupt Clear** 0_B no effect 1_B clear status bit
RPMO	5	w	**Raw Periodic Months Interrupt Clear** 0_B no effect 1_B clear status bit
RPYE	6	w	**Raw Periodic Years Interrupt Clear** 0_B no effect 1_B clear status bit
RAI	8	w	**Raw Alarm Interrupt Clear** 0_B no effect 1_B clear status bit
0	4, 7, 31:9	r	**Reserved**

16.8.7 Register ATIM0

RTC Alarm Time Register 0 serves purpose of programming single alarm time at a desired point of time reflecting comparison against ***TIM0*** register. The ATM0 register contains portion of bit fields for seconds, minutes, hours and days. Upon attempts to write an invalid value to a bit bield e.g. exceeding maximum value a default value gets programmed as described for each individual bit fields.

ATIM0 Address: 18_H

RTC Alarm Time Register 0 Reset Value: $0000\ 0000_H$



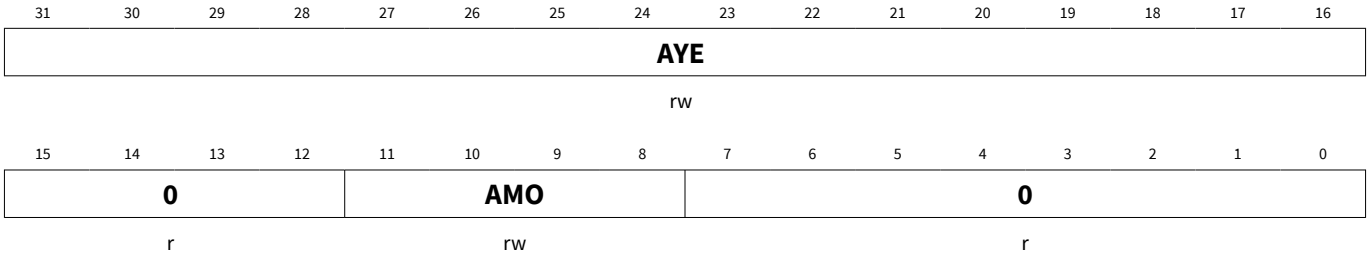
Field	Bits	Type	Description
ASE	5:0	rw	**Alarm Seconds Compare Value** Match of seconds timer count to this value triggers alarm seconds interrupt. Setting value equal or above $3C_H$ results in setting the field value to 0_H
AMI	13:8	rw	**Alarm Minutes Compare Value** Match of minutes timer count to this value triggers alarm minutes interrupt. Setting value equal or above $3C_H$ results in setting the field value to 0_H
AHO	20:16	rw	**Alarm Hours Compare Value** Match of hours timer count to this value triggers alarm hours interrupt. Setting value equal or above 18_H results in setting the field value to 0_H
ADA	28:24	rw	**Alarm Days Compare Value** Match of days timer count to this value triggers alarm days interrupt. Setting valueequal above $1F_H$ results in setting the field value to 0_H
0	7:6, 15:14, 23:21, 31:29	r	**Reserved**

16.8.8 Register ATIM1

RTC Alarm Time Register 1 serves purpose of programming single alarm time at a desired point of time reflecting comparison against ***TIM1*** register. The ATM1 register contains portion of bit fields for months and years. Upon attempts to write an invalid value to a bit bield e.g. exceeding maximum value a default value gets programmed as described for each individual bit fields.

ATIM1 Address: $1C_H$

RTC Alarm Time Register 1 Reset Value: $0000\ 0000_H$



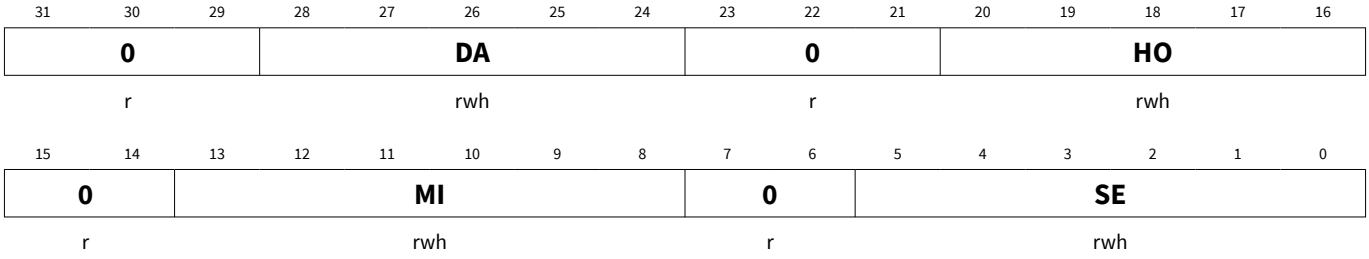
Field	Bits	Type	Description
AMO	11:8	rw	**Alarm Month Compare Value** Match of months timer count to this value triggers alarm month interrupt. Setting value equal or above the number of days of the actual month count results in setting the field value to 0_H
AYE	31:16	rw	**Alarm Year Compare Value** Match of years timer count to this value triggers alarm years interrupt.
0	7:0, 15:12	r	**Reserved**

16.8.9 Register TIM0

RTC Time Register 0 contains current time value for seconds, minutes, hours and days. The bit fields get updated in intervals corresponding with their meaning accordingly. The register needs to be programmed to reflect actual time after initial power up and will continue counting time also while in sleep or deep sleep mode if enabled. Upon attempts to write an invalid value to a bit bield e.g. exceeding maximum value a default value gets programmed as described for each individual bit fields.

TIM0 Address: 20_H

RTC Time Register 0 Reset Value: $0000\ 0000_H$



Field	Bits	Type	Description
SE	5:0	rwh	**Seconds Time Value** Setting value equal or above $3C_H$ results in setting the field value to 0_H. Value can only be written, when RTC is disabled via bit CTR.ENB.

(continued)

Field	Bits	Type	Description
MI	13:8	rwh	**Minutes Time Value** Setting value equal or above $3C_H$ results in setting the field value to 0_H. Value can only be written, when RTC is disabled via bit CTR.ENB.
HO	20:16	rwh	**Hours Time Value** Setting value equal or above 18_H results in setting the field value to 0_H Value can only be written, when RTC is disabled via bit CTR.ENB.
DA	28:24	rwh	**Days Time Value** Setting value equal or above the number of days of the actual month count results in setting the field value to 0_H Value can only be written, when RTC is disabled via bit CTR.ENB. Days counter starts with value 0 for the first day of month.
0	7:6, 15:14, 23:21, 31:29	r	**Reserved**

16.8.10 Register TIM1

RTC Time Register 1 contains current time value for days of week, months and years. The bit fields get updated in intervals corresponding with their meaning accordingly. The register needs to be programmed to reflect actual time after initial power up and will continue counting time also while in sleep or deep sleep if enabled. Upon attempts to write an invalid value to a bit bield e.g. exceeding maximum value a default value gets programmed as described for each individual bit fields.

TIM1 Address: 24_H

RTC Time Register 1 Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
YE															
rwh															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				**MO**				**0**					**DAWE**		
r				rwh				r					rwh		

Field	Bits	Type	Description
DAWE	2:0	rwh	**Days of Week Time Value** Setting value above 6_H results in setting the field value to 0_H Value can only be written, when RTC is disabled via bit CTR.ENB. Days counter starts with value 0 for the first day of week.

(continued)

Field	Bits	Type	Description
MO	11:8	rwh	**Month Time Value** Setting value equal or above C_H results in setting the field value to 0_H. Value can only be written, when RTC is disabled via bit CTR.ENB. Months counter starts with value 0 for the first month of year.
YE	31:16	rwh	**Year Time Value** Value can only be written, when RTC is disabled.
0	7:3, 15:12	r	**Reserved**

16.9 Interconnects

Table 182 Pin Connections

Input/Output	I/O	Connected To	Description
Clock Signals			
f_{RTC}	I	SCU.CCU	32.768 kHz clock selected
Debug Signals			
HALTED	I	CPU	Indicates the processor is in debug state and halted
Service Request Connectivity			
periodic_event	O	SCU.GCU	Timer periodic service request
alarm	O	SCU.GCU	Alarm service request

17 Pseudo Random Number Generator (PRNG)

17.1 Overview

The pseudo random bit generator (PRNG) provides random data with fast generation times.

17.1.1 Features

The PRNG includes the following features:

- Fast random data generation times:
  - 17 to 18 clock cycles generation time for 16-bit random data
  - 9 to 10 clock cycles generation time for 8-bit random data
- Fulfills statistical tests according to NIST-800

17.2 Description of Operation Modes

17.2.1 Key Loading Mode

Before the PRNG can be used it has to be initialized by the user software.

The key (seed) k of the PRNG is a bit string $k = (k_{n-1}, k_{n-2}, ..., k_2, k_1, k_0)$ of length n. A key length of 80 bits is recommended, although smaller or larger key lengths are possible. It is recommended to use chip individual seed values.

The initialization of the PRNG consists of two basic phases:

1. Key loading
2. Warm-up

Key loading is initialized by setting the bit ***PRNG_CTRL***.KLD to "1". In the key loading mode, ***PRNG_WORD*** acts always as a 16 bit destination register. The p partial words W_i (0 <= i < p) of the key $k = (W_{p-1}, ..., W_1, W_0)$, with $W_i = (k_{15}, ..., k_1, k_0)$, are sequentially written to ***PRNG_WORD*** in the order $W_0, W_1, ..., W_{p-1}$. A useful seed size is 80 bits (i.e., 5 data words, p=5). Because the bits of the partial key word are sequentially loaded into the internal state of the PRNG, loading of a key word will take 16 clock cycles. The ***PRNG_CHK***.RDV flag is set to "0" while loading is in progress. A flag value of "1" indicates that the next partial key word can be written to ***PRNG_WORD***.

After the complete key has been loaded, the ***PRNG_CTRL***.KLD flag must be set to "0" to prepare the following warm-up phase. This operation takes one clock cycle.

The warm-up phase provides a thorough diffusion of the key bits. For this purpose the user must read and discard 64 random bits from the register ***PRNG_WORD***. The random data output block must be set to either b = 8 or 16 bits. This is achieved by setting the corresponding value of the ***PRNG_CTRL***.RDBS field.

The flag ***PRNG_CHK***.RDV set to "1" indicates that the next random data block of width b can be read from ***PRNG_WORD***.

If, for any reason, ***PRNG_CTRL***.RDBS is reset to the default value of 00_B, the PRNG must be initialized once more – i.e., a key must be loaded and a warm-up phase carried out.

17.2.2 Streaming Mode

The flag ***PRNG_CHK***.RDV set to 1_B indicates that the next random data block can be read from ***PRNG_WORD***. After a word has been read the flag ***PRNG_CHK***.RDV is reset to 0_B by the hardware and generation of new random bits starts. The PRNG requires 17–18 clock cycles to generate a 16 random bits and 9–10 clock cycles to generate eight random bits. From a software point of view it is not necessary to poll the ***PRNG_CHK***.RDV flag. Consecutive read accesses to ***PRNG_WORD*** will be delayed automatically by hardware as long as ***PRNG_CHK***.RDV is "0".

The width of the output data block is changed by setting the value of ***PRNG_CTRL***.RDBS. This should be done before entering streaming mode, otherwise if the change is made during streaming, the new setting will not come into effect until the next generation cycle is started. The hardware checks that the selected number of bits are available and the flag ***PRNG_CHK***.RDV is set when this condition is true.

In order to avoid reading a duplicate random byte when switching from 8-bit to 16-bit operation mode the last byte generated in the 8-bit mode should first be discarded before switching to 16-bit mode.

Note: PRNG_WORD should be accessed as 16 bit register, the upper 16 bits (of a 32 bit access) are ignored on a write and zeroes on a read and therefore contains no random data.

17.2.3 Refreshing and Restarting a Random Bit Stream

The random bit sequence can be refreshed with a new key. In this case the entropy contained in the last internal state is not cleared, but instead the new key is mixed into the current PRNG state. This is referred to as refreshing.

Refreshing is a means of introducing additional entropy into the generation of the random bit sequence. Without refreshing, the entire entropy rests in the inital key (or seed) that was used for initializing the PRNG during first key loading. Thereafter, the generation of the random bit sequence is purely deterministic. The deterministic process is broken whenever refreshing is performed. Refreshing implies that it is not possible to reproduce the same random result using the same key for data generation.

Since the internal state of the PRNG cannot be read and set directly, a sequence cannot be restored from any given state. A random bit sequence based on a certain initial key can, however, be continued. To this means, a segment s of the output sequence is stored and this segment is used as a initial key later on. The segment $s = (s_{n-1}, s_{n-2}, ..., s_2, s_1, s_0)$of length n should be fresh – i.e., generated after the last bits used in the application. The length of s should be at least n = 80 bits. This way a pseudorandom bit sequence can be continued after a system reset without requiring new key material. This process is known as restarting.

Note: Integration in a multi-application/multitasking environment together with the requirement to obtain a reproducible pseudorandom bit sequence would necessitate a state saving and restoring feature. Hence the OS must be able to save the PRNG state before giving control to application 2 and restore the state before returning control to application 1. This is not possible with the PRNG module.

17.3 Service Request Generation

The PRNG does not generate any service request.

17.4 Debug Behavior

The PRNG does not support a suspend mode while the system is halted by the debugger. That means that the PRNG continues its operation during debug halt.

17.5 Power, Reset and Clock

The PRNG module is located in the core power domain. The module can be reset to its default state by a system reset.

The PRNG module is clocked by the main clock, MCLK, from SCU.

17.6 Initialization and System Dependencies

The PRNG is always available after reset.

Refer to ***Chapter 17.2.1*** for the initialization steps.

17.7 Registers

The interface of the PRNG comprises the registers PRNG_WORD, PRNG_CHK and PRNG_CTRL.

Table 183 Registers Address Space

Module	Base Address	End Address	Note
PRNG	$4802\ 0000_H$	$4802\ 000F_H$	

Table 184 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
Data Registers			
PRNG_WORD	PRNG word register	00_H	Page ***324***
PRNG_CHK	PRNG status check register	04_H	Page ***325***
Control Registers			
PRNG_CTRL	PRNG control register	$0C_H$	Page ***325***

Registers Access

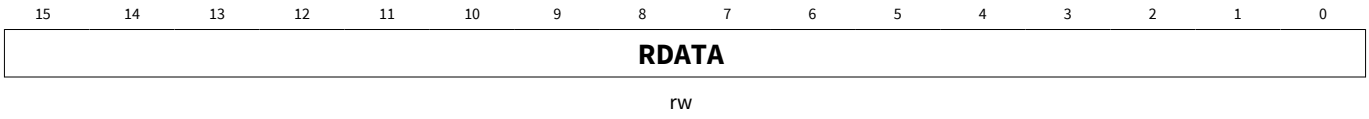
The register is addressed wordwise.

17.7.1 Data Registers

17.7.1.1 Register PRNG_WORD

PRNG_WORD Address: 00_H

PRNG Word Register Reset Value: 0000_H



Field	Bits	Type	Description
RDATA	15:0	rw	**Random Data** Random bit block or key to load. In the streaming mode the range of valid random bits is defined by the settings given by PRNG_CTRL.RDSB and the value of the flag PRNG_CHK.RDV. In the key loading mode the seed value (key) is written via this register. In this case, the key is written in units of 16 bits.

Additional Information

Notes:

1. *Reading PRNG_WORD while the PRNG is running in key loading mode (configured by setting PRNG_CTRL.KLD) will return the last value written to the register, whereas write accesses to the register while the PRNG is running in streaming mode (PRNG_CTRL.KLD = '0') will be ignored.*
2. *Write access to SFR PRNG_WORD: It is strongly recommended to wait until the SFR bit PRNG_CHK.RDV indicates that the register PRNG_WORD is ready to receive (new) data (which will be used to seed the PRNG.)*
3. *Read access to SFR PRNG_WORD: It is strongly recommended to check the SFR bit PRNG_CHK.RDV before reading SFR PRNG_WORD.*

17.7.1.2 Register PRNG_CHK

PRNG_CHK Address: 04_H

PRNG Status Check Register Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0															**RDV**
r															r

Field	Bits	Type	Description
RDV	0	r	**Random Data / Key Valid Flag** 0_B INV, New random data block is not yet ready to be read. In ***Key Loading Mode*** on page ***322***) this flag is set to 0_B while loading is in progress. 1_B VAL, Random data block is valid. In key loading mode this value indicates that the next partial key word can be written to ***PRNG_WORD***.
0	15:1	r	**Reserved**

Additional Information

*Note: If a word or byte is read from **PRNG_WORD** although the data is not ready (**PRNG_CHK**.RDV = 0_B), the system stalls until the data becomes ready.*

17.7.2 Control Registers

17.7.2.1 Register PRNG_CTRL

PRNG_CTRL Address: $0C_H$

PRNG Control Register Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0												**KLD**	**RDBS**		**0**
r												rw	rw		r

Field	Bits	Type	Description
KLD	3	rw	**Key Load Operation Mode** 0_B STRM, Streaming mode (default) 1_B KLD, Key loading mode
RDBS	2:1	rw	**Random Data Block Size** Set random data block size for read access (16 bits always used for key loading) 00_B RES, Reset state (no random data block size defined)[33], value of ***PRNG_WORD*** is undefined. 01_B BYTE, 8 bits in PRNG_WORD.RDATA[7:0] 10_B WORD, 16 bits in PRNG_WORD.RDATA[15:0] 11_B RFU, Reserved for future use, value of ***PRNG_WORD*** is undefined.
0	0	r	**Reserved**
0	15:4	r	**Reserved**

Additional Information

*Note: It is recommended not to change the **PRNG_CTRL**.KLD flag during key load. Otherwise the distribution of the bits of the PRNG will not be equal.*

33 Once the reset value for RDBS (00_B) is set, the PRNG must be fully initialized before the functionality can be used. Initialization requires key loading, followed by a warm-up phase.

18 Universal Serial Interface Channel (USIC)

The Universal Serial Interface Channel module (USIC) is a flexible interface module covering several serial communication protocols. A USIC module contains two independent communication channels named USICx_CH0 and USICx_CH1, with x being the number of the USIC module (e.g. channel 0 of USIC module 0 is referenced as USIC0_CH0). The user can program during run-time which protocol will be handled by each communication channel and which pins are used.

Table 185 Abbreviations

CTQ	Time Quanta Counter
DSU	Data Shift Unit
f_{PERIPH}	USIC module clock frequency
f_{PIN}	Input frequency to baud rate generator
MCLK	Master Clock *Note: In the USIC chapter, the module clock is referred to as f_{PERIPH}*
PPP	Protocol Pre-Processor
RSR	Receive Shift Register
SCLK	Shift Clock
TSR	Transmit Shift Register

18.1 Overview

This section gives an overview about the feature set of the USIC.

18.1.1 Features

Each USIC channel can be individually configured to match the application needs, e.g. the protocol can be selected or changed during run time without the need for a reset. The following protocols are supported:

- **UART** (ASC, asynchronous serial channel)
  - Module capability: receiver/transmitter with max. baud rate f_{PERIPH} / 4
  - Wide baud rate range down to single-digit baud rates
  - Number of data bits per data frame: 1 to 63
  - MSB or LSB first
- **LIN** Support by hardware (Local Interconnect Network)
  - Data transfers based on ASC protocol
  - Baud rate detection possible by built-in capture event of baud rate generator
  - Checksum generation under software control for higher flexibility
- **SSC/SPI** (synchronous serial channel with or without slave select lines)
  - Standard, Dual and Quad SPI format supported
  - Module capability: maximum baud rate f_{PERIPH} / 2, limited by loop delay
  - Number of data bits per data frame 1 to 63, more with explicit stop condition

  - Parity bit generation supported
  - MSB or LSB first
- **IIC** (Inter-IC Bus)
  - Application baud rate 100 kbit/s to 400 kbit/s
  - 7-bit and 10-bit addressing supported
  - Full master and slave device capability

Note: The real baud rates that can be achieved in a real application depend on the operating frequency of the device, timing parameters as described in the Data Sheet, signal delays on the PCB and timings of the peer device.

In addition to the flexible choice of the communication protocol, the USIC structure has been designed to reduce the system load (CPU load) allowing efficient data handling. The following aspects have been considered:

Data buffer capability

The standard buffer capability includes a double word buffer for receive data and a single word buffer for transmit data. This allows longer CPU reaction times (e.g. interrupt latency).

Additional FIFO buffer capability

In addition to the standard buffer capability, the received data and the data to be transmitted can be buffered in a FIFO buffer structure. The size of the receive and the transmit FIFO buffer can be programmed independently. Depending on the application needs, a total buffer capability of 64 data words can be assigned to the receive and transmit FIFO buffers of a USIC module (the two channels of the USIC module share the 64 data word buffer).

In addition to the FIFO buffer, a bypass mechanism allows the introduction of high-priority data without flushing the FIFO buffer.

Transmit control information

For each data word to be transmitted, a 5-bit transmit control information has been added to automatically control some transmission parameters, such as word length, frame length, or the slave select control for the SPI protocol. The transmit control information is generated automatically by analyzing the address where the user software has written the data word to be transmitted (32 input locations = 2^5 = 5 bit transmit control information).

This feature allows individual handling of each data word, e.g. the transmit control information associated to the data words stored in a transmit FIFO can automatically modify the slave select outputs to select different communication targets (slave devices) without CPU load. Alternatively, it can be used to control the frame length.

Flexible frame length control

The number of bits to be transferred within a data frame is independent of the data word length and can be handled in two different ways. The first option allows automatic generation of frames up to 63 bits with a known length. The second option supports longer frames (even unlimited length) or frames with a dynamically controlled length.

Interrupt capability

The events of each USIC channel can be individually routed to one of 6 service request outputs SR[5:0] available for each USIC module, depending on the application needs. Furthermore, specific start and end of frame indications are supported in addition to protocol-specific events.

Flexible interface routing

Each USIC channel offers the choice between several possible input and output pins connections for the communications signals. This allows a flexible assignment of USIC signals to pins that can be changed without resetting the device.

Input conditioning

Each input signal is handled by a programmable input conditioning stage with programmable filtering and synchronization capability.

Baud rate generation

Each USIC channel contains its own baud rate generator. The baud rate generation can be based either on the internal module clock or on an external frequency input. This structure allows data transfers with a frequency that can not be generated internally, e.g. to synchronize several communication partners.

Transfer trigger capability

In master mode, data transfers can be triggered by events generated outside the USIC module, e.g. by an input pin or a timer unit (transmit data validation). This feature allows time base related data transmission.

Debugger support

The USIC offers specific addresses to read out received data without interaction with the FIFO buffer mechanism. This feature allows debugger accesses without the risk of a corrupted receive data sequence.

To reach a desired baud rate, two criteria have to be respected, the module capability and the application environment. The module capability is defined with respect to the module's input clock frequency, being the base for the module operation. Although the module's capability being much higher (depending on the module clock and the number of module clock cycles needed to represent a data bit), the reachable baud rate is generally limited by the application environment. In most cases, the application environment limits the maximum reachable baud rate due to driver delays, signal propagation times, or due to EMI reasons.

Note: Depending on the selected additional functions (such as digital filters, input synchronization stages, sample point adjustment, data structure, etc.), the maximum reachable baud rate can be limited. Please also take care about additional delays, such as (internal or external) propagation delays and driver delays (e.g. for collision detection in ASC mode, for IIC, etc.).

A block diagram of the USIC module/channel structure is shown in ***Figure 50***.

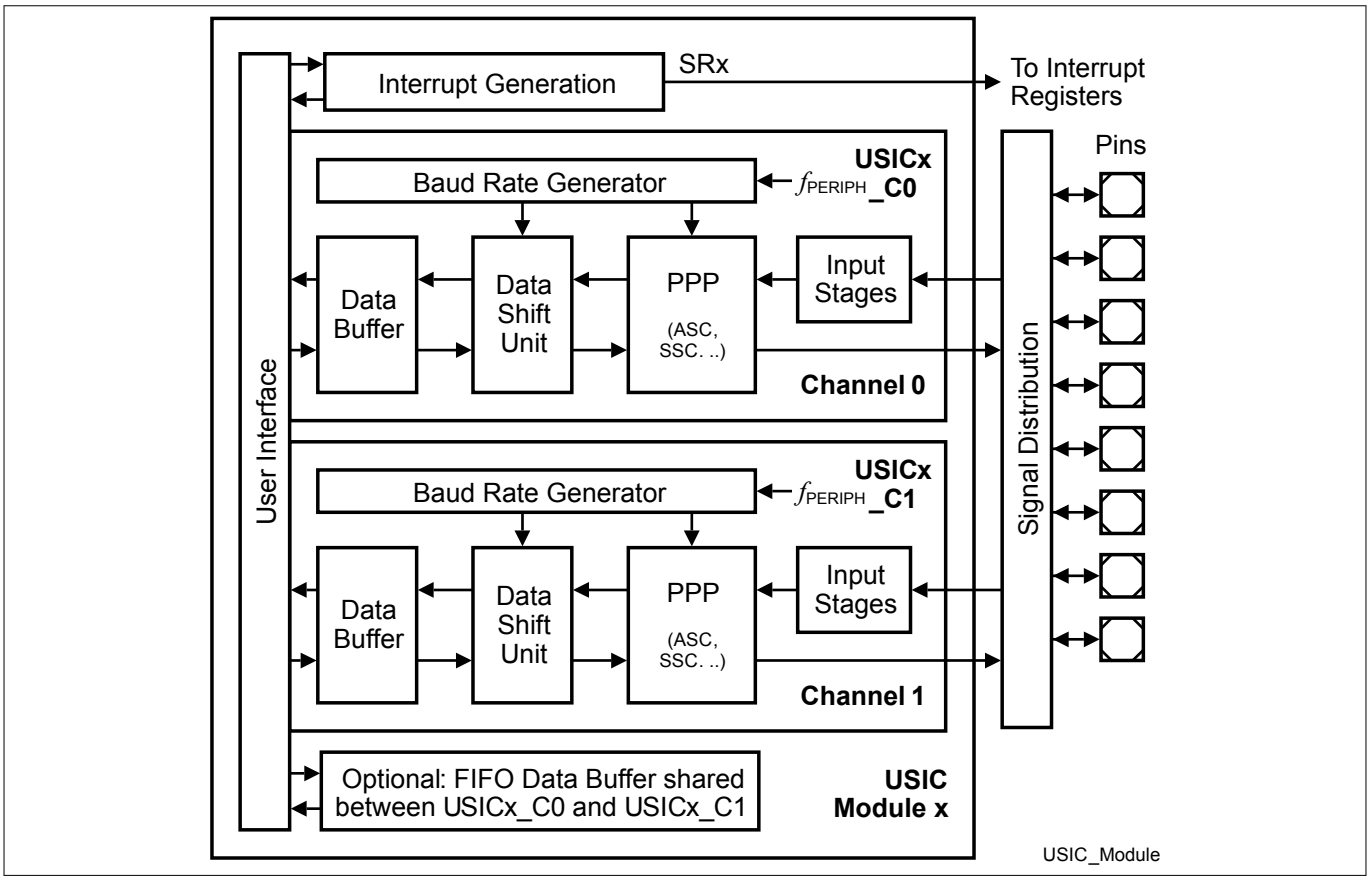


Figure 50 USIC Module/Channel Structure

18.2 Operating the USIC

This section describes how to operate the USIC communication channel.

18.2.1 USIC Structure Overview

This section introduces the USIC structure.

18.2.1.1 Channel Structure

The USIC module contains two independent communication channels, with a structure as shown in ***Figure 50***.

The data shift unit and the data buffering of each channel support full-duplex data transfers. The protocol-specific actions are handled by the protocol pre-processors (PPP). In order to simplify data handling, an additional FIFO data buffer is optionally available for each USIC module to store transmit and receive data for each channel.

Due to the independent channel control and baud rate generation, the communication protocol, baud rate and the data format can be independently programmed for each communication channel.

18.2.1.2 Input Stages

For each protocol, the number of input signals used depends on the selected protocol. Each input signal is handled by an input stage (called DXn, where n=0-5) for signal conditioning, such as input selection, polarity control, or a digital input filter. They can be classified according to their meaning for the protocols, see ***Table 186***.

The inputs marked as “optional” are not needed for the standard function of a protocol and may be used for enhancements. The descriptions of protocol-specific items are given in the related protocol chapters. For the external frequency input, please refer to the baud rate generator section, and for the transmit data validation, to the data handling section.

Table 186 Input Signals for Different Protocols

Selected Protocol	Shift Data Input(s) (handled by DX0, DX3, DX4 and DX5)[34]	Shift Clock Input (handled by DX1)	Shift Control Input (handled by DX2)
ASC, LIN	RXD	optional: external frequency input or TXD collision detection	optional: transmit data validation
Standard SSC, SPI (Master)	DIN0 (MRST, MISO)	optional: external frequency input or delay compensation	optional: transmit data validation or delay compensation
Standard SSC, SPI (Slave)	DIN0 (MTSR, MOSI)	SCLKIN	SELIN
Dual- SSC, SPI (Master)	DIN[1:0] (MRST[1:0], MISO[1:0])	optional: external frequency input or delay compensation	optional: transmit data validation or delay compensation
Dual- SSC, SPI (Slave)	DIN[1:0] (MTSR[1:0], MOSI[1:0])	SCLKIN	SELIN
Quad- SSC, SPI (Master)	DIN[3:0] (MRST[3:0], MISO[3:0])	optional: external frequency input or delay compensation	optional: transmit data validation or delay compensation
Quad- SSC, SPI (Slave)	DIN[3:0] (MTSR[3:0], MOSI[3:0])	SCLKIN	SELIN
IIC	SDA	SCL	optional: transmit data validation

Note: To allow a certain flexibility in assigning required USIC input functions to port pins of the device, each input stage can select the desired input location among several possibilities.

The available USIC signals and their port locations are listed in the interconnects section, see ***Interconnects*** *on page 504.*

34 ASC, IIC and standard SSC protocols use only DX0 as the shift data input.

18.2.1.3 Output Signals

For each protocol, up to 14 protocol-related output signals are available. The number of actually used outputs depends on the selected protocol. They can be classified according to their meaning for the protocols, see ***Table 187***.

The outputs marked as “optional” are not needed for the standard function of a protocol and may be used for enhancements. The descriptions of protocol-specific items are given in the related protocol chapters.

The MCLKOUT output signal has a stable frequency relation to the shift clock output (the frequency of MCLKOUT can be higher than for SCLKOUT) for synchronization purposes of a slave device to a master device. If the baud rate generator is not needed for a specific protocol (e.g. in SSC slave mode), the SCLKOUT and MCLKOUT signals can be used as clock outputs with 50% duty cycle with a frequency that can be independent from the communication baud rate.

Table 187 Output Signals for Different Protocols

Selected Protocol	Shift Data Output(s) DOUT[3:0][35)]	Shift Clock Output SCLKOUT	Shift Control Outputs SELO[7:0]	Master Clock Output MCLKOUT
ASC, LIN	TXD	not used	not used	optional: master time base
Standard SSC, SPI (Master)	DOUT0 (MTSR, MOSI)	master shift clock	slave select, chip select	optional: master time base
Standard SSC, SPI (Slave)	DOUT0 (MRST, MISO)	optional: independent clock output	not used	optional: independent clock output
Dual- SSC, SPI (Master)	DOUT[1:0] (MTSR[1:0], MOSI[1:0])	master shift clock	slave select, chip select	optional: master time base
Dual- SSC, SPI (Slave)	DOUT[1:0] (MRST[1:0], MISO[1:0])	optional: independent clock output	not used	optional: independent clock output
Quad- SSC, SPI (Master)	DOUT[3:0] (MTSR[3:0], MOSI[3:0])	master shift clock	slave select, chip select	optional: master time base
Quad- SSC, SPI (Slave)	DOUT[3:0] (MRST[3:0], MISO[3:0])	optional: independent clock output	not used	optional: independent clock output
IIC	SDA	SCL	not used	optional: master time base

Note: To allow a certain flexibility in assigning required USIC output functions to port pins of the device, most output signals are made available on several port pins. The port control itself defines pin-by-pin which signal is used as output signal for a port pin (see port chapter).

35 ASC, IIC and standard SSC protocols use only DOUT0 as the shift data output.

The available USIC signals and their port locations are listed in the interconnects section, see ***Interconnects*** *on page 504.*

18.2.1.4 Baud Rate Generator

Each USIC Channel contains a baud rate generator structured as shown in ***Figure 51***. It is based on coupled divider stages, providing the frequencies needed for the different protocols. It contains:

- A fractional divider to generate the input frequency $f_{PIN} = f_{FD}$ for baud rate generation based on the internal system frequency f_{PERIPH}.
- The DX1 input to generate the input frequency $f_{PIN} = f_{DX1}$ for baud rate generation based on an external signal.
- Two protocol-related counters: the divider mode counter to provide the master clock signal MCLK, the shift clock signal SCLK, and other protocol-related signals; and the capture mode timer for time interval measurement, e.g. baud rate detection.
- A time quanta counter associated to the protocol pre-processor defining protocol-specific timings, such shift control signals or bit timings, based on the input frequency f_{CTQIN}.
- The output signals MCLKOUT and SCLKOUT of the protocol-related divider that can be made available on pins. In order to adapt to different applications, some output characteristics of these signals can be configured.

  For device-specific details about availability of USIC signals on pins refer to the interconnects section.

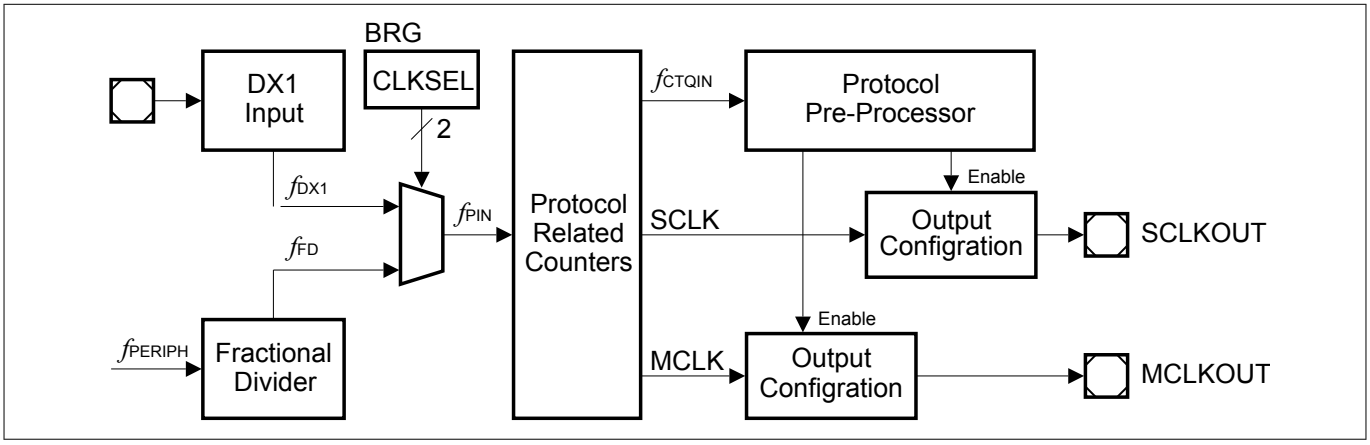


Figure 51 Baud Rate Generator

18.2.1.5 Channel Events and Interrupts

The notification of the user about events occurring during data traffic and data handling is based on:

- Data transfer events related to the transmission or reception of a data word, independent of the selected protocol.
- Protocol-specific events depending on the selected protocol.
- Data buffer events related to data handling by the optional FIFO data buffers.

18.2.1.6 Data Shifting and Handling

The data handling of the USIC module is based on an independent data shift unit (DSU) and a buffer structure that is similar for the supported protocols. The data shift and buffer registers are 16-bit wide (maximum data word length), but several data words can be concatenated to achieve longer data frames. The DSU inputs are

the shift data (handled by input stage DX0, DX3, DX4 and DX5), the shift clock (handled by the input stage DX1), and the shift control (handled by the input stage DX2). The signal DOUT[3:0] represents the shift data outputs.

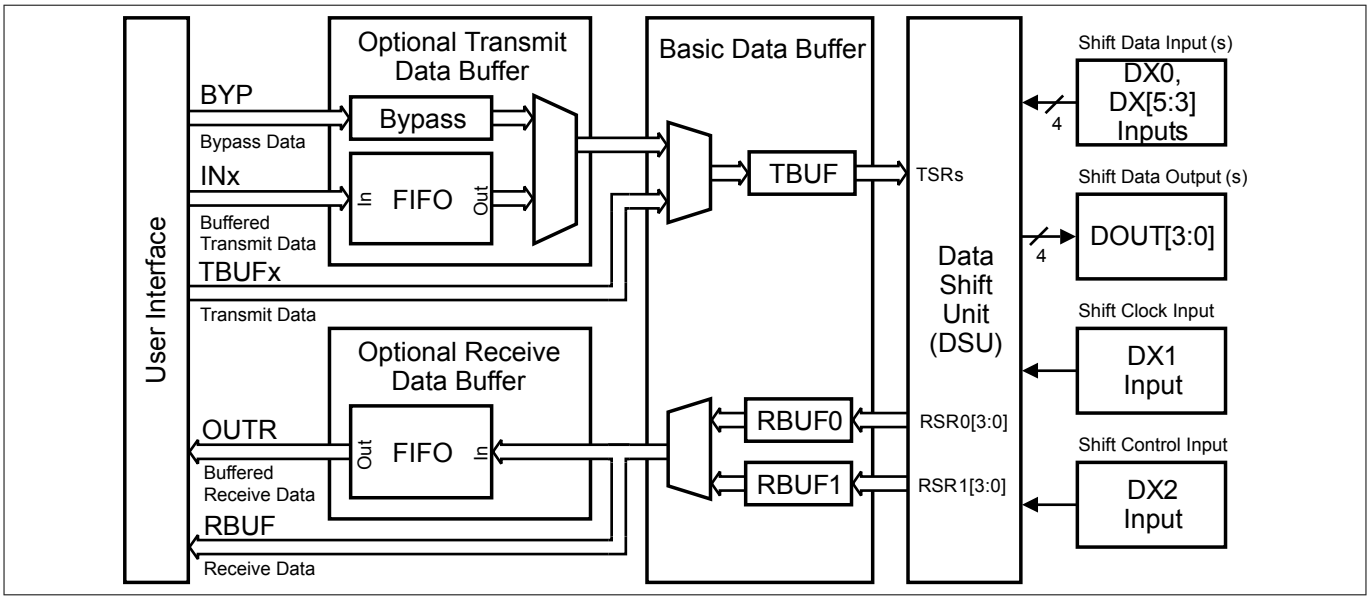


Figure 52 Principle of Data Buffering

The principle of data handling comprises:

- A transmitter with transmit shift registers (TSR and TSR[3:0]) in the DSU and a transmit data buffer (TBUF). A data validation scheme allows triggering and gating of data transfers by external events under certain conditions.
- A receiver with two alternating sets of receive shift registers (RSR0[3:0] and RSR1[3:0]) in the DSU and a double receive buffer structure (RBUF0, RBUF1). The alternating receive shift registers support the reception of data streams and data frames longer than one data word.
- A user interface to handle data, interrupts, and status and control information.

18.2.1.6.1 Basic Data Buffer Structure

The read access to received data and the write access of data to be transmitted can be handled by a basic data buffer structure.

The received data stored in the receiver buffers RBUF0/RBUF1 can be read directly from these registers. In this case, the user has to take care about the reception sequence to read these registers in the correct order. To simplify the use of the receive buffer structure, register RBUF has been introduced. A read action from this register delivers the data word received first (oldest data) to respect the reception sequence. With a read access from at least the low byte of RBUF, the data is automatically declared to be no longer new and the next received data word becomes visible in RBUF and can be read out next.

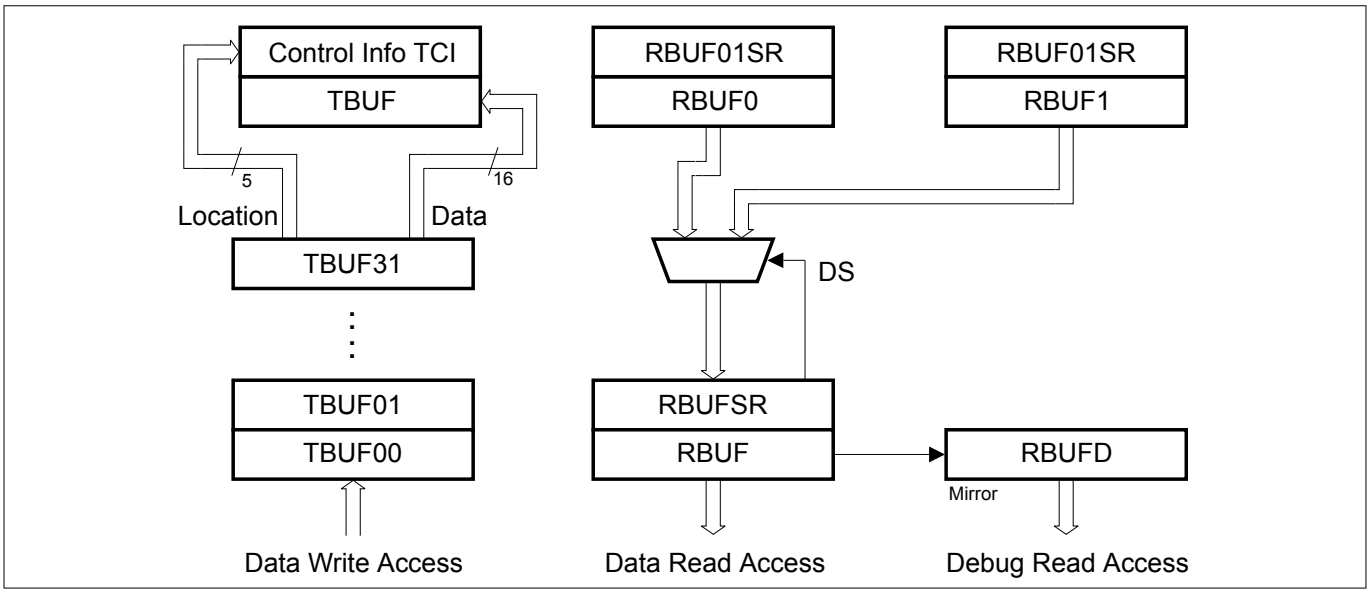


Figure 53 Data Access Structure without additional Data Buffer

It is recommended to read the received data words by accesses to RBUF and to avoid handling of RBUF0 and RBUF1. The USIC module also supports the use of debug accesses to receive data words. Debugger read accesses should not disturb the receive data sequence and, as a consequence, should not target RBUF. Therefore, register RBUFD has been introduced. It contains the same value as RBUF, but a read access from RBUFD does not change the status of the data (same data can be read several times). In addition to the received data, some additional status information about each received data word is available in the receiver buffer status register RBUF01SR (related to data in RBUF0 and RBUF1) and RBUFSR (related to data in RBUF).

Transmit data can be loaded to TBUF by software by writing to the transmit buffer input locations TBUFx (x = 00-31), consisting of 32 consecutive addresses. The data written to one of these input locations is stored in the transmit buffer TBUF. Additionally, the address of the written location is evaluated and can be used for additional control purposes. This 5-bit wide information (named Transmit Control Information TCI) can be used for different purposes in different protocols.

18.2.1.6.2 FIFO Buffer Structure

To allow easier data setup and handling, an additional data buffering mechanism can be optionally supported. The data buffer is based on the first-in-first-out principle (FIFO) that ensures that the sequence of transferred data words is respected.

If a FIFO buffer structure is used, the data handling scheme (data with associated control information) is similar to the one without FIFO. The additional FIFO buffer can be independently enabled/disabled for transmission and reception (e.g. if data FIFO buffers are available for a specific USIC channel, it is possible to configure the transmit data path without and the receive data path with FIFO buffering).

The transmit FIFO buffer is addressed by using 32 consecutive address locations for INx instead of TBUFx (x=00-31) regardless of the FIFO depth. The 32 addresses are used to store the 5-bit TCI (together with the written data) associated with each FIFO entry.

The receive FIFO can be read out at two independent addresses, OUTR and OUTDR instead of RBUF and RBUFD. A read from the OUTR location triggers the next data packet to be available for the next read (general FIFO mechanism). In order to allow non-intrusive debugging (without risk of data loss), a second address location (OUTDR) has been introduced. A read at this location delivers the same value as OUTR, but without modifying the FIFO contents.

The transmit FIFO also has the capability to bypass the data stream and to load bypass data to TBUF. This can be used to generate high-priority messages or to send an emergency message if the transmit FIFO runs empty.

The transmission control of the FIFO buffer can also use the transfer trigger and transfer gating scheme of the transmission logic for data validation (e.g. to trigger data transfers by events).

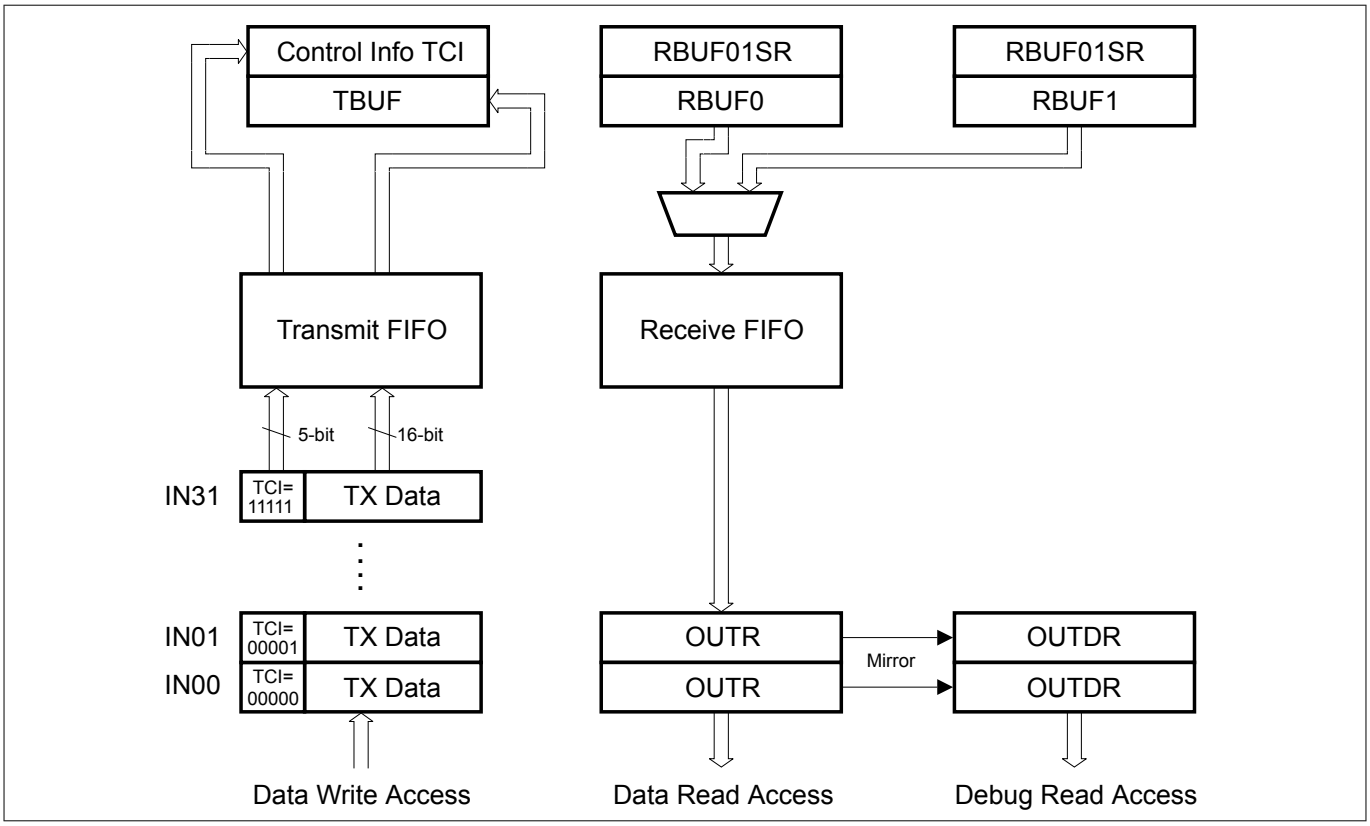


Figure 54 Data Access Structure with FIFO

18.2.2 Operating the USIC Communication Channel

This section describes how to operate a USIC communication channel, including protocol control and status, and mode control. The following aspects have to be taken into account:

- Enable the USIC module for operation and configure the behavior for the different device operation modes (see ***Mode Control*** on page 337).
- Configure the pinning (refer to description in the corresponding protocol section).
- Configure the data structure (shift direction, word length, frame length, polarity, etc.).
- Configure the data buffer structure of the optional FIFO buffer area.
- Select a protocol by CCR.MODE.

18.2.2.1 Protocol Control and Status

The protocol-related control and status information are located in the protocol control register PCR and in the protocol status register PSR. These registers are shared between the available protocols. As a consequence, the meaning of the bit positions in these registers is different within the protocols.

Use of PCR Bits

The signification of the bits in register PCR is indicated by the protocol-related alias names for the different protocols.

- PCR for the ASC protocol (see page ***450***)
- PCR for the SSC protocol (see page ***453***)
- PCR for the IIC protocol (see page ***455***)

Use of PSR Flags

The signification of the flags in register PSR is indicated by the protocol-related alias names for the different protocols.

- PSR flags for the ASC protocol (see page ***459***)
- PSR flags for the SSC protocol (see page ***461***)
- PSR flags for the IIC protocol (see page ***463***)

18.2.2.2 Mode Control

The mode control concept for system control tasks, such as suspend request for debugging, allows to program the module behavior under different device operating conditions.

The behavior of a communication channel can be programmed for each of the device operating modes (normal operation, suspend mode). Therefore, each communication channel has an associated kernel state configuration register KSCFG defining its behavior in the following operating modes:

Normal operation

This operating mode is the default operating mode when no suspend request is pending. The module clock is not switched off and the USIC registers can be read or written. The channel behavior is defined by KSCFG.NOMCFG.

Suspend mode

This operating mode is requested when a suspend request is pending in the device. The module clock is not switched off and the USIC registers can be read or written. The channel behavior is defined by KSCFG.SUMCFG.

The four kernel modes defined by the register KSCFG are shown in ***Table 188***.

Table 188 USIC Communication Channel Behavior

Kernel Mode	Channel Behavior	KSCFG.NOMCFG/SUMCFG
Run mode 0	Channel operation as specified, no impact on data transfer	00_B
Run mode 1		01_B
Stop mode 0	Explicit stop condition as described in the protocol chapters	10_B
Stop mode 1		11_B

Generally, bit field KSCFG.NOMCFG should be configured for run mode 0 as default setting for standard operation. The definition of each kernel mode may differ across protocols and is described in the respective protocol's section on mode control behaviour.

If a communication channel should not react to a suspend request (and to continue its operation as in normal mode), bit field KSCFG.SUMCFG has to be configured with the same value as KSCFG.NOMCFG.

If the communication channel should show a different behavior and stop operation when a specific stop condition is reached, the code for stop mode 0 or stop mode 1 have to be written to KSCFG.SUMCFG.

Note: The stop mode selection strongly depends on the application needs and it is very unlikely that different stop modes are required in parallel in the same application. As a result, only one stop mode type (either 0 or 1) should be used in the bit fields in register KSCFG. Do not mix stop mode 0 and stop mode 1 and avoid transitions from stop mode 0 to stop mode 1 (or vice versa) for the same communication channel.

Note: In IMC300A, bit field KSCFG.SUMCFG is reset to its default value by any reset. If the suspend function is required during debugging, it is recommended that it is enabled in the user initialization code. Before programming the bit field, the module clock has to be enabled and special care needs to be taken while enabling the module clock as described in the CCU (Clock Gating Control) section of the SCU chapter.

18.2.3 Operating the Input Stages

All input stages offer the same feature set, unless stated otherwise. They are used for all protocols, because the signal conditioning can be adapted in a very flexible way and the digital filters can be switched on and off separately.

18.2.3.1 General Input Structure

There are generally two types of input stages:

- One for the data input stages DX0, DX[5:3] (***Figure 55***)
- The other for non-data input stages DX[2:1] (***Figure 56***)

The difference is that for the data input stages, the input signal can be additionally selected from the port signal HWINn if hardware port control is enabled through CCR.HPCEN bit.

All other enable/disable functions and selections are controlled independently for each input stage by bits in the registers DXnCR.

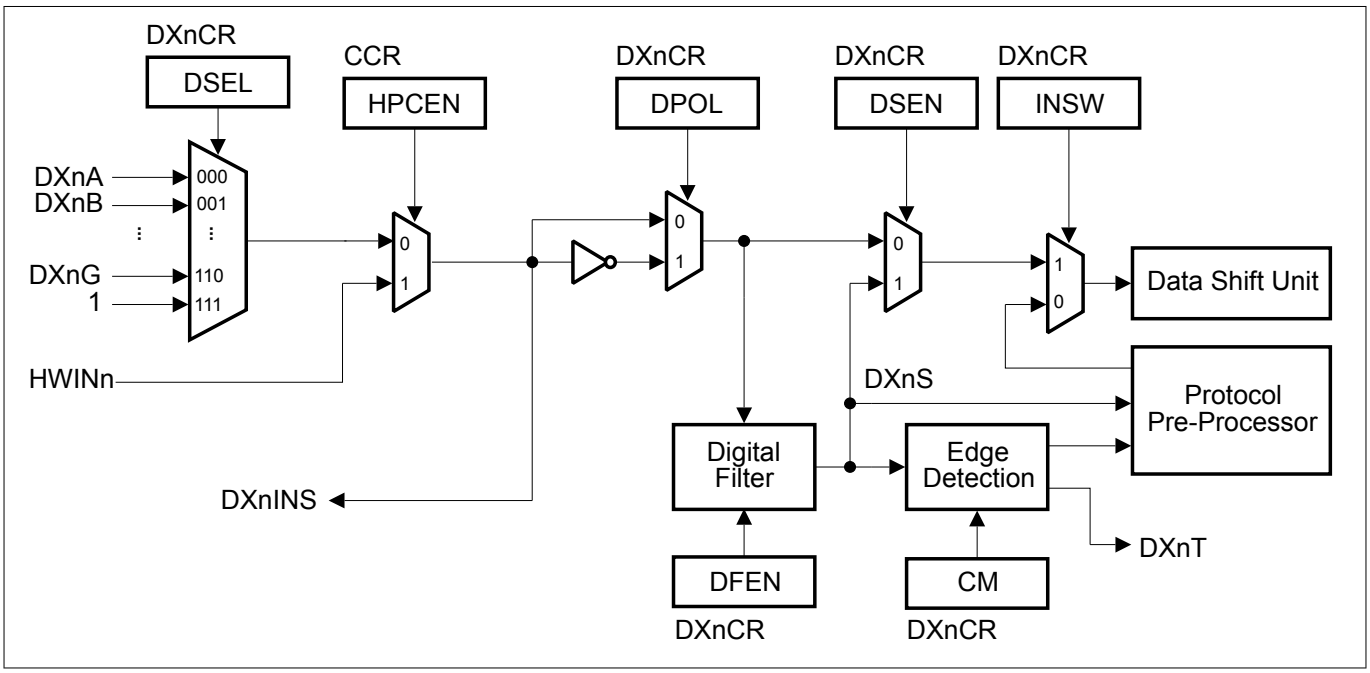


Figure 55 Input Conditioning for DX0 and DX[5:3]

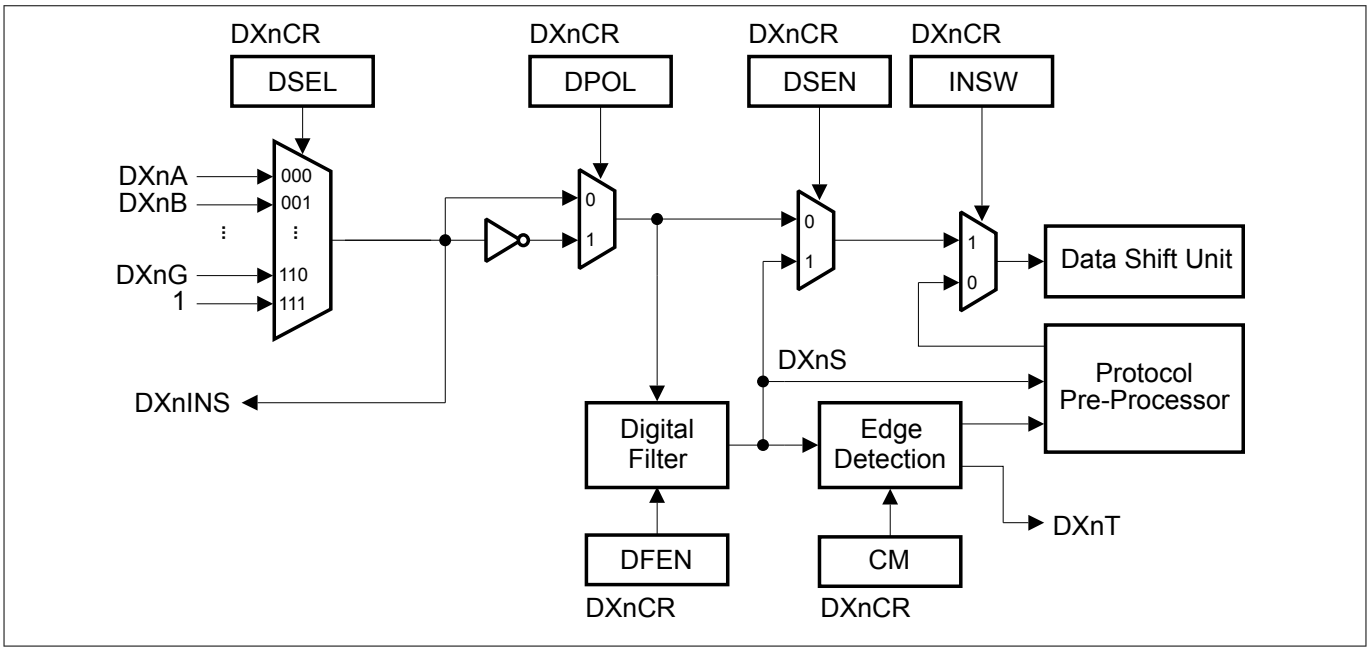


Figure 56 Input Conditioning for DX[2:1]

18.2.3.2 Input Selection

The desired input signal can be selected among the input lines DXnA to DXnG and a permanent 1-level by programming bit field DSEL (for the data input stages, hardware port control must be disabled for DSEL to take effect).

Refer to the interconnects section (***Chapter 18.11***) for the device-specific input signal assignment.

18.2.3.3 Input Conditioning

Bit DPOL allows a polarity inversion of the selected input signal to adapt the input signal polarity to the internal polarity of the data shift unit and the protocol state machine.

For some protocols, the input signals can be directly forwarded to the data shift unit for the data transfers (DSEN = 0, INSW = 1) without any further signal conditioning. In this case, the data path does not contain any delay due to synchronization or filtering.

In the case of noise on the input signals, there is the possibility to synchronize the input signal (signal DXnS is synchronized to f_{PERIPH}) and additionally to enable a digital noise filter in the signal path. The synchronized input signal (and optionally filtered if DFEN = 1) is taken into account by DSEN = 1. Please note that the synchronization leads to a delay in the signal path of 2-3 times the period of f_{PERIPH}.

If the input signals are handled by a protocol pre-processor, the data shift unit is directly connected to the protocol pre-processor by INSW = 0. The protocol pre-processor is connected to the synchronized input signal DXnS and, depending on the selected protocol, also evaluates the edges.

18.2.3.4 Digital Filter

The digital filter can be enabled to reduce noise on the input signals. Before being filtered, the input signal becomes synchronized to f_{PERIPH}. If the filter is disabled, signal DXnS corresponds to the synchronized input signal. If the filter is enabled, pulses shorter than one filter sampling period are suppressed in signal DXnS. After an edge of the synchronized input signal, signal DXnS changes to the new value if two consecutive samples of the new value have been detected.

In order to adapt the filter sampling period to different applications, it can be programmed. The first possibility is the system frequency f_{PERIPH}. Longer pulses can be suppressed if the fractional divider output frequency f_{FD} is selected. This frequency is programmable in a wide range and can also be used to determine the baud rate of the data transfers.

In addition to the synchronization delay of 2-3 periods of f_{PERIPH}, an enabled filter adds a delay of up to two filter sampling periods between the selected input and signal DXnS.

18.2.3.5 Edge Detection

The synchronized (and optionally filtered) signal DXnS can be used as input to the data shift unit and is also an input to the selected protocol pre-processor.

If the protocol pre-processor does not use the DXnS signal for protocol-specific handling, DXnS can be used for other tasks, e.g. to control data transmissions in master mode (a data word can be tagged valid for transmission, see chapter about data buffering).

A programmable edge detection indicates that the desired event has occurred by activating the trigger signal DXnT (introducing a delay of one period of f_{PERIPH} before a reaction to this event can take place).

18.2.3.6 Selected Input Monitoring

The selected input signal of each input stage has been made available with the signals DXnINS. These signals can be used in the system to trigger other actions, e.g. to generate interrupts.

18.2.3.7 Loop Back Mode

The USIC transmitter output signals can be connected to the receiver inputs of the same communication channel to form a loop back mode.

This can be done with an indirect connection through intermediate input stages (assuming these are not used by the application). For example, connecting the receiver input signal USIC0_CH0.DX0G to the transmitter output signal USIC0_CH0.DOUT0 through the DX3 input stage (DOUT0 -> DX3G -> DX3INS -> DX0G).

In the loop back mode, drivers for ASC, SSC, and IIS can be evaluated on-chip without the connections to port pins. Data transferred by the transmitter can be received by the receiver as if it would have been sent by another communication partner.

18.2.3.8 Delay Compensation in DX1

To support delay compensation in SSC and IIS protocols, the DX1 input stage additionally allows the receive shift clock to be controlled independently from the transmit shift clock through the bit DCEN, as shown in ***Figure 57***.

- When DCEN = 0, the shift clock source is selected by INSW and is the same for both receive and transmit.
- When DCEN = 1, the receive shift clock is derived from the selected input line.

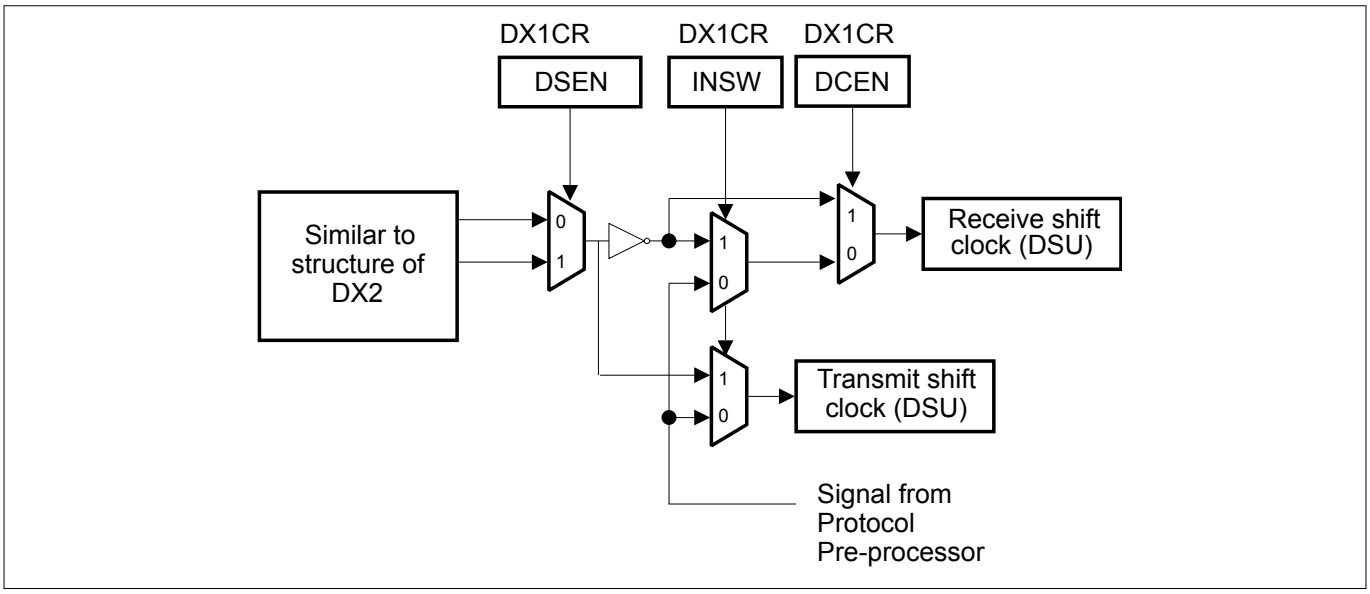


Figure 57 Delay Compensation Enable in DX1

18.2.4 Operating the Baud Rate Generator

The following blocks can be configured to operate the baud rate generator, see also ***Figure 51***.

18.2.4.1 Fractional Divider

The fractional divider generates its output frequency f_{FD} by either dividing the input frequency f_{PERIPH} by an integer factor n or by multiplication of n/1024. It has two operating modes:

Normal divider mode (FDR.DM = 01_B)

In this mode, the output frequency f_{FD} is derived from the input clock f_{PERIPH} by an integer division by a value between 1 and 1024. The division is based on a counter FDR.RESULT that is incremented by 1 with f_{PERIPH}. After reaching the value $3FF_H$, the counter is loaded with FDR.STEP and then continues counting. In order to achieve $f_{FD} = f_{PERIPH}$, the value of STEP has to be programmed with $3FF_H$.

The output frequency in normal divider mode is defined by the equation:

$$f_{FD} = f_{PERIPH} \times \frac{1}{n} \quad \text{with n = 1024 - STEP}$$

Equation 9

Fractional divider mode (FDR.DM = 10_B)

In this mode, the output frequency f_{FD} is derived from the input clock f_{PERIPH} by a fractional multiplication of n/1024 for a value of n between 0 and 1023. In general, the fractional divider mode allows to program the average output clock frequency with a finer granularity than in normal divider mode.

The frequency f_{FD} is generated by an addition of FDR.STEP to FDR.RESULT with f_{PERIPH}. The frequency f_{FD} is based on the overflow of the addition result over $3FF_H$.

The output frequency in fractional divider mode is defined by the equation:

Note: Fractional divider mode f_{FD} can introduce a maximum period jitter of one f_{PERIPH} period. This jitter is not accumulated over several cycles.

$$f_{FD} = f_{PERIPH} \times \frac{n}{1024} \quad \text{with n = STEP}$$

Equation 10

The output frequency f_{FD} of the fractional divider is selected for baud rate generation by BRG.CLKSEL = 00_B ($f_{PIN} = f_{FD}$).

18.2.4.2 External Frequency Input

The baud rate can be generated referring to an external frequency input (instead of to f_{PERIPH}) if the input stage DX1 is not needed (DX1CTR.INSW = 0) in the selected protocol.

In this case, an external frequency input signal at the DX1 input stage can be synchronized and sampled with the system frequency f_{PERIPH}. It can be optionally filtered by the digital filter in the input stage. This feature allows data transfers with frequencies that can not be generated by the device itself, e.g. for specific audio frequencies.

If BRG.CLKSEL = 10_B, the trigger signal DX1T determines f_{DX1}. In this mode, either the rising edge, the falling edge, or both edges of the input signal can be used for baud rate generation, depending on the configuration of the DX1T trigger event by bit field DX1CTR.CM. The signal MCLK toggles with each trigger event of DX1T.

If BRG.CLKSEL = 11_B, the rising edges of the input signal can be used for baud rate generation. The signal MCLK represents the synchronized input signal DX1S.

Both, the high time and the low time of external input signal must each have a length of minimum 2 periods of f_{PERIPH} to be used for baud rate generation.

18.2.4.3 Divider Mode Counter

The divider mode counter is used for an integer division delivering the output frequency f_{PDIV}. Additionally, two divider stages with a fixed division by 2 provide the output signals MCLK and SCLK with 50% duty cycle.

If the fractional divider mode is used, the maximum fractional jitter of 1 period of f_{PERIPH} can also appear in these signals. The output frequencies of this divider is controlled by register BRG.

In order to define a frequency ratio between the master clock MCLK and the shift clock SCLK, the divider stage for MCLK is located in front of the divider by PDIV+1, whereas the divider stage for SCLK is located at the output of this divider.

$$f_{MCLK} = \frac{f_{PIN}}{2}$$

Equation 11

$$f_{SCLK} = \frac{f_{PDIV}}{2}$$

Equation 12

In the case that the master clock is used as reference for external devices (e.g. for IIS components) and a fixed phase relation to SCLK and other timing signals is required, it is recommended to use the MCLK signal as input for the PDIV divider (PPPEN = 1). If the MCLK signal is not used or a fixed phase relation is not necessary, the faster frequency f_{PIN} can be selected as input frequency (PPPEN = 0).

$$f_{PDIV} = f_{PIN} \times \frac{1}{PDIV + 1} \quad \text{if PPPEN = 0}$$
$$f_{PDIV} = f_{MCLK} \times \frac{1}{PDIV + 1} \quad \text{if PPPEN = 1}$$

Equation 13

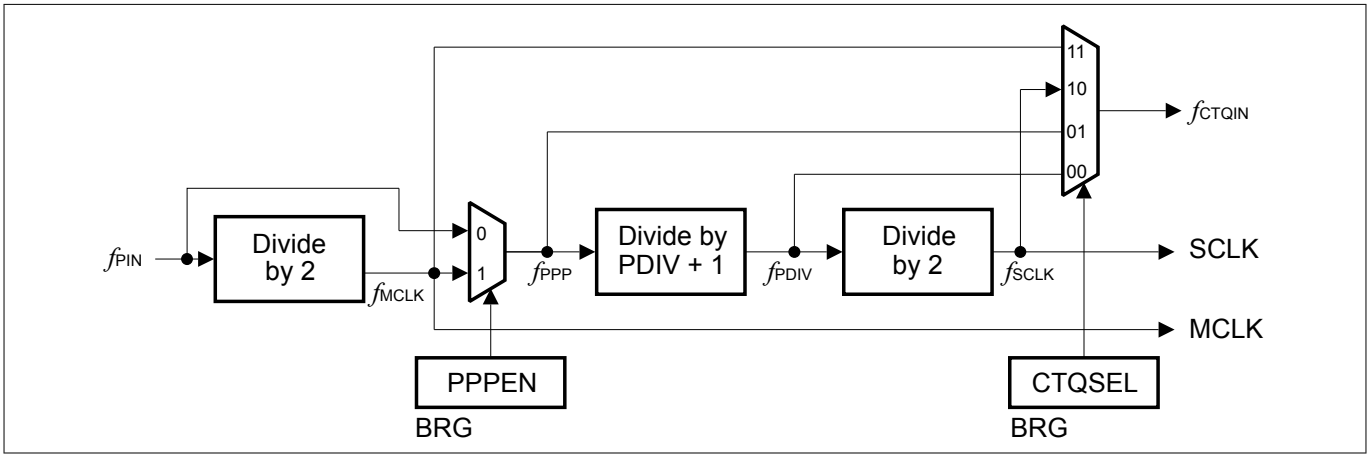


Figure 58 Divider Mode Counter

18.2.4.4 Capture Mode Timer

The capture mode timer is used for time interval measurement and is enabled by BRG.TMEN = 1. The timer works independently from the divider mode counter. Therefore, any serial data reception or transmission can continue while the timer is performing timing measurements. The timer counts f_{PPP} periods and stops counting when it reaches its maximum value. Additionally, a baud rate generator interrupt event is generated (bit PSR.BRGIF becomes set).

If an event is indicated by DX0T or DX1T, the actual timer value is captured into bit field CMTR.CTV and the timer restarts from 0. Additionally, a transmit shift interrupt event is generated (bit PSR.TSIF becomes set).

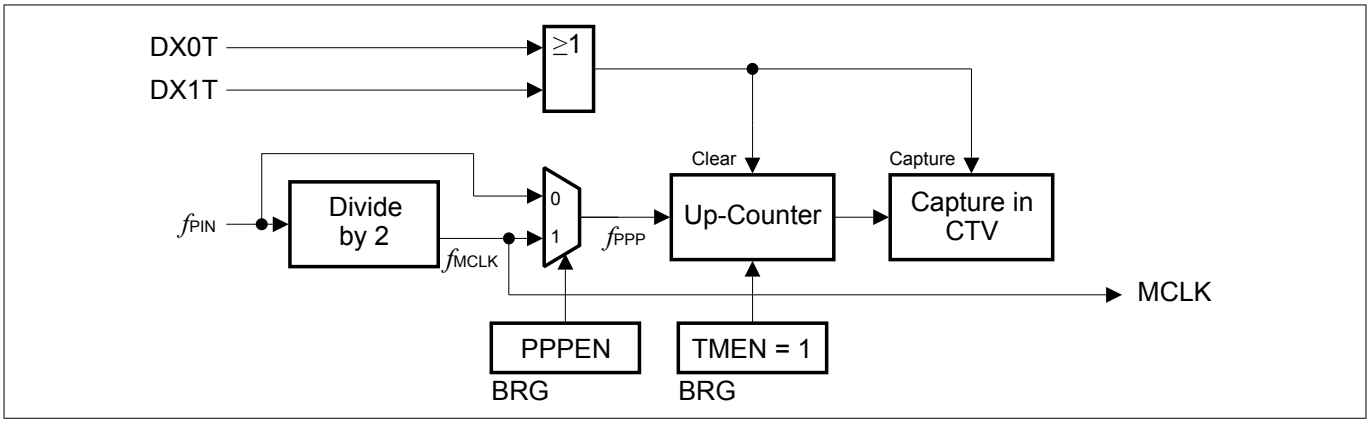


Figure 59 Protocol-Related Counter (Capture Mode)

The capture mode timer can be used to measure the baud rate in slave mode before starting or during data transfers, e.g. to measure the time between two edges of a data signal (by DX0T) or of a shift clock signal (by DX1T). The conditions to activate the DXnT trigger signals can be configured in each input stage.

18.2.4.5 Time Quanta Counter

The time quanta counter CTQ associated to the protocol pre-processor allows to generate time intervals for protocol-specific purposes. The length of a time quantum t_q is given by the selected input frequency f_{CTQIN} and the programmed pre-divider value. The meaning of the time quanta depend on the selected protocol, please refer to the corresponding chapters for more protocol-specific information.

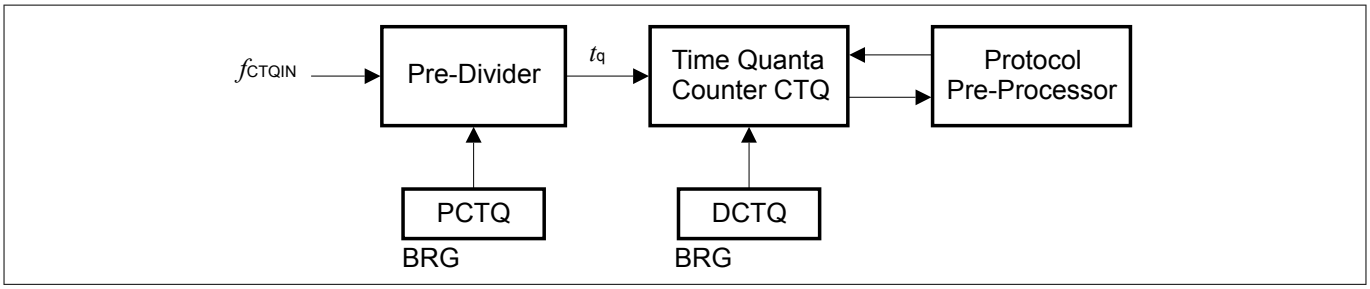


Figure 60 Time Quanta Counter

18.2.4.6 Master and Shift Clock Output Configuration

The master clock output signal MCLKOUT available at the corresponding output pin can be configured in polarity. The MCLK signal can be generated for each protocol in order to provide a kind of higher frequency time base compared to the shift clock.

The configuration mechanism of the master clock output signal MCLKOUT ensures that no shortened pulses can occur. Each MCLK period consists of two phases, an active phase, followed by a passive phase. The polarity of the MCLKOUT signal during the active phase is defined by the inverted level of bit BRG.MCLKCFG, evaluated at the start of the active phase. The polarity of the MCLKOUT signal during the passive phase is defined by bit BRG.MCLKCFG, evaluated at the start of the passive phase. If bit BRG.MCLKCFG is programmed with another value, the change is taken into account with the next change between the phases. This mechanism ensures that no shorter pulses than the length of a phase occur at the MCLKOUT output. In the example shown in ***Figure 61***, the value of BRG.MCLKCFG is changed from 0 to 1 during the passive phase of MCLK period 2.

The generation of the MCLKOUT signal is enabled/disabled by the protocol pre-processor, based on bit PCR.MCLK. After this bit has become set, signal MCLKOUT is generated with the next active phase of the MCLK period. If PCR.MCLK = 0 (MCLKOUT generation disabled), the level for the passive phase is also applied for active phase.

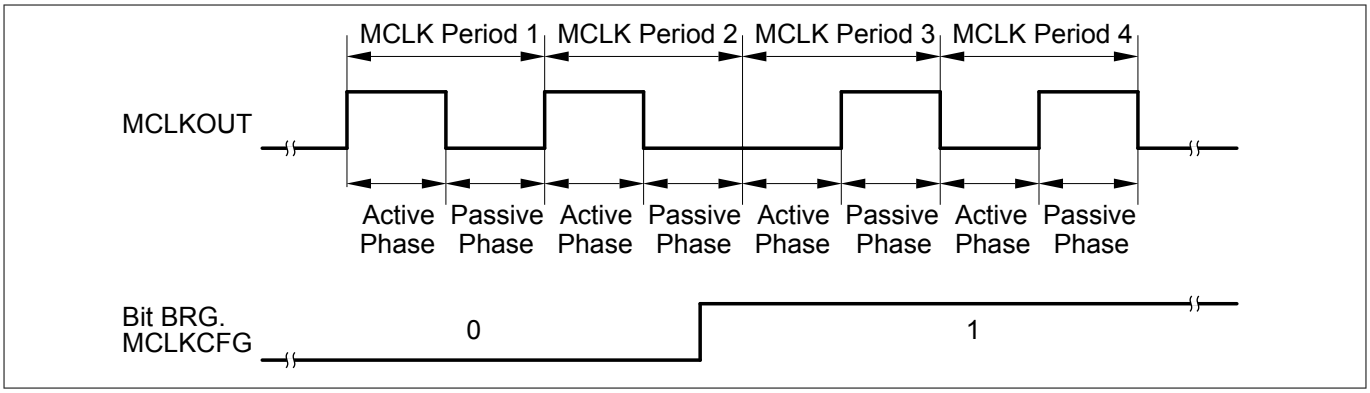


Figure 61 Master Clock Output Configuration

The shift clock output signal SCLKOUT available at the corresponding output pin can be configured in polarity and additionally, a delay of one period of f_{PDIV} (= half SCLK period) can be introduced. The delay allows to adapt the order of the shift clock edges to the application requirements. If the delay is used, it has to be taken into account for the calculation of the signal propagation times and loop delays.

The mechanism for the polarity control of the SCLKOUT signal is similar to the one for MCLKOUT, but based on bit field BRG.SCLKCFG. The generation of the SCLKOUT signal is enabled/disabled by the protocol pre-processor. Depending on the selected protocol, the protocol pre-processor can control the generation of the SCLKOUT signal independently of the divider chain, e.g. for protocols without the need of a shift clock available at a pin, the SCLKOUT generation is disabled.

18.2.5 Operating the Transmit Data Path

The transmit data path is based on 16-bit wide transmit shift registers (TSR and TSR[3:0]) and a transmit buffer TBUF. The data transfer parameters like data word length, data frame length, or the shift direction are controlled commonly for transmission and reception by the shift control register SCTR. The transmit control and status register TCSR controls the transmit data handling and monitors the transmit status.

A change of the value of the data shift output signal DOUTx only happens at the corresponding edge of the shift clock input signal. The level of the last data bit of a data word/frame is held constant at DOUTx until the next data word begins with the next corresponding edge of the shift clock.

18.2.5.1 Transmit Buffering

The transmit shift registers can not be directly accessed by software, because they are automatically updated with the value stored in the transmit buffer TBUF if a currently transmitted data word is finished and new data is valid for transmission. Data words can be loaded directly into TBUF by writing to one of the transmit buffer input locations TBUFx (see ***Transmit Control Information*** on page 346) or, optionally, by a FIFO buffer stage (see ***Operating the FIFO Data Buffer*** on page 351).

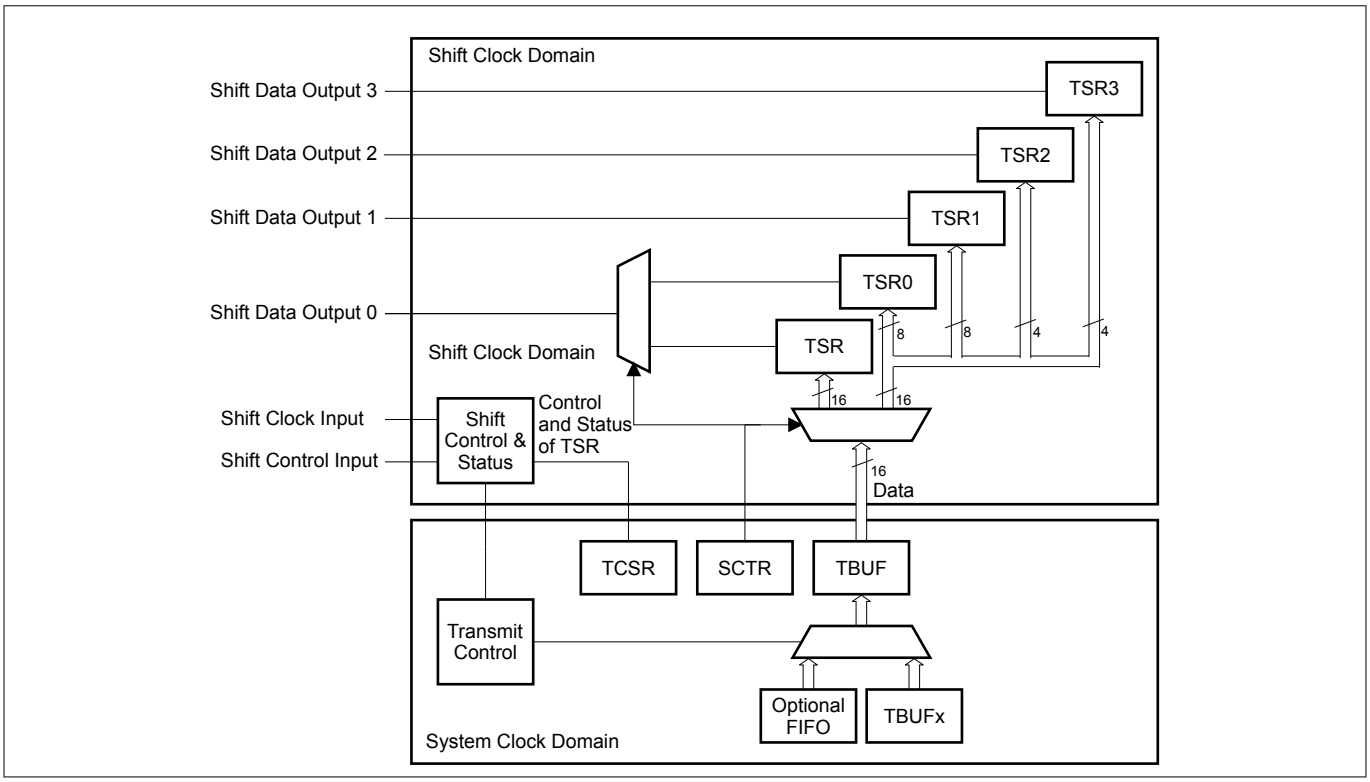


Figure 62 Transmit Data Path

18.2.5.2 Transmit Data Shift Mode

The transmit shift data can be selected to be shifted out one, two or four bits at a time through the corresponding number of output lines. This option allows the USIC to support protocols such as the Dual- and Quad-SSC. The selection is done through the bit field DSM in the shift control register SCTR.

Note: The bit field SCTR.DSM controls the data shift mode for both the transmit and receive paths to allow the transmission and reception of data through one to four data lines.

For the shift mode with two or four parallel data outputs, the data word and frame length must be in multiples of two or four respectively. The number of data shifts required to output a specific data word or data frame length is thus reduced by the factor of the number of parallel data output lines. For example, to transmit a 16-bit data word through four output lines, only four shifts are required.

Depending on the shift mode, different transmit shift registers with different bit composition are used as shown in ***Table 189***. Note that the 'n' in the table denotes the shift number less one, i.e. for the first data shift n = 0, the second data shift n = 1 and continues until the total number of shifts less one is reached.

For all transmit shift registers, whether the first bit shifted out is the MSB or LSB depends on the setting of SCTR.SDIR.

Table 189 Transmit Shift Register Composition

Transmit Shift Registers	Single Data Output (SCTR.DSM = 00_B)	Two Data Outputs (SCTR.DSM = 10_B)	Four Data Outputs (SCTR.DSM = 11_B)
TSR	All data bits	Not used	Not used
TSR0	Not used	Bit n*2	Bit n*4
TSR1	Not used	Bit n*2 + 1	Bit n*4 + 1
TSR2	Not used	Not used	Bit n*4 + 2
TSR3	Not used	Not used	Bit n*4 + 3

18.2.5.3 Transmit Control Information

The transmit control information TCI is a 5-bit value derived from the address x of the written TBUFx or INx input location. For example, writing to TBUF31 generates a TCI of 11111_B.

The TCI can be used as an additional control parameter for data transfers to dynamically change the data word length, the data frame length, or other protocol-specific functions (for more details about this topic, refer to the corresponding protocol chapters).

The way how the TCI is used in different applications can be programmed by the bits WLEMD, FLEMD, SELMD, WAMD and HPCMD in register TCSR.

Note: There can be only one TCI mode enabled at any one time, i.e. one mode bit is programmed to 1 and all the rest to 0. Concurrent TCI modes are not supported.

Table 190 TCI Modes

TCI Mode	Effects	Usage
Word length control (WLEMD = 1)	Bit field SCTR.WLE is updated with TCI[3:0] if a transmit buffer input location TBUFx is written	Can be used in all protocols to dynamically change the data word length between 1 and 16 data bits per data word
	Additionally, bit TCSR.EOF is updated with TCI[4]	Can be used in SSC master mode to control the slave select generation to finish data frames
Frame length control (FLEMD = 1)	Bit field SCTR.FLE[4:0] is updated with TCI[4:0] and SCTR.FLE[5] becomes 0 if a transmit buffer input location TBUFx is written	Can be used in all protocols to dynamically change the data frame length between 1 and 32 data bits per data frame
Select output control (SELMD = 1)	Bit field PCR.CTR[20:16] is updated with TCI[4:0] and PCR.CTR[23:21] becomes 0 if a transmit buffer input location TBUFx is written	Can be used in SSC master mode to define the targeted slave device(s)
Word address control (WAMD = 1)	Bit TCSR.WA is updated with TCI[4] if a transmit buffer input location TBUFx is written	Can be used in IIS mode to define if the data word is transmitted on the right or the left channel
Hardware Port control (HPCMD = 1)	Bit field SCTR.DSM is updated with TCI[1:0] if a transmit buffer input location TBUFx is written	Can be used in SSC protocols to dynamically change the number of data input and output lines to set up for standard, dual and quad SSC formats
	Additionally, bit TCSR.HPCDIR is updated with TCI[2]	Can be used in SSC protocols to control the pin(s) direction when the hardware port control function is enabled through CCR.HPCEN = 1

18.2.5.4 Transmit Data Validation

The data word in the transmit buffer TBUF can be tagged valid or invalid for transmission by bit TCSR.TDV (transmit data valid). A combination of data flow related and event related criteria define whether the data word is considered valid for transmission. A data validation logic checks the start conditions for each data word. Depending on the result of the check, the transmit shift register is loaded with different values, according to the following rules:

- If a USIC channel is the communication master (it defines the start of each data word transfer), a data word transfer can only be started with valid data in the transmit buffer TBUF. In this case, the transmit shift register is loaded with the content of TBUF, that is not changed due to this action.
- If a USIC channel is a communication slave (it can not define the start itself, but has to react), a data word transfer requested by the communication master has to be started independently of the status of the data word in TBUF. If a data word transfer is requested and started by the master, the transmit shift register is loaded at the first corresponding shift clock edge either with the data word in TBUF (if it is valid for transmission) or with the level defined by bit SCTR.PDL (if the content of TBUF has not been valid at the transmission start). In both cases, the content of TBUF is not changed.

The control and status bits for the data validation are located in register TCSR. The data validation is based on the logic blocks shown in ***Figure 63***.

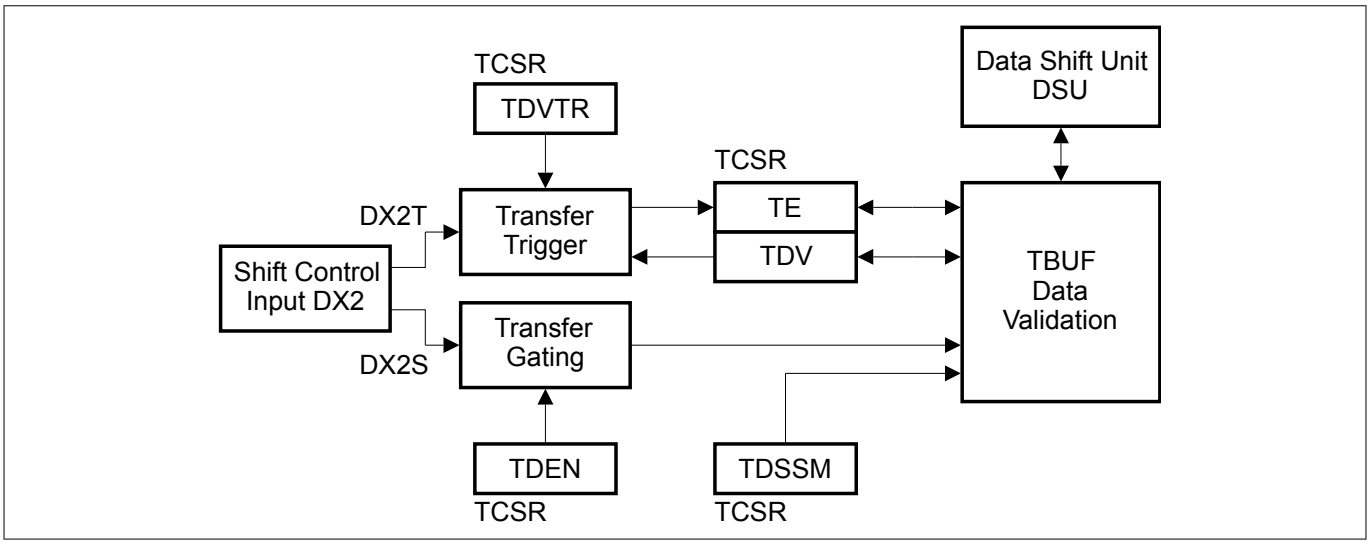


Figure 63 Transmit Data Validation

Transfer Gating

A transfer gating logic enables or disables the data word transfer from TBUF under software or under hardware control.

If the input stage DX2 is not needed for data shifting, signal DX2S can be used for gating purposes.

The transfer gating logic is controlled by bit field TCSR.TDEN.

Transfer Trigger

A transfer trigger logic supports data word transfers related to events, e.g. timer based or related to an input pin.

If the input stage DX2 is not needed for data shifting, signal DX2T can be used for trigger purposes. For example, this can be used for triggering the data transfer upon receiving the Clear to Send (CTS) signal at DX2 in the RS-232 protocol.

The transfer trigger logic is controlled by bit TCSR.TDVTR and the occurrence of a trigger event is indicated by bit TCSR.TE.

TBUF Data Validation

A data validation logic combines the inputs from the gating logic, the triggering logic and DSU signals. A transmission of the data word located in TBUF can only be started if the gating enables the start, bit TCSR.TDV = 1, and bit TCSR.TE = 1.

The content of the transmit buffer TBUF should not be overwritten with new data while it is valid for transmission and a new transmission can start. If the content of TBUF has to be changed, it is recommended to clear bit TCSR.TDV by writing FMR.MTDV = 10_B before updating the data.

Bit TCSR.TDV becomes automatically set when TBUF is updated with new data. Another possibility are the interrupts TBI (for ASC and IIC) or RSI (for SSC and IIS) indicating that a transmission has started. While a transmission is in progress, TBUF can be loaded with new data. In this case the user has to take care that an update of the TBUF content takes place before a new transmission starts.

With this structure, the following data transfer functionality can be achieved:

- If bit TCSR.TDSSM = 0, the content of the transmit buffer TBUF is always considered as valid for transmission. The transfer trigger mechanism can be used to start the transfer of the same data word based on the selected event (e.g. on a timer base or an edge at a pin) to realize a kind of life-sign mechanism. Furthermore, in slave mode, it is ensured that always a correct data word is transmitted instead of the passive data level.

- Bit TCSR.TDSSM = 1 has to be programmed to allow word-by-word data transmission with a kind of single-shot mechanism. After each transmission start, a new data word has to be loaded into the transmit buffer TBUF, either by software write actions to one of the transmit buffer input locations TBUFx or by an optional data buffer (e.g. FIFO buffer). To avoid that data words are sent out several times or to allow data handling with an additional data buffer (e.g. FIFO), bit TCSR.TDSSM has to be 1.
- Bit TCSR.TDV becoming automatically set when a new data word is loaded into the transmit buffer TBUF, a transmission start can be requested by a write action of the data to be transmitted to at least the low byte of one of the transmit buffer input locations TBUFx. The additional information TCI can be used to control the data word length or other parameters independently for each data word by a single write access.
- Bit field FMR.MTDV allows software driven modification (set or clear) of bit TCSR.TDV. Together with the gating control bit field TCSR.TDEN, the user can set up the transmit data word without starting the transmission. A possible program sequence could be:
  - Clear TCSR.TDEN = 00_B
  - Write data to TBUFx
  - Clear TCSR.TDV by writing FMR.MTDV = 10_B
  - Re-enable the gating with TCSR.TDEN = 01_B
  - And then set TCSR.TDV under software control by writing FMR.MTDV = 01_B.

18.2.6 Operating the Receive Data Path

The receive data path is based on two sets of 16-bit wide receive shift registers RSR0[3:0] and RSR1[3:0] and a receive buffer for each of the set (RBUF0 and RBUF1). The data transfer parameters like data word length, data frame length, or the shift direction are controlled commonly for transmission and reception by the shift control registers.

Register RBUF01SR monitors the status of RBUF0 and RBUF1.

18.2.6.1 Receive Buffering

The receive shift registers cannot be directly accessed by software, but their contents are automatically loaded into the receive buffer registers RBUF0 (or RBUF1 respectively) if a complete data word has been received or the frame is finished. The received data words in RBUF0 or RBUF1 can be read out in the correct order directly from register RBUF or, optionally, from a FIFO buffer stage (see ***Operating the FIFO Data Buffer*** on page 351).

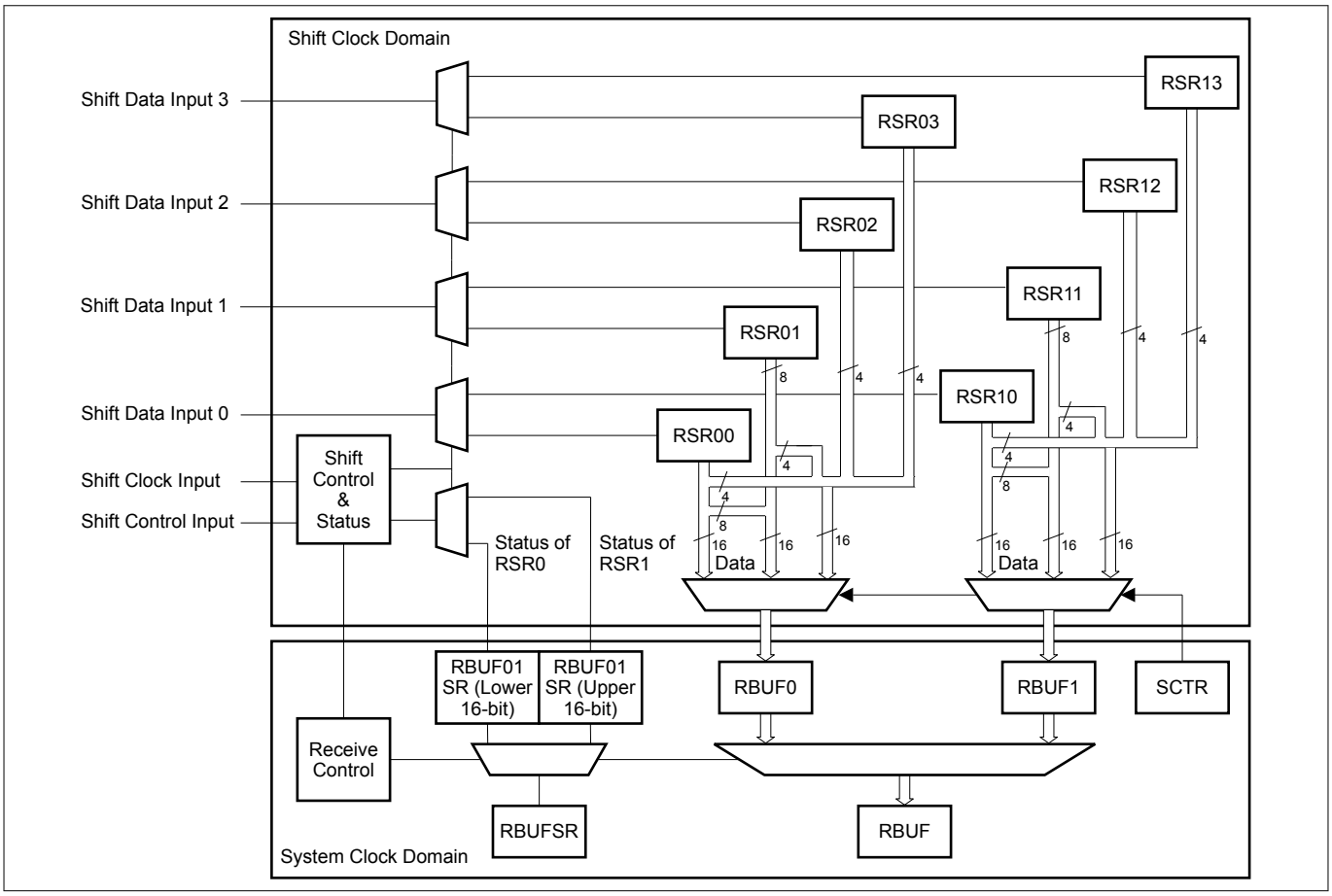


Figure 64 Receive Data Path

18.2.6.2 Receive Data Shift Mode

Receive data can be selected to be shifted in one, two or four bits at a time through the corresponding number of input stages and data input lines. This option allows the USIC to support protocols such as the Dual- and Quad-SSC. The selection is done through the bit field DSM in the shift control register SCTR.

Note: The bit field SCTR.DSM controls the data shift mode for both the transmit and receive paths to allow the transmission and reception of data through one to four data lines.

For the shift mode with two or four parallel data inputs, the data word and frame length must be in multiples of two or four respectively. The number of data shifts required to input a specific data word or data frame length is thus reduced by the factor of the number of parallel data input lines. For example, to receive a 16-bit data word through four input lines, only four shifts are required.

Depending on the shift mode, different receive shift registers with different bit composition are used as shown in ***Table 189***. Note that the 'n' in the table denotes the shift number less one, i.e. for the first data shift n = 0, the second data shift n = 1 and continues until the total number of shifts less one is reached.

For all receive shift registers, whether the first bit shifted in is the MSB or LSB depends on the setting of SCTR.SDIR.

Table 191 Receive Shift Register Composition

Receive Shift Registers	Input stage used	Single Data Input (SCTR.DSM = 00_B)	Two Data Inputs (SCTR.DSM = 10_B)	Four Data Inputs (SCTR.DSM = 11_B)
RSRx0	DX0	All data bits	Bit n*2	Bit n*4

Table 191 Receive Shift Register Composition (continued)

Receive Shift Registers	Input stage used	Single Data Input (SCTR.DSM = 00_B)	Two Data Inputs (SCTR.DSM = 10_B)	Four Data Inputs (SCTR.DSM = 11_B)
RSRx1	DX3	Not used	Bit n*2 + 1	Bit n*4 + 1
RSRx2	DX4	Not used	Not used	Bit n*4 + 2
RSRx3	DX5	Not used	Not used	Bit n*4 + 3

18.2.6.3 Baud Rate Constraints

The following baud rate constraints have to be respected to ensure correct data reception and buffering. The user has to take care about these restrictions when selecting the baud rate and the data word length with respect to the module clock frequency f_{PERIPH}.

- A received data word in a receiver shift registers RSRx[3:0] must be held constant for at least 4 periods of f_{PERIPH} in order to ensure correct loading of the related receiver buffer register RBUFx.
- The shift control signal has to be constant inactive for at least 5 periods of f_{PERIPH} between two consecutive frames in order to correctly detect the end of a frame.
- The shift control signal has to be constant active for at least 1 period of f_{PERIPH} in order to correctly detect a frame (shortest frame).
- A minimum setup and hold time of the shift control signal with respect to the shift clock signal has to be ensured.

18.2.7 Hardware Port Control

Hardware port control is intended for SSC protocols with half-duplex configurations, where a single port pin is used for both input and output data functions, to control the pin direction through a dedicated hardware interface.

All settings in Pn_IOCRy.PCx, except for the input pull device selection and output driver type (open drain or push-pull), are overruled by the hardware port control.

Input pull device selection is done through the Pn_IOCRy.PCx as before, while the output driver is fixed to push-pull-only in this mode.

One, two or four port pins can be selected with the hardware port control to support SSC protocols with multiple bi-directional data lines, such as dual- and quad-SSC. This selection and the enable/disable of the hardware port control is done through CCR.HPCEN. The direction of all selected pins is controlled through a single bit SCTR.HPCDIR.

SCTR.HPCDIR is automatically shadowed with the start of each data word to prevent changing of the pin direction in the middle of a data word transfer.

Note: If the number of port pins enabled through CCR.HPCEN is less than the number requested through SCTR.DSM, the unused pins output the passive data level defined by SCTR.PDL.

18.2.8 Operating the FIFO Data Buffer

The FIFO data buffers of a USIC module are built in a similar way, with transmit buffer and receive buffer capability for each channel.

Each USIC module has 64 buffer entries that can be distributed among the transmit or receive FIFO buffers of both channels of the module.

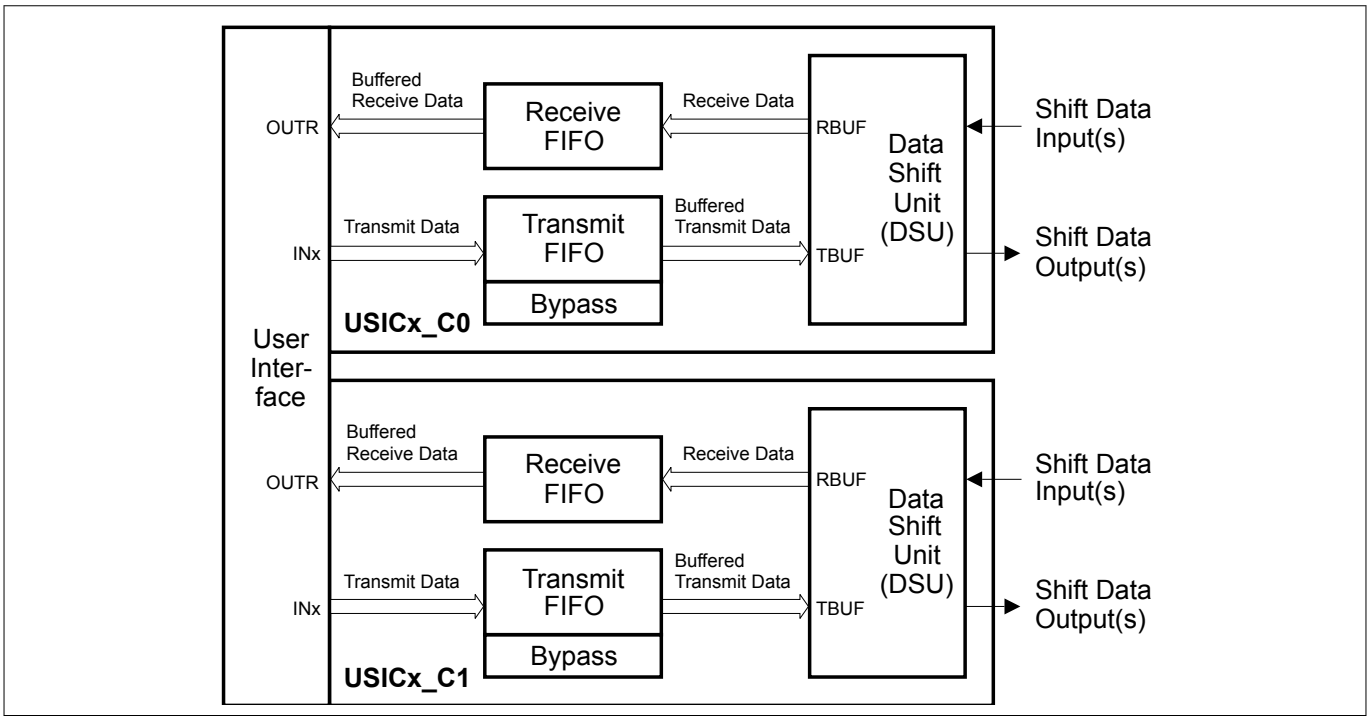


Figure 65 FIFO Buffer Overview

In order to operate the FIFO data buffers, the following issues have to be considered:

- FIFO buffer available and selected:

  It is recommended to configure all buffer parameters while there is no data traffic for this USIC channel and the FIFO mechanism is disabled by TBCTR.SIZE = 0 (for transmit buffer) or RBCTR.SIZE = 0 (for receive buffer). The allocation of a buffer area by writing TBCTR or RBCTR has to be done while the corresponding FIFO buffer is disabled. The FIFO buffer interrupt control bits can be modified independently of data traffic.
- FIFO buffer setup:

  The total amount of available FIFO buffer entries limits the length of the transmit and receive buffers for each USIC channel.
- Bypass setup:

  In addition to the transmit FIFO buffer, a bypass can be configured as described on ***FIFO Buffer Bypass*** on page 365.

18.2.8.1 FIFO Buffer Partitioning

The FIFO buffer area consists of a defined number of FIFO buffer entries, each containing a data part and the associated control information (RCI for receive data, TCI for transmit data).

One FIFO buffer entry represents the finest granularity that can be allocated to a receive FIFO buffer or a transmit FIFO buffer.

All available FIFO buffer entries of a USIC module are located one after the other in the FIFO buffer area. The overall counting starts with FIFO entry 0, followed by 1, 2, etc.

For each USIC module, 64 FIFO entries are available, that can be allocated to the channels of the same USIC module. It is not possible to assign FIFO buffer area to USIC channels that are not located within the same USIC module.

For each USIC channel, the size of the transmit and the receive FIFO buffer can be chosen independently. For example, it is possible to allocate the full amount of available FIFO entries as transmit buffer for one USIC channel. Some possible scenarios of FIFO buffer partitioning are shown in ***Figure 66***.

Each FIFO buffer consists of a set of consecutive FIFO entries. The size of a FIFO data buffer can only be programmed as a power of 2, starting with 2 entries, then 4 entries, then 8 entries, etc. A FIFO data buffer can only start at a FIFO entry aligned to its size.

For example, a FIFO buffer containing n entries can only start with FIFO entry 0, n, 2*n, 3*n, etc. and consists of the FIFO entries [x*n, (x+1)*n-1], with x being an integer number (incl. 0). It is not possible to have “holes” with unused FIFO entries within a FIFO buffer, whereas there can be unused FIFO entries between two FIFO buffers.

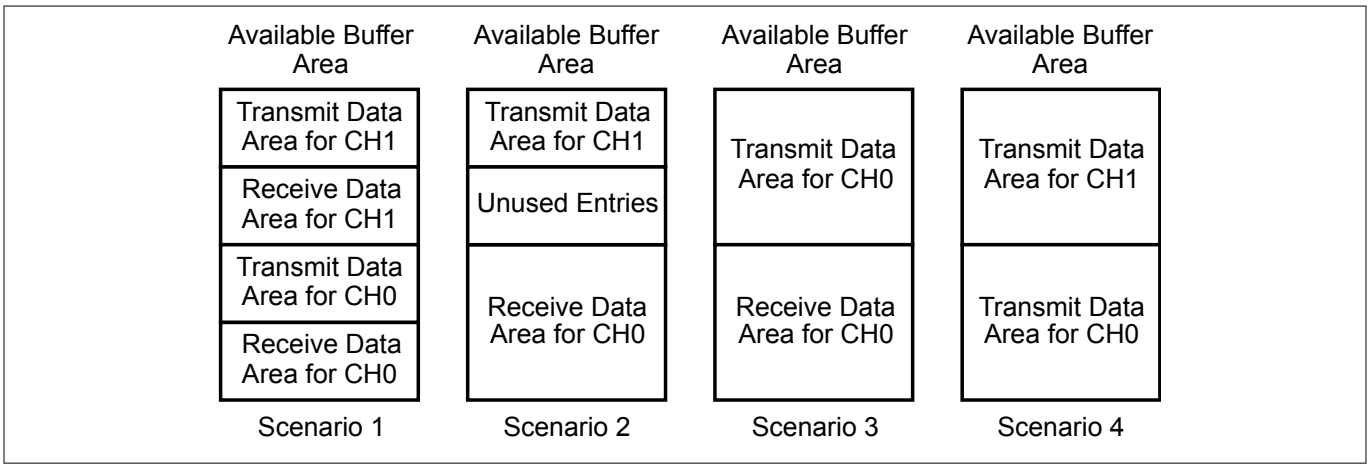


Figure 66 FIFO Buffer Partitioning

The data storage inside the FIFO buffers is based on pointers, that are internally updated whenever the data contents of the FIFO buffers have been modified. This happens automatically when new data is put into a FIFO buffer or the oldest data is taken from a FIFO buffer.

As a consequence, the user program does not need to modify the pointers for data handling. Only during the initialization phase, the start entry of a FIFO buffer has to be defined by writing the number of the first FIFO buffer entry in the FIFO buffer to the corresponding bit field DPTR in register RBCTR (for a receive FIFO buffer) or TBCTR (for a transmit FIFO buffer) while the related bit field RBCTR.SIZE=0 (or TBCTR.SIZE = 0, respectively).

The assignment of buffer entries to a FIFO buffer (regarding to size and pointers) must not be changed by software while the related USIC channel is taking part in data traffic.

18.2.8.2 Transmit FIFO Buffer Modes

The transmit FIFO buffer provides two operation modes with different triggering mechanisms for the standard transmit buffer events.

The modes are selectable through the bit field TBCTR.STBTEN.

STBTEN = 0 (Default)

When TBCTR.STBTEN = 0, a standard transmit buffer event is triggered only under the condition of the filling level of the transmit buffer (given by TRBSR.TBFLVL) transiting away from a programmed limit (TBCTR.LIMIT).

- When TBCTR.LOF = 0, the standard transmit buffer event is triggered by TBFLVL falling below LIMIT.
- When TBCTR.LOF = 1, the standard transmit buffer event is triggered by TBFLVL exceeding LIMIT.

The standard transmit buffer event is indicated by the flag STBI.

Note: The standard transmit buffer event indicated by TRBSR.STBI is triggered based on the transition of the fill level from equal to below or above the limit, not the fact of being below or above.

STBTEN = 1

When TBCTR.STBTEN = 1, a standard transmit buffer event can be triggered in two ways:

1. Similar to the case where STBTEN = 0, with the difference that the flag TRBSR.STBT is also set in addition to STBI.
2. While STBT = 1, a standard transmit buffer event will be additionally triggered each time there is either a transfer data to TBUF event (for the case where LOF = 0) or write data to INx event (for the case where LOF = 1).

Note: Standard transmit buffer events triggered by TRBSR.STBT does not affect the TRBSR.STBI flag.

The STBT flag is cleared depending on the setting of TBCTR.STBTM bit:

- When STBTM = 0, STBT is automatically cleared by hardware when the buffer fill level equals the programmed limit again (TRBSR.TBFLVL = TBCTR.LIMIT).
- When STBTM = 1, STBT is automatically cleared by hardware when the buffer fill level equals the buffer size (TRBSR.TBFLVL = TBCTR.SIZE).

Standard Transmit Buffer Event Examples

Figure 67 shows examples of the standard transmit buffer event generation with the different TBCTR.STBTEN and TBCTR.STBTM settings. These examples are meant to illustrate the hardware behaviour and might not always represent real application use cases.

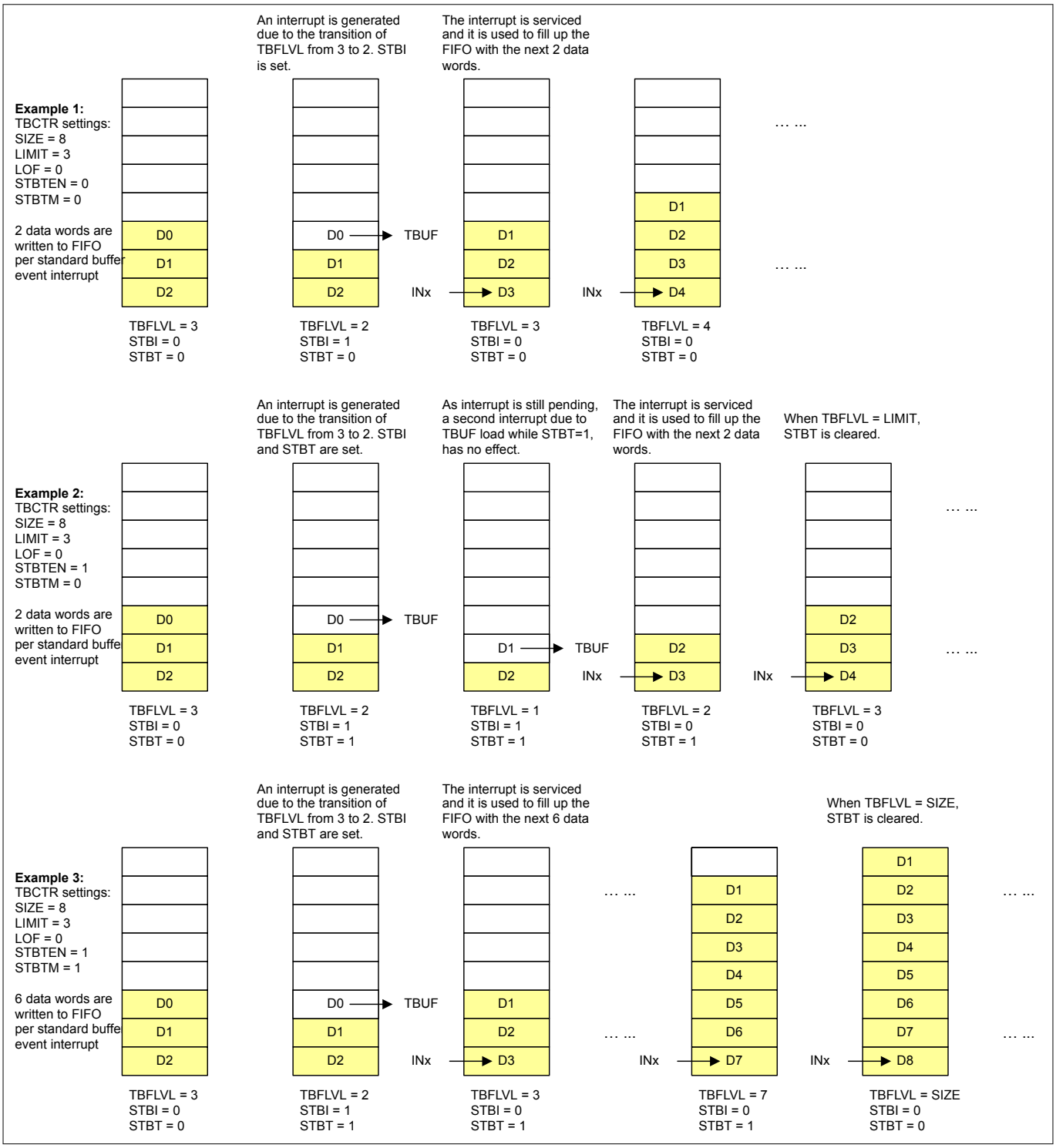


Figure 67 Standard Transmit Buffer Event Examples

18.2.8.3 Transmit Buffer Events and Interrupts

The transmit FIFO buffer mechanism detects the following events, that can lead to interrupts (if enabled):

- Standard transmit buffer event
- Transmit buffer error event

Standard Transmit Buffer Event

The standard transmit buffer event is triggered by either:

- The filling level of the transmit buffer (given by TRBSR.TBFLVL) exceeding (TBCTR.LOF = 1) or falling below (TBCTR.LOF = 0)[36] a programmed limit (TBCTR.LIMIT).
  - Applicable for all settings of TBCTR.STBTEN.
- A transfer data to TBUF event or write data to INx event, depending on TBCTR.LOF setting while TRBSR.STBT = 1.
  - Applicable only for TBCTR.STBTEN = 1.

Transmit Buffer Error Event

The transmit buffer error event is triggered when software has written to a full buffer. The written value is ignored.

Transmit Buffer Events and Interrupt Handling

Figure 68 shows the transmit buffer events and interrupts.

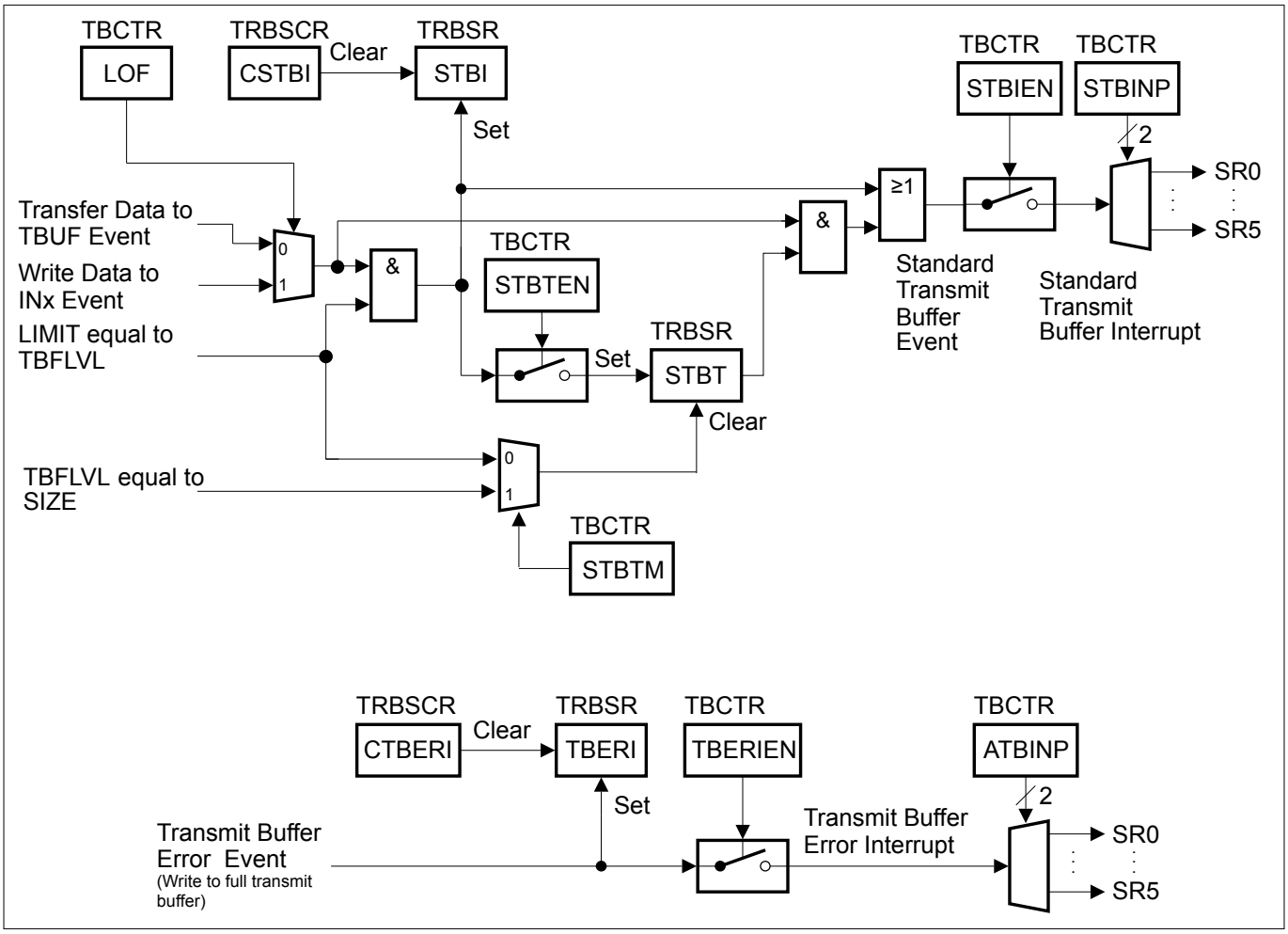


Figure 68 Transmit Buffer Events

Table 192 shows the registers, bits and bit fields to indicate the transmit buffer events and to control the interrupts related to the transmit FIFO buffers of a USIC channel.

36 If the standard transmit buffer event is used to indicate that new data has to be written to one of the INx locations, TBCTR.LOF = 0 should be programmed.

Table 192 Transmit Buffer Events and Interrupt Handling

Event	Indication Flag	Indication cleared by	Interrupt enabled by	SRx Output selected by
Standard transmit buffer event	TRBSR.STBI	TRBSCR.CSTBI	TBCTR.STBIEN	TBCTR.STBINP
	TRBSR.STBT	Cleared by hardware		
Transmit buffer error event	TRBSR.TBERI	TRBSCR.CTBERI	TBCTR.TBERIEN	TBCTR.ATBINP

18.2.8.4 Transmit FIFO Buffer Usage Example

To illustrate the usage of the transmit FIFO buffer, assume the following hypothetical application use case:

- A data set of 128 words is expected to be transmitted.
- 16 buffer entries are allocated as the channel's transmit data area.
- The target transmit buffer filling level is set at 9 to ensure that there is always transmit data in the buffer during the transmission of the complete data set.

TXFIFO Initialization

The following code initializes the transmit FIFO buffer in the given example:

```
/// ----------------------------------------------------------------
/// Configure TXFIFO
///    - TXFIFO starts from FIFO buffer entry 0
///    - TXFIFO size of 16 words
///    - Standard transmit buffer event is triggered when fill level
///         falls below 9, i.e. transition from 9 to 8
/// ----------------------------------------------------------------
    //              LOF     SIZE   STBTEN   STBTM  LIMIT   DPTR
 USIC0_CH1->TBCTR=(0<<28)|(4<<24)|(0<<15)|(0<<14)|(9<<8)|(0<<0);
```

TXFIFO Data Flow

Figure 69 shows a simplified data transmission flow for the given example.

Data transmission is started when the first data word is written to the transmit buffer input location INx. The application software continues to fill the buffer until all of the first 16 words are written to the buffer.

The buffer fill level is decremented with the transmission of each data word. When the fill level drops below the predefined limit of 9 to 8, a standard transmit buffer event is flagged through the bit TRBSR.STBI.

The standard transmit buffer event indicates to the application software that the next 8 data words should be written to the transmit buffer. A total of 14 iterations of the standard transmit buffer event is required to transmit all 128 words.

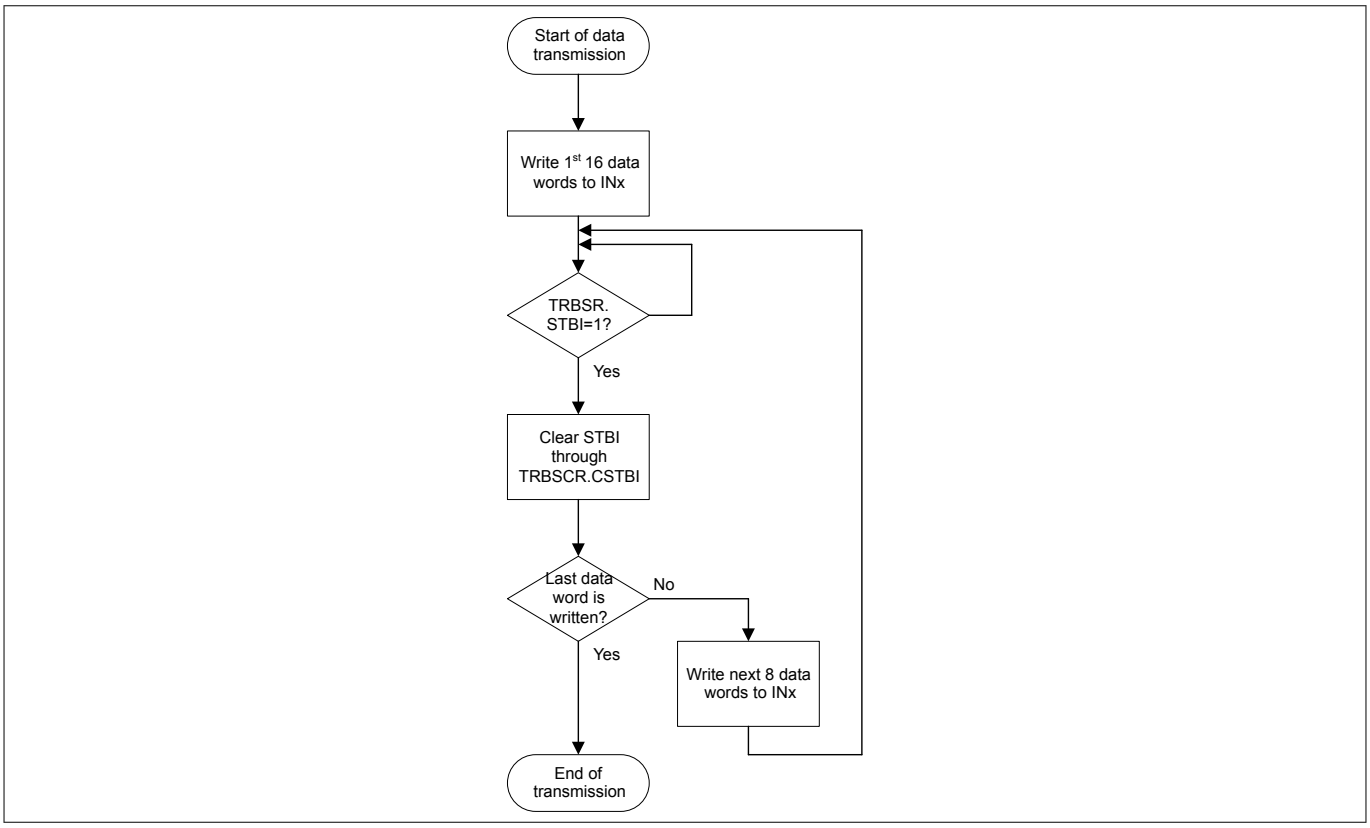


Figure 69 Simplified Data Transmission Flow With Transmit FIFO

18.2.8.5 Receive FIFO Buffer Modes

The receive FIFO buffer supports two main operation modes determined by the bit field RBCTR.RNM:

- Filling level mode (RNM = 0)
- Receive control information (RCI) mode (RNM = 1)

RCI Mode (RBCTR.RNM = 1)

In the RCI mode, each time a new data word becomes available in OUTR, an event is detected:

- If bit OUTR.RCI[4] = 0, a standard receive buffer event is signaled.
- If bit OUTR.RCI[4] = 1, an alternative receive buffer event is signaled.

The filling level of the receive buffer is not taken into account for the generation of the standard and alternate receive buffer events.

Depending on the selected protocol and the setting of RBCTR.RCIM, the value of RCI[4] can hold different information that can be used for protocol-specific interrupt handling (see protocol sections for more details).

Filling Level Mode (RBCTR.RNM = 0)

In the filling level mode, only the standard receive buffer event is used, whereas the alternative receive buffer event is not used.

This mode can be selected to indicate that a certain amount of data has been received, without regarding the content of the associated RCI.

The receive FIFO buffer further provides two operation sub-modes with different triggering mechanisms for the standard receive buffer events, selectable through the bit field RBCTR.SRBTEN.

Filling Level Sub-Mode with SRBTEN = 0

When RBCTR.SRBTEN = 0, a standard receive buffer event is triggered only under the condition of the filling level of the receive buffer (given by TRBSR.RBFLVL) transiting away from a programmed limit (RBCTR.LIMIT).

- When RBCTR.LOF = 0, the standard transmit buffer event is triggered by RBFLVL falling below LIMIT.
- When RBCTR.LOF = 1, the standard transmit buffer event is triggered by RBFLVL exceeding LIMIT.

The standard receive buffer event is indicated by the flag SRBI.

Note: The standard receive buffer event indicated by TRBSR.SRBI is triggered based on the transition of the fill level from equal to below or above the limit, not the fact of being below or above.

Filling Level Sub-Mode with SRBTEN = 1

When RBCTR.SRBTEN = 1, a standard receive buffer event can be triggered in two ways:

1. Similar to the case where SRBTEN = 0, with the difference that the flag TRBSR.SRBT is also set in addition to SRBI.
2. While SRBT = 1, a standard receive buffer event will be additionally triggered there is either a data read out event (for the case where LOF = 0) or new data received event (for the case where LOF = 1).

Note: Standard receive buffer events triggered by TRBSR.SRBT does not affect the TRBSR.SRBI flag.

The SRBT flag is cleared depending on the setting of RBCTR.SRBTM bit:

- When SRBTM = 0, SRBT is automatically cleared by hardware when the buffer fill level equals the programmed limit again (TRBSR.RBFLVL = RBCTR.LIMIT).
- When SRBTM = 1, SRBT is automatically cleared by hardware when the buffer fill level equals 0 (TRBSR.RBFLVL = 0).

Standard Receive Buffer Event Examples in Filling Level Mode

Figure 70 shows examples of the standard receive buffer event with the different RBCTR.SRBTEN and RBCTR.SRBTM settings. These examples are meant to illustrate the hardware behaviour and might not always represent real application use cases.

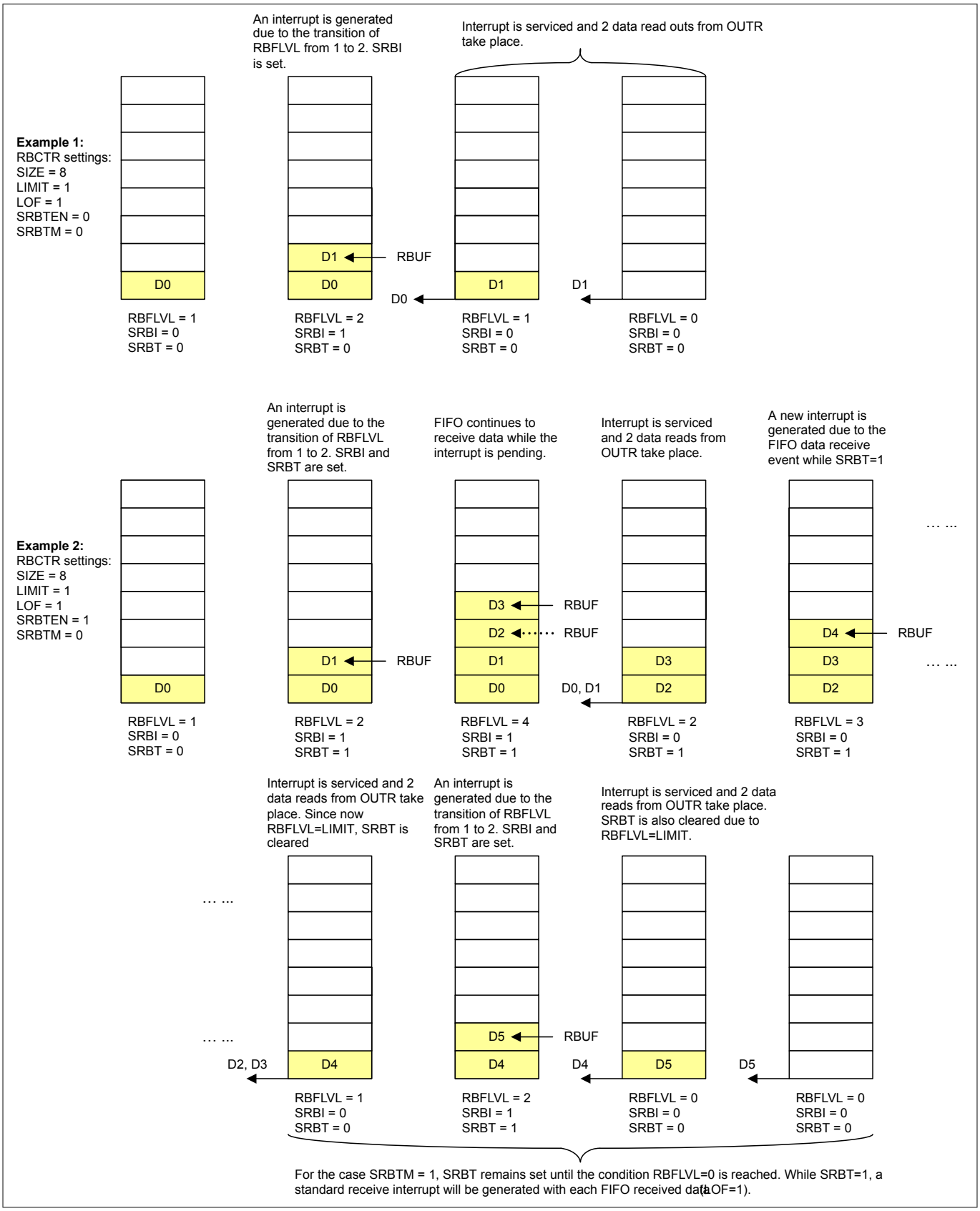


Figure 70 Standard Receive Buffer Event Examples

18.2.8.6 Receive Buffer Events and Interrupts

The receive FIFO buffer mechanism detects the following events, that can lead to an interrupt (if enabled):

- Standard receive buffer event
- Alternative receive buffer event
- Receive buffer error event

Standard Receive Buffer Event in Filling Level Mode

In filling level mode (RBCTR.RNM = 0), the standard transmit buffer event is triggered by either:

- The filling level of the receive buffer (given by TRBSR.RBFLVL) exceeding (RBCTR.LOF = 1) or falling below (RBCTR.LOF = 0) a programmed limit (RBCTR.LIMIT)[37].
  - Applicable for all settings of RBCTR.SRBTEN.
- A data read out event or new data received event, depending on RBCTR.LOF setting while TRBSR.SRBT = 1.
  - Applicable only for RBCTR.SRBTEN = 1.

Standard and Alternate Receive Buffer Events in RCI Mode

In RCI mode (RBCTR.RNM = 1), the standard receive buffer event is triggered when the OUTR stage is updated with a new data value with RCI[4] = 0.

If the OUTR stage is updated with a new data value with RCI[4] = 1, an alternate receive buffer event is triggered instead.

Receive Buffer Error Event

The receive buffer error event is triggered if the software reads from an empty buffer, regardless of RBCTR.RNM value. The read data is invalid.

Receive Buffer Events and Interrupt Handling

Figure 71 shows the receiver buffer events and interrupts in filling level mode.

37 If the standard receive buffer event is used to indicate that new data has to be read from OUTR, RBCTR.LOF = 1 should be programmed.

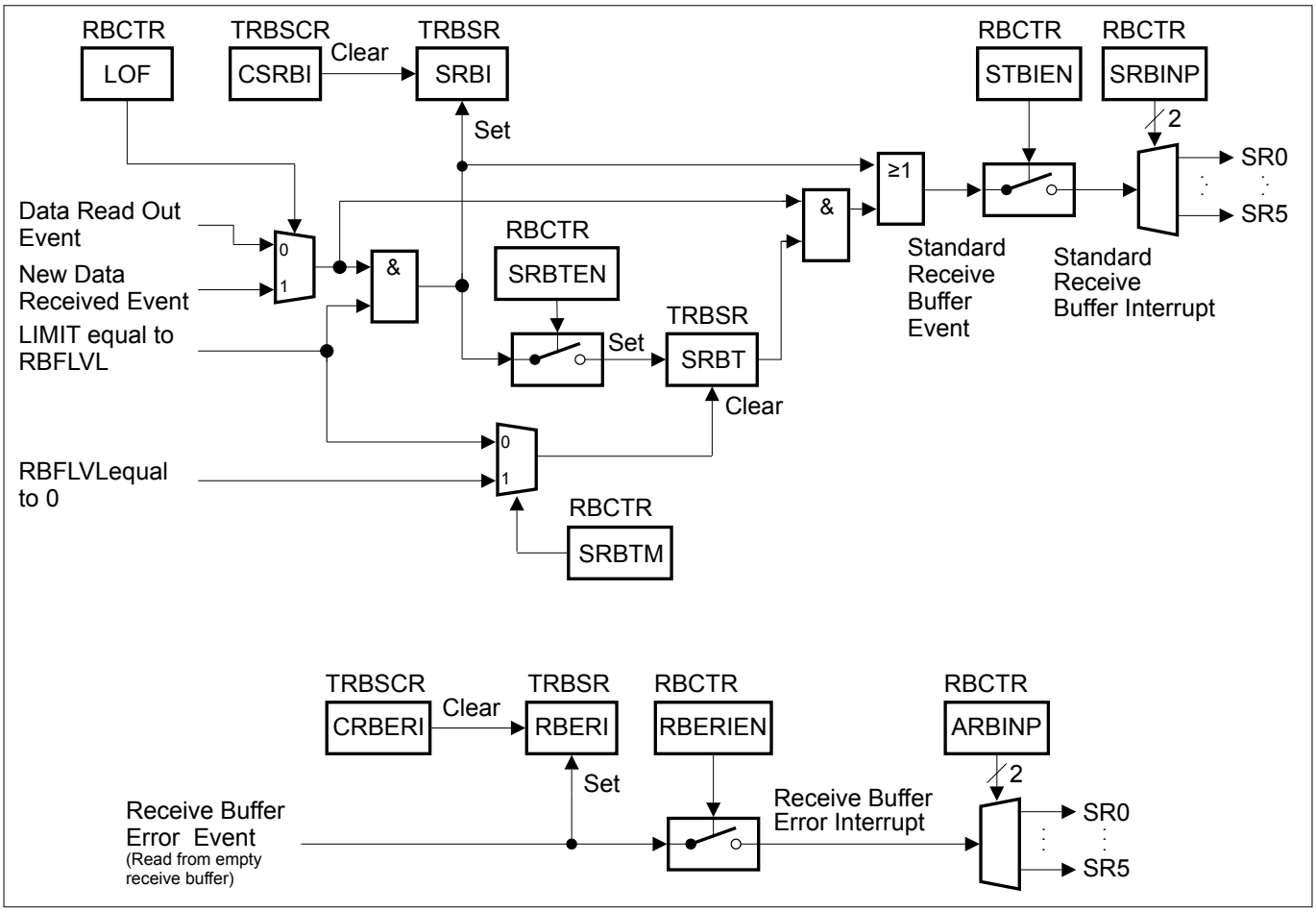


Figure 71 Receiver Buffer Events in Filling Level Mode

Figure 72 shows the receiver buffer events and interrupts in RCI mode.

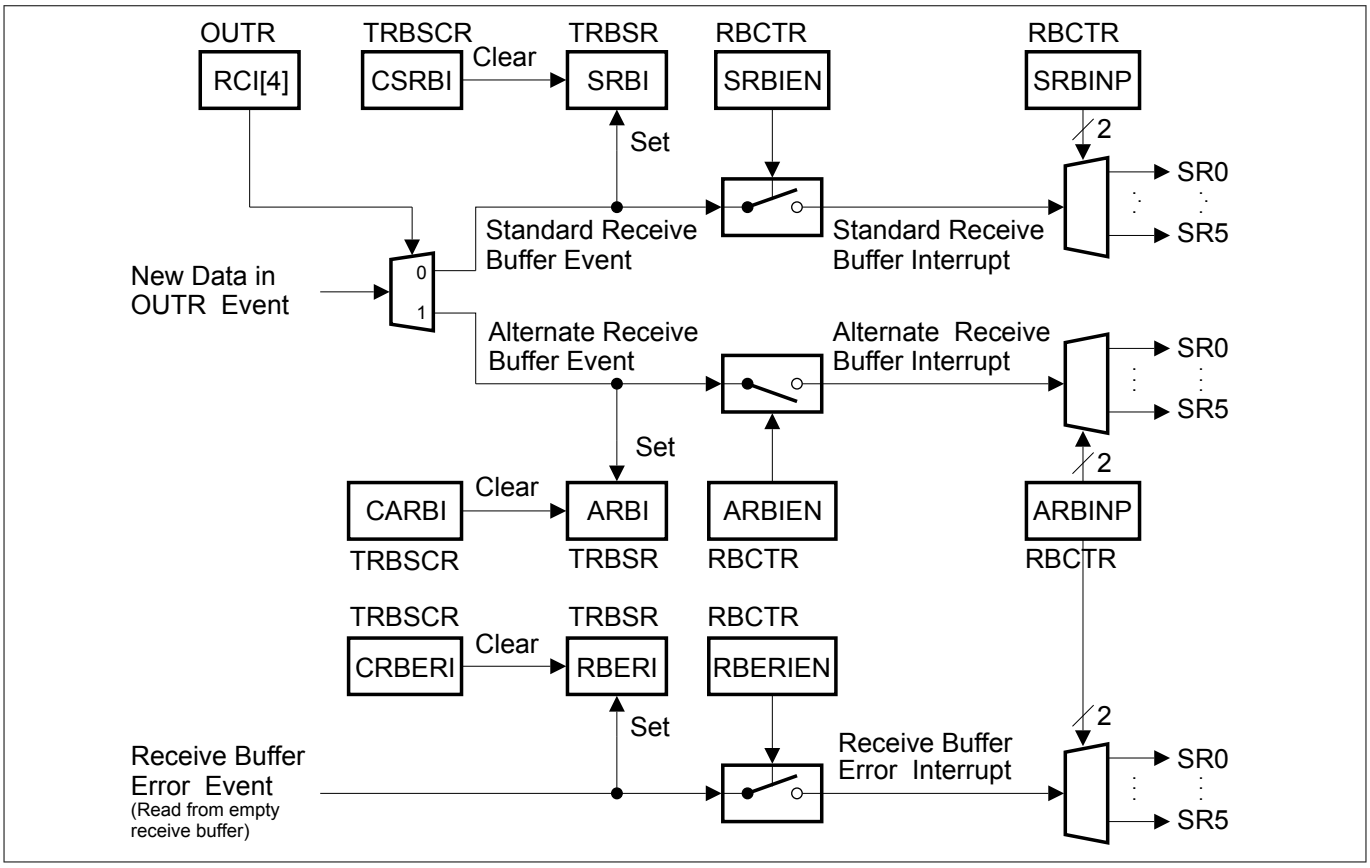


Figure 72 Receiver Buffer Events in RCI Mode

Table 193 shows the registers, bits and bit fields to indicate the receive buffer events and to control the interrupts related to the receive FIFO buffers of a USIC channel.

Table 193 Receive Buffer Events and Interrupt Handling

Event	Indication Flag	Indication cleared by	Interrupt enabled by	SRx Output selected by
Standard receive buffer event	TRBSR.SRBI	TRBSCR.CSRBI	RBCTR.SRBIEN	RBCTR.SRBINP
	TRBSR.SRBT	Cleared by hardware		
Alternative receive buffer event	TRBSR.ARBI	TRBSCR.CARBI	RBCTR.ARBIEN	RBCTR.ARBINP
Receive buffer error event	TRBSR.RBERI	TRBSCR.CRBERI	RBCTR.RBERIEN	RBCTR.ARBINP

18.2.8.7 Receive FIFO Buffer in Filling Level Mode Usage Example

To illustrate the usage of the receive FIFO buffer, assume the following hypothetical application use case:

- A data set of 128 words is expected to be received.
- 16 buffer entries are allocated as the channel's receive data area.
- The receive buffer filling level mode is selected and the standard receive buffer event is flagged each time the fill level reaches 8.

RXFIFO Initialization

The following code initializes the receive FIFO buffer in the given example:

```
/// ----------------------------------------------------------------------
/// Configure RXFIFO
///     - RXFIFO starts from FIFO buffer entry 32
///     - RXFIFO size of 16 data words
///     - Standard receive buffer event is triggered when fill level
///         exceeds 7, i.e. transition from 7 to 8
/// ----------------------------------------------------------------------
 USIC0_CH1->RBCTR=(1<<28)|(0<<27)|(4<<24)|(0<<15)|(0<<14)|(7<<8)|(32<<0);
//                  LOF    RNM     SIZE    SRBTEN  SRBTM   LIMIT  DPTR
```

RXFIFO Data Flow

Figure 73 shows a simplified data reception flow for the given example.

The buffer fill level is incremented with the reception of each data word. When the fill level exceeds the predefined limit of 7 and transits to 8, a standard receive buffer event is flagged through the bit TRBSR.SRBI.

The application software reads out the 8 data words in the buffer, through the receive buffer output register OUTR, with each standard receive buffer event. A total of 16 iterations of the standard receive buffer event is required to receive all 128 words.

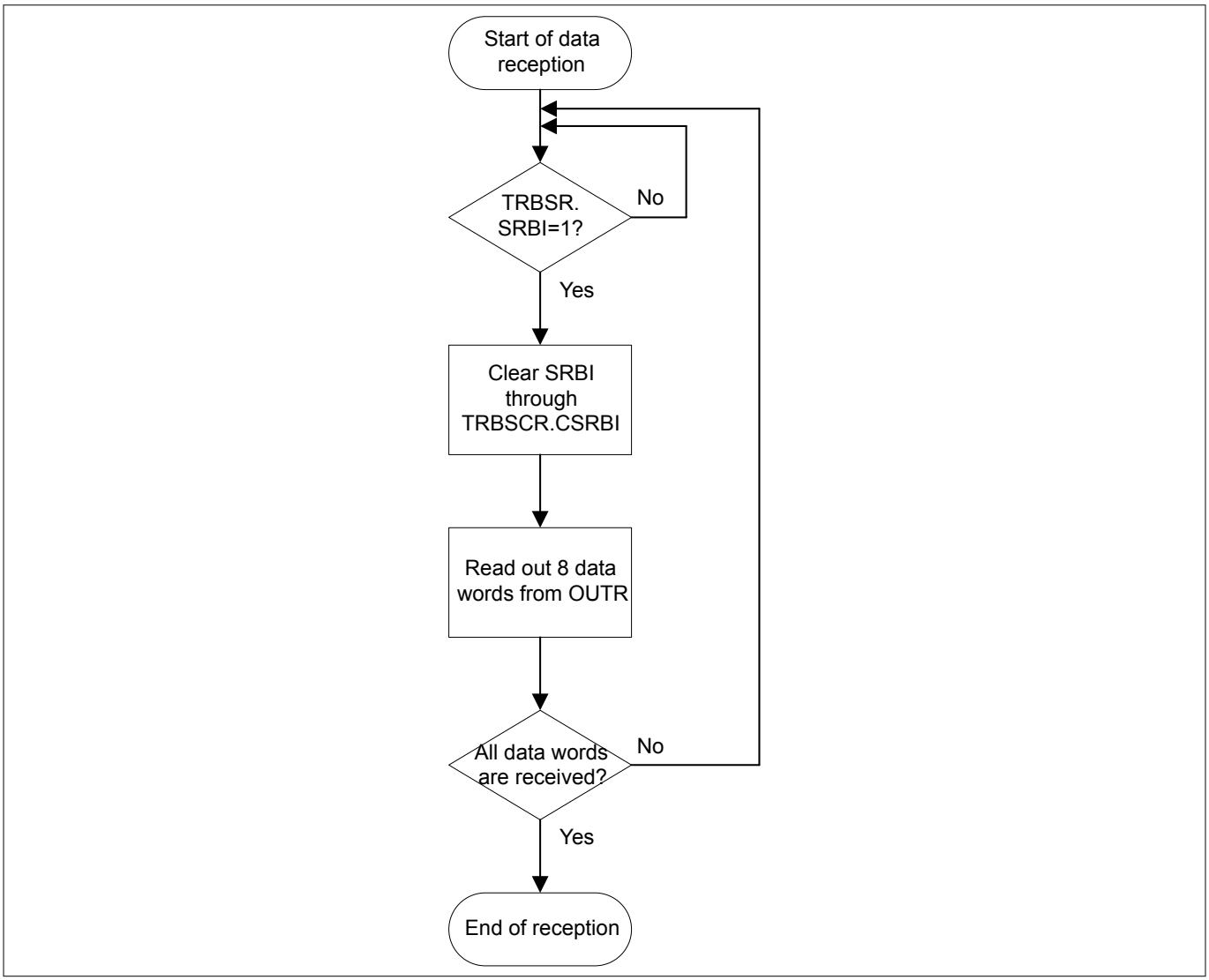


Figure 73 Simplified Data Reception Flow in Receive Buffer Filling Level Mode

18.2.8.8 FIFO Buffer Bypass

The data bypass mechanism is part of the transmit FIFO control block. It allows to introduce a data word in the data stream without modifying the transmit FIFO buffer contents, e.g. to send a high-priority message.

The bypass structure consists of a bypass data word of maximum 16 bits in register BYP and some associated control information in register BYPCR. For example, these bits define the word length of the bypass data word and configure a transfer trigger and gating mechanism similar to the one for the transmit buffer TBUF.

The bypass data word can be tagged valid or invalid for transmission by bit BYRCR.BDV (bypass data valid). A combination of data flow related and event related criteria define whether the bypass data word is considered valid for transmission. A data validation logic checks the start conditions for this data word. Depending on the result of the check, the transmit buffer register TBUF is loaded with different values, according to the following rules:

- Data from the transmit FIFO buffer or the bypass data can only be transferred to TBUF if TCSR.TDV = 0 (TBUF is empty).
- Bypass data can only be transferred to TBUF if the bypass is enabled by BYPCR.BDEN or the selecting gating condition is met.

- If the bypass data is valid for transmission and has either a higher transmit priority than the FIFO data or if the transmit FIFO is empty, the bypass data is transferred to TBUF.
- If the bypass data is valid for transmission and has a lower transmit priority than the FIFO buffer that contains valid data, the oldest transmit FIFO data is transferred to TBUF.
- If the bypass data is not valid for transmission and the FIFO buffer contains valid data, the oldest FIFO data is transferred to TBUF.
- If neither the bypass data is valid for transmission nor the transmit FIFO buffer contains valid data, TBUF is unchanged.

The bypass data validation is based on the logic blocks shown in ***Figure 74***.

- A transfer gating logic enables or disables the bypass data word transfer to TBUF under software or under hardware control. If the input stage DX2 is not needed for data shifting, signal DX2S can be used for gating purposes. The transfer gating logic is controlled by bit field BYPCR.BDEN.
- A transfer trigger logic supports data word transfers related to events, e.g. timer based or related to an input pin. If the input stage DX2 is not needed for data shifting, signal DX2T can be used for trigger purposes. The transfer trigger logic is controlled by bit BYPCR.BDVTR.
- A bypass data validation logic combining the inputs from the gating logic, the triggering logic and TCSR.TDV.

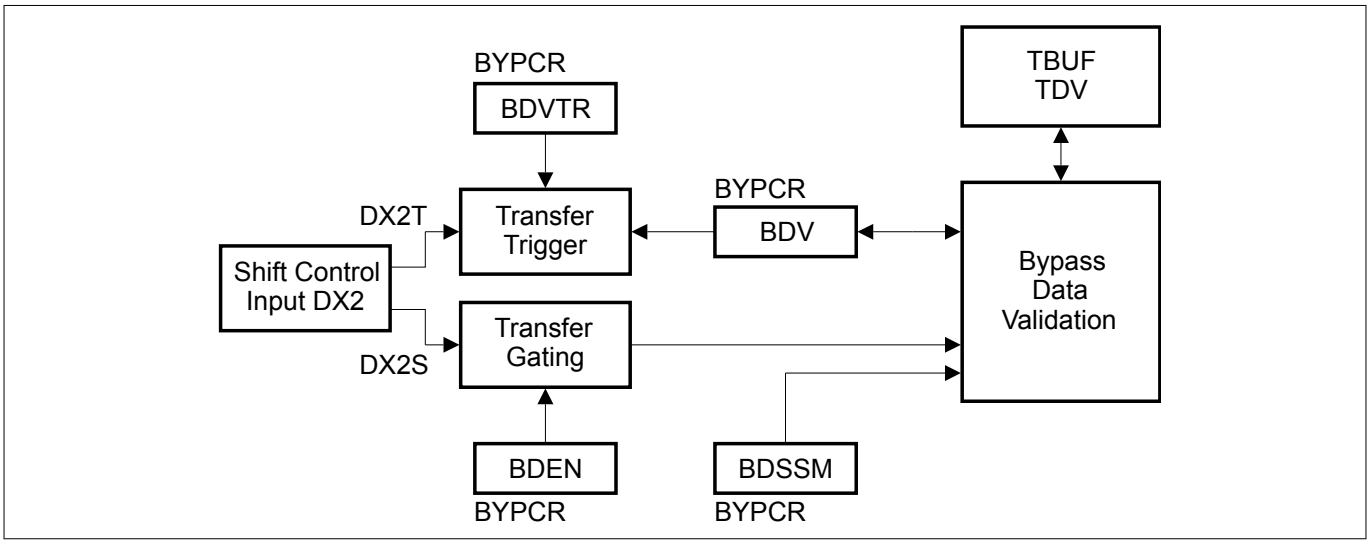


Figure 74 Bypass Data Validation

With this structure, the following bypass data transfer functionality can be achieved:

- Bit BYPCR.BDSSM = 1 has to be programmed for a single-shot mechanism. After each transfer of the bypass data word to TBUF, the bypass data word has to be tagged valid again. This can be achieved either by writing a new bypass data word to BYP or by DX2T if BDVTR = 1 (e.g. trigger on a timer base or an edge at a pin).
- Bit BYPCR.BDSSM = 0 has to be programmed if the bypass data is permanently valid for transmission (e.g. as alternative data if the data FIFO runs empty).

18.2.8.9 FIFO Access Constraints

The data in the shared FIFO buffer area is accessed by the hardware mechanisms for data transfer of each communication channel (for transmission and reception) and by software to read out received data or to write data to be transmitted. As a consequence, the data delivery rate can be limited by the FIFO mechanism. Each access by hardware to the FIFO buffer area has priority over a software access, that is delayed in case of an access collision.

In order to avoid data loss and stalling of the CPU due to delayed software accesses, the baud rate, the word length and the software access mechanism have to be taken into account. Each access to the FIFO data buffer area by software or by hardware takes one period of f_{PERIPH}. Especially a continuous flow of very short, consecutive data words can lead to an access limitation.

18.2.8.10 Handling of FIFO Transmit Control Information

In addition to the transmit data, the transmit control information TCI can be transferred from the transmit FIFO or bypass structure to the USIC channel. Depending on the selected protocol and the enabled update mechanism, some settings of the USIC channel parameters can be modified.

The modifications are based on the TCI of the FIFO data word loaded to TBUF or by the bypass control information if the bypass data is loaded into TBUF, as shown in ***Table 194*** and ***Figure 75***.

See ***Chapter 18.2.5.3*** for more details on TCI.

Table 194 TCI Handling with FIFO / Bypass

TCSR Setting	Modifications of USIC Channel Parameters
SELMD = 1	• Update of PCR.CTR[20:16] by FIFO TCI or BYPCR.BSELO • Additional clear of PCR.CTR[23:21]
WLEMD = 1	• Update of SCTR.WLE and TCSR.EOF by FIFO TCI or BYPCR.BWLE (if the WLE information is overwritten by TCI or BWLE, the user has to take care that FLE is set accordingly)
FLEMD = 1	• Update of SCTR.FLE[4:0] by FIFO TCI or BYPCR.BWLE • Additional clear of SCTR.FLE[5]
HPCMD = 1	• Update of SCTR.DSM and SCTR.HPCDIR by FIFO TCI or BYPCR.BHPC
WAMD = 1	• Update of TCSR.WA by FIFO TCI[4]

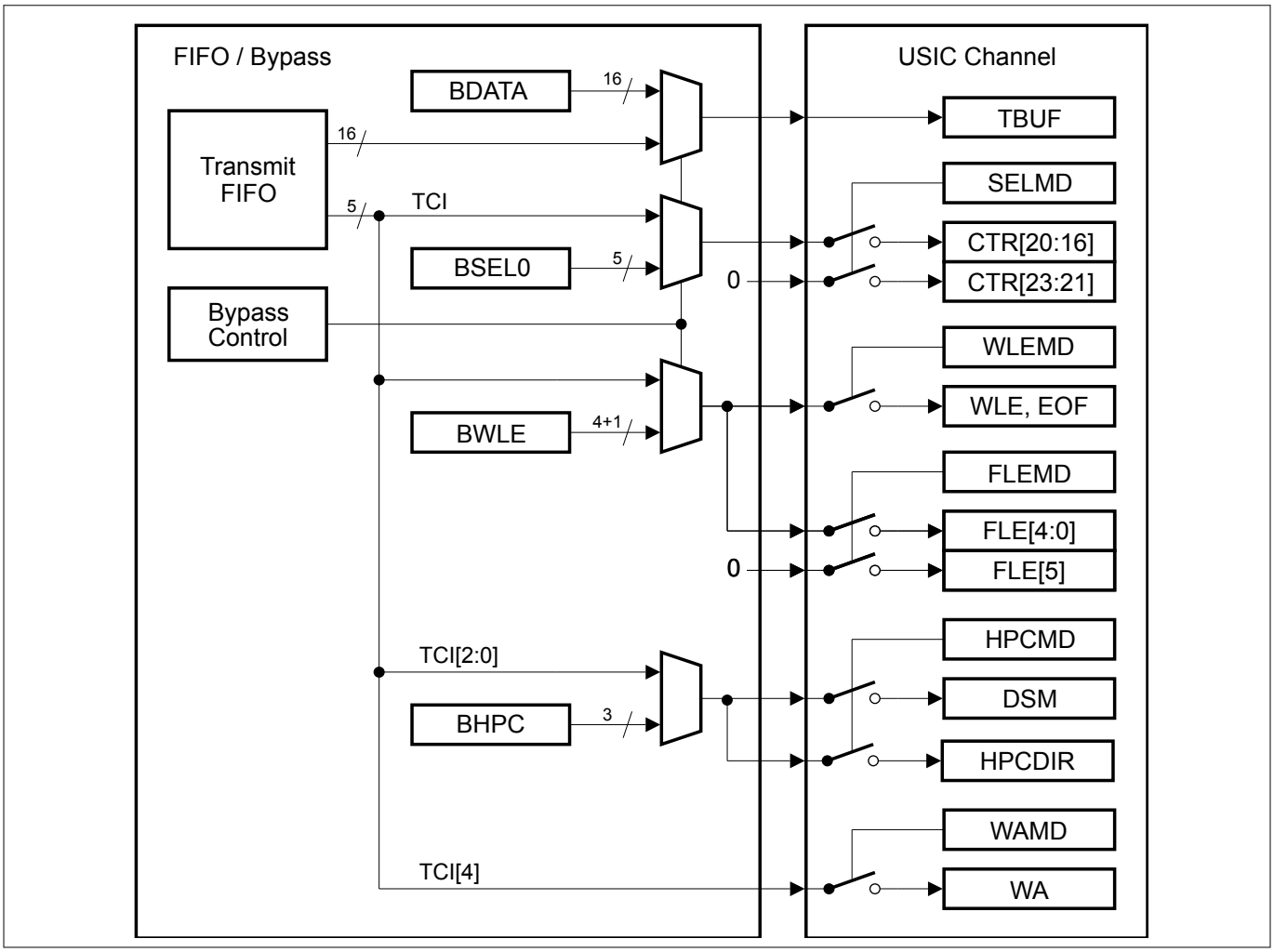


Figure 75 TCI Handling with FIFO / Bypass

18.3 Asynchronous Serial Channel (ASC = UART)

The asynchronous serial channel ASC covers the reception and the transmission of asynchronous data frames and provides hardware LIN support.

The receiver and transmitter being independent, frames can start at different points in time for transmission and reception.

The ASC mode is selected by CCR.MODE = 0010_B.

18.3.1 Signal Description

An ASC connection is characterized by the use of a single connection line between a transmitter and a receiver. The receiver input RXD signal is handled by the input stage DX0.

18.3.1.1 ASC Full-Duplex Communication

For full-duplex communication, an independent communication line is needed for each transfer direction.

Figure 76 shows an example with a point-to-point full-duplex connection between two communication partners ASC A and ASC B.

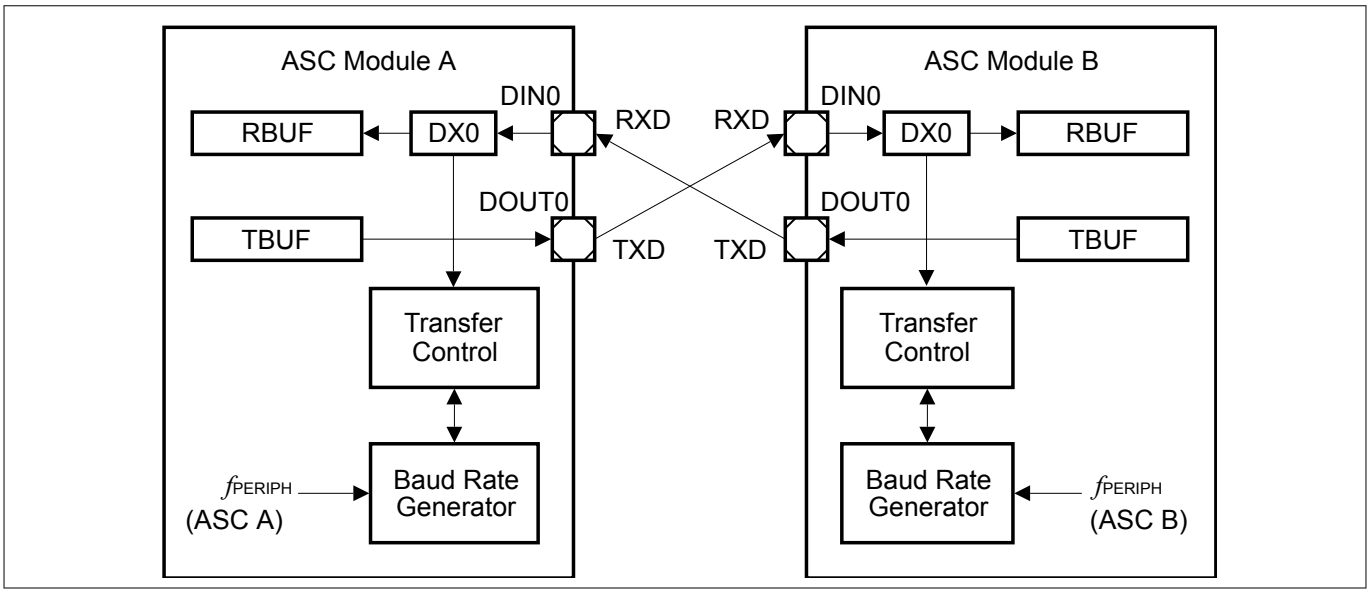


Figure 76 ASC Signal Connections for Full-Duplex Communication

18.3.1.2 ASC Half-Duplex Communication

For half-duplex or multi-transmitter communication, a single communication line is shared between the communication partners.

The user has to take care that only one transmitter is active at a time.

In order to support transmitter collision detection, the input stage DX1 can be used to monitor the level of the transmit line and to check if the line is in the idle state or if a collision occurred.

Figure 77 shows an example with a point-to-point half-duplex connection between ASC A and ASC B.

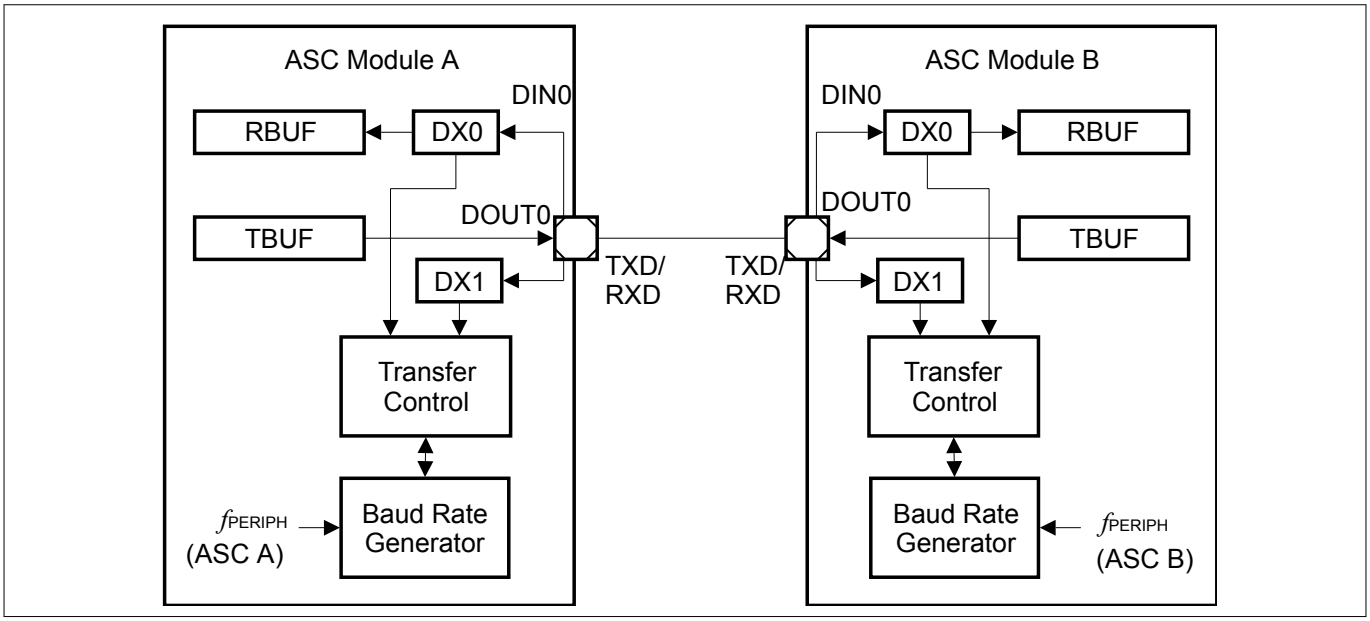


Figure 77 ASC Signal Connections for Half-Duplex Communication

18.3.2 Frame Format

A standard ASC frame is shown in ***Figure 78***. It consists of:

- An idle time with the signal level 1.
- One start of frame bit (SOF) with the signal level 0.
- A data field containing a programmable number of data bits (1-63).
- A parity bit (P), programmable for either even or odd parity. It is optionally possible to handle frames without parity bit.
- One or two stop bits with the signal level 1.

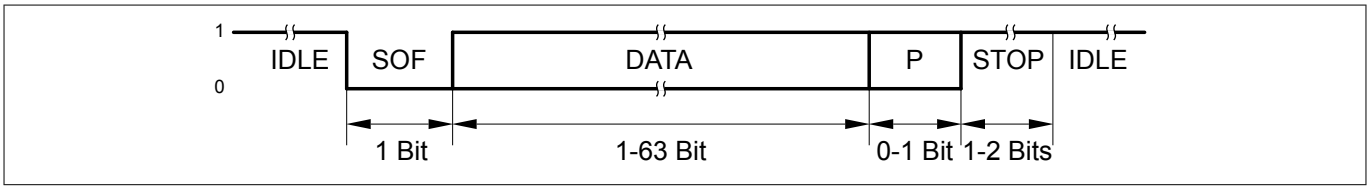


Figure 78 Standard ASC Frame Format

The protocol specific bits (SOF, P, STOP) are automatically handled by the ASC protocol state machine and do not appear in the data flow via the receive and transmit buffers.

18.3.2.1 Idle Detection

The receiver and the transmitter independently check the respective data input lines (DX0, DX1) for being idle. The idle detection ensures that an SOF bit of a recently enabled ASC module does not collide with an already running frame of another ASC module.

In order to start the idle detection, the user software has to clear bits PSR.RXIDLE and/or PSR.TXIDLE, e.g. before selecting the ASC mode or during operation. If a bit is cleared by software while a data transfer is in progress, the currently running frame transfer is finished normally before starting the idle detection again. Frame reception is only possible if PSR.RXIDLE = 1 and frame transmission is only possible if PSR.TXIDLE = 1. The duration of the idle detection depends on the setting of bit PCR.IDM. In the case that a collision is not possible, the duration can be shortened and the bus can be declared as being idle by setting PCR.IDM = 0.

In the case that the complete idle detection is enabled by PCR.IDM = 1, the data input of DX0 is considered as idle (PSR.RXIDLE becomes set) if a certain number of consecutive passive bit times has been detected. The same scheme applies for the transmitter's data input of DX1. Here, bit PSR.TXIDLE becomes set if the idle condition of this input signal has been detected.

The duration of the complete idle detection is given by the number of programmed data bits per frame plus 2 (in the case without parity) or plus 3 (in the case with parity). The counting of consecutive bit times with 1 level restarts from the beginning each time an edge is found, after leaving a stop mode or if ASC mode becomes enabled.

If the idle detection bits PSR.RXIDLE and/or TXIDLE are cleared by software, the counting scheme is not stopped (no re-start from the beginning). As a result, the cleared bit(s) can become set immediately again if the respective input line still meets the idle criterion.

Please note that the idle time check is based on bit times, so the maximum time can be up to 1 bit time more than programmed value (but not less).

18.3.2.2 Start Bit Detection

The receiver input signal DIN0 (selected signal of input stage DX0) is checked for a falling edge. An SOF bit is detected when a falling edge occurs while the receiver is idle or after the sampling point of the last stop bit.

To increase noise immunity, the SOF bit timing starts with the first falling edge that is detected. If the sampled bit value of the SOF is 1, the previous falling edge is considered to be due to noise and the receiver is considered to be idle again.

18.3.2.3 Data Field

The length of the data field (number of data bits) can be programmed by bit field SCTR.FLE. It can vary between 1 and 63 data bits, corresponding to values of SCTR.FLE = 0 to 62 (the value of 63 is reserved and must not be programmed in ASC mode).

The data field can consist of several data words, e.g. a transfer of 12 data bits can be composed of two 8-bit words, with the 12 bits being split into 8-bits of the first word and 4 bits of the second word. The user software has to take care that the transmit data is available in-time, once a frame has been started. If the transmit buffer runs empty during a running data frame, the passive data level (SCTR.PDL) is sent out.

The shift direction can be programmed by SCTR.SDIR. The standard setting for ASC frames with LSB first is achieved with the default setting SDIR = 0.

18.3.2.4 Parity Bit

The ASC allows parity generation for transmission and parity check for reception on frame base. The type of parity can be selected by bit field CCR.PM, common for transmission and reception (no parity, even or odd parity).

If the parity handling is disabled, the ASC frame does not contain any parity bit. For consistency reasons, all communication partners have to be programmed to the same parity mode.

After the last data bit of the data field, the transmitter automatically sends out its calculated parity bit if parity generation has been enabled. The receiver interprets this bit as received parity and compares it to its internally calculated one. The received parity bit value and the result of the parity check are monitored in the receiver buffer status registers, RBUFSR and RBUF01SR, as receiver buffer status information. These registers contain bits to monitor a protocol-related argument (PAR) and protocol-related error indication (PERR).

18.3.2.5 Stop Bit(s)

Each ASC frame is completed by 1 or 2 of stop bits with the signal level 1 (same level as the idle level). The number of stop bits is programmable by bit PSR.STPB.

A new start bit can be transferred directly after the last stop bit.

18.3.3 Operating the ASC

In order to operate the ASC protocol, the USIC channel has to be first initialized.

It is recommended to configure all parameters of the ASC that do not change during run time while CCR.MODE = 0000_B, except stated otherwise.

The main initialization steps are outlined below:

- Enable USIC channel
  - Enable the module by writing 1s to MODEN and BPMODEN bits in KSCFG register.
- Configure baud rate generator
  - Select either fractional divider mode or normal divider mode with FDR.DM bit.
  - Configure the bit timing and baud rate setting through register BRG and FDR.STEP bit field.
- Configure input pins
  - Establish a connection of input stage DX0 with the receive data input pin (signal DIN0) selected by DX0CR.DSEL bit field and with bit DX0CR.INSW = 0.
  - Due to the handling of the input data stream by the synchronous protocol handler, the propagation delay of the synchronization in the input stage has to be considered.
  - For collision or idle detection of the transmitter, the input stage DX1 has to be connected to the selected transmit output pin, also with DX1CR.INSW = 0. Additionally, program DX2CR.INSW = 0.

- Configure data format
  - The word length, the frame length, and the shift direction have to be set up according to the application requirements by programming the register SCTR.
  - Write SCTR.TRM = 01_B to enable ASC data transfers.
  - If required by the application, the data input and output signals can be inverted with DX0CR.DPOL and SCTR.DOCFG respectively.
- Configure data transfer parameters
  - Write TCSR.TDSSM = 1 and TCSR.TDEN = 01_B to enable data transmission in single shot mode.
- Configure protocol control parameters
  - Select the idle detection mode, number of stop bits, sample mode and sample point through the register PCR.
- Select ASC protocol
  - Enable ASC mode with CCR.MODE = 0010_B.
  - Additionally, the parity mode can be configured with CCR.PM.
- Configure output pins
  - Configure the transmit data output pin (signal DOUT0) through the selected pin's port control register Pn_IOCR0/4/8/12. Refer to the port chapter.
  - The step to enable the output pin functions should only be done after the ASC mode is enabled with CCR.MODE, to avoided unintended spikes on the output.

Please note that not all feature combinations can be supported by the application at the same time, e.g. due to propagation delays.

For example, the length of a frame is limited by the frequency difference of the transmitter and the receiver device.

Furthermore, in order to use the average of samples (SMD = 1), the sampling point has to be chosen to respect the signal settling and data propagation times.

An initialization code example is given in ***Chapter 18.3.3.12***.

18.3.3.1 Bit Timing

In ASC mode, each bit (incl. protocol bits) is divided into time quanta in order to provide granularity in the sub-bit range to adjust the sample point to the application requirements. The number of time quanta per bit is defined by bit fields BRG.DCTQ and the length of a time quantum is given by BRG.PCTQ.

In the example given in ***Figure 79***, one bit time is composed of 16 time quanta (BRG.DCTQ = 15). It is not recommended to program less than 4 time quanta per bit time.

Bit field PCR.SP determines the position of the sampling point for the bit value. The value of PCR.SP must not be set to a value greater than BRG.DCTQ.

It is possible to sample the bit value only once per bit time or to take the average of samples. Depending on bit PCR.SMD, either the current input value is directly sampled as bit value, or a majority decision over the input values sampled at the latest three time quanta is taken into account.

The standard ASC bit timing consists of 16 time quanta (BRG.DCTQ = 15) with sampling after 8 or 9 time quanta (PCR.SP = 8 or 9) with majority decision (PCR.SMD = 1).

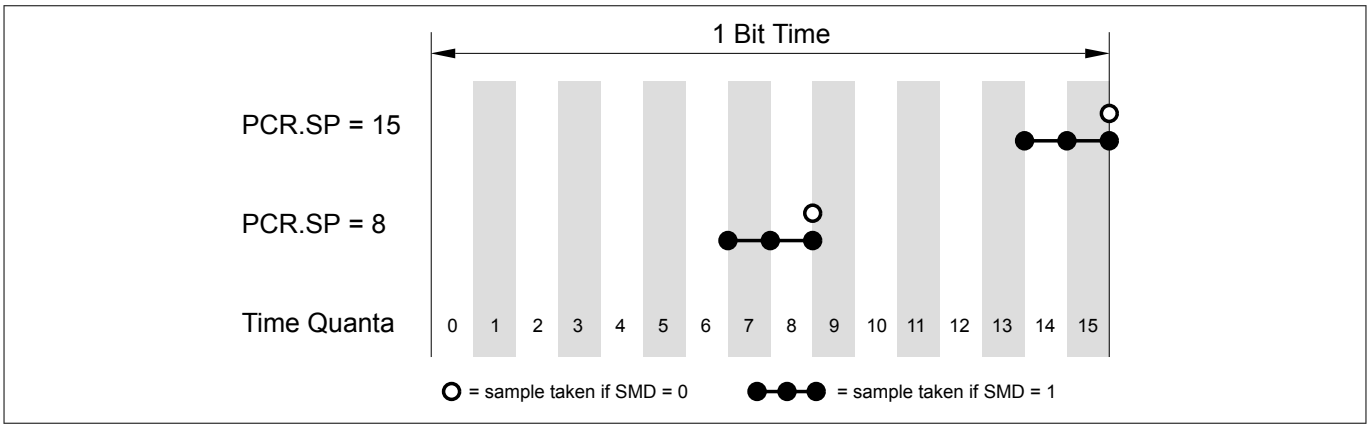


Figure 79 ASC Bit Timing

The bit timing setup (number of time quanta and the sampling point definition) is common for the transmitter and the receiver. Due to independent bit timing blocks, the receiver and the transmitter can be in different time quanta or bit positions inside their frames. The transmission of a frame is aligned to the time quanta generation.

The sample point setting has to be adjusted carefully if collision or idle detection is enabled (via DX1 input signal), because the driver delay and some external delays have to be taken into account. The sample point for the transmit line has to be set to a value where the bit level is stable enough to be evaluated.

If the sample point is located late in the bit time, the signal itself has more time to become stable, but the robustness against differences in the clock frequency of transmitter and receiver decreases.

18.3.3.2 Baud Rate Generation

The baud rate f_{ASC} in ASC mode depends on the number of time quanta per bit time and their timing. The bits in register BRG define the baud rate setting:

- BRG.CTQSEL
  to define the input frequency f_{CTQIN} for the time quanta generation
- BRG.PCTQ
  to define the length of a time quantum (division of f_{CTQIN} by 1, 2, 3, or 4)
- BRG.DCTQ
  to define the number of time quanta per bit time

The baud rate is given by:

$$f_{ASC} = f_{CTQIN} \times \frac{1}{PCTQ + 1} \times \frac{1}{DCTQ + 1}$$

Equation 14

The standard setting is given by CTQSEL = 00_B ($f_{CTQIN} = f_{PDIV}$), PPPEN = 0 ($f_{PPP} = f_{PIN}$) and CLKSEL = 00_B ($f_{PIN} = f_{FD}$). Under these conditions, the baud rate can further be equated to either ***Equation 15*** or ***Equation 16***, depending on the selected divider mode:

$$f_{ASC} = f_{PERIPH} \times \frac{1}{1024 - STEP} \times \frac{1}{PDIV + 1} \times \frac{1}{PCTQ + 1} \times \frac{1}{DCTQ + 1}$$

Equation 15 Normal divider mode (FDR.DM = 01_B)

$$f_{ASC} = f_{PERIPH} \times \frac{STEP}{1024} \times \frac{1}{PDIV + 1} \times \frac{1}{PCTQ + 1} \times \frac{1}{DCTQ + 1}$$

Equation 16 Fractional divider mode (FDR.DM = 10_B)

Table 195 shows examples of the baud rate calculation in fractional divider mode (FDR.DM = 10_B).

Table 195 ASC Baud Rate Calculation in Fractional Divider Mode

f_{PERIPH} (MHz)	FDR.STEP	BRG.PDIV	BRG.PCTQ	BRG.DCTQ	f_{ASC} (kbit/s)	Deviation Error
48	472	71	1	15	9.6	0.03%
48	472	35	1	15	19.2	0.03%
48	472	5	1	15	115.2	0.03%
48	512	2	0	7	1000	0.00%

The baud rate setting should only be changed while the transmitter and the receiver are idle.

18.3.3.3 Automatic Shadow Mechanism

The contents of the protocol control register PCR, as well as bit field SCTR.FLE are internally kept constant while a data frame is transferred by an automatic shadow mechanism (shadowing takes place with each frame start).

The registers can be programmed all the time with new settings that are taken into account for the next data frame. During a data frame transfer, the applied (shadowed) setting is not changed, although new values have been written after the start of the data frame.

Bit fields SCTR.WLE and SCTR.SDIR are shadowed automatically with the start of each data word. As a result, a data frame can consist of data words with a different length. It is recommended to change SCTR.SDIR only when no data frame is running to avoid interference between hardware and software.

Please note that the starting point of a data word can be different for a transmitter and a receiver. In order to ensure correct handling, it is recommended to modify SCTR.WLE only while transmitter and receiver are both idle. If the transmitter and the receiver are referring to the same data signal (e.g. in a LIN bus system), SCTR.WLE can be modified while a data transfer is in progress after the RSI event has been detected.

18.3.3.4 Mode Control Behavior

In ASC mode, the following kernel modes are supported:

- Run Mode 0/1:

  Behavior as programmed, no impact on data transfers. Default is Run Mode 0.
- Stop Mode 0:

  Bit PSR.TXIDLE is cleared. A new transmission is not started. A current transmission is finished normally. Bit PSR.RXIDLE is not modified. Reception is still possible. When leaving stop mode 0, bit TXIDLE is set according to PCR.IDM.
- Stop Mode 1:

  Bit PSR.TXIDLE is cleared. A new transmission is not started. A current transmission is finished normally. Bit PSR.RXIDLE is cleared. A new reception is not possible. A current reception is finished normally. When leaving stop mode 1, bits TXIDLE and RXIDLE are set according to PCR.IDM.

18.3.3.5 Disabling ASC Mode

In order to switch off ASC mode without any data corruption, the receiver and the transmitter have to be both idle. This is ensured by requesting Stop Mode 1 in register KSCFG. After waiting for the end of the frame, the ASC mode can be disabled.

18.3.3.6 Data Transfer Interrupt Handling

The data transfer interrupts indicate events related to ASC frame handling.

Table 196 ASC data transfer interrupt handling

Interrupt	Indicated by bit	Description
Transmit buffer interrupt	PSR.TBIF	Set after the start of first data bit of a data word. With this event, bit TCSR.TDV is cleared and new data can be loaded to the transmit buffer. This is the earliest point in time when a new data word can be written to TBUF.
Transmit shift interrupt	PSR.TSIF	Set after the start of the last data bit of a data word.
Receiver start interrupt	PSR.RSIF	Set after the sample point of the first data bit of a data word.
Receiver interrupt	PSR.RIF	RIF is set after the sampling point of the last data bit of a data word if this data word is not directly followed by a parity bit (parity generation disabled or not the last word of a data frame). If the data word is directly followed by a parity bit (last data word of a data frame and parity generation enabled), RIF is set after the sampling point of the parity bit if no parity error has been detected. If a parity error has been detected, AIF is set instead of RIF. The first data word of a data frame is indicated by RBUFSR.SOF = 1 for the received word.
Alternative interrupt	PSR.AIF	
Data lost interrupt	PSR.DLIF	Set if the data word available in register RBUF (oldest data word from RBUF0 or RBUF1) has not been read out before it becomes overwritten with new incoming data.

18.3.3.7 Protocol Interrupt Events

The following protocol-related events are generated in ASC mode and can lead to a protocol interrupt.

Please note that the bits in register PSR are not automatically cleared by hardware and have to be cleared by software in order to monitor new incoming events.

Table 197 ASC protocol interrupt events

Events	Event flag	Description	Flag clear	Interrupt enable
Transmitter events				

Table 197 ASC protocol interrupt events (continued)

Events	Event flag	Description	Flag clear	Interrupt enable
Collision detection	PSR.COL	Transmitted value (DOUT0) does not match with the input value of the DX1 input stage at the sample point of a bit.	PSCR.CST3	PCR.CDEN
Transmitter frame finished	PSR.TFF	Transmitter has completely finished a frame. TFF becomes set at the end of the last stop bit. The DOUT0 signal assignment to port pins can be changed while no transmission is in progress.	PSCR.CST8	PCR.FFIEN
Receiver events				
Receiver frame finished	PSR.RFF	Receiver has completely finished a frame. RFF becomes set at the end of the last stop bit. The DIN0 signal assignment to port pins can be changed while no reception is in progress.	PSCR.CST7	PCR.FFIEN
Synchroni-zation break detection	PSR.SBD	Used in LIN networks to indicate the reception of the synchronization break symbol (at the beginning of a LIN frame).	PSCR.CST2	PCR.SBIEN
Receiver noise detection	PSR.RNS	Input value at the sample point of a bit and at the two time quanta before are not identical.	PSCR.CST4	PCR.RNIEN
Format error	PSR. FER0/FER1	A format error is signalled if the sampled bit value of a stop bit is 0.	PSCR. CST5/CST6	PCR.FEIEN

18.3.3.8 Baud Rate Generator Interrupt Handling

The baud rate generator interrupt indicate that the capture mode timer has reached its maximum value. With this event, the bit PSR.BRGIF is set.

18.3.3.9 Protocol-Related Argument and Error

The protocol-related argument (RBUFSR.PAR) and the protocol-related error (RBUFSR.PERR) are two flags that are assigned to each received data word in the corresponding receiver buffer status registers.

In ASC mode, the received parity bit is monitored by the PAR flag and the result of the parity check by the PERR flag (0 = received parity bit equal to calculated parity value).

This information being elaborated only for the last received data word of each data frame, both bit positions are 0 for data words that are not the last data word of a data frame or if the parity generation is disabled.

18.3.3.10 Receive FIFO Buffer Handling

If a receive FIFO buffer is enabled for data handling (RBCTR.SIZE > 0), it is recommended to set RBCTR.RCIM = 11_B in ASC mode. This leads to the following indications on the 5-bit field OUTR.RCI:

- RCI[0]: A 1 indicates that the data word has been the first data word of a new data frame
- RCI[3]: The bit containes the received parity bit value
- RCI[4]: A 1 indicates a parity error

The standard receive buffer event and the alternative receive buffer event can be used for the following operations in RCI mode (RBCTR.RNM = 1):

- A standard receive buffer event (TRBSR.SRBI = 1) indicates that a data word can be read from OUTR that has been received without parity error.
- An alternative receive buffer event (TRBSR.ARBI = 1) indicates that a data word can be read from OUTR that has been received with parity error.

18.3.3.11 Data Flow Handling

This section describes the data flow during data transmission and reception.

Data Transmission

Data transmission is initiated by loading the transmit buffer TBUF with the data word to be transmitted, through one of the transmit buffer input locations (TBUFx). If the transmit FIFO is used, one of the transmit FIFO buffer input locations (INx) should be used instead of TBUFx.

If the transmitter is not busy transmitting a previous data word, the data word will be immediately updated to the transmit shift register. This is indicated by a transmit buffer interrupt event (PSR.TBIF = 1).

The transmit buffer interrupt event can be used to indicate that the next data word can now be loaded to TBUF.

For each data word, the start of transmission of the last data bit is indicated by a transmit shift interrupt event (PSR.TSIF = 1). The end of transmission of a complete data frame is indicated by the transmit frame finished event (PSR.TFF = 1).

Figure 80 shows a simplified data transmission flow with TBUFx. For an example with transmit FIFO, refer to ***Chapter 18.2.8.4***.

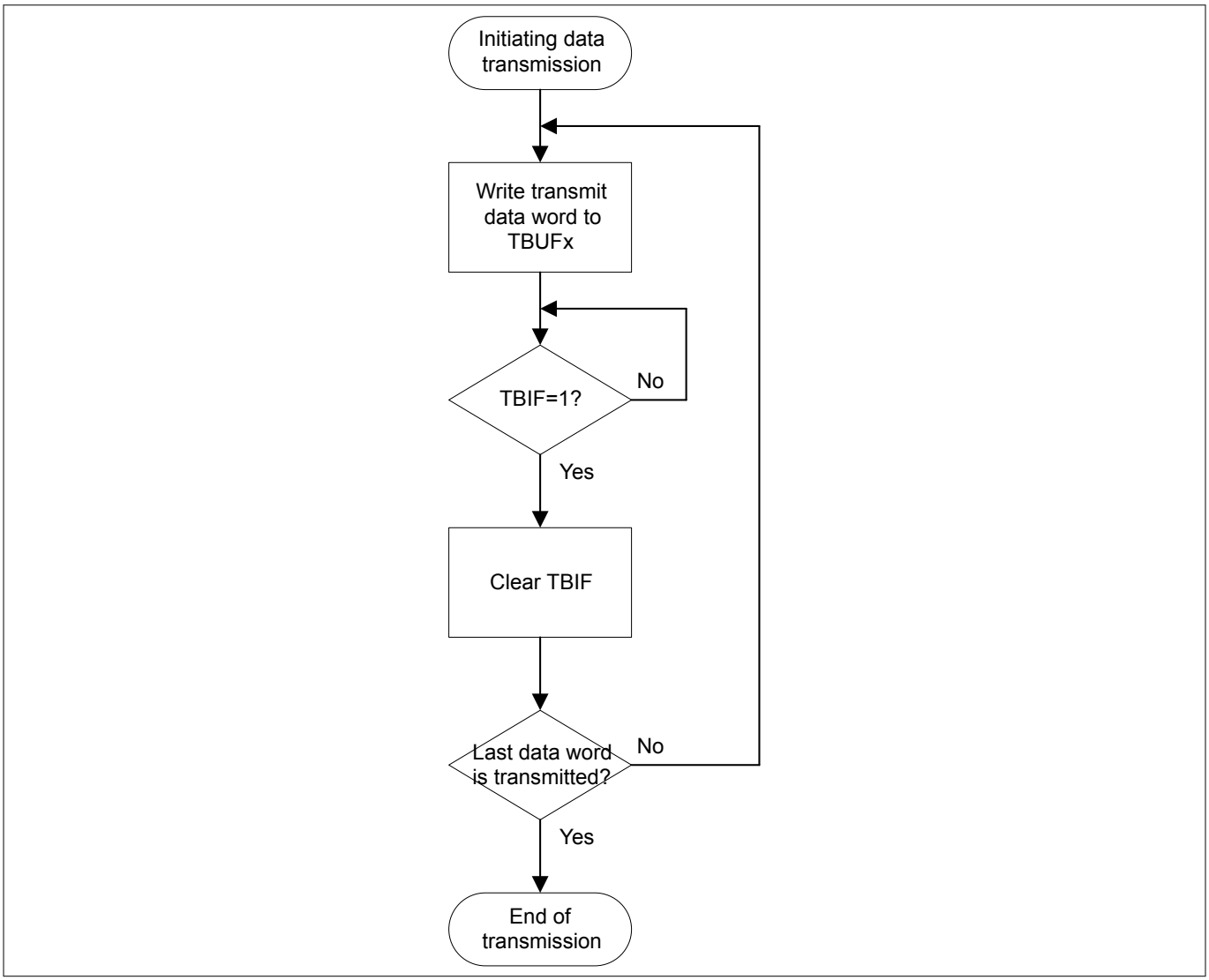


Figure 80 Simplified Data Transmission Flow

Data Reception

Data reception is initiated with the detection of a valid start bit on the receive input line.The receiver continues to sample the incoming data frame and shifts it into the available receive shift register.

For each data word, the sampling of the first data bit is indicated by a receive start interrupt event (PSR.RSIF = 1).

When the number of bits corresponding to the data word length is received, the contents of the receive shift register are transferred to the corresponding receive buffer (RBUF0 or RBUF1). This is indicated by a receive interrupt event (PSR.RIF) or an alternate receive interrupt event (PSR.AIF) if parity is enabled and a parity error is detected.

The reception of a complete data frame, after the last stop bit is received, is indicated by the receive frame finished event (PSR.RFF).

The user needs to read only the RBUF register for the received data word. If the receive FIFO buffer is used, the received data word should be read from register OUTR instead of RBUF.

Figure 81 shows a simplified data reception flow with RBUF. For an example with receive FIFO buffer, refer to ***Chapter 18.2.8.7***.

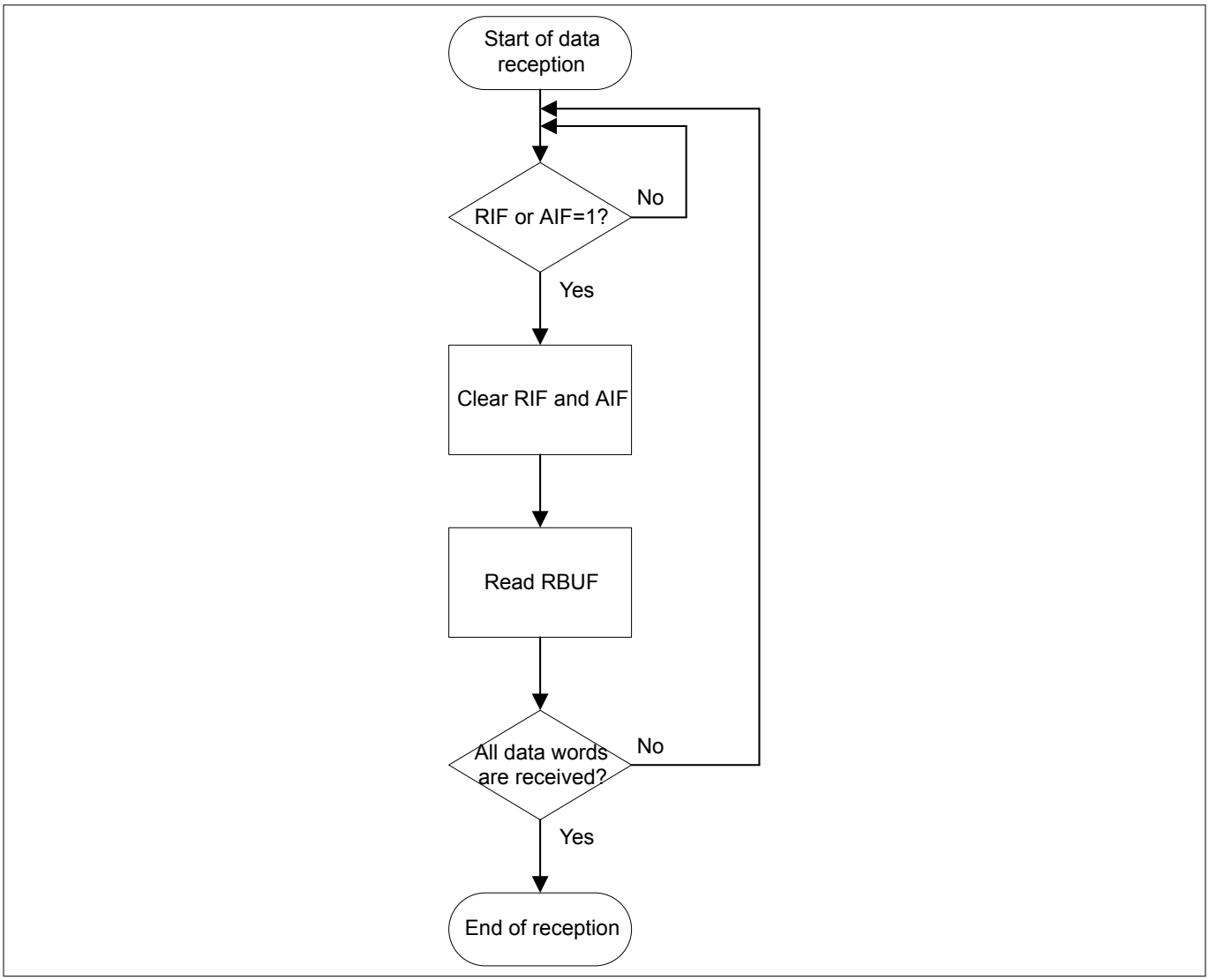


Figure 81 Simplified Data Reception Flow

Interrupt Events on Data Transfer

Figure 82 shows the interrupt events during an ASC data transfer for both the transmitter and the receiver.

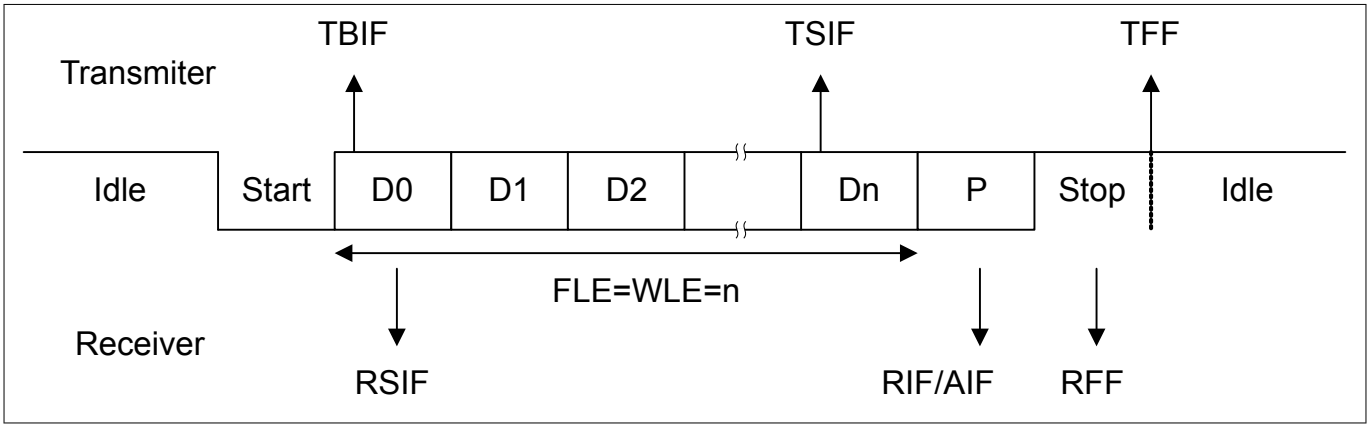


Figure 82 Interrupt Events on Data Transfer

18.3.3.12 Initialization Code Example

The following code shows an example of an ASC initialization sequence:

```
void USIC0_CH1_Init(void)
{
/// ----------------------------------------------------------------------
/// 1. Enable USIC0 channel 1
/// ----------------------------------------------------------------------
    //                    BPMODEN     MODEN
    USIC0_CH1->KSCFG |= (1 << 1) | (1 << 0);

/// ----------------------------------------------------------------------
/// 2. Configure baud rate generator
///    - Fractional divider mode
///    - Baud rate = 19200 bit/s
///    - 16 time quanta per bit time
///    - Length of time quanta = 2 / f_CTQIN
/// ----------------------------------------------------------------------
    //                   DM          STEP
    USIC0_CH1->FDR = (2 << 14) | (472 << 0);
    //                   PDIV        DCTQ         PCTQ
    USIC0_CH1->BRG = (35 << 16) | (15 << 10) | (1 << 8);

/// ----------------------------------------------------------------------
/// 3. Configure input stages
///    - Select input DX0C
///    - Protocol pre-processor to control input of data shift unit
/// ----------------------------------------------------------------------
    //                    INSW       DSEL
    USIC0_CH1->DX0CR = (0 << 4) | (2 << 0);

/// ----------------------------------------------------------------------
/// 4. Configure data format
///    - Data word = data frame = 8 bits
///    - Data transfer allowed with passive level = 1 and LSB first
/// ----------------------------------------------------------------------
    //                    WLE       FLE       TRM     PDL      SDIR
    USIC0_CH1->SCTR = (7 << 24)|(7 << 16)|(1 << 8)|(1 << 1)|(0 << 0);

/// ----------------------------------------------------------------------
/// 5. Configure data transfer parameters
///    - Single shot transmission of data word when a valid word
///      is available
/// ----------------------------------------------------------------------
    //                   TDEN      TDSSM
    USIC0_CH1->TCSR = (1 << 10)|(1 << 8);

/// ----------------------------------------------------------------------
/// 6. Configure ASC protocol-specific parameters
///    - 1 stop bit
///    - Bit value is majority of the values sampled at the
///      latest 3 time quanta with respect to bit 8
```

```
/// ----------------------------------------------------------------------
    //                   SP       STPB     SMD
    USIC0_CH1->PCR = (8 << 8)|(0 << 1)|(1 << 0);

/// ----------------------------------------------------------------------
/// 7. Enable ASC protocol and select parity mode
///    - No parity is selected
/// ----------------------------------------------------------------------
    //                   PM      MODE
    USIC0_CH1->CCR = (0 << 8)|(2 << 0);
/// ----------------------------------------------------------------------
/// 8. Configure ASC output function pins
///    - Assume P0.7 ALT7 function is assigned to DOUT0
/// ----------------------------------------------------------------------
    //                    PC7
    PORT0->IOCR4 |= (0x17 << 27);
}
```

18.3.4 Additional Features

The next sub-sections describe additional features supported in the ASC mode.

18.3.4.1 Noise Detection

The ASC receiver permanently checks the data input line of the DX0 stage for noise (the check is independent from the setting of bit PCR.SMD).

Bit PSR.RNS (receiver noise) becomes set if the three input samples of the majority decision are not identical at the sample point for the bit value.

The information about receiver noise gets accumulated over several bits in bit PSR.RNS (it has to be cleared by software) and can trigger a protocol interrupt each time noise is detected if enabled by PCR.RNIEN.

18.3.4.2 Collision Detection

In some applications, such as data transfer over a single data line shared by several sending devices (see ***Figure 77***), several transmitters have the possibility to send on the same data output line TXD.

In order to avoid collisions of transmitters being active at the same time or to allow a kind of arbitration, a collision detection has been implemented. The data value read at the RXD input at the DX1 stage and the transmitted data bit value are compared after the sampling of each bit value.

If enabled by PCR.CDEN = 1 and a bit sent is not equal to the bit read back, a collision is detected and bit PSR.COL is set. The transmitter stops its data transmission (the data output lines become 1) and generates a protocol interrupt. The content of the transmit shift register is considered as invalid, so the transmit buffer has to be programmed again.

18.3.4.3 Pulse Shaping

For some applications, the 0 level of transmitted bits with the bit value 0 is not applied at the transmit output during the complete bit time. Instead of driving the original 0 level, only a 0 pulse is generated and the remaining time quanta of the bit time are driven with 1 level. The length of a bit time is not changed by the pulse shaping, only the signalling is changed.

In the standard ASC signalling scheme, the 0 level is signalled during the complete bit time with bit value 0 (ensured by programming PCR.PL = 000_B). In the case PCR.PL > 000_B, the transmit output signal becomes 0 for

the number of time quanta defined by PCR.PL. In order to support correct reception with pulse shaping by the transmitter, the sample point has to be adjusted in the receiver according to the applied pulse length.

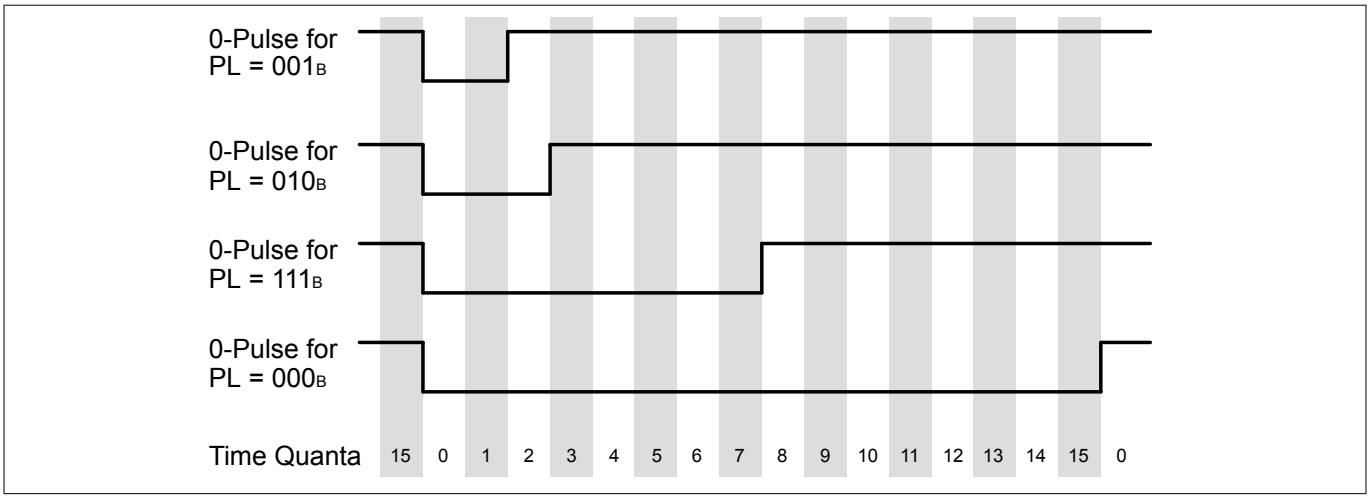


Figure 83 Transmitter Pulse Length Control

Figure 84 shows an example for the transmission of an 8-bit data word with LSB first and one stop bit (e.g. like for IrDA). The polarity of the transmit output signal has been inverted by SCTR.DOCFG = 01_B.

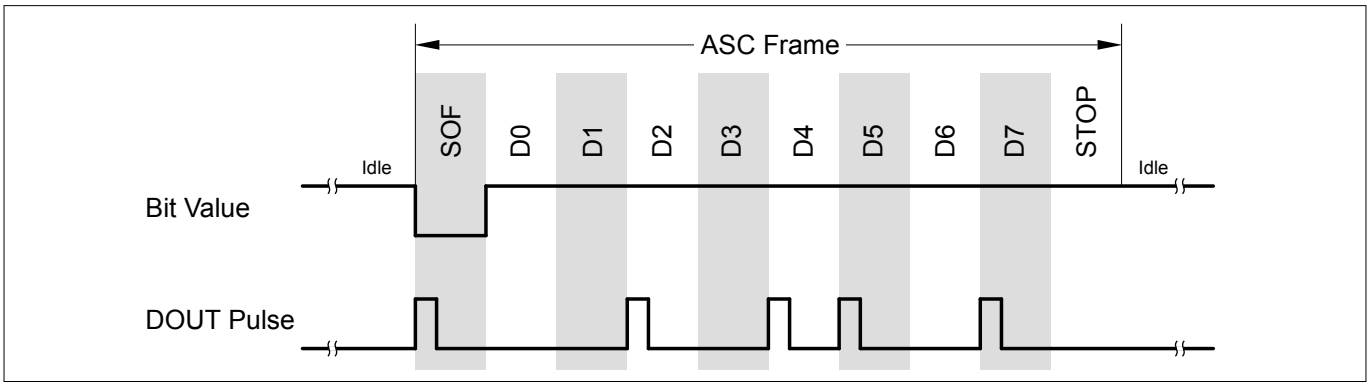


Figure 84 Pulse Output Example

18.3.4.4 End of Frame Control

The number of bits per ASC frame is defined by bit field SCTR.FLE.

In order to support different frame length settings for consecutively transmitted frames, this bit field can be modified by hardware. The automatic update mechanism is enabled by TCSR.FLEMD = 1 (in this case, bits TCSR.WLEMD, SELMD, WAMD and HPCMD have to be written with 0).

If enabled, the transmit control information TCI automatically overwrites the bit field SCTR.FLE when the ASC frame is started (leading to frames with 1 to 32 data bits).

The TCI value represents the written address location of TBUFx (if FIFO is not used) or INxx (if FIFO is used). With this mechanism, an ASC with 8 data bits is generated by writing a data word to TBUF07 (IN07, respectively).

18.3.4.5 Sync-Break Detection

The receiver permanently checks the DIN0 signal for a certain number of consecutive bit times with 0 level. The number is given by the number of programmed bits per frame (SCTR.FLE) plus 2 (in the case without parity) or plus 3 (in the case with parity).

If a 0 level is detected at a sample point of a bit after this event has been found, bit PSR.SBD is set and additionally, a protocol interrupt can be generated (if enabled by PCR.SBIEN = 1).

The counting restarts from 0 each time a falling edge is found at input DIN0.

This feature can be used for the detection of a synchronization break for slave devices in a LIN bus system (the master does not check for sync break).

For example, in a configuration for 8 data bits without parity generation, bit PCR.SBD is set at the next sample point at 0 level after 10 complete bit times have elapsed (representing the sample point of the 11th bit time since the first falling edge).

18.3.4.6 Transfer Status Indication

The receiver status can be monitored by flag PSR.BUSY if the receiver status enable bit PCR.RSTEN is set. In this case, BUSY is set during a complete frame reception from the beginning of the start of frame bit to the end of the last stop bit.

The transmitter status can be monitored by the same BUSY flag if the transmitter status enable bit PCR.TSTEN is set. In this case, bit BUSY is set during a complete frame transmission from the beginning of the start of frame bit to the end of the last stop bit.

If both bits RSTEN and TSTEN are set, flag BUSY indicates the logical OR-combination of the receiver and the transmitter status.

If both bits are cleared, flag BUSY is not modified depending on the transfer status (status changes are ignored).

18.3.5 Hardware LIN Support

In order to support the LIN protocol, bit TCSR.FLEMD = 1 should be set for the master. For slave devices, it can be cleared and the fixed number of 8 data bits has to be set (SCTR.FLE = 7_H). For both, master and slave devices, the parity generation has to be switched off (CCR.PM = 00_B) and transfers take place with LSB first (SCTR.SDIR = 0) and 1 stop bit (PCR.STPB = 0).

The Local Interconnect Network (LIN) data exchange protocol contains several symbols that can all be handled in ASC mode. Each single LIN symbol represents a complete ASC frame. The LIN bus is a master-slave bus system with a single master and multiple slaves (for the exact definition please refer to the official LIN specification).

A complete LIN frame contains the following symbols:

- Synchronization break:

  The master sends a synchronization break to signal the beginning of a new frame. It contains at least 13 consecutive bit times at 0 level, followed by at least one bit time at 1 level (corresponding to 1 stop bit). Therefore, TBUF11 if the transmit buffer is used, (or IN11 if the FIFO buffer is used) has to be written with 0 (leading to a frame with SOF followed by 12 data bits at 0 level). A slave device shall detect 11 consecutive bit times at 0 level, which done by the synchronization break detection. Bit PSR.SBD is set if such an event is detected and a protocol interrupt can be generated. Additionally, the received data value of 0 appears in the receive buffer and a format error is signaled. If the baud rate of the slave has to be adapted to the master, the baud rate measurement has to be enabled for falling edges by setting BRG.TMEN = 1, DX0CR.CM = 10_H and DX1CR.CM = 00_H before the next symbol starts.
- Synchronization byte:

  The master sends this symbol after writing the data value 55_H to TBUF07 (or IN07). A slave device can either receive this symbol without any further action (and can discard it) or it can use the falling edges for baud rate measurement. Bit PSR.TSIF = 1 (with optionally the corresponding interrupt) indicates the detection of a falling edge and the capturing of the elapsed time since the last falling edge in CMTR.CTV. Valid captured values can be read out after the second, third, fourth and fifth activation of TSIF. After the fifth activation of TSIF within this symbol, the baud rate detection can be disabled (BRG.TMEN = 0) and BRG.PDIV can be

programmed with the captured CMTR.CTV value divided by twice the number of time quanta per bit (assuming BRG.PCTQ = 00_B).

- Other symbols:

  The other symbols of a LIN frame can be handled with ASC data frames without specific actions.

If LIN frames should be sent out on a frame base by the LIN master, the input DX2 can be connected to external timers to trigger the transmit actions (e.g. the synchronization break symbol has been prepared but is started if a trigger occurs). Please note that during the baud rate measurement of the ASC receiver, the ASC transmitter of the same USIC channel can still perform a transmission.

18.4 Synchronous Serial Channel (SSC)

The synchronous serial channel SSC covers the data transfer function of an SPI-like module. It can handle reception and transmission of synchronous data frames between a device operating in master mode and at least one device in slave mode.

Besides the standard SSC protocol consisting of one input and one output data line, SSC protocols with two (Dual-SSC) or four (Quad-SSC) input/output data lines are also supported.

The SSC mode is selected by CCR.MODE = 0001_B.

18.4.1 Signal Description

A synchronous SSC data transfer is characterized by a simultaneous transfer of a shift clock signal together with the transmit and/or receive data signal(s) to determine when the data is valid (definition of transmit and sample point).

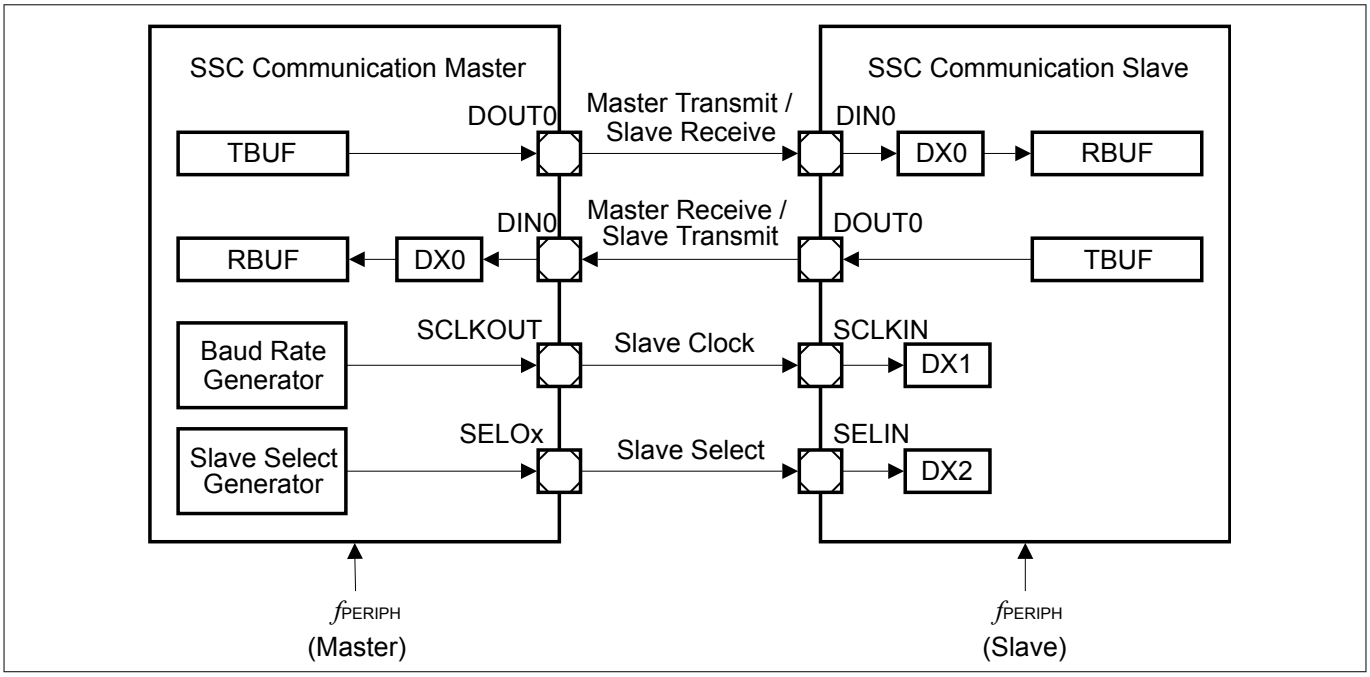


Figure 85 SSC Signals for Standard Full-Duplex Communication

In order to explicitly indicate the start and the end of a data transfer and to address more than one slave devices individually, the SSC module supports the handling of slave select signals. They are optional and are not necessarily needed for SSC data transfers. The SSC module supports up to 8 different slave select output signals for master mode operation (named SELOx, with x = 0-7) and 1 slave select input SELIN for slave mode. In most applications, the slave select signals are active low.

A device operating in master mode controls the start and end of a data frame, as well as the generation of the shift clock and slave select signals. This comprises the baud rate setting for the shift clock and the delays between the shift clock and the slave select output signals. If several SSC modules are connected together, there can be only one SSC master at a time, but several slaves. Slave devices receive the shift clock and optionally a slave select signal(s).

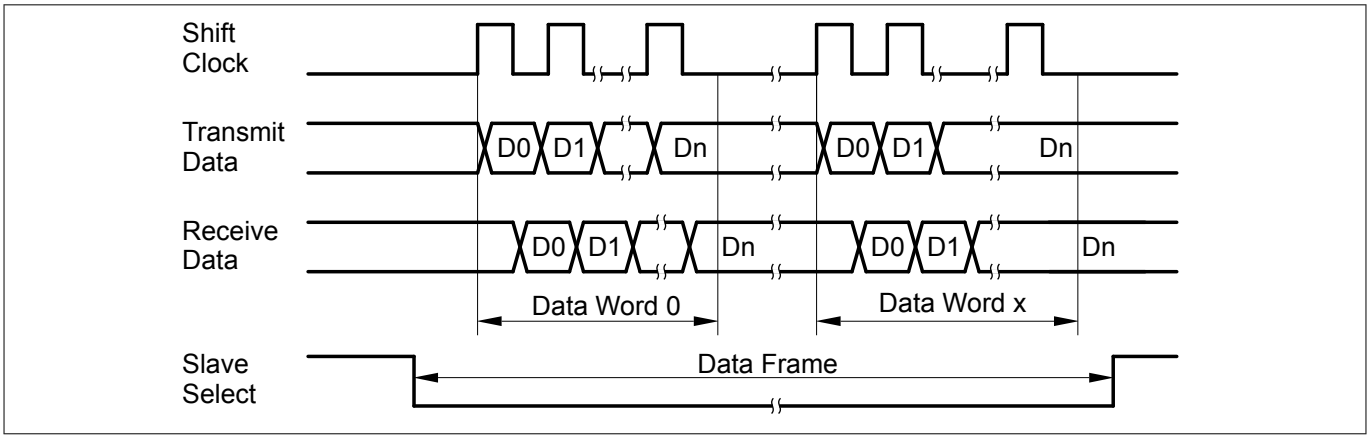


Figure 86 4-Wire SSC Standard Communication Signals

18.4.1.1 Transmit and Receive Data Signals

In standard SSC **half-duplex mode**, a single data line is used, either for data transfer from the master to a slave or from a slave to the master. In this case, MRST and MTSR are connected together, one signal as input, the other one as output, depending on the data direction. The user software has to take care about the data direction to avoid data collision (e.g. by preparing dummy data of all 1s for transmission in case of a wired AND connection with open-drain drivers, by enabling/disabling push/pull output drivers or by switching pin direction with hardware port control enabled).

In **full-duplex mode**, data transfers take place in parallel between the master device and a slave device via two independent data signals MTSR and MRST, as shown in ***Figure 85***.

Figure 87 shows the SSC data signal paths for both Master and Slave modes.

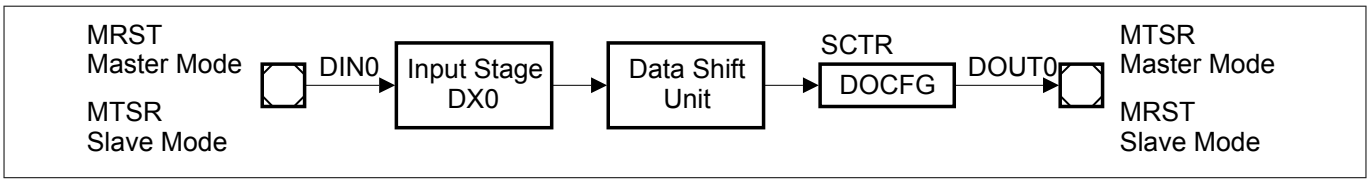


Figure 87 SSC Data Signals

The receive data input signal DIN0 is handled by the input stage DX0. In master mode (referring to MRST) as well as in slave mode (referring to MTSR), the data input signal DIN0 is taken from an input pin.

The signal polarity of DOUT0 (data output) with respect to the data bit value can be configured in block DOCFG (data output configuration) by bit field SCTR.DOCFG.

Note: For dual- and quad-SSC modes that require multiple input and output data lines to be used, additional input stages, DINx and DOUTx signals need to be set up.

18.4.1.2 Shift Clock Signals

Figure 88 shows the SSC shift clock signal paths for both Master and Slave modes.

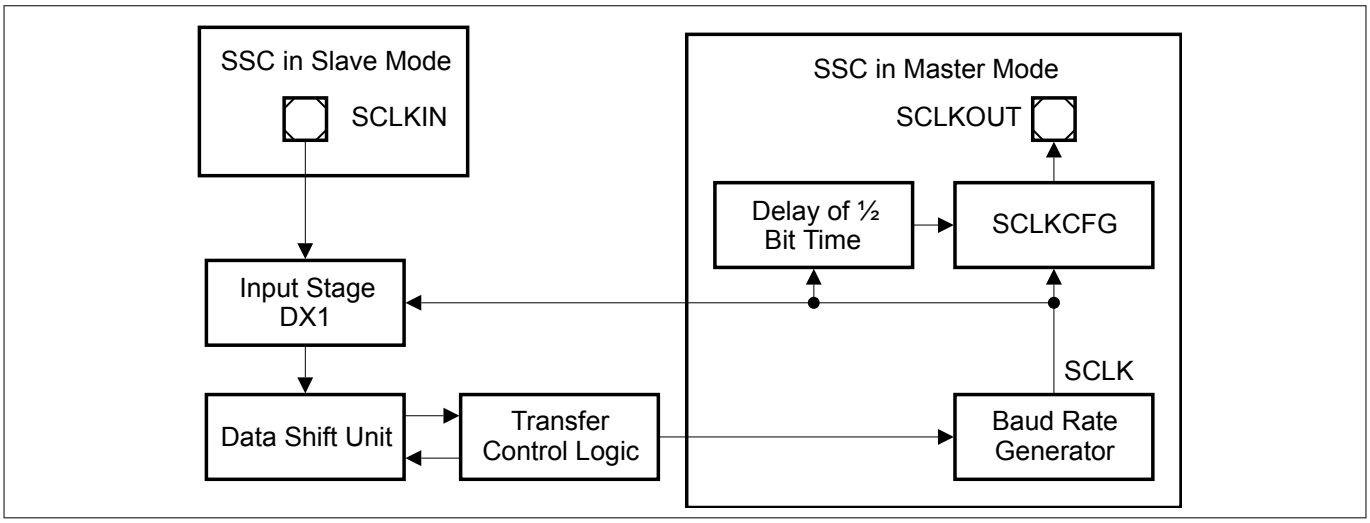


Figure 88 SSC Shift Clock Signals

Master Mode

In master mode, the shift clock is generated by the internal baud rate generator. The output signal SCLK of the baud rate generator is taken as shift clock input for the data shift unit.

The internal signal SCLK is made available for external slave devices by signal SCLKOUT.

Shift Clock Configuration in Master Mode

Due to the multitude of different SSC applications, there are different ways to configure the shift clock output signal SCLKOUT with respect to SCLK.

This is done in the block SCLKCFG (shift clock configuration) by bit field BRG.SCLKCFG, allowing 4 possible settings, which are described in ***Figure 89*** and ***Table 198***.

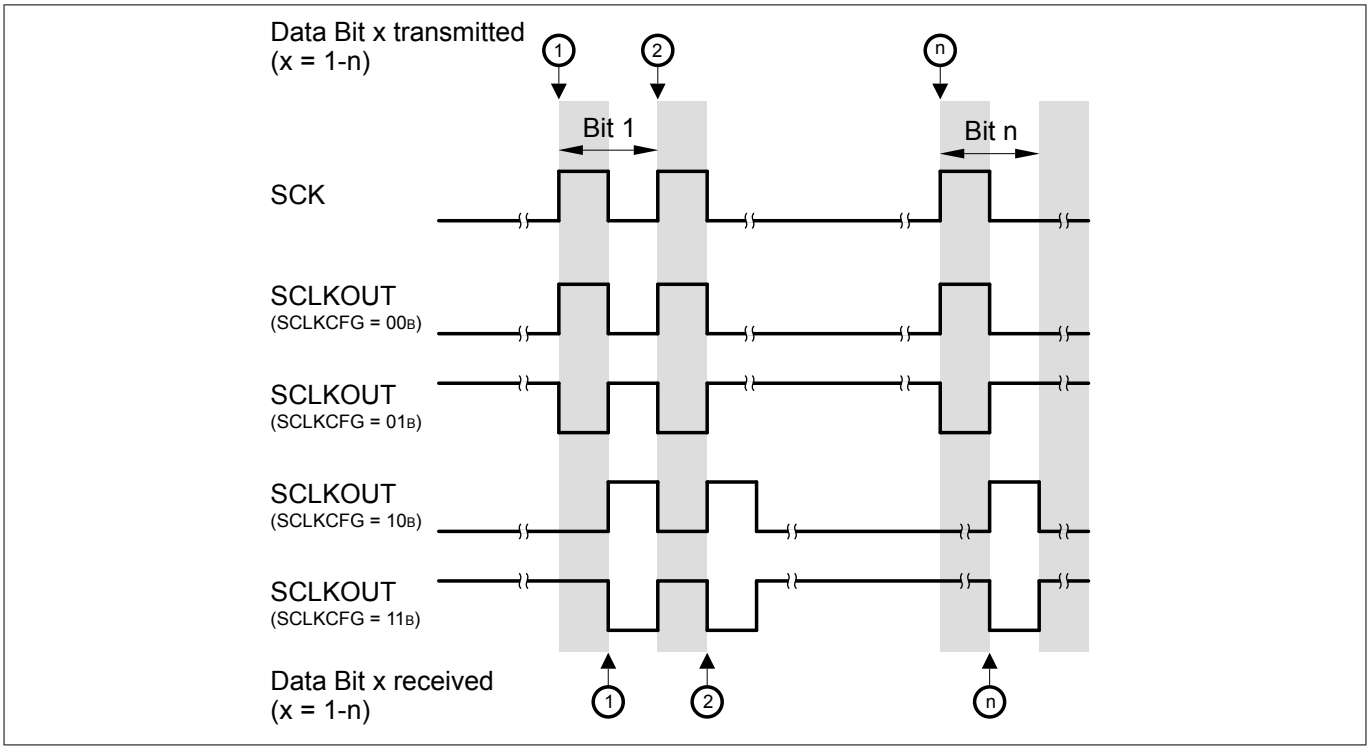


Figure 89 SCLKOUT Configuration in SSC Master Mode

Table 198 Shift Clock Configuration in Master Mode

SCLKCFG	Description
00	No delay, no polarity inversion (SCLKOUT equals SCLK) • The inactive level of SCLKOUT is 0, while no data frame is transferred. • The first data bit of a new data frame is transmitted with the first rising edge of SCLKOUT and the first data bit is received in with the first falling edge of SCLKOUT. • The last data bit of a data frame is transmitted with the last rising clock edge of SCLKOUT and the last data bit is received in with the last falling edge of SCLKOUT. • This setting corresponds to the behavior of the internal data shift unit.
01	No delay, with polarity inversion • The inactive level of SCLKOUT is 1, while no data frame is transferred. • The first data bit of a new data frame is transmitted with the first falling clock edge of SCLKOUT and the first data bit is received with the first rising edge of SCLKOUT. • The last data bit of a data frame is transmitted with the last falling edge of SCLKOUT and the last data bit is received with the last rising edge of SCLKOUT.
10	SCLKOUT delayed by 1/2 shift clock period, no polarity inversion • The inactive level of SCLKOUT is 0, while no data frame is transferred. • The first data bit of a new data frame is transmitted 1/2 shift clock period before the first rising clock edge of SCLKOUT. • Due to the delay, the next data bits seem to be transmitted with the falling edges of SCLKOUT. • The last data bit of a data frame is transmitted 1/2 period of SCLKOUT before the last rising clock edge of SCLKOUT. • The first data bit is received 1/2 shift clock period before the first falling edge of SCLKOUT. • Due to the delay, the next data bits seem to be received with the rising edges of SCLKOUT. • The last data bit is received 1/2 period of SCLKOUT before the last falling clock edge of SCLKOUT. *Note: The connected slave has to provide the first data bit before the first SCLKOUT edge, e.g. as soon as it is addressed by its slave select.*
11	SCLKOUT delayed by 1/2 shift clock period, with polarity inversion • The inactive level of SCLKOUT is 1, while no data frame is transferred. • The first data bit of a new data frame is transmitted 1/2 shift clock period before the first falling clock edge of SCLKOUT. • Due to the delay, the next data bits seem to be transmitted with the rising edges of SCLKOUT. • The last data bit of a data frame is transmitted 1/2 period of SCLKOUT before the last falling clock edge of SCLKOUT. • The first data bit is received 1/2 shift clock period before the first rising edge of SCLKOUT. • Due to the delay, the next data bits seem to be received with the falling edges of SCLKOUT. • The last data bit is received 1/2 period of SCLKOUT before the last rising clock edge of SCLKOUT. *Note: The connected slave has to provide the first data bit before the first SCLKOUT edge, e.g. as soon as it is addressed by its slave select.*

Slave Mode

In slave mode, the shift clock signal is handled by the input stage DX1.

The signal SCLKIN is received from an external master, so the DX1 stage has to be connected to an input pin.

For complete closed loop delay compensation in slave mode, the transmit shift clock from the input stage DX1 can be additionally routed to the SCLKOUT signal, which is otherwise not used in the slave mode. The selection is done through the bit BRG.SCLKOSEL. See ***Chapter 18.4.6.3*** for details.

Supporting Different Shift Clock Configurations in Slave Mode

The DX1 input stage can invert the received input signal with bit DX1CR.DPOL to adapt to the polarity of SCLKIN to the function of the data shift unit (data transmission on rising edges, data reception on falling edges).

In addition, the bit PCR.SLPHSEL can be used to configure the clock phase of the data shift.

- When SLPHSEL = 0_B, the slave SSC transmits data bits with each leading edge of the selected shift clock input (SCLKIN) and receives data bits with each trailing edge of SCLKIN
- When SLPHSEL = 1_B, the slave SSC transmits the first data bit once the selected slave select input (SELIN) becomes active. If SELIN is not used, the DX2 stage has to deliver a 1-level to the data shift unit to shift out the first bit. Subsequent data bits are then transmitted with each trailing edge of SCLKIN. The SSC slave receives all data bits with each leading edge of SCLKIN.

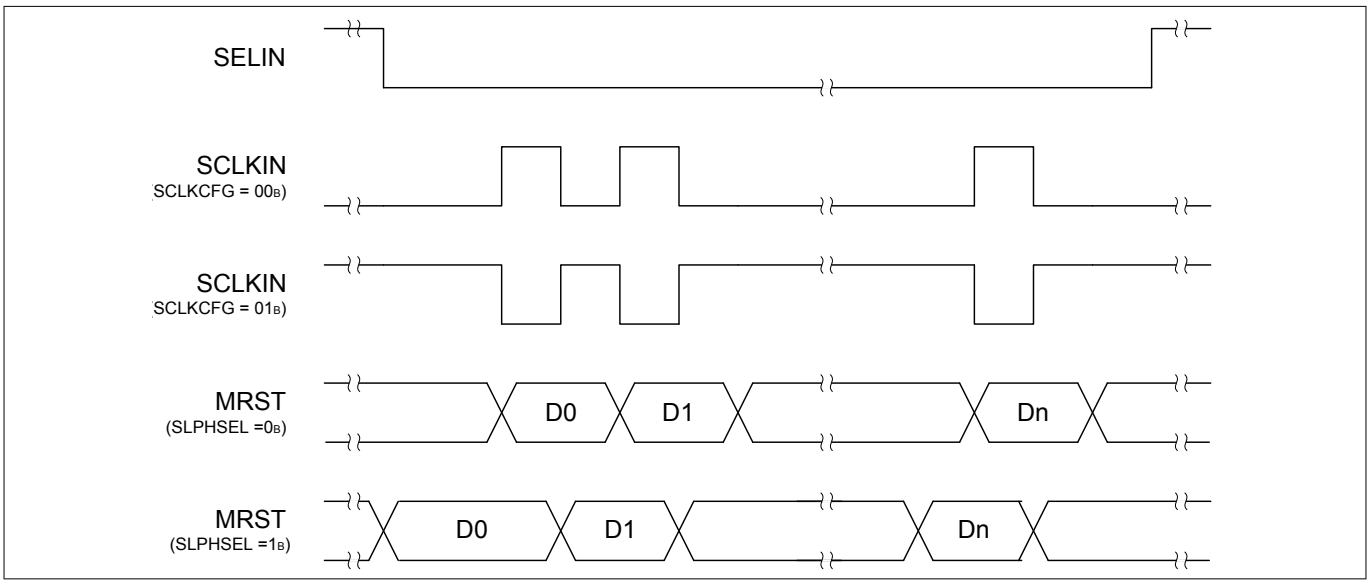


Figure 90 SLPHSEL Configuration in SSC Slave Mode

18.4.1.3 Slave Select Signals

Figure 91 shows the SSC slave select signal paths for both Master and Slave modes.

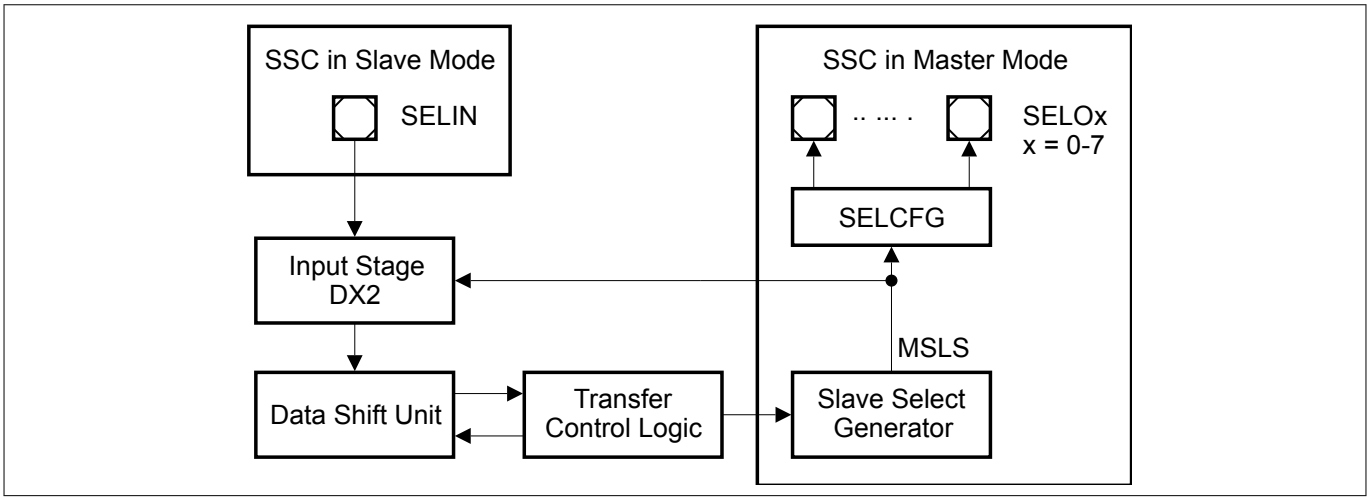


Figure 91 SSC Slave Select Signals

Master Mode

In master mode, a master slave select signal MSLS is generated by the internal slave select generator.

In order to address different external slave devices independently, the internal MSLS signal is made available externally via up to 8 SELOx output signals that can be configured by the block SELCFG (select configuration).

The control of the SELCFG block is based on protocol specific bits and bit fields in the protocol control register PCR:

- PCR.SELCTR to chose between direct and coded select mode
- PCR.SELINV to invert the SELOx outputs
- PCR.SELO[7:0] as individual value for each SELOx line

For the generation of the MSLS signal please refer to ***Chapter 18.4.3.2***.

The SELCFG block supports the following configurations of the SELOx output signals:

- Direct Select Mode (SELCTR = 1):

  Each SELOx line (with x = 0-7) can be directly connected to an external slave device. If bit x in bit field SELO is 0, the SELOx output is permanently inactive. A SELOx output becomes active while the internal signal MSLS is active and bit x in bit field SELO is 1. Several external slave devices can be addressed in parallel if more than one bit in bit field SELO are set during a data frame. The number of external slave devices that can be addressed individually is limited to the number of available SELOx outputs.
- Coded Select Mode (SELCTR = 0):

  The SELOx lines (with x = 1-7) can be used as addresses for an external address decoder to increase the number of external slave devices. These lines only change with the start of a new data frame and have no other relation to MSLS. Signal SELO0 can be used as enable signal for the external address decoder. It is active while MSLS is active (during a data frame) and bit 0 in bit field SELO is 1. Furthermore, in coded select mode, this output line is delayed by one cycle of f_{PERIPH} compared to MSLS to allow the other SELOx lines to stabilize before enabling the address decoder.

Slave Mode

In slave mode, the slave select signal is handled by the input stage DX2. The input signal SELIN is received from an external master via an input pin.

The input stage can invert the received input signal to adapt the polarity of signal SELIN to the function of the data shift unit (the module internal signals are considered as high active, so a data transfer is only possible while the slave select input of the data shift unit is at 1-level, otherwise, shift clock pulses are ignored and do not lead to data transfers).

If an input signal SELIN is low active, it should be inverted in the DX2 input stage.

18.4.2 Operating the SSC

This chapter contains SSC issues, that are of general interest and not directly linked to either master mode or slave mode.

18.4.2.1 Automatic Shadow Mechanism

The contents of the baud rate control register BRG, bit fields SCTR.FLE as well as the protocol control register PCR are internally kept constant while a data frame is transferred (= while MSLS is active) by an automatic shadow mechanism. The registers can be programmed all the time with new settings that are taken into account for the next data frame. During a data frame, the applied (shadowed) setting is not changed, although new values have been written after the start of the data frame.

Bit fields SCTR.WLE, SCTR.DSM, SCTR.HPCDIR and SCTR.SDIR are shadowed automatically with the start of each data word. As a result, a data frame can consist of data words with a different length, or data words that are transmitted or received through different number of data lines. It is recommended to change SCTR.SDIR only when no data frame is running to avoid interference between hardware and software.

Please note that the starting point of a data word are different for a transmitter (first bit transmitted) and a receiver (first bit received). In order to ensure correct handling, it is recommended to refer to the receive start interrupt RSI before modifying SCTR.WLE. If TCSR.WLEMD = 1, it is recommended to update TCSR and TBUFx after the receiver start interrupt has been generated.

18.4.2.2 Mode Control Behavior

In SSC mode, the following kernel modes are supported:

- Run Mode 0/1:

  Behavior as programmed, no impact on data transfers.
- Stop Mode 0/1:

  The content of the transmit buffer is considered as not valid for transmission. Although being considered as 0, bit TCSR.TDV it is not modified by the stop mode condition.

  - In master mode, a currently running word transfer is finished normally, but no new data word is started (the stop condition is not considered as end-of-frame condition).
  - In slave mode, a currently running word transfer is finished normally.

    Passive data will be sent out instead of a valid data word if a data word transfer is started by the external master while the slave device is in stop mode. In order to avoid passive slave transmit data, it is recommended not to program stop mode for an SSC slave device if the master device does not respect the slave device’s stop mode.

18.4.2.3 Disabling SSC Mode

In order to disable SSC mode without any data corruption, the receiver and the transmitter have to be both idle. This is ensured by requesting Stop Mode 1 in register KSCFG and waiting for a currently running word transfer to finish.

18.4.2.4 Data Frame Control

An SSC data frame can consist of several consecutive data words that may be separated by an inter-word delay. Without inter-word delay, the data words seem to form a longer data word, being equivalent to a data frame. The length of the data words are most commonly identical within a data frame, but may also differ from one word to another.

The data word length information (defined by SCTR.WLE) is evaluated for each new data word, whereas the frame length information (defined by SCTR.FLE) is evaluated at the beginning at each start of a new frame.

The length of an SSC data frame can be defined in two different ways:

- By the number of bits per frame:

  If the number of bits per data frame is defined (frame length FLE), a slave select signal is not necessarily required to indicate the start and the end of a data frame. If the programmed number of bits per frame is reached within a data word, the frame is considered as finished and remaining data bits in the last data word are ignored and are not transferred.

  This method can be applied for data frames with up to 63 data bits.
- By the slave select signal:

  If the number of bits per data frame is not known, the start/end information of a data frame is given by a slave select signal. If a deactivation of the slave select signal is detected within a data word, the frame is considered as finished and remaining data bits in the last data word are ignored and are not transferred.

  This method has to be applied for frames with more than 63 data bits (programming limit of FLE). The advantage of slave select signals is the clearly defined start and end condition of data frames in a data stream. Furthermore, slave select signals allow to address slave devices individually.

18.4.2.5 Parity Mode

The SSC allows parity generation for transmission and parity check for reception on frame base. The type of parity can be selected by bit field CCR.PM, common for transmission and reception (no parity, even or odd parity). If the parity handling is disabled, the SSC frame does not contain any parity bit.

For consistency reasons, all communication partners have to be programmed to the same parity mode.

If parity generation has been enabled, the transmitter automatically extends the clock by one cycle after the last data word of the data frame, and sends out its calculated parity bit in this cycle.

Figure 92 shows how a parity bit is added to the transmitted data bits of a frame. The number of the transmitted bits of a complete frame with parity is always one more than that without parity. The parity bit is transmitted as the last bit of a frame, following the data bits, independent of the shift direction (SCTR.SDIR).

Note: For dual and quad SSC protocols, the parity bit will be transmitted and received only on DOUT0 and DX0 respectively in the extended clock cycle.

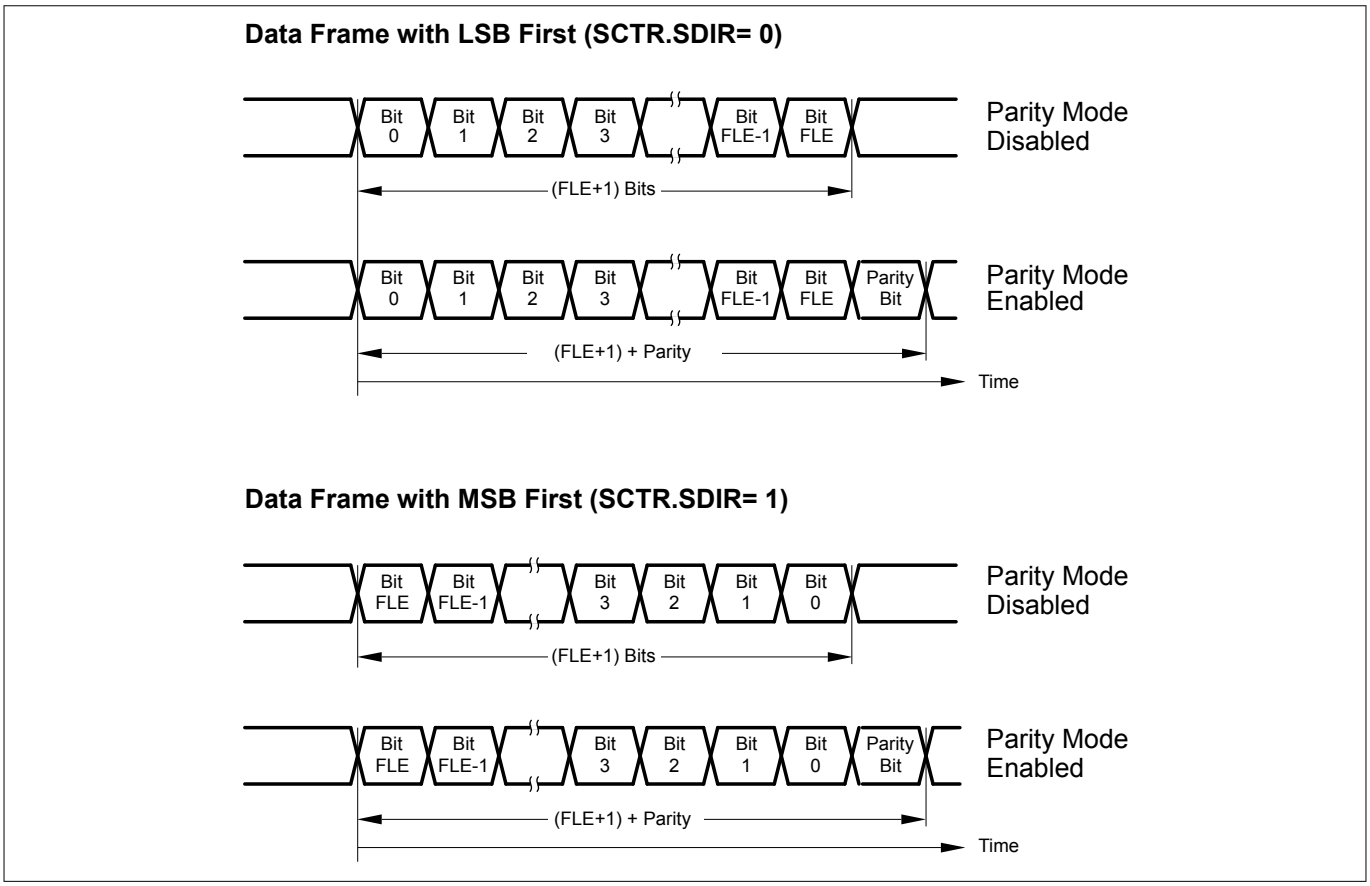


Figure 92 Data Frames without/with Parity

Similarly, after the receiver receives the last word of a data frame as defined by FLE, it expects an additional one clock cycle, which will contain the parity bit. The receiver interprets this bit as received parity and separates it from the received data. The received parity bit value is instead monitored in the protocol-related argument (PAR) of the receiver buffer status registers as receiver buffer status information. The receiver compares the bit to its internally calculated parity and the result of the parity check is indicated by the flag PSR.PARERR. The parity error event generates a protocol interrupt if PCR.PARIEN = 1.

Parity bit generation and detection is not supported for the following cases:

- When frame length is 64 data bits or greater, i.e. FLE = 63_H;
- When in slave mode, the end of frame occurs before the number of data bits defined by FLE is reached.
- When in slave mode, the content of the TBUF is not valid at the transmission start. In this case, the slave outputs the level defined by SCTR.PDL including for the parity bit. This might result in the detection of a parity error at the master.

18.4.2.6 Data Transfer Interrupt Handling

The data transfer interrupts indicate events related to SSC frame handling.

Table 199 SSC Data transfer interrupt handling

Interrupt	Indicated by bit	Description
Transmit buffer interrupt	PSR.TBIF	Set after the start of first data bit of a data word.

Table 199 SSC Data transfer interrupt handling (continued)

Interrupt	Indicated by bit	Description
Transmit shift interrupt	PSR.TSIF	Set after the start of the last data bit of a data word.
Receiver start interrupt	PSR.RSIF	Set after the reception of the first data bit of a data word. This is the earliest point in time when a new data word can be written to TBUF. With this event, bit TCSR.TDV is cleared and new data can be loaded to the transmit buffer.
Receiver interrupt	PSR.RIF	The reception of the second, third, and all subsequent words in a multi-word frame is always indicated by RBUFSR.SOF = 0. Bit PSR.RIF is set after the reception of the last data bit of a data word if RBUFSR.SOF = 0. Bit RBUFSR.SOF indicates whether the received data word has been the first data word of a multi-word frame or some subsequent word. In SSC mode, it decides if alternative interrupt or receive interrupt is generated.
Alternative interrupt	PSR.AIF	The reception of the first word in a frame is always indicated by RBUFSR.SOF = 1. Bit PSR.AIF is set after the reception of the last data bit of a data word if RBUFSR.SOF = 1. This is true both in case of reception of multi-word frames and single-word frames.
Data lost interrupt	PSR.DLIF	Set if the data word available in register RBUF (oldest data word from RBUF0 or RBUF1) has not been read out before it becomes overwritten with new incoming data.

18.4.2.7 Protocol-Related Argument and Error

The protocol-related argument (RBUFSR.PAR) and the protocol-related error (RBUFSR.PERR) are two flags that are assigned to each received data word in the corresponding receiver buffer status registers.

In SSC mode, the received parity bit is monitored by the protocol-related argument. The received start of frame indication is monitored by the protocol-related error indication (0 = received word is not the first word of a frame, 1 = received word is the first word of a new frame).

Note: For SSC, the parity error event indication bit is located in the PSR.PARERR register bit field.

18.4.2.8 Receive Buffer Handling

If the FIFO buffer is enabled for data handling (RBCTR.SIZE > 0), it is recommended to set RBCTR.RCIM = 01_B in SSC mode.

This leads to an indication that the data word has been the first data word of a new data frame if bit OUTR.RCI[4] = 1, and the word length of the received data is given by OUTR.RCI[3:0].

The standard receive buffer event and the alternative receive buffer event can be used for the following operation in RCI mode (RBCTR.RNM = 1):

- A standard receive buffer event indicates that a data word can be read from OUTR that has not been the first word of a data frame.
- An alternative receive buffer event indicates that the first data word of a new data frame can be read from OUTR.

18.4.3 Operating the SSC in Master Mode

In order to operate the SSC in master mode, the USIC channel has to be first initialized.

It is recommended to configure all parameters of the SSC that do not change during run time while CCR.MODE = 0000_B, except stated otherwise.

The main initialization steps are outlined below:

- Enable USIC channel
  - Enable the module by writing 1s to MODEN and BPMODEN bits in KSCFG register.
- Configure baud rate generator
  - Select either fractional divider mode or normal divider mode with FDR.DM bit.
  - Configure the baud rate setting through register BRG and FDR.STEP bit field.
- Configure input pins
  - Establish a connection of input stage DX0 with the receive data input pin (signal DIN0) selected by DX0CR.DSEL bit field and with bit DX0CR.INSW = 1.
  - Program Bit DX1CR.INSW to use the baud rate generator output SCLK directly as input for the data shift unit.
  - Program Bit DX2CR.INSW to use the slave select generator output MSLS as input for the data shift unit.
- Configure data format
  - The word length, the frame length, the shift direction and the shift mode have to be set up according to the application requirements by programming the register SCTR.
  - Write SCTR.TRM = 01 to enable SSC data transfers.
- Configure data transfer parameters
  - Write TCSR.TDSSM = 1 and TCSR.TDEN = 01 to enable data transmission in single shot mode.
- Configure protocol control parameters
  - Enable slave select generation by setting bit field PCR.MSLSEN = 1.
  - Select the mode, the polarity and the active slave select output signal through the bit fields SELCTR, SELINV and SELO in PCR register respectively.
  - Configure the slave select delays if necessary, through registers BRG and PCR, see ***Chapter 18.4.3.3***.
  - Select the frame end mode with the bit field PCR.FEM.
- Select SSC protocol
  - Enable SSC mode with CCR.MODE = 0001_B.
- Configure output pins
  - Configure the transmit data (signal DOUT0), the shift clock (signal SCLKOUT) and slave select (signal SELOx) output pins through the selected pins' port control registers Pn_IOCR0/4/8/12. Refer to the port chapter.
  - The step to enable the output pin functions should only be done after the SSC mode is enabled with CCR.MODE, to avoided unintended spikes on the output.

An initialization code example is given in ***Chapter 18.4.3.8***.

Note: The USIC can only receive in master mode if it is transmitting, because the master frame handling refers to bit TDV of the transmitter part.

18.4.3.1 Baud Rate Generation

The baud rate (determining the length of one data bit) of the SSC is defined by the frequency of the SCLK signal (one period of f_{SCLK} represents one data bit).

The SSC baud rate generation does not imply any time quanta counter.

The standard setting is given by PPPEN = 0 ($f_{PPP} = f_{PIN}$) and CLKSEL = 00_B ($f_{PIN} = f_{FD}$). Under these conditions, the baud rate is given by either ***Equation 17*** or ***Equation 18***, depending on the selected divider mode:

$$f_{SCLK} = \frac{1}{2} \times f_{PERIPH} \times \frac{1}{1024 - STEP} \times \frac{1}{PDIV + 1}$$

Equation 17 Normal divider mode (FDR.DM = 01_B)

$$f_{SCLK} = \frac{1}{2} \times f_{PERIPH} \times \frac{STEP}{1024} \times \frac{1}{PDIV + 1}$$

Equation 18 Fractional divider mode (FDR.DM = 10_B)

Table 200 shows examples of the baud rate calculation in fractional divider mode (FDR.DM = 10_B).

Table 200 SSC Baud Rate Calculation in Fractional Divider Mode

f_{PERIPH} (MHz)	FDR.STEP	BRG.PDIV	f_{SCLK} (kbit/s)	Deviation Error
48	256	624	9.6	0.00%
48	512	23	500	0.00%
48	512	7	1500	0.00%
48	512	0	12000	0.00%

18.4.3.2 MSLS Generation and Slave Select Delays

The slave select signals indicate the start and the end of a data frame and are also used by the communication master to individually select the desired slave device.

A slave select output of the communication master becomes active a programmable time before a data part of the frame is started (**leading delay T_{ld}**), necessary to prepare the slave device for the following communication.

After the transfer of a data part of the frame, it becomes inactive again a programmable time after the end of the last bit (**trailing delay T_{td}**) to respect the slave hold time requirements.

If data frames are transferred back-to-back one after the other, the minimum time between the deactivation of the slave select and the next activation of a slave select is programmable (**next-frame delay T_{nf}**).

If a data frame consists of more than one data word, an optional delay between the data words can also be programmed (**inter-word delay T_{iw}**).

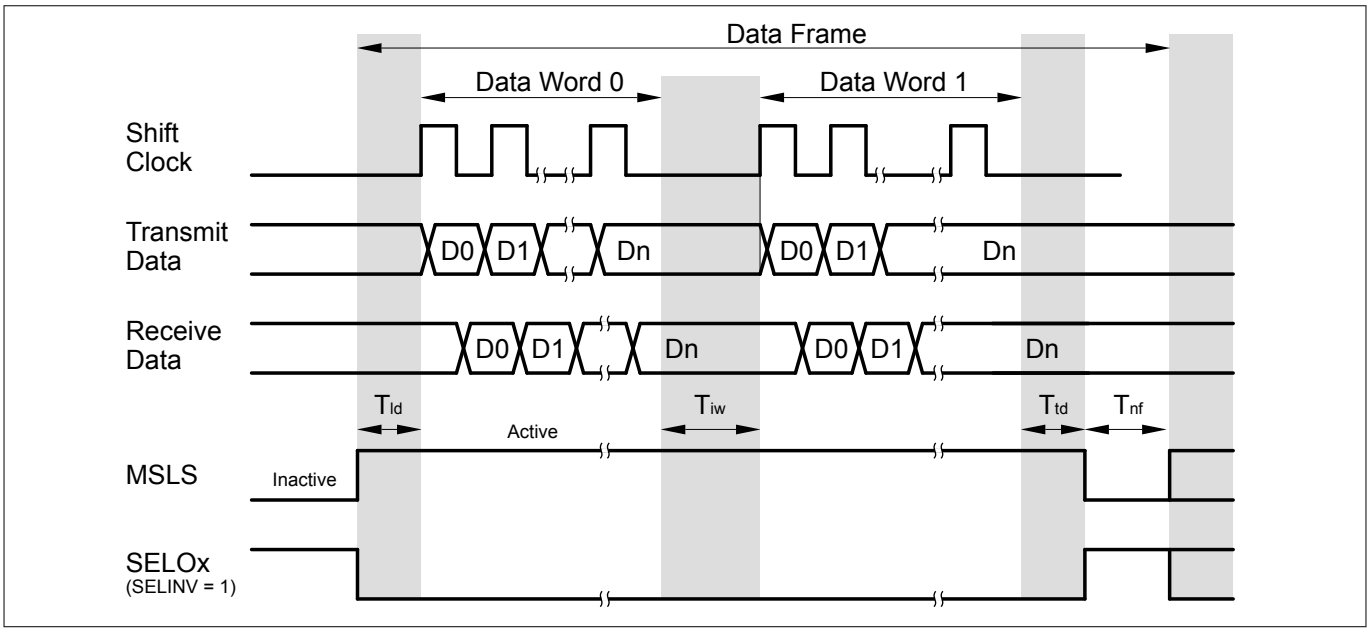


Figure 93 MSLS Generation in SSC Master Mode

In SSC master mode, the slave select delays are defined as follows:

Leading delay T_{ld}

The leading delay starts if valid data is available for transmission. The internal signal MSLS becomes active with the start of the leading delay. The first shift clock edge (rising edge) of SCLK is generated by the baud rate generator after the leading delay has elapsed.

Trailing delay T_{td}

The trailing delay starts at the end of the last SCLK cycle of a data frame. The internal signal MSLS becomes inactive with the end of the trailing delay.

Inter-word delay T_{iw}

This delay is optional and can be enabled/disabled by PCR.TIWEN. If the inter-word delay is disabled (TIWEN = 0), the last data bit of a data word is directly followed by the first data bit of the next data word of the same data frame. If enabled (TIWEN = 1), the inter-word delay starts at the end of the last SCLK cycle of a data word. The first SCLK cycle of the following data word of the same data frame is started when the inter-word delay has elapsed. During this time, no shift clock pulses are generated and signal MSLS stays active. The communication partner has time to “digest” the previous data word or to prepare for the next one.

Next-frame delay T_{nf}

The next-frame delay starts at the end of the trailing delay. During this time, no shift clock pulses are generated and signal MSLS stays inactive. A frame is considered as finished after the next-frame delay has elapsed.

18.4.3.3 Configuration of Slave Select Delays

The slave select delay generation is based on time quanta. The length of a time quantum (defined by the period of the f_{CTQIN}) and the number of time quanta per delay can be programmed.

In standard SSC applications, the leading delay T_{ld} and the trailing delay T_{td} are mainly used to ensure stability on the input and output lines as well as to respect setup and hold times of the input stages. These two delays have the same length (in most cases shorter than a bit time) and can be programmed with the same set of bit fields.

- BRG.CTQSEL
  to define the input frequency f_{CTQIN} for the time quanta generation for T_{ld} and T_{td}
- BRG.PCTQ
  to define the length of a time quantum (division of f_{CTQIN} by 1, 2, 3, or 4) for T_{ld} and T_{td}
- BRG.DCTQ
  to define the number of time quanta for the delay generation for T_{ld} and T_{td}

The inter-word delay T_{iw} and the next-frame delay T_{nf} are used to handle received data or to prepare data for the next word or frame. These two delays have the same length (in most cases in the bit time range) and can be programmed with a second, independent set of bit fields.

- PCR.CTQSEL1
  to define the input frequency f_{CTQIN} for the time quanta generation for T_{nf} and T_{iw}
- PCR.PCTQ1
  to define the length of a time quantum (division of f_{CTQIN} by 1, 2, 3, or 4) for T_{nf} and T_{iw}
- PCR.DCTQ1
  to define the number of time quanta for the delay generation for T_{nf} and T_{iw}
- PCR.TIWEN
  to enable/disable the inter-word delay T_{iw}

Each delay depends on the length of a time quantum and the programmed number of time quanta given by the bit fields CTQSEL/CTQSEL1, PCTQ/DCTQ and PCTQ1/DCTQ1 (the coding of CTQSEL1 is similar to CTQSEL, etc.).

To provide a high flexibility in programming the delay length, the input frequencies can be selected between several possibilities (e.g. based on bit times or on the faster inputs of the protocol-related divider). The delay times are defined as follows:

$$T_{ld} = T_{td} = \frac{(PCTQ + 1) \times (DCTQ + 1)}{f_{CTQIN}}$$

$$T_{iw} = T_{nf} = \frac{(PCTQ1 + 1) \times (DCTQ1 + 1)}{f_{CTQIN}}$$

Equation 19

18.4.3.4 Automatic Slave Select Update

If the number of bits per SSC frame and the word length are defined by bit fields SCTR.FLE and SCTR.WLE, the transmit control information TCI can be used to update the slave select setting PCR.CTR[23:16] to control the SELOx select outputs.

The automatic update mechanism is enabled by TCSR.SELMD = 1 (bits TCSR.WLEMD, FLEMD, and WAMD have to be cleared). In this case, the TCI of the first data word of a frame defines the slave select setting of the complete frame due to the automatic shadow mechanism (see ***Automatic Shadow Mechanism*** on page 390).

18.4.3.5 Protocol Interrupt Events

The following protocol-related events generated in SSC mode and can lead to a protocol interrupt.

They are related to the start and the end of a data frame. After the start of a data frame a new setting could be programmed for the next data frame and after the end of a data frame the SSC connections to pins can be changed.

Please note that the bits in register PSR are not all automatically cleared by hardware and have to be cleared by software in order to monitor new incoming events.

Table 201 SSC master mode protocol interrupt events

Events	Event flag	Description	Flag clear	Interrupt enable
MSLS interrupt	PSR.MSLSEV	Set with any change of the internal MSLS signal in maser mode (MSLS generation enabled). This event indicates that a data frame has been started (activation of MSLS) or finished (deactivation of MSLS). The actual state of the internal MSLS signal can be read out at PSR.MSLS to take appropriate actions when this interrupt has been detected.	PSCR.CST2	PCR.MSLSIEN
DX2T interrupt	PSR.DX2TEV	Set after an activation of the trigger signal DX2T. This event monitors edges of the input signal of the DX2 stage (although this signal is not used as slave select input for data transfers). The actual state of the selected input signal can be read out at PSR.DX2S to take appropriate actions when this interrupt has been detected.	PSCR.CST3	PCR.DX2TIEN
Parity error interrupt	PSR.PARERR	Set if there is a mismatch between the received parity bit (in RBUFSR.PAR) and the calculated parity bit, of the data frame.	PSCR.CST4	PCR.PARIEN

18.4.3.6 End-of-Frame Control

The information about the frame length is required for the MSLS generator of the master device.

In addition to the mechanism based on the number of bits per frame (selected with SCTR.FLE < 63), the following alternative mechanisms for end of frame handling are supported.

It is recommended to set SCTRFLE = 63 (if several end of frame mechanisms are activated in parallel, the first end condition being found finishes the frame).

Software-based start of frame indication TCSR.SOF

This mechanism can be used if software handles the TBUF data without data FIFO. If bit SOF is set, a valid content of TBUF is considered as first word of a new frame. Bit SOF has to be set before the content of TBUF is transferred to the transmit shift register, so it is recommended to write it before writing data to TBUF. A current data word transfer is finished completely and the slave select delays T_{td} and T_{nf} are applied before starting a new data frame with T_{ld} and the content of TBUF.

For software-handling of bit SOF, bit TCSR.WLEMD = 0 has to be programmed. In this case, all TBUFx (x = 00 to 31) address locations show an identical behavior (TCI not taken into account for data handling).

Software-based end of frame indication TCSR.EOF

This mechanism can be used if software handles the TBUF data without data FIFO. If bit EOF is set, a valid content of TBUF is considered as last word of a new frame. Bit EOF has to be set before the content of TBUF is transferred to the transmit shift register, so it is recommended to write it before writing data to TBUF. The

data word in TBUF is sent out completely and the slave select delays T_{td} and T_{nf} are applied. A new data frame can start with T_{ld} with the next valid TBUF value.

For software-handling of bit EOF, bit TCSR.WLEMD = 0 has to be programmed. In this case, all TBUFx address locations show an identical behavior (TCI not taken into account for data handling).

Software-based address related end of frame handling

This mechanism can be used if software handles the TBUF data without data FIFO. If bit TCSR.WLEMD = 1, the address of the written TBUFx is used as transmit control information TCI[4:0] to update SCTR.WLE (= TCI[3:0]) and TCSR.EOF (= TCI[4]) for each data word. The written TBUFx address location defines the word length and the end of a frame (locations TBUF16 to TBUF31 lead to a frame end).

For example, writing transmit data to TBUF07 results in a data word of 8-bit length without finishing the frame, whereas writing transmit data to TBUF31 leads to a data word length of 16 bits, followed by T_{td}, the deactivation of MSLS and T_{nf}.

If TCSR.WLEMD = 1, bits TCSR.EOF and SOF, as well as SCTR.WLE must not be written by software after writing data to a TBUF location. Furthermore, it is recommended to clear bits TCSR.SELMD, FLEMD and WAMD.

FIFO-based address related end of frame handling

This mechanism can be used if a data FIFO is used to store the transmit data. The general behavior is similar to the software-based address related end of frame handling, except that transmit data is not written to the locations TBUFx, but to the FIFO input locations INx (x = 00 to 31) instead. In this case, software must not write to any of the TBUF locations.

TBUF related end of frame handling

If bit PCR.FEM = 0, an end of frame is assumed if the transmit buffer TBUF does not contain valid transmit data at the end of a data word transmission (TCSR.TDV = 0 or in Stop Mode). In this case, the software has to take care that TBUF does not run empty during a data frame in Run Mode. If bit PCR.FEM = 1, signal MSLS stays active while the transmit buffer is waiting for new data (TCSR.TDV = 1 again) or until Stop Mode is left.

Explicit end of frame by software

The software can explicitly stop a frame by clearing bit PSR.MSLS by writing a 1 to the related bit position in register PSCR. This write action immediately clears bit PSR.MSLS, whereas the internal MSLS signal becomes inactive after finishing a currently running word transfer and respecting the slave select delays T_{td} and T_{nf}.

18.4.3.7 Data Flow Handling

Data transmission is initiated by loading the transmit buffer TBUF with the data word to be transmitted, through one of the transmit buffer input locations (TBUFx). If the transmit FIFO is used, one of the transmit FIFO buffer input locations (INx) should be used instead of TBUFx.

If the transmitter is not busy transmitting a previous data word, the MSLS signal becomes active to indicate a start of frame through the MSLS interrupt event (PSR.MSLSEV = 1).

The data word will then be updated to the transmit shift register. This is indicated by a transmit buffer interrupt event (PSR.TBIF = 1).

In the same clock cycle that the first data bit is placed onto the output line MTSR but in the opposite clock edge, the first data bit on the input line MRST is latched and shifted into the available receive shift register. This is indicated by a receive start interrupt event (PSR.RSIF = 1). The receive start interrupt event can be used to indicate that the next data word can now be loaded to TBUF.

For each data word, the start of transmission of the last data bit is indicated by a transmit shift interrupt event (PSR.TSIF = 1).

When the number of bits corresponding to the data word length is received, the contents of the receive shift register are transferred to the corresponding receive buffer (RBUF0 or RBUF1). This is indicated by an alternate receive interrupt event (PSR.AIF) if the received word is the first word of the frame, or by a receive interrupt event (PSR.RIF) if the received word represents subsequent words of the frame.

After the last word of the frame has been completely transmitted, the MSLS signal becomes inactive to indicate an end of frame. A MSLS interrupt event (PSR.MSLSEV = 1) is again triggered.

Figure 94 shows the simplified data transmission and reception flows with TBUFx and RBUF. For examples with FIFO buffer, refer to ***Chapter 18.2.8.4*** and ***Chapter 18.2.8.7***.

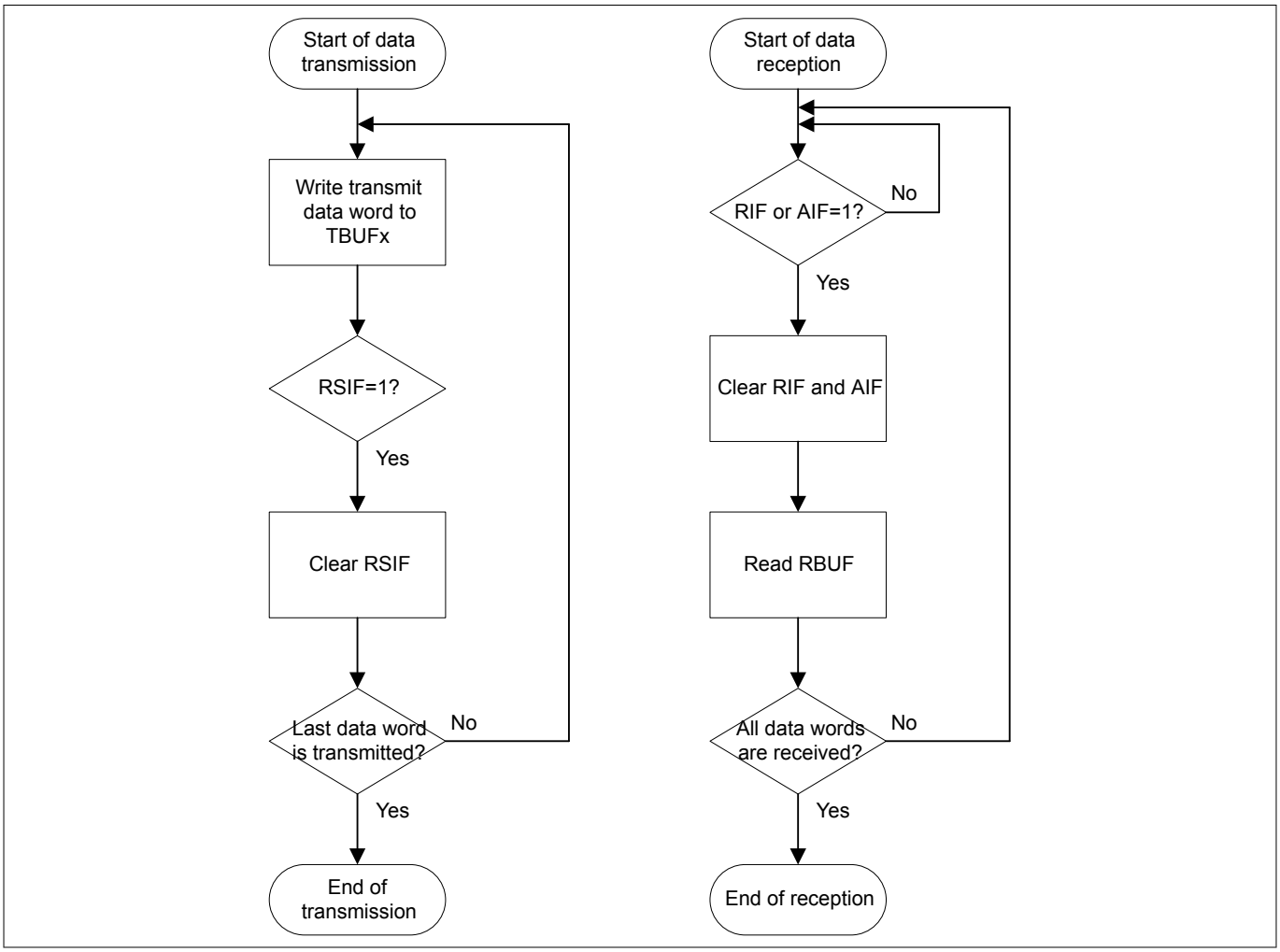


Figure 94 Simplified Data Transmission and Reception Flow

Figure 95 shows the interrupt events during a SSC master mode data transfer.

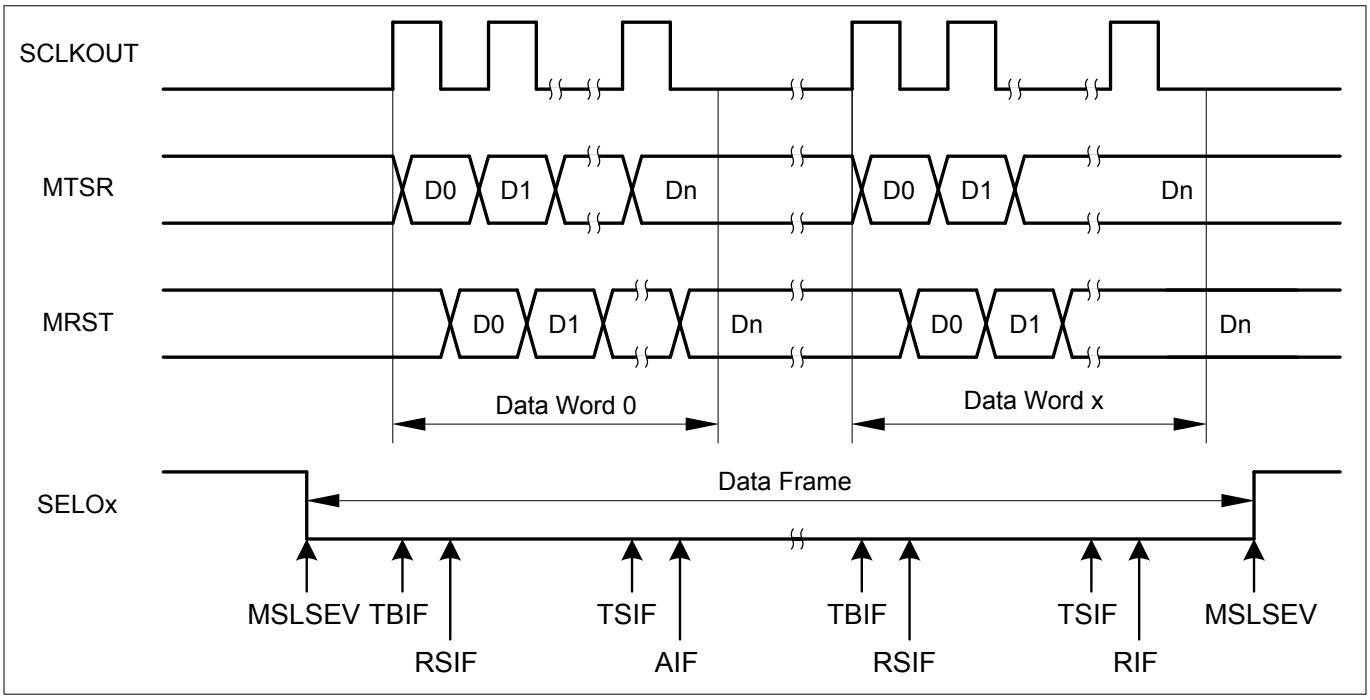


Figure 95 Interrupt Events on Data Transfer

18.4.3.8 Initialization Code Example

The following code example implements a function to initialize a USIC channel for SSC master mode data transfers with a baud rate of 1500 kbit/s (f_{PERIPH} = 48 MHz):

```
void USIC0_CH1_SSC_MasterMode_Init(void)
{
/// ----------------------------------------------------------------------
/// 1. Enable USIC0 channel 1
/// ----------------------------------------------------------------------
    //                    BPMODEN     MODEN
    USIC0_CH1->KSCFG |= (1 << 1) | (1 << 0);

/// ----------------------------------------------------------------------
/// 2. Configure baud rate generator
///    - Fractional divider mode
///    - Baud rate = 1500 kbit/s
/// ----------------------------------------------------------------------
    //                   DM           STEP
    USIC0_CH1->FDR = (2 << 14) | (512 << 0);
    //                  PDIV
    USIC0_CH1->BRG = (7 << 16);

/// ----------------------------------------------------------------------
/// 3. Configure input stages
///    - Select input DX0C
///    - Derive input of data shift unit directly from input pin
/// ----------------------------------------------------------------------
    //                    INSW        DSEL
    USIC0_CH1->DX0CR = (1 << 4) | (2 << 0);

/// ----------------------------------------------------------------------
/// 4. Configure data format
///    - Data word = data frame = 15 bits
///    - Data transfer allowed with passive level = 1 and MSB first
/// ----------------------------------------------------------------------
    //                     WLE        FLE      TRM       PDL      SDIR
    USIC0_CH1->SCTR = (15 << 24)|(15 << 16)|(1 << 8)|(1 << 1)|(1 << 0);

/// ----------------------------------------------------------------------
/// 5. Configure data transfer parameters
///    - Single shot transmission of data word when a valid word
///      is available
/// ----------------------------------------------------------------------
    //                   TDEN        TDSSM
    USIC0_CH1->TCSR = (1 << 10) | (1 << 8);

/// ----------------------------------------------------------------------
/// 6. Configure SSC protocol-specific parameters
///    - Slave select generation is enabled
///    - Direct slave select mode with inversion is selected
///    - End of frame condition is required for the frame to be
///      considered as finished
```

```
///    - SELO0 is selected as the active select signal
/// ----------------------------------------------------------------------
    //                  SELO      FEM    SELINV   SELCTR   MSLSEN
    USIC0_CH1->PCR = (1 << 16)|(1 << 3)|(1 << 2)|(1 << 1)|(1 << 0);

/// ----------------------------------------------------------------------
/// 7. Enable SSC protocol
/// ----------------------------------------------------------------------
    //                 MODE
    USIC0_CH1->CCR = (1 << 0);

/// ----------------------------------------------------------------------
/// 8. Configure SSC output function pins
///    - Assume
///        - P0.7 ALT7 function is assigned to DOUT0
///        - P0.8 ALT7 function is assigned to SCLKOUT
///        - P0.9 ALT7 function is assigned to SELO0
/// ----------------------------------------------------------------------
    //                   PC7
    PORT0->IOCR4 |= (0x27 << 26);
    //                   PC9            PC8
    PORT0->IOCR8 |= (0x27 << 10) | (0x27 << 2);
}
```

18.4.4 Operating the SSC in Slave Mode

In order to operate the SSC in slave mode, the USIC channel has to be first initialized.

It is recommended to configure all parameters of the SSC that do not change during run time while CCR.MODE = 0000_B, except stated otherwise.

The main initialization steps are outlined below:

- Enable USIC channel
  - Enable the module by writing 1s to MODEN and BPMODEN bits in KSCFG register.
- Configure input pins
  - Establish a connection of input stage DX0 with the receive data input pin (signal DIN0) selected by DX0CR.DSEL bit field and with bit DX0CR.INSW = 1.
  - Establish a connection of input stage DX1 with the shift clock input pin (signal SCLKIN) selected by DX1CR.DSEL bit field and with DX1CR.INSW = 1.
  - Establish a connection of input stage DX2 with the slave select input pin (signal SELIN) selected by DX2CR.DSEL bit field and with DX2CR.INSW = 1.

    If no slave select input signal is used, the DX2 stage has to deliver a 1-level to the data shift unit to allow data reception and transmission.

    If a slave device is not selected (DX2 stage delivers a 0 to the data shift unit) and a shift clock pulse are received, the incoming data is not received and the DOUTx signal outputs the passive data level defined by SCTR.PDL.
- Configure data format
  - The word length, the frame length, the shift direction and the shift mode have to be set up according to the application requirements by programming the register SCTR.
  - Write SCTR.TRM = 01_B to enable SSC data transfers.

- Configure data transfer parameters
  - Write TCSR.TDSSM = 1 and TCSR.TDEN = 01_B to enable data transmission in single shot mode.
- Select SSC protocol
  - Enable SSC mode with CCR.MODE = 0001_B.
- Configure output pins
  - Configure the transmit data (signal DOUT0) output pin through the selected pin's port control register Pn_IOCR0/4/8/12. Refer to the port chapter.
  - The step to enable the output pin functions should only be done after the SSC mode is enabled with CCR.MODE, to avoided unintended spikes on the output.

An initialization code example is given in ***Chapter 18.4.4.4***.

Note: In SSC slave mode, the baud rate generator and the slave select generation are not needed and can be switched off. All related bit fields (e.g. FDR.DM, PCR.MSLSEN, etc.) can be programmed to 0.

18.4.4.1 Protocol Interrupts

The following protocol-related events generated in SSC mode and can lead to a protocol interrupt. They are related to the start and the end of a data frame. After the start of a data frame a new setting could be programmed for the next data frame and after the end of a data frame the SSC connections to pins can be changed.

Please note that the bits in register PSR are not all automatically cleared by hardware and have to be cleared by software in order to monitor new incoming events.

Table 202 SSC slave mode protocol interrupt events

Events	Event flag	Description	Flag clear	Interrupt enable
DX2T interrupt	PSR.DX2TEV	Set after an activation of the trigger signal DX2T. This event monitors edges of the input signal of the DX2 stage (although this signal is not used as slave select input for data transfers). The actual state of the selected input signal can be read out at PSR.DX2S to take appropriate actions when this interrupt has been detected.	PSCR.CST3	PCR.DX2TIEN
Parity error interrupt	PSR.PARERR	Set if there is a mismatch between the received parity bit (in RBUFSR.PAR) and the calculated parity bit, of the data frame.	PSCR.CST4	PCR.PARIEN

18.4.4.2 End-of-Frame Control

In slave mode, the following possibilities exist to determine the frame length. The slave device either has to refer to an external slave select signal, or to the number of received data bits.

Frame length known in advance by the slave device, no slave select

In this case bit field SCTR.FLE can be programmed to the known value (if it does not exceed 63 bits). A currently running data word transfer is considered as finished if the programmed frame length is reached.

Frame length not known by the slave, no slave select

In this case, the slave device's software has to decide on data word base if a frame is finished. Bit field SCTR.FLE can be either programmed to the word length SCTR.WLE, or to its maximum value to disable the slave internal frame length evaluation by counting received bits.

Slave device addressed via slave select signal SELIN

If the slave device is addressed by a slave select signal delivered by the communication master, the frame start and end information are given by this signal. In this case, bit field SCTR.FLE should be programmed to its maximum value to disable the slave internal frame length evaluation.

18.4.4.3 Data Flow Handling

To prepare the SSC slave for data transfer, the first data word is written to one of the transmit buffer input locations (TBUFx) by software. If the transmit FIFO is used, one of the transmit FIFO buffer input locations (INx) should be used instead of TBUFx.

Then slave then waits for the SSC master to initiate the data transfer. Once the data transfer is started, the data word will then be updated to the transmit shift register. This is indicated by a transmit buffer interrupt event (PSR.TBIF = 1).

In the same clock cycle that the first data bit is placed onto the output line MTSR but in the opposite clock edge, the first data bit on the input line MRST is latched and shifted into the available receive shift register. This is indicated by a receive start interrupt event (PSR.RSIF = 1). The receive start interrupt event can be used to indicate that the next data word can now be loaded to TBUF.

For each data word, the start of transmission of the last data bit is indicated by a transmit shift interrupt event (PSR.TSIF = 1).

When the number of bits corresponding to the data word length is received, the contents of the receive shift register are transferred to the corresponding receive buffer (RBUF0 or RBUF1). This is indicated by an alternate receive interrupt event (PSR.AIF) if the received word is the first word of the frame, or by a receive interrupt event (PSR.RIF) if the received word represents subsequent words of the frame.

Figure 96 shows the simplified data transmission and reception flows with TBUFx and RBUF. For examples with FIFO buffer, refer to ***Chapter 18.2.8.4*** and ***Chapter 18.2.8.7***.

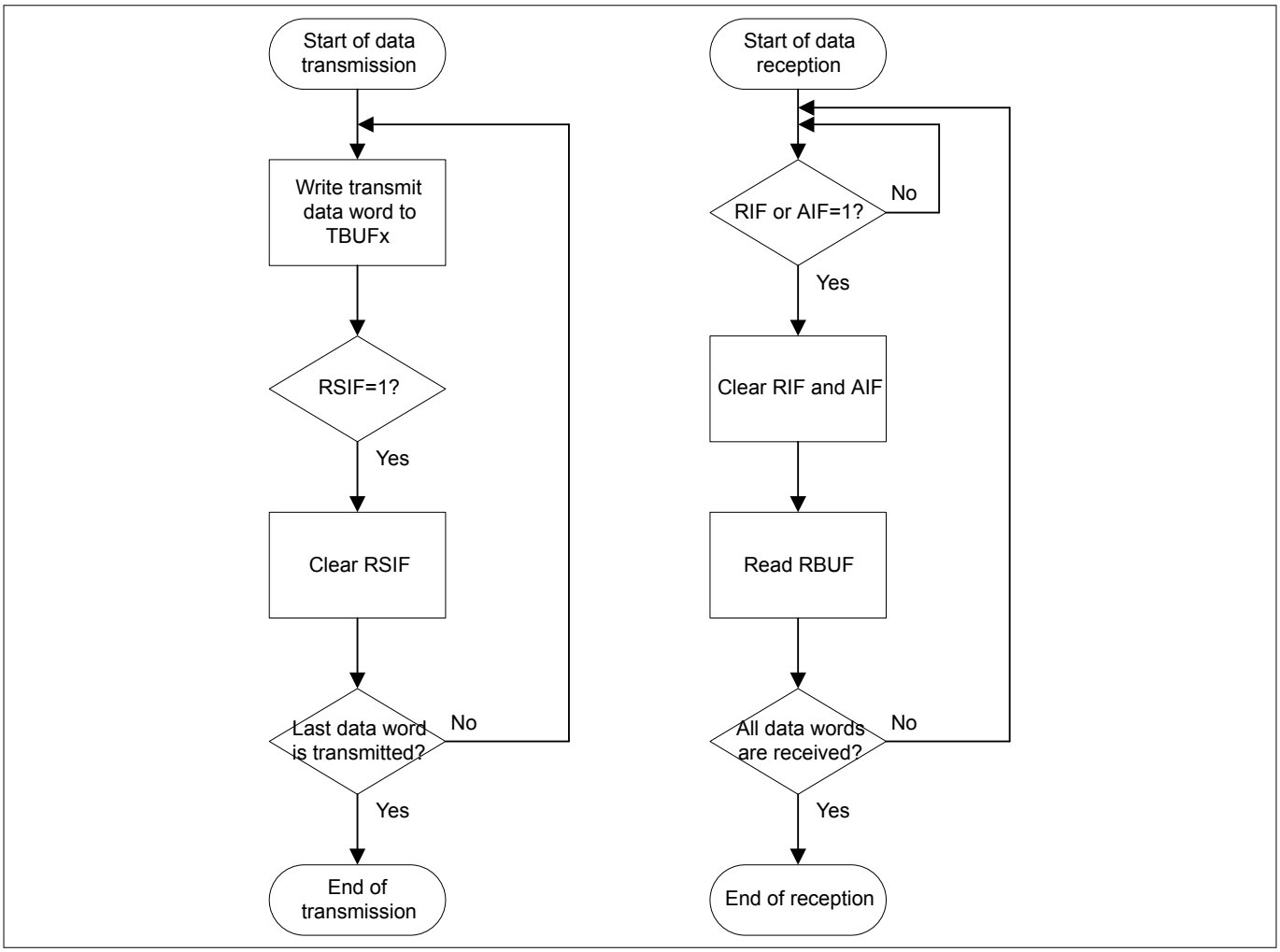


Figure 96 Simplified Data Transmission and Reception Flow

Figure 97 shows the interrupt events during a SSC slave mode data transfer.

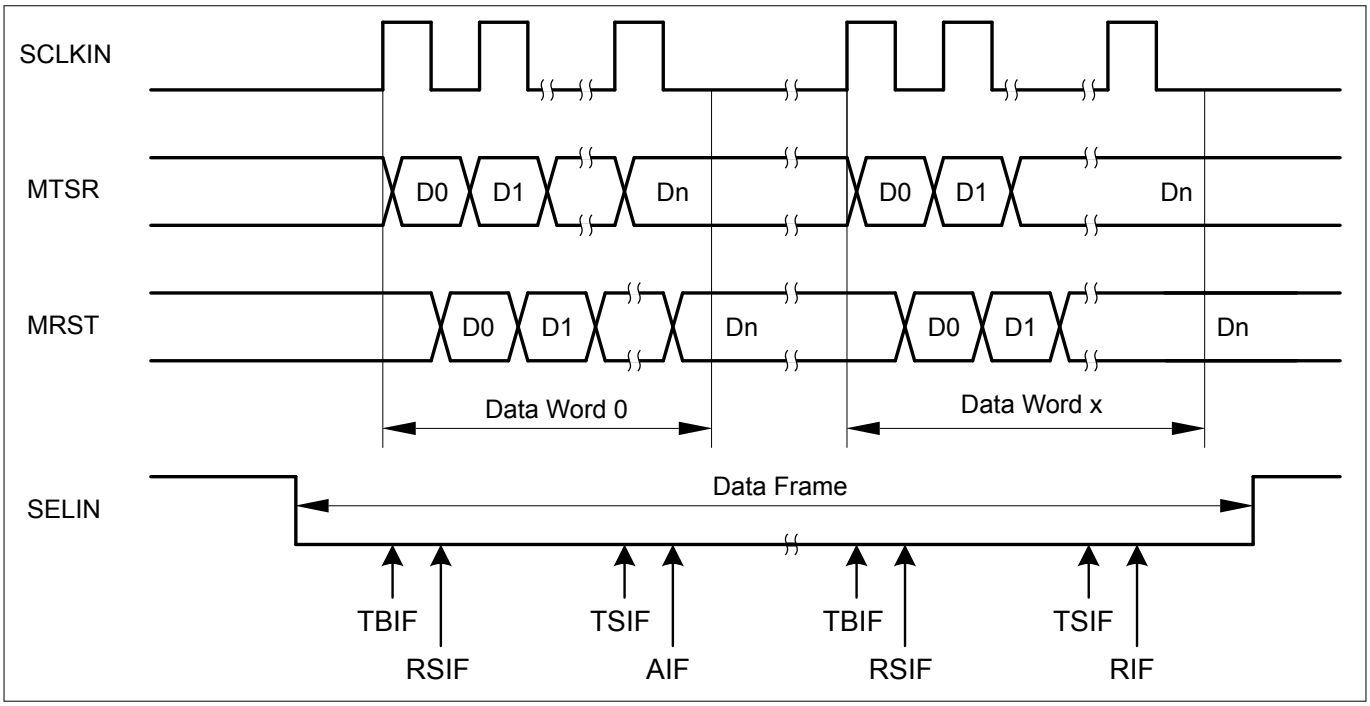


Figure 97 Interrupt Events on Data Transfer

18.4.4.4 Initialization Code Example

The following code example implements a function to initialize a USIC channel for SSC slave mode data transfers:

```
void USIC0_CH1_SSC_SlaveMode_Init(void)
{
/// ----------------------------------------------------------------------
/// 1. Enable USIC0 channel 1
/// ----------------------------------------------------------------------
    //                    BPMODEN     MODEN
    USIC0_CH1->KSCFG |= (1 << 1) | (1 << 0);

/// ----------------------------------------------------------------------
/// 2. Configure input stages
///    - Select inputs DX0D, DX1B and DX2B
///    - Derive all input signals directly from input pins
/// ----------------------------------------------------------------------
    //                    INSW       DSEL
    USIC0_CH1->DX0CR = (1 << 4) | (3 << 0);
    //                    INSW       DSEL
    USIC0_CH1->DX1CR = (1 << 4) | (1 << 0);
    //                    DPOL       INSW      DSEL
    USIC0_CH1->DX2CR = (1 << 8) | (1 << 4) |(1 << 0);

/// ----------------------------------------------------------------------
/// 3. Configure data format
///    - Data word = data frame = 15 bits
///    - Data transfer allowed with passive level = 1 and MSB first
/// ----------------------------------------------------------------------
    //                     WLE        FLE       TRM       PDL     SDIR
    USIC0_CH1->SCTR = (15 << 24)|(15 << 16)|(1 << 8)|(1 << 1)|(1 << 0);

/// ----------------------------------------------------------------------
/// 4. Configure data transfer parameters
///    - Single shot transmission of data word when a valid word
///      is available
/// ----------------------------------------------------------------------
    //                   TDEN       TDSSM
    USIC0_CH1->TCSR = (1 << 10) | (1 << 8);

/// ----------------------------------------------------------------------
/// 5. Enable SSC protocol
/// ----------------------------------------------------------------------
    //                  MODE
    USIC0_CH1->CCR = (1 << 0);

/// ----------------------------------------------------------------------
/// 6. Configure SSC output function pins
///    - Assume P0.6 ALT7 function is assigned to DOUT0
/// ----------------------------------------------------------------------
    //                   PC6
```

```
    PORT0->IOCR4 |= (0x27 << 18);
}
```

18.4.5 Multi-IO SSC Protocols

Multi-IO SSC protocols, or specifically Dual-SSC and Quad-SSC, are extensions of the standard SSC protocol to double and quadruple the effective data transfer rates. This is achieved by transmitting and receiving data through two or four IO lines in parallel, in a half-duplex configuration.

Figure 98 shows the connections between a SSC master and a SSC slave, in Quad-SSC configurations. For Dual-SSC, the DX4/DOUT2 and DX5/DOUT3 pins are not used.

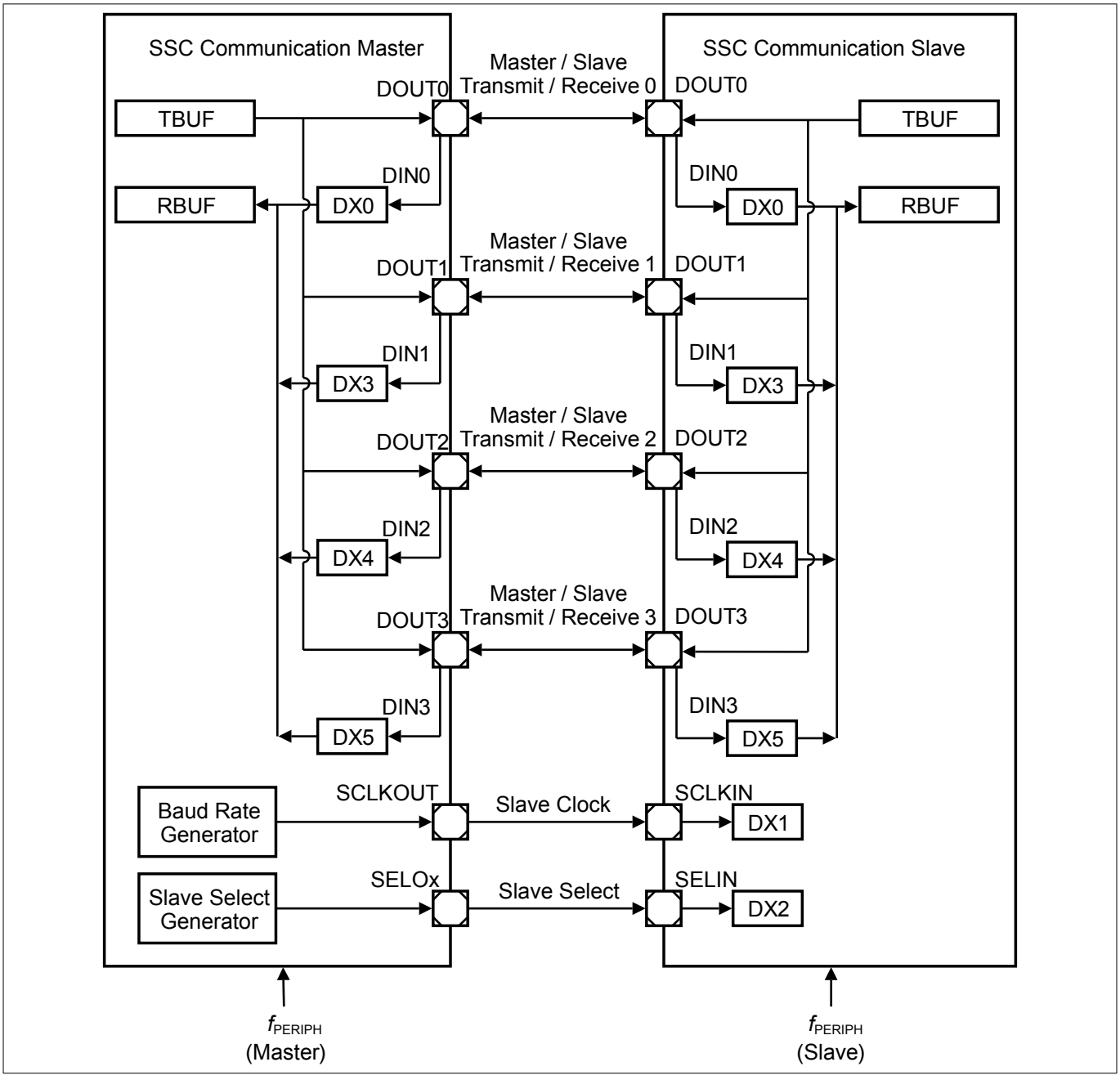


Figure 98 Quad-SSC Signal Connections

18.4.5.1 Operating the SSC in Multi-IO Modes

In order to operate the multi-IO SSC in either master or slave mode, the following steps have to be taken in addition to the USIC channel initialization steps outlined in ***Chapter 18.4.3*** and ***Chapter 18.4.4***:

- Enable hardware port control
  - Enable the dedicated hardware port interface to the DX0/DOUT0 and DX3/DOUT1 pins (dual-SSC) and additionally, DX4/DOUT2 and DX5/DOUT3 pins (Quad-SSC) by configuring the bit field CCR.HPCEN.
- Enable dynamic update of transfer parameters with TCI
  - Enable the dynamic control of both the shift mode and pin direction during data transfers, i.e. SCTR.DSM and SCTR.HPCDIR bit fields are updated with TCI.
  - This is done by setting the bit TCSR.HPCMD to 1.

18.4.5.2 Quad-SSC Example

Figure 99 shows an example of a Quad-SSC protocol, which requires the master SSC to first transmit a command byte (to request a quad output read from the slave) and a dummy byte through a single data line. At the end of the dummy byte, both master and slave SSC switches to quad data lines, and with the roles of transmitter and receiver reversed. The master SSC then receives the data four bits per shift clock from the slave through the MRST[3:0] lines.

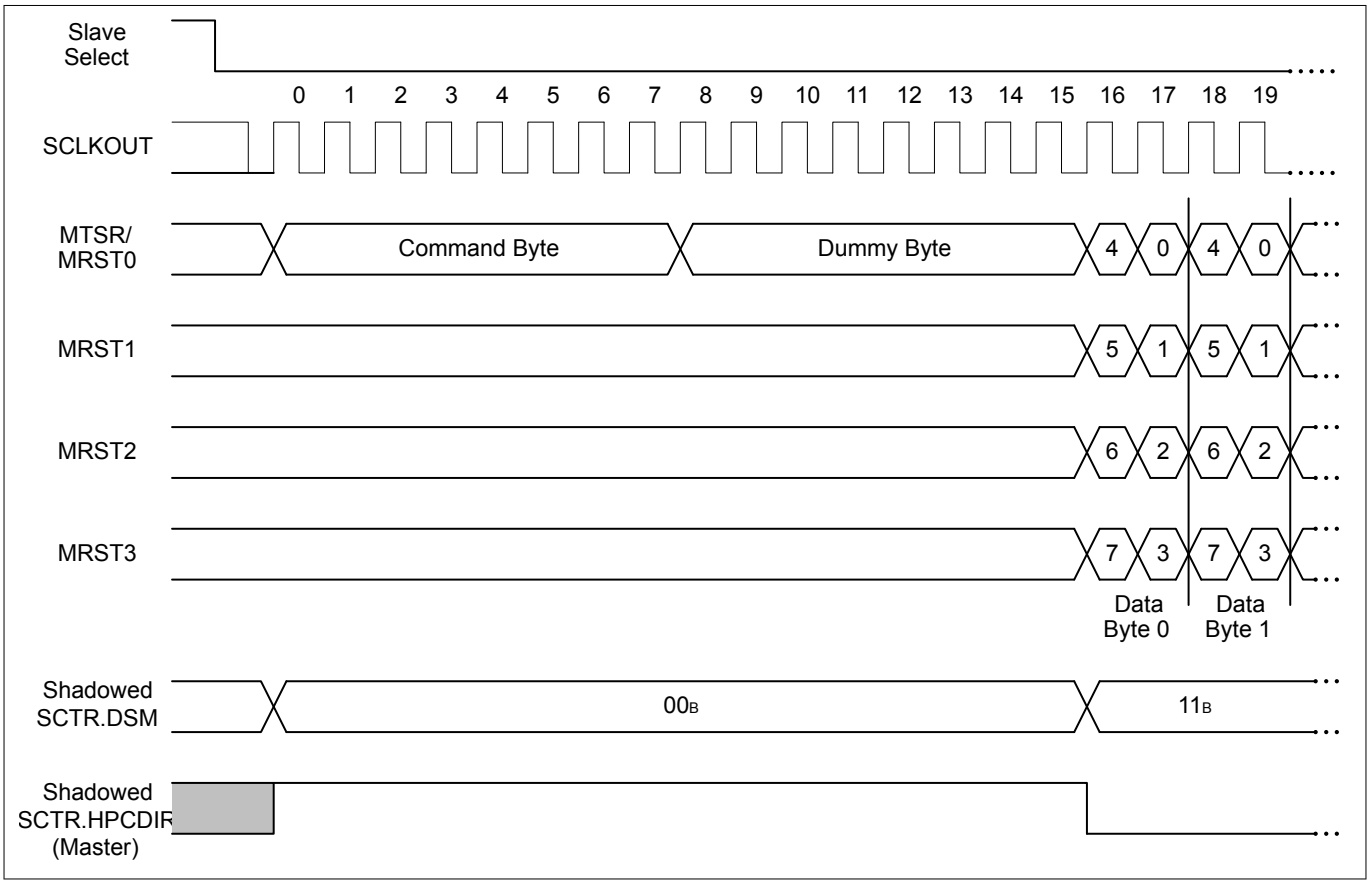


Figure 99 Quad-SSC Example

Initialization

The following code modifications can be made to the initialization code examples in ***Chapter 18.4.3.8*** or ***Chapter 18.4.4.4*** to configure the USIC channel as a Quad-SSC master or slave:

```
/// ----------------------------------------------------------
/// 5. Configure data transfer parameters
///    - Single shot transmission of data word when a valid word
///      is available
///    - Hardware port control TCI mode is enabled
/// ----------------------------------------------------------
    //                    TDEN       TDSSM      HPCMD
    USIC0_CH1->TCSR = (1 << 10) | (1 << 8) | (1 << 6);

/// ----------------------------------------------------------
/// 7. Enable SSC protocol and hardware port control
/// ----------------------------------------------------------
    //                   HPCEN      MODE
    USIC0_CH1->CCR = (3 << 6) | (1 << 0);
```

Data Flow

To start the data transfer:

- For the master SSC, write the command and dummy bytes into TBUF04 to select a single data line in output mode and initiate the data transfer.
- For the slave SSC, dummy data can be preloaded into TBUF00 to select a single data line in input mode.

To switch to quad data lines and pin direction:

- For the master SSC, write subsequent dummy data to TBUF03 to select quad data lines in input mode to read in valid slave data.
- For the slave SSC, write valid data to TBUF07 for transmission through quad data lines in output mode.

18.4.6 SSC Timing Considerations

The input and output signals have to respect certain timings in order to ensure correct data reception and transmission. In addition to module internal timings (due to input filters, reaction times on events, etc.), also the timings from the input pin via the input stage (T_{in}) to the module and from the module via the output driver stage to the pin (T_{out}), as well as the signal propagation on the wires (T_{prop}) have to be taken into account.

Please note that there might be additional delays in the DXn input stages, because the digital filter and the synchronization stages lead to systematic delays, that have to be considered if these functions are used.

18.4.6.1 Closed-loop Delay

A system-inherent limiting factor for the baud rate of an SSC connection is the closed-loop delay. In a typical application setup, a communication master device is connected to a slave device in full-duplex mode with independent lines for transmit and receive data. In a general case, all transmitters refer to one shift clock edge for transmission and all receivers refer to the other shift clock edge for reception. The master device's SSC module sends out the transmit data, the shift clock and optionally the slave select signal. Therefore, the baud rate generation (BRG) and slave select generation (SSG) are part of the master device. The frame control is similar for SSC modules in master and slave mode, the main difference is the fact which module generates the shift clock and optionally, the slave select signals.

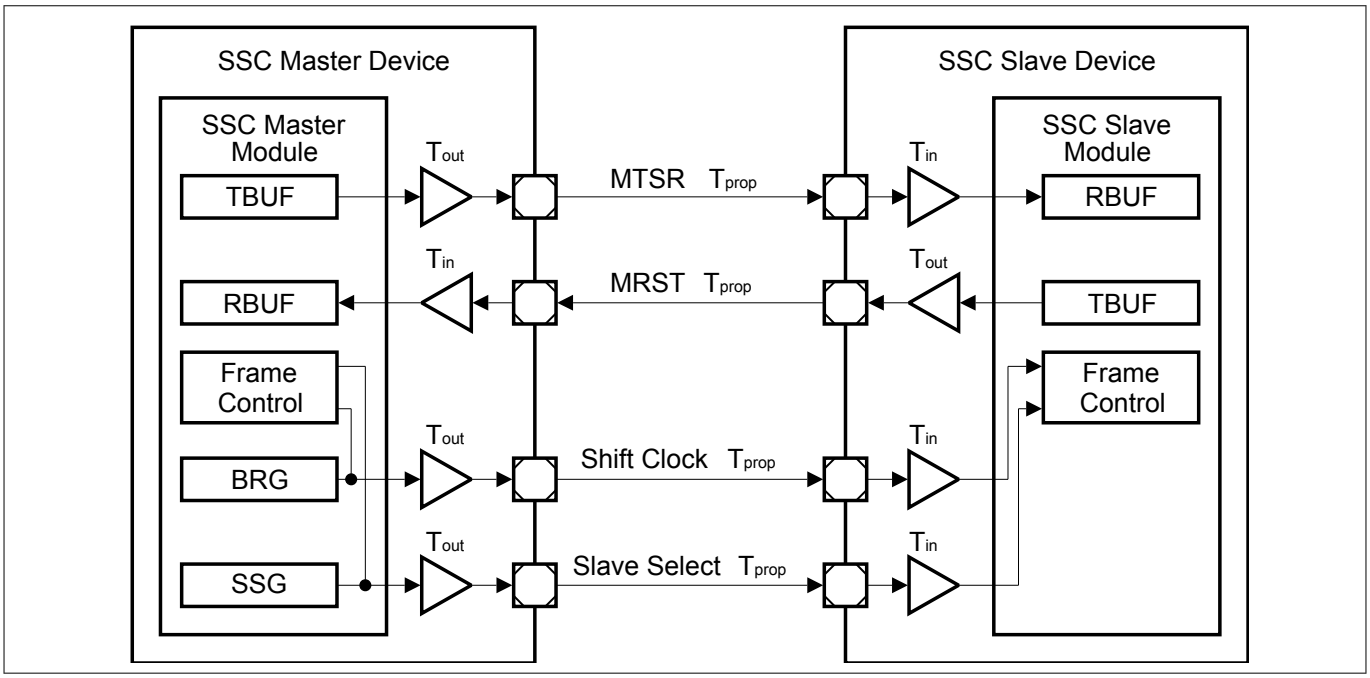


Figure 100 SSC Closed-loop Delay

The signal path between the SSC modules of the master and the slave device includes the master's output driver, the wiring to the slave device and the slave device's input stage. With the received shift clock edges, the slave device receives the master's transmit data and transmits its own data back to the master device, passing by a similar signal path in the other direction. The master module receives the slave's transmit data related to its internal shift clock edges. In order to ensure correct data reception in the master device, the slave's transmit data has to be stable (respecting setup and hold times) as master receive data with the next shift clock edge of the master (generally 1/2 shift clock period). To avoid data corruption, the accumulated delays of the input and output stages, the signal propagation on the wiring and the reaction times of the transmitter/receiver have to be carefully considered, especially at high baud rates. In the given example, the time between the generation of the shift clock signal and the evaluation of the receive data by the master SSC module is given by the sum of $T_{out_master} + 2 \times T_{prop} + T_{in_slave} + T_{out_slave} + T_{in_master}$ + module reaction times + input setup times. The input path is characterized by an input delay depending mainly on the input stage characteristics of the pads. The output path delay is determined by the output driver delay and its slew rate, the external load and current capability of the driver. The device specific values for the input/output driver are given in the Data Sheet.

Figure 101 describes graphically the closed-loop delay and the effect of two delay compensation options discussed in ***Chapter 18.4.6.2*** and ***Chapter 18.4.6.3***.

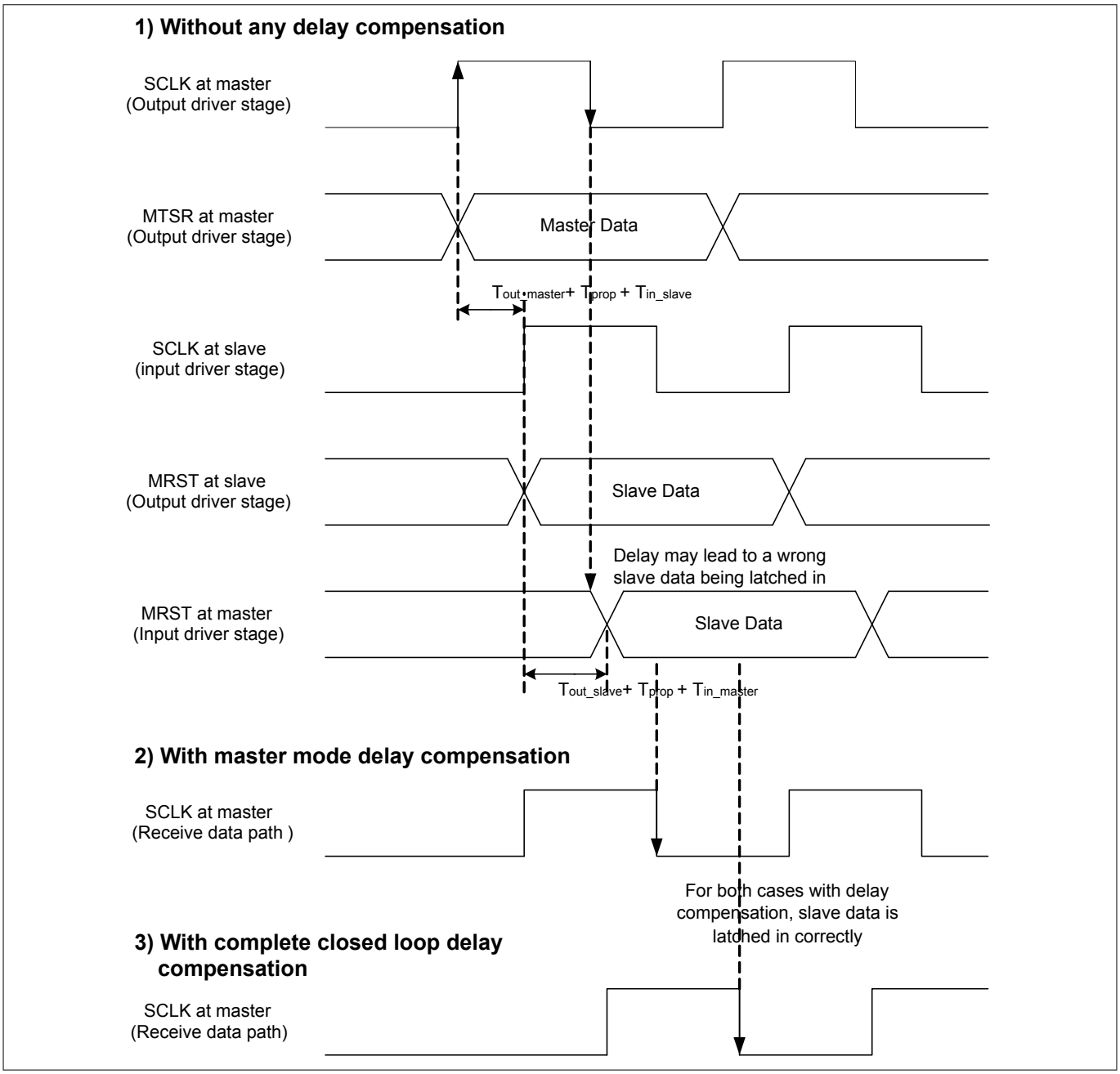


Figure 101 SSC Closed-loop Delay Timing Waveform

18.4.6.2 Delay Compensation in Master Mode

A higher baud rate can be reached by delay compensation in master mode. This compensation is possible if (at least) the shift clock pin is bidirectional.

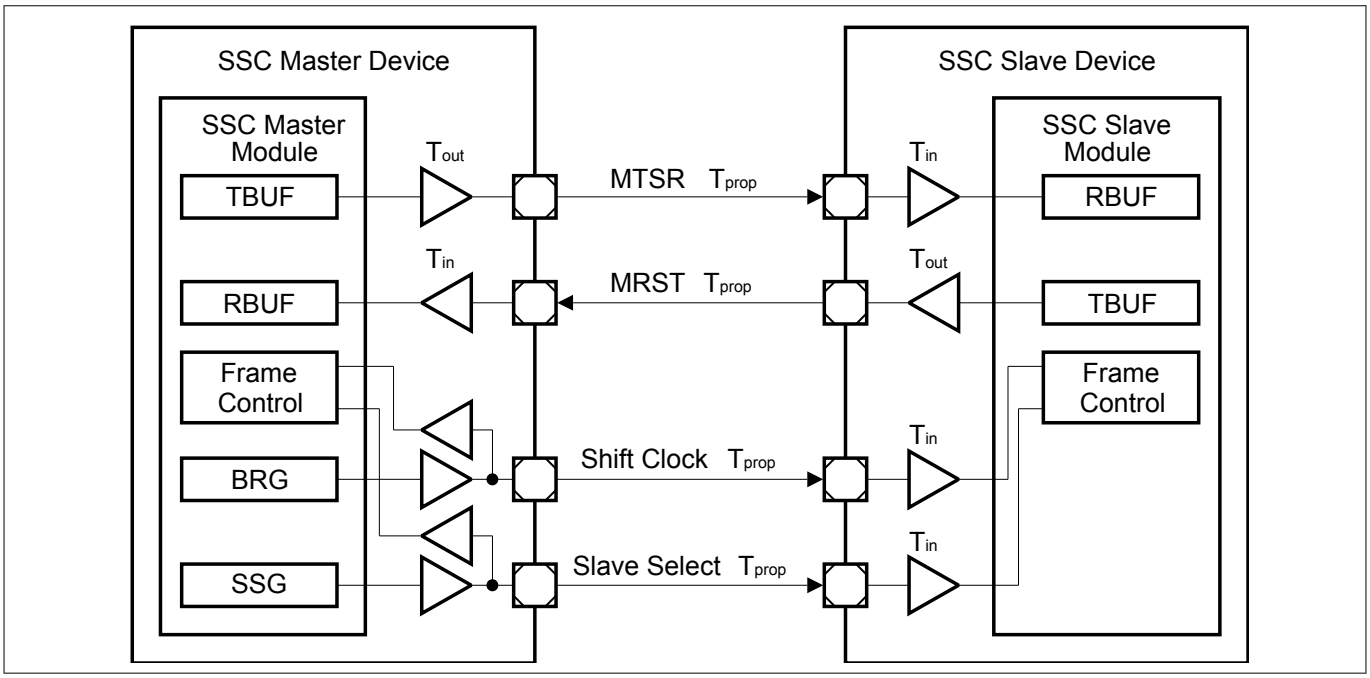


Figure 102 SSC Master Mode with Delay Compensation

If the receive shift clock signal in master mode is directly taken from the input function in parallel to the output signal, the output delay of the master device's shift clock output is compensated and only the difference between the input delays of the master and the slave devices have to be taken into account instead of the complete master's output delay and the slave's input delay of the shift clock path. The delay compensation is enabled with DX1CR.DCEN = 1 while DX1CR.INSW = 0 (transmit shift clock is taken from the baud-rate generator).

In the given example, the time between the evaluation of the shift clock signal and the receive data by the master SSC module is reduced by $T_{in_master} + T_{out_master}$.

Although being a master mode, the shift clock input and optionally the slave select signal are not directly connected internally to the data shift unit, but are taken as external signals from input pins. The delay compensation does not lead to additional pins for the SSC communication if the shift clock output pin (slave select output pin, respectively) is/are bidirectional. In this case, the input signal is decoupled from other internal signals, because it is related to the signal level at the pin itself.

18.4.6.3 Complete Closed-loop Delay Compensation

Alternatively, the complete closed-loop delay can be compensated by using one additional pin on both the SSC master and slave devices for the SSC communication.

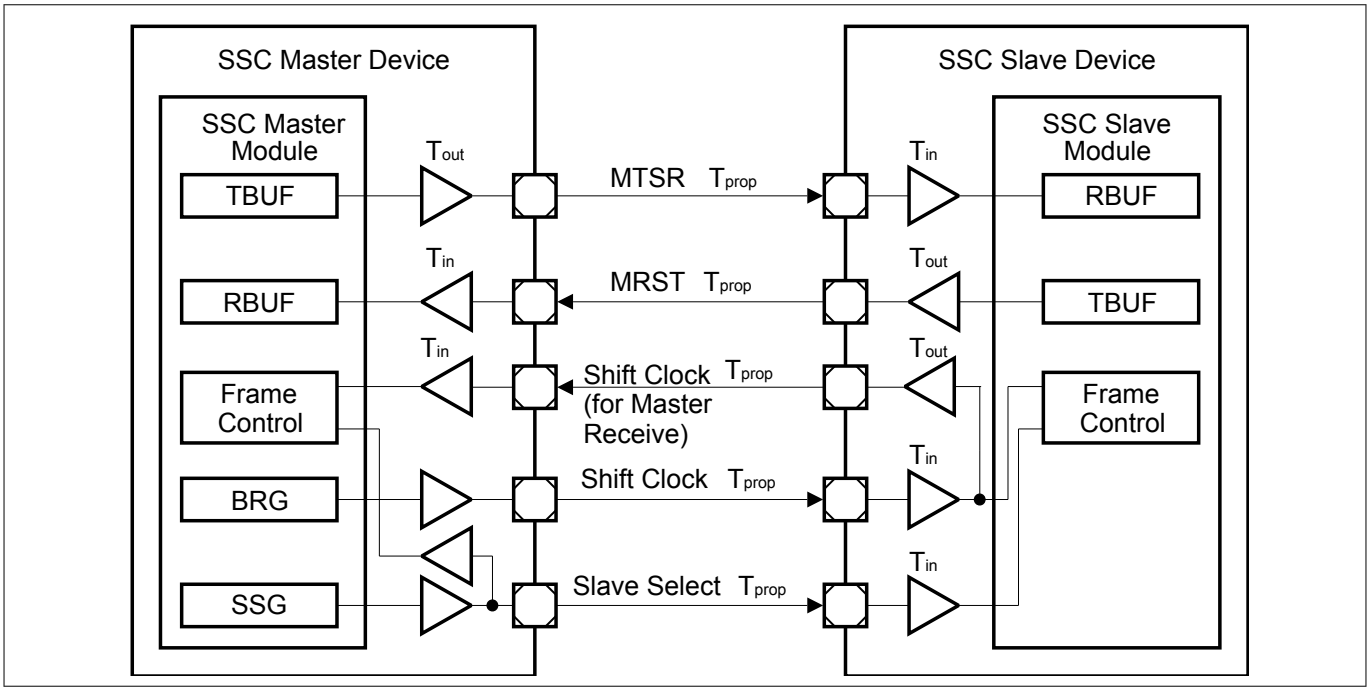


Figure 103 SSC Complete Closed-loop Delay Compensation

The principle behind this delay compensation method is to have the slave feedback the shift clock back to the master, which uses it as the receive shift clock. By going through a complete closed-loop signal path, the receive shift clock is thus fully compensated.

The slave has to setup the SCLKOUT pin function to output the shift clock by setting the bit BRG.SCLKOSEL to 1, while the master has to setup the DX1 pin function to receive the shift clock from the slave and enable the delay compensation with DX1CR.DCEN = 1 and DX1CR.INSW = 0.

18.5 Inter-IC Bus Protocol (IIC)

The IIC protocol of the USIC refers to the IIC bus specification *[9]*.

Contrary to that specification, the USIC device assumes rise/fall times of the bus signals of max. 300 ns in all modes. Please refer to the pad characteristics in the AC/DC chapter for the driver capability. CBUS mode and HS mode are not supported.

The IIC mode is selected by CCR.MODE = 0100_B.

18.5.1 Introduction

USIC IIC Features:

- Two-wire interface, with one line for shift clock transfer and synchronization (shift clock SCL), the other one for the data transfer (shift data SDA)
- Communication in standard mode (100 kBit/s) or in fast mode (up to 400 kBit/s)
- Support of 7-bit addressing, as well as 10-bit addressing
- Master mode operation,
  where the IIC controls the bus transactions and provides the clock signal.
- Slave mode operation,
  where an external master controls the bus transactions and provides the clock signal.
- Multi-master mode operation,

where several masters can be connected to the bus and bus arbitration can take place, i.e. the IIC module can be master or slave. The master/slave operation of an IIC bus participant can change from frame to frame.

- Efficient frame handling (low software effort)
- Powerful interrupt handling due to multitude of indication flags
- Compensation support for input delays

18.5.1.1 Signal Description

An IIC connection is characterized by two wires (SDA and SCL).

The output drivers for these signals must have open-drain characteristics to allow the wired-AND connection of all SDA lines together and all SCL lines together to form the IIC bus system.

Due to this structure, a high level driven by an output stage does not necessarily lead immediately to a high level at the corresponding input.

Therefore, each SDA or SCL connection has to be input and output at the same time, because the input function always monitors the level of the signal, also while sending.

- Shift data SDA: input handled by DX0 stage, output signal DOUT0
- Shift clock SCL: input handled by DX1 stage, output signal SCLKOUT

Figure 104 shows a connection of two IIC bus participants (modules IIC A and IIC B) using the USIC.

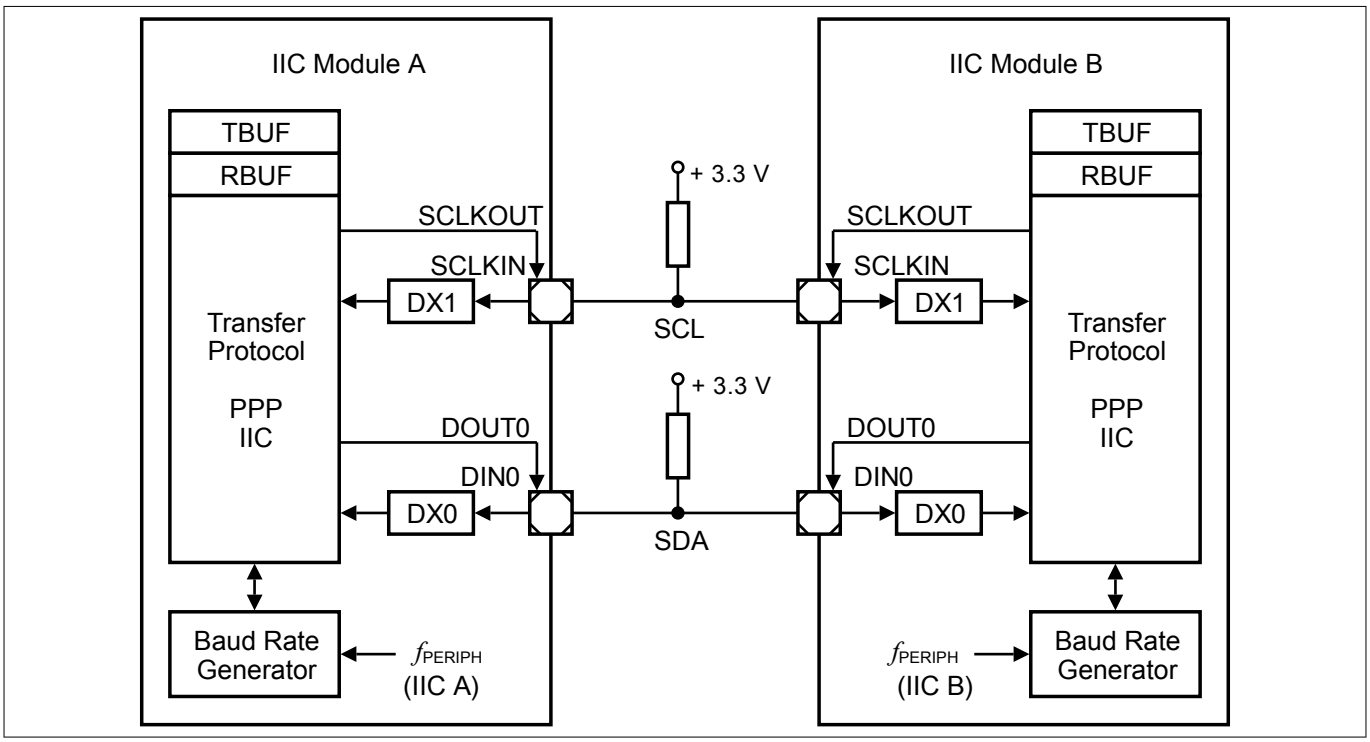


Figure 104 IIC Signal Connections

18.5.1.2 Symbols

A symbol is a sequence of edges on the lines SDA and SCL. Symbols contain 10 or 25 time quanta t_q, depending on the selected baud rate.

The baud rate generator determines the length of the time quanta t_q, the sequence of edges in a symbol is handled by the IIC protocol pre-processor, and the sequence of symbols can be programmed by the user according to the application needs.

Table 203 IIC Symbol Definition

Symbol	Definition
Bus idle	SDA and SCL are high. No data transfer takes place currently.
Data bit	SDA stable during the high phase of SCL. SDA then represents the transferred bit value. There is one clock pulse on SCL for each transferred bit of data. During data transfers SDA may only change while SCL is low.
Start	Signal SDA being high followed by a falling edge of SDA while SCL is high indicates a start condition. This start condition initiates a data transfer over the IIC bus after the bus has been idle.
Repeated start	This start condition initiates a data transfer over the bus after a data symbol when the bus has not been idle. Therefore, SDA is set high and SCL low, followed by a start symbol.
Stop	A rising edge on SDA while SCL is high indicates a stop condition. This stop condition terminates a data transfer to release the bus to idle state. Between a start condition and a stop condition an arbitrary number of bytes may be transferred.

18.5.1.3 Frame Format

Data is transferred by the 2-line IIC bus (SDA, SCL) using a protocol that ensures reliable and efficient transfers. The sender of a (data) byte receives and checks the value of the following acknowledge field. The IIC being a wired-AND bus system, a 0 of at least one device leads to a 0 on the bus, which is received by all devices.

A data word consists of 8 data bit symbols for the data value, followed by another data bit symbol for the acknowledge bit. The data word can be interpreted as address information (after a start symbol) or as transferred data (after the address).

In order to be able to receive an acknowledge signal, the sender of the data bits has to release the SDA line by sending a 1 as acknowledge value. Depending on the internal state of the receiver, the acknowledge bit is either sent active or passive.

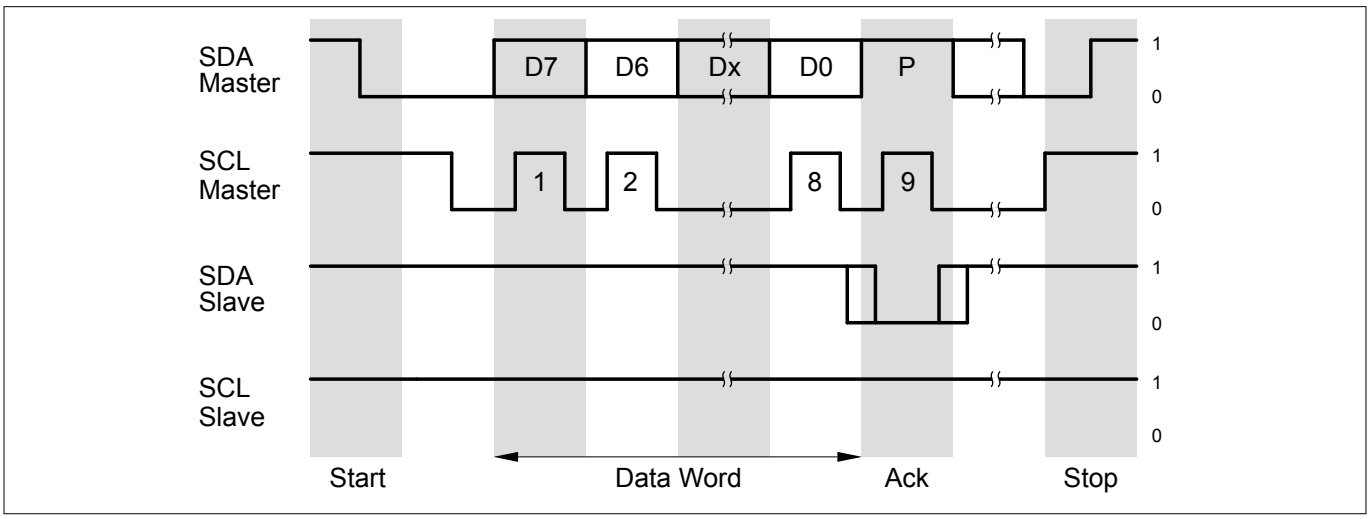


Figure 105 IIC Frame Example (simplified)

18.5.2 Symbol Timing

The symbol timing of the IIC is determined by the master generating the shift clock line SCL. It is different in each of the modes.

- 100 kBaud standard mode (PCR.STIM = 0):
  The symbol timing is based on 10 time quanta t_q per symbol. A minimum module clock frequency f_{PERIPH} = 2 MHz is required.
- 400 kBaud fast mode (PCR.STIM = 1):
  The symbol timing is based on 25 time quanta t_q per symbol. A minimum module clock frequency f_{PERIPH} = 10 MHz is required.
  Additionally, if the digital filter stage should be used to eliminate spikes up to 50 ns, a filter frequency of 20 MHz is necessary.

To respect the specified SDA hold time of 300 ns for standard mode and fast mode after a falling edge of signal SCL, a hold delay t_{HDEL} has been introduced. It also prevents an erroneous detection of a start or a stop condition.

The length of this delay can be programmed by bit field PCR.HDEL. Taking into account the input sampling and output update, bit field HDEL can be programmed according to:

$$HDEL \geq 300\,ns \times f_{PPP} - \left(3 \times \frac{f_{PPP}}{f_{PERIPH}}\right) + 1 \quad \text{with digital filter and HDELmin = 2}$$

$$HDEL \geq 300\,ns \times f_{PPP} - \left(3 \times \frac{f_{PPP}}{f_{PERIPH}}\right) + 2 \quad \text{without digital filter and HDELmin = 1}$$

Equation 20

For BRG.CLKSEL = 00_B and BRG.PPPEN = 0, $f_{PPP} = f_{FD}$, which is the output frequency of the fractional divider (see ***Chapter 18.2.4.1***).

If the digital input filter is used, HDEL compensates the filter delay of 2 filter periods (f_{PPP} should be used) in case of a spike on the input signal. This ensures that a data bit on the SDA line changing just before the rising edge or behind the falling edge of SCL will not be treated as a start or stop condition.

18.5.2.1 Start Symbol

Figure 106 shows the general start symbol timing.

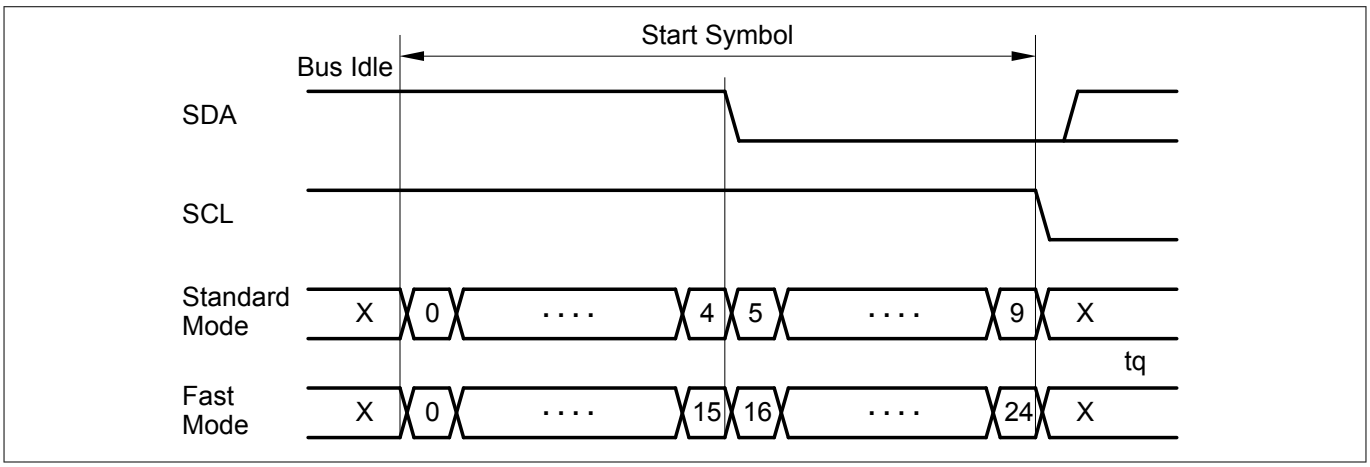


Figure 106 Start Symbol Timing

18.5.2.2 Repeated Start Symbol

During the first part of a repeated start symbol, an SCL low value is driven for the specified number of time quanta. Then a high value is output. After the detection of a rising edge at the SCL input, a normal start symbol is generated, as shown in ***Figure 107***.

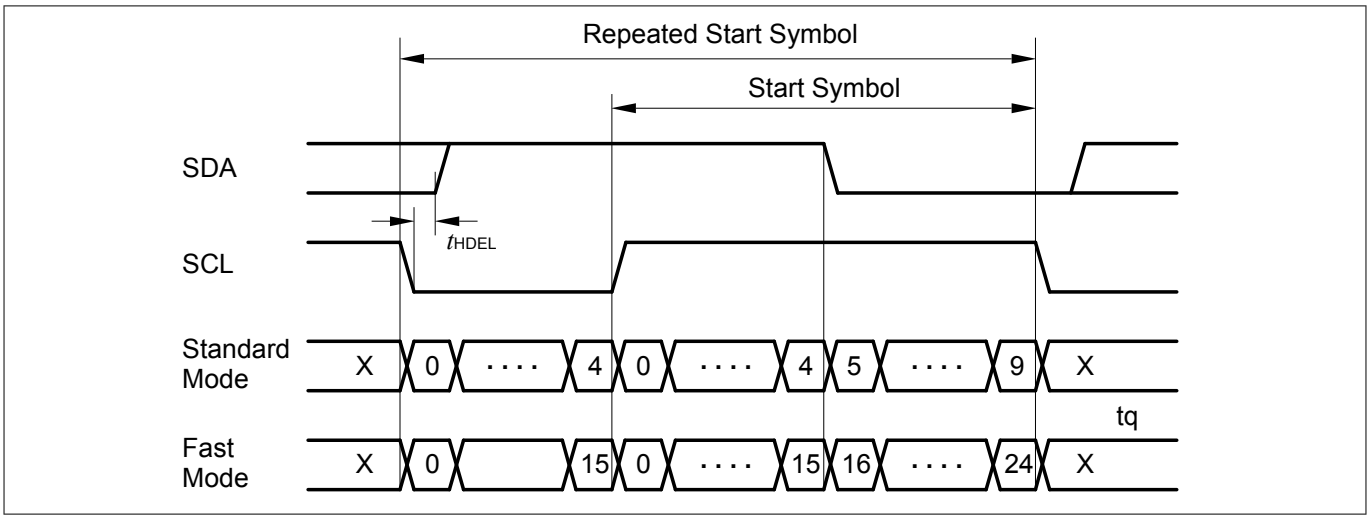


Figure 107 Repeated Start Symbol Timing

18.5.2.3 Stop Symbol

Figure 108 shows the stop symbol timing.

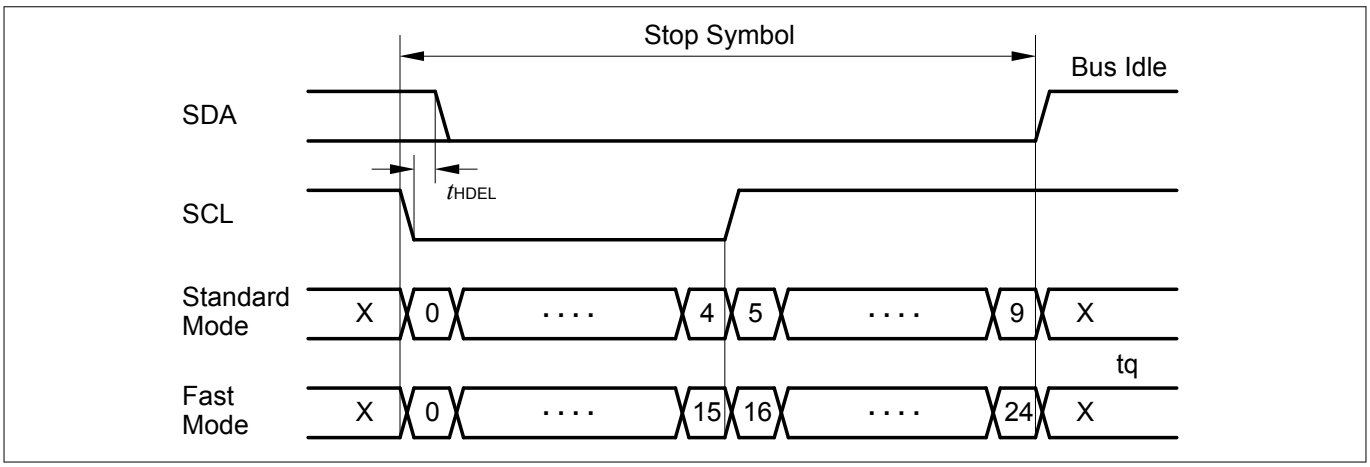


Figure 108 Stop Symbol Timing

18.5.2.4 Data Bit Symbol

Figure 109 shows the general data bit symbol timing.

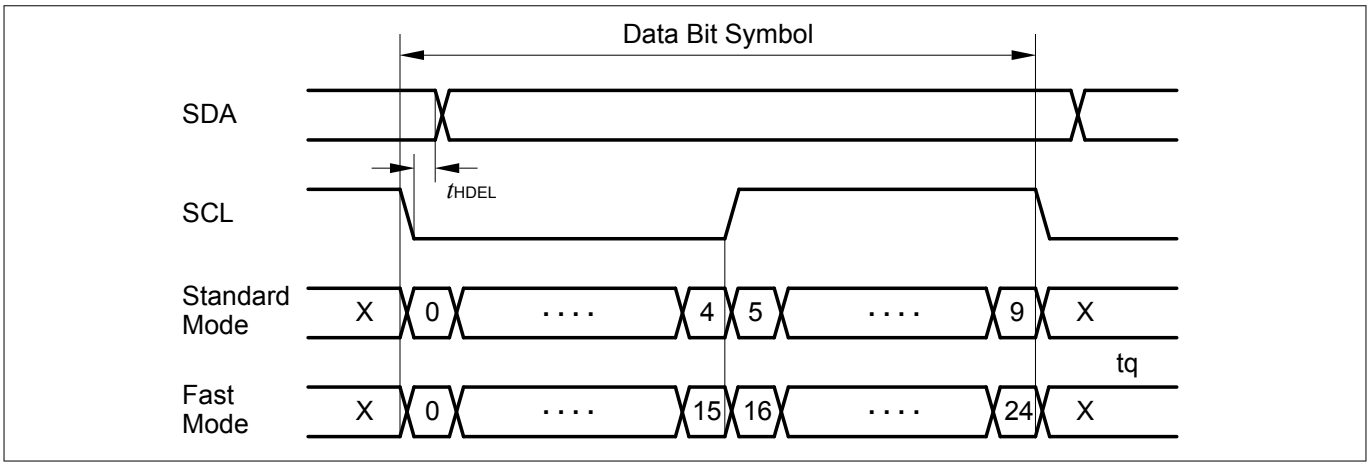


Figure 109 Data Bit Symbol

Output SDA changes after the time t_{HDEL} defined by PCR.HDEL has elapsed if a falling edge is detected at the SCL input to respect the SDA hold time. The value of PCR.HDEL allows compensation of the delay of the SCL input path (sampling, filtering).

In the case of an acknowledge transmission, the USIC IIC waits for the receiver indicating that a complete byte has been received. This adds an additional delay of 3 periods of f_{PERIPH} to the path. The minimum module input frequency has to be selected properly to ensure the SDA setup time to SCL rising edge.

18.5.3 Operating the IIC

In order to operate the IIC protocol, the USIC channel has to be first initialized.

It is recommended to configure all parameters of the IIC that do not change during run time while CCR.MODE = 0000_B, except stated otherwise.

The main initialization steps are outlined below:

- Enable USIC channel
  - Enable the module by writing 1s to MODEN and BPMODEN bits in KSCFG register.
- Configure baud rate generator
  - Select either fractional divider mode or normal divider mode with FDR.DM bit.
  - Configure the bit timing and baud rate setting through register bit fields BRG.PCTQ, BRG.DCTQ, BRG.PDIV and FDR.STEP, while BRG.SCLKCFG = 00_B.
  - There could be an uncertainty in the SCL high phase timing of maximum $1/f_{PPP}$ if another IIC participant lengthens the SCL low phase on the bus.
- Configure input pins
  - Establish a connection of input stage DX0 to the shift data pin SDA (signal DIN0) selected by DX0CR.DSEL bit field, and with both bit DX0CR.INSW and bit DX0CR.DPOL = 0.
  - Similarly, establish a connection of input stage DX1 to the shift clock line SCL (signal SCLKIN) selected by DX1CR.DSEL bit field, and with both bit DX1CR.INSW and DX1CR.DPOL = 0.
  - If the digital input filters are enabled in the DX0/1 stages, their delays have to be taken into account for correct calculation of the signal timings.
- Configure data format
  - Configure the data format for 8 data bits (SCTR.WLE = 7), unlimited data flow (SCTR.FLE = $3F_H$) and MSB shifted first (SCTR.SDIR = 1).

  - Select the passive output level to be high (SCTR.PDL = 1) and for the data output to be without inversion (SCTR.DOCFG = 00_B).
  - Write SCTR.TRM = 11_B to enable IIC data transfers.
- Configure data transfer parameters
  - Write TCSR.TDSSM = 1 and TCSR.TDEN = 01_B to enable data transmission in single shot mode.
- Configure protocol control parameters
  - Select 25 time quanta per symbol for IIC fast mode (PCR.STIM = 1).
  - Configure the hardware delay (PCR.HDEL = 7) to ensure the SDA hold time after a falling SCL edge.
- Select IIC protocol
  - Enable IIC mode with CCR.MODE = 0100_B.
- Configure output pins
  - Select the transmit data SDA output pin (signal DOUT0) to be the same pin used for the SDA input.
  - Similarly, configure the shift clock SCL output pin (signal SCLKOUT) to be the same pin used for the SCL input.
  - The pins used for SDA and SCL have to be set to open-drain mode to support the wired-AND structure of the IIC bus lines.
  - Selection of the output pins and their behaviour are done through the respective pins' port control register Pn_IOCR0/4/8/12. Refer to the port chapter.
  - The step to enable the output pin functions should only be done after the IIC mode is enabled with CCR.MODE, to avoided unintended spikes on the output.

An initialization code example is given in ***Chapter 18.5.3.12***.

18.5.3.1 Baud Rate Generation

The baud rate f_{IIC} in IIC mode depends on the number of time quanta per bit time and their timing. The bits in register BRG define the baud rate setting:

- BRG.CTQSEL
  to define the input frequency f_{CTQIN} for the time quanta generation
- BRG.PCTQ
  to define the length of a time quantum (division of f_{CTQIN} by 1, 2, 3, or 4)
- BRG.DCTQ
  to define the number of time quanta per bit time (DCTQ = 9_H for standard mode or DCTQ = 18_H for fast mode

The baud rate is given by:

$$f_{IIC} = f_{CTQIN} \times \frac{1}{PCTQ + 1} \times \frac{1}{DCTQ + 1}$$

Equation 21

The standard setting is given by CTQSEL = 00_B ($f_{CTQIN} = f_{PDIV}$), PPPEN = 0 ($f_{PPP} = f_{PIN}$) and CLKSEL = 00_B ($f_{PIN} = f_{FD}$). Under these conditions, the baud rate can further be equated to either ***Equation 22*** or ***Equation 23***, depending on the selected divider mode:

$$f_{IIC} = f_{PERIPH} \times \frac{1}{1024 - STEP} \times \frac{1}{PDIV + 1} \times \frac{1}{PCTQ + 1} \times \frac{1}{DCTQ + 1}$$

Equation 22 Normal divider mode (FDR.DM = 01_B)

$$f_{IIC} = f_{PERIPH} \times \frac{STEP}{1024} \times \frac{1}{PDIV+1} \times \frac{1}{PCTQ+1} \times \frac{1}{DCTQ+1}$$

Equation 23 Fractional divider mode (FDR.DM = 10_B)

Table 204 shows examples of the baud rate calculation in fractional divider mode (FDR.DM = 10_B).

Table 204 IIC Baud Rate Calculation in Fractional Divider Mode

f_{PERIPH} (MHz)	FDR.STEP	BRG.PDIV	BRG.PCTQ	BRG.DCTQ	f_{IIC} (kbit/s)	Deviation Error
48	512	11	1	9	100	0.00%
48	427	0	1	24	400	0.08%

Note: The values shown in Table 204 should be used only as a reference. The actual IIC baud rates are highly influenced by external factors such as the pull-up resistance on the bus, the slave speed, etc.

The baud rate setting should only be changed while the transmitter and the receiver are idle or CCR.MODE = 0.

18.5.3.2 Transmission Chain

The IIC bus protocol requiring a kind of in-bit-response during the arbitration phase and while a slave is transmitting, the resulting loop delay of the transmission chain can limit the reachable maximal baud rate, strongly depending on the bus characteristics (bus load, module frequency, etc.).

Figure 104 shows the general signal path and the delays in the case of a slave transmission. The shift clock SCL is generated by the master device, output on the wire, then it passes through the input stage and the input filter. Now, the edges can be detected and the SDA data signal can be generated accordingly. The SDA signal passes through the output stage and the wire to the master receiver part. There, it passes through the input stage and the input filter before it is sampled.

This complete loop has to be finished (including all settling times to obtain stable signal levels) before the SCL signal changes again. The delays in this path have to be taken into account for the calculation of the baud rate as a function of f_{PERIPH} and f_{PPP}.

18.5.3.3 Byte Stretching

If a device is selected as transceiver and should transmit a data byte but the transmit buffer TBUF does not contain valid data to be transmitted, the device ties down SCL = 0 at the end of the previous acknowledge bit.

The waiting period is finished if new valid data has been detected in TBUF.

18.5.3.4 Master Arbitration

During the address and data transmission, the master transmitter checks at the rising edge of SCL for each data bit if the value it is sending is equal to the value read on the SDA line.

- If yes, the next data bit values can be 0.
- If this is not the case (transmitted value = 1, value read = 0), the master has lost the transmit arbitration.
  - This is indicated by status flag PSR.ARL and can generate a protocol interrupt if enabled by PCR.ARLIEN.

When the transmit arbitration has been lost, the software has to initialize the complete frame again, starting with the first address byte together with the start condition for a new master transmit attempt. Arbitration also takes place for the ACK bit.

18.5.3.5 Not Acknowledge and Error Conditions

In case of a not acknowledge or an error, the TCSR.TDV flag remains set, but no further transmission will take place.

User software must invalidate the transmit buffer and disable transmissions (by writing FMRL.MTDV = 10_B), before configuring the transmission (by writing TBUF) again with appropriate values to react on the previous event.

In the case the FIFO data buffer is used, additionally the FIFO buffer needs to be flushed and filled again.

A software recovery sequence can include the following steps:

1. Flush the FIFO buffer (if FIFO buffer is used):
   a. Write 1_B to both TRBSCR.FLUSHTB and TRBSCR.FLUSHRB bits.
2. Invalidate the internal transmit buffer TBUF:
   a. Write 10_B to FMR.MTDV bit field.
3. Clear all status bits if necessary.

For the IIC slave, it might be additionally required to first disable the SDA and SCL output port functions (write 0 to the corresponding IOCRx.PCy bit fields). This ensures that the SDA and SCL lines are not held low infinitely by the slave. The port functions can be enabled again at the end of the sequence.

18.5.3.6 Mode Control Behavior

In IIC mode, the following kernel modes are supported:

- Run Mode 0:

  Behavior as programmed. If TCSR.TDV = 0 (no new valid TBUF entry found) when a new TBUF entry needs to be processed, the IIC module waits for TDV becoming set to continue operation.
- Run Mode 1:

  Behavior as programmed. If in master mode, TCSR.TDV = 0 (no new valid TBUF entry found) when a new TBUF entry needs to be processed, the IIC module sends a stop condition to finish the frame. In slave mode, no difference to run mode 0.
- Stop Mode 0:

  Bit TCSR.TDV is internally considered as 0 (the bit itself is not modified by the stop mode). A currently running word is finished normally, but no new word is started in case of master mode (wait for TDV active).

  Bit TDV being considered as 0 for master and slave, the slave will force a wait state on the bus if read by an external master, too.

  Additionally, it is not possible to force the generation of a STOP condition out of the wait state. The reason is, that a master read transfer must be finished with a not-acknowledged followed by a STOP condition to allow the slave to release his SDA line. Otherwise the slave may force the SDA line to 0 (first data bit of next byte) making it impossible to generate the STOP condition (rising edge on SDA).

  To continue operation, the mode must be switched to run mode 0
- Stop Mode 1:

  Same as stop mode 0, but additionally, a master sends a STOP condition to finish the frame.

  If stop mode 1 is requested for a master device after the first byte of a 10 bit address, a stop condition will be sent out. In this case, a slave device will issue an error interrupt.

Note: In multi-master mode, only run mode 0 and stop mode 0 are supported, the other modes must not be programmed.

18.5.3.7 Data Transfer Interrupt Handling

The data transfer interrupts indicate events related to IIC frame handling.

As the data input and output pins are the same in IIC protocol, a IIC transmitter also receives the output data at its input pin. However, no receive related interrupts will be generated in this case.

Table 205 IIC data transfer interrupt handling

Interrupt	Indicated by bit	Description
Transmit buffer interrupt	PSR.TBIF	Set after the content of the transmit buffer TBUF has been loaded to the transmit shift register. With this event, bit TCSR.TDV is cleared and new data can be loaded to the transmit buffer. This interrupt can be used to write the next TBUF entry while the last one is in progress (handled by the transmitter part).
Transmit shift interrupt	PSR.TSIF	Set after the start of the last data bit of a data word.
Receiver start interrupt	PSR.RSIF	Set after the sample point of the first data bit of a data word.
Receiver interrupt	PSR.RIF	Set after a data byte, which is not the first byte of a frame, is received (after the falling edge of SCL) in the receive buffer RBUF0/1. This interrupt can be used to read out the received data while a new data byte can be in progress (handled by the receiver part).
Alternative interrupt	PSR.AIF	Similar to PSR.RIF except that PSR.AIF indicates that the data byte received is the first byte of a new frame. AIF is based on bit RBUFSR[9] (same as RBUF[9]).
Data lost interrupt	PSR.DLIF	Set if the data word available in register RBUF (oldest data word from RBUF0 or RBUF1) has not been read out before it becomes overwritten with new incoming data.

Note: The transmit shift and receive start events can be ignored if the application does not require them during the IIC data transfer.

18.5.3.8 IIC Protocol Interrupt Events

The following protocol-related events are generated in IIC mode and can lead to a protocol interrupt.

Please note that the bits in register PSR are not all automatically cleared by hardware and have to be cleared by software in order to monitor new incoming events.

Table 206 IIC protocol interrupt events

Events	Event flag	Description	Flag clear	Interrupt enable
Start condition	PSR.SCR	Set after a valid start condition is detected.	PSCR.CST2	PCR.SCRIEN

Table 206 IIC protocol interrupt events (continued)

Events	Event flag	Description	Flag clear	Interrupt enable
Repeated start condition	PSR.RSCR	Set after a valid repeated start condition is detected.	PSCR.CST3	PCR.RSCRIEN
Stop condition	PSR.PCR	Set after a valid stop condition is detected.	PSCR.CST4	PCR.PCRIEN
Master arbitration lost	PSR.ARL	Set after the master arbitration is lost while in master mode.	PSCR.CST6	PCR.ARLIEN
Slave read requested	PSR.SRR	Set after a slave read is requested while in slave mode.	PSCR.CST7	PCR.SRRIEN
ACK received	PSR.ACK	Set after an acknowledge bit is received while in master mode.	PSCR.CST9	PCR.ACKIEN
NACK received	PSR.NACK	Set after a not acknowledge bit is received while in master mode.	PSCR.CST5	PCR.NACKIEN
Error condition	PSR.ERR	Set after one of the following has occurred: • Start condition not at the expected position in a frame • Stop condition not at the expected position in a frame • 10-bit address interrupted by a stop condition after the first address byte in slave mode	PSCR.CST8	PCR.ERRIEN
TDF code error	PSR.WTDF	Set after one of the following has occurred: • TDF slave code in master mode • TDF master code in slave mode • Reserved TDF code found • Start condition code during a running frame in master mode • Data byte transmission code after transfer direction has been changed to reception (master read) in master mode	PSCR.CST1	

If a wrong TDF code is found in TBUF, the error event is active until the TDF value is either corrected or invalidated. If the related interrupt is enabled, the interrupt handler should check PSR.WDTF first and correct or invalidate TBUF, before dealing with the other possible interrupt events.

18.5.3.9 Receiver Address Acknowledge

After a (repeated) start condition, the master sends a slave address to identify the target device of the communication. The start address can comprise one or two address bytes (for 7-bit or for 10-bit addressing schemes). After an address byte, a slave sensitive to the transmitted address has to acknowledge the reception.

Therefore, the slave's address can be programmed in the device, where it is compared to the received address. In case of a match, the slave answers with an acknowledge (SDA = 0). Slaves that are not targeted answer with an non-acknowledge (SDA = 1).

In addition to the match of the programmed address, the slave can also be configured to acknowledge the address byte 00_H, which indicates a general call address. This is done by setting the bit PCR.ACK00 to 1.

In order to allow selective acknowledges for the different values of the address byte(s), the following control mechanism is implemented:

- The address byte 00_H is acknowledged if bit PCR.ACK00 is set.
- The first 7 bits of a received first address byte are compared to the programmed slave address (PCR.SLAD[15:9]). If these bits match, the slave sends an acknowledge.
- If the slave address is programmed to 1111 $0XX_B$, the slave device waits for a second address byte and compares it also to PCR.SLAD[7:0] and sends an acknowledge accordingly to cover the 10-bit addressing mode.

Under each of these conditions, bit PSR.SLSEL will be set when the addressing delivered a match. This bit is cleared automatically by a (repeated) start condition.

Note: The address byte 01_H (START byte) and other reserved addresses (refer to IIC specification) are not acknowledged.

18.5.3.10 Receiver Handling

A selected slave receiver always acknowledges a received data byte. If the receive buffers RBUF0/1 are already full and can not accept more data, the respective register is overwritten (PSR.DLIF becomes set in this case and a protocol interrupt can be generated).

An address reception also uses the registers RBUF0/1 to store the address before checking if the device is selected. The received addresses do not set RDV0/1, so the addresses are not handled like received data.

18.5.3.11 Receiver Status Information

In addition to the received data byte, some IIC protocol related information is stored in the 16-bit data word of the receive buffer.

The received data byte is available at the bit positions RBUF[7:0], whereas the additional information is monitored at the bit positions RBUF[12:8].

This structure allows to identify the meaning of each received data byte without reading additional registers, also when using a FIFO data buffer.

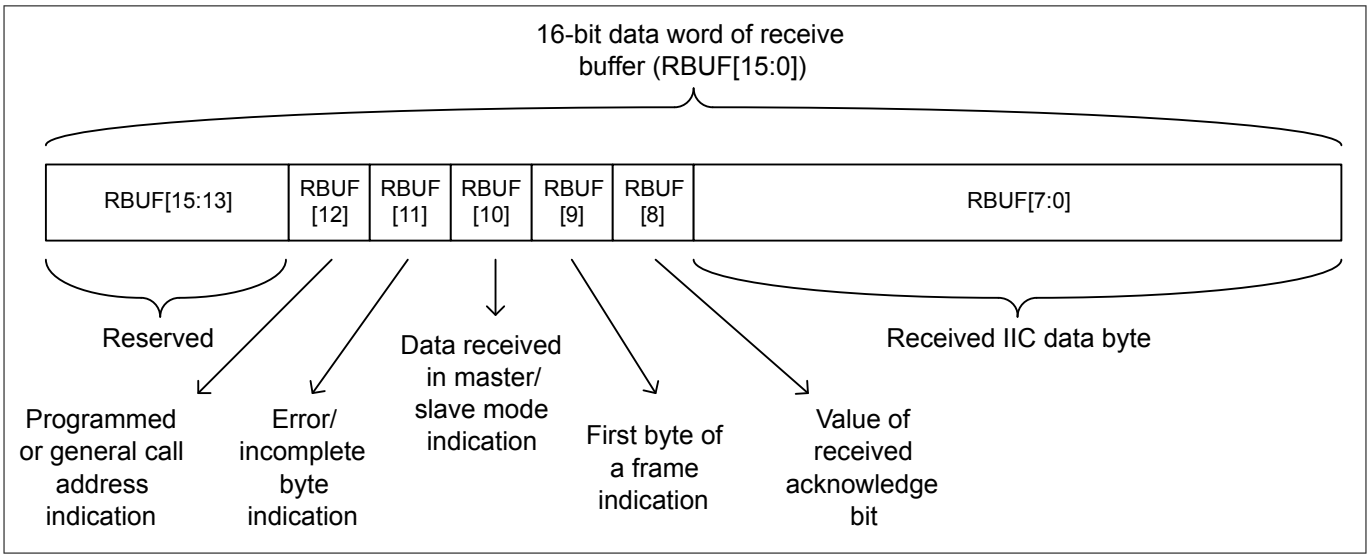


Figure 110 IIC received data word

Table 207 IIC protocol related information in RBUF register

Field	Description
RBUF[8]	Value of the received acknowledge bit. This information is also available in RBUFSR[8] as protocol argument.
RBUF[9]	This bit indicates the data byte received after a (repeated) start condition and following the address reception: 0_B Subsequent data bytes of a frame has been received. 1_B The first data byte of a new frame has been received. This information is also available in RBUFSR[9], allowing different interrupt routines for the address and data handling.
RBUF[10]	0_B Data byte has been received while in slave mode. 1_B Data byte has been received while in master mode.
RBUF[11]	0_B Data byte is received correctly. 1_B An incomplete/erroneous data byte in the receive buffer caused by a wrong position of a START or STOP condition in the frame. The bit is not identical to the frame error status bit in PSR, because the bit in the PSR has to be cleared by software (“sticky” bit), whereas RBUF[11] is evaluated data byte by data byte.
RBUF[12]	0_B The programmed address has been received. 1_B A general call address has been received.

18.5.3.12 IIC Initialization Code Example

The following code example implements a function to initialize USIC0 channel 1 for IIC data transfers with a baud rate of 400 kbit/s (f_{PERIPH} = 48 MHz).

The same code can be used for master and slave mode operation. If the slave address is not needed (i.e. master only operation), the bit field PCR.SLAD can be programmed to 0.

```
void USIC0_CH1_IIC_Init(void)
{
/// ----------------------------------------------------------------------
/// 1. Enable USIC0 channel 1
/// ----------------------------------------------------------------------
    //                    BPMODEN    MODEN
    USIC0_CH1->KSCFG |= (1 << 1) | (1 << 0);

/// ----------------------------------------------------------------------
/// 2. Configure baud rate generator
///    - Fractional divider mode
///    - Baud rate = 400 kbit/s
/// ----------------------------------------------------------------------
    //                   DM           STEP
    USIC0_CH1->FDR = (2 << 14) | (427 << 0);
    //                  PDIV         DCTQ       PCTQ
    USIC0_CH1->BRG = (0 << 16) | (24 << 10) | (1 << 8);

/// ----------------------------------------------------------------------
/// 3. Configure input stages
///    - Select inputs DX0D and DX1B
///    - Protocol pre-processor to control data shift unit inputs
/// ----------------------------------------------------------------------
    //                    INSW       DSEL
    USIC0_CH1->DX0CR = (0 << 4) | (3 << 0);
    //                    INSW       DSEL
    USIC0_CH1->DX1CR = (0 << 4) | (1 << 0);

/// ----------------------------------------------------------------------
/// 4. Configure data format
///    - Data word = 8 bits with unlimited data flow
///    - Data transfer allowed with passive level = 1 and MSB first
/// ----------------------------------------------------------------------
    //                    WLE       FLE       TRM       PDL       SDIR
    USIC0_CH1->SCTR = (7 << 24)|(63 << 16)|(3 << 8)|(1 << 1)|(1 << 0);

/// ----------------------------------------------------------------------
/// 5. Configure data transfer parameters
///    - Single shot transmission of data word when a valid word
///      is available
/// ----------------------------------------------------------------------
    //                   TDEN        TDSSM
    USIC0_CH1->TCSR = (1 << 10) | (1 << 8);

/// ----------------------------------------------------------------------
/// 6. Configure IIC protocol-specific parameters
///    - 1 symbol = 25 time quanta
///    - Configure HDEL for SDA hold time
///    - Configure slave address (assume 7-bit address = 0x5)
/// ----------------------------------------------------------------------
```

```
    //                   HDEL       STIM        SLAD
    USIC0_CH1->PCR = (7 << 26) | (1 << 17) | (5 << 9);;

/// ----------------------------------------------------------------------
/// 7. Enable IIC protocol
/// ----------------------------------------------------------------------
    //                  MODE
    USIC0_CH1->CCR = (4 << 0);

/// ----------------------------------------------------------------------
/// 8. Configure IIC output function pins
///    - Assume
///        - P0.7 ALT7 function is assigned to DOUT0
///        - P0.8 ALT7 function is assigned to SCLKOUT
/// ----------------------------------------------------------------------
    //                    PC7
    PORT0->IOCR4 |= (0x27 << 26);
    //                    PC8
    PORT0->IOCR8 |= (0x27 << 2);
}
```

18.5.4 Data Flow Handling

The handling of the data flow and the sequence of the symbols in an IIC frame is controlled by the IIC transmitter part of the USIC communication channel. The IIC bus protocol is byte-oriented, whereas a USIC data buffer word can contain up to 16 data bits. In addition to the data byte to be transmitted (located at TBUF[7:0]), bit field TDF (transmit data format) to control the IIC sequence is located at the bit positions TBUF[10:8]. The TDF code defines for each data byte how it should be transmitted (IIC master or IIC slave), and controls the transmission of (repeated) start and stop symbols. This structure allows the definition of a complete IIC frame for an IIC master device only by writing to TBUFx or by using a FIFO data buffer mechanism, because no other control registers have to be accessed. Alternatively, polling of the ACK and NACK bits in PSR register can be performed, and the next data byte is transmitted only after an ACK is received.

If a wrong or unexpected TDF code is encountered (e.g. due to a software error during setup of the transmit buffer), a stop condition will be sent out by the master. This leads to an abort of the currently running frame. A slave module waits for a valid TDF code and sets SCL = 0. The software then has to invalidate the unexpected TDF code and write a valid one.

Note: During an arbitration phase in multi-master bus systems an unpredictable bus behavior may occur due to an unexpected stop condition.

18.5.4.1 Transmit Data Formats

The following transmit data formats are available in master mode:

Table 208 Master Transmit Data Formats

TDF Code	Description
000_B	Send data byte as master This format is used to transmit a data byte from the master to a slave. The transmitter sends its data byte (TBUF[7:0]), receives and checks the acknowledge bit sent by the slave.

Table 208 Master Transmit Data Formats (continued)

TDF Code	Description
010_B	Receive data byte and send acknowledge This format is used by the master to read a data byte from a slave. The master acknowledges the transfer with a 0-level to continue the transfer. The content of TBUF[7:0] is ignored.
011_B	Receive data byte and send not-acknowledge This format is used by the master to read a data byte from a slave. The master does not acknowledge the transfer with a 1-level to finish the transfer. The content of TBUF[7:0] is ignored.
100_B	Send start condition If TBUF contains this entry while the bus is idle, a start condition will be generated. The content of TBUF[7:0] is taken as first address byte for the transmission (bits TBUF[7:1] are the address, the LSB is the read/write control).
101_B	Send repeated start condition If TBUF contains this entry and SCL = 0 and a byte transfer is not in progress, a repeated start condition will be sent out if the device is the current master. The current master is defined as the device that has set the start condition (and also won the master arbitration) for the current message. The content of TBUF[7:0] is taken as first address byte for the transmission (bits TBUF[7:1] are the address, the LSB is the read/write control).
110_B	Send stop condition If the current master has finished its last byte transfer (including acknowledge), it sends a stop condition if this format is in TBUF. The content of TBUF[7:0] is ignored.
111_B	Reserved This code must not be programmed. No additional action except releasing the TBUF entry and setting the error bit in PSR (that can lead to a protocol interrupt).

The following transmit data format is available in slave mode (the symbols in a frame are controlled by the master and the slave only has to send data if it has been “asked” by the master):

Table 209 Slave Transmit Data Format

TDF Code	Description
001_B	Send data byte as slave This format is used to transmit a data byte from a slave to the master. The transmitter sends its data byte (TBUF[7:0]) plus the acknowledge bit as a 1.

18.5.4.2 Valid Master Transmit Data Formats

Due to the IIC frame format definitions, only some specific sequences of TDF codes are possible and valid. If the USIC IIC module detects a wrong TDF code in a running frame, the transfer is aborted and flag PCR.WTDF is set. Additionally, an interrupt can be generated if enabled by the user. In case of a wrong TDF code, the frame will be aborted immediately with a STOP condition if the USIC IIC master still owns the SDA line. But if the accessed slave owns the SDA line (read transfer), the master must perform a dummy read with a non-acknowledge so that the slave releases the SDA line before a STOP condition can be sent. The received data byte of the dummy

read will be stored in RBUF0/1, but RDV0/1 will not be set. Therefore the dummy read will not generate a receive interrupt and the data byte will not be stored into the receive FIFO.

If the transfer direction has changed in the current frame (master read access), the transmit data request (TDF = 000_B) is not possible and won't be accepted (leading to a wrong TDF Code indication).

Table 210 Valid TDF Codes Overview

Frame Position	Valid TDF Codes
First TDF code (master idle)	Start (100_B)
Read transfer: second TDF code (after start or repeated start)	Receive with acknowledge (010_B) or receive with not-acknowledge (011_B)
Write transfer: second TDF code (after start or repeated start)	Transmit (000_B), repeated start (101_B), or stop (110_B)
Read transfer: third and subsequent TDF code after acknowledge	Receive with acknowledge (010_B) or receive with not-acknowledge (011_B)
Read transfer: third and subsequent TDF code after not-acknowledge	Repeated start (101_B) or stop (110_B)
Write transfer: third and subsequent TDF code	Transmit (000_B), repeated start (101_B), or stop (110_B)

- First TDF code:

  A master transfer starts with the TDF start code (100_B). All other codes are ignored, but no WTDF error will be indicated.
- TDF code after a start (100_B) or repeated start code (101_B) in case of a read access:

  If a master-read transfer is started (determined by the LSB of the address byte = 1), the transfer direction of SDA changes and the slave will actively drive the data line. In this case, only the codes 010_B and 011_B are valid. To abort the transfer in case of a wrong code, a dummy read must be performed by the master before the STOP condition can be generated.
- TDF code after a start (100_B) or repeated start code (101_B) in case of a write access:

  If a master-write transfer is started (determined by the LSB of the address byte = 0), the master still owns the SDA line. In this case, the transmit (000_B), repeated start (101_B) and stop (110_B) codes are valid. The other codes are considered as wrong. To abort the transfer in case of a wrong code, the STOP condition is generated immediately.
- TDF code of the third and subsequent command in case of a read access with acknowledged previous data byte:

  If a master-read transfer is started (determined by the LSB of the address byte), the transfer direction of SDA changes and the slave will actively drive the data line. To force the slave to release the SDA line, the master has to not-acknowledge a byte transfer. In this case, only the receive codes 010_B and 011_B are valid. To abort the transfer in case of a wrong code, a dummy read must be performed by the master before the STOP condition can be generated.
- TDF code of the third and subsequent command in case of a read access with a not-acknowledged previous data byte:

  If a master-read transfer is started (determined by the LSB of the address byte), the transfer direction of SDA changes and the slave will actively drive the data line. To force the slave to release the SDA line, the master has to not-acknowledge a byte transfer. In this case, only the restart (101_B) and stop code (110_B) are valid. To abort the transfer in case of a wrong code, the STOP condition is generated immediately.
- TDF code of the third and subsequent command in case of a write access:

  If a master-write transfer is started (determined by the LSB of the address byte), the master still owns the SDA line. In this case, the transmit (000_B), repeated start (101_B) and stop (110_B) codes are valid. The other

codes are considered as wrong. To abort the transfer in case of a wrong code, the STOP condition is generated immediately.

- After a master device has received a non-acknowledge from a slave device, a stop condition will be sent out automatically, except if the following TDF code requests a repeated start condition. In this case, the TDF code is taken into account, whereas all other TDF codes are ignored.

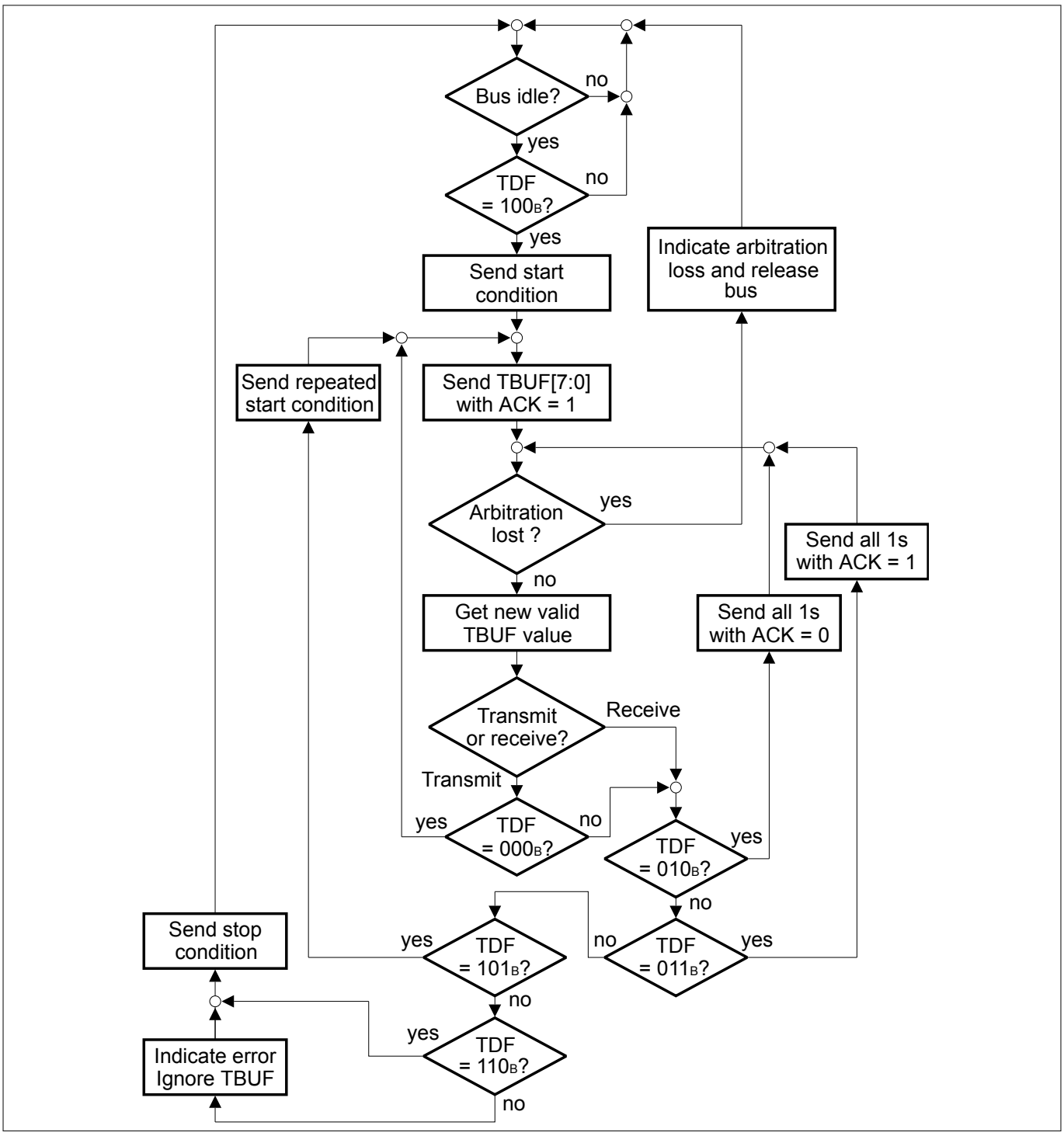


Figure 111 IIC Master Transmission

18.5.4.3 Master Transmit/Receive Modes

In master transmit mode, the IIC sends a number of data bytes to a slave receiver. The TDF code sequence for the master transmit mode is shown in ***Table 211***.

Table 211 TDF Code Sequence for Master Transmit

TDF Code Sequence	TBUF[10:8] (TDF Code)	TBUF[7:0]	IIC Response	Interrupt Events
1st code	100_B	Slave address + write bit	Send START condition, slave address and write bit	SCR: Indicates a START condition is detected TBIF: Next word can be written to TBUF
2nd code	000_B	Data or 2nd slave address byte	Send data or 2nd slave address byte	TBIF: Next word can be written to TBUF
Subsequent codes for data transmit	000_B	Data	Send data	TBIF: Next word can be written to TBUF
Last code	110_B	Don't care	Send STOP condition	PCR: Indicates a STOP condition is detected

In master receive mode, the IIC receives a number of data bytes from a slave transmitter. The TDF code sequence for the master receive 7-bit and 10-bit addressing modes are shown in ***Table 212*** and ***Table 213***.

Table 212 TDF Code Sequence for Master Receive (7-bit Addressing Mode)

TDF Code Sequence	TBUF[10:8] (TDF Code)	TBUF[7:0]	IIC Response	Interrupt Events
1st code	100_B	Slave address + read bit	Send START condition, slave address and read bit	SCR: Indicates a START condition is detected TBIF: Next word can be written to TBUF
2nd code	010_B	Don't care	Receive data and send ACK bit	TBIF: Next word can be written to TBUF AIF: First data received can be read
Subsequent codes for data receive	010_B	Don't care	Receive data and send ACK bit	TBIF: Next word can be written to TBUF RIF: Subsequent data received can be read
Code for last data to be received	011_B	Don't care	Receive data and send NACK bit	TBIF: Next word can be written to TBUF RIF: Last data received can be read
Last code	110_B	Don't care	Send STOP condition	PCR: Indicates a STOP condition is detected

Table 213 TDF Code Sequence for Master Receive (10-bit Addressing Mode)

TDF Code Sequence	TBUF[10:8] (TDF Code)	TBUF[7:0]	IIC Response	Interrupt Events
1st code	100_B	Slave address (1st byte) + write bit	Send START condition, slave address (1st byte) and write bit	SCR: Indicates a START condition is detected TBIF: Next word can be written to TBUF
2nd code	000_B	Slave address (2nd byte)	Send address (2nd byte)	TBIF: Next word can be written to TBUF
3rd code	101_B	1st slave address + read bit	Send repeated START condition, slave address (1st byte) and read bit	RSCR: Indicates a repeated START condition is detected TBIF: Next word can be written to TBUF
4th code	010_B	Don’t care	Receive data and send ACK bit	TBIF: Next word can be written to TBUF AIF: First data received can be read
Subsequent codes for data receive	010_B	Don’t care	Receive data and send ACK bit	TBIF: Next word can be written to TBUF RIF: Subsequent data received can be read
Code for last data to be received	011_B	Don’t care	Receive data and send NACK bit	TBIF: Next word can be written to TBUF RIF: Last data received from slave can be read
Last code	110_B	Don’t care	Send STOP condition	PCR: Indicates a STOP condition is detected

Figure 112 shows the interrupt events during the master transmit-slave receive and master receive/slave transmit sequences.

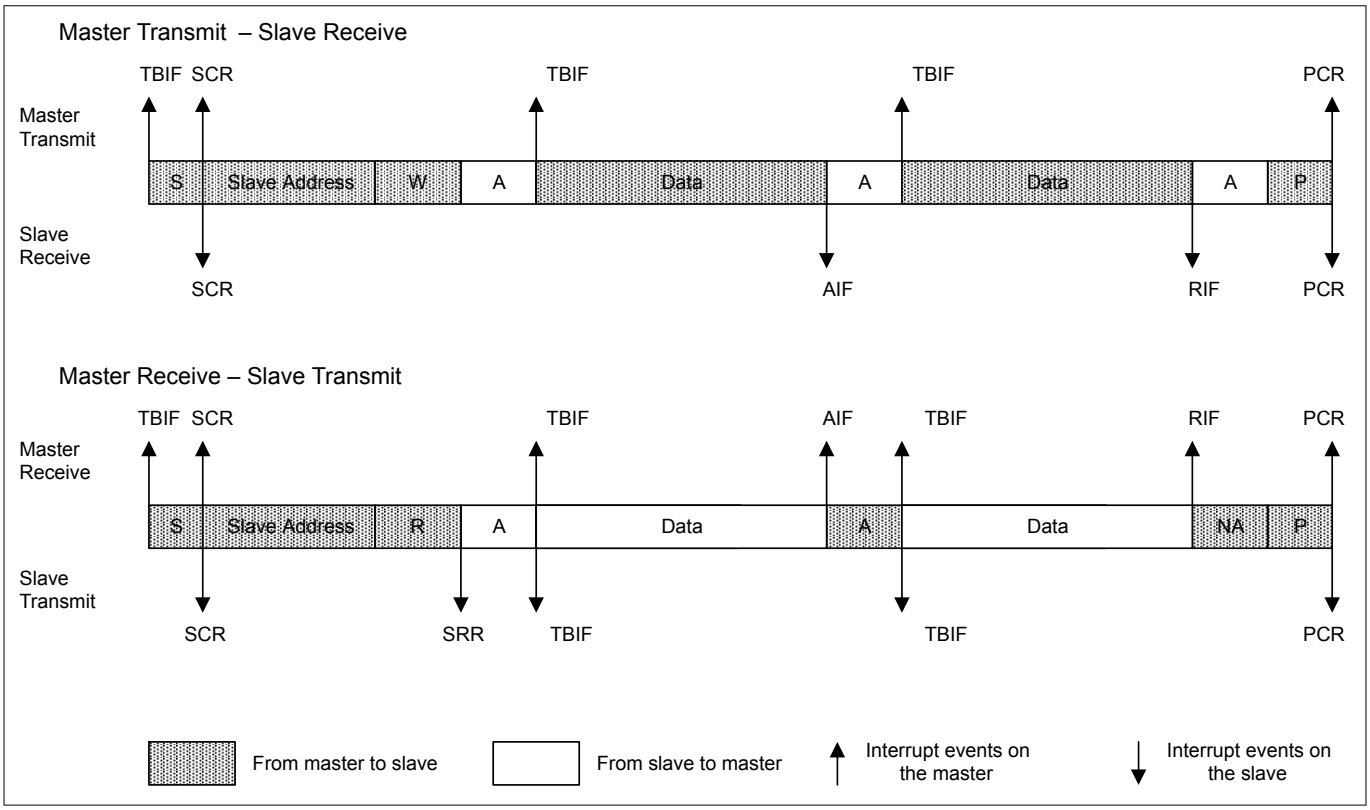


Figure 112 Interrupt Events on Data Transfers

18.5.4.4 Slave Transmit/Receive Modes

In slave receive mode, no TDF code needs to be written and data reception is indicated by the alternate receive (AIF) or receive (RIF) events.

In slave transmit mode, upon receiving its own slave address or general call address if this option is enabled, a slave read request event (SRR) will be triggered. The slave IIC then writes the TDF code 001 and the requested data to TBUF to transmit the data to the master. The slave does not check if the master reply with an ACK or NACK to the transmitted data.

In both cases, the data transfer is terminated by the master sending a STOP condition, which is indicated by a PCR event. See also ***Figure 112***.

18.6 Service Request Generation

The USIC module provides 6 service request outputs SR[5:0] to be shared between two channels. The service request outputs SR[5:0] are connected to interrupt nodes in the Nested Vectored Interrupt Controller (NVIC).

Each USIC communication channel can be connected to up to 6 service request handlers (connected to USICx.SR[5:0], though 3 or 4 are normally used, e.g. one for transmission, one for reception, one or two for protocol or error handling, or for the alternative receive events).

18.6.1 General Channel Events and Interrupts

The general event and interrupt structure is shown in ***Figure 113***. If a defined condition is met, an event is detected and an event indication flag becomes automatically set. The flag stays set until it is cleared by software. If enabled, an interrupt can be generated if an event is detected. The actual status of the event indication flag has no influence on the interrupt generation. As a consequence, the event indication flag does not need to be cleared to generate further interrupts.

Additionally, the service request output SRx of the USIC channel that becomes activated in case of an event condition can be selected by an interrupt node pointer. This structure allows to assign events to interrupts, e.g. depending on the application, several events can share the same interrupt routine (several events activate the same SRx output) or can be handled individually (only one event activates one SRx output).

The SRx outputs are connected to the NVIC interrupt nodes for CPU processing of the service requests. This assignment is described in the interconnects section on page ***504***.

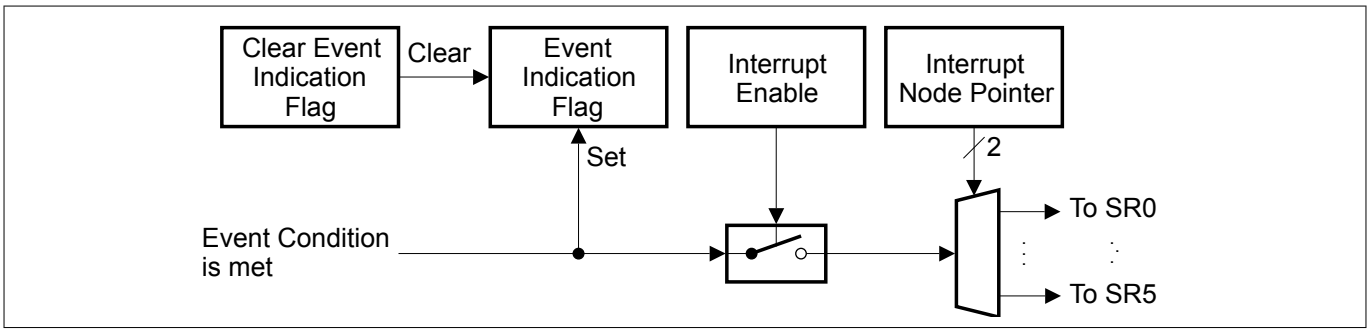


Figure 113 General Event and Interrupt Structure

18.6.2 Data Transfer Events and Interrupts

The data transfer events are based on the transmission or reception of a data word and are described in the corresponding protocol chapters.

All events can be individually enabled for interrupt generation.

Table 214 shows the registers, bits and bit fields indicating the data transfer events and controlling the interrupts of a USIC channel.

Table 214 Data Transfer Events and Interrupt Handling

Event	Indication Flag	Indication cleared by	Interrupt enabled by	SRx Output selected by
Standard receive event	PSR.RIF	PSCR.CRIF	CCR.RIEN	INPR.RINP
Receive start event	PSR.RSIF	PSCR.CRSIF	CCR.RSIEN	INPR.TBINP
Alternative receive event	PSR.AIF	PSCR.CAIF	CCR.AIEN	INPR.AINP
Transmit shift event	PSR.TSIF	PSCR.CTSIF	CCR.TSIEN	INPR.TSINP
Transmit buffer event	PSR.TBIF	PSCR.CTBIF	CCR.TBIEN	INPR.TBINP
Data lost event	PSR.DLIF	PSCR.CDLIF	CCR.DLIEN	INPR.PINP

Figure 114 shows the two transmit events and interrupts.

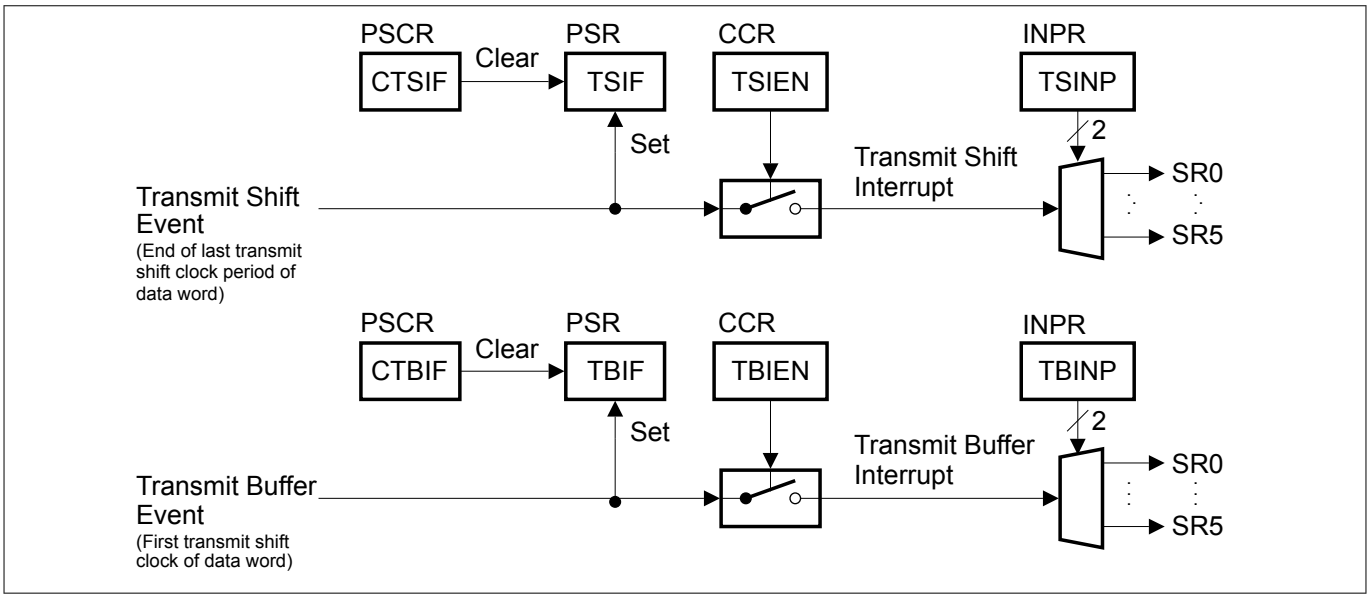


Figure 114 Transmit Events and Interrupts

Figure 115 shows the receive events and interrupts.

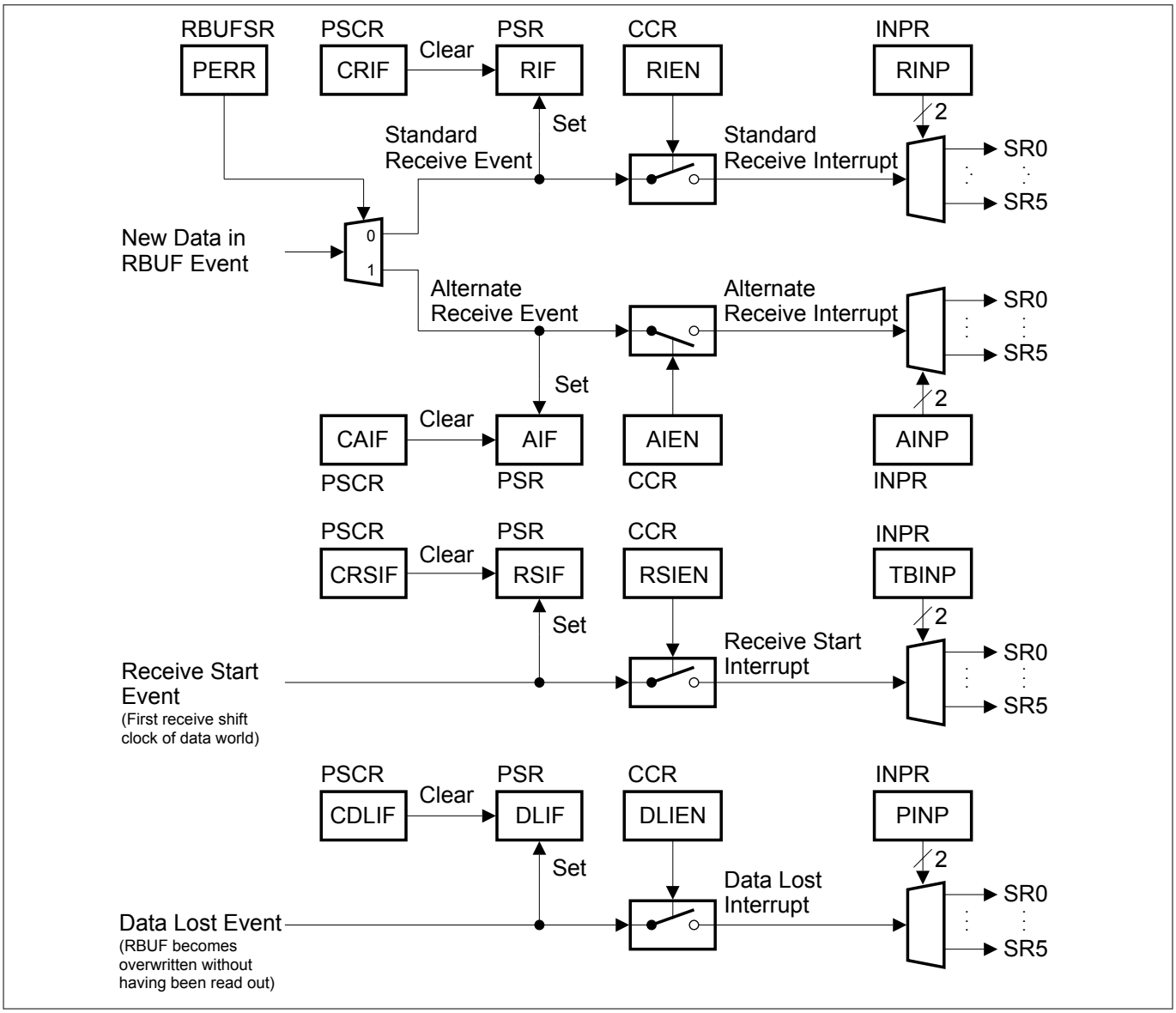


Figure 115 Receive Events and Interrupts

18.6.3 Baud Rate Generator Event and Interrupt

The baud rate generator event is based on the capture mode timer reaching its maximum value.

It can be enabled for the generation of a protocol interrupt.

Table 215 shows the registers, bits and bit fields indicating the baud rate generator event and controlling the interrupt of a USIC channel.

Table 215 Baud Rate Generator Event and Interrupt Handling

Event	Indication Flag	Indication cleared by	Interrupt enabled by	SRx Output selected by
Baud rate generator event	PSR.BRGIF	PSCR.CBRGIF	CCR.BRGIEN	INPR.PINP

Figure 116 shows the baud rate generator event and interrupt.

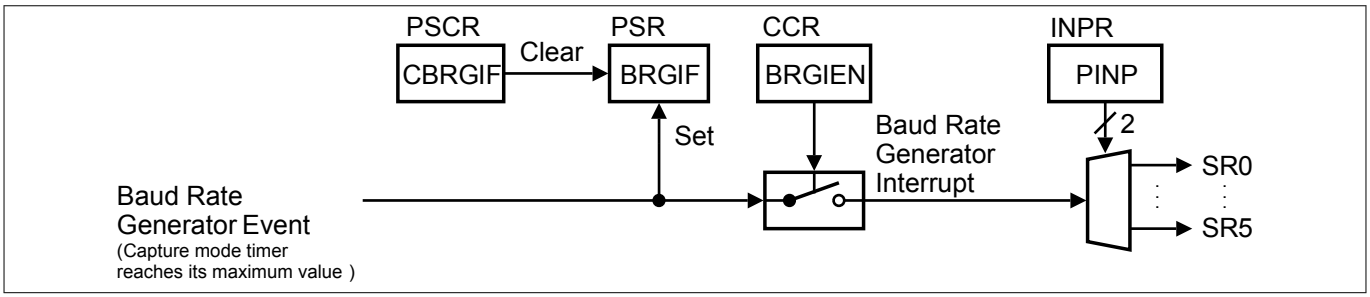


Figure 116 Baud Rate Generator Event and Interrupt

18.6.4 Protocol-specific Events and Interrupts

These events are related to protocol-specific actions that are described in the corresponding protocol chapters.

- ASC (***Chapter 18.3.3.7***)
- SSC master mode (***Chapter 18.4.3.5***)
- SSC slave mode (***Chapter 18.4.4.1***)
- IIC (***Chapter 18.5.3.8***)

All events can be individually enabled for the generation of the common protocol interrupt.

Table 216 Protocol-specific Events and Interrupt Handling

Event	Indication Flag	Indication cleared by	Interrupt enabled by	SRx Output selected by
Protocol-specific events in ASC mode	PSR.ST[8:2]	PSCR.CST[8:2]	PCR.CTR[7:3]	INPR.PINP
Protocol-specific events in SSC mode	PSR.ST[3:2]	PSCR.CST[3:2]	PCR.CTR[15:14]	INPR.PINP
Protocol-specific events in IIC mode	PSR.ST[8:1]	PSCR.CST[8:1]	PCR.CTR[24:18]	INPR.PINP

18.7 Debug Behaviour

Each USIC communication channel can be pre-configured to enter one of four kernel modes, when the program execution of the CPU is halted by the debugger.

Selection is done through the bit field KSCFG.SUMCFG and the definition of the four kernel modes may differ across protocols. Refer to the protocol sections for details:

- ASC (***Chapter 18.3.3.4***)
- SSC (***Chapter 18.4.2.2***)
- IIC (***Chapter 18.5.3.6***)

To avoid disturbing the receive data sequence and causing the loss of data, the debugger read accesses should not target the receive buffer RBUF (or OUTR if the receive FIFO buffer is used). Instead, the alternative address location at RBUFD (or OUTDR) should be used. A read at this location delivers the same value as RBUF (or OUTR) but does not affect the status of the read data.

18.8 Power, Reset and Clock

The USIC module is located in the core power domain. The module can be reset to its default state by a system reset.

The USIC module is clocked by the main clock, MCLK, from SCU. MCLK is disabled by default and can be enabled via the SCU_CGATCLR0 register. Enabling and disabling the module clock could cause a load change and clock blanking could occur as described in the CCU (Clock Gating Control) section of the SCU chapter. It is strongly recommended to set up the module clock in the user initialization code to avoid clock blanking during runtime.

Note: To differentiate from the USIC baud rate generator output, master clock (MCLK), the SCU MCLK is referenced throughout the USIC chapter as f_{PERIPH}.

18.9 Initialization and System Dependencies

The application has to apply the following initialization sequence before operating the USIC module:

- Disable the system level clock gating of the USIC module(s) by writing one(s) to the USICx bits in the SCU register CGATCLR0.

For the initialization of the USIC channel for a specific protocol, refer to the protocol section:

- ASC (***Chapter 18.3.3***)
- SSC master mode (***Chapter 18.4.3***)
- SSC slave mode (***Chapter 18.4.4***)
- IIC (***Chapter 18.5.3***)

18.10 Registers

Table 217 shows all registers which are required for programming a USIC channel, as well as the FIFO buffer. It summarizes the USIC communication channel registers and defines the relative addresses and the reset values.

All registers can be accessed with any access width (8-bit, 16-bit, 32-bit), independent of the described width.

Note: The register bits marked "w" always deliver 0 when read. They are used to modify flip-flops in other registers or to trigger internal actions.

Figure 117 shows the register types of the USIC module registers and channel registers. In a specific microcontroller, module registers of USIC module "x" are marked by the module prefix "USICx_". Channel registers of USIC module "x" are marked by the channel prefix "USICx_CH0_" and "USICx_CH1_".

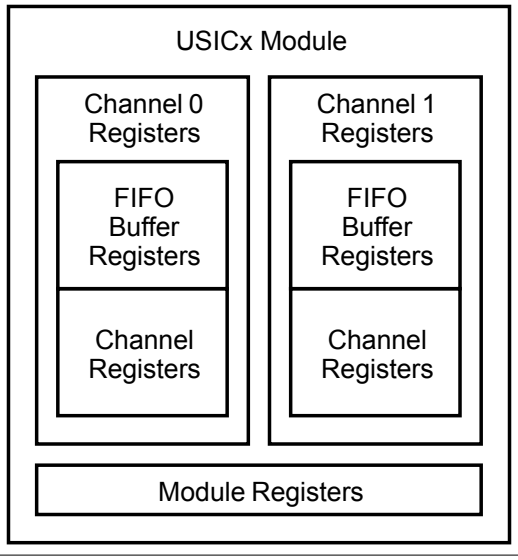


Figure 117 USIC Module and Channel Registers

Table 217 USIC Kernel-Related and Kernel Registers

Register Short Name	Register Long Name	Offset Addr.	Access Mode		Description see
			Read	Write	
Module Registers[38]					
ID	Module Identification Register	008_H	U, PV	U, PV	Page 443
Channel Registers					
–	reserved	000_H	BE	BE	–
CCFG	Channel Configuration Register	004_H	U, PV	U, PV	Page 446
KSCFG	Kernel State Configuration Register	$00C_H$	U, PV	U, PV	Page 447
FDR	Fractional Divider Register	010_H	U, PV	PV	Page 471
BRG	Baud Rate Generator Register	014_H	U, PV	PV	Page 472
INPR	Interrupt Node Pointer Register	018_H	U, PV	U, PV	Page 449
DX0CR	Input Control Register 0	$01C_H$	U, PV	U, PV	Page 467
DX1CR	Input Control Register 1	020_H	U, PV	U, PV	Page 469
DX2CR	Input Control Register 2	024_H	U, PV	U, PV	Page 467
DX3CR	Input Control Register 3	028_H	U, PV	U, PV	
DX4CR	Input Control Register 4	$02C_H$	U, PV	U, PV	
DX5CR	Input Control Register 5	030_H	U, PV	U, PV	
SCTR	Shift Control Register	034_H	U, PV	U, PV	Page 474
TCSR	Transmit Control/Status Register	038_H	U, PV	U, PV	Page 476
PCR	Protocol Control Register	$03C_H$	U, PV	U, PV	Page 450[39]
			U, PV	U, PV	Page 450[40]
			U, PV	U, PV	Page 453[41]
			U, PV	U, PV	Page 456[42]
CCR	Channel Control Register	040_H	U, PV	PV	Page 444
CMTR	Capture Mode Timer Register	044_H	U, PV	U, PV	Page 474
PSR	Protocol Status Register	048_H	U, PV	U, PV	Page 458[39]
			U, PV	U, PV	Page 459[40]
			U, PV	U, PV	Page 461[41]
			U, PV	U, PV	Page 463[42]
PSCR	Protocol Status Clear Register	$04C_H$	U, PV	U, PV	Page 466
RBUFSR	Receiver Buffer Status Register	050_H	U, PV	U, PV	Page 488

38 Details of the module identification registers are described in the implementation section (see page 443).
39 This page shows the general register layout.
40 This page shows the register layout in ASC mode.
41 This page shows the register layout in SSC mode.

Table 217 USIC Kernel-Related and Kernel Registers (continued)

Register Short Name	Register Long Name	Offset Addr.	Access Mode		Description see
			Read	Write	
RBUF	Receiver Buffer Register	054_H	U, PV	U, PV	Page 487
RBUFD	Receiver Buffer Register for Debugger	058_H	U, PV	U, PV	Page 488
RBUF0	Receiver Buffer Register 0	$05C_H$	U, PV	U, PV	Page 482
RBUF1	Receiver Buffer Register 1	060_H	U, PV	U, PV	Page 483
RBUF01SR	Receiver Buffer 01 Status Register	064_H	U, PV	U, PV	Page 483
FMR	Flag Modification Register	068_H	U, PV	U, PV	Page 481
–	reserved; do not access this location	$06C_H$	U, PV	BE	–
–	reserved	070_H - $07C_H$	BE	BE	–
TBUFx	Transmit Buffer Input Location x (x = 00-31)	080_H + x*4	U, PV	U, PV	Page 482
FIFO Buffer Registers					
BYP	Bypass Data Register	100_H	U, PV	U, PV	Page 489
BYPCR	Bypass Control Register	104_H	U, PV	U, PV	Page 490
TBCTR	Transmit Buffer Control Register	108_H	U, PV	U, PV	Page 496
RBCTR	Receive Buffer Control Register	$10C_H$	U, PV	U, PV	Page 499
TRBPTR	Transmit/Receive Buffer Pointer Register	110_H	U, PV	U, PV	Page 504
TRBSR	Transmit/Receive Buffer Status Register	114_H	U, PV	U, PV	Page 492
TRBSCR	Transmit/Receive Buffer Status Clear Register	118_H	U, PV	U, PV	Page 495
OUTR	Receive Buffer Output Register	$11C_H$	U, PV	U, PV	Page 502
OUTDR	Receive Buffer Output Register for Debugger	120_H	U, PV	U, PV	Page 503
–	reserved	124_H - $17C_H$	BE	BE	–
INx	Transmit FIFO Buffer Input Location x (x = 00-31)	180_H + x*4	U, PV	U, PV	Page 502

18.10.1 Address Map

The registers of the USIC communication channel are available at the following base addresses. The exact register address is given by the relative address of the register (given in *Table 217*) plus the channel base address (given in *Table 218*).

42 This page shows the register layout in IIC mode.
39 This page shows the general register layout.
40 This page shows the register layout in ASC mode.
41 This page shows the register layout in SSC mode.

Table 218 Registers Address Space

Module	Base Address	End Address	Note
USIC0_CH0	48000000_H	$480001FF_H$	–
USIC0_CH1	48000200_H	$480003FF_H$	–
USIC1_CH0	48004000_H	$480041FF_H$	–
USIC1_CH1	48004200_H	$480043FF_H$	–

Table 219 FIFO and Reserved Address Space

Module	Base Address	End Address	Access Mode		Note
			Read	Write	
USIC0	48000400_H	$480007FF_H$	nBE	nBE if in direct RAM test mode; otherwise BE	USIC0 RAM area, shared between USIC0_CH0 and USIC0_CH1
reserved	48000800_H	$48003FFF_H$	BE	BE	–
USIC1	48004400_H	$480047FF_H$	nBE	nBE if in direct RAM test mode; otherwise BE	USIC1 RAM area, shared between USIC1_CH0 and USIC1_CH1
reserved	48004800_H	$48007FFF_H$	BE	BE	–

18.10.2 Module Identification Registers

The module identification registers indicate the function and the design step of the USIC modules.

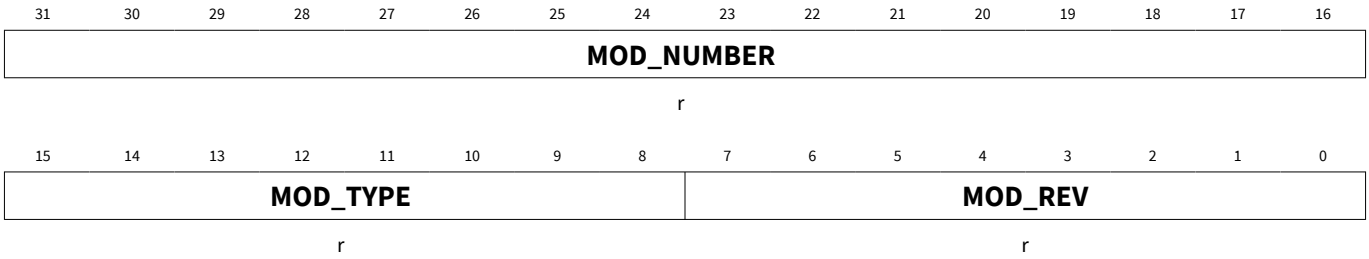
18.10.2.1 Register USIC0_ID / USIC1_ID

USIC0_ID Address: $4800\ 0008_H$

Module Identification Register Reset Value: $00AA\ C0XX_H$

USIC1_ID Address: $4800\ 4008_H$

Module Identification Register Reset Value: $00AA\ C0XX_H$



Field	Bits	Type	Description
MOD_REV	7:0	r	**Module Revision Number** MOD_REV defines the revision number. The value of a module revision starts with 01_H (first revision).

(continued)

Field	Bits	Type	Description
MOD_TYPE	15:8	r	**Module Type** This bit field is $C0_H$. It defines the module as a 32-bit module.
MOD_NUMBER	31:16	r	**Module Number Value** This bit field defines the USIC module identification number ($00AA_H$ = USIC).

18.10.3 Channel Control and Configuration Registers

18.10.3.1 Register CCR

The channel control register contains the enable/disable bits for hardware port control and interrupt generation on channel events, the control of the parity generation and the protocol selection of a USIC channel.

FDR can be written only with a privilege mode access.

CCR Address: 40_H

Channel Control Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															BRGIEN
r															rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AIEN	RIEN	TBIEN	TSIEN	DLIEN	RSIEN	PM		HPCEN		0		MODE			
rw	rw	rw	rw	rw	rw	rw		rw		r		rw			

Field	Bits	Type	Description
MODE	3:0	rw	**Operating Mode** This bit field selects the protocol for this USIC channel. Selecting a protocol that is not available (see register CCFG) or a reserved combination disables the USIC channel. When switching between two protocols, the USIC channel has to be disabled before selecting a new protocol. In this case, registers PCR and PSR have to be cleared or updated by software. 0_H The USIC channel is disabled. All protocol-related state machines are set to an idle state. 1_H The SSC (SPI) protocol is selected. 2_H The ASC (SCI, UART) protocol is selected. 4_H The IIC protocol is selected. Other bit combinations are reserved.

(continued)

Field	Bits	Type	Description
HPCEN	7:6	rw	**Hardware Port Control Enable** This bit enables the hardware port control for the specified set of DX[3:0] and DOUT[3:0] pins. 00_B The hardware port control is disabled. 01_B The hardware port control is enabled for DX0 and DOUT0. 10_B The hardware port control is enabled for DX3, DX0 and DOUT[1:0]. 11_B The hardware port control is enabled for DX0, DX[5:3] and DOUT[3:0]. *Note: The hardware port control feature is useful only for SSC protocols in half-duplex configurations, such as dual- and quad-SSC. For all other protocols HPCEN must always be written with 00_B.*
PM	9:8	rw	**Parity Mode** This bit field defines the parity generation of the sampled input values. 00_B The parity generation is disabled. 01_B Reserved 10_B Even parity is selected (parity bit = 1 on odd number of 1s in data, parity bit = 0 on even number of 1s in data). 11_B Odd parity is selected (parity bit = 0 on odd number of 1s in data, parity bit = 1 on even number of 1s in data).
RSIEN	10	rw	**Receiver Start Interrupt Enable** This bit enables the interrupt generation in case of a receiver start event. 0_B The receiver start interrupt is disabled. 1_B The receiver start interrupt is enabled. In case of a receiver start event, the service request output SRx indicated by INPR.TBINP is activated.
DLIEN	11	rw	**Data Lost Interrupt Enable** This bit enables the interrupt generation in case of a data lost event (data received in RBUFx while RDVx = 1). 0_B The data lost interrupt is disabled. 1_B The data lost interrupt is enabled. In case of a data lost event, the service request output SRx indicated by INPR.PINP is activated.
TSIEN	12	rw	**Transmit Shift Interrupt Enable** This bit enables the interrupt generation in case of a transmit shift event. 0_B The transmit shift interrupt is disabled. 1_B The transmit shift interrupt is enabled. In case of a transmit shift interrupt event, the service request output SRx indicated by INPR.TSINP is activated.

(continued)

Field	Bits	Type	Description
TBIEN	13	rw	**Transmit Buffer Interrupt Enable** This bit enables the interrupt generation in case of a transmit buffer event. 0_B The transmit buffer interrupt is disabled. 1_B The transmit buffer interrupt is enabled. In case of a transmit buffer event, the service request output SRx indicated by INPR.TBINP is activated.
RIEN	14	rw	**Receive Interrupt Enable** This bit enables the interrupt generation in case of a receive event. 0_B The receive interrupt is disabled. 1_B The receive interrupt is enabled. In case of a receive event, the service request output SRx indicated by INPR.RINP is activated.
AIEN	15	rw	**Alternative Receive Interrupt Enable** This bit enables the interrupt generation in case of a alternative receive event. 0_B The alternative receive interrupt is disabled. 1_B The alternative receive interrupt is enabled. In case of an alternative receive event, the service request output SRx indicated by INPR.AINP is activated.
BRGIEN	16	rw	**Baud Rate Generator Interrupt Enable** This bit enables the interrupt generation in case of a baud rate generator event. 0_B The baud rate generator interrupt is disabled. 1_B The baud rate generator interrupt is enabled. In case of a baud rate generator event, the service request output SRx indicated by INPR.PINP is activated.
0	5:4, 31:17	r	**Reserved** Read as 0; should be written with 0.

18.10.3.2 Register CCFG

The channel configuration register contains indicates the functionality that is available in the USIC channel.

CCFG Address: 04_H

Channel Configuration Register Reset Value: $0000\ 80CF_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0							TB	RB	0		1	IIC	ASC	SSC
r	r							r	r	r		r	r	r	r

Field	Bits	Type	Description
SSC	0	r	**SSC Protocol Available** This bit indicates if the SSC protocol is available. 0_B The SSC protocol is not available. 1_B The SSC protocol is available.
ASC	1	r	**ASC Protocol Available** This bit indicates if the ASC protocol is available. 0_B The ASC protocol is not available. 1_B The ASC protocol is available.
IIC	2	r	**IIC Protocol Available** This bit indicates if the IIC functionality is available. 0_B The IIC protocol is not available. 1_B The IIC protocol is available.
RB	6	r	**Receive FIFO Buffer Available** This bit indicates if an additional receive FIFO buffer is available. 0_B A receive FIFO buffer is not available. 1_B A receive FIFO buffer is available.
TB	7	r	**Transmit FIFO Buffer Available** This bit indicates if an additional transmit FIFO buffer is available. 0_B A transmit FIFO buffer is not available. 1_B A transmit FIFO buffer is available.
1	3, 15	r	**Reserved** Read as 1; should be written with 1.
0	5:4, 14:8, 31:16	r	**Reserved** Read as 0; should be written with 0.

18.10.3.3 Register KSCFG

The kernel state configuration register KSCFG allows the selection of the desired kernel modes for the different device operating modes.

KSCFG Address: $0C_H$

Kernel State Configuration Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				BPSUM	0	SUMCFG		BPNOM	0	NOMCFG		0		BPMODEN	MODEN
r				w	r	rw		w	r	rw		r		w	rw

Field	Bits	Type	Description
MODEN	0	rw	**Module Enable** This bit enables the module kernel clock and the module functionality. 0_B The module is switched off immediately (without respecting a stop condition). It does not react on mode control actions and the module clock is switched off. The module does not react on read accesses and ignores write accesses (except to KSCFG). 1_B The module is switched on and can operate. After writing 1 to MODEN, it is recommended to read register KSCFG to avoid pipeline effects in the control block before accessing other USIC registers.
BPMODEN	1	w	**Bit Protection for MODEN** This bit enables the write access to the bit MODEN. It always reads 0. 0_B MODEN is not changed. 1_B MODEN is updated with the written value.
NOMCFG	5:4	rw	**Normal Operation Mode Configuration** This bit field defines the kernel mode applied in normal operation mode. 00_B Run mode 0 is selected. 01_B Run mode 1 is selected. 10_B Stop mode 0 is selected. 11_B Stop mode 1 is selected.
BPNOM	7	w	**Bit Protection for NOMCFG** This bit enables the write access to the bit field NOMCFG. It always reads 0. 0_B NOMCFG is not changed. 1_B NOMCFG is updated with the written value.
SUMCFG	9:8	rw	**Suspend Mode Configuration** This bit field defines the kernel mode applied in suspend mode. Coding like NOMCFG.
BPSUM	11	w	**Bit Protection for SUMCFG** This bit enables the write access to the bit field SUMCFG. It always reads 0. 0_B SUMCFG is not changed. 1_B SUMCFG is updated with the written value.
0	3:2, 6, 10, 31:12	r	**Reserved** Read as 0; should be written with 0. Bit 2 can read as 1 after BootROM exit (but can be ignored).

18.10.3.4 Register INPR

The interrupt node pointer register defines the service request output SRx that is activated if the corresponding event occurs and interrupt generation is enabled.

INPR Address: 18_H

Interrupt Node Pointer Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0													PINP		
r													rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	AINP			0	RINP			0	TBINP			0	TSINP		
r	rw			r	rw			r	rw			r	rw		

Field	Bits	Type	Description
TSINP	2:0	rw	**Transmit Shift Interrupt Node Pointer** This bit field defines which service request output SRx becomes activated in case of a transmit shift interrupt. 000_B Output SR0 becomes activated. 001_B Output SR1 becomes activated. 010_B Output SR2 becomes activated. 011_B Output SR3 becomes activated. 100_B Output SR4 becomes activated. 101_B Output SR5 becomes activated. *Note: All other settings of the bit field are reserved.*
TBINP	6:4	rw	**Transmit Buffer Interrupt Node Pointer** This bit field defines which service request output SRx will be activated in case of a transmit buffer interrupt or a receive start interrupt. Coding like TSINP.
RINP	10:8	rw	**Receive Interrupt Node Pointer** This bit field defines which service request output SRx will be activated in case of a receive interrupt. Coding like TSINP.
AINP	14:12	rw	**Alternative Receive Interrupt Node Pointer** This bit field defines which service request output SRx will be activated in case of a alternative receive interrupt. Coding like TSINP.
PINP	18:16	rw	**Protocol Interrupt Node Pointer** This bit field defines which service request output SRx becomes activated in case of a protocol interrupt. Coding like TSINP.
0	3, 7, 11, 15, 31:19	r	**Reserved** Read as 0; should be written with 0.

18.10.4 Protocol Related Registers

18.10.4.1 Protocol Control Register

The bits in the protocol control register define protocol-specific functions. They have to be configured by software before enabling a new protocol. Only the bits used for the selected protocol are taken into account, whereas the other bit positions always read as 0. The protocol-specific meaning is described in the next four sections.

18.10.4.1.1 Register PCR

PCR Address: $3C_H$

Protocol Control Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CTR31	**CTR30**	**CTR29**	**CTR28**	**CTR27**	**CTR26**	**CTR25**	**CTR24**	**CTR23**	**CTR22**	**CTR21**	**CTR20**	**CTR19**	**CTR18**	**CTR17**	**CTR16**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CTR15	**CTR14**	**CTR13**	**CTR12**	**CTR11**	**CTR10**	**CTR9**	**CTR8**	**CTR7**	**CTR6**	**CTR5**	**CTR4**	**CTR3**	**CTR2**	**CTR1**	**CTR0**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
CTRx (x=0-31)	x	rw	**Protocol Control Bit x** This bit is a protocol control bit.

18.10.4.1.2 Register PCR [ASC Mode]

In ASC mode, the PCR register bits or bit fields are defined as described in this section.

PCR Address: $3C_H$

Protocol Control Register [ASC Mode] Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MCLK	**0**													**TSTEN**	**RSTEN**
rw	r													rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PL			**SP**					**FFIEN**	**FEIEN**	**RNIEN**	**CDEN**	**SBIEN**	**IDM**	**STPB**	**SMD**
rw			rw					rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
SMD	0	rw	**Sample Mode** This bit field defines the sample mode of the ASC receiver. The selected data input signal can be sampled only once per bit time or three times (in consecutive time quanta). When sampling three times, the bit value shifted in the receiver shift register is given by a majority decision among the three sampled values. 0_B Only one sample is taken per bit time. The current input value is sampled. 1_B Three samples are taken per bit time and a majority decision is made.
STPB	1	rw	**Stop Bits** This bit defines the number of stop bits in an ASC frame. 0_B The number of stop bits is 1. 1_B The number of stop bits is 2.
IDM	2	rw	**Idle Detection Mode** This bit defines if the idle detection is switched off or based on the frame length. 0_B The bus idle detection is switched off and bits PSR.TXIDLE and PSR.RXIDLE are set automatically to enable data transfers without checking the inputs before. 1_B The bus is considered as idle after a number of consecutive passive bit times defined by SCTR.FLE plus 2 (in the case without parity bit) or plus 3 (in the case with parity bit).
SBIEN	3	rw	**Synchronization Break Interrupt Enable** This bit enables the generation of a protocol interrupt if a synchronization break is detected. The automatic detection is always active, so bit SBD can be set independently of SBIEN. 0_B The interrupt generation is disabled. 1_B The interrupt generation is enabled.
CDEN	4	rw	**Collision Detection Enable** This bit enables the reaction of a transmitter to the collision detection. 0_B The collision detection is disabled. 1_B If a collision is detected, the transmitter stops its data transmission, outputs a 1, sets bit PSR.COL and generates a protocol interrupt. In order to allow data transmission again, PSR.COL has to be cleared by software.
RNIEN	5	rw	**Receiver Noise Detection Interrupt Enable** This bit enables the generation of a protocol interrupt if receiver noise is detected. The automatic detection is always active, so bit PSR.RNS can be set independently of PCR.RNIEN. 0_B The interrupt generation is disabled. 1_B The interrupt generation is enabled.

(continued)

Field	Bits	Type	Description
FEIEN	6	rw	**Format Error Interrupt Enable** This bit enables the generation of a protocol interrupt if a format error is detected. The automatic detection is always active, so bits PSR.FER0/FER1 can be set independently of PCR.FEIEN. 0_B The interrupt generation is disabled. 1_B The interrupt generation is enabled.
FFIEN	7	rw	**Frame Finished Interrupt Enable** This bit enables the generation of a protocol interrupt if the receiver or the transmitter reach the end of a frame. The automatic detection is always active, so bits PSR.RFF or PSR.TFF can be set independently of PCR.FFIEN. 0_B The interrupt generation is disabled. 1_B The interrupt generation is enabled.
SP	12:8	rw	**Sample Point** This bit field defines the sample point of the bit value. The sample point must not be located outside the programmed bit timing (PCR.SP ≤ BRG.DCTQ).
PL	15:13	rw	**Pulse Length** This bit field defines the length of a 0 data bit, counted in time quanta, starting with the time quantum 0 of each bit time. Each bit value that is a 0 can lead to a 0 pulse that is shorter than a bit time, e.g. for IrDA applications. The length of a bit time is not changed by PL, only the length of the 0 at the output signal. The pulse length must not be longer than the programmed bit timing (PCR.PL ≤ BRG.DCTQ). This bit field is only taken into account by the transmitter and is ignored by the receiver. 000_B The pulse length is equal to the bit length (no shortened 0). 001_B The pulse length of a 0 bit is 2 time quanta. 010_B The pulse length of a 0 bit is 3 time quanta. ...
RSTEN	16	rw	**Receiver Status Enable** This bit enables the modification of flag PSR[9] = BUSY according to the receiver status. 0_B Flag PSR[9] is not modified depending on the receiver status. 1_B Flag PSR[9] is set during the complete reception of a frame.
TSTEN	17	rw	**Transmitter Status Enable** This bit enables the modification of flag PSR[9] = BUSY according to the transmitter status. 0_B Flag PSR[9] is not modified depending on the transmitter status. 1_B Flag PSR[9] is set during the complete transmission of a frame.

(continued)

Field	Bits	Type	Description
MCLK	31	rw	**Master Clock Enable** This bit enables the generation of the master clock MCLK. 0_B The MCLK generation is disabled and the MCLK signal is 0. 1_B The MCLK generation is enabled.
0	30:18	r	**Reserved** Returns 0 if read; should be written with 0.

18.10.4.1.3 Register PCR [SSC Mode]

In SSC mode, the PCR register bits or bit fields are defined as described in this section.

PCR Address: $3C_H$

Protocol Control Register [SSC Mode] Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MCLK	**0**					**SLP HSEL**	**TIWE N**	**SELO**							
rw	rw					rw	rw	rw							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DX2TI EN	**MSL SIEN**	**PARI EN**	**DCTQ1**					**PCTQ1**		**CTQSEL1**		**FEM**	**SELI NV**	**SELC TR**	**MSL SEN**
rw	rw	rw	rw					rw		rw		rw	rw	rw	rw

Field	Bits	Type	Description
MSLSEN	0	rw	**MSLS Enable** This bit enables/disables the generation of the master slave select signal MSLS. If the SSC is a transfer slave, the SLS information is read from a pin and the internal generation is not needed. If the SSC is a transfer master, it has to provide the MSLS signal. 0_B The MSLS generation is disabled (MSLS = 0). This is the setting for SSC slave mode. 1_B The MSLS generation is enabled. This is the setting for SSC master mode.
SELCTR	1	rw	**Select Control** This bit selects the operating mode for the SELO[7:0] outputs. 0_B The coded select mode is enabled. 1_B The direct select mode is enabled.

(continued)

Field	Bits	Type	Description
SELINV	2	rw	**Select Inversion** This bit defines if the polarity of the SELO[7:0] outputs in relation to the master slave select signal MSLS. 0_B The SELO outputs have the same polarity as the MSLS signal (active high). 1_B The SELO outputs have the inverted polarity to the MSLS signal (active low).
FEM	3	rw	**Frame End Mode** This bit defines if a transmit buffer content that is not valid for transmission is considered as an end of frame condition for the slave select generation. 0_B The current data frame is considered as finished when the last bit of a data word has been sent out and the transmit buffer TBUF does not contain new data (TDV = 0). 1_B The MSLS signal is kept active also while no new data is available and no other end of frame condition is reached. In this case, the software can accept delays in delivering the data without automatic deactivation of MSLS in multi-word data frames.
CTQSEL1	5:4	rw	**Input Frequency Selection** This bit field defines the input frequency f_{CTQIN} for the generation of the slave select delays T_{iw} and T_{nf}. 00_B $f_{CTQIN} = f_{PDIV}$ 01_B $f_{CTQIN} = f_{PPP}$ 10_B $f_{CTQIN} = f_{SCLK}$ 11_B $f_{CTQIN} = f_{MCLK}$
PCTQ1	7:6	rw	**Divider Factor PCTQ1 for T_{iw} and T_{nf}** This bit field represents the divider factor PCTQ1 (range = 0 - 3) for the generation of the inter-word delay and the next-frame delay. $T_{iw} = T_{nf} = 1/f_{CTQIN} \times (PCTQ1 + 1) \times (DCTQ1 + 1)$
DCTQ1	12:8	rw	**Divider Factor DCTQ1 for T_{iw} and T_{nf}** This bit field represents the divider factor DCTQ1 (range = 0 - 31) for the generation of the inter-word delay and the next-frame delay. $T_{iw} = T_{nf} = 1/f_{CTQIN} \times (PCTQ1 + 1) \times (DCTQ1 + 1)$
PARIEN	13	rw	**Parity Error Interrupt Enable** This bit enables/disables the generation of a protocol interrupt with the detection of a parity error. 0_B A protocol interrupt is not generated with the detection of a parity error. 1_B A protocol interrupt is generated with the detection of a parity error.

(continued)

Field	Bits	Type	Description
MSLSIEN	14	rw	**MSLS Interrupt Enable** This bit enables/disables the generation of a protocol interrupt if the state of the MSLS signal changes (indicated by PSR.MSLSEV = 1). 0_B A protocol interrupt is not generated if a change of signal MSLS is detected. 1_B A protocol interrupt is generated if a change of signal MSLS is detected.
DX2TIEN	15	rw	**DX2T Interrupt Enable** This bit enables/disables the generation of a protocol interrupt if the DX2T signal becomes activated (indicated by PSR.DX2TEV = 1). 0_B A protocol interrupt is not generated if DX2T is activated. 1_B A protocol interrupt is generated if DX2T is activated.
SELO	23:16	rw	**Select Output** This bit field defines the setting of the SELO[7:0] output lines. 0_B The corresponding SELOx line cannot be activated. 1_B The corresponding SELOx line can be activated (according to the mode selected by SELCTR).
TIWEN	24	rw	**Enable Inter-Word Delay T_{iw}** This bit enables/disables the inter-word delay T_{iw} after the transmission of a data word. 0_B No delay between data words of the same frame. 1_B The inter-word delay T_{iw} is enabled and introduced between data words of the same frame.
SLPHSEL	25	rw	**Slave Mode Clock Phase Select** This bit selects the clock phase for the data shifting in slave mode. 0_B Data bits are shifted out with the leading edge of the shift clock signal and latched in with the trailing edge. 1_B The first data bit is shifted out when the data shift unit receives a low to high transition from the DX2 stage. Subsequent bits are shifted out with the trailing edge of the shift clock signal. Data bits are always latched in with the leading edge.
MCLK	31	rw	**Master Clock Enable** This bit enables/disables the generation of the master clock output signal MCLK, independent from master or slave mode. 0_B The MCLK generation is disabled and output MCLK = 0. 1_B The MCLK generation is enabled.
0	30:26	rw	**Reserved** Returns 0 if read; should be written with 0.

18.10.4.1.4 Register PCR [IIC Mode]

In IIC mode, the PCR register bits or bit fields are defined as described in this section.

PCR Address: $3C_H$

Protocol Control Register [IIC Mode] Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MCLK	**ACKIEN**	**HDEL**				**SACKDIS**	**ERRIEN**	**SRRIEN**	**ARLIEN**	**NACKIEN**	**PCRIEN**	**RSCRIEN**	**SCRIEN**	**STIM**	**ACK00**
rw	rw	rw				rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SLAD															
rw															

Field	Bits	Type	Description
SLAD	15:0	rw	**Slave Address** This bit field contains the programmed slave address. The corresponding bits in the first received address byte are compared to the bits SLAD[15:9] to check for address match. If SLAD[15:11] = 11110_B, then the second address byte is also compared to SLAD[7:0].
ACK00	16	rw	**Acknowledge 00_H** This bit defines if a slave device should be sensitive to the slave address 00_H. 0_B The slave device is not sensitive to this address. 1_B The slave device is sensitive to this address.
STIM	17	rw	**Symbol Timing** This bit defines how many time quanta are used in a symbol. 0_B A symbol contains 10 time quanta. The timing is adapted for standard mode (100 kBaud). 1_B A symbol contains 25 time quanta. The timing is adapted for fast mode (400 kBaud).
SCRIEN	18	rw	**Start Condition Received Interrupt Enable** This bit enables the generation of a protocol interrupt if a start condition is detected. 0_B The start condition interrupt is disabled. 1_B The start condition interrupt is enabled.
RSCRIEN	19	rw	**Repeated Start Condition Received Interrupt Enable** This bit enables the generation of a protocol interrupt if a repeated start condition is detected. 0_B The repeated start condition interrupt is disabled. 1_B The repeated start condition interrupt is enabled.
PCRIEN	20	rw	**Stop Condition Received Interrupt Enable** This bit enables the generation of a protocol interrupt if a stop condition is detected. 0_B The stop condition interrupt is disabled. 1_B The stop condition interrupt is enabled.

(continued)

Field	Bits	Type	Description
NACKIEN	21	rw	**Non-Acknowledge Interrupt Enable** This bit enables the generation of a protocol interrupt if a non-acknowledge is detected by a master. 0_B The non-acknowledge interrupt is disabled. 1_B The non-acknowledge interrupt is enabled.
ARLIEN	22	rw	**Arbitration Lost Interrupt Enable** This bit enables the generation of a protocol interrupt if an arbitration lost event is detected. 0_B The arbitration lost interrupt is disabled. 1_B The arbitration lost interrupt is enabled.
SRRIEN	23	rw	**Slave Read Request Interrupt Enable** This bit enables the generation of a protocol interrupt if a slave read request is detected. 0_B The slave read request interrupt is disabled. 1_B The slave read request interrupt is enabled.
ERRIEN	24	rw	**Error Interrupt Enable** This bit enables the generation of a protocol interrupt if an IIC error condition is detected (indicated by PSR.ERR or PSR.WTDF). 0_B The error interrupt is disabled. 1_B The error interrupt is enabled.
SACKDIS	25	rw	**Slave Acknowledge Disable** This bit disables the generation of an active acknowledge signal for a slave device (active acknowledge = 0 level). Once set by software, it is automatically cleared with each (repeated) start condition. If this bit is set after a byte has been received (indicated by an interrupt) but before the next acknowledge bit has started, the next acknowledge bit will be sent with passive level. This would indicate that the receiver does not accept more bytes. As a result, a minimum of 2 bytes will be received if the first receive interrupt is used to set this bit. 0_B The generation of an active slave acknowledge is enabled (slave acknowledge with 0 level = more bytes can be received). 1_B The generation of an active slave acknowledge is disabled (slave acknowledge with 1 level = reception stopped).
HDEL	29:26	rw	**Hardware Delay** This bit field defines the delay used to compensate the internal treatment of the SCL signal (see ***Symbol Timing*** on page 418) in order to respect the SDA hold time specified for the IIC protocol.
ACKIEN	30	rw	**Acknowledge Interrupt Enable** This bit enables the generation of a protocol interrupt if an acknowledge is detected by a master. 0_B The acknowledge interrupt is disabled. 1_B The acknowledge interrupt is enabled.

(continued)

Field	Bits	Type	Description
MCLK	31	rw	**Master Clock Enable** This bit enables generation of the master clock MCLK (not directly used for IIC protocol, can be used as general frequency output). 0_B The MCLK generation is disabled and MCLK is 0. 1_B The MCLK generation is enabled.

18.10.4.2 Protocol Status Register

The flags in the protocol status register can be cleared by writing a 1 to the corresponding bit position in register PSCR. Writing a 1 to a bit position in PSR sets the corresponding flag, but does not lead to further actions (no interrupt generation). Writing a 0 has no effect. These flags should be cleared by software before enabling a new protocol. The protocol-specific meaning is described in the next four sections.

18.10.4.2.1 Register PSR

PSR Address: 48_H

Protocol Status Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															BRGIF
r															rwh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AIF	RIF	TBIF	TSIF	DLIF	RSIF	ST9	ST8	ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
STx (x=0-9)	x	rwh	**Protocol Status Flag x** See protocol specific description.
RSIF	10	rwh	**Receiver Start Indication Flag** 0_B A receiver start event has not occurred. 1_B A receiver start event has occurred.
DLIF	11	rwh	**Data Lost Indication Flag** 0_B A data lost event has not occurred. 1_B A data lost event has occurred.
TSIF	12	rwh	**Transmit Shift Indication Flag** 0_B A transmit shift event has not occurred. 1_B A transmit shift event has occurred.
TBIF	13	rwh	**Transmit Buffer Indication Flag** 0_B A transmit buffer event has not occurred. 1_B A transmit buffer event has occurred.

(continued)

Field	Bits	Type	Description
RIF	14	rwh	**Receive Indication Flag** 0_B A receive event has not occurred. 1_B A receive event has occurred.
AIF	15	rwh	**Alternative Receive Indication Flag** 0_B An alternative receive event has not occurred. 1_B An alternative receive event has occurred.
BRGIF	16	rwh	**Baud Rate Generator Indication Flag** 0_B A baud rate generator event has not occurred. 1_B A baud rate generator event has occurred.
0	31:17	r	**Reserved;** read as 0; should be written with 0;

18.10.4.2.2 Register PSR [ASC Mode]

In ASC mode, the PSR register bits or bit fields are defined as described in this section.

PSR Address: 48_H

Protocol Status Register [ASC Mode] Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															BRGIF
r															rwh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AIF	RIF	TBIF	TSIF	DLIF	RSIF	BUSY	TFF	RFF	FER1	FER0	RNS	COL	SBD	RXIDLE	TXIDLE
rwh	rwh	rwh	rwh	rwh	rwh	r	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
TXIDLE	0	rwh	**Transmission Idle** This bit shows if the transmit line (DX1) has been idle. A frame transmission can only be started if TXIDLE is set. 0_B The transmitter line has not yet been idle. 1_B The transmitter line has been idle and frame transmission is possible.
RXIDLE	1	rwh	**Reception Idle** This bit shows if the receive line (DX0) has been idle. A frame reception can only be started if RXIDLE is set. 0_B The receiver line has not yet been idle. 1_B The receiver line has been idle and frame reception is possible.

(continued)

Field	Bits	Type	Description
SBD	2	rwh	**Synchronization Break Detected**[43] This bit is set if a programmed number of consecutive bit values with level 0 has been detected (called synchronization break, e.g. in a LIN bus system). 0_B A synchronization break has not yet been detected. 1_B A synchronization break has been detected.
COL	3	rwh	**Collision Detected**[43] This bit is set if a collision has been detected (with PCR.CDEN = 1). 0_B A collision has not yet been detected and frame transmission is possible. 1_B A collision has been detected and frame transmission is not possible.
RNS	4	rwh	**Receiver Noise Detected**[43] This bit is set if receiver noise has been detected. 0_B Receiver noise has not been detected. 1_B Receiver noise has been detected.
FER0	5	rwh	**Format Error in Stop Bit 0**[43] This bit is set if a 0 has been sampled in the stop bit 0 (called format error 0). 0_B A format error 0 has not been detected. 1_B A format error 0 has been detected.
FER1	6	rwh	**Format Error in Stop Bit 1**[43] This bit is set if a 0 has been sampled in the stop bit 1 (called format error 1). 0_B A format error 1 has not been detected. 1_B A format error 1 has been detected.
RFF	7	rwh	**Receive Frame Finished**[43] This bit is set if the receiver has finished the last stop bit. 0_B The received frame is not yet finished. 1_B The received frame is finished.
TFF	8	rwh	**Transmitter Frame Finished**[43] This bit is set if the transmitter has finished the last stop bit. 0_B The transmitter frame is not yet finished. 1_B The transmitter frame is finished.
BUSY	9	r	**Transfer Status BUSY** This bit indicates the receiver status (if PCR.RSTEN = 1) or the transmitter status (if PCR.TSTEN = 1) or the logical OR combination of both (if PCR.RSTEN = PCR.TSTEN = 1). 0_B A data transfer does not take place. 1_B A data transfer currently takes place.

43 This status bit can generate a protocol interrupt (see ***Protocol-specific Events and Interrupts*** on page 439). The general interrupt status flags are described in the general interrupt chapter.

(continued)

Field	Bits	Type	Description
RSIF	10	rwh	**Receiver Start Indication Flag** 0_B A receiver start event has not occurred. 1_B A receiver start event has occurred.
DLIF	11	rwh	**Data Lost Indication Flag** 0_B A data lost event has not occurred. 1_B A data lost event has occurred.
TSIF	12	rwh	**Transmit Shift Indication Flag** 0_B A transmit shift event has not occurred. 1_B A transmit shift event has occurred.
TBIF	13	rwh	**Transmit Buffer Indication Flag** 0_B A transmit buffer event has not occurred. 1_B A transmit buffer event has occurred.
RIF	14	rwh	**Receive Indication Flag** 0_B A receive event has not occurred. 1_B A receive event has occurred.
AIF	15	rwh	**Alternative Receive Indication Flag** 0_B An alternative receive event has not occurred. 1_B An alternative receive event has occurred.
BRGIF	16	rwh	**Baud Rate Generator Indication Flag** 0_B A baud rate generator event has not occurred. 1_B A baud rate generator event has occurred.
0	31:17	r	**Reserved** Returns 0 if read; should be written with 0.

18.10.4.2.3 Register PSR [SSC Mode]

In SSC mode, the PSR register bits or bit fields are defined as described in this section.

PSR Address: 48_H

Protocol Status Register [SSC Mode] Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															BRGIF
r															rwh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AIF	RIF	TBIF	TSIF	DLIF	RSIF	0					PARERR	DX2TEV	MSLSEV	DX2S	MSLS
rwh	rwh	rwh	rwh	rwh	rwh	r					rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
MSLS	0	rwh	**MSLS Status** This bit indicates the current status of the MSLS signal. It must be cleared by software to stop a running frame. 0_B The internal signal MSLS is inactive (0). 1_B The internal signal MSLS is active (1).
DX2S	1	rwh	**DX2S Status** This bit indicates the current status of the DX2S signal that can be used as slave select input SELIN. 0_B DX2S is 0. 1_B DX2S is 1.
MSLSEV	2	rwh	**MSLS Event Detected**[44] This bit indicates that the MSLS signal has changed its state since MSLSEV has been cleared. Together with the MSLS status bit, the activation/deactivation of the MSLS signal can be monitored. 0_B The MSLS signal has not changed its state. 1_B The MSLS signal has changed its state.
DX2TEV	3	rwh	**DX2T Event Detected**[44] This bit indicates that the DX2T trigger signal has been activated since DX2TEV has been cleared. 0_B The DX2T signal has not been activated. 1_B The DX2T signal has been activated.
PARERR	4	rwh	**Parity Error Event Detected**[44] This bit indicates that there is a mismatch in the received parity bit (in RBUFSR.PAR) with the calculated parity bit of the last received word of the data frame. 0_B A parity error event has not been activated. 1_B A parity error event has been activated.
RSIF	10	rwh	**Receiver Start Indication Flag** 0_B A receiver start event has not occurred. 1_B A receiver start event has occurred.
DLIF	11	rwh	**Data Lost Indication Flag** 0_B A data lost event has not occurred. 1_B A data lost event has occurred.
TSIF	12	rwh	**Transmit Shift Indication Flag** 0_B A transmit shift event has not occurred. 1_B A transmit shift event has occurred.
TBIF	13	rwh	**Transmit Buffer Indication Flag** 0_B A transmit buffer event has not occurred. 1_B A transmit buffer event has occurred.

44 This status bit can generate a protocol interrupt in SSC mode (see ***Protocol-specific Events and Interrupts*** on page 439). The general interrupt status flags are described in the general interrupt chapter.

(continued)

Field	Bits	Type	Description
RIF	14	rwh	**Receive Indication Flag** 0_B A receive event has not occurred. 1_B A receive event has occurred.
AIF	15	rwh	**Alternative Receive Indication Flag** 0_B An alternative receive event has not occurred. 1_B An alternative receive event has occurred.
BRGIF	16	rwh	**Baud Rate Generator Indication Flag** 0_B A baud rate generator event has not occurred. 1_B A baud rate generator event has occurred.
0	9:5, 31:17	r	**Reserved** Returns 0 if read; not modified in SSC mode.

18.10.4.2.4 Register PSR [IIC Mode]

The following PSR status bits or bit fields are available in IIC mode.

PSR Address: 48_H

Protocol Status Register [IIC Mode] Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															BRGIF
r															rwh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AIF	RIF	TBIF	TSIF	DLIF	RSIF	ACK	ERR	SRR	ARL	NACK	PCR	RSCR	SCR	WTDF	SLSEL
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
SLSEL	0	rwh	**Slave Select** This bit indicates that this device has been selected as slave. 0_B The device is not selected as slave. 1_B The device is selected as slave.
WTDF	1	rwh	**Wrong TDF Code Found**[45] This bit indicates that an unexpected/wrong TDF code has been found. A protocol interrupt can be generated if PCR.ERRIEN = 1. 0_B A wrong TDF code has not been found. 1_B A wrong TDF code has been found.

45 This status bit can generate a protocol interrupt (see ***Protocol-specific Events and Interrupts*** on page 439). The general interrupt status flags are described in the general interrupt chapter.

(continued)

Field	Bits	Type	Description
SCR	2	rwh	**Start Condition Received**[45] This bit indicates that a start condition has been detected on the IIC bus lines.A protocol interrupt can be generated if PCR.SCRIEN = 1. 0_B A start condition has not yet been detected. 1_B A start condition has been detected.
RSCR	3	rwh	**Repeated Start Condition Received**[45] This bit indicates that a repeated start condition has been detected on the IIC bus lines. A protocol interrupt can be generated if PCR.RSCRIEN = 1. 0_B A repeated start condition has not yet been detected. 1_B A repeated start condition has been detected.
PCR	4	rwh	**Stop Condition Received**[45] This bit indicates that a stop condition has been detected on the IIC bus lines. A protocol interrupt can be generated if PCR.PCRIEN = 1. 0_B A stop condition has not yet been detected. 1_B A stop condition has been detected.
NACK	5	rwh	**Non-Acknowledge Received**[45] This bit indicates that a non-acknowledge has been received in master mode. This bit is not set in slave mode. A protocol interrupt can be generated if PCR.NACKIEN = 1. 0_B A non-acknowledge has not been received. 1_B A non-acknowledge has been received.
ARL	6	rwh	**Arbitration Lost**[45] This bit indicates that an arbitration has been lost. A protocol interrupt can be generated if PCR.ARLIEN = 1. 0_B An arbitration has not been lost. 1_B An arbitration has been lost.
SRR	7	rwh	**Slave Read Request**[45] This bit indicates that a slave read request has been detected. It becomes active to request the first data byte to be made available in the transmit buffer. For further consecutive data bytes, the transmit buffer issues more interrupts. For the end of the transfer, the master transmitter sends a stop condition. A protocol interrupt can be generated if PCR.SRRIEN = 1. 0_B A slave read request has not been detected. 1_B A slave read request has been detected.

45 This status bit can generate a protocol interrupt (see ***Protocol-specific Events and Interrupts*** on page 439). The general interrupt status flags are described in the general interrupt chapter.

(continued)

Field	Bits	Type	Description
ERR	8	rwh	**Error**[45] This bit indicates that an IIC error (frame format or TDF code) has been detected. A protocol interrupt can be generated if PCR.ERRIEN = 1. 0_B An IIC error has not been detected. 1_B An IIC error has been detected.
ACK	9	rwh	**Acknowledge Received**[45] This bit indicates that an acknowledge has been received in master mode. This bit is not set in slave mode. A protocol interrupt can be generated if PCR.ACKIEN = 1. 0_B An acknowledge has not been received. 1_B An acknowledge has been received.
RSIF	10	rwh	**Receiver Start Indication Flag** 0_B A receiver start event has not occurred. 1_B A receiver start event has occurred.
DLIF	11	rwh	**Data Lost Indication Flag** 0_B A data lost event has not occurred. 1_B A data lost event has occurred.
TSIF	12	rwh	**Transmit Shift Indication Flag** 0_B A transmit shift event has not occurred. 1_B A transmit shift event has occurred.
TBIF	13	rwh	**Transmit Buffer Indication Flag** 0_B A transmit buffer event has not occurred. 1_B A transmit buffer event has occurred.
RIF	14	rwh	**Receive Indication Flag** 0_B A receive event has not occurred. 1_B A receive event has occurred.
AIF	15	rwh	**Alternative Receive Indication Flag** 0_B An alternative receive event has not occurred. 1_B An alternative receive event has occurred.
BRGIF	16	rwh	**Baud Rate Generator Indication Flag** 0_B A baud rate generator event has not occurred. 1_B A baud rate generator event has occurred.
0	31:17	r	**Reserved** Returns 0 if read; not modified in IIC mode.

18.10.4.2.5 Register PSCR

Read accesses to this register always deliver 0 at all bit positions.

45 This status bit can generate a protocol interrupt (see ***Protocol-specific Events and Interrupts*** on page 439). The general interrupt status flags are described in the general interrupt chapter.

PSCR Address: $4C_H$

Protocol Status Clear Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															CBRGIF
r															w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAIF	CRIF	CTBIF	CTSIF	CDLIF	CRSIF	CST9	CST8	CST7	CST6	CST5	CST4	CST3	CST2	CST1	CST0
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

Field	Bits	Type	Description
CSTx (x=0-9)	x	w	**Clear Status Flag x in PSR** 0_B No action 1_B Flag PSR.STx is cleared.
CRSIF	10	w	**Clear Receiver Start Indication Flag** 0_B No action 1_B Flag PSR.RSIF is cleared.
CDLIF	11	w	**Clear Data Lost Indication Flag** 0_B No action 1_B Flag PSR.DLIF is cleared.
CTSIF	12	w	**Clear Transmit Shift Indication Flag** 0_B No action 1_B Flag PSR.TSIF is cleared.
CTBIF	13	w	**Clear Transmit Buffer Indication Flag** 0_B No action 1_B Flag PSR.TBIF is cleared.
CRIF	14	w	**Clear Receive Indication Flag** 0_B No action 1_B Flag PSR.RIF is cleared.
CAIF	15	w	**Clear Alternative Receive Indication Flag** 0_B No action 1_B Flag PSR.AIF is cleared.
CBRGIF	16	w	**Clear Baud Rate Generator Indication Flag** 0_B No action 1_B Flag PSR.BRGIF is cleared.
0	31:17	r	**Reserved;** read as 0; should be written with 0;

18.10.5 Input Stage Register

18.10.5.1 Input Control Registers

The input control registers contain the bits to define the characteristics of the input stages (input stage DX0 is controlled by register DX0CR, etc.).

18.10.5.1.1 Register DX0CR, DX2CR, DX3CR, DX4CR, DX5CR

DX0CR	Address:	$1C_H$
Input Control Register 0	Reset Value:	$0000\ 0000_H$
DX2CR	Address:	24_H
Input Control Register 2	Reset Value:	$0000\ 0000_H$
DX3CR	Address:	28_H
Input Control Register 3	Reset Value:	$0000\ 0000_H$
DX4CR	Address:	$2C_H$
Input Control Register 4	Reset Value:	$0000\ 0000_H$
DX5CR	Address:	30_H
Input Control Register 5	Reset Value:	$0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DXS	**0**			**CM**		**SFSEL**	**DPOL**	**0**	**DSEN**	**DFEN**	**INSW**	**0**	**DSEL**		
rh	r			rw		rw	rw	r	rw	rw	rw	r	rw		

Field	Bits	Type	Description
DSEL	2:0	rw	**Data Selection for Input Signal** This bit field defines the input data signal for the corresponding input line for protocol pre-processor. The selection can be made from the input vector DXn[G:A]. 000_B The data input DXnA is selected. 001_B The data input DXnB is selected. 010_B The data input DXnC is selected. 011_B The data input DXnD is selected. 100_B The data input DXnE is selected. 101_B The data input DXnF is selected. 110_B The data input DXnG is selected. 111_B The data input is always 1.

(continued)

Field	Bits	Type	Description
INSW	4	rw	**Input Switch** This bit defines if the data shift unit input is derived from the input data path DXn or from the selected protocol pre-processors. 0_B The input of the data shift unit is controlled by the protocol pre-processor. 1_B The input of the data shift unit is connected to the selected data input line. This setting is used if the signals are directly derived from an input pin without treatment by the protocol pre-processor.
DFEN	5	rw	**Digital Filter Enable** This bit enables/disables the digital filter for signal DXnS. 0_B The input signal is not digitally filtered. 1_B The input signal is digitally filtered.
DSEN	6	rw	**Data Synchronization Enable** This bit selects if the asynchronous input signal or the synchronized (and optionally filtered) signal DXnS can be used as input for the data shift unit. 0_B The un-synchronized signal can be taken as input for the data shift unit. 1_B The synchronized signal can be taken as input for the data shift unit.
DPOL	8	rw	**Data Polarity for DXn** This bit defines the signal polarity of the input signal. 0_B The input signal is not inverted. 1_B The input signal is inverted.
SFSEL	9	rw	**Sampling Frequency Selection** This bit defines the sampling frequency of the digital filter for the synchronized signal DXnS. 0_B The sampling frequency is f_{PERIPH}. 1_B The sampling frequency is f_{FD}.
CM	11:10	rw	**Combination Mode** This bit field selects which edge of the synchronized (and optionally filtered) signal DXnS actives the trigger output DXnT of the input stage. 00_B The trigger activation is disabled. 01_B A rising edge activates DXnT. 10_B A falling edge activates DXnT. 11_B Both edges activate DXnT.
DXS	15	rh	**Synchronized Data Value** This bit indicates the value of the synchronized (and optionally filtered) input signal. 0_B The current value of DXnS is 0. 1_B The current value of DXnS is 1.

(continued)

Field	Bits	Type	Description
0	3, 7, 14:12, 31:16	r	**Reserved** Read as 0; should be written with 0.

18.10.5.1.2 Register DX1CR

DX1CR Address: 20_H

Input Control Register 1 Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DXS	**0**			**CM**		**SFSEL**	**DPOL**	**0**	**DSEN**	**DFEN**	**INSW**	**DCEN**	**DSEL**		
rh	r			rw		rw	rw	r	rw	rw	rw	rw	rw		

Field	Bits	Type	Description
DSEL	2:0	rw	**Data Selection for Input Signal** This bit field defines the input data signal for the corresponding input line for protocol pre-processor. The selection can be made from the input vector DX1[G:A]. 000_B The data input DX1A is selected. 001_B The data input DX1B is selected. 010_B The data input DX1C is selected. 011_B The data input DX1D is selected. 100_B The data input DX1E is selected. 101_B The data input DX1F is selected. 110_B The data input DX1G is selected. 111_B The data input is always 1.
DCEN	3	rw	**Delay Compensation Enable** This bit selects if the receive shift clock is controlled by INSW or derived from the input data path DX1. 0_B The receive shift clock is dependent on INSW selection. 1_B The receive shift clock is connected to the selected data input line. This setting is used if delay compensation is required in SSC and IIS protocols, else DCEN should always be 0.

(continued)

Field	Bits	Type	Description
INSW	4	rw	**Input Switch** This bit defines if the data shift unit input is derived from the input data path DX1 or from the selected protocol pre-processors. 0_B The input of the data shift unit is controlled by the protocol pre-processor. 1_B The input of the data shift unit is connected to the selected data input line. This setting is used if the signals are directly derived from an input pin without treatment by the protocol pre-processor.
DFEN	5	rw	**Digital Filter Enable** This bit enables/disables the digital filter for signal DX1S. 0_B The input signal is not digitally filtered. 1_B The input signal is digitally filtered.
DSEN	6	rw	**Data Synchronization Enable** This bit selects if the asynchronous input signal or the synchronized (and optionally filtered) signal DX1S can be used as input for the data shift unit. 0_B The un-synchronized signal can be taken as input for the data shift unit. 1_B The synchronized signal can be taken as input for the data shift unit.
DPOL	8	rw	**Data Polarity for DXn** This bit defines the signal polarity of the input signal. 0_B The input signal is not inverted. 1_B The input signal is inverted.
SFSEL	9	rw	**Sampling Frequency Selection** This bit defines the sampling frequency of the digital filter for the synchronized signal DX1S. 0_B The sampling frequency is f_{PERIPH}. 1_B The sampling frequency is f_{FD}.
CM	11:10	rw	**Combination Mode** This bit field selects which edge of the synchronized (and optionally filtered) signal DX1S actives the trigger output DX1T of the input stage. 00_B The trigger activation is disabled. 01_B A rising edge activates DX1T. 10_B A falling edge activates DX1T. 11_B Both edges activate DX1T.
DXS	15	rh	**Synchronized Data Value** This bit indicates the value of the synchronized (and optionally filtered) input signal. 0_B The current value of DX1S is 0. 1_B The current value of DX1S is 1.

(continued)

Field	Bits	Type	Description
0	7, 14:12, 31:16	r	**Reserved** Read as 0; should be written with 0.

18.10.6 Baud Rate Generator Registers

18.10.6.1 Register FDR

The fractional divider register FDR allows the generation of the internal frequency f_{FD}, that is derived from the system clock f_{PERIPH}.

FDR Address: 10_H

Fractional Divider Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0		**0**				**RESULT**									
rw		r				rh									

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DM		**0**				**STEP**									
rw		r				rw									

Field	Bits	Type	Description
STEP	9:0	rw	**Step Value** In normal divider mode STEP contains the reload value for RESULT after RESULT has reached $3FF_H$. In fractional divider mode STEP defines the value added to RESULT with each input clock cycle.
DM	15:14	rw	**Divider Mode** This bit fields defines the functionality of the fractional divider block. 00_B The divider is switched off, $f_{FD} = 0$. 01_B Normal divider mode selected. 10_B Fractional divider mode selected. 11_B The divider is switched off, $f_{FD} = 0$.
RESULT	25:16	rh	**Result Value** In normal divider mode this bit field is updated with f_{PERIPH} according to: RESULT = RESULT + 1 In fractional divider mode this bit field is updated with f_{PERIPH} according to: RESULT = RESULT + STEP If bit field DM is written with 01_B or 10_B, RESULT is loaded with a start value of $3FF_H$.
0	31:30	rw	**Reserved for Future Use** Must be written with 0 to allow correct fractional divider operation.

(continued)

Field	Bits	Type	Description
0	13:10, 29:26	r	**Reserved** Read as 0; should be written with 0.

18.10.6.2 Register BRG

The protocol-related counters for baud rate generation and timing measurement are controlled by the register BRG.

BRG Address: 14_H

Baud Rate Generator Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCLKCFG		MCLKCFG	SCLKOSEL	0		PDIV									
rw		rw	rw	r		rw									

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	DCTQ					PCTQ		CTQSEL		0	PPPEN	TMEN	0	CLKSEL	
r	rw					rw		rw		r	rw	rw	r	rw	

Field	Bits	Type	Description
CLKSEL	1:0	rw	**Clock Selection** This bit field defines the input frequency f_{PIN} 00_B The fractional divider frequency f_{FD} is selected. 01_B Reserved, no action 10_B The trigger signal DX1T defines f_{PIN}. Signal MCLK toggles with f_{PIN}. 11_B Signal MCLK corresponds to the DX1S signal and the frequency f_{PIN} is derived from the rising edges of DX1S.
TMEN	3	rw	**Timing Measurement Enable** This bit enables the timing measurement of the capture mode timer. 0_B Timing measurement is disabled: The trigger signals DX0T and DX1T are ignored. 1_B Timing measurement is enabled: The 10-bit counter is incremented by 1 with f_{PPP} and stops counting when reaching its maximum value. If one of the trigger signals DX0T or DX1T become active, the counter value is captured into bit field CTV, the counter is cleared and a transmit shift event is generated.
PPPEN	4	rw	**Enable 2:1 Divider for f_{PPP}** This bit defines the input frequency f_{PPP}. 0_B The 2:1 divider for f_{PPP} is disabled. $f_{PPP} = f_{PIN}$ 1_B The 2:1 divider for f_{PPP} is enabled. $f_{PPP} = f_{MCLK} = f_{PIN} / 2$.

(continued)

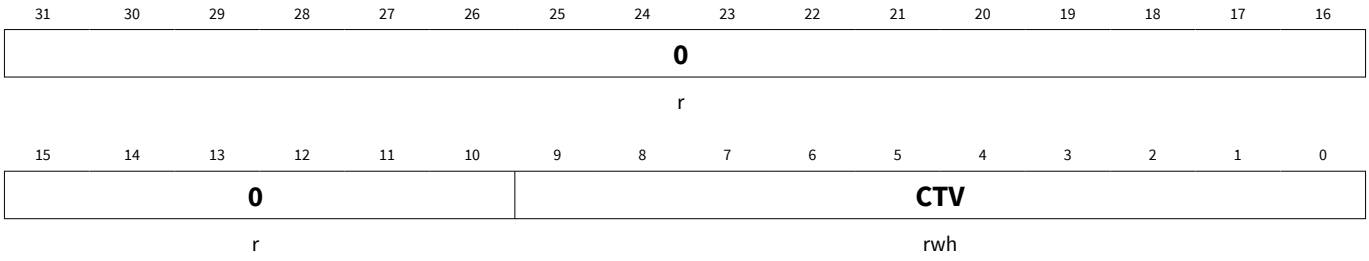
Field	Bits	Type	Description
CTQSEL	7:6	rw	**Input Selection for CTQ** This bit defines the length of a time quantum for the protocol pre-processor. 00_B $f_{CTQIN} = f_{PDIV}$ 01_B $f_{CTQIN} = f_{PPP}$ 10_B $f_{CTQIN} = f_{SCLK}$ 11_B $f_{CTQIN} = f_{MCLK}$
PCTQ	9:8	rw	**Pre-Divider for Time Quanta Counter** This bit field defines length of a time quantum tq for the time quanta counter in the protocol pre-processor. $t_Q = (PCTQ + 1) / f_{CTQIN}$
DCTQ	14:10	rw	**Denominator for Time Quanta Counter** This bit field defines the number of time quanta t_q taken into account by the time quanta counter in the protocol pre-processor.
PDIV	25:16	rw	**Divider Mode: Divider Factor to Generate f_{PDIV}** This bit field defines the ratio between the input frequency f_{PPP} and the divider frequency f_{PDIV}.
SCLKOSEL	28	rw	**Shift Clock Output Select** This bit field selects the input source for the SCLKOUT signal. 0_B SCLK from the baud rate generator is selected as the SCLKOUT input source. 1_B The transmit shift clock from DX1 input stage is selected as the SCLKOUT input source. *Note: The setting SCLKOSEL = 1 is used only when complete closed loop delay compensation is required for a slave SSC/IIS. The default setting of SCLKOSEL = 0 should be always used for all other cases.*
MCLKCFG	29	rw	**Master Clock Configuration** This bit field defines the level of the passive phase of the MCLKOUT signal. 0_B The passive level is 0. 1_B The passive level is 1.
SCLKCFG	31:30	rw	**Shift Clock Output Configuration** This bit field defines the level of the passive phase of the SCLKOUT signal and enables/disables a delay of half of a SCLK period. 00_B The passive level is 0 and the delay is disabled. 01_B The passive level is 1 and the delay is disabled. 10_B The passive level is 0 and the delay is enabled. 11_B The passive level is 1 and the delay is enabled.
0	2, 5, 15, 27:26	r	**Reserved** Read as 0; should be written with 0.

18.10.6.3 Register CMTR

The captured timer value is provided by the register CMTR.

CMTR Address: 44_H

Capture Mode Timer Register Reset Value: $0000\ 0000_H$



Field	Bits	Type	Description
CTV	9:0	rwh	**Captured Timer Value** The value of the counter is captured into this bit field if one of the trigger signals DX0T or DX1T are activated by the corresponding input stage.
0	31:10	r	**Reserved** Read as 0; should be written with 0.

18.10.7 Transfer Control and Status Registers

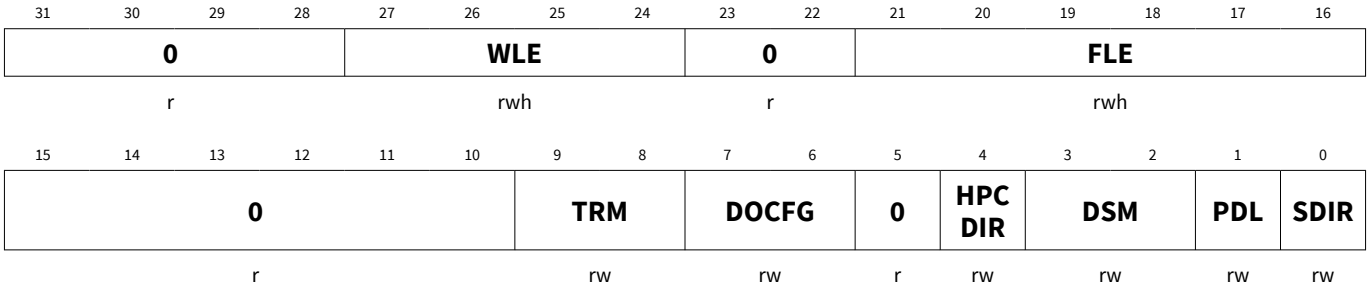
18.10.7.1 Register SCTR

The data shift unit is controlled by the register SCTR. The values in this register are applied for data transmission and reception.

Please note that the shift control settings SDIR, WLE, FLE, DSM and HPCDIR are shared between transmitter and receiver. They are internally “frozen” for a each data word transfer in the transmitter with the first transmit shift clock edge and with the first receive shift clock edge in the receiver. The software has to take care that updates of these bit fields by software are done coherently (e.g. refer to the receiver start event indication PSR.RSIF).

SCTR Address: 34_H

Shift Control Register Reset Value: $0000\ 0000_H$



Field	Bits	Type	Description
SDIR	0	rw	**Shift Direction** This bit defines the shift direction of the data words for transmission and reception. 0_B Shift LSB first. The first data bit of a data word is located at bit position 0. 1_B Shift MSB first. The first data bit of a data word is located at the bit position given by bit field SCTR.WLE.
PDL	1	rw	**Passive Data Level** This bit defines the output level at the shift data output signal when no data is available for transmission. The PDL level is output with the first relevant transmit shift clock edge of a data word. 0_B The passive data level is 0. 1_B The passive data level is 1.
DSM	3:2	rw	**Data Shift Mode** This bit field describes how the receive and transmit data is shifted in and out. 00_B Receive and transmit data is shifted in and out one bit at a time through DX0 and DOUT0. 01_B Reserved. 10_B Receive and transmit data is shifted in and out two bits at a time through two input stages (DX0 and DX3) and DOUT[1:0] respectively. 11_B Receive and transmit data is shifted in and out four bits at a time through four input stages (DX0, DX[5:3]) and DOUT[3:0] respectively. *Note: Dual- and Quad-output modes are used only by the SSC protocol. For all other protocols DSM must always be written with 00_B.*
HPCDIR	4	rw	**Port Control Direction** This bit defines the direction of the port pin(s) which allows hardware pin control (CCR.PCEN = 1). 0_B The pin(s) with hardware pin control enabled are selected to be in input mode. 1_B The pin(s) with hardware pin control enabled are selected to be in output mode.
DOCFG	7:6	rw	**Data Output Configuration** This bit defines the relation between the internal shift data value and the data output signal DOUTx. $X0_B$ DOUTx = shift data value $X1_B$ DOUTx = inverted shift data value

(continued)

Field	Bits	Type	Description
TRM	9:8	rw	**Transmission Mode** This bit field describes how the shift control signal is interpreted by the DSU. Data transfers are only possible while the shift control signal is active. 00_B The shift control signal is considered as inactive and data frame transfers are not possible. 01_B The shift control signal is considered active if it is at 1-level. This is the setting to be programmed to allow data transfers. 10_B The shift control signal is considered active if it is at 0-level. It is recommended to avoid this setting and to use the inversion in the DX2 stage in case of a low-active signal. 11_B The shift control signal is considered active without referring to the actual signal level. Data frame transfer is possible after each edge of the signal.
FLE	21:16	rwh	**Frame Length** This bit field defines how many bits are transferred within a data frame. A data frame can consist of several concatenated data words. If TCSR.FLEMD = 1, the value can be updated automatically by the data handler.
WLE	27:24	rwh	**Word Length** This bit field defines the data word length (amount of bits that are transferred in each data word) for reception and transmission. The data word is always right-aligned in the data buffer at the bit positions [WLE down to 0]. If TCSR.WLEMD = 1, the value can be updated automatically by the data handler. 0_H The data word contains 1 data bit located at bit position 0. 1_H The data word contains 2 data bits located at bit positions [1:0]. ... E_H The data word contains 15 data bits located at bit positions [14:0]. F_H The data word contains 16 data bits located at bit positions [15:0].
0	5, 15:10, 23:22, 31:28	r	**Reserved** Read as 0; should be written with 0.

18.10.7.2 Register TCSR

The data transmission is controlled and monitored by register TCSR.

TCSR	Address:	38_H
Transmit Control/Status Register	Reset Value:	$0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0			TE	TVC	TV	0	TSOF	0							
r			rh	rh	rh	r	rh	r							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		WA	TDVTR	TDEN		0	TDSSM	TDV	EOF	SOF	HPCMD	WAMD	FLEMD	SELMD	WLEMD
r		rwh	rw	rw		r	rw	rh	rwh	rwh	rw	rw	rw	rw	rw

Field	Bits	Type	Description
WLEMD	0	rw	**WLE Mode** This bit enables the data handler to automatically update the bit field SCTR.WLE by the transmit control information TCI[3:0] and bit TCSR.EOF by TCI[4] (see page ***346***). If enabled, an automatic update takes place when new data is loaded to register TBUF, either by writing to one of the transmit buffer input locations TBUFx or by an optional data buffer. 0_B The automatic update of SCTR.WLE and TCSR.EOF is disabled. 1_B The automatic update of SCTR.WLE and TCSR.EOF is enabled.
SELMD	1	rw	**Select Mode** This bit can be used mainly for the SSC protocol. It enables the data handler to automatically update bit field PCR.CTR[20:16] by the transmit control information TCI[4:0] and clear bit field PCR.CTR[23:21] (see page ***346***). If enabled, an automatic update takes place when new data is loaded to register TBUF, either by writing to one of the transmit buffer input locations TBUFx or by an optional data buffer. 0_B The automatic update of PCR.CTR[23:16] is disabled. 1_B The automatic update of PCR.CTR[23:16] is disabled.
FLEMD	2	rw	**FLE Mode** This bit enables the data handler to automatically update bits SCTR.FLE[4:0] by the transmit control information TCI[4:0] and to clear bit SCTR.FLE[5] (see page ***346***). If enabled, an automatic update takes place when new data is loaded to register TBUF, either by writing to one of the transmit buffer input locations TBUFx or by an optional data buffer. 0_B The automatic update of FLE is disabled. 1_B The automatic update of FLE is enabled.
WAMD	3	rw	**WA Mode** This bit can be used mainly for the IIS protocol. It enables the data handler to automatically update bit TCSR.WA by the transmit control information TCI[4] (see page ***346***). If enabled, an automatic update takes place when new data is loaded to register TBUF, either by writing to one of the transmit buffer input locations TBUFx or by an optional data buffer. 0_B The automatic update of bit WA is disabled. 1_B The automatic update of bit WA is enabled.

(continued)

Field	Bits	Type	Description
HPCMD	4	rw	**Hardware Port Control Mode** This bit can be used mainly for the dual and quad SSC protocol. It enables the data handler to automatically update bit SCTR.DSM by the transmit control information TCI[1:0] and bit SCTR.HPCDIR by TCI[2] (see page 346). If enabled, an automatic update takes place when new data is loaded to register TBUF, either by writing to one of the transmit buffer input locations TBUFx or by an optional data buffer. 0_B The automatic update of bits SCTR.DSM and SCTR.HPCDIR is disabled. 1_B The automatic update of bits SCTR.DSM and SCTR.HPCDIR is enabled.
SOF	5	rwh	**Start Of Frame** This bit is only taken into account for the SSC protocol, otherwise it is ignored. It indicates that the data word in TBUF is considered as the first word of a new SSC frame if it is valid for transmission (TCSR.TDV = 1). This bit becomes cleared when the TBUF data word is transferred to the transmit shift register. 0_B The data word in TBUF is not considered as first word of a frame. 1_B The data word in TBUF is considered as first word of a frame. A currently running frame is finished and MSLS becomes deactivated (respecting the programmed delays).
EOF	6	rwh	**End Of Frame** This bit is only taken into account for the SSC protocol, otherwise it is ignored. It can be modified automatically by the data handler if bit WLEMD = 1. It indicates that the data word in TBUF is considered as the last word of an SSC frame. If it is the last word, the MSLS signal becomes inactive after the transfer, respecting the programmed delays. This bit becomes cleared when the TBUF data word is transferred to the transmit shift register. 0_B The data word in TBUF is not considered as last word of an SSC frame. 1_B The data word in TBUF is considered as last word of an SSC frame.
TDV	7	rh	**Transmit Data Valid** This bit indicates that the data word in the transmit buffer TBUF can be considered as valid for transmission. The TBUF data word can only be sent out if TDV = 1. It is automatically set when data is moved to TBUF (by writing to one of the transmit buffer input locations TBUFx, or optionally, by the bypass or FIFO mechanism). 0_B The data word in TBUF is not valid for transmission. 1_B The data word in TBUF is valid for transmission and a transmission start is possible. New data should not be written to a TBUFx input location while TDV = 1.

(continued)

Field	Bits	Type	Description
TDSSM	8	rw	**TBUF Data Single Shot Mode** This bit defines if the data word TBUF data is considered as permanently valid or if the data should only be transferred once. 0_B The data word in TBUF is not considered as invalid after it has been loaded into the transmit shift register. The loading of the TBUF data into the shift register does not clear TDV. 1_B The data word in TBUF is considered as invalid after it has been loaded into the shift register. In ASC and IIC mode, TDV is cleared with the TBI event, whereas in SSC and IIS mode, it is cleared with the RSI event. TDSSM = 1 has to be programmed if an optional data buffer is used.
TDEN	11:10	rw	**TBUF Data Enable** This bit field controls the gating of the transmission start of the data word in the transmit buffer TBUF. 00_B A transmission start of the data word in TBUF is disabled. If a transmission is started, the passive data level is sent out. 01_B A transmission of the data word in TBUF can be started if TDV = 1. 10_B A transmission of the data word in TBUF can be started if TDV = 1 while DX2S = 0. 11_B A transmission of the data word in TBUF can be started if TDV = 1 while DX2S = 1.
TDVTR	12	rw	**TBUF Data Valid Trigger** This bit enables the transfer trigger unit to set bit TCSR.TE if the trigger signal DX2T becomes active for event driven transfer starts, e.g. timer-based or depending on an event at an input pin. Bit TDVTR has to be 0 for protocols where the input stage DX2 is used for data shifting. 0_B Bit TCSR.TE is permanently set. 1_B Bit TCSR.TE is set if DX2T becomes active while TDV = 1.
WA	13	rwh	**Word Address** This bit is only taken into account for the IIS protocol, otherwise it is ignored. It can be modified automatically by the data handler if bit WAMD = 1. Bit WA defines for which channel the data stored in TBUF will be transmitted. 0_B The data word in TBUF will be transmitted after a falling edge of WA has been detected (referring to PSR.WA). 1_B The data word in TBUF will be transmitted after a rising edge of WA has been detected (referring to PSR.WA).

(continued)

Field	Bits	Type	Description
TSOF	24	rh	**Transmitted Start Of Frame** This bit indicates if the latest start of a data word transmission has taken place for the first data word of a new data frame. This bit is updated with the transmission start of each data word. 0_B The latest data word transmission has not been started for the first word of a data frame. 1_B The latest data word transmission has been started for the first word of a data frame.
TV	26	rh	**Transmission Valid** This bit represents the transmit buffer underflow and indicates if the latest start of a data word transmission has taken place with a valid data word from the transmit buffer TBUF. This bit is updated with the transmission start of each data word. 0_B The latest start of a data word transmission has taken place while no valid data was available. As a result, the transmission of a data words with passive level (SCTR.PDL) has been started. 1_B The latest start of a data word transmission has taken place with valid data from TBUF.
TVC	27	rh	**Transmission Valid Cumulated** This bit cumulates the transmit buffer underflow indication TV. It is cleared automatically together with bit TV and has to be set by writing FMR.ATVC = 1. 0_B Since TVC has been set, at least one data buffer underflow condition has occurred. 1_B Since TVC has been set, no data buffer underflow condition has occurred.
TE	28	rh	**Trigger Event** If the transfer trigger mechanism is enabled, this bit indicates that a trigger event has been detected (DX2T = 1) while TCSR.TDV = 1. If the event trigger mechanism is disabled, the bit TE is permanently set. It is cleared by writing FMR.MTDV = 10_B or when the data word located in TBUF is loaded into the shift register. 0_B The trigger event has not yet been detected. A transmission of the data word in TBUF can not be started. 1_B The trigger event has been detected (or the trigger mechanism is switched off) and a transmission of the data word in TBUF can be started.
0	9, 23:14, 25, 31:29	r	**Reserved** Read as 0; should be written with 0.

18.10.7.3 Register FMR

The flag modification register FMR allows the modification of control and status flags related to data handling by using only write accesses. Read accesses to FMR always deliver 0 at all bit positions.

Additionally, the service request outputs of this USIC channel can be activated by software (the activation is triggered by the write access and is deactivated automatically).

FMR Address: 68_H

Flag Modification Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0										SIO5	SIO4	SIO3	SIO2	SIO1	SIO0
r										w	w	w	w	w	w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRDV1	CRDV0	0									ATVC	0		MTDV	
w	w	r									w	r		w	

Field	Bits	Type	Description
MTDV	1:0	w	**Modify Transmit Data Valid** Writing to this bit field can modify bits TCSR.TDV and TCSR.TE to control the start of a data word transmission by software. 00_B No action. 01_B Bit TDV is set, TE is unchanged. 10_B Bits TDV and TE are cleared. 11_B Reserved
ATVC	4	w	**Activate Bit TVC** Writing to this bit can set bit TCSR.TVC to start a new cumulation of the transmit buffer underflow condition. 0_B No action. 1_B Bit TCSR.TVC is set.
CRDV0	14	w	**Clear Bits RDV for RBUF0** Writing 1 to this bit clears bits RBUF01SR.RDV00 and RBUF01SR.RDV10 to declare the received data in RBUF0 as no longer valid (to emulate a read action). 0_B No action. 1_B Bits RBUF01SR.RDV00 and RBUF01SR.RDV10 are cleared.
CRDV1	15	w	**Clear Bit RDV for RBUF1** Writing 1 to this bit clears bits RBUF01SR.RDV01 and RBUF01SR.RDV11 to declare the received data in RBUF1 as no longer valid (to emulate a read action). 0_B No action. 1_B Bits RBUF01SR.RDV01 and RBUF01SR.RDV11 are cleared.
SIOx (x=0-5)	x+16	w	**Set Interrupt Output SRx** Writing a 1 to this bit field activates the service request output SRx of this USIC channel. It has no impact on service request outputs of other USIC channels. 0_B No action. 1_B The service request output SRx is activated.
0	3:2, 13:5, 31:22	r	**Reserved** Read as 0; should be written with 0.

18.10.8 Data Buffer Registers

18.10.8.1 Transmit Buffer Locations

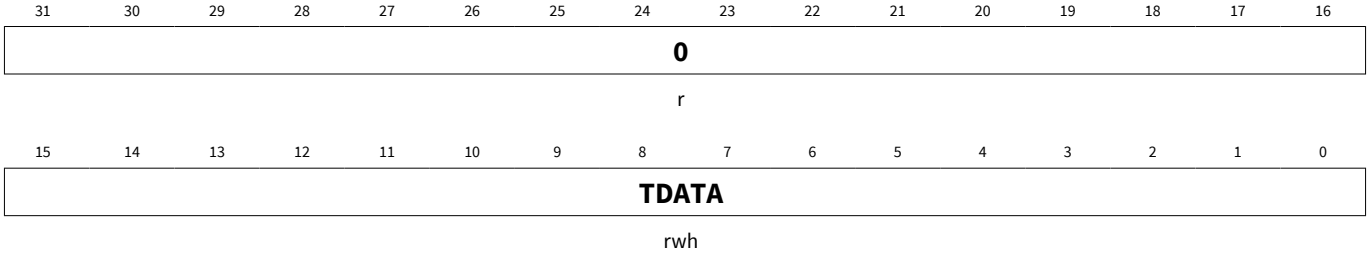
The 32 independent data input locations TBUF00 to TBUF31 are address locations that can be used as data entry locations for the transmit buffer. Data written to one of these locations will appear in a common register TBUF. Additionally, the 5 bit coding of the number [31:0] of the addressed data input location represents the transmit control information TCI (please refer to the protocol sections for more details).

The internal transmit buffer register TBUF contains the data that will be loaded to the transmit shift register for the next transmission of a data word. It can be read out at all TBUF00 to TBUF31 addresses.

18.10.8.1.1 Register TBUFx

TBUFx (x = 00-31) Address: $80_H + x*4$

Transmit Buffer Input Location x Reset Value: $0000\ 0000_H$



Field	Bits	Type	Description
TDATA	15:0	rwh	**Transmit Data** This bit field contains the data to be transmitted (read view). A data write action to at least the low byte of TDATA sets TCSR.TDV.
0	31:16	r	**Reserved** Read as 0; should be written with 0.

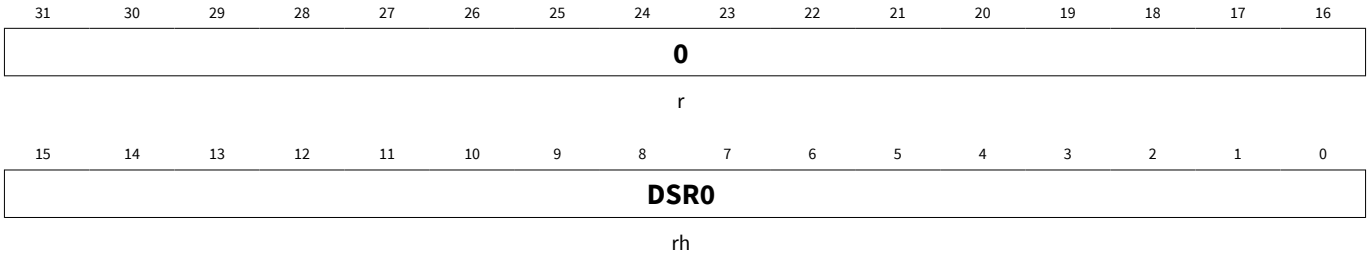
18.10.8.2 Receive Buffer Registers RBUF0, RBUF1, RBUF01SR

18.10.8.2.1 Register RBUF0

The receive buffer register RBUF0 contains the data received from RSR0[3:0]. A read action does not change the status of the receive data from “not yet read = valid” to “already read = not valid”.

RBUF0 Address: $5C_H$

Receiver Buffer Register 0 Reset Value: $0000\ 0000_H$



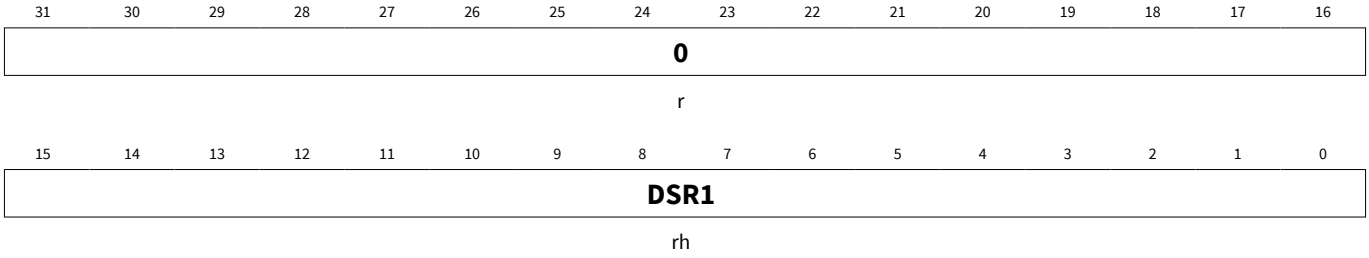
Field	Bits	Type	Description
DSR0	15:0	rh	**Data of Shift Registers 0[3:0]**
0	31:16	r	**Reserved** Read as 0; should be written with 0.

18.10.8.2.2 Register RBUF1

The receive buffer register RBUF1 contains the data received from RSR1[3:0]. A read action does not change the status of the receive data from “not yet read = valid” to “already read = not valid”.

RBUF1 Address: 60_H

Receiver Buffer Register 1 Reset Value: $0000\ 0000_H$



Field	Bits	Type	Description
DSR1	15:0	rh	**Data of Shift Registers 1[3:0]**
0	31:16	r	**Reserved** Read as 0; should be written with 0.

18.10.8.2.3 Register RBUF01SR

The receive buffer status register RBUF01SR provides the status of the data in receive buffers RBUF0 and RBUF1.

RBUF01SR Address: 64_H

Receiver Buffer 01 Status Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DS1	**RDV11**	**RDV10**	**0**			**PERR1**	**PAR1**	**0**	**SOF1**	**0**		**WLEN1**			
rh	rh	rh	r			rh	rh	r	rh	r		rh			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DS0	**RDV01**	**RDV00**	**0**			**PERR0**	**PAR0**	**0**	**SOF0**	**0**		**WLEN0**			
rh	rh	rh	r			rh	rh	r	rh	r		rh			

Field	Bits	Type	Description
WLEN0	3:0	rh	**Received Data Word Length in RBUF0** This bit field indicates how many bits have been received within the last data word stored in RBUF0. This number indicates how many data bits have to be considered as receive data, whereas the other bits in RBUF0 have been cleared automatically. The received bits are always right-aligned. For all protocol modes besides dual and quad SSC, Received data word length = WLEN0 + 1 For dual SSC mode, Received data word length = WLEN0 + 2 For quad SSC mode, Received data word length = WLEN0 + 4
SOF0	6	rh	**Start of Frame in RBUF0** This bit indicates whether the data word in RBUF0 has been the first data word of a data frame. 0_B The data in RBUF0 has not been the first data word of a data frame. 1_B The data in RBUF0 has been the first data word of a data frame.
PAR0	8	rh	**Protocol-Related Argument in RBUF0** This bit indicates the value of the protocol-related argument. This value is elaborated depending on the selected protocol and adds additional information to the data word in RBUF0. The meaning of this bit is described in the corresponding protocol chapter.

(continued)

Field	Bits	Type	Description
PERR0	9	rh	**Protocol-related Error in RBUF0** This bit indicates if the value of the protocol-related argument meets an expected value. This value is elaborated depending on the selected protocol and adds additional information to the data word in RBUF0. The meaning of this bit is described in the corresponding protocol chapter. 0_B The received protocol-related argument PAR matches the expected value. The reception of the data word sets bit PSR.RIF and can generate a receive interrupt. 1_B The received protocol-related argument PAR does not match the expected value. The reception of the data word sets bit PSR.AIF and can generate an alternative receive interrupt.
RDV00	13	rh	**Receive Data Valid in RBUF0** This bit indicates the status of the data content of register RBUF0. This bit is identical to bit RBUF01SR.RDV10 and allows consisting reading of information for the receive buffer registers. It is set when a new data word is stored in RBUF0 and automatically cleared if it is read out via RBUF. 0_B Register RBUF0 does not contain data that has not yet been read out. 1_B Register RBUF0 contains data that has not yet been read out.
RDV01	14	rh	**Receive Data Valid in RBUF1** This bit indicates the status of the data content of register RBUF1. This bit is identical to bit RBUF01SR.RDV11 and allows consisting reading of information for the receive buffer registers. It is set when a new data word is stored in RBUF1 and automatically cleared if it is read out via RBUF. 0_B Register RBUF1 does not contain data that has not yet been read out. 1_B Register RBUF1 contains data that has not yet been read out.
DS0	15	rh	**Data Source** This bit indicates which receive buffer register (RBUF0 or RBUF1) is currently visible in registers RBUF(D) and in RBUFSR for the associated status information. It indicates which buffer contains the oldest data (the data that has been received first). This bit is identical to bit RBUF01SR.DS1 and allows consisting reading of information for the receive buffer registers. 0_B The register RBUF contains the data of RBUF0 (same for associated status information). 1_B The register RBUF contains the data of RBUF1 (same for associated status information).

(continued)

Field	Bits	Type	Description
WLEN1	19:16	rh	**Received Data Word Length in RBUF1** This bit field indicates how many bits have been received within the last data word stored in RBUF1. This number indicates how many data bits have to be considered as receive data, whereas the other bits in RBUF1 have been cleared automatically. The received bits are always right-aligned. For all protocol modes besides dual and quad SSC, Received data word length = WLEN1 + 1 For dual SSC mode, Received data word length = WLEN1 + 2 For quad SSC mode, Received data word length = WLEN1 + 4
SOF1	22	rh	**Start of Frame in RBUF1** This bit indicates whether the data word in RBUF1 has been the first data word of a data frame. 0_B The data in RBUF1 has not been the first data word of a data frame. 1_B The data in RBUF1 has been the first data word of a data frame.
PAR1	24	rh	**Protocol-Related Argument in RBUF1** This bit indicates the value of the protocol-related argument. This value is elaborated depending on the selected protocol and adds additional information to the data word in RBUF1. The meaning of this bit is described in the corresponding protocol chapter.
PERR1	25	rh	**Protocol-related Error in RBUF1** This bit indicates if the value of the protocol-related argument meets an expected value. This value is elaborated depending on the selected protocol and adds additional information to the data word in RBUF1. The meaning of this bit is described in the corresponding protocol chapter. 0_B The received protocol-related argument PAR matches the expected value. The reception of the data word sets bit PSR.RIF and can generate a receive interrupt. 1_B The received protocol-related argument PAR does not match the expected value. The reception of the data word sets bit PSR.AIF and can generate an alternative receive interrupt.
RDV10	29	rh	**Receive Data Valid in RBUF0** This bit indicates the status of the data content of register RBUF0. This bit is identical to bit RBUF01SR.RDV00 and allows consisting reading of information for the receive buffer registers. 0_B Register RBUF0 does not contain data that has not yet been read out. 1_B Register RBUF0 contains data that has not yet been read out.

(continued)

Field	Bits	Type	Description
RDV11	30	rh	**Receive Data Valid in RBUF1** This bit indicates the status of the data content of register RBUF1. This bit is identical to bit RBUF01SR.RDV01 and allows consisting reading of information for the receive buffer registers. 0_B Register RBUF1 does not contain data that has not yet been read out. 1_B Register RBUF1 contains data that has not yet been read out.
DS1	31	rh	**Data Source** This bit indicates which receive buffer register (RBUF0 or RBUF1) is currently visible in registers RBUF(D) and in RBUFSR for the associated status information. It indicates which buffer contains the oldest data (the data that has been received first). This bit is identical to bit RBUF01SR.DS0 and allows consisting reading of information for the receive buffer registers. 0_B The register RBUF contains the data of RBUF0 (same for associated status information). 1_B The register RBUF contains the data of RBUF1 (same for associated status information).
0	5:4, 7, 12:10, 21:20, 23, 28:26	r	**Reserved** Read as 0; should be written with 0.

18.10.8.3 Receive Buffer Registers RBUF, RBUFD, RBUFSR

18.10.8.3.1 Register RBUF

The receiver buffer register RBUF shows the content of the either RBUF0 or RBUF1, depending on the order of reception. Always the oldest data (the data word that has been received first) from both receive buffers can be read from RBUF. It is recommended to read out the received data from RBUF instead of RBUF0/1. With a read access of at least the low byte of RBUF, the status of the receive data is automatically changed from “not yet read = valid” to “already read = not valid”, the content of RBUF becomes updated, and the next received data word becomes visible in RBUF.

RBUF Address: 54_H

Receiver Buffer Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DSR															
rh															

Field	Bits	Type	Description
DSR	15:0	rh	**Received Data** This bit field monitors the content of either RBUF0 or RBUF1, depending on the reception sequence.
0	31:16	r	**Reserved** Read as 0; should be written with 0.

18.10.8.3.2 Register RBUFD

If a debugger should be used to monitor the received data, the automatic update mechanism has to be de-activated to guaranty data consistency. Therefore, the receiver buffer register for debugging RBUFD is available. It is similar to RBUF, but without the automatic update mechanism by a read action. So a debugger (or other monitoring function) can read RBUFD without disturbing the receive sequence.

RBUFD Address: 58_H

Receiver Buffer Register for Debugger Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DSR															
rh															

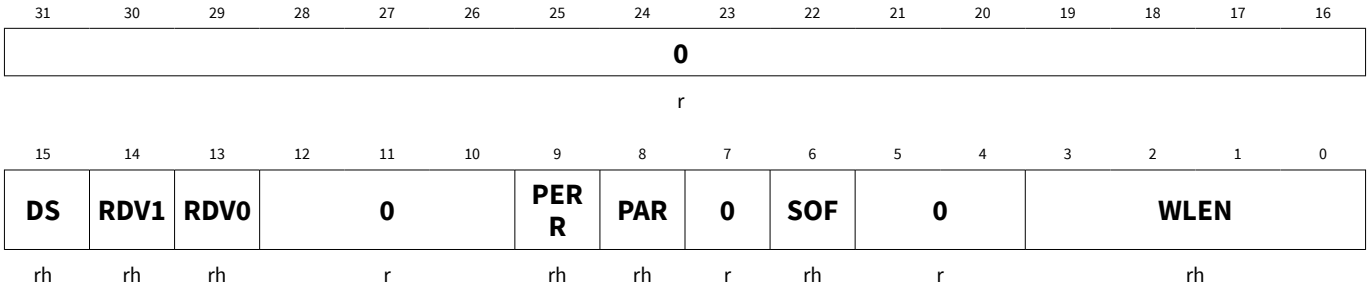
Field	Bits	Type	Description
DSR	15:0	rh	**Data from Shift Register** Same as RBUF.DSR, but without releasing the buffer after a read action.
0	31:16	r	**Reserved** Read as 0; should be written with 0.

18.10.8.3.3 Register RBUFSR

The receive buffer status register RBUFSR provides the status of the data in receive buffers RBUF and RBUFD. If bits RBUF01SR.DS0 (or RBUF01SR.DS1) are 0, the lower 16-bit content of RBUF01SR is monitored in RBUFSR, otherwise the upper 16-bit content of RBUF01SR is shown.

RBUFSR Address: 50_H

Receiver Buffer Status Register Reset Value: $0000\ 0000_H$



Field	Bits	Type	Description
WLEN	3:0	rh	**Received Data Word Length in RBUF or RBUFD** Description see RBUF01SR.WLEN0 or RBUF01SR.WLEN1.
SOF	6	rh	**Start of Frame in RBUF or RBUFD** Description see RBUF01SR.SOF0 or RBUF01SR.SOF1.
PAR	8	rh	**Protocol-Related Argument in RBUF or RBUFD** Description see RBUF01SR.PAR0 or RBUF01SR.PAR1.
PERR	9	rh	**Protocol-related Error in RBUF or RBUFD** Description see RBUF01SR.PERR0 or RBUF01SR.PERR1.
RDV0	13	rh	**Receive Data Valid in RBUF or RBUFD** Description see RBUF01SR.RDV00 or RBUF01SR.RDV10.
RDV1	14	rh	**Receive Data Valid in RBUF or RBUFD** Description see RBUF01SR.RDV01 or RBUF01SR.RDV11.
DS	15	rh	**Data Source of RBUF or RBUFD** Description see RBUF01SR.DS0 or RBUF01SR.DS1.
0	5:4, 7, 12:10, 31:16	r	**Reserved** Read as 0; should be written with 0.

18.10.9 FIFO Buffer and Bypass Registers

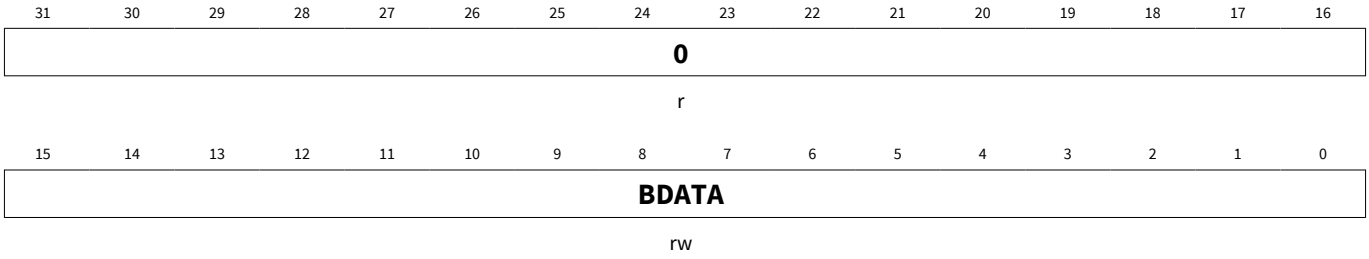
18.10.9.1 Bypass Registers

A write action to at least the low byte of the bypass data register sets BYPCR.BDV = 1 (bypass data tagged valid).

18.10.9.1.1 Register BYP

BYP Address: 100_H

Bypass Data Register Reset Value: $0000\ 0000_H$

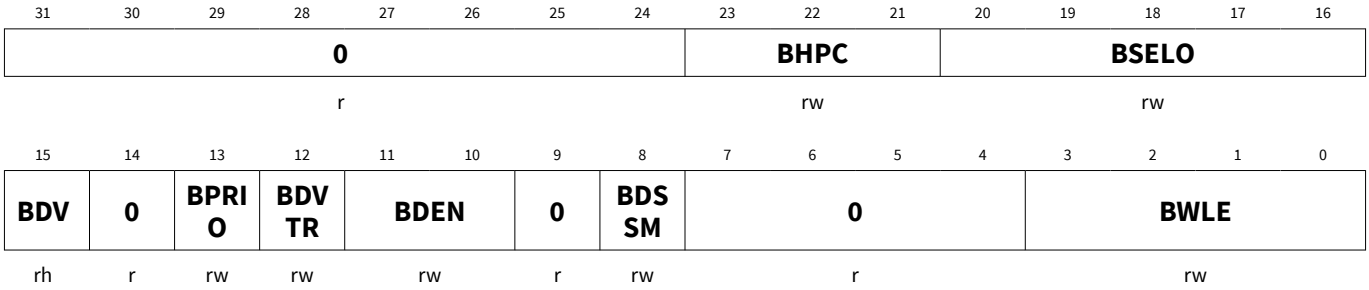


Field	Bits	Type	Description
BDATA	15:0	rw	**Bypass Data** This bit field contains the bypass data.
0	31:16	r	**Reserved** Read as 0; should be written with 0.

18.10.9.1.2 Register BYPCR

BYPCR Address: 104_H

Bypass Control Register Reset Value: $0000\ 0000_H$



Field	Bits	Type	Description
BWLE	3:0	rw	**Bypass Word Length** This bit field defines the word length of the bypass data. The word length is given by BWLE + 1 with the data word being right-aligned in the data buffer at the bit positions [BWLE down to 0]. The bypass data word is always considered as an own frame with the length of BWLE. Same coding as SCTR.WLE.
BDSSM	8	rw	**Bypass Data Single Shot Mode** This bit defines if the bypass data is considered as permanently valid or if the bypass data is only transferred once (single shot mode). 0_B The bypass data is still considered as valid after it has been loaded into TBUF. The loading of the data into TBUF does not clear BDV. 1_B The bypass data is considered as invalid after it has been loaded into TBUF. The loading of the data into TBUF clears BDV.

(continued)

Field	Bits	Type	Description
BDEN	11:10	rw	**Bypass Data Enable** This bit field defines if and how the transfer of bypass data to TBUF is enabled. 00_B The transfer of bypass data is disabled. 01_B The transfer of bypass data to TBUF is possible. Bypass data will be transferred to TBUF according to its priority if BDV = 1. 10_B Gated bypass data transfer is enabled. Bypass data will be transferred to TBUF according to its priority if BDV = 1 and while DX2S = 0. 11_B Gated bypass data transfer is enabled. Bypass data will be transferred to TBUF according to its priority if BDV = 1 and while DX2S = 1.
BDVTR	12	rw	**Bypass Data Valid Trigger** This bit enables the bypass data for being tagged valid when DX2T is active (for time framing or time-out purposes). 0_B Bit BDV is not influenced by DX2T. 1_B Bit BDV is set if DX2T is active.
BPRIO	13	rw	**Bypass Priority** This bit defines the priority between the bypass data and the transmit FIFO data. 0_B The transmit FIFO data has a higher priority than the bypass data. 1_B The bypass data has a higher priority than the transmit FIFO data.
BDV	15	rh	**Bypass Data Valid** This bit defines if the bypass data is valid for a transfer to TBUF. This bit is set automatically by a write access to at least the low-byte of register BYP. It can be cleared by software by writing TRBSCR.CBDV. 0_B The bypass data is not valid. 1_B The bypass data is valid.
BSELO	20:16	rw	**Bypass Select Outputs** This bit field contains the value that is written to PCR.CTR[20:16] if bypass data is transferred to TBUF while TCSR.SELMD = 1. In the SSC protocol, this bit field can be used to define which SELOx output line will be activated when bypass data is transmitted.
BHPC	23:21	rw	**Bypass Hardware Port Control** This bit field contains the value that is written to SCTR[4:2] if bypass data is transferred to TBUF while TCSR.HPCMD = 1. In the SSC protocol, this bit field can be used to define the data shift mode and if hardware port control is enabled through CCR.HPCEN = 1, the pin direction when bypass data is transmitted.
0	7:4, 9, 14, 31:24	r	**Reserved** Read as 0; should be written with 0.

18.10.9.2 General FIFO Buffer Control Registers

The transmit and receive FIFO status information of USICx_CHy is given in registers USICx_CHy.TRBSR.

The bits related to the transmitter buffer in this register can only by written if the transmit buffer functionality is enabled by CCFG.TB = 1, otherwise write accesses are ignored. A similar behavior applies for the bits related to the receive buffer referring to CCFG.RB = 1.

The interrupt flags (event flags) in the transmit and receive FIFO status register TRBSR can be cleared by writing a 1 to the corresponding bit position in register TRBSCR, whereas writing a 0 has to effect on these bits. Writing a 1 by software to SRBI, RBERI, ARBI, STBI, or TBERI sets the corresponding bit to simulate the detection of a transmit/receive buffer event, but without activating any service request output (therefore, see FMR.SIOx).

Bits TBUS and RBUS have been implemented for testing purposes. They can be ignored by data handling software. Please note that a read action can deliver either a 0 or a 1 for these bits. It is recommended to treat them as “don’t care”.

18.10.9.2.1 Register TRBSR

TRBSR Address: 114_H

Transmit/Receive Buffer Status Register Reset Value: $0000\ 0808_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**TBFLVL**							**0**	**RBFLVL**						
r	rh							r	rh						

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**STBT**	**TBUS**	**TFULL**	**TEMPTY**	**0**	**TBERI**	**STBI**	**0**	**SRBT**	**RBUS**	**RFULL**	**REMPTY**	**ARBI**	**RBERI**	**SRBI**
r	rh	rh	rh	rh	r	rwh	rwh	r	rh	rh	rh	rh	rwh	rwh	rwh

Field	Bits	Type	Description
SRBI	0	rwh	**Standard Receive Buffer Event** This bit indicates that a standard receive buffer event has been detected. It is cleared by writing TRBSCR.CSRBI = 1. If enabled by RBCTR.SRBIEN, the service request output SRx selected by RBCTR.SRBINP becomes activated if a standard receive buffer event is detected. 0_B A standard receive buffer event has not been detected. 1_B A standard receive buffer event has been detected.
RBERI	1	rwh	**Receive Buffer Error Event** This bit indicates that a receive buffer error event has been detected. It is cleared by writing TRBSCR.CRBERI = 1. If enabled by RBCTR.RBERIEN, the service request output SRx selected by RBCTR.ARBINP becomes activated if a receive buffer error event is detected. 0_B A receive buffer error event has not been detected. 1_B A receive buffer error event has been detected.

(continued)

Field	Bits	Type	Description
ARBI	2	rwh	**Alternative Receive Buffer Event** This bit indicates that an alternative receive buffer event has been detected. It is cleared by writing TRBSCR.CARBI = 1. If enabled by RBCTR.ARBIEN, the service request output SRx selected by RBCTR.ARBINP becomes activated if an alternative receive buffer event is detected. 0_B An alternative receive buffer event has not been detected. 1_B An alternative receive buffer event has been detected.
REMPTY	3	rh	**Receive Buffer Empty** This bit indicates whether the receive buffer is empty. 0_B The receive buffer is not empty. 1_B The receive buffer is empty.
RFULL	4	rh	**Receive Buffer Full** This bit indicates whether the receive buffer is full. 0_B The receive buffer is not full. 1_B The receive buffer is full.
RBUS	5	rh	**Receive Buffer Busy** This bit indicates whether the receive buffer is currently updated by the FIFO handler. 0_B The receive buffer information has been completely updated. 1_B The OUTR update from the FIFO memory is ongoing. A read from OUTR will be delayed. FIFO pointers from the previous read are not yet updated.
SRBT	6	rh	**Standard Receive Buffer Event Trigger** This bit triggers a standard receive buffer event when set. If enabled by RBCTR.SRBIEN, the service request output SRx selected by RBCTR.SRBINP becomes activated until the bit is cleared. 0_B A standard receive buffer event is not triggered using this bit. 1_B A standard receive buffer event is triggered using this bit.
STBI	8	rwh	**Standard Transmit Buffer Event** This bit indicates that a standard transmit buffer event has been detected. It is cleared by writing TRBSCR.CSTBI = 1. If enabled by TBCTR.STBIEN, the service request output SRx selected by TBCTR.STBINP becomes activated if a standard transmit buffer event is detected. 0_B A standard transmit buffer event has not been detected. 1_B A standard transmit buffer event has been detected.

(continued)

Field	Bits	Type	Description
TBERI	9	rwh	**Transmit Buffer Error Event** This bit indicates that a transmit buffer error event has been detected. It is cleared by writing TRBSCR.CTBERI = 1. If enabled by TBCTR.TBERIEN, the service request output SRx selected by TBCTR.ATBINP becomes activated if a transmit buffer error event is detected. 0_B A transmit buffer error event has not been detected. 1_B A transmit buffer error event has been detected.
TEMPTY	11	rh	**Transmit Buffer Empty** This bit indicates whether the transmit buffer is empty. 0_B The transmit buffer is not empty. 1_B The transmit buffer is empty.
TFULL	12	rh	**Transmit Buffer Full** This bit indicates whether the transmit buffer is full. 0_B The transmit buffer is not full. 1_B The transmit buffer is full.
TBUS	13	rh	**Transmit Buffer Busy** This bit indicates whether the transmit buffer is currently updated by the FIFO handler. 0_B The transmit buffer information has been completely updated. 1_B The FIFO memory update after write to INx is ongoing. A write to INx will be delayed. FIFO pointers from the previous INx write are not yet updated.
STBT	14	rh	**Standard Transmit Buffer Event Trigger** This bit triggers a standard transmit buffer event when set. If enabled by TBCTR.STBIEN, the service request output SRx selected by TBCTR.STBINP becomes activated until the bit is cleared. 0_B A standard transmit buffer event is not triggered using this bit. 1_B A standard transmit buffer event is triggered using this bit.
RBFLVL	22:16	rh	**Receive Buffer Filling Level** This bit field indicates the filling level of the receive buffer, starting with 0 for an empty buffer.
TBFLVL	30:24	rh	**Transmit Buffer Filling Level** This bit field indicates the filling level of the transmit buffer, starting with 0 for an empty buffer. *Note: The first data word written to Transmit FIFO will be loaded immediately to TBUF and removed from FIFO.*
0	7, 10, 15, 23, 31	r	**Reserved** Read as 0; should be written with 0.

18.10.9.2.2 Register TRBSCR

The bits in register TRBSCR are used to clear the notification bits in register TRBSR or to clear the FIFO mechanism for the transmit or receive buffer. A read action always delivers 0.

TRBSCR Address: 118_H

Transmit/Receive Buffer Status Clear Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FLUSHTB	FLUSHRB	0			CBDV	CTBERI	CSTBI	0					CARBI	CRBERI	CSRBI
w	w	r			w	w	w	r					w	w	w

Field	Bits	Type	Description
CSRBI	0	w	**Clear Standard Receive Buffer Event** 0_B No effect. 1_B Clear TRBSR.SRBI.
CRBERI	1	w	**Clear Receive Buffer Error Event** 0_B No effect. 1_B Clear TRBSR.RBERI.
CARBI	2	w	**Clear Alternative Receive Buffer Event** 0_B No effect. 1_B Clear TRBSR.ARBI.
CSTBI	8	w	**Clear Standard Transmit Buffer Event** 0_B No effect. 1_B Clear TRBSR.STBI.
CTBERI	9	w	**Clear Transmit Buffer Error Event** 0_B No effect. 1_B Clear TRBSR.TBERI.
CBDV	10	w	**Clear Bypass Data Valid** 0_B No effect. 1_B Clear BYPCR.BDV.
FLUSHRB	14	w	**Flush Receive Buffer** 0_B No effect. 1_B The receive FIFO buffer is cleared (filling level is cleared and output pointer is set to input pointer value). Should only be used while the FIFO buffer is not taking part in data traffic.

(continued)

Field	Bits	Type	Description
FLUSHTB	15	w	**Flush Transmit Buffer** 0_B No effect. 1_B The transmit FIFO buffer is cleared (filling level is cleared and output pointer is set to input pointer value). Should only be used while the FIFO buffer is not taking part in data traffic.
0	7:3, 13:11, 31:16	r	**Reserved** Read as 0; should be written with 0.

18.10.9.3 Transmit FIFO Buffer Control Registers

The transmit FIFO buffer is controlled by register TBCTR. TBCTR can only by written if the transmit buffer functionality is enabled by CCFG.TB = 1, otherwise write accesses are ignored.

18.10.9.3.1 Register TBCTR

TBCTR Address: 108_H

Transmitter Buffer Control Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TBERIEN	**STBIEN**	**0**	**LOF**	**0**	**SIZE**			**0**		**ATBINP**			**STBINP**		
rw	rw	r	rw	r	rw			r		rw			rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STBTEN	**STBTM**	**LIMIT**						**0**		**DPTR**					
rw	rw	rw						r		w					

Field	Bits	Type	Description
DPTR	5:0	w	**Data Pointer** This bit field defines the start value for the transmit buffer pointers when assigning the FIFO entries to the transmit FIFO buffer. A read always delivers 0. When writing DPTR while SIZE = 0, both transmitter pointers TDIPTR and RTDOPTR in register TRBPTR are updated with the written value and the buffer is considered as empty. A write access to DPTR while SIZE > 0 is ignored and does not modify the pointers.
LIMIT	13:8	rw	**Limit For Interrupt Generation** This bit field defines the target filling level of the transmit FIFO buffer that is used for the standard transmit buffer event detection.

(continued)

Field	Bits	Type	Description
STBTM	14	rw	**Standard Transmit Buffer Trigger Mode** This bit selects the standard transmit buffer event trigger mode. 0_B Trigger mode 0: While TRBSR.STBT=1, a standard transmit buffer event will be generated whenever there is a data transfer to TBUF or data write to INx (depending on TBCTR.LOF setting). STBT is cleared when TRBSR.TBFLVL=TBCTR.LIMIT. 1_B Trigger mode 1: While TRBSR.STBT=1, a standard transmit buffer event will be generated whenever there is a data transfer to TBUF or data write to INx (depending on TBCTR.LOF setting). STBT is cleared when TRBSR.TBFLVL=TBCTR.SIZE.
STBTEN	15	rw	**Standard Transmit Buffer Trigger Enable** This bit enables/disables triggering of the standard transmit buffer event through bit TRBSR.STBT. 0_B The standard transmit buffer event trigger through bit TRBSR.STBT is disabled. 1_B The standard transmit buffer event trigger through bit TRBSR.STBT is enabled.
STBINP	18:16	rw	**Standard Transmit Buffer Interrupt Node Pointer** This bit field defines which service request output SRx becomes activated in case of a standard transmit buffer event. 000_B Output SR0 becomes activated. 001_B Output SR1 becomes activated. 010_B Output SR2 becomes activated. 011_B Output SR3 becomes activated. 100_B Output SR4 becomes activated. 101_B Output SR5 becomes activated. *Note: All other settings of the bit field are reserved.*
ATBINP	21:19	rw	**Alternative Transmit Buffer Interrupt Node Pointer** This bit field define which service request output SRx will be activated in case of a transmit buffer error event. 000_B Output SR0 becomes activated. 001_B Output SR1 becomes activated. 010_B Output SR2 becomes activated. 011_B Output SR3 becomes activated. 100_B Output SR4 becomes activated. 101_B Output SR5 becomes activated. *Note: All other settings of the bit field are reserved.*

(continued)

Field	Bits	Type	Description
SIZE	26:24	rw	**Buffer Size** This bit field defines the number of FIFO entries assigned to the transmit FIFO buffer. 000_B The FIFO mechanism is disabled. The buffer does not accept any request for data. 001_B The FIFO buffer contains 2 entries. 010_B The FIFO buffer contains 4 entries. 011_B The FIFO buffer contains 8 entries. 100_B The FIFO buffer contains 16 entries. 101_B The FIFO buffer contains 32 entries. 110_B The FIFO buffer contains 64 entries. 111_B Reserved
LOF	28	rw	**Buffer Event on Limit Overflow** This bit defines which relation between filling level and programmed limit leads to a standard transmit buffer event. 0_B A standard transmit buffer event occurs when the filling level equals the limit value and gets lower due to transmission of a data word. 1_B A standard transmit buffer interrupt event occurs when the filling level equals the limit value and gets bigger due to a write access to a data input location INx.
STBIEN	30	rw	**Standard Transmit Buffer Interrupt Enable** This bit enables/disables the generation of a standard transmit buffer interrupt in case of a standard transmit buffer event. 0_B The standard transmit buffer interrupt generation is disabled. 1_B The standard transmit buffer interrupt generation is enabled.
TBERIEN	31	rw	**Transmit Buffer Error Interrupt Enable** This bit enables/disables the generation of a transmit buffer error interrupt in case of a transmit buffer error event (software writes to a full transmit buffer). 0_B The transmit buffer error interrupt generation is disabled. 1_B The transmit buffer error interrupt generation is enabled.
0	7:6, 23:22, 27, 29	r	**Reserved** Read as 0; should be written with 0.

18.10.9.4 Receive FIFO Buffer Control Registers

The receive FIFO buffer is controlled by register RBCTR. This register can only be written if the receive buffer functionality is enabled by CCFG.RB = 1, otherwise write accesses are ignored.

18.10.9.4.1 Register RBCTR

RBCTR Address: $10C_H$

Receiver Buffer Control Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RBERIEN	**SRBIEN**	**ARBIEN**	**LOF**	**RNM**	**SIZE**			**RCIM**		**ARBINP**			**SRBINP**		
rw	rw	rw	rw	rw	rw			rw		rw			rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRBTEN	**SRBTM**	**LIMIT**						**0**		**DPTR**					
rw	rw	rw						r		w					

Field	Bits	Type	Description
DPTR	5:0	w	**Data Pointer** This bit field defines the start value for the receive buffer pointers when assigning the FIFO entries to the receive FIFO buffer. A read always delivers 0. When writing DPTR while SIZE = 0, both receiver pointers RDIPTR and RDOPTR in register TRBPTR are updated with the written value and the buffer is considered as empty. A write access to DPTR while SIZE > 0 is ignored and does not modify the pointers.
LIMIT	13:8	rw	**Limit For Interrupt Generation** This bit field defines the target filling level of the receive FIFO buffer that is used for the standard receive buffer event detection.
SRBTM	14	rw	**Standard Receive Buffer Trigger Mode** This bit selects the standard receive buffer event trigger mode. 0_B Trigger mode 0: While TRBSR.SRBT=1, a standard receive buffer event will be generated whenever there is a new data received or data read out (depending on RBCTR.LOF setting). SRBT is cleared when TRBSR.RBFLVL=RBCTR.LIMIT. 1_B Trigger mode 1: While TRBSR.SRBT=1, a standard receive buffer event will be generated whenever there is a new data received or data read out (depending on RBCTR.LOF setting). SRBT is cleared when TRBSR.RBFLVL=0.
SRBTEN	15	rw	**Standard Receive Buffer Trigger Enable** This bit enables/disables triggering of the standard receive buffer event through bit TRBSR.SRBT. 0_B The standard receive buffer event trigger through bit TRBSR.SRBT is disabled. 1_B The standard receive buffer event trigger through bit TRBSR.SRBT is enabled.

(continued)

Field	Bits	Type	Description
SRBINP	18:16	rw	**Standard Receive Buffer Interrupt Node Pointer** This bit field defines which service request output SRx becomes activated in case of a standard receive buffer event. 000_B Output SR0 becomes activated. 001_B Output SR1 becomes activated. 010_B Output SR2 becomes activated. 011_B Output SR3 becomes activated. 100_B Output SR4 becomes activated. 101_B Output SR5 becomes activated. *Note: All other settings of the bit field are reserved.*
ARBINP	21:19	rw	**Alternative Receive Buffer Interrupt Node Pointer** This bit field defines which service request output SRx becomes activated in case of an alternative receive buffer event or a receive buffer error event. 000_B Output SR0 becomes activated. 001_B Output SR1 becomes activated. 010_B Output SR2 becomes activated. 011_B Output SR3 becomes activated. 100_B Output SR4 becomes activated. 101_B Output SR5 becomes activated. *Note: All other settings of the bit field are reserved.*
RCIM	23:22	rw	**Receiver Control Information Mode** This bit field defines which information from the receiver status register RBUFSR is propagated as 5 bit receiver control information RCI[4:0] to the receive FIFO buffer and can be read out in registers OUT(D)R. 00_B RCI[4] = PERR, RCI[3:0] = WLEN 01_B RCI[4] = SOF, RCI[3:0] = WLEN 10_B RCI[4] = 0, RCI[3:0] = WLEN 11_B RCI[4] = PERR, RCI[3] = PAR, RCI[2:1] = 00_B, RCI[0] = SOF
SIZE	26:24	rw	**Buffer Size** This bit field defines the number of FIFO entries assigned to the receive FIFO buffer. 000_B The FIFO mechanism is disabled. The buffer does not accept any request for data. 001_B The FIFO buffer contains 2 entries. 010_B The FIFO buffer contains 4 entries. 011_B The FIFO buffer contains 8 entries. 100_B The FIFO buffer contains 16 entries. 101_B The FIFO buffer contains 32 entries. 110_B The FIFO buffer contains 64 entries. 111_B Reserved

(continued)

Field	Bits	Type	Description
RNM	27	rw	**Receiver Notification Mode** This bit defines the receive buffer event mode. The receive buffer error event is not affected by RNM. 0_B Filling level mode: A standard receive buffer event occurs when the filling level equals the limit value and changes, either due to a read access from OUTR (LOF = 0) or due to a new received data word (LOF = 1). 1_B RCI mode: A standard receive buffer event occurs when register OUTR is updated with a new value if the corresponding value in OUTR.RCI[4] = 0. If OUTR.RCI[4] = 1, an alternative receive buffer event occurs instead of the standard receive buffer event.
LOF	28	rw	**Buffer Event on Limit Overflow** This bit defines which relation between filling level and programmed limit leads to a standard receive buffer event in filling level mode (RNM = 0). In RCI mode (RNM = 1), bit fields LIMIT and LOF are ignored. 0_B A standard receive buffer event occurs when the filling level equals the limit value and gets lower due to a read access from OUTR. 1_B A standard receive buffer event occurs when the filling level equals the limit value and gets bigger due to the reception of a new data word.
ARBIEN	29	rw	**Alternative Receive Buffer Interrupt Enable** This bit enables/disables the generation of an alternative receive buffer interrupt in case of an alternative receive buffer event. 0_B The alternative receive buffer interrupt generation is disabled. 1_B The alternative receive buffer interrupt generation is enabled.
SRBIEN	30	rw	**Standard Receive Buffer Interrupt Enable** This bit enables/disables the generation of a standard receive buffer interrupt in case of a standard receive buffer event. 0_B The standard receive buffer interrupt generation is disabled. 1_B The standard receive buffer interrupt generation is enabled.
RBERIEN	31	rw	**Receive Buffer Error Interrupt Enable** This bit enables/disables the generation of a receive buffer error interrupt in case of a receive buffer error event (the software reads from an empty receive buffer). 0_B The receive buffer error interrupt generation is disabled. 1_B The receive buffer error interrupt generation is enabled.
0	7:6	r	**Reserved** Read as 0; should be written with 0.

18.10.9.5 FIFO Buffer Data Registers

18.10.9.5.1 Register INx

The 32 independent data input locations IN00 to IN31 are addresses that can be used as data entry locations for the transmit FIFO buffer. Data written to one of these locations will be stored in the transmit buffer FIFO. Additionally, the 5-bit coding of the number [31:0] of the addressed data input location represents the transmit control information TCI.

If the FIFO is already full and new data is written to it, the write access is ignored and a transmit buffer error event is signaled.

INx (x = 00-31) Address: $180_H + x * 4$

Transmit FIFO Buffer Input Location x Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDATA															
w															

Field	Bits	Type	Description
TDATA	15:0	w	**Transmit Data** This bit field contains the data to be transmitted (write view), read actions deliver 0. A write action to at least the low byte of TDATA triggers the data storage in the FIFO.
0	31:16	r	**Reserved** Read as 0; should be written with 0.

18.10.9.5.2 Register OUTR

The receiver FIFO buffer output register OUTR shows the oldest received data word in the FIFO buffer and contains the receiver control information RCI containing the information selected by RBCTR.RCIM. A read action from this address location delivers the received data. With a read access of at least the low byte, the data is declared to be read and the next entry becomes visible. Write accesses to OUTR are ignored.

OUTR Address: $11C_H$

Receiver Buffer Output Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0											**RCI**				
r											rh				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DSR															
rh															

Field	Bits	Type	Description
DSR	15:0	rh	**Received Data** This bit field monitors the content of the oldest data word in the receive FIFO. Reading at least the low byte releases the buffer entry currently shown in DSR.
RCI	20:16	rh	**Receiver Control Information** This bit field monitors the receiver control information associated to DSR. The bit structure of RCI depends on bit field RBCTR.RCIM.
0	31:21	r	**Reserved** Read as 0; should be written with 0.

18.10.9.5.3 Register OUTDR

If a debugger should be used to monitor the received data in the FIFO buffer, the FIFO mechanism must not be activated in order to guaranty data consistency. Therefore, a second address set is available, named OUTDR (D like debugger), having the same bit fields like the original buffer output register OUTR, but without the FIFO mechanism. A debugger can read here (in order to monitor the receive data flow) without the risk of data corruption. Write accesses to OUTDR are ignored.

OUTDR Address: 120_H

Receiver Buffer Output Register L for Debugger Reset Value: $0000\ 0000_H$



Field	Bits	Type	Description
DSR	15:0	rh	**Data from Shift Register** Same as OUTR.DSR, but without releasing the buffer after a read action.
RCI	20:16	rh	**Receive Control Information from Shift Register** Same as OUTR.RCI.
0	31:21	r	**Reserved** Read as 0; should be written with 0.

18.10.9.6 FIFO Buffer Pointer Registers

The pointers for FIFO handling of the transmit and receive FIFO buffers are located in register TRBPTR. The pointers are automatically handled by the FIFO buffer mechanism and do not need to be modified by software. As a consequence, these registers can only be read by software (e.g. for verification purposes), whereas write accesses are ignored.

18.10.9.6.1 Register TRBPTR

TRBPTR Address: 110_H

Transmit/Receive Buffer Pointer Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0		**RDOPTR**						**0**		**RDIPTR**					
r		rh						r		rh					

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		**TDOPTR**						**0**		**TDIPTR**					
r		rh						r		rh					

Field	Bits	Type	Description
TDIPTR	5:0	rh	**Transmitter Data Input Pointer** This bit field indicates the buffer entry that will be used for the next transmit data coming from the INx addresses.
TDOPTR	13:8	rh	**Transmitter Data Output Pointer** This bit field indicates the buffer entry that will be used for the next transmit data to be output to TBUF.
RDIPTR	21:16	rh	**Receiver Data Input Pointer** This bit field indicates the buffer entry that will be used for the next receive data coming from RBUF.
RDOPTR	29:24	rh	**Receiver Data Output Pointer** This bit field indicates the buffer entry that will be used for the next receive data to be output at the OUT(D)R addresses.
0	7:6, 15:14, 23:22, 31:30	r	**Reserved** Read as 0; should be written with 0.

18.11 Interconnects

The IMC300A device contains two USIC modules (USIC0 and USIC1) with 2 communication channels each but one channel is required for the JCOM interface.

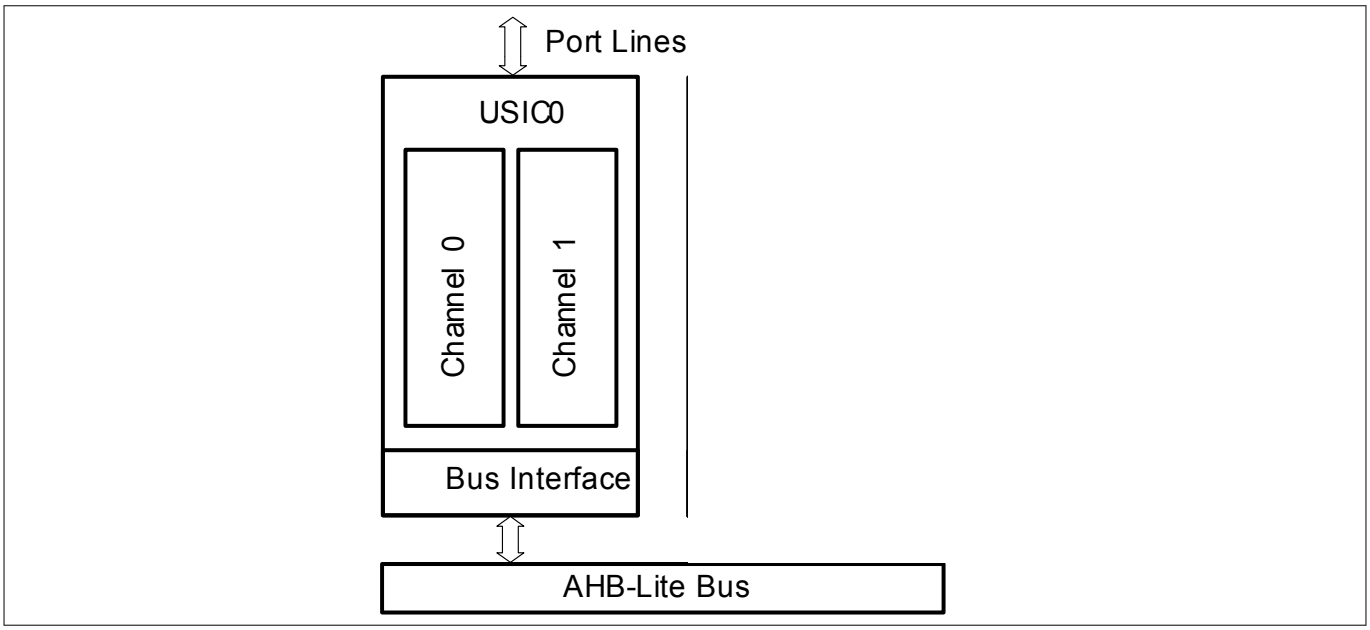


Figure 118 USIC Module Structure in IMC300A

The next sections define the pin assignments and internal connections of each USIC module and channel in the IMC300A device.

The meaning of these I/O lines with respect to each protocol is described in the protocols' respective chapters and summarized in ***Table 186*** and ***Table 187***.

Naming convention: USICx_CHy refers to USIC module x channel y.

18.11.1 USIC0 Module Interconnects

The interconnects of USIC0 module is grouped into the following categories:

- USIC0_CH0 Interconnects (***Chapter 18.11.1.1***)
- USIC0_CH1 Interconnects (***Chapter 18.11.1.2***)
- USIC0 Global Interconnects (***Chapter 18.11.1.3***)

18.11.1.1 USIC0 Channel 0 Interconnects

Table 220 shows the interconnects for USIC0 Channel 0.

Table 220 USIC0 Channel 0 Interconnects

Input/Output	I/O	Connected To	Description
Data Inputs (DX0)			
USIC0_CH0.DX0A	I	P0.14	Shift data input; used for: • ASC RXD • SSC MTSR/MRST • IIC SDA
USIC0_CH0.DX0B	I	P0.15	
USIC0_CH0.DX0C	I	P1.0	
USIC0_CH0.DX0D	I	P1.1	
USIC0_CH0.DX0E	I	P2.0	
USIC0_CH0.DX0F	I	P2.1	
USIC0_CH0.DX0G	I	USIC0_CH0.DX3INS	

Table 220 USIC0 Channel 0 Interconnects (continued)

Input/Output	I/O	Connected To	Description
USIC0_CH0.HWIN0	I	P1.0	HW controlled shift data input
Clock Inputs			
USIC0_CH0.DX1A	I	P0.14	Shift clock input; used for: • SSC Slave SCLKIN • IIC SCL • Optional for ASC, SSC Master
USIC0_CH0.DX1B	I	P0.8	
USIC0_CH0.DX1C	I		
USIC0_CH0.DX1D	I	P1.1	
USIC0_CH0.DX1E	I	P2.0	
USIC0_CH0.DX1F	I	USIC0_CH0.DX0INS	
USIC0_CH0.DX1G	I	USIC0_CH0.DX4INS	
Control Inputs			
USIC0_CH0.DX2A	I		Shift control input; used for: • SSC Slave SELIN • Optional for ASC, SSC Master, IIC Master
USIC0_CH0.DX2B	I	P0.9	
USIC0_CH0.DX2C	I	P0.10	
USIC0_CH0.DX2D	I	P0.11	
USIC0_CH0.DX2E	I	P0.12	
USIC0_CH0.DX2F	I	P0.13	
USIC0_CH0.DX2G	I	USIC0_CH0.DX5INS	
Data Inputs (DX3)			
USIC0_CH0.DX3A	I	P2.2	Shift data input; used for: • Dual and Quad SSC MTSR1/MRST1 • Can be ignored for all other protocols
USIC0_CH0.DX3B	I		
USIC0_CH0.DX3C	I	P2.10	
USIC0_CH0.DX3D	I	P2.8	
USIC0_CH0.DX3E	I	P2.6	
USIC0_CH0.DX3F	I	USIC0_CH0.DX5INS	
USIC0_CH0.DX3G	I	USIC0_CH0.DOUT0	
USIC0_CH0.HWIN1	I	P1.1	HW controlled shift data input
Data Inputs (DX4)			
USIC0_CH0.DX4A	I	P2.2	Shift data input; used for: • Quad SSC MTSR2/MRST2 • Can be ignored for all other protocols
USIC0_CH0.DX4B	I		
USIC0_CH0.DX4C	I	P2.10	
USIC0_CH0.DX4D	I	P2.8	
USIC0_CH0.DX4E	I	P2.6	
USIC0_CH0.DX4F	I	USIC0_CH0.DX5INS	
USIC0_CH0.DX4G	I	USIC0_CH0.SCLKOUT	

Table 220 USIC0 Channel 0 Interconnects (continued)

Input/Output	I/O	Connected To	Description
USIC0_CH0.HWIN2	I		HW controlled shift data input
Data Inputs (DX5)			
USIC0_CH0.DX5A	I		Shift data input; used for: • Quad SSC MTSR3/MRST3 • Can be ignored for all other protocols
USIC0_CH0.DX5B	I		
USIC0_CH0.DX5C	I		
USIC0_CH0.DX5D	I		
USIC0_CH0.DX5E	I		
USIC0_CH0.DX5F	I		
USIC0_CH0.DX5G	I	USIC0_CH0.SELO0	
USIC0_CH0.HWIN3	I		HW controlled shift data input
Data Outputs			
USIC0_CH0.DOUT0	O	P0.14; P0.15; P1.0; P1.1; P2.0; P2.1; P1.0 (HW1_OUT); USIC0_CH0.DX3G;	Shift data output; used for: • ASC TXD • SSC MTSR/MRST • IIC SDA
USIC0_CH0.DOUT1	O	P1.1 (HW1_OUT)	Shift data output; used for: • Dual and Quad SSC MTSR1/MRST1 • Can be ignored for all other protocols
USIC0_CH0.DOUT2	O		Shift data output; used for: • Quad SSC MTSR2/MRST2 • Can be ignored for all other protocols
USIC0_CH0.DOUT3	O		Shift data output; used for: • Quad SSC MTSR3/MRST3 • Can be ignored for all other protocols
Clock Outputs			
USIC0_CH0.MCLKOUT	O	P0.11	Master clock output (optional for all protocols)
USIC0_CH0.SCLKOUT	O	P0.8; P0.14; P2.0; USIC0_CH0.DX4G;	Shift clock output; used for: • Master SCLKOUT in SSC • IIC SCL • Can be ignored in ASC
Control Outputs			

Table 220 USIC0 Channel 0 Interconnects (continued)

Input/Output	I/O	Connected To	Description
USIC0_CH0.SELO0	O	P0.9; USIC0_CH0.DX5G	Shift control output; used for: • SSC Master SELO • Can be ignored for all other protocols
USIC0_CH0.SELO1	O	P0.10;	
USIC0_CH0.SELO2	O	P0.11;	
USIC0_CH0.SELO3	O	P0.12	
USIC0_CH0.SELO4	O	P0.13	
USIC0_CH0.SELO5	O	not connected	
USIC0_CH0.SELO6	O	not connected	
USIC0_CH0.SELO7	O	not connected	
System Related Outputs			
USIC0_CH0.DX0INS	O	USIC0_CH0.DX1F	Selected DX0 input signal
USIC0_CH0.DX1INS	O	not connected	Selected DX1 input signal
USIC0_CH0.DX2INS	O	CCU40.IN0AL	Selected DX2 input signal
USIC0_CH0.DX3INS	O	USIC0_CH0.DX0G	Selected DX3 input signal
USIC0_CH0.DX4INS	O	USIC0_CH0.DX1G	Selected DX4 input signal
USIC0_CH0.DX5INS	O	USIC0_CH0.DX2G; USIC0_CH0.DX3F; USIC0_CH0.DX4F	Selected DX5 input signal

18.11.1.2 USIC0 Channel 1 Interconnects

Table 221 shows the interconnects for USIC0 Channel 1.

Table 221 USIC0 Channel 1 Interconnects

Input/Output	I/O	Connected To	Description
Data Inputs (DX0)			
USIC0_CH1.DX0A	I		Shift data input; used for: • ASC RXD • SSC MTSR/MRST • IIC SDA
USIC0_CH1.DX0B	I		
USIC0_CH1.DX0C	I		
USIC0_CH1.DX0D	I		
USIC0_CH1.DX0E	I	P2.11	
USIC0_CH1.DX0F	I	P2.10	
USIC0_CH1.DX0G	I	USIC0_CH1.DX3INS	
USIC0_CH1.HWIN0	I	ERU0.PDOUT0	HW controlled shift data input
Clock Inputs			

Table 221 USIC0 Channel 1 Interconnects (continued)

Input/Output	I/O	Connected To	Description
USIC0_CH1.DX1A	I		Shift clock input; used for: • SSC Slave SCLKIN • IIC SCL • Optional for ASC, SSC Master
USIC0_CH1.DX1B	I	P0.8	
USIC0_CH1.DX1C	I		
USIC0_CH1.DX1D	I	0	
USIC0_CH1.DX1E	I	P2.11	
USIC0_CH1.DX1F	I	USIC0_CH1.DX0INS	
USIC0_CH1.DX1G	I	USIC0_CH1.DX4INS	
Control Inputs			
USIC0_CH1.DX2A	I		Shift control input; used for: • SSC Slave SELIN • Optional for ASC, SSC Master, IIC Master
USIC0_CH1.DX2B	I	P0.9	
USIC0_CH1.DX2C	I	P0.10	
USIC0_CH1.DX2D	I	P0.11	
USIC0_CH1.DX2E	I	P1.1	
USIC0_CH1.DX2F	I	P2.0	
USIC0_CH1.DX2G	I	USIC0_CH1.DX5INS	
Data Inputs (DX3)			
USIC0_CH1.DX3A	I	P2.1	Shift data input; used for: • Dual and Quad SSC MTSR1/MRST1 • Can be ignored for all other protocols
USIC0_CH1.DX3B	I		
USIC0_CH1.DX3C	I		
USIC0_CH1.DX3D	I		
USIC0_CH1.DX3E	I		
USIC0_CH1.DX3F	I	USIC0_CH1.DX5INS	
USIC0_CH1.DX3G	I	USIC0_CH1.DOUT0	
USIC0_CH1.HWIN1	I	0	HW controlled shift data input
Data Inputs (DX4)			
USIC0_CH1.DX4A	I	P2.1	Shift data input; used for: • Quad SSC MTSR2/MRST2 • Can be ignored for all other protocols
USIC0_CH1.DX4B	I		
USIC0_CH1.DX4C	I		
USIC0_CH1.DX4D	I		
USIC0_CH1.DX4E	I		
USIC0_CH1.DX4F	I	USIC0_CH1.DX5INS	
USIC0_CH1.DX4G	I	USIC0_CH1.SCLKOUT	
USIC0_CH1.HWIN2	I	ERU0.PDOUT1	HW controlled shift data input
Data Inputs (DX5)			

Table 221 USIC0 Channel 1 Interconnects (continued)

Input/Output	I/O	Connected To	Description
USIC0_CH1.DX5A	I	P2.2	Shift data input; used for: • Quad SSC MTSR3/MRST3 • Can be ignored for all other protocols
USIC0_CH1.DX5B	I		
USIC0_CH1.DX5C	I	P2.8	
USIC0_CH1.DX5D	I	P2.6	
USIC0_CH1.DX5E	I		
USIC0_CH1.DX5F	I		
USIC0_CH1.DX5G	I	USIC0.SR0	
USIC0_CH1.HWIN3	I	USIC0_CH1.DOUT0	HW controlled shift data input
Data Outputs			
USIC0_CH1.DOUT0	O	P2.10; P2.11; USIC0_CH1.DX3G; USIC0_CH1.HWIN3;	Shift data output; used for: • ASC TXD • SSC MTSR/MRST • IIC SDA
USIC0_CH1.DOUT1	O	not connected	Shift data output; used for: • Dual and Quad SSC MTSR1/MRST1 • Can be ignored for all other protocols
USIC0_CH1.DOUT2	O	not connected	Shift data output; used for: • Quad SSC MTSR2/MRST2 • Can be ignored for all other protocols
USIC0_CH1.DOUT3	O	not connected	Shift data output; used for: • Quad SSC MTSR3/MRST3 • Can be ignored for all other protocols
Clock Outputs			
USIC0_CH1.MCLKOUT	O	P0.15;	Master clock output (optional for all protocols)
USIC0_CH1.SCLKOUT	O	P0.8; P2.1; P2.11; USIC0_CH1.DX4G;	Shift clock output; used for: • Master SCLKOUT in SSC • IIC SCL • Can be ignored in ASC
Control Outputs			
USIC0_CH1.SELO0	O	P0.9; P1.1;	Shift control output; used for: • SSC Master SELO • Can be ignored for all other protocols
USIC0_CH1.SELO1	O	P0.10;	
USIC0_CH1.SELO2	O	P0.11;	
USIC0_CH1.SELO3	O		

Table 221 USIC0 Channel 1 Interconnects (continued)

Input/Output	I/O	Connected To	Description
USIC0_CH1.SELO4	O	not connected	
USIC0_CH1.SELO5	O	not connected	
USIC0_CH1.SELO6	O	not connected	
USIC0_CH1.SELO7	O	not connected	
System Related Outputs			
USIC0_CH1.DX0INS	O	USIC0_CH1.DX1F	Selected DX0 input signal
USIC0_CH1.DX1INS	O	not connected	Selected DX1 input signal
USIC0_CH1.DX2INS	O	CCU40.IN1AL	Selected DX2 input signal
USIC0_CH1.DX3INS	O	USIC0_CH1.DX0G	Selected DX3 input signal
USIC0_CH1.DX4INS	O	USIC0_CH1.DX1G	Selected DX4 input signal
USIC0_CH1.DX5INS	O	USIC0_CH1.DX2G; USIC0_CH1.DX3F; USIC0_CH1.DX4F;	Selected DX5 input signal

18.11.1.3 USIC0 Global Interconnects

Table 222 shows the global interconnects for USIC0 module.

Table 222 USIC0 Global Interconnects

Input/Output	I/O	Connected To	Description
USIC0_SR0	O	NVIC; USIC0_CH1.DX5G	Service request Output 0
USIC0_SR1	O	NVIC	Service request Output 1
USIC0_SR2	O	NVIC	Service request Output 2
USIC0_SR3	O	NVIC	Service request Output 3
USIC0_SR4	O	NVIC	Service request Output 4
USIC0_SR5	O	NVIC	Service request Output 5

18.11.2 USIC1 Module Interconnects

The interconnects of USIC1 module is grouped into the following categories:

- USIC1_CH0 Interconnects (***Chapter 18.11.2.1***)
- USIC1_CH1 Interconnects (***Chapter 18.11.2.2***)
- USIC1 Global Interconnects (***Chapter 18.11.2.3***)

18.11.2.1 USIC1 Channel 0 Interconnects

Table 223 shows the interconnects for USIC1 Channel 0.

Table 223 USIC1 Channel 0 Interconnects

Input/Output	I/O	Connected To	Description
Data Inputs (DX0)			
USIC1_CH0.DX0A	I		Shift data input; used for: • ASC RXD • SSC MTSR/MRST • IIC SDA
USIC1_CH0.DX0B	I		
USIC1_CH0.DX0C	I	P4.4	
USIC1_CH0.DX0D	I	P4.5	
USIC1_CH0.DX0E	I		
USIC1_CH0.DX0F	I		
USIC1_CH0.DX0G	I	USIC1_CH0.DX3INS	
USIC1_CH0.HWIN0	I		HW controlled shift data input
Clock Inputs			
USIC1_CH0.DX1A	I		Shift clock input; used for: • SSC Slave SCLKIN • IIC SCL • Optional for ASC, SSC Master
USIC1_CH0.DX1B	I	P4.3	
USIC1_CH0.DX1C	I	P4.5	
USIC1_CH0.DX1D	I	P4.6	
USIC1_CH0.DX1E	I		
USIC1_CH0.DX1F	I	USIC1_CH0.DX0INS	
USIC1_CH0.DX1G	I	USIC1_CH0.DX4INS	
Control Inputs			
USIC1_CH0.DX2A	I	P4.7	Shift control input; used for: • SSC Slave SELIN • Optional for ASC, SSC Master, IIC Master
USIC1_CH0.DX2B	I		
USIC1_CH0.DX2C	I		
USIC1_CH0.DX2D	I		
USIC1_CH0.DX2E	I		
USIC1_CH0.DX2F	I		
USIC1_CH0.DX2G	I	USIC1_CH0.DX5INS	
Data Inputs (DX3)			
USIC1_CH0.DX3A	I		Shift data input; used for: • Dual and Quad SSC MTSR1/MRST1 • Can be ignored for all other protocols
USIC1_CH0.DX3B	I		
USIC1_CH0.DX3C	I		
USIC1_CH0.DX3D	I	P4.0	
USIC1_CH0.DX3E	I		
USIC1_CH0.DX3F	I	USIC1_CH0.DX5.INS	
USIC1_CH0.DX3G	I	USIC1_CH0.DOUT0	
USIC1_CH0.HWIN1	I		HW controlled shift data input

Table 223 USIC1 Channel 0 Interconnects (continued)

Input/Output	I/O	Connected To	Description
Data Inputs (DX4)			
USIC1_CH0.DX4A	I		Shift data input; used for: • Quad SSC MTSR2/MRST2 • Can be ignored for all other protocols
USIC1_CH0.DX4B	I		
USIC1_CH0.DX4C	I		
USIC1_CH0.DX4D	I	P4.0	
USIC1_CH0.DX4E	I		
USIC1_CH0.DX4F	I	USIC1_CH0.DX5INS	
USIC1_CH0.DX4G	I	USIC1_CH0.SCLKOUT0	
USIC1_CH0.HWIN2	I		HW controlled shift data input
Data Inputs (DX5)			
USIC1_CH0.DX5A	I		Shift data input; used for: • Quad SSC MTSR3/MRST3 • Can be ignored for all other protocols
USIC1_CH0.DX5B	I		
USIC1_CH0.DX5C	I	P4.1	
USIC1_CH0.DX5D	I	P4.2	
USIC1_CH0.DX5E	I	P2.2	
USIC1_CH0.DX5F	I		
USIC1_CH0.DX5G	I	USIC1_CH0.SELO0	
USIC1_CH0.HWIN3	I		HW controlled shift data input
Data Outputs			
USIC1_CH0.DOUT0	O	P4.4; P4.5; USIC1_CH0.DX3G	Shift data output; used for: • ASC TXD • SSC MTSR/MRST • IIC SDA
USIC1_CH0.DOUT1	O		Shift data output; used for: • Dual and Quad SSC MTSR1/MRST1 • Can be ignored for all other protocols
USIC1_CH0.DOUT2	O		Shift data output; used for: • Quad SSC MTSR2/MRST2 • Can be ignored for all other protocols
USIC1_CH0.DOUT3	O		Shift data output; used for: • Quad SSC MTSR3/MRST3 • Can be ignored for all other protocols
Clock Outputs			
USIC1_CH0.MCLKOUT	O		Master clock output (optional for all protocols)

Table 223 USIC1 Channel 0 Interconnects (continued)

Input/Output	I/O	Connected To	Description
USIC1_CH0.SCLKOUT	O	P4.3; P4.5; P4.6; USIC1_CH0.DX4G	Shift clock output; used for: • Master SCLKOUT in SSC • IIC SCL • Can be ignored in ASC
Control Outputs			
USIC1_CH0.SELO0	O	P4.7; USIC1_CH0.DX5G;	Shift control output; used for: • SSC Master SELO • Can be ignored for all other protocols
USIC1_CH0.SELO1	O		
USIC1_CH0.SELO2	O		
USIC1_CH0.SELO3	O		
USIC1_CH0.SELO4	O		
USIC1_CH0.SELO5	O	not connected	
USIC1_CH0.SELO6	O	not connected	
USIC1_CH0.SELO7	O	not connected	
System Related Outputs			
USIC1_CH0.DX0INS	O	USIC1_CH0.DX1F	Selected DX0 input signal
USIC1_CH0.DX1INS	O	not connected	Selected DX1 input signal
USIC1_CH0.DX2INS	O	CCU41.IN0BC	Selected DX2 input signal
USIC1_CH0.DX3INS	O	USIC1_CH0.DX0G	Selected DX3 input signal
USIC1_CH0.DX4INS	O	USIC1_CH0.DX1G	Selected DX4 input signal
USIC1_CH0.DX5INS	O	USIC1_CH0.DX2G; USIC1_CH0.DX3F; USIC1_CH0.DX4F	Selected DX5 input signal

Figure 119 shows a graphical representation of the USIC1 Channel 0 interconnects.

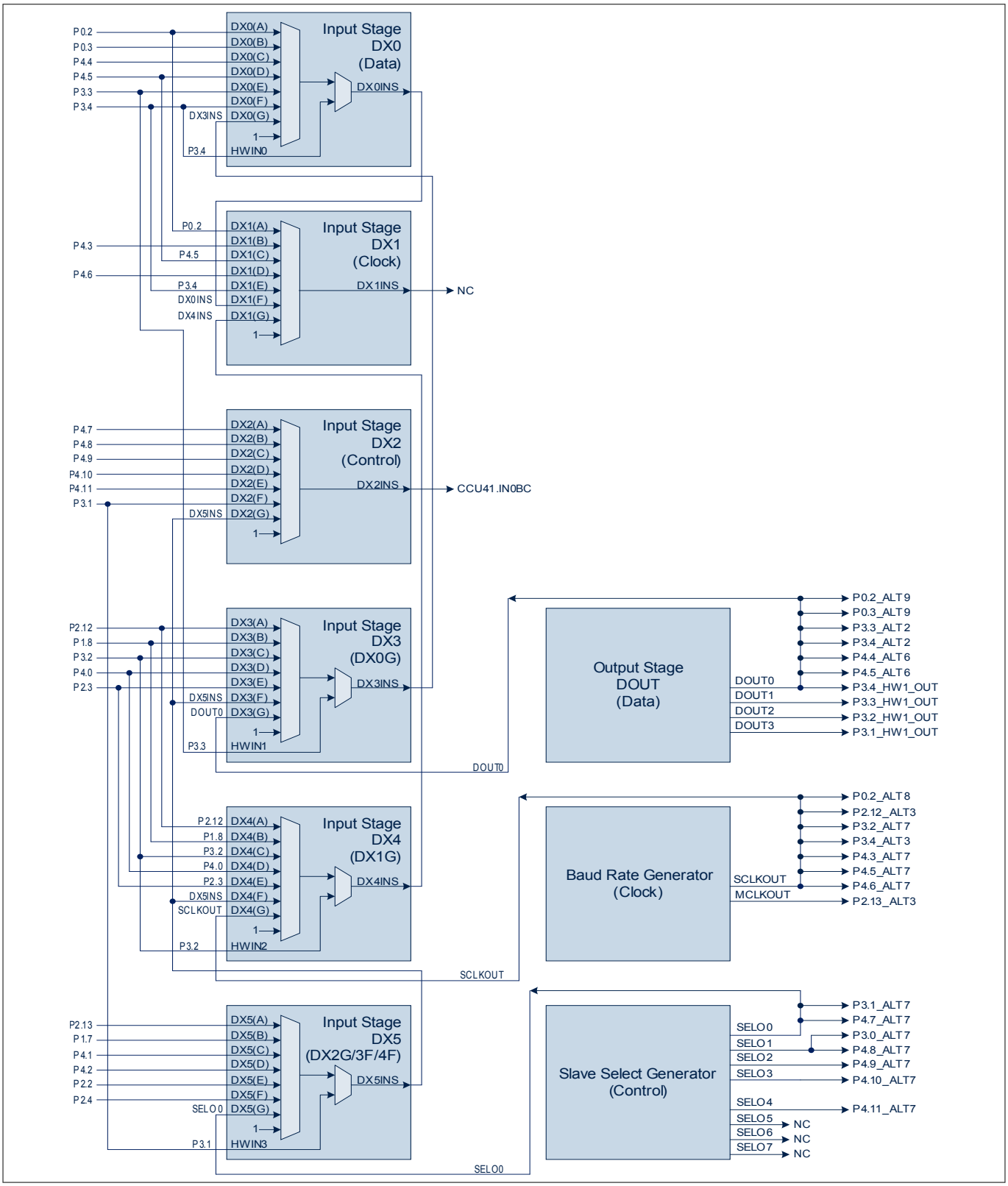


Figure 119 USIC1 Channel 0 Interconnects

18.11.2.2 USIC1 Channel 1 Interconnects

Table 224 shows the interconnects for USIC1 Channel 1.

Table 224 USIC1 Channel 1 Interconnects

Input/Output	I/O	Connected To	Description
Data Inputs (DX0)			
USIC1_CH1.DX0A	I		Shift data input; used for: • ASC RXD • SSC MTSR/MRST • IIC SDA
USIC1_CH1.DX0B	I		
USIC1_CH1.DX0C	I		
USIC1_CH1.DX0D	I		
USIC1_CH1.DX0E	I		
USIC1_CH1.DX0F	I		
USIC1_CH1.DX0G	I	USIC1_CH1.DX3INS	
USIC1_CH1.HWIN0	I	ERU1.PDOUT0	HW controlled shift data input
Clock Inputs			
USIC1_CH1.DX1A	I		Shift clock input; used for: • SSC Slave SCLKIN • IIC SCL • Optional for ASC, SSC Master
USIC1_CH1.DX1B	I		
USIC1_CH1.DX1C	I		
USIC1_CH1.DX1D	I		
USIC1_CH1.DX1E	I	0	
USIC1_CH1.DX1F	I	USIC1_CH1.DX0INS	
USIC1_CH1.DX1G	I	USIC1_CH1.DX4INS	
Control Inputs			
USIC1_CH1.DX2A	I		Shift control input; used for: • SSC Slave SELIN • Optional for ASC, SSC Master, IIC Master
USIC1_CH1.DX2B	I		
USIC1_CH1.DX2C	I		
USIC1_CH1.DX2D	I	0	
USIC1_CH1.DX2E	I	0	
USIC1_CH1.DX2F	I	USIC.SR0	
USIC1_CH1.DX2G	I	USIC1_CH1.DX5.INS	
Data Inputs (DX3)			
USIC1_CH1.DX3A	I		Shift data input; used for: • Dual and Quad SSC MTSR1/MRST1 • Can be ignored for all other protocols
USIC1_CH1.DX3B	I	P0.15	
USIC1_CH1.DX3C	I		
USIC1_CH1.DX3D	I		
USIC1_CH1.DX3E	I	P2.6	
USIC1_CH1.DX3F	I	USIC1_CH1.DX5.INS	
USIC1_CH1.DX3G	I	USIC1_CH1.DOUT0	
USIC1_CH1.HWIN1	I	0	HW controlled shift data input

Table 224 USIC1 Channel 1 Interconnects (continued)

Input/Output	I/O	Connected To	Description
Data Inputs (DX4)			
USIC1_CH1.DX4A	I		Shift data input; used for: • Quad SSC MTSR2/MRST2 • Can be ignored for all other protocols
USIC1_CH1.DX4B	I	P0.15	
USIC1_CH1.DX4C	I		
USIC1_CH1.DX4D	I		
USIC1_CH1.DX4E	I	P2.6	
USIC1_CH1.DX4F	I	USIC1_CH1.DX5INS	
USIC1_CH1.DX4G	I	USIC1_CH1.SCLKOUT0	
USIC1_CH1.HWIN2	I	ERU1.PDOUT1	HW controlled shift data input
Data Inputs (DX5)			
USIC1_CH1.DX5A	I		Shift data input; used for: • Quad SSC MTSR3/MRST3 • Can be ignored for all other protocols
USIC1_CH1.DX5B	I	P0.14	
USIC1_CH1.DX5C	I		
USIC1_CH1.DX5D	I		
USIC1_CH1.DX5E	I		
USIC1_CH1.DX5F	I	P4.4	
USIC1_CH1.DX5G	I	USIC1_CH1.SELO0	
USIC1_CH1.HWIN3	I	USIC1_CH1.DOUT0	HW controlled shift data input
Data Outputs			
USIC1_CH1.DOUT0	O	USIC1_CH1.DX3G; USIC1_CH1.HWIN3;	Shift data output; used for: • ASC TXD • SSC MTSR/MRST • IIC SDA
USIC1_CH1.DOUT1	O	not connected	Shift data output; used for: • Dual and Quad SSC MTSR1/MRST1 • Can be ignored for all other protocols
USIC1_CH1.DOUT2	O	not connected	Shift data output; used for: • Quad SSC MTSR2/MRST2 • Can be ignored for all other protocols
USIC1_CH1.DOUT3	O	not connected	Shift data output; used for: • Quad SSC MTSR3/MRST3 • Can be ignored for all other protocols
Clock Outputs			
USIC1_CH1.MCLKOUT	O		Master clock output (optional for all protocols)

Table 224 USIC1 Channel 1 Interconnects (continued)

Input/Output	I/O	Connected To	Description
USIC1_CH1.SCLKOUT	O	USIC1_CH1.DX4G;	Shift clock output; used for: • Master SCLKOUT in SSC • IIC SCL • Can be ignored in ASC
Control Outputs			
USIC1_CH1.SELO0	O	USIC1_CH1.DX5G;	Shift control output; used for: • SSC Master SELO • Can be ignored for all other protocols
USIC1_CH1.SELO1	O	P4.0;	
USIC1_CH1.SELO2	O	P4.1	
USIC1_CH1.SELO3	O	P4.2	
USIC1_CH1.SELO4	O	not connected	
USIC1_CH1.SELO5	O	not connected	
USIC1_CH1.SELO6	O	not connected	
USIC1_CH1.SELO7	O	not connected	
System Related Outputs			
USIC1_CH1.DX0INS	O	USIC1_CH0.DX1F	Selected DX0 input signal
USIC1_CH1.DX1INS	O	not connected	Selected DX1 input signal
USIC1_CH1.DX2INS	O	CCU41.IN0BC	Selected DX2 input signal
USIC1_CH1.DX3INS	O	USIC1_CH0.DX0G	Selected DX3 input signal
USIC1_CH1.DX4INS	O	USIC1_CH0.DX1G	Selected DX4 input signal
USIC1_CH1.DX5INS	O	USIC1_CH0.DX2G; USIC1_CH0.DX3F; USIC1_CH0.DX4F	Selected DX5 input signal

Figure 120 shows a graphical representation of the USIC1 Channel 1 interconnects.

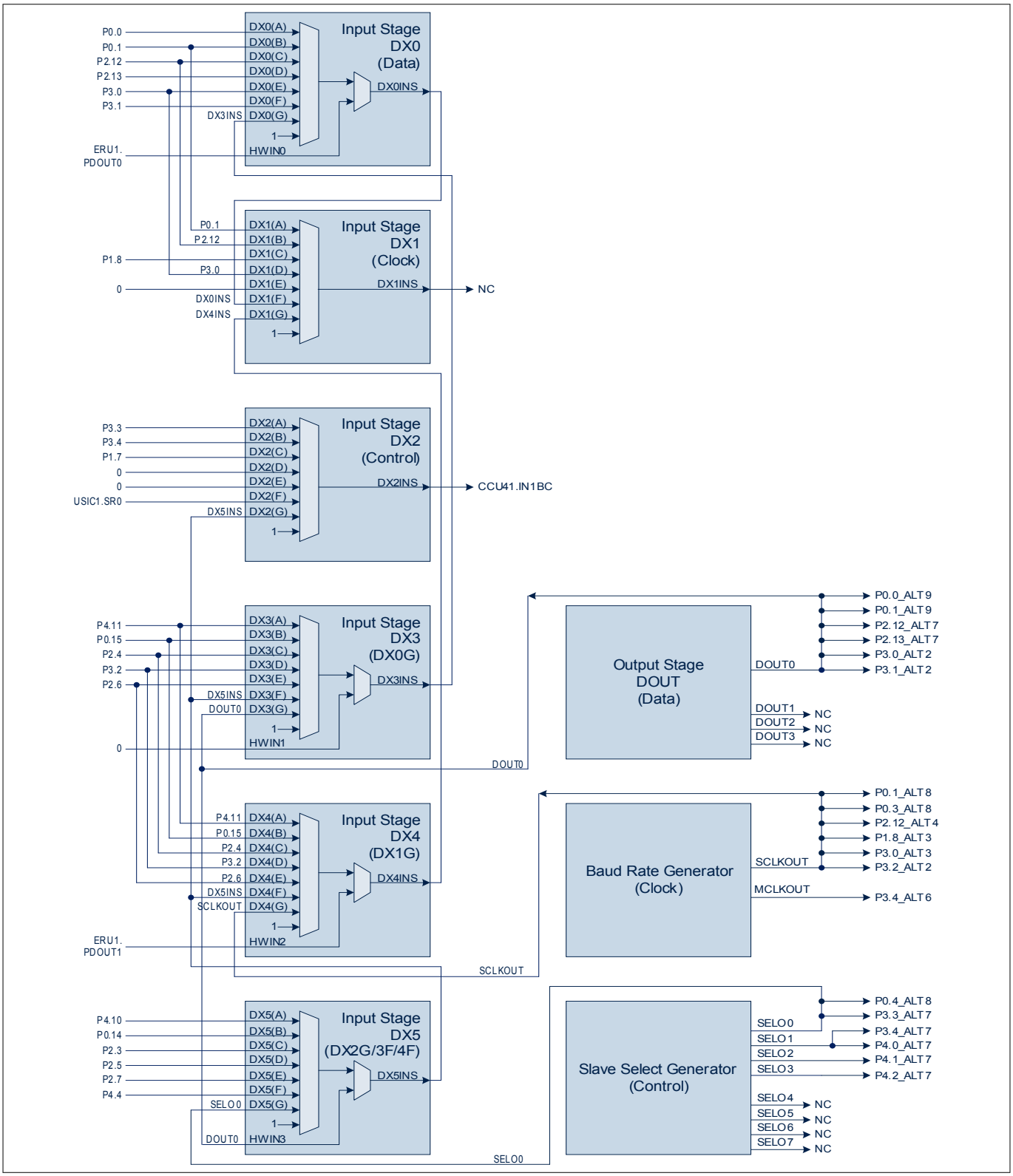


Figure 120 USIC1 Channel 1 Interconnects

18.11.2.3 USIC1 Global Interconnects

Table 225 shows the global interconnects for USIC1 module.

Table 225 USIC1 Global Interconnects

Input/Output	I/O	Connected To	Description
USIC1_SR0	O	NVIC; USIC1_CH1.DX2F	Service request Output 0
USIC1_SR1	O	NVIC	Service request Output 1
USIC1_SR2	O	NVIC	Service request Output 2
USIC1_SR3	O	NVIC	Service request Output 3
USIC1_SR4	O	NVIC	Service request Output 4
USIC1_SR5	O	NVIC	Service request Output 5

19 Controller Area Network Controller (MulticanCAN+)

This chapter describes the MulticanCAN+ controller of the IMC300A. It contains the following sections:

- CAN basics (see page ***521***)
- Overview of the CAN Module in the IMC300A (see page ***526***)
- Functional description of the MulticanCAN+ Kernel (see page ***528***)
- MulticanCAN+ Kernel register description (see page ***562***)
- IMC300A implementation-specific details (port connections and control, interrupt control, address decoding, clock control, see page ***600***).

Table 226 Fixed Module Constants

Constant	Description
n_objects	Number of Message Objects available.
n_interrupts	Number of Interrupt Output Lines available.
n_pendings n_pendingregs	Number of Message Pending Bits available. • There are n_pendings/32 message pending registers.
n_lists	Number of Lists available for allocation of Message Objects.
n_nodes	Number of CAN Nodes available • As each CAN node has its own list in addition to the list of un-allocated elements, the relation n_nodes < n_lists is true.

19.1 CAN Basics

CAN is an asynchronous serial bus system with one logical bus line. It has an open, linear bus structure with equal bus participants called nodes. A CAN bus consists of two or more nodes.

The bus logic corresponds to a “wired-AND” mechanism. Recessive bits (equivalent to the logic 1 level) are overwritten by dominant bits (logic 0 level). As long as no bus node is sending a dominant bit, the bus is in the recessive state. In this state, a dominant bit from any bus node generates a dominant bus state. The maximum CAN bus speed is, by definition, 1 Mbit/s. This speed limits the CAN bus to a length of up to 40 m. For bus lengths longer than 40 m, the bus speed must be reduced.

The binary data of a CAN frame is coded in NRZ code (Non-Return-to-Zero). To ensure re-synchronization of all bus nodes, bit stuffing is used. This means that during the transmission of a message, a maximum of five consecutive bits can have the same polarity. Whenever five consecutive bits of the same polarity have been transmitted, the transmitter will insert one additional bit (stuff bit) of the opposite polarity into the bit stream before transmitting further bits. The receiver also checks the number of bits with the same polarity and removes the stuff bits from the bit stream (= destuffing).

19.1.1 Addressing and Bus Arbitration

In the CAN protocol, address information is defined in the identifier field of a message. The identifier indicates the contents of the message and its priority. The lower the binary value of the identifier, the higher is the priority of the message.

For bus arbitration, CSMA/CD with NDA (Carrier Sense Multiple Access/Collision Detection with Non-Destructive Arbitration) is used. If bus node A attempts to transmit a message across the network, it first checks that the bus is in the idle state (“Carrier Sense”) i.e. no node is currently transmitting. If this is the case (and no other node wishes to start a transmission at the same moment), node A becomes the bus master and sends its message. All

other nodes switch to receive mode during the first transmitted bit (Start-Of-Frame bit). After correct reception of the message (acknowledged by each node), each bus node checks the message identifier and stores the message, if required. Otherwise, the message is discarded.

If two or more bus nodes start their transmission at the same time (“Multiple Access”), bus collision of the messages is avoided by bit-wise arbitration (“Collision Detection / Non-Destructive Arbitration” together with the “Wired-AND” mechanism, dominant bits override recessive bits). Each node that sends also reads back the bus level. When a recessive bit is sent but a dominant one is read back, bus arbitration is lost and the transmitting node switches to receive mode. This condition occurs for example when the message identifier of a competing node has a lower binary value and therefore sends a message with a higher priority. In this way, the bus node with the highest priority message wins arbitration without losing time by having to repeat the message. Other nodes that lost arbitration will automatically try to repeat their transmission once the bus returns to idle state. Therefore, the same identifier can be sent in a Data Frame only by one node in the system. There must not be more than one node programmed to send Data Frames with the same identifier.

Standard message identifier has a length of 11 bits. CAN specification 2.0B extended the message identifier lengths to 29 bits, i.e. the extended identifier. Both frame formats are part of the ISO 11898-1. The identifier is avaialble for Classical CAN.

19.1.2 CAN Frame Types

There are three types of CAN frames:

- Data Frames
- Remote Frames
- Error Frames

A Data Frame for Classical CAN contains a Data Field of 0 to 8 bytes in length. A Remote Frame contains no Data Field and is typically generated as a request for data (e.g. from a sensor). Data and Remote Frames can use an 11-bit “Standard” identifier or a 29-bit “Extended” identifier. An Error Frame can be generated by any node that detects a CAN bus error.

19.1.2.1 Data Frames

There are two types of Data Frames defined (see ***Figure 121***):

- 11bit ID Data Frame
- 29bit ID Data Frame

11-bit Data Frame (Classical CAN Format)

A Data Frame begins with the Start-Of-Frame bit (SOF = dominant level) for hard synchronization of all nodes. The SOF is followed by the Arbitration Field consisting of 12 bits, the 11-bit identifier (reflecting the contents and priority of the message), and the RTR (Remote Transmission Request for Classical CAN) bit. With RTR at dominant level, the frame is marked as Data Frame. With RTR at recessive level, the frame is defined as a Remote Frame.

The next field is the Control Field consisting of 6 bits. The first bit of this field is the IDE (Identifier Extension) bit and is at dominant level for the Standard Data Frame. The following bit is reserved and defined as a dominant bit. The remaining 4 bits of the Control Field are the Data Length Code (DLC) that specifies the number of bytes in the Data Field. The Data Field can be 0 to 8 bytes wide. The Cyclic Redundancy (CRC) Field that follows the data bytes is used to detect possible transmission errors. It consists of a 15-bit CRC sequence completed by a recessive CRC delimiter bit.

The final field is the Acknowledge Field. During the ACK Slot, the transmitting node sends out a recessive bit. Any node that has received an error free frame acknowledges the correct reception of the frame by sending back a dominant bit, regardless of whether or not the node is configured to accept that specific message. This behavior assigns the CAN protocol to the “in-bit-response” group of protocols. The recessive ACK delimiter bit, which must not be overwritten by a dominant bit, completes the Acknowledge Field.

Seven recessive End-of-Frame (EOF) bits finish the Data Frame. Between any two consecutive frames, the bus must remain in the recessive state for at least 3 bit times (called Inter Frame Space). If after the Inter Frame Space, no other nodes attempt to transmit the bus remains in idle state with a recessive level.

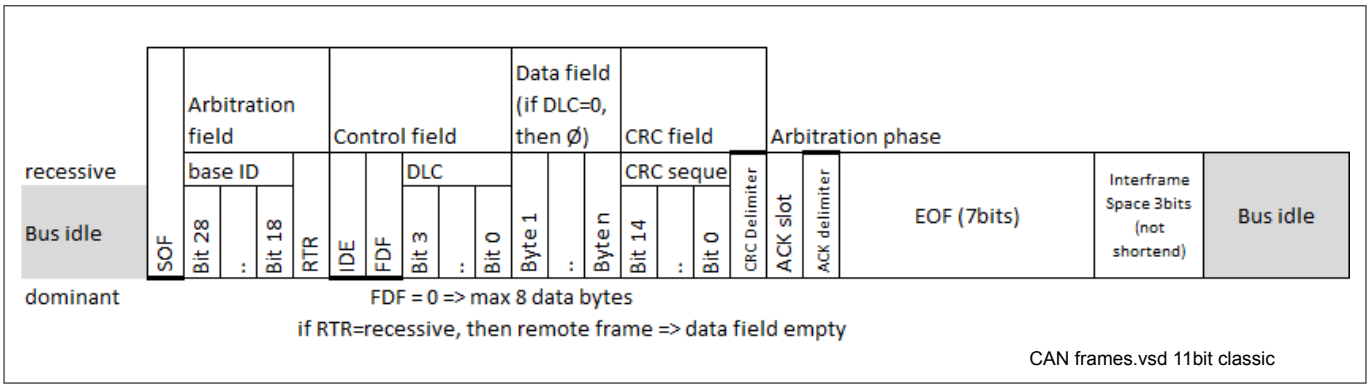


Figure 121 Classical11bit ID CAN Data Frame

Extended Data Frame (Classical CAN Format)

In the Extended CAN Data Frame, the message identifier of the standard frame has been extended to 29-bit. A split of the extended identifier into two parts, an 11-bit least significant section (as in classical CAN frame) and an 18-bit most significant section, ensures that the Identifier Extension bit (IDE) can remain at the same bit position in both standard and extended frames.

In the Extended CAN Data Frame, the SOF bit is followed by the 32-bit Arbitration Field. The first 11 bits are the least significant bits of the 29-bit Identifier (“Base-ID”). These 11 bits are followed by the recessive Substitute Remote Request (SRR) bit. The SRR is further followed by the recessive IDE bit, which indicates the frame to be an Extended CAN frame. If arbitration remains unresolved after transmission of the first 11 bits of the identifier, and if one of the nodes involved in arbitration is sending a classical CAN frame, then the CAN frame will win arbitration due to the assertion of its dominant IDE bit. Therefore, the SRR bit in an Extended CAN frame is recessive to allow the assertion of a dominant RTR bit by a node that is sending a CAN Remote Frame. The SRR and IDE bits are followed by the remaining 18 bits of the extended identifier and the RTR bit.

Control field and frame termination is identical to the Classical Data Frame.

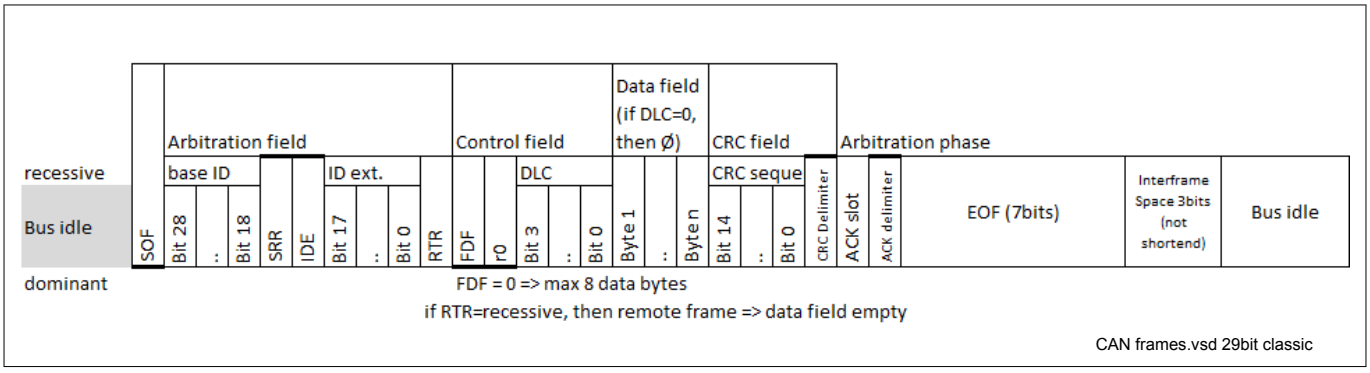


Figure 122 29 bit ID CAN Data Frame

19.1.2.2 Remote Frames

Normally, data transmission is performed on an autonomous basis with the data source node (e.g. a sensor) sending out a Data Frame. It is also possible, however, for a destination node (or nodes) to request the data from the source. For this purpose, the destination node sends a Remote Frame with an identifier that matches the identifier of the required Data Frame. The appropriate data source node will then send a Data Frame as a response to this remote request.

There are 2 differences between a Remote Frame and a Data Frame.

- The RTR bit is in the recessive state in a Remote Frame.
- There is no Data Field in a Remote Frame.

If a Data Frame and a Remote Frame with the same identifier are transmitted at the same time, the Data Frame wins arbitration due to the dominant RTR bit following the identifier. In this way, the node that transmitted the Remote Frame receives the requested data immediately.

19.1.2.3 Error Frames

An Error Frame is generated by any node that detects a bus error. An Error Frame consists of two fields, an Error Flag field followed by an Error Delimiter field. The Error Delimiter Field consists of 8 recessive bits and allows the bus nodes to restart bus communications after an error. There are, however, two forms of Error Flag fields. The form of the Error Flag field depends on the error status of the node that detects the error.

When an error-active node detects a bus error, the node generates an Error Frame with an active-error flag. The error-active flag is composed of six consecutive dominant bits that actively violate the bit-stuffing rule. All other stations recognize a bit-stuffing error and generate Error Frames themselves. The resulting Error Flag field on the CAN bus therefore consists of six to twelve consecutive dominant bits (generated by one or more nodes). The Error Delimiter field completes the Error Frame. After completion of the Error Frame, bus activity returns to normal and the interrupted node attempts to re-send the aborted message.

If an error-passive node detects a bus error, the node transmits an error-passive flag followed, again, by the Error Delimiter field. The error-passive flag consists of six consecutive recessive bits, and therefore the Error Frame (for an error-passive node) consists of 14 recessive bits (i.e. no dominant bits). Therefore, the transmission of an Error Frame by an error-passive node will not affect any other node on the network, unless the bus error is detected by the node that is actually transmitting (i.e. the bus master). If the bus master node generates an error-passive flag, this may cause other nodes to generate Error Frames due to the resulting bit-stuffing violation. After transmission of an Error Frame an error-passive node must wait for 6 consecutive recessive bits on the bus before attempting to rejoin bus communications.

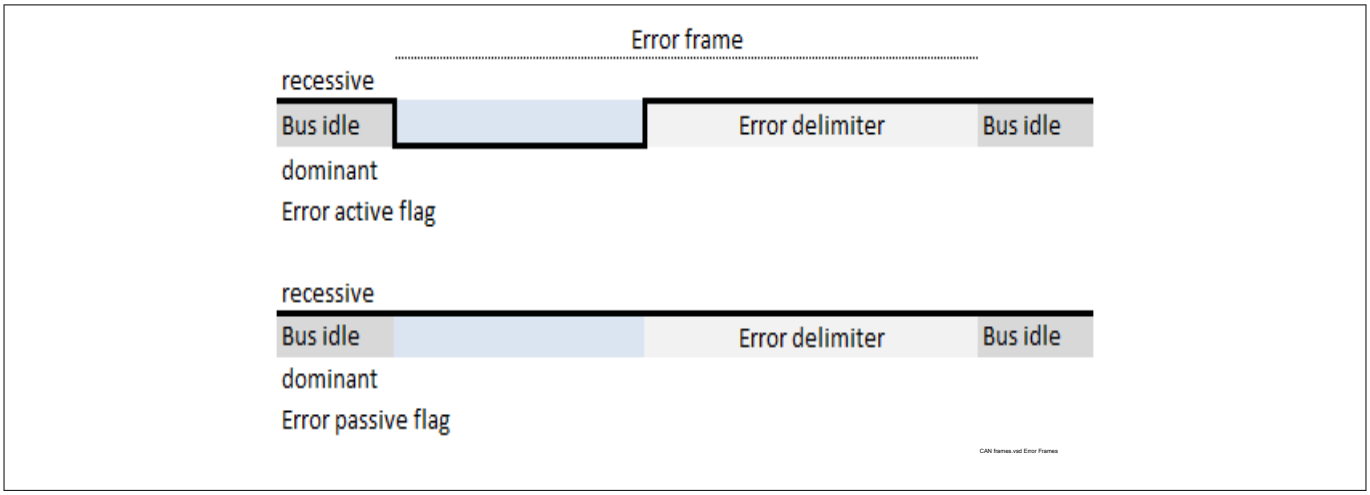


Figure 123 CAN Error Frames

19.1.3 The Nominal Bit Time

One bit cell (this means one high or low pulse of the NRZ code) is composed by four segments. Each segment is an integer multiple of Time Quanta t_Q. The Time Quanta is the smallest discrete timing resolution used by a CAN node. The nominal bit time definition with its segments is shown in ***Figure 124***.

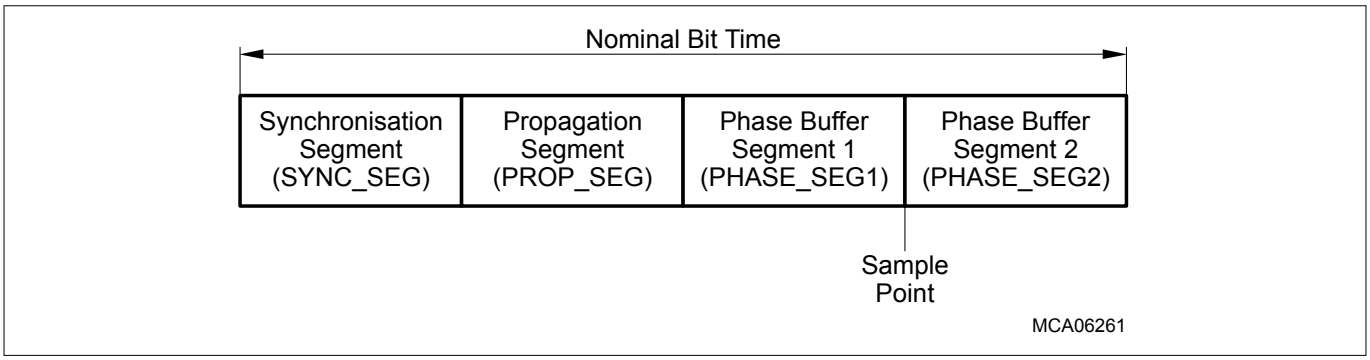


Figure 124 Partition of Nominal Bit Time

The Synchronization Segment (SYNC_SEG) is used to synchronize the various bus nodes. If there is a bit state change between the previous bit and the current bit, then the bus state change is expected to occur within this segment. The length of this segment is always 1 t_Q.

The Propagation Segment (PROP_SEG) is used to compensate for signal delays across the network. These delays are caused by signal propagation delay on the bus line and through the electronic interface circuits of the bus nodes.

The Phase Segments 1 and 2 (PHASE_SEG1, PHASE_SEG2) are used to compensate for edge phase errors. These segments can be lengthened or shortened by re-synchronization. PHASE_SEG2 is reserved for calculation of the subsequent bit level, and is ≥ 2 t_Q. At the sample point, the bus level is read and interpreted as the value of the bit cell. It occurs at the end of PHASE_SEG1.

The total number of t_Q in a bit time is between 8 and 25.

As a result of re-synchronization, PHASE_SEG1 can be lengthened or PHASE_SEG2 can be shortened. The amount of lengthening or shortening the phase buffer segments has an upper limit given by the re-synchronization jump width. The re-synchronization jump width may be between 1 and 4 t_Q, but it may not be longer than PHASE_SEG1.

19.1.4 Error Detection and Error Handling

The CAN protocol has sophisticated error detection mechanisms. The following errors can be detected:

Cyclic Redundancy Check (CRC) Error

With the CRC, the transmitter calculates special check bits for the bit sequence from the start of a frame until the end of the Data Field. This CRC sequence is transmitted in the CRC Field. The receiving node also calculates the CRC sequence using the same formula, and performs a comparison to the received sequence. If a mismatch is detected, a CRC error has occurred and an Error Frame is generated. The message is repeated.

Acknowledge Error

In the Acknowledge Field of a message, the transmitter checks whether a dominant bit is read during the Acknowledge Slot (that is sent out as a recessive bit). If not, no other node has received the frame correctly, an Acknowledge Error has occurred, and the message must be repeated. No Error Frame is generated.

Form Error

If a transmitter detects a dominant bit in one of the four segments End of Frame, Interframe Space, Acknowledge Delimiter, or CRC Delimiter, a Form Error has occurred, and an Error Frame is generated. The message is repeated

Bit Error

A Bit Error occurs if a) a transmitter sends a dominant bit and detects a recessive bit or b) if the transmitter sends a recessive bit and detects a dominant bit when monitoring the actual bus level and comparing it to

the just transmitted bit. In case b), no error occurs during the Arbitration Field (ID, RTR, IDE) and the Acknowledge Slot.

Stuff Error

If between Start of Frame and CRC Delimiter, six consecutive bits with the same polarity are detected, the bit-stuffing rule has been violated. A stuff error occurs and an Error Frame is generated. The message is repeated.

Detected errors are made public to all other nodes via Error Frames (except Acknowledge Errors). The transmission of the erroneous message is aborted and the frame is repeated as soon as possible. Furthermore, each CAN node is in one of the three error states (error-active, error-passive or bus-off) according to the value of the internal error counters. The error-active state is the usual state where the bus node can transmit messages and active-error frames (made of dominant bits) without any restrictions. In the error-passive state, messages and passive-error frames (made of recessive bits) may be transmitted. The bus-off state makes it temporarily impossible for the node to participate in the bus communication. During this state, messages can be neither received nor transmitted.

Basic CAN, Full CAN

There is one more CAN characteristic that is related to the interface of a CAN module (controller) and the host CPU: Basic-CAN and Full-CAN functionality.

In Basic-CAN devices, only basic functions of the protocol are implemented in hardware, such as the generation and the check of the bit stream. The decision, whether a received message has to be stored or not (acceptance filtering), and the complete message management must be done by software.

Full-CAN devices (this is the case for the MulticanCAN+ controller as implemented in IMC300A) manage the whole bus protocol in hardware, including the acceptance filtering and message management. Full-CAN devices contain message objects that handle autonomously the identifier, the data, the direction (receive or transmit) and the information of CAN operation. During the initialization of the device, the host CPU determines which messages are to be sent and which are to be received. The host CPU is informed by interrupt if the identifier of a received message matches with one of the programmed (receive-) message objects. The CPU load of Full-CAN devices is greatly reduced. When using Full-CAN devices, high baud rates and high bus loads with many messages can be handled.

Normally, the CAN device also provides only one transmit buffer and one or two receive buffers. Therefore, the host CPU load is quite high when using Basic-CAN modules. The main advantage of Basic-CAN is a reduced chip size leading to low costs of these devices.

19.2 Overview

The MulticanCAN+ module provides a communication interface which is fully compliant with CAN specification V2.0B (active), providing communications at up to 1 Mbit/s in Classical CAN (ISO 11898-1:2003(E) mode).

The MulticanCAN+ module for the IMC300A consists of 1 module (i.e MultiCAN with 2 CAN nodes), representing 2 serial communication interfaces. Each CAN node communicates over two pins (TXD and RXD). The device ports which are used for TXD and RXD may be individually configured within the PORTS block. Several port configuration options are available to provide application-specific flexibility.

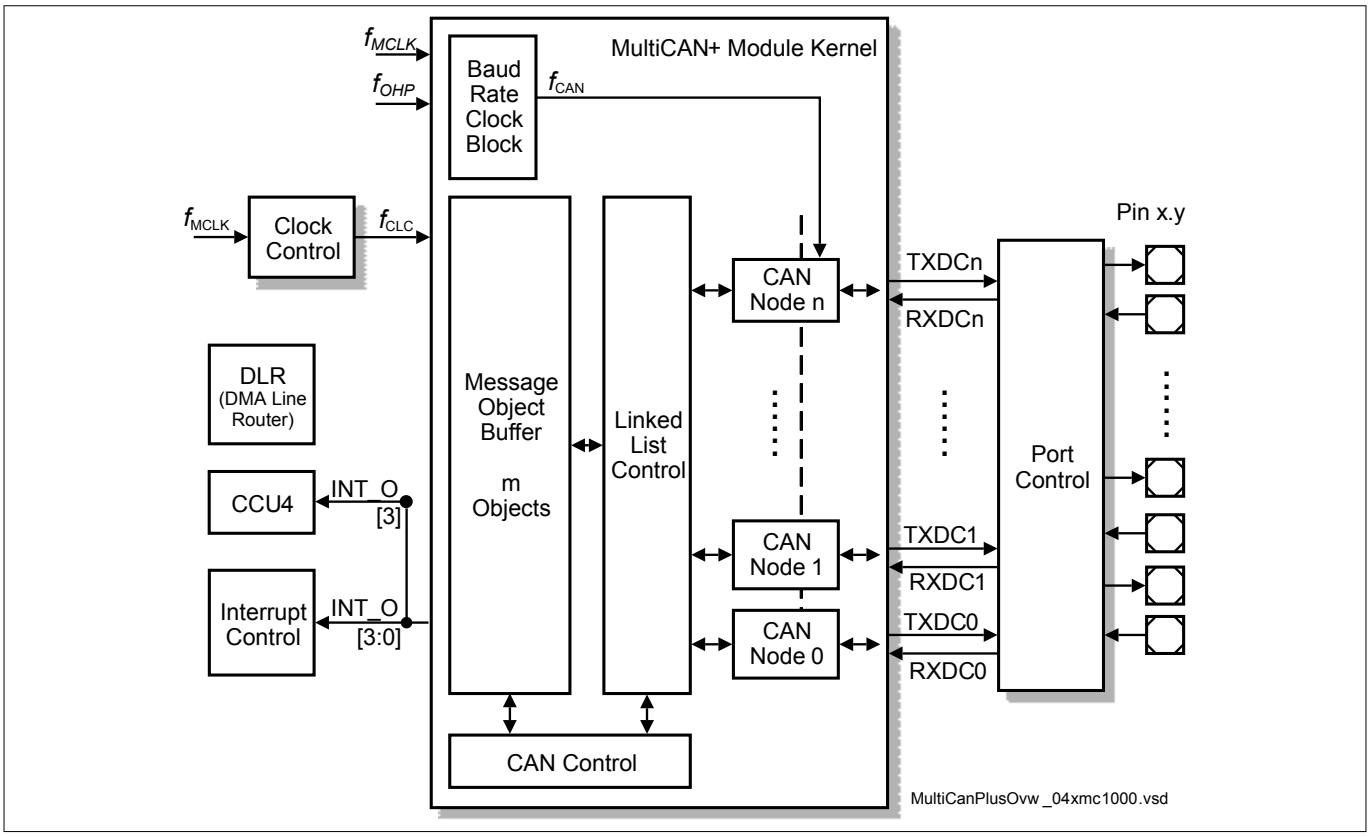


Figure 125 Overview of the MulticanCAN+ Module. The module has 2 nodes and 32 objects.

The MulticanCAN+ module contains 2 independently operating CAN nodes with Full-CAN functionality that are able to exchange Data and Remote Frames via a gateway function. Each CAN node can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

All CAN nodes share a common set of 32 message objects. Each message object can be individually allocated to one of the CAN nodes.Besides serving as a storage container for incoming and outgoing frames, message objects can be combined to build gateways between the CAN nodes or to setup a FIFO buffer.

The message objects are organized in double-chained linked lists, where each CAN node has its own list of message objects. A CAN node stores frames only into message objects that are allocated to the message object list of the CAN node, and it transmits only messages belonging to this message object list. A powerful, command-driven list controller performs all message object list operations.

The bit timings for the CAN nodes are derived from the module timer clock (f_{CAN}) and are programmable up to a data rate of 1 Mbit/s. External bus transceivers are connected to a CAN node via a pair of receive and transmit pins.

19.2.1 Features List

The MultiCAN+ module provides the following features:

- Compliant with ISO 11898 and SAE J 1939
- CAN functionality according to CAN specification V2.0 B active
- Dedicated control registers for each CAN node
- Data transfer rates up to 1 Mbit/s
- Support for asynchronous clock sources for baud rate generation by providing separate frequency domain and input:
  - System frequency clock f_{CLC}

  - Low-jitter E-Ray PLL clock
  - Direct oscillator clock (e.g. from ceramic resonator)
- Frequency jitter calibration based on external CAN messages during runtime
- Flexible and powerful message transfer control and error handling capabilities
- Advanced CAN bus bit timing analysis and baud rate detection for each CAN node via a frame counter
- Full-CAN functionality: A set of 32 message objects can be individually
  - Allocated (assigned) to any CAN node
  - Configured as transmit or receive object
  - Setup to handle frames with 11-bit or 29-bit identifier
  - Identified by a timestamp via a frame counter
  - Configured to remote monitoring mode
- Advanced Acceptance Filtering
  - Each message object provides an individual acceptance mask to filter incoming frames
  - A message object can be configured to accept standard or extended frames or to accept both standard and extended frames
  - Message objects can be grouped into different priority classes for transmission and reception
  - The selection of the message to be transmitted first can be based on frame identifier, IDE bit and RTR bit according to CAN arbitration rules, or on its order in the list
- Advanced CAN node features
  - Analyzer Mode supports monitoring of bus traffic without actively participating on the bus
  - Internal Loop-Back Mode is available for test purposes
  - Data transmission from a node can be stopped without affecting reception
  - Programmable minimum delay between two consecutive messages
- Advanced message object functionality
  - Message objects can be combined to build FIFO message buffers of arbitrary size, limited only by the total number of message objects
  - Message objects can be linked to form a gateway that automatically transfers frames between 2 different CAN buses. A single gateway can link any two CAN nodes. An arbitrary number of gateways can be defined
- Advanced data management
  - The message objects are organized in double-chained lists
  - List reorganizations can be performed at any time, even during full operation of the CAN nodes
  - A powerful, command-driven list controller manages the organization of the list structure and ensures consistency of the list
  - Message FIFOs are based on the list structure and can easily be scaled in size during CAN operation
- Advanced interrupt handling
  - Message interrupts, node interrupts can be generated
  - Interrupt requests can be routed individually to one of the 8 interrupt output lines
  - Message post-processing notifications can be combined flexibly into a dedicated register field of 256 notification bits

19.3 MulticanCAN+ Kernel Functional Description

This section describes the functionality of the MulticanCAN+ module.

19.3.1 Module Structure

Figure 126 shows the general structure of the MulticanCAN+ module.

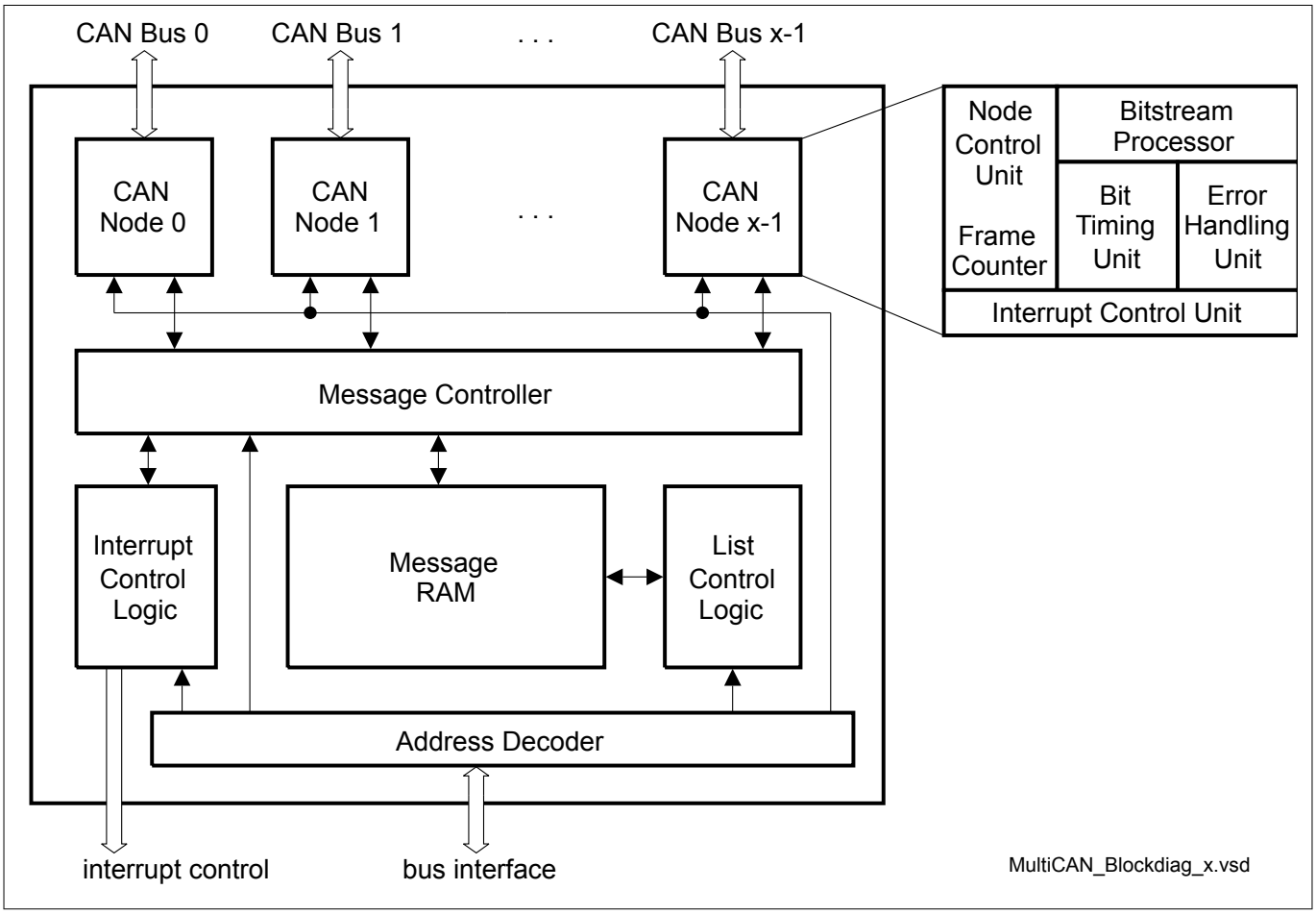


Figure 126 MulticanCAN+ Block Diagram

CAN Nodes

Each CAN node consists of several sub-units.

Bitstream Processor

The Bitstream Processor performs data, remote, error and overload frame processing according to the ISO 11898 standard. This includes conversion between the serial data stream and the input/output registers.

Bit Timing Unit

The Bit Timing Unit determines the length of a bit time and the location of the sample point according to the user settings, taking into account propagation delays and phase shift errors. The Bit Timing Unit also performs resynchronization.

Error Handling Unit

The Error Handling Unit manages the receive and transmit error counter. Depending on the contents of both counters, the CAN node is set into an error-active, error passive or bus-off state.

Node Control Unit

The Node Control Unit coordinates the operation of the CAN node:

- Enable/disable CAN transfer of the node

- Enable/disable and generate node-specific events that lead to an interrupt request (CAN bus errors, successful frame transfers etc.)
- Administration of the frame counter

Interrupt Control Unit

The Interrupt Control Unit in the CAN node controls the interrupt generation for the different conditions that can occur in the CAN node.

Message Controller

The Message Controller handles the exchange of CAN frames between the CAN nodes and the message objects that are stored in the Message RAM. The Message Controller performs several functions:

- Receive acceptance filtering to determine the correct message object for storing of a received CAN frame
- Transmit acceptance filtering to determine the message object to be transmitted first, individually for each CAN node
- Transfer contents between message objects and the CAN nodes, taking into account the status/control bits of the message objects
- Handling of the FIFO buffering and gateway functionality
- Aggregation of message-pending notification bits

List Controller

The List Controller performs all operations that lead to a modification of the double- chained message object lists. Only the list controller is allowed to modify the list structure. The allocation/deallocation or reallocation of a message object can be requested via a user command interface (command panel). The list controller state machine then performs the requested command autonomously.

Interrupt Control

The general interrupt structure is shown in ***Figure 127***. The interrupt event can trigger the interrupt generation. The interrupt pulse is generated independently of the interrupt flag in the interrupt status register. The interrupt flag can be reset by software by writing a 0 to it.

If enabled by the related interrupt enable bit in the interrupt enable register, an interrupt pulse can be generated at one of the 8 interrupt output lines INT_Om of the MulticanCAN+ module. If more than one interrupt source is connected to the same interrupt node pointer (in the interrupt node pointer register), the requests are combined to one common line.

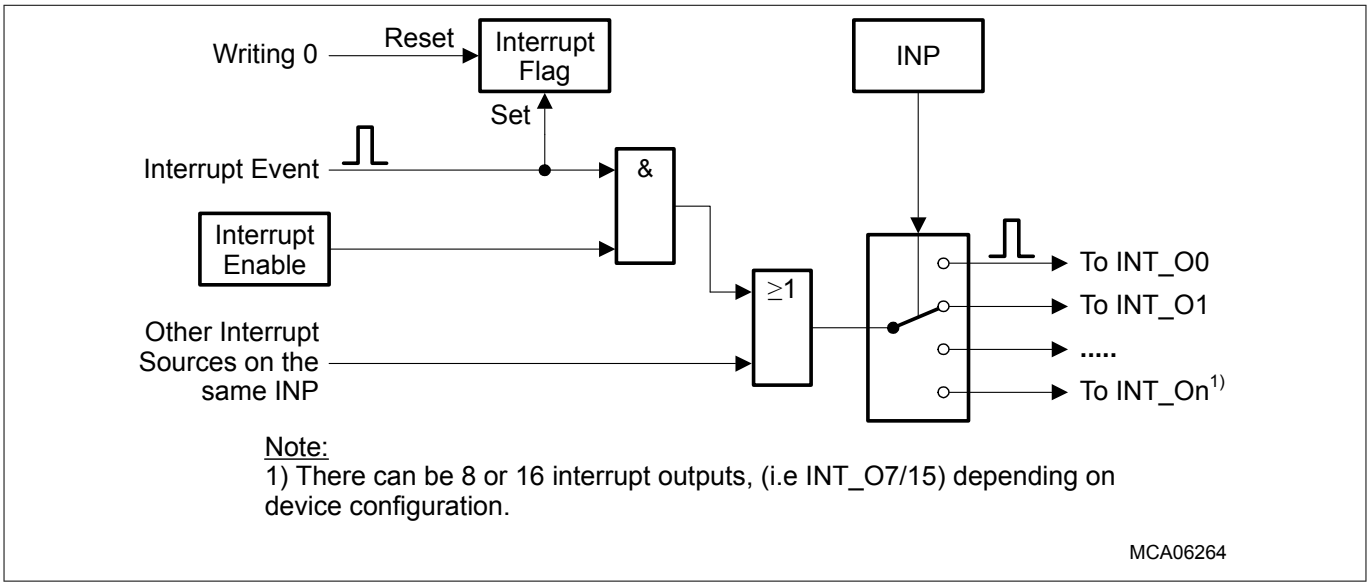


Figure 127 General Interrupt Structure

19.3.2 Clock Control

The CAN module timer clock f_{CAN} of the functional blocks of the MulticanCAN+ module is derived from the synchronous clock source. The Fractional Divider is used to generate f_{CAN} used for bit timing calculation, The frequency of f_{CAN} is identical for all CAN nodes. The register file operates with the module control clock f_{CLC}. See also ***Figure 128*** on page 531.

The output clock f_{CAN} of the Fractional Divider is based on the clock f_A, but only every nth clock pulse is taken.

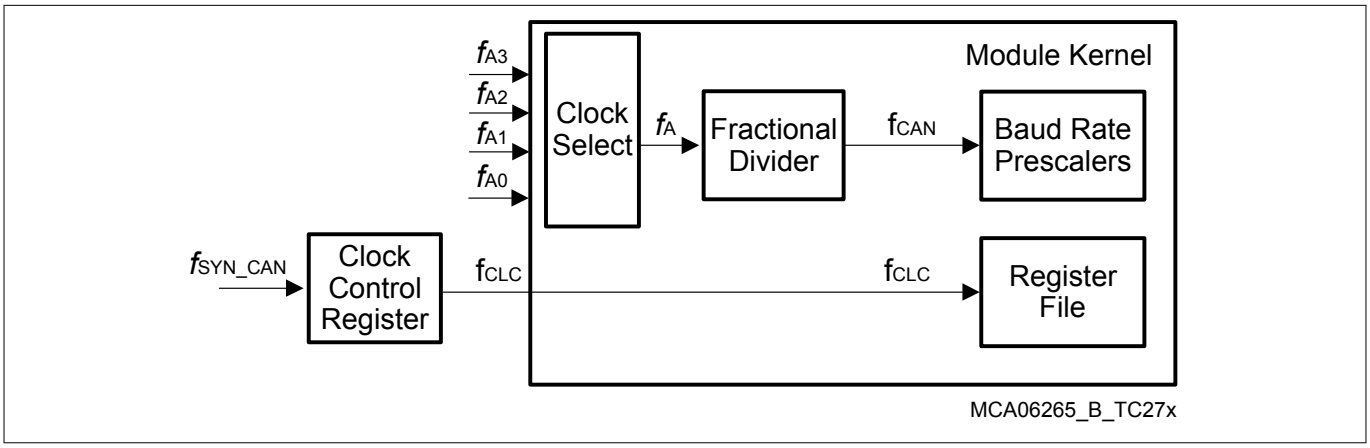


Figure 128 MulticanCAN+ Clock Generation

The f_{SYN_CAN} is identical to f_{MCLK}. f_{Ai} is the asynchronous clock input.

Table 227 indicates the minimum operating frequencies in MHz for f_{CLC} that are required for a baud rate of 1 Mbit/s for the active CAN nodes. If a lower baud rate is desired, the values can be scaled linearly (e.g. for a maximum of 500 kbit/s, 50% of the indicated value are required).

The values imply that the CPU executes maximum accesses to the MulticanCAN+ module. The values may contain rounding effects.

Table 227 Minimum Operating Frequencies[46] [MHz]

Number of allocated message objects MO[47],	Number of Active CAN Nodes				
	1	**2**	**3**	**4**	**5**
16 MO	12	19	26	33	40
32 MO	15	23	30	37	44
64 MO	21	28	37	46	53
128 MO	40	45	50	55	61
256 MO	72	77	82	88	93

The baud rate generation of the MulticanCAN+ being based on f_A, this frequency has to be chosen carefully to allow correct CAN bit timing. The required value of f_A is given by an integer multiple (n) of the CAN baud rate multiplied by the number of time quanta per CAN bit time. For example, to reach 1 Mbit/s with 20 tq per bit time, possible values of f_A are given by formula [n × 20] MHz, with n being an integer value, starting at 1.

It is not advised to use fractional divider mode.

Additionally, for correct operation of the MultiCAN, the following conditions have to be fulfilled,

46 In the case of 15 time quanta, the minimum operating frequency required is 15 MHz.

47 Only those message objects have to be taken into account that are allocated to a CAN node. The unallocated message objects have no influence on the minimum operating frequency.

$$\text{Baudrate}_{max} = [(8 \times T_{CAN}) + (8 \times T_{CLC}) + (4 \times \text{No. of active CAN nodes} \times T_{CLC})]$$
also
NBTR.SJW < NBTR.TSEG1

Equation 24

As an example, when f_{CLC} = 10 MHz, f_{CAN} = 20 MHz, No of active CAN nodes = 2,
Baudrate_{max}=[(8 x 50 ns) + (8 x 100 ns) + (4 x 2 x 100 ns)] = 2000 ns = 500 kBaud
Table 228 below illustrates the minimum CAN module timer clock f_{CAN} and Module Control Clock f_{CLC} that's required to support a baudrate generation of 500 kBaud. If a higher baudrate is desired, the values need to be calculated as per ***Equation 24***.

Table 228 Minimum Operating Frequencies [MHz] required for 500kBaud

No. of active CAN nodes	$f_{CAN} = f_{CLC}$ (MHz)	$f_{CAN} \neq f_{CLC}$ (MHz)	
		f_{CAN}	f_{CLC}
1	10	16	8
		20	8
		24	8
		80	7
2	12	16	11
		20	10
		24	10
		80	9
3	14	16	14
		20	13
		24	12
		80	11

19.3.3 Port Input Control

It is possible to select the input lines for the RXDCx inputs for the CAN nodes. The selected input is connected to the CAN node and is also available to wake-up the system. More details are defined in ***Chapter 19.6.4.2*** on page 605.

19.3.4 CAN Node Control

Each CAN node may be configured and run independently of the other CAN node. Each CAN node is equipped with its own node control logic to configure the global behavior and to provide status information.

Note: In the following descriptions, index “x” stands for the node number and index “n” represents the message object number.

Configuration Mode is activated when bit NCRx.CCE is set to 1. This mode allows CAN bit timing parameters and the error counter registers to be modified.

CAN Analyzer Mode

CAN Analyzer Mode is activated when bit NCRx.CALM is set to 1. In this operation mode, Data And Remote Frames are monitored without active participation in any CAN transfer (CAN transmit pin is held on recessive level). Incoming Remote Frames are stored in a corresponding transmit message object, while arriving data frames are saved in a matching receive message object.

In CAN Analyzer Mode, the entire configuration information of the valid (including ACK) received frame is stored in the corresponding message object, and can be evaluated by the CPU to determine their identifier, IDE bit information and data length code (ID and DLC optionally if the Remote Monitoring Mode is active, bit MOFCRn.RMM = 1). Incoming frames are not acknowledged, and no Error Frames are generated. If CAN Analyzer Mode is enabled, Remote Frames are not responded to by the corresponding Data Frame, and Data Frames cannot be transmitted by setting the transmit request bit MOSTATn.TXRQ. Receive interrupts are generated in CAN Analyzer Mode (if enabled) for all error free received frames.

The node-specific interrupt configuration is also defined by the Node Control Logic via the NCRx register bits TRIE, ALIE and LECIE:

- If control bit TRIE is set to 1, a transfer interrupt is generated when the NSRx register has been updated (after each successfully completed message transfer).
- If control bit ALIE is set to 1, an alert interrupt is generated when a “bus-off” condition has been recognized or the Error Warning Level has been exceeded or under-run. Additionally, list or object errors lead to this type of interrupt.
- If control bit LECIE is set to 1, a last error code interrupt is generated when an error code > 0 is written into bit field NSRx.LEC by hardware.

Setting bit TXDIS in register NCRx stops the transmit activity of this node without affecting reception; bit CANDIS disables the node completely.

The Node x Status Register NSRx provides an overview about the current state of the respective CAN node x, comprising information about CAN transfers, CAN node status, and error conditions.

The CAN frame counter can be used to check the transfer sequence of message objects or to obtain information about the instant a frame has been transmitted or received from the associated CAN bus. CAN frame counting is performed by a 16-bit counter, controlled by register NFCRx. Bit fields NFCRx.CFMOD and NFCRx.CFSEL determine the operation mode and the trigger event incrementing the frame counter.

19.3.4.1 Bit Timing Unit

According to the ISO 11898 standard, a CAN bit time is subdivided into different segments (***Figure 129***). Each segment consists of multiples of a time quantum t_q. The magnitude of t_q is adjusted by Node x Bit Timing Register bit fields NBTRx.BRP and NBTRx.DIV8, both controlling the baud rate prescaler (register NBTRx is described on page ***581***). The baud rate prescaler is driven by the module timer clock f_{CAN} (generation and control of f_{CAN} is described on page ***602***).

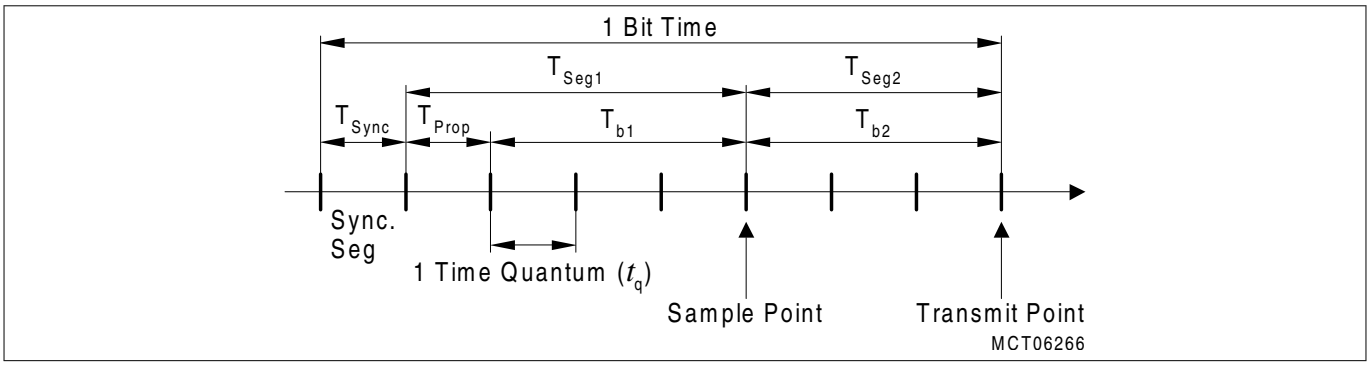


Figure 129 CAN Bus Bit Timing Standard

The Synchronization Segment (T_{Sync}) allows phase synchronization between transmitter and receiver time base. The Synchronization Segment length is always one t_q. The Propagation Time Segment (T_{Prop}) takes into

account the physical propagation delay in the transmitter output driver on the CAN bus line and in the transceiver circuit. For a working collision detection mechanism, T_{Prop} must be two times the sum of all propagation delay quantities rounded up to a multiple of t_q. The phase buffer segments 1 and 2 (T_{b1}, T_{b2}) before and after the signal sample point are used to compensate for a mismatch between transmitter and receiver clock phases detected in the synchronization segment.

The maximum number of time quanta allowed for re-synchronization is defined by bit field NBTRx.SJW. The Propagation Time Segment and the Phase Buffer Segment 1 are combined to parameter T_{Seg1}, which is defined by the value NBTRx.TSEG1. A minimum of 3 time quanta is demanded by the ISO standard. Parameter T_{Seg2}, which is defined by the value of NBTRx.TSEG2, covers the Phase Buffer Segment 2. A minimum of 2 time quanta is demanded by the ISO standard. According to ISO standard, a CAN bit time, calculated as the sum of T_{Sync}, T_{Seg1} and T_{Seg2}, must not fall below 8 time quanta.

Calculation of the bit time:

t_q	$= (BRP + 1) / f_{CAN}$	if DIV8 = 0
	$= 8 \times (BRP + 1) / f_{CAN}$	if DIV8 = 1
T_{Sync}	$= 1 \times t_q$	
T_{Seg1}	$= (TSEG1 + 1) \times t_q$	(min. 3 t_q)
T_{Seg2}	$= (TSEG2 + 1) \times t_q$	(min. 2 t_q)
bit time	$= T_{Sync} + T_{Seg1} + T_{Seg2}$	(min. 8 t_q)

To compensate phase shifts between clocks of different CAN controllers, the CAN controller must synchronize on any edge from the recessive to the dominant bus level. The hard synchronization is enabled (at the start of frame), the bit time is restarted at the synchronization segment. Otherwise, the re-synchronization jump width T_{SJW} defines the maximum number of time quanta, a bit time may be shortened or lengthened by one re-synchronization. The value of SJW is defined by bit field NBTRx.SJW.

T_{SJW}	$= (SJW + 1) \times t_q$
T_{Seg1}	$\geq T_{SJW} + T_{prop}$
T_{Seg2}	$\geq T_{SJW}$

The maximum relative tolerance for f_{CAN} depends on the Phase Buffer Segments, re-synchronization jump width and the bit time.

df_{CAN}	$\leq \min (T_{b1}, T_{b2}) / [2 \times (13 \times \text{bit time} - T_{b2})]$	AND
df_{CAN}	$\leq T_{SJW} / 20 \times \text{bit time}$	

A valid CAN bit timing must be written to the CAN Node Bit Timing Register NBTR before resetting the INIT bit in the Node Control Register, i.e. before enabling the operation of the CAN node.

The Node Bit Timing Register may be written only if bit CCE (Configuration Change Enable) is set in the corresponding Node Control Register.

19.3.4.2 Bitstream Processor

Based on the message objects in the message buffer, the Bitstream Processor generates the remote and Data Frames to be transmitted via the CAN bus. It controls the CRC generator and adds the checksum information to the new remote or Data Frame. After including the SOF bit and the EOF field, the Bitstream Processor starts the CAN bus arbitration procedure and continues with the frame transmission when the bus was found in idle state. While the data transmission is running, the Bitstream Processor continuously monitors the I/O line. If (outside the CAN bus arbitration phase or the acknowledge slot) a mismatch is detected between the voltage level on the I/O line and the logic state of the bit currently sent out by the transmit shift register, a CAN LEC error interrupt request is generated, and the error code is indicated by the Node x Status Register bit field NSRx.LEC.

The data consistency of an incoming frame is verified by checking the associated CRC field. When an error has been detected, a CAN LEC error interrupt request is generated and the associated error code is presented in the Node x Status Register NSRx. Furthermore, an Error Frame is generated and transmitted on the CAN bus. After decomposing a faultless frame into identifier and data portion, the received information is transferred to the message buffer executing remote and Data Frame handling, interrupt generation and status processing.

19.3.4.3 Error Handling Unit

The Error Handling Unit of a CAN node x is responsible for the fault confinement of the CAN device. Its two counters, the Receive Error Counter REC and the Transmit Error Counter TEC (bit fields of the Node x Error Counter Register NECNTx, see page ***582***) are incremented and decremented by commands from the Bitstream Processor. If the Bitstream Processor itself detects an error while a transmit operation is running, the Transmit Error Counter is incremented by 8. An increment of 1 is used when the error condition was reported by an external CAN node via an Error Frame generation. For error analysis, the transfer direction of the disturbed message and the node that recognizes the transfer error are indicated for the respective CAN node x in register NECNTx. Depending on the values of the error counters, the CAN node is set into error- active, error-passive, or bus-off state.

The CAN node is in error-active state if both error counters are below the error-passive limit of 128. The CAN node is in error-passive state, if at least one of the error counters is equal to or greater than 128.

The bus-off state is activated if the Transmit Error Counter is equal to or greater than the bus-off limit of 256. This state is reported for CAN node x by the Node x Status Register flag NSRx.BOFF. The device remains in this state, until the “bus-off” recovery sequence is finished. Additionally, Node x Status Register flag NSRx.EWRN is set when at least one of the error counters is equal to or greater than the error warning limit defined by the Node x Error Count Register bit field NECNTx.EWRNLVL. Bit NSRx.EWRN is reset if both error counters fall below the error warning limit again (see page ***575***).

19.3.4.4 CAN Frame Counter

Each CAN node is equipped with a frame counter that counts transmitted/received CAN frames or obtains information about the time when a frame has been started to transmit or be received by the CAN node. CAN frame counting/bit time counting is performed by a 16-bit counter that is controlled by Node x Frame Counter Register NFCRx (see page ***583***). Bit field NFCRx.CFSEL determines the operation mode of the frame counter:

Frame Count Mode

After the successful transmission and/or reception of a CAN frame, the frame counter is copied into the CFCVAL bit field of the MOIPRn register of the message object involved in the transfer. Afterwards, the frame counter is incremented.

Time Stamp Mode

The frame counter is incremented (internally) with the beginning of a new bit time. Its value is permanently sampled in the CFC field while the bus is idle. The value sampled just before the SOF bit of a new frame is detected is written to the corresponding message object. When the treatment of a message object is finished, the sampling continues.

Bit Timing Mode

Used for baud rate detection and analysis of the bit timing (***Chapter 19.3.6.3***).

Error Count Mode

The frame counter is incremented when an error frame is received or an error is detected by the node (001_B to 110_B) (see ***Table 234*** for ***Encoding of the LEC Bit field***). If the NFCRx.CFCIE interrupt bit is enabled, the NFCRx.CFCOV overflow flag will be set when the frame counter overflows. Configuration of CFSEL has no influence.

19.3.4.5 CAN Node Interrupts

Each CAN node has four hardware triggered interrupt request types that are able to generate an interrupt request upon:

- The successful transmission or reception of a frame
- A CAN protocol error with a last error code
- An alert condition: Transmit/receive error counters reach the warning limit, bus-off state changes, a List Length Error occurs, or a List Object Error occurs
- An overflow of the frame counter

Besides the hardware generated interrupts, software initiated interrupts can be generated using the Module Interrupt Trigger Register MITR. Writing a 1 to bit n of bit field MITR.IT generates an interrupt request signal on the corresponding interrupt output line INT_On. When writing MITR.IT more than one bit can be set resulting in activation of multiple INT_On interrupt output lines at the same time. See also ***Interrupt Control*** on page 606 for further processing of the CAN node interrupts.

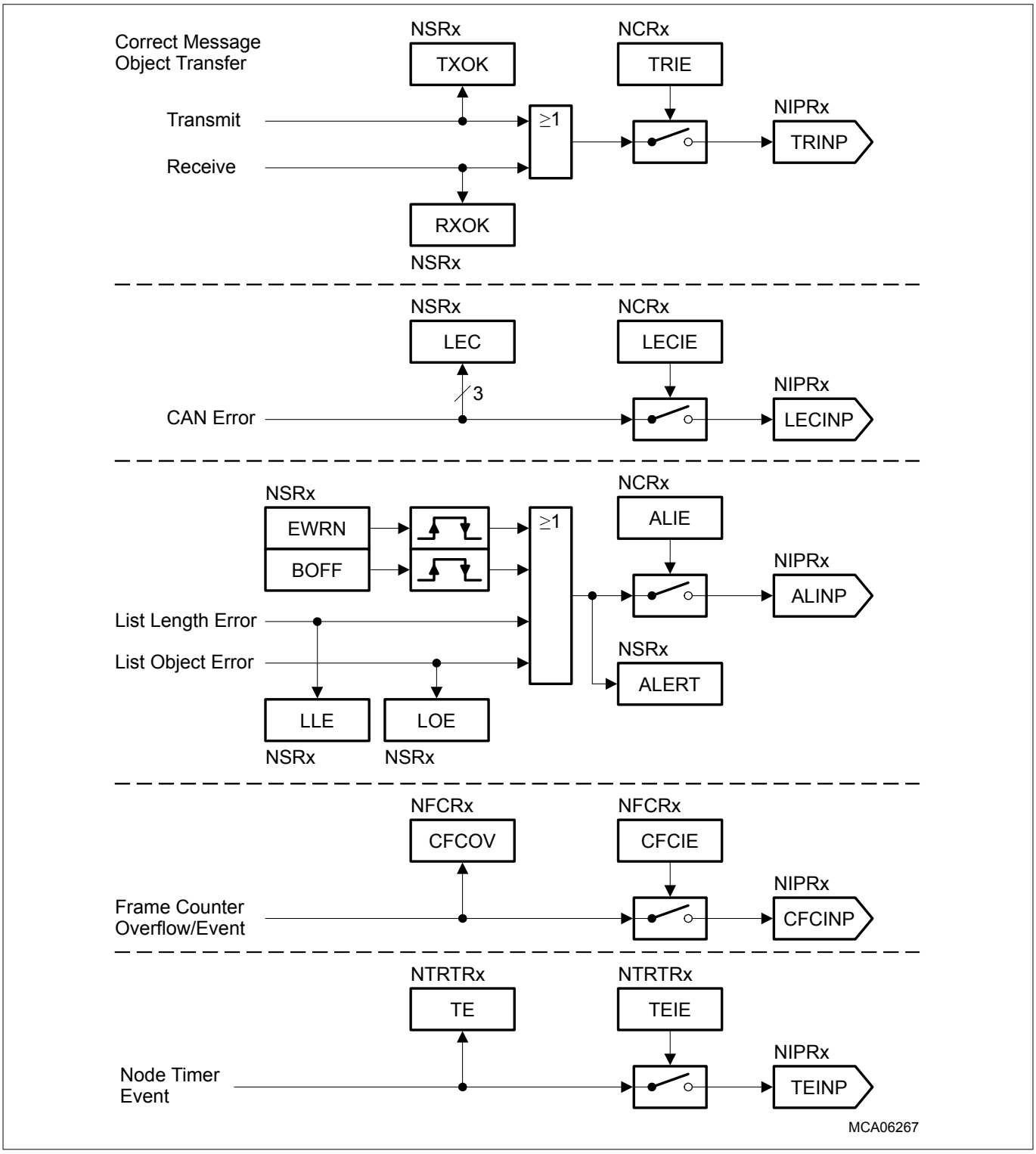


Figure 130 CAN Node Interrupts

19.3.5 Message Object List Structure

This section describes the structure of the message object lists in the MulticanCAN+ module.

19.3.5.1 Basics

The message objects of the MulticanCAN+ module are organized in double-chained lists, where each message object has a pointer to the previous message object in the list as well as a pointer to the next message object in the list. The MulticanCAN+ module provides 16 lists. Each message object is allocated to one of these lists. In the example in ***Figure 131***, the three message objects (3, 5, and 16) are allocated to the list with index 2 (List Register LIST2).

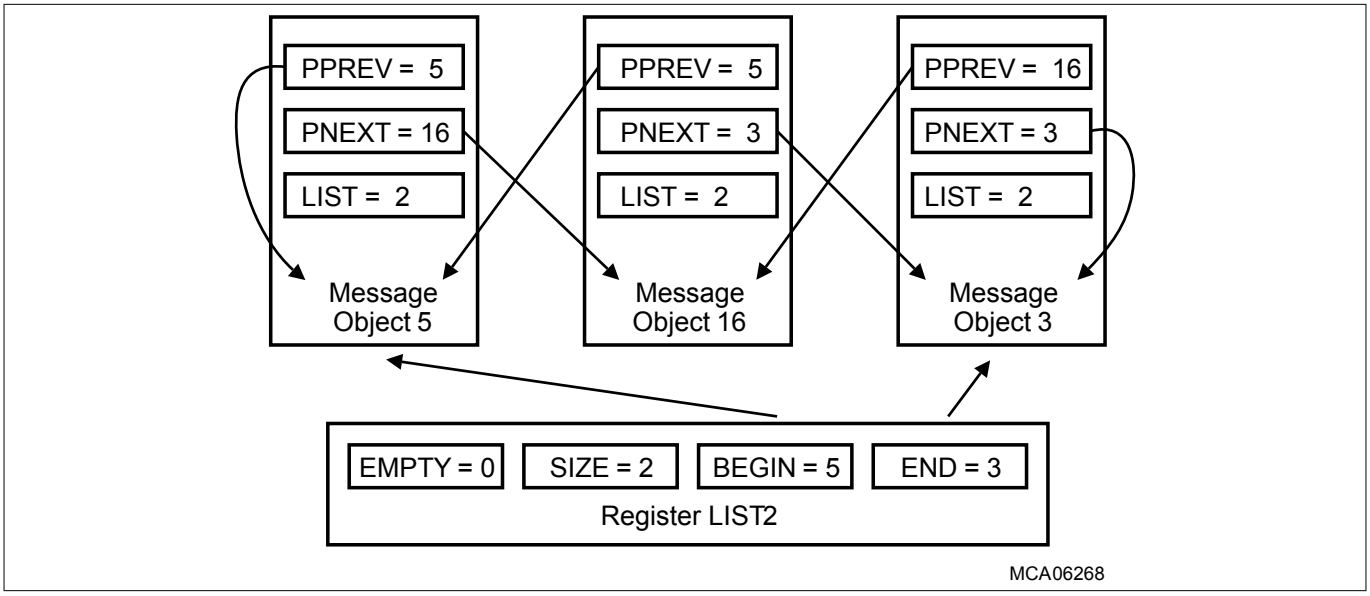


Figure 131 Example Allocation of Message Objects to a List

Bit field BEGIN in the List Register (for definition, see page ***572***) points to the first element in the list (object 5 in the example), and bit field END points to the last element in the list (object 3 in the example). The number of elements in the list is indicated by bit field SIZE of the List Register (SIZE = number of list elements - 1, thus SIZE = 2 for the 3 elements in the example). The EMPTY bit of the List Register indicates whether or not a list is empty (EMPTY = 0 in the example, because list 2 is not empty).

Each message object n has a pointer PNEXT in its Message Object n Status Register MOSTATn (see page ***589***) that points to the next message object in the list, and a pointer PPREV that points to the previous message object in the list. PPREV of the first message object points to the message object itself because the first message object has no predecessor (in the example message object 5 is the first message object in the list, indicated by PPREV = 5). PNEXT of the last message object also points to the message object itself because the last message object has no successor (in the example, object 3 is the last message object in the list, indicated by PNEXT = 3).

Bit field MOSTATn.LIST indicates the list index number to which the message object is currently allocated to. The message objects of the example are allocated to list 2. Therefore, all LIST bit fields for the message objects assigned to list 2 are set to LIST = 2.

19.3.5.2 List of Unallocated Elements

The list with list index 0 has a special meaning: it is the list of all unallocated elements. An element is called unallocated if it belongs to list 0 (MOSTATn.LIST = 0). It is called allocated if it belongs to a list with an index not equal to 0 (MOSTATn.LIST > 0).

After reset, all message objects are unallocated. This means that they are assigned to the list of unallocated elements with MOSTATn.LIST = 0. After this initial allocation of the message objects caused by reset, the list of all unallocated message objects is ordered by message number (predecessor of message object n is object n-1, successor of object n is object n+1).

19.3.5.3 Connection to the CAN Nodes

Each CAN node is linked to one unique list of message objects. A CAN node performs message transfer only with the message objects that are allocated to the list of the CAN node. This is illustrated in ***Figure 132***. Frames that are received on a CAN node may only be stored in one of the message objects that belongs to the CAN node; frames to be transmitted on a CAN node are selected only from the message objects that are allocated to that node, as indicated by the vertical arrows.

There are more lists (16) than CAN nodes (2). This means that some lists are not linked to one of the CAN nodes. A message object that is allocated to one of these unlinked lists cannot receive messages directly from a CAN node and it may not transmit messages.

FIFO and gateway mechanisms refer to message numbers and not directly to a specific list. The user must take care that the message objects targeted by FIFO/gateway belong to the desired list. The mechanisms make it possible to work with lists that do not belong to the CAN node.

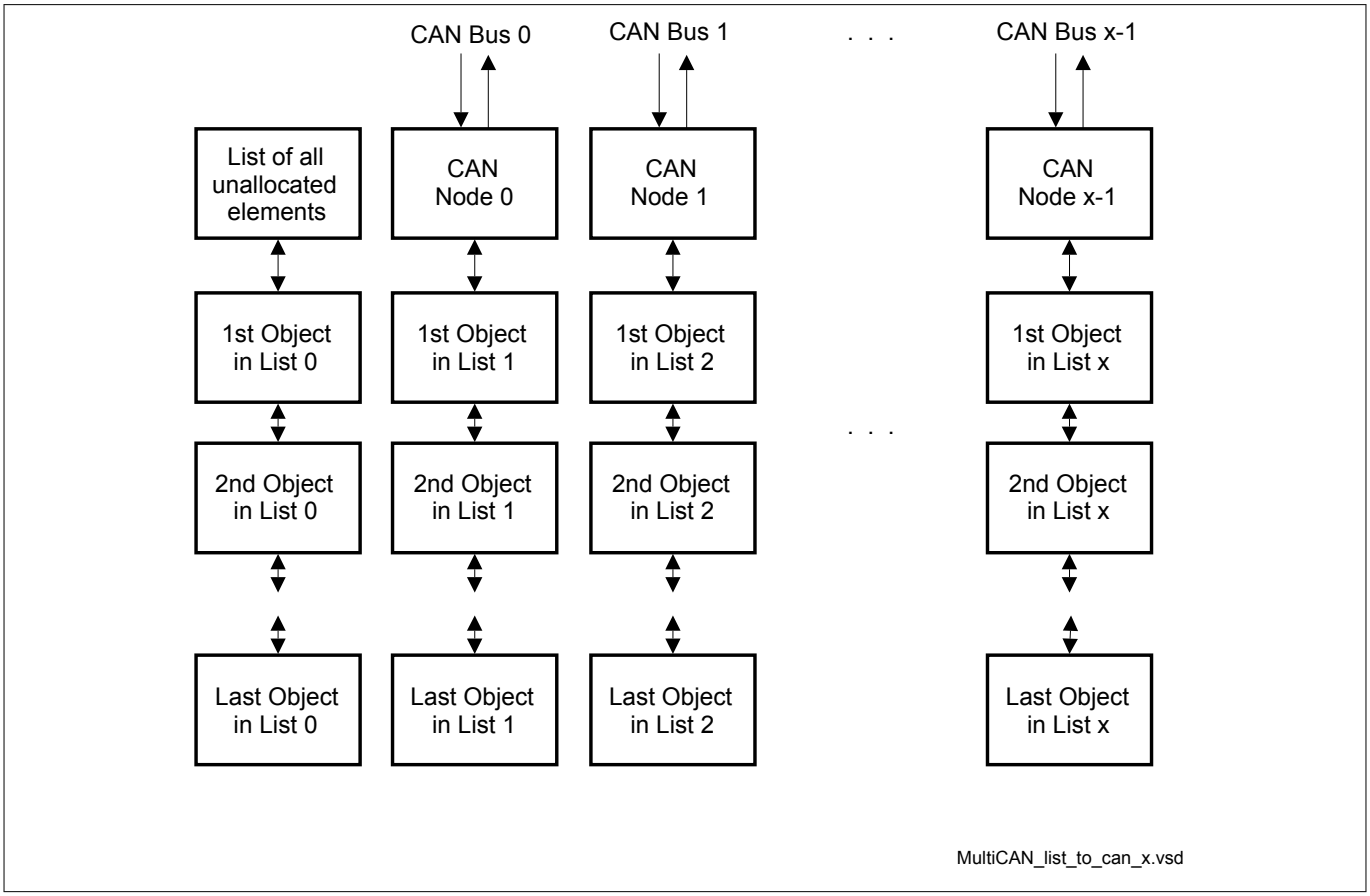


Figure 132 Message Objects Linked to CAN Nodes

19.3.5.4 List Command Panel

The list structure cannot be modified directly by write accesses to the LIST registers and the PPREV, PNEXT and LIST bit fields in the Message Object Status Registers, as they are read only. The list structure is managed by and limited to the list controller inside the MulticanCAN+ module. The list controller is controlled via a command panel allowing the user to issue list allocation commands to the list controller. The list controller has two main purposes:

1. Ensure that all operations that modify the list structure result in a consistent list structure.
2. Present maximum ease of use and flexibility to the user.

The list controller and the associated command panel allows the programmer to concentrate on the final properties of the list, which are characterized by the allocation of message objects to a CAN node, and the ordering relation between objects that are allocated to the same list. The process of list (re-)building is done in the list controller.

Table 229 gives an overview on the available panel commands while ***Table 233*** on page ***568*** describes the panel commands in more detail.

Table 229 Panel Commands Overview

Command Name	Description
No Operation	No new command is started.
Initialize Lists	Run the initialization sequence to reset the CTRL and LIST field of all message objects.
Static Allocate	Allocate message object to a list.
Dynamic Allocate	Allocate the first message object of the list of unallocated objects to the selected list.
Static Insert Before	Remove a message object (source object) from the list that it currently belongs to, and insert it before a given destination object into the list structure of the destination object.
Dynamic Insert Before	Insert a new message object before a given destination object.
Static Insert Behind	Remove a message object (source object) from the list that it currently belongs to, and insert it behind a given destination object into the list structure of the destination object.
Dynamic Insert Behind	Insert a new message object behind a given destination object.

A panel command is started by writing the respective command code into the Panel Control Register bit field PANCTR.PANCMD (see page ***567***). The corresponding command arguments must be written into bit fields PANCTR.PANAR1 and PANCTR.PANAR2 before writing the command code, or latest along with the command code in a single 32-bit write access to the Panel Control Register.

With the write operation of a valid command code, the PANCTR.BUSY flag is set and further write accesses to the Panel Control Register are ignored. The BUSY flag remains active and the control panel remains locked until the execution of the requested command has been completed. After a reset and resetting the CLC.DISR (see page ***603***) register, the list controller builds up list 0. Afterwards the BUSY bit is set, dependent on core speed this might be visible. During list controller initialization, BUSY is set and other accesses to the CAN RAM are forbidden. The CAN RAM can be accessed again when BUSY becomes inactive.

Note: The CAN RAM is automatically initialized after enabling the clocks of the module, by the list controller in order to ensure correct list pointers in each message object. The operation is indicated by automatically setting the BUSY bit. The end of this CAN RAM initialization is indicated by bit PANCTR.BUSY becoming inactive. It is advised to initialize some registers within the CAN controller before polling the PANCTR.BUSY the first time.

In case of a dynamic allocation command that takes an element from the list of unallocated objects, the PANCTR.RBUSY bit is also set along with the BUSY bit (RBUSY = BUSY = 1). This indicates that bit fields PANAR1 and PANAR2 are going to be updated by the list controller in the following way:

1. The message number of the message object taken from the list of unallocated elements is written to PANAR1.
2. If ERR (bit 7 of PANAR2) is set to 1, the list of unallocated elements was empty and the command is aborted. If ERR is 0, the list was not empty and the command will be performed successfully.

The results of a dynamic allocation command are written before the list controller starts the actual allocation process. As soon as the results are available, RBUSY becomes inactive (RBUSY = 0) again, while BUSY still remains active until completion of the command. This allows the user to set up the new message object while it is still in the process of list allocation. The access to message objects is not limited during ongoing list operations. However, any access to a register resource located inside the RAM delays the ongoing allocation process by one access cycle.

As soon as the command is finished, the BUSY flag becomes inactive (BUSY = 0) and write accesses to the Panel Control Register are enabled again. Also, the “No Operation” command code is automatically written to the PANCTR.PANCMD field. A new command may be started any time when BUSY = 0.

All fields of the Panel Control Register PANCTR except BUSY and RBUSY may be written by the user. This makes it possible to save and restore the Panel Control Register if the Command Panel is used within independent (mutually interruptible) interrupt service routines. If this is the case, any task that uses the Command Panel and that may interrupt another task that also uses the Command Panel should poll the BUSY flag until it becomes inactive and save the whole PANCTR register to a memory location before issuing a command. At the end of the interrupt service routine, the task should restore PANCTR from the memory location.

Before a message object that is allocated to the list of an active CAN node shall be moved to another list or to another position within the same list, bit MOSTATn.MSGVAL (“Message Valid”) of message object n must be cleared.

19.3.6 CAN Node Analyzer Mode

The chapter describes the CAN node analyzer capabilities of the MulticanCAN+ module.

19.3.6.1 Analyzer Mode

The CAN Analyzer Mode makes it possible to monitor the CAN traffic for each CAN node individually without affecting the logical state of the CAN bus. The CAN Analyzer Mode for CAN node x is selected by setting Node x Control Register bit NCRx.CALM.

In CAN Analyzer Mode, the transmit pin of a CAN node is held at a recessive level permanently. The CAN node may receive frames (Data, Remote, and Error Frames) but is not allowed to transmit. Received Data/Remote Frames are not acknowledged (i.e. acknowledge slot is sent recessive) but will be received and stored in matching message objects as long as there is any other node that acknowledges the frame. The complete message object functionality is available, but no transmit request will be executed.

19.3.6.2 Loop-Back Mode

The MulticanCAN+ module provides a Loop-Back Mode to enable an in-system test of the MulticanCAN+ module as well as the development of CAN driver software without access to an external CAN bus.

The loop-back feature consists of an internal CAN bus (inside the MulticanCAN+ module) and a bus select switch for each CAN node (see ***Figure 133***). With the switch, each CAN node can be connected either to the internal CAN bus (Loop-Back Mode activated) or the external CAN bus, respectively to transmit and receive pins (normal operation). The CAN bus that is not currently selected is driven recessive; this means the transmit pin is held at 1, and the receive pin is ignored by the CAN nodes that are in Loop-Back Mode.

The Loop-Back Mode is selected for CAN node x by setting the Node x Port Control Register bit NPCRx.LBM. All CAN nodes that are in Loop-Back Mode may communicate together via the internal CAN bus without affecting the normal operation of the other CAN nodes that are not in Loop-Back Mode.

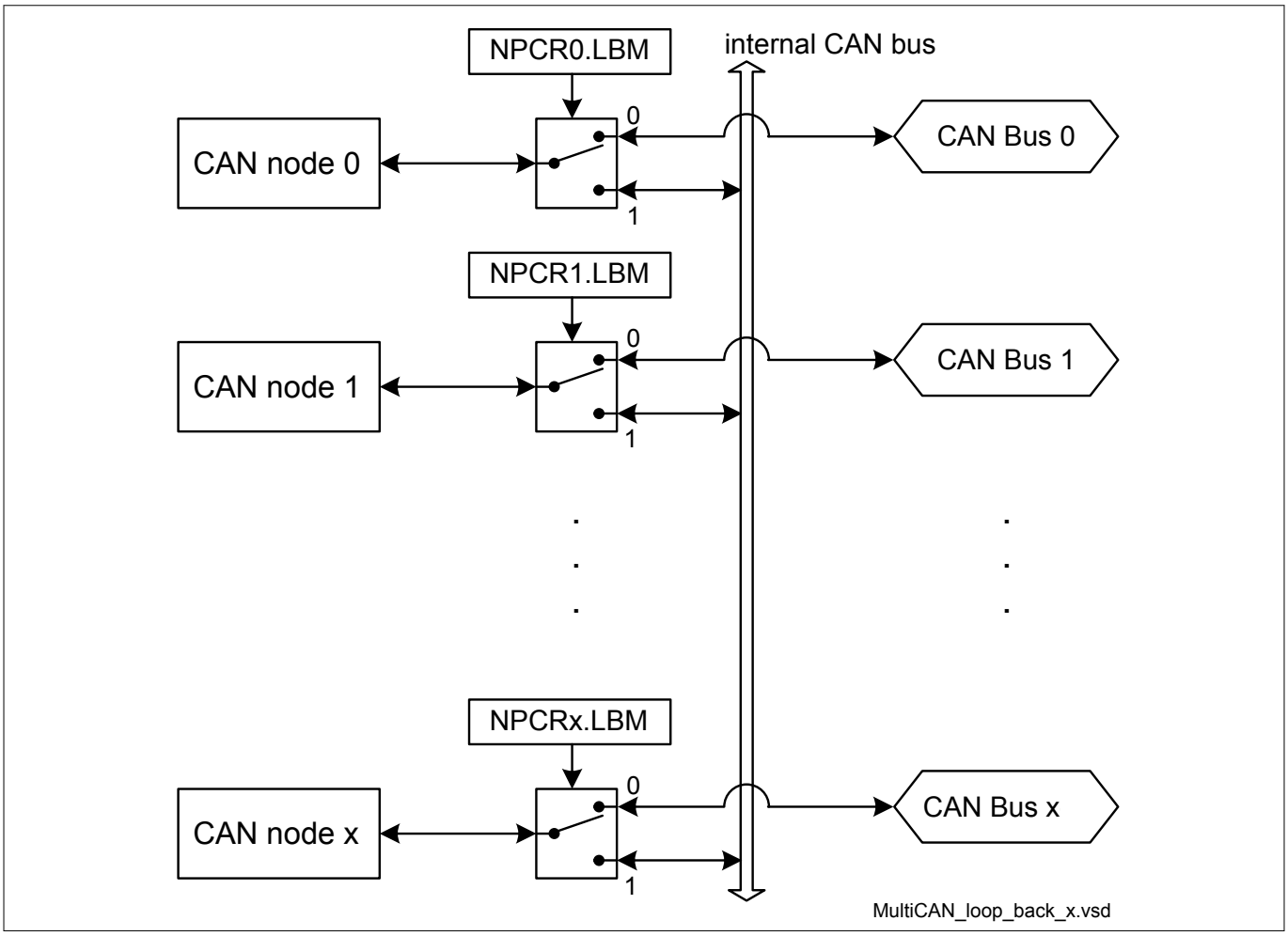


Figure 133 Loop-Back Mode

19.3.6.3 Bit Timing Analysis

Detailed analysis of the bit timing can be performed for each CAN node using the analysis modes of the CAN frame counter. The bit timing analysis functionality of the frame counter may be used for automatic detection of the CAN baud rate, as well as to analyze the timing of the CAN network.

Bit timing analysis for CAN node x is selected when bit field NFCRx.CFMOD = 10_B. Bit timing analysis does not affect the operation of the CAN node.

The bit timing measurement results are written into the NFCRx.CFC bit field. Whenever NFCRx.CFC is updated in bit timing analysis mode, bit NFCRx.CFCOV is also set to indicate the CFC update event. The value of NFCRx.CFC is valid one module cycle later when NFCRx.CFCOV is set. If NFCRx.CFCIE is set, an interrupt request can be generated (see ***Figure 130***).

Automatic Baud Rate Detection

For automatic baud rate detection, the time between the observation of subsequent dominant edges on the CAN bus must be measured. This measurement is automatically performed if bit field NFCRx.CFSEL = 000_B. With each dominant edge monitored on the CAN receive input line, the time (measured in f_{CLC} clock cycles) between this edge and the most recent dominant edge is stored in the NFCRx.CFC bit field.

Synchronization Analysis

The bit time synchronization is monitored if NFCRx.CFSEL = 010_B. The time between the first dominant edge and the sample point is measured and stored in the NFCRx.CFC bit field. The bit timing synchronization offset

may be derived from this time as the first edge after the sample point triggers synchronization and there is only one synchronization between consecutive sample points.

Synchronization analysis can be used, for example, for fine tuning of the baud rate during reception of the first CAN frame with the measured baud rate.

Driver Delay Measurement

The delay between a transmitted edge and the corresponding received edge is measured when NFCRx.CFSEL = 011_B (dominant to dominant) and NFCRx.CFSEL = 100_B (recessive to recessive). These delays indicate the time needed to represent a new bit value on the physical implementation of the CAN bus.

19.3.7 Message Acceptance Filtering

The chapter describes the Message Acceptance Filtering capabilities of the MulticanCAN+ module.

19.3.7.1 Receive Acceptance Filtering

When a CAN frame is received by a CAN node, a unique message object is determined in which the received frame is stored after successful frame reception. A message object is qualified for reception of a frame if the following six conditions are met.

- The message object is allocated to the message object list of the CAN node by which the frame is received.
- Bit MOSTATn.MSGVAL in the Message Object Status Register (see page ***589***) is set.
- Bit MOSTATn.RXEN is set.
- Bit MOSTATn.DIR is equal to bit RTR of the received frame.

  If bit MOSTATn.DIR = 1 (transmit object), the message object accepts only Remote Frames. If bit MOSTATn.DIR = 0 (receive object), the message object accepts only Data Frames.
- If bit MOAMRn.MIDE = 1, the IDE bit of the received frame becomes evaluated in the following way: If MOARn.IDE = 1, the IDE bit of the received frame must be set (indicates extended identifier). If MOARn.IDE = 0, the IDE bit of the received frame must be cleared (indicates standard identifier).

  If bit MOAMRn.MIDE = 0, the IDE bit of the received frame is “don’t care”. In this case, message objects with standard and extended frames are accepted.
- The identifier of the received frame matches the identifier stored in the Arbitration Register of the message object as qualified by the acceptance mask in the MOAMRn register. This means that each bit of the received message object identifier is equal to the bit field MOARn.ID, except those bits for which the corresponding acceptance mask bits in bit field MOAMRn.AM are cleared. These identifier bits are “don’t care” for reception. ***Figure 134*** illustrates this receive message identifier check.

Among all messages that fulfill all six qualifying criteria the message object with the highest receive priority wins receive acceptance filtering and becomes selected to store the received frame. All other message objects lose receive acceptance filtering. The following priority scheme is defined for the message objects:

A message object a (MOa) has higher receive priority than a message object b (MOb) if the following two conditions are fulfilled (see page ***598***):

1. MOa has a higher priority class than MOb. This means, the 2-bit priority bit field MOARa.PRI must be equal or less than bit field MOARb.PRI.
2. If both message objects have the same priority class (MOARa.PRI = MOARb.PRI), MOb is a list successor of MOa. This means that MOb can be reached by means of successively stepping forward in the list, starting from a.

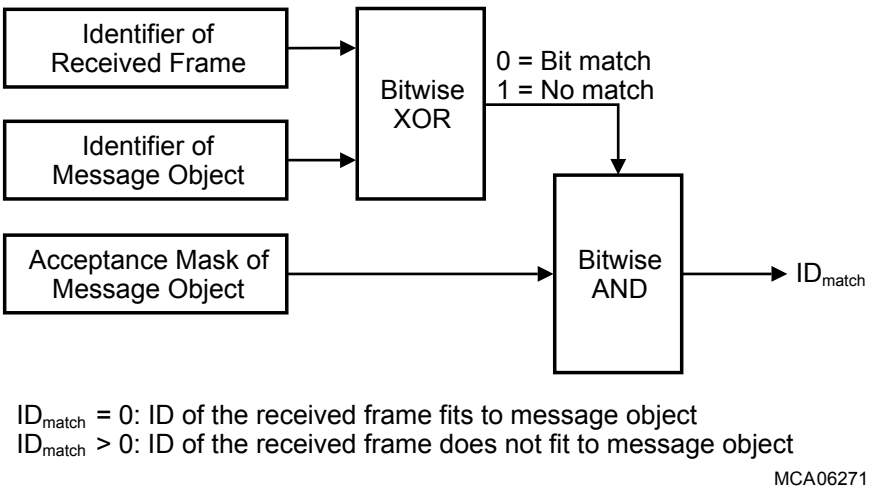


Figure 134 Received Message Identifier Acceptance Check

19.3.7.2 Transmit Acceptance Filtering

A message is requested for transmission by setting a transmit request in the message object that holds the message. If more than one message object have a valid transmit request for the same CAN node, one of these message objects is chosen for transmission, because only a single message object can be transmitted at one time on a CAN bus.

A message object is qualified for transmission on a CAN node if the following four conditions are met (see also ***Figure 135***).

1. The message object is allocated to the message object list of the CAN node.
2. Bit MOSTATn.MSGVAL is set.
3. Bit MOSTATn.TXRQ is set.
4. Bit MOSTATn.TXEN0 and MOSTATn.TXEN1 are set.

A priority scheme determines which one of all qualifying message objects is transmitted first. It is assumed that message object a (MOa) and message object b (MOb) are two message objects qualified for transmission. MOb is a list successor of MOa. For both message objects, CAN messages CANa and CANb are defined (identifier, IDE, and RTR are taken from the message-specific bit fields and bits MOARn.ID, MOARn.IDE and MOSTATn.DIR).

If both message objects belong to the same priority class (identical PRI bit field in register MOARn), MOa has a higher transmit priority than MOb if one of the following conditions is fulfilled.

- PRI = 10_B and CAN message MOa has higher or equal priority than CAN message MOb with respect to CAN arbitration rules (see ***Table 239*** on page ***598***).
- PRI = 01_B or PRI = 11_B (priority by list order).
- PRI = 00_B is reserved and makes the message object to have no function.

The message object that is qualified for transmission and has highest transmit priority wins the transmit acceptance filtering, and will be transmitted first. All other message objects lose the current transmit acceptance filtering round. They get a new chance in subsequent acceptance filtering rounds.

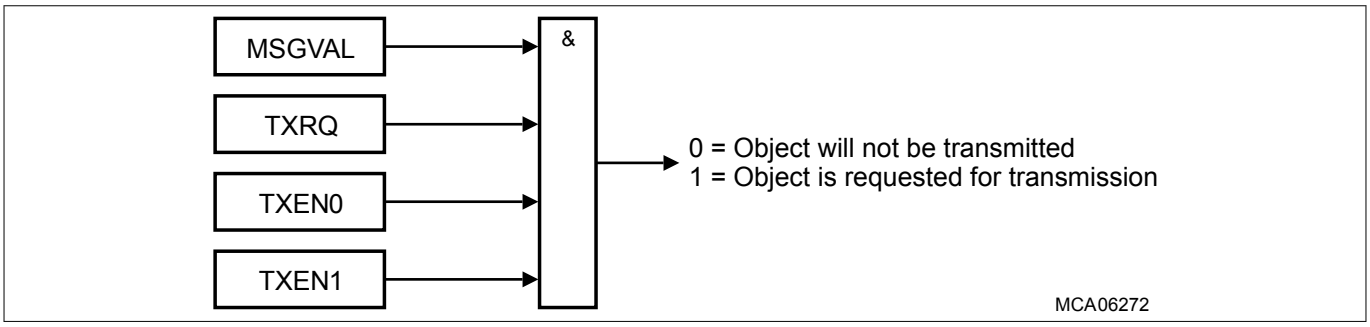


Figure 135 Effective Transmit Request of Message Object

19.3.8 Message Postprocessing

After a message object has successfully received or transmitted a frame, the CPU can be notified to perform a postprocessing on the message object. The postprocessing of the MulticanCAN+ module consists of two elements:

1. Message interrupts to trigger postprocessing.
2. Message pending registers to collect pending message interrupts into a common structure for postprocessing.

19.3.8.1 Message Object Interrupts

When the storage of a received frame into a message object or the successful transmission of a frame is completed, a message interrupt can be issued. For each message object, a transmit and a receive interrupt can be generated and routed to one of the sixteen CAN interrupt output lines (see ***Figure 136***). A receive interrupt occurs also after a frame storage event that has been induced by a FIFO or a gateway action. The status bits TXPND and RXPND in the Message Object n Status Register are always set after a successful transmission/ reception, whether or not the respective message interrupt is enabled.

A third FIFO full interrupt condition of a message object is provided. If bit field MOFCRn.OVIE (Overflow Interrupt Enable) is set, the FIFO full interrupt will be activated depending on the actual message object type.

In case of a Receive FIFO Base Object (MOFCRn.MMC = 0001_B), the FIFO full interrupt is routed to the interrupt output line INT_Om as defined by the transmit interrupt node pointer MOIPRn.TXINP.

In case of a Transmit FIFO Base Object (MOFCRn.MMC = 0010_B), the FIFO full interrupt becomes routed to the interrupt output line INT_Om as defined by the receive interrupt node pointer MOIPRn.RXINP.

See also ***Interrupt Control*** on page 606 for further processing of the message object interrupts.

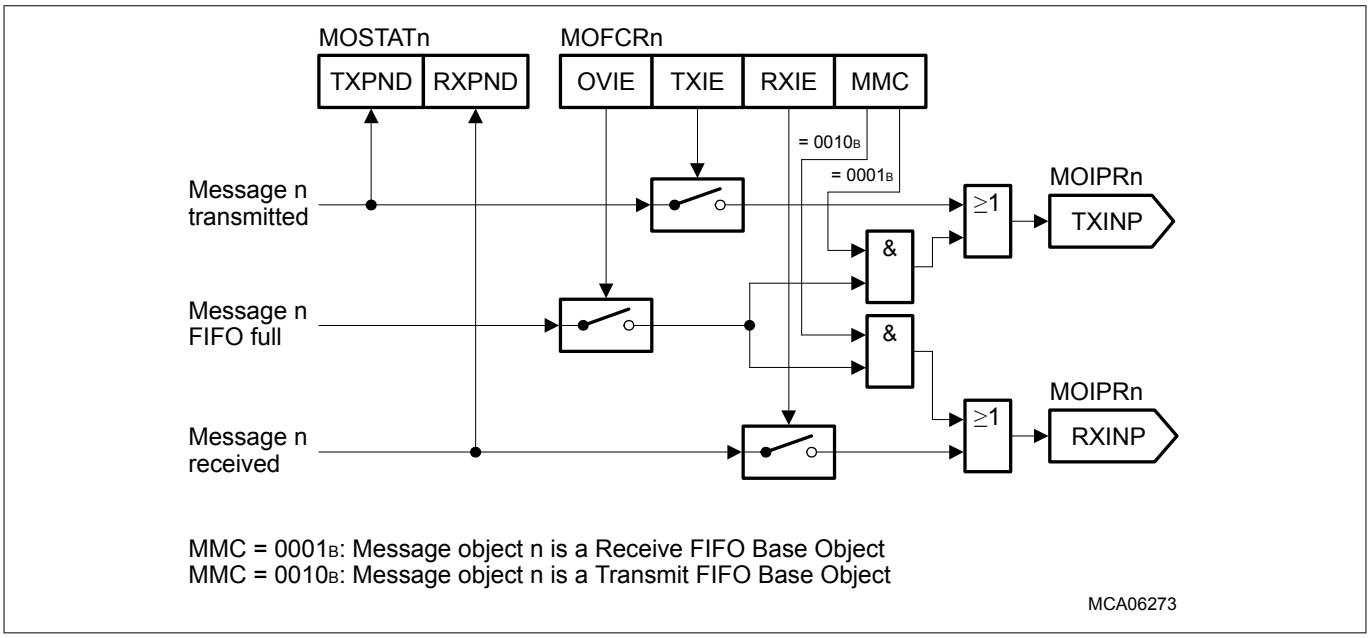


Figure 136 Message Interrupt Request Routing

19.3.8.2 Pending Messages

When a message interrupt request is generated, a message pending bit is set in one of the Message Pending Registers. There are 8 Message Pending Registers, MSPNDk (k = 0-7) with 32 pending bits available each. The general ***Figure 137*** shows the allocation of the message pending bits in case that the maximum possible number of eight Message Pending Registers are implemented and available on the chip.

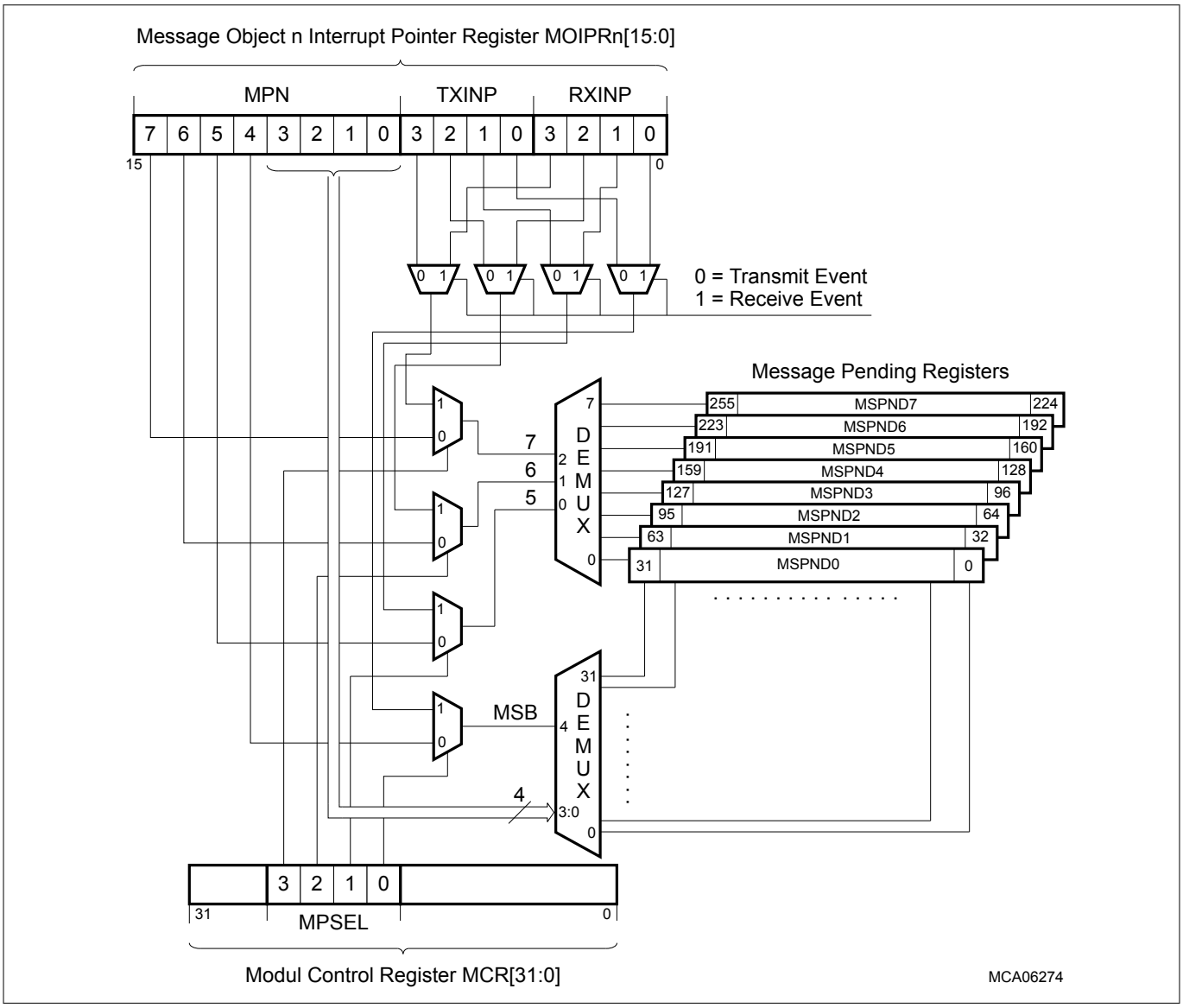


Figure 137 Message Pending Bit Allocation

The location of a pending bit is defined by two demultiplexers selecting the number k of the MSPNDk registers (3-bit demux), and the bit location within the corresponding MSPNDk register (5-bit demux).

Allocation Case 1

In this allocation case, bit field MCR.MPSEL = 0000_B (see page ***571***). The location selection consists of 2 parts:

- The upper three bits of MOIPRn.MPN (MPN[7:5]) select the number k of a Message Pending Register MSPNDk in which the pending bit will be set.
- The lower five bits of MOIPRn.MPN (MPN[4:0]) select the bit position (0-31) in MSPNDk for the pending bit to be set.

Allocation Case 2

In this allocation case, bit field MCR.MPSEL is taken into account for pending bit allocation. Bit field MCR.MPSEL makes it possible to include the interrupt request node pointer for reception (MOIPRn.RXINP) or transmission (MOIPRn.TXINP) for pending bit allocation in such a way that different target locations for the pending bits are used in receive and transmit case. If MPSEL = 1111_B, the location selection operates in the following way:

- At a transmit event, the upper 3 bits of TXINP determine the number k of a Message Pending Register MSPNDk in which the pending bit will be set. At a receive event, the upper 3 bits of RXINP determine the number k.
- The bit position (0-31) in MSPNDk for the pending bit to be set is selected by the lowest bit of TXINP or RXINP (selects between low and high half-word of MSPNDk) and the four least significant bits of MPN.

General Hints

The Message Pending Registers MSPNDk can be written by software. Bits that are written with 1 are left unchanged, and bits which are written with 0 are cleared. This makes it possible to clear individual MSPNDk bits with a single register write access. Therefore, access conflicts are avoided when the MulticanCAN+ module (hardware) sets another pending bit at the same time when software writes to the register.

Each Message Pending Register MSPNDk is associated with a Message Index Register MSIDk (see page ***574***) which indicates the lowest bit position of all set (1) bits in Message Pending Register k. The MSIDk register is a read-only register that is updated immediately when a value in the corresponding Message Pending Register k is changed by software or hardware.

19.3.9 Message Object Data Handling

This chapter describes the handling capabilities for the Message Object Data of the MulticanCAN+ module.

19.3.9.1 Frame Reception

After the reception of a message, it is stored in a message object according to the scheme shown in ***Figure 138***. The MulticanCAN+ module not only copies the received data into the message object, and it provides advanced features to enable consistent data exchange between MulticanCAN+ and CPU.

MSGVAL

Bit MSGVAL (Message Valid) in the Message Object n Status Register MOSTATn is the main switch of the message object. During the frame reception, information is stored in the message object only when MSGVAL = 1. If bit MSGVAL is reset by the CPU, the MulticanCAN+ module stops all ongoing write accesses to the message object. Now the message object can be re-configured by the CPU with subsequent write accesses to it without being disturbed by the MulticanCAN+.

RTSEL

When the CPU re-configures a message object during CAN operation (for example, clears MSGVAL, modifies the message object and sets MSGVAL again), the following scenario can occur:

1. The message object wins receive acceptance filtering.
2. The CPU clears MSGVAL to re-configure the message object.
3. The CPU sets MSGVAL again after re-configuration.
4. The end of the received frame is reached. As MSGVAL is set, the received data is stored in the message object, a message interrupt request is generated, gateway and FIFO actions are processed, etc.

After the re-configuration of the message object (after step 3 above) the storage of further received data may be undesirable. This can be achieved through bit MOSTATn.RTSEL (Receive/Transmit Selected) that makes it possible to disconnect a message object from an ongoing frame reception.

When a message object wins the receive acceptance filtering, its RTSEL bit is set by the MulticanCAN+ module to indicate an upcoming frame delivery. The MulticanCAN+ module checks RTSEL whether it is set on successful frame reception to verify that the object is still ready for receiving the frame. The received frame is then stored in the message object (along with all subsequent actions such as message interrupts, FIFO & gateway actions, flag updates) only if RTSEL = 1.

When a message object is invalidated during CAN operation (resetting bit MSGVAL), RTSEL should be cleared before setting MSGVAL again (latest with the same write access that sets MSGVAL) to prevent the storage of a

frame that belongs to the old context of the message object. Therefore, a message object re-configuration should consist of the following steps:

1. Clear MSGVAL bit
2. Re-configure the message object while MSGVAL = 0
3. Clear RTSEL bit and set MSGVAL again

RXEN

Bit MOSTATn.RXEN enables a message object for frame reception. A message object can receive CAN messages from the CAN bus only if RXEN = 1. The MulticanCAN+ module evaluates RXEN only during receive acceptance filtering. After receive acceptance filtering, RXEN is ignored and has no further influence on the actual storage of a received message in a message object.

Bit RXEN enables the “soft phase out” of a message object: after clearing RXEN, a currently received CAN message for which the message object has won acceptance filtering is still stored in the message object but for subsequent messages the message object no longer wins receive acceptance filtering.

RXUPD, NEWDAT and MSGLST

An ongoing frame storage process is indicated by the RXUPD (Receive Updating) flag in the MOSTATn register. RXUPD is set with the start and cleared with the end of a message object update, which consists of frame storage as well as flag updates.

After storing the received frame (identifier, IDE bit, DLC; including the Data Field for Data Frames), the NEWDAT (New Data) bit of the message object is set. If NEWDAT was already set before it becomes set again, bit MSGLST (Message Lost) is set to indicate a data loss condition.

The RXUPD and NEWDAT flags can help to read consistent frame data from the message object during an ongoing CAN operation. The following steps are recommended to be executed:

1. Clear NEWDAT bit.
2. Read message content (identifier, data etc.) from the message object.
3. Check that both, NEWDAT and RXUPD, are cleared. If this is not the case, go back to step 1.
4. When step 3 was successful, the message object contents is consistent and has not been updated by the MulticanCAN+ module while reading.

Bits RXUPD, NEWDAT and MSGLST have the same behavior for the reception of Data as well as Remote Frames.

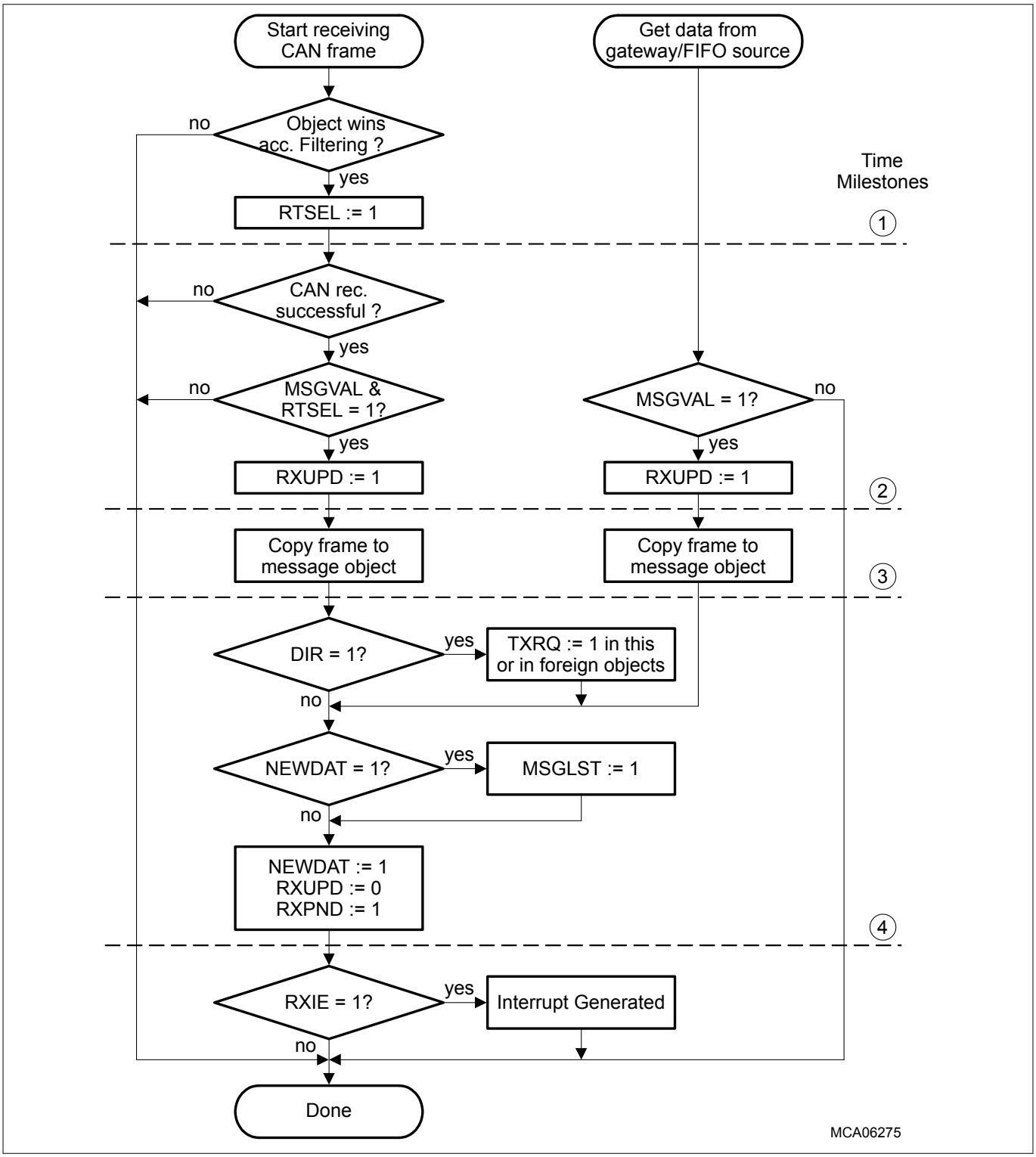


Figure 138 Reception of a Message Object

19.3.9.2 Frame Transmission

The process of a message object transmission is shown in ***Figure 139***. Along with the copy of the message object content to be transmitted (identifier, IDE bit, RTR = DIR bit, DLC, including the Data Field for Data Frames) into the internal transmit buffer of the assigned CAN node, several status flags are also served and monitored to control consistent data handling.

The transmission process of a message object starting after the transmit acceptance filtering is identical for Remote and Data Frames.

MSGVAL, TXRQ, TXEN0, TXEN1

A message can only be transmitted if all four bits in registers MOSTATn, MSGVAL (Message Valid), TXRQ (Transmit Request), TXEN0 (Transmit Enable 0), TXEN1 (Transmit Enable 1) are set as shown in ***Figure 135***. Although these bits are equivalent with respect to the transmission process, they have different semantics:

Table 230 Message Transmission Bit Definitions

Bit	Description
MSGVAL	Message Valid This is the main switch bit of the message object.
TXRQ	Transmit Request This is the standard transmit request bit. This bit must be set whenever a message object should be transmitted. TXRQ is cleared by hardware at the end of a successful transmission, except when there is new data (indicated by NEWDAT = 1) to be transmitted. When bit MOFCRn.STT (“Single Transmit Trial”) is set, TXRQ becomes already cleared when the contents of the message object are copied into the transmit frame buffer of the CAN node. A received remote request (after a Remote Frame reception) sets bit TXRQ to request the transmission of the requested data frame.
TXEN0	Transmit Enable 0 This bit can be temporarily cleared by software to suppress the transmission of this message object when it writes new content to the Data Field. This avoids transmission of inconsistent frames that consist of a mixture of old and new data. Remote requests are still accepted when TXEN0 = 0, but transmission of the Data Frame is suspended until transmission is re-enabled by software (setting TXEN0).
TXEN1	Transmit Enable 1 This bit is used in transmit FIFOs to select the message object that is transmit active within the FIFO structure. For message objects that are not transmit FIFO elements, TXEN1 can either be set permanently to 1 or can be used as a second independent transmission enable bit.

RTSEL

When a message object has been identified to be transmitted next after transmission acceptance filtering, bit MOSTATn.RTSEL (Receive/Transmit Selected) is set.

When the message object is copied into the internal transmit buffer, bit RTSEL is checked, and the message is transmitted only if RTSEL = 1. After the successful transmission of the message, bit RTSEL is checked again and the message postprocessing is only executed if RTSEL = 1.

For a complete re-configuration of a valid message object, the following steps should be executed:

1. Clear MSGVAL bit
2. Re-configure the message object while MSGVAL = 0
3. Clear RTSEL and set MSGVAL

Clearing of RTSEL ensures that the message object is disconnected from an ongoing/scheduled transmission and no message object processing (copying message to transmit buffer including clearing NEWDAT, clearing TXRQ, time stamp update, message interrupt, etc.) within the old context of the object can occur after the message object becomes valid again, but within a new context.

NEWDAT

When the contents of a message object have been transferred to the internal transmit buffer of the CAN node, bit MOSTATn.NEWDAT (New Data) is cleared by hardware to indicate that the transmit message object data is no longer new.

When the transmission of the frame is successful and NEWDAT is still cleared (if no new data has been copied into the message object meanwhile), TXRQ (Transmit Request) is cleared automatically by hardware.

If, however, the NEWDAT bit has been set again by the software (because a new frame should be transmitted), TXRQ is not cleared to enable the transmission of the new data.

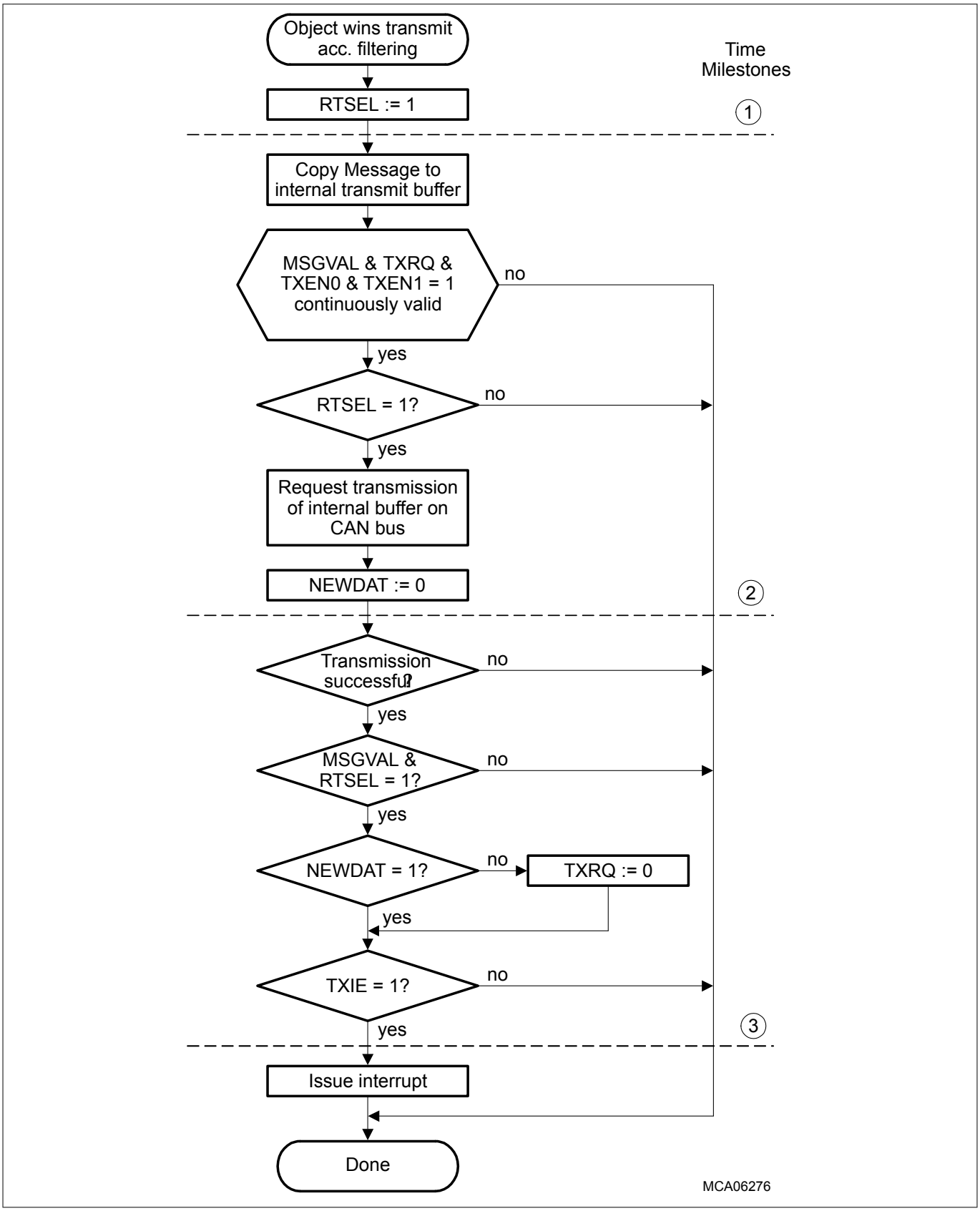


Figure 139 Transmission of a Message Object

19.3.10 Message Object Functionality

This chapter describes the functionality of the Message Objects in the MulticanCAN+ module.

19.3.10.1 Standard Message Object

A message object is selected as standard message object when bit field MOFCRn.MMC = 0000_B (see page ***583***). The standard message object can transmit and receive CAN frames according to the basic rules described in the previous sections. Additional services such as Single Data Transfer Mode or Single Transmit Trial (see following sections) are available and can be individually selected.

19.3.10.2 Single Data Transfer Mode

Single Data Transfer Mode is a useful feature in order to broadcast data over the CAN bus without unintended duplication of information. Single Data Transfer Mode is selected via bit MOFCRn.SDT.

Message Reception

When a received message stored in a message object is overwritten by a new received message, the contents of the first message are lost and replaced with the contents of the new received message (indicated by MSGLST = 1).

If SDT is set (Single Data Transfer Mode activated), bit MSGVAL of the message object is automatically cleared by hardware after the storage of a received Data or Remote Frame. This prevents the reception of further messages.

Message Transmission

When a message object receives a series of multiple remote requests, it transmits several Data Frames in response to the remote requests. If the data within the message object has not been updated in the time between the transmissions, the same data can be sent more than once on the CAN bus.

In Single Data Transfer Mode (SDT = 1), this is avoided because MSGVAL is automatically cleared after the successful transmission of a Data or Remote Frame.

19.3.10.3 Single Transmit Trial

If the bit STT in the message object function register is set (STT = 1), the transmission request is cleared (TXRQ = 0) when the frame contents of the message object have been copied to the internal transmit buffer of the CAN node. Thus, the transmission of the message object is not tried again when it fails due to CAN bus errors.

19.3.10.4 Message Object FIFO Structure

In case of high CPU load it may be difficult to process a series of CAN frames in time. This may happen if multiple messages are received or must be transmitted in short time.

Therefore, a FIFO buffer structure is available to avoid loss of incoming messages and to minimize the setup time for outgoing messages. The FIFO structure can also be used to automate the reception or transmission of a series of CAN messages and to generate a single message interrupt when the whole CAN frame series is done.

There can be several FIFOs in parallel. The number of FIFOs and their size are limited only by the number of available message objects. A FIFO can be installed, resized and de-installed at any time, even during CAN operation.

The basic structure of a FIFO is shown in ***Figure 140***. A FIFO consists of one base object and n slave objects. The slave objects are chained together in a list structure (similar as in message object lists). The base object may be allocated to any list. Although ***Figure 140*** shows the base object as a separate part beside the slave objects, it is also possible to integrate the base object at any place into the chain of slave objects. This means that the base

object is slave object, too (not possible for gateways). The absolute object numbers of the message objects have no impact on the operation of the FIFO.

The base object does not need to be allocated to the same list as the slave objects. Only the slave object must be allocated to a common list (as they are chained together). Several pointers (BOT, CUR and TOP) that are located in the Message Object n FIFO/Gateway Pointer Register MOFGPRn link the base object to the slave objects, regardless whether the base object is allocated to the same or to another **list** than the slave objects.

The smallest FIFO would be a single message object which is both, FIFO base and FIFO slave (not very useful). The biggest possible FIFO structure would include all message objects of the MulticanCAN+ module. Any FIFO sizes between these limits are possible.

In the FIFO base object, the FIFO boundaries are defined. Bit field MOFGPRn.BOT of the base object points to (includes the number of) the bottom slave object in the FIFO structure. The MOFGPRn.TOP bit field points to (includes the number of) the top slave object in the FIFO structure. The MOFGPRn.CUR bit field points to (includes the number of) the slave object that is actually selected by the MulticanCAN+ module for message transfer. When a message transfer takes place with this object, CUR is set to the next message object in the list structure of the slave objects (CUR = PNEXT of current object). If CUR was equal to TOP (top of the FIFO reached), the next update of CUR will result in CUR = BOT (wrap-around from the top to the bottom of the FIFO). This scheme represents a circular FIFO structure where the bit fields BOT and TOP establish the link from the last to the first element.

Bit field MOFGPRn.SEL of the base object can be used for monitoring purposes. It makes it possible to define a slave object within the list at which a message interrupt is generated whenever the CUR pointer reaches the value of the SEL pointer. Thus SEL makes it possible to detect the end of a predefined message transfer series or to issue a warning interrupt when the FIFO becomes full.

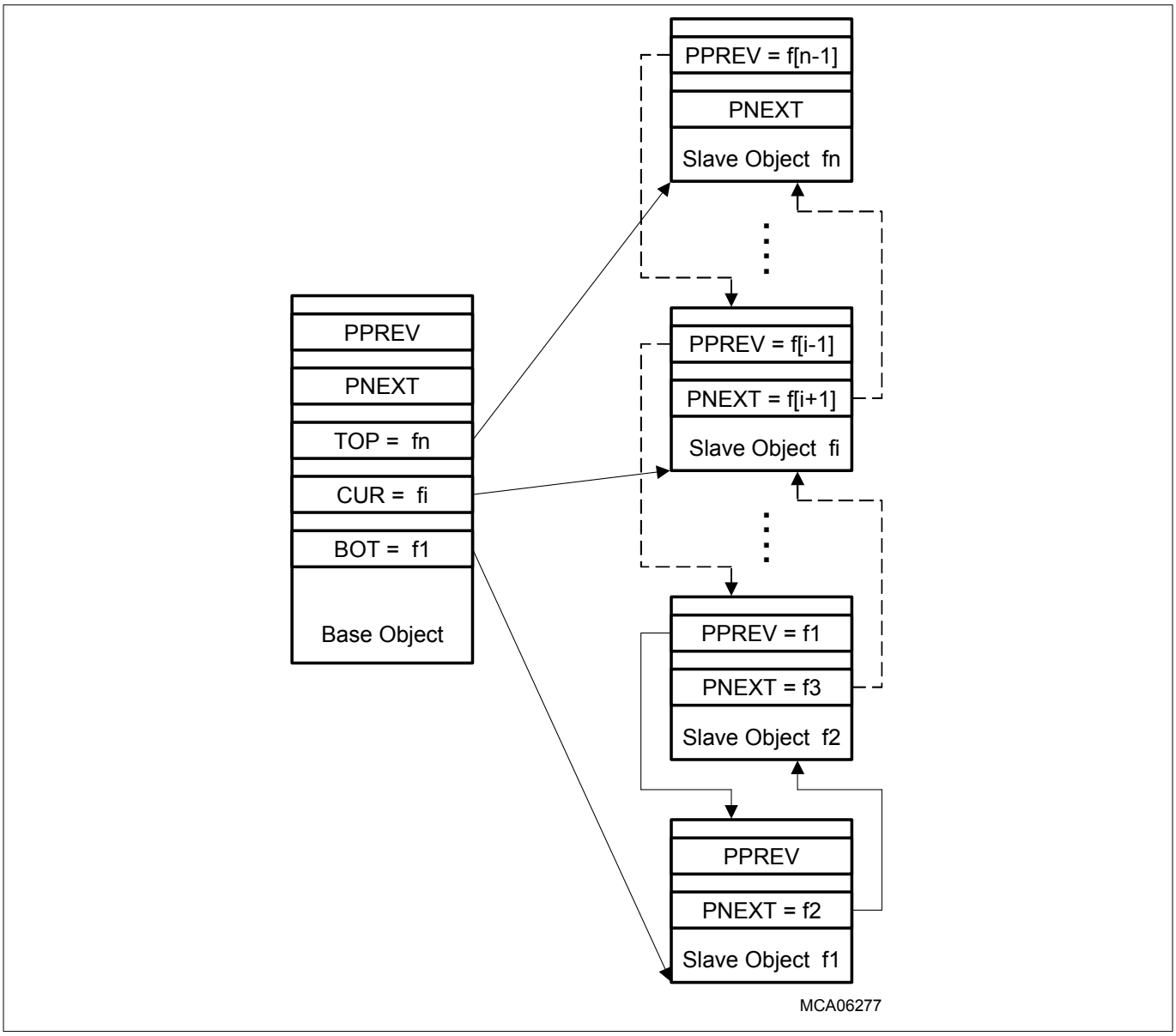


Figure 140 FIFO Structure with FIFO Base Object and n FIFO Slave Objects

19.3.10.5 Receive FIFO

The Receive FIFO structure is used to buffer incoming (received) Remote or Data Frames.

A Receive FIFO is selected by setting MOFCRn.MMC = 0001_B in the FIFO base object. This MMC code automatically designates a message object as FIFO base object. The message modes of the FIFO slave objects are not relevant for the operation of the Receive FIFO.

When the FIFO base object receives a frame from the CAN node it belongs to, the frame is not stored in the base object itself but in the message object that is selected by the base object's MOFGPRn.CUR pointer. This message object receives the CAN message as if it is the direct receiver of the message. However, MOFCRn.MMC = 0000_B is implicitly assumed for the FIFO slave object, and a standard message delivery is performed. The actual message mode (MMC setting) of the FIFO slave object is ignored. For the slave object, no acceptance filtering takes place that checks the received frame for a match with the identifier, IDE bit, and DIR bit.

With the reception of a CAN frame, the current pointer CUR of the base object is set to the number of the next message object in the FIFO structure. This message object will then be used to store the next incoming message.

If bit field MOFCRn.OVIE (“Overflow Interrupt Enable”) of the FIFO base object is set and the current pointer MOFGPRn.CUR becomes equal to MOFGPRn.SEL, a FIFO overflow interrupt request is generated. This interrupt request is generated on interrupt node TXINP of the base object immediately after the storage of the received frame in the slave object. Transmit interrupts are still generated if TXIE is set.

A CAN message is stored in FIFO base and slave object only if MSGVAL = 1.

In order to avoid direct reception of a message by a slave message object, as if it was an independent message object and not a part of a FIFO, the bit RXEN of each slave object must be cleared. The setting of the bit RXEN is “don’t care” only if the slave object is located in a list not assigned to a CAN node.

19.3.10.6 Transmit FIFO

The Transmit FIFO structure is used to buffer a series of Data or Remote Frames that must be transmitted. A transmit FIFO consists of one base message object and one or more slave message objects.

A Transmit FIFO is selected by setting MOFCRn.MMC = 0010_B in the FIFO base object. Unlike the Receive FIFO, slave objects assigned to the Transmit FIFO must explicitly set their bit fields MOFCRn.MMC = 0011_B. The CUR pointer in all slave objects must point back to the Transmit FIFO Base Object (to be initialized by software).

The MOSTATn.TXEN1 bits (Transmit Enable 1) of all message objects except the one which is selected by the CUR pointer of the base object must be cleared by software. TXEN1 of the message (slave) object selected by CUR must be set. CUR (of the base object) may be initialized to any FIFO slave object.

When tagging the message objects of the FIFO as valid to start the operation of the FIFO, then the base object must be tagged valid (MSGVAL = 1) first.

Before a Transmit FIFO becomes de-installed during operation, its slave objects must be tagged invalid (MSGVAL = 0).

The Transmit FIFO uses the TXEN1 bit in the Message Object Status Register of all FIFO elements to select the actual message for transmission. Transmit acceptance filtering evaluates TXEN1 for each message object and a message object can win transmit acceptance filtering only if its TXEN1 bit is set. When a FIFO object has transmitted a message, the hardware clears its TXEN1 bit in addition to standard transmit postprocessing (clear TXRQ, transmit interrupt etc.), and moves the CUR pointer in the next FIFO base object to be transmitted. TXEN1 is set automatically (by hardware) in the next message object. Thus, TXEN1 moves along the Transmit FIFO structure as a token that selects the active element.

If bit field MOFCRn.OVIE (“Overflow Interrupt Enable”) of the FIFO base object is set and the current pointer CUR becomes equal to MOFGPRn.SEL, a FIFO overflow interrupt request is generated. The interrupt request is generated on interrupt node RXINP of the base object after postprocessing of the received frame. Receive interrupts are still generated for the Transmit FIFO base object if bit RXIE is set.

19.3.10.7 Gateway Mode

The Gateway Mode makes it possible to establish an automatic information transfer between two independent CAN buses without CPU interaction.

The Gateway Mode operates on message object level. In Gateway mode, information is transferred between two message objects, resulting in an information transfer between the two CAN nodes to which the message objects are allocated. A gateway may be established with any pair of CAN nodes, and there can be as many gateways as there are message objects available to build the gateway structure.

Gateway Mode is selected by setting MOFCRs.MMC = 0100_B for the gateway source object s. The gateway destination object d is selected by the MOFGPRs.CUR=d pointer of the source object. The gateway destination object only needs to be valid (its MSGVAL = 1). All other settings are not relevant for the information transfer from the source object to the destination object.

Gateway source object behaves as a standard message object with the difference that some additional actions are performed by the MulticanCAN+ module when a CAN frame has been received and stored in the source object (see ***Figure 141***):

1. If bit MOFCRs.DLCC is set, the data length code MOFCRs.DLC is copied from the gateway source object to the gateway destination object.
2. If bit MOFCRs.IDC is set, the identifier MOARs.ID and the identifier extension MOARs.IDE are copied from the gateway source object to the gateway destination object.
3. If bit MOFCRs.DATC is set, the data bytes stored in the two data registers MODATALs and MODATAHs are copied from the gateway source object to the gateway destination object. All 8 data bytes are copied, even if MOFCRs.DLC indicates less than 8 data bytes.
4. If bit MOFCRs.GDFS is set, the transmit request flag MOSTATd.TXRQ is set in the gateway destination object.
5. The receive pending bit MOSTATd.RXPND and the new data bit MOSTATd.NEWDAT are set in the gateway destination object.
6. A message interrupt request is generated for the gateway destination object if its MOSTATd.RXIE is set.
7. The current object pointer MOFGPRs.CUR of the gateway source object is moved to the next destination object according to the FIFO rules as described on page ***554***. A gateway with a single (static) destination object is obtained by setting MOFGPRs.TOP = MOFGPRs.BOT = MOFGPRs.CUR = destination object.

The link from the gateway source object to the gateway destination object works in the same way as the link from a FIFO base to a FIFO slave. This means that a gateway with an integrated destination FIFO may be created; in ***Figure 140***, the object on the left is the gateway source object and the message object on the right side is the gateway destination objects.

The gateway operates equivalent for the reception of data frames (source object is receive object, i.e. DIR = 0) as well as for the reception of Remote Frames (source object is transmit object).

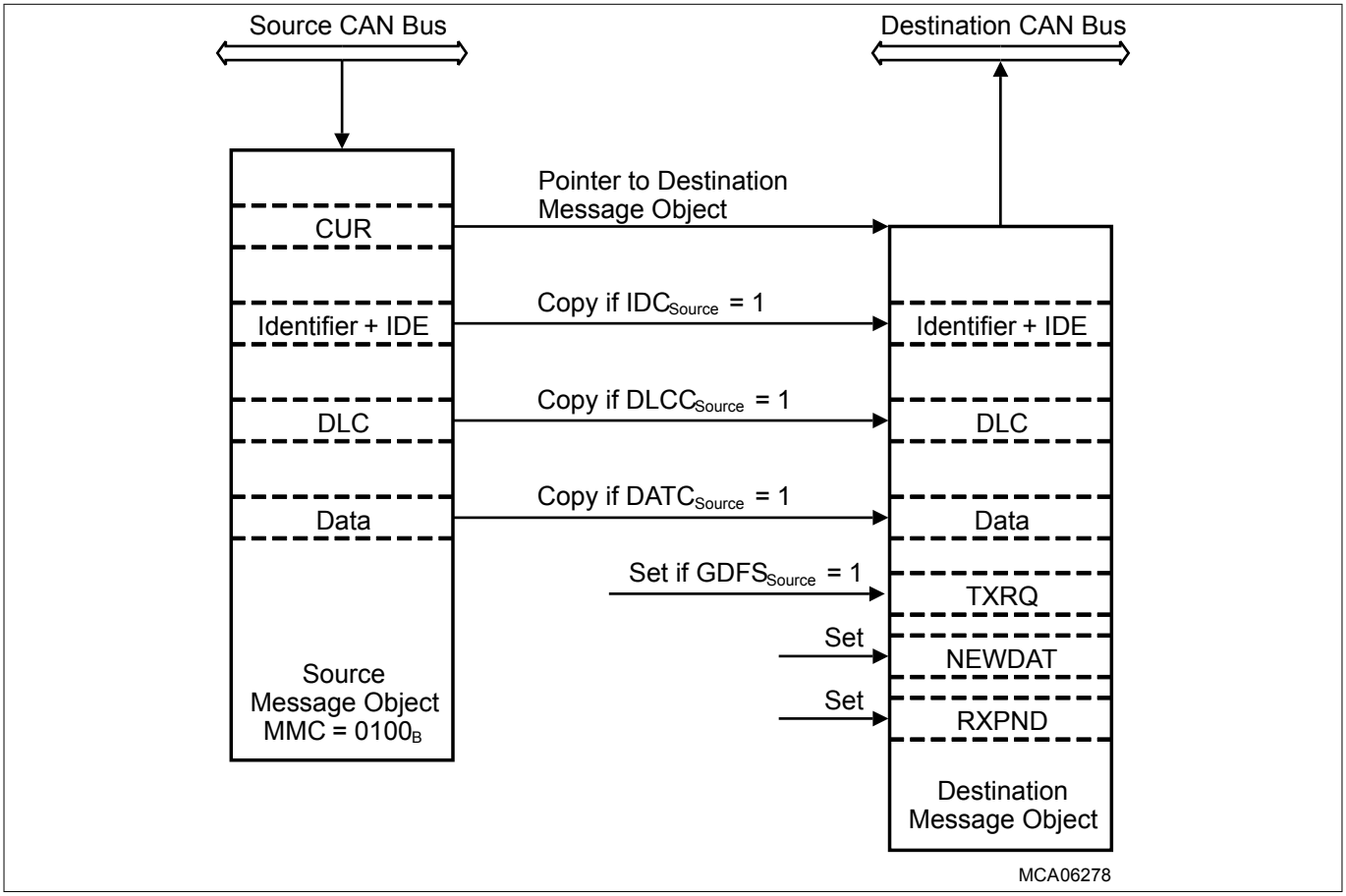


Figure 141 Gateway Transfer from Source to Destination

19.3.10.8 Foreign Remote Requests

When a Remote Frame has been received on a CAN node and is stored in a message object, a transmit request is set to trigger the answer (transmission of a Data Frame) to the request or to automatically issue a secondary request. If the Foreign Remote Request Enable bit MOFCRn.FRREN is cleared in the message object in which the remote request is stored, MOSTATn.TXRQ is set in the same message object.

If bit FRREN is set (FRREN = 1: foreign remote request enabled), TXRQ is set in the message object that is referenced by pointer MOFGPRn.CUR. The value of CUR is, however, not changed by this feature.

Although the foreign remote request feature works independently of the selected message mode, it is especially useful for gateways to issue a remote request on the source bus of a gateway after the reception of a remote request on the gateway destination bus. According to the setting of FRREN in the gateway destination object, there are two capabilities to handle remote requests that appear on the destination side (assuming that the source object is a receive object and the destination is a transmit object, i.e. $DIR_{source} = 0$ and $DIR_{destination} = 1$):

FRREN = 0 in the Gateway Destination Object

1. A Remote Frame is received by gateway destination object.
2. TXRQ is set automatically in the gateway destination object.
3. A Data Frame with the current data stored in the destination object is transmitted on the destination bus.

FRREN = 1 in the Gateway Destination Object

1. A Remote Frame is received by gateway destination object.
2. TXRQ is set automatically in the gateway source object (must be referenced by CUR pointer of the destination object).
3. A remote request is transmitted by the source object (which is a receive object) on the source CAN bus.
4. The receiver of the remote request responds with a Data Frame on the source bus.
5. The Data Frame is stored in the source object.
6. The Data Frame is copied to the destination object (gateway action).
7. TXRQ is set in the destination object (assuming $GDFS_{source} = 1$).
8. The new data stored in the destination object is transmitted on the destination bus, in response to the initial remote request on the destination bus.

19.4 Use Case Example MultiCAN+

This section explains the core functionality of the MultiCAN+ module with a code example. The example realizes sending a CAN message via internal CAN-bus from node 0 to node 1.

The MulticanCAN+ module for the IMC300A consists of module (i.e MultiCAN with 2 CAN nodes), representing serial communication interfaces. Each CAN node can either be connected to a port or to the internal CAN bus (see ***Figure 144***). So a maximum of 2 CAN channels can be realized with the MultiCAN+ module (For more information and further functions see ***Chapter 19.2***).

All CAN nodes share a common set of 32 message objects. A message object function like a container for a specific CAN message; both transmitting and receiving of CAN messages can be realized. The message objects are organized in double-chained lists, each list is dedicated to a certain CAN node (list 1 is node 0, list 2 is node 1, etc.). After a reset, all message objects are unallocated and therefore assigned to list 0, this list does not belong to a CAN node. During initialization it is possible to allocate the message objects individually to certain CAN node lists. Each allocated message object can be set up with all necessary information like the message ID etc. (see chapter 26.2 and following for further explanations of the CAN module).

In the use case example CAN node 0 will send a CAN message via internal CAN bus to CAN node 1. The transmitting message object (MO) will be MO 0 and the receiving message object will be MO 1. As soon as the CAN frame successfully receives at MO 1 a receive interrupt will occur. The initialization process follows the following order:

1. Load global MuliCAN+ module registers

2. Initialize the CAN nodes
3. Allocate the message objects to the CAN nodes
4. Initialize the message objects
5. Start the CAN nodes
6. Start transmit request for CAN message from node 0 to node 1.
7. Receive message at node 1, Rx interrupt occurs.

Step description to initialize the MultiCAN+ module:

(Line 2)

enable control of the module, in clock control register CLC (***CLC***).

(Line 3)

read back (dummy variable has to be defined). The reading process ensures that the write process from line 2 is done.

(Line 4)

load fractional divider to $f_{CAN} = f_{MCLK}$ (see also 26.3.2 Clock Control (***Fractional Divider***), f_{MCLK} see ***MCR***).

(Line 5)

read back (dummy variable to be defined).

(Line 6)

set clk source to f_{MCLK} in module control register MCR(***MCR***).

Note: The reconfiguration of the clk source must be done by two writes and a certain delay between these. See MCR for more details.

(Line 7)

The setting of protection CCE[6] and INIT[0] activates the initialization and configuration mode for CAN node 0. This is necessary for the upcoming changes in CAN node 0. (see also node configuration register NCRn (***CAN_NCRx (x = 0-1)***))

(Line 8)

This example uses the internal loop-back mode, so this line connects CAN node 0 to the internal CAN Bus. (see also Figure 26-13(***Figure 133***) and node port control register NPCR(***CAN_NPCRx (x = 0-1)***))

(Line 9)

The CAN bit time is subdivided into different segments. (see also 26.3.6.1 Bit Timing Unit(***Bit Timing Unit***)). Assuming f_{CAN} = 100 MHz this line then sets the baudrate to 500 kBaud and the sample point to 80% in the node bit timing register NBTR (***CAN_NBTRx (x = 0-1)***).

(Line 10 - 12)

same as line 7 - 9 but with node 1.

(Line 13)

The allocation of the message objects to certain CAN node lists function via a list command panel. The panel control register PANCTR(***PANCTR***) can only be written if both busy flags are reset. Therefore this while loop waits until the register is ready.

(Line 14)

This line allocates message object 0 to list 1 (belongs to CAN node 0).

(Line 15)

see line 13.

(Line 16)

This line allocates message object 1 to list 2 (belongs to CAN node 0).

(Line 17)

Initialize MO 0 in the message object register MOCTR(***CAN_MOCTRz (z = 0-30)***) as transmit MO by setting bits [27:25]. Set also MSGVAL[21], that's the main switch bit of the MO.

(Line 18)

this line sets the message data length of MO 0 to 8 bytes.(see also message object function control register MOFCR (***CAN_MOFCRn (n = 0-31)***)).

(Line 19)

the message ID of MO 0 gets set to standard message (11 bit length) with a message ID of FF_H in the Message object arbitration register MOAR (***CAN_MOARn (n = 0-31)***).

(Line 20)

Initialize MO 1 in the message object register MOCTR as receive MO by setting bit RXEN[23]. Set also MSGVAL[21], that's the main switch bit of the MO.

(Line 21)

the receive interrupt gets enabled in the message object function control register MOFCR .

(Line 22)

same as Line 19 but for MO 1. The same message ID is necessary to receive CAN messages from the bus with this specific ID.

(Line 23)

the Rx interrupt gets connected to the CAN interrupt output line 1.(see also MOIPR(***CAN_MOIPRn (n = 0-31)***))

(Line 24)

This line enables the Rx interrupt in the service request control register SRC_CANINT1 and sets the interrupt priority to CAN_SR1INT (1...255)

(Line 25)

This function sets the interrupt priority of the receive interrupt.

(Line 26)

The 4 lower data bytes are getting loaded in the MODATAL(***CAN_MODATALn (n = 0-31)***) register. the data itself is here just an example.

(Line 27)

The 4 higher data bytes are getting loaded in the MODATAH(***CAN_MODATAHn (n = 0-31)***) register. (just an data example as well)

(Line 28)

This line resets INIT[0] and CCE[6] bit in the node control register from node 0. The node is now synchronizing itself to the bus.

(Line 29)

same as line 28, but with node 1.

(Line 30)

The NEWDATA bit gets set in the MOCTR register, this should always be done after a write process in the data registers from line 26/27. The transmit request bit TXRQ gets set, this starts the transmission of the CAN message. The RTSEL gets reset to ensure the transmission.

(Line 31)

If the message is received the MOCTR.NEWDAT[19] bit in the receive MO 1 is set. This line just waits for the reception. The occurrence of the Rx interrupt can also be used as a proof that the message arrived.

(Line 32/33)

Access the data bytes without clearing NEWDAT.

Note: The Rx ISR function prototype would be: void CAN1_Rx_irq (void); here could be your ISR code;

Note: Line 1 does not apply for ARM products, therefore this line does not exist.

Initialization of the MultiCAN+ module:

```
// Load global MultiCAN+ registers:
(2)    CAN_CLC = 0x000;                    // enable module control
(3)    dummy = CAN_CLC;                    // read to check the made changes
(4)    CAN_FDR = (1 << 14)| 0x3FF;         // DM=1,STEP=1023

(5)    dummy = CAN_FDR;                    // read to check the made changes
(6)    CAN_MCR = 0x1;                      // CLKSEL=1
//Init CAN nodes 0 and 1:
(7)    CAN_NCR0 = (1 << 6)| 1;             // CCE=1,INIT=1
(8)    CAN_NPCR0 = (1 << 8);               // LBM=1
(9)    CAN_NBTR0 = 0x3EC9;                 // set bit segments
(10)    CAN_NCR1 = (1 << 6)| 1;            // CCE=1,INIT=1
(11)    CAN_NPCR1 = (1 << 8);              // LBM=1
(12)    CAN_NBTR1 = 0x3EC9;                // set bit segments
//Allocate message objects to CAN nodes:
(13)    while(CAN_PANCTR.U & (0x00000100 | 0x00000200));    // busy?
(14)    CAN_PANCTR = (1 << 24)|(0 << 16)| 2;                // MO 0 to list 1
(15)    while(CAN_PANCTR.U & (0x00000100 | 0x00000200));    // busy?
(16)    CAN_PANCTR = (2 << 24)|(1 << 16)| 2;                // MO 1 to list 2
//Init MO_0 (list 1, node 0)
(17)    CAN_MOCTR0 = (1<<27)|(1<<26)|(1<<25)|(1<<21);       // set to Tx
(18)    CAN_MOFCR0 = (8 << 24);                             // DLC=8
(19)    CAN_MOAR0 =  (1 << 30)|(0xFF << 18);                // PRI=01,ID=0xFF
//Init MO_1 (list 2, node 1)
(20)    CAN_MOCTR1 = (1 << 23)|(1 << 21);                   // set to Rx
(21)    CAN_MOFCR1 = (1 << 16);                             // RXIE=1
(22)    CAN_MOAR1 =  (1 << 30)|(0xFF << 18);                // PRI=01, ID=0xFF
(23)    CAN_MOIPR1 = 0x1;                                   // RXINP=1 -> select INT_O1
(24)    SRC_CANINT1 = (1 << 10) | CAN_SRN1INT;              // enable INT_01
(25)    NVIC_SetPriority (CAN_SRN1INT, & CAN1_Rx_irq);
// Load Data, Start CAN nodes
(26)    CAN_MODATAL0 = 0x0D0D0D0D;          // load data, lower 4 Bytes
(27)    CAN_MODATAH0 = 0x0E0E0E0E;          // load data, higher 4 Bytes
(28)    CAN_NCR0 &= ~((1<<6)| 1);           // reset CCE and INIT
(29)    CAN_NCR1 &= ~((1<<6)| 1);           // reset CCE and INIT
// set transmit request to send message
(30)    CAN_MOCTR0 = (1<<24)|(1<<19)|(1<<6);    // TXRQ=1,NEWDAT=1
(31)    while((CAN_MOSTAT1.B.NEWDAT) != 1);     // check if Rx
(32)    readfirstfourdatabytes1=CAN_MODATAL1;   // read_receive
(33)    readnextfourdatabytes1=CAN_MODATAH1;    // read_receive
```

19.5 MulticanCAN+ Kernel Registers

This section describes the kernel registers of the MulticanCAN+ module. All MulticanCAN+ kernel register names described in this section are also referenced in other parts of the IMC300A Reference Manual by the module name prefix “CAN_”.

MulticanCAN+ Kernel Register Overview

The MulticanCAN+ Kernel include three blocks of registers:

- Global Module Registers
- Node Registers, for each CAN node x
- Message Object Registers, for each message object n

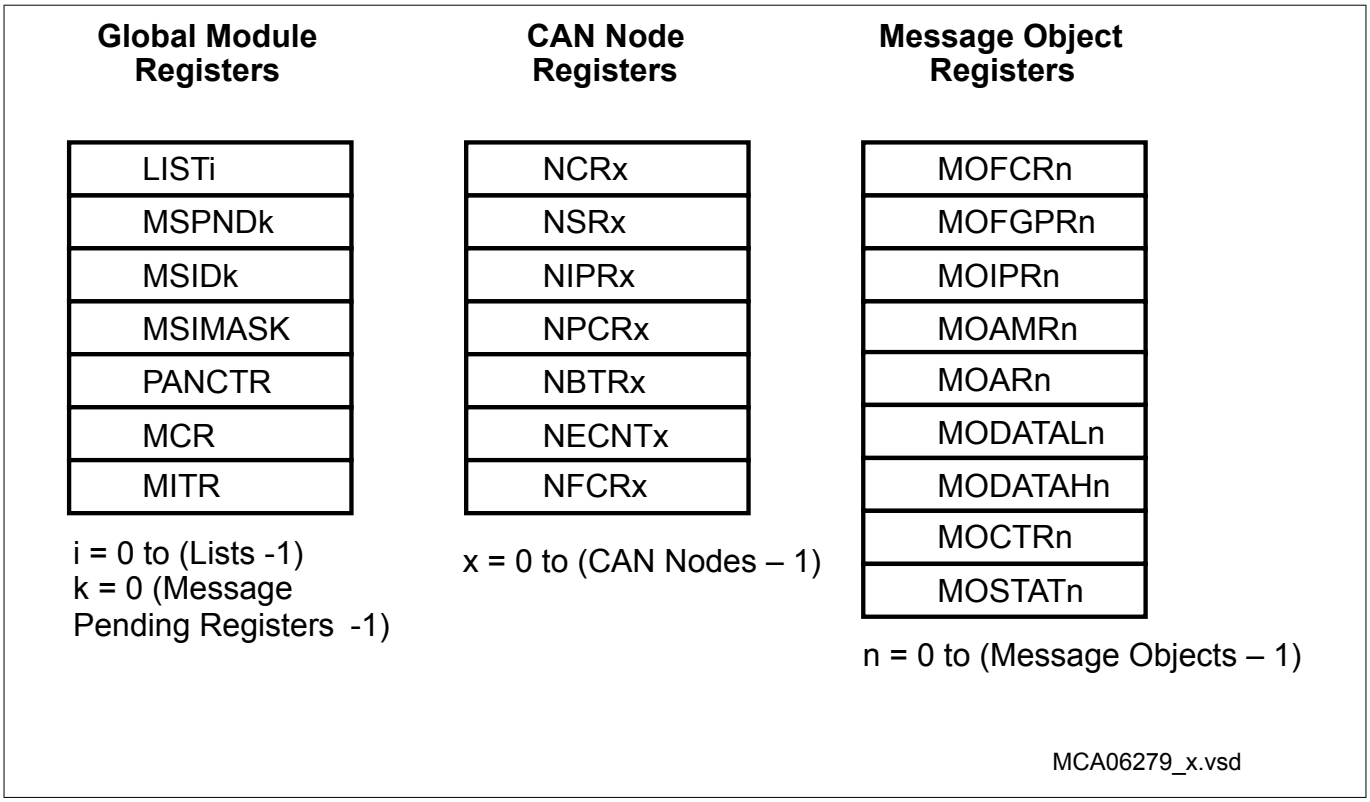


Figure 142 MulticanCAN+ Kernel Registers

The registers of the MulticanCAN+ module kernel are listed below.

Table 231 Registers Address Space - MulticanCAN+ Kernel Registers

Module	Base Address	End Address	Note
CAN	$5004\ 0000_H$	$5004\ 3FFF_H$	-

Table 232 Registers Overview - MulticanCAN+ Kernel Registers

Short Name	Description	Offset Addr[48]	Access Mode[49]		Reset	Description see
			Read	Write		
Global Module Registers						
LISTi	List Register i	$0100_H + i \times 4_H$	U, PV	U, PV	Application Reset	Page 572

48 The absolute register address is calculated as follows: Module Base Address (*Table 231*) + Offset Address (shown in this column) Further, the following ranges for parameters i, k, x, and n are valid: i = 0-15, k = 0-7, x = 0-1, n = 0-31.

49 Accesses to empty addresses: nBE

Table 232 Registers Overview - MulticanCAN+ Kernel Registers (continued)

Short Name	Description	Offset Addr[48]	Access Mode[49]		Reset	Description see
			Read	Write		
MSPNDk	Message Pending Register k	$0140_H + k \times 4_H$	U, PV	U, PV	Application Reset	Page 573
MSIDk	Message Index Register k	$0180_H + k \times 4_H$	U, PV	U, PV	Application Reset	Page 574
MSIMASK	Message Index Mask Register	$01C0_H$	U, PV	U, PV	Application Reset	Page 574
PANCTR	Panel Control Register	$01C4_H$	U, PV	U, PV	Application Reset	Page 567
MCR	Module Control Register	$01C8_H$	U, PV	U, PV	Application Reset	Page 571
MITR	Module Interrupt Trigger Reg.	$01CC_H$	U, PV	U, PV	Application Reset	Page 571
CAN Node Registers						
NCRx	Node x Control Register	$0200_H + x \times 100_H$	U, PV	U, PV	Application Reset	Page 575
NSRx	Node x Status Register	$0204_H + x \times 100_H$	U, PV	U, PV	Application Reset	Page 577
NIPRx	Node x Interrupt Pointer Reg.	$0208_H + x \times 100_H$	U, PV	U, PV	Application Reset	Page 579
NPCRx	Node x Port Control Register	$020C_H + x \times 100_H$	U, PV	U, PV	Application Reset	Page 580
NBTRx	Node x Bit Timing Register	$0210_H + x \times 100_H$	U, PV	U, PV	Application Reset	Page 581
NECNTx	Node x Error Counter Register	$0214_H + x \times 100_H$	U, PV	U, PV	Application Reset	Page 582
NFCRx	Node x Frame Counter Register	$0218_H + x \times 100_H$	U, PV	U, PV	Application Reset	Page 583
Message Object Registers						
MOFCRn	Message Object n Function Control Register	$1000_H + n \times 20_H$	U, PV	U, PV	Application Reset	Page 593
MOFGPRn	Message Object n FIFO/Gateway Pointer Register	$1004_H + n \times 20_H$	U, PV	U, PV	Application Reset	Page 595

48 The absolute register address is calculated as follows: Module Base Address (*Table 231*) + Offset Address (shown in this column) Further, the following ranges for parameters i, k, x, and n are valid: i = 0-15, k = 0-7, x = 0-1, n = 0-31.

49 Accesses to empty addresses: nBE

Table 232 Registers Overview - MulticanCAN+ Kernel Registers (continued)

Short Name	Description	Offset Addr[48]	Access Mode[49]		Reset	Description see
			Read	Write		
MOIPRn	Message Object n Interrupt Pointer Register	$1008_H + n \times 20_H$	U, PV	U, PV	Application Reset	Page 592
MOAMRn	Message Object n Acceptance Mask Register	$100C_H + n \times 20_H$	U, PV	U, PV	Application Reset	Page 596
MODATALn	Message Object n Data Register Low	$1010_H + n \times 20_H$	U, PV	U, PV	Application Reset	Page 599
MODATAHn	Message Object n Data Register High	$1014_H + n \times 20_H$	U, PV	U, PV	Application Reset	Page 599
MOARn	Message Object n Arbitration Register	$1018_H + n \times 20_H$	U, PV	U, PV	Application Reset	Page 597
MOCTRn MOSTATn	Message Object n Control Reg. Message Object n Status Reg.	$101C_H + n \times 20_H$	U, PV	U, PV	Application Reset	Page 586 Page 589

48 The absolute register address is calculated as follows: Module Base Address (Table 231) + Offset Address (shown in this column) Further, the following ranges for parameters i, k, x, and n are valid: i = 0-15, k = 0-7, x = 0-1, n = 0-31.

49 Accesses to empty addresses: nBE

Figure 143

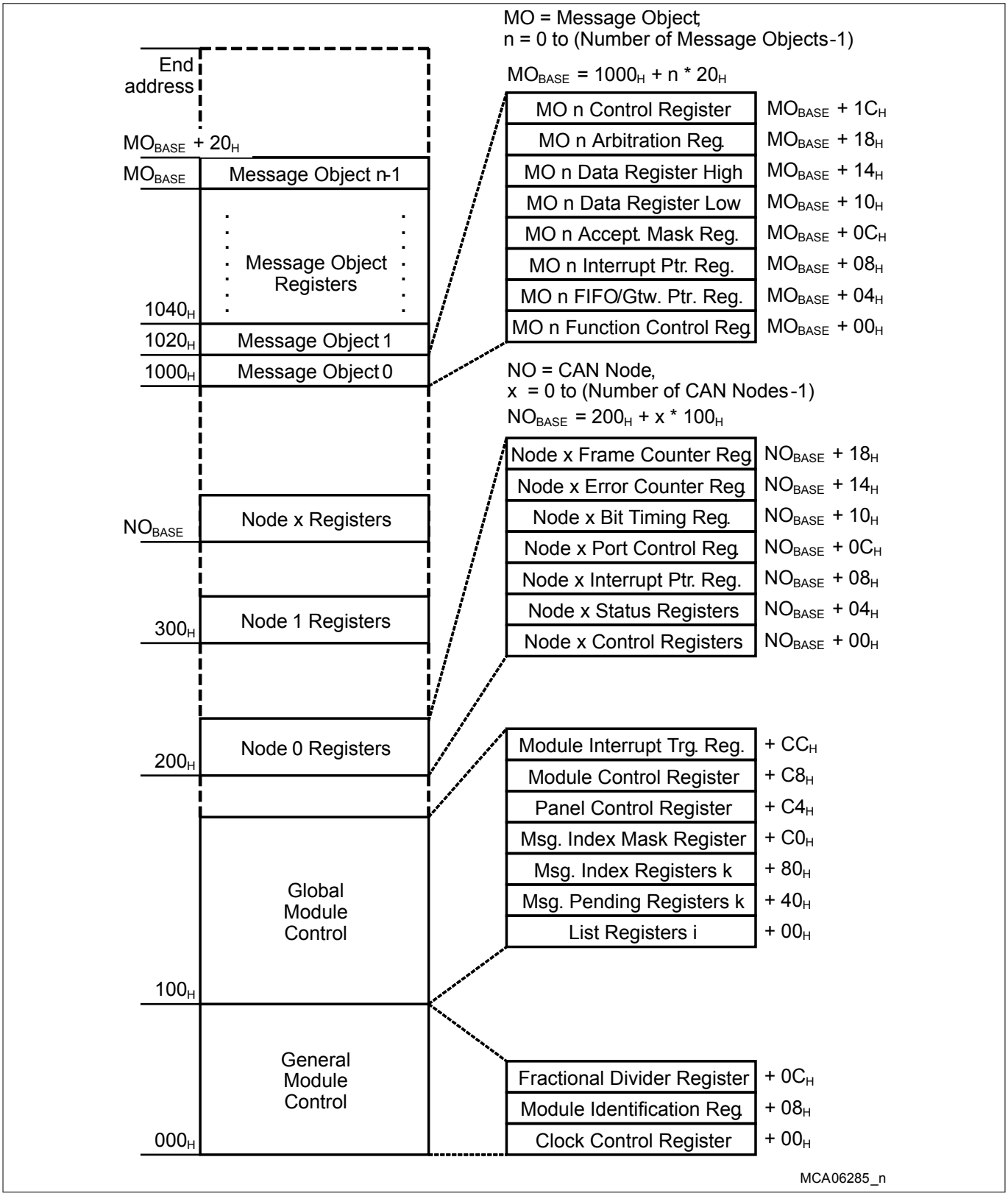


Figure 143 MulticanCAN+ Register Address Map

19.5.1 Global Module Registers

All list operations such as allocation, de-allocation and relocation of message objects within the list structure are performed via the Command Panel. It is not possible to modify the list structure directly by software by writing to the message objects and the LIST registers.

19.5.1.1 Register ID

ID Address: 008_H

Module Identification Register Reset Value: $00B5\ C0XX_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MOD_NUMBER															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOD_TYPE								MOD_REV							
r								r							

Field	Bits	Type	Description
MOD_REV	7:0	r	**Module Revision Number** MOD_REV defines the revision number. The value of a module revision starts with 01_H (first revision).
MOD_TYPE	15:8	r	**Module Type**
MOD_NUMBER	31:16	r	**Module Number Value** This bit field defines the MulticanCAN+ module identification number (=00B5H)

19.5.1.2 Register PANCTR

The Panel Control Register PANCTR is used to start a new command by writing the command arguments and the command code into its bit fields.

PANCTR Address: $1C4_H$

Panel Control Register Reset Value: $0000\ 0301_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PANAR2								PANAR1							
rwh								rwh							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0						RBUSY	BUSY	PANCMD							
r						rh	rh	rwh							

Field	Bits	Type	Description
PANCMD	7:0	rwh	**Panel Command** This bit field is used to start a new command by writing a panel command code into it. At the end of a panel command, the NOP (no operation) command code is automatically written into PANCMD. The coding of PANCMD is defined in ***Table 233***.
BUSY	8	rh	**Panel Busy Flag** 0_B Panel has finished command and is ready to accept a new command. 1_B Panel operation is in progress. Initial list controller initialization must be finalized, when INIT bit is reset.
RBUSY	9	rh	**Result Busy Flag** 0_B No update of PANAR1 and PANAR2 is scheduled by the list controller. 1_B A list command is running (BUSY = 1) that will write results to PANAR1 and PANAR2, but the results are not yet available.
PANAR1	23:16	rwh	**Panel Argument 1** See ***Table 233***.
PANAR2	31:24	rwh	**Panel Argument 2** See ***Table 233***.
0	15:10	r	**Reserved** Read as 0; should be written with 0.

Panel Commands

A panel operation consists of a command code (PANCMD) and up to two panel arguments (PANAR1, PANAR2). Commands that have a return value deliver it to the PANAR1 bit field. Commands that return an error flag deliver it to bit 31 of the Panel Control Register, this means bit 7 of PANAR2.

Table 233 Panel Commands

PANCMD	PANAR2	PANAR1	Command Description
00_H	–	–	**No Operation** Writing 00_H to PANCMD has no effect. No new command is started.

Table 233 Panel Commands (continued)

PANCMD	PANAR2	PANAR1	Command Description
01_H	**Result:** Bit 7: ERR Bit 6-0: undefined	–	**Initialize Lists** Run the initialization sequence to reset the CTRL and LIST fields of all message objects. List registers LIST[7:0] are set to their reset values. This results in the de-allocation of all message objects. The initialization command requires that bits NCRx.INIT and NCRx.CCE are set for all CAN nodes. Bit 7 of PANAR2 (ERR) reports the success of the operation: 0_B Initialization was successful 1_B Not all NCRx.INIT and NCRx.CCE bits are set. Therefore, no initialization is performed. The initialize lists command is automatically performed with each reset of the MulticanCAN+ module, but with the exception that all message object registers are reset, too.
02_H	**Argument:** List Index	**Argument:** Message Object Number	**Static Allocate** Allocate message object to a list. The message object is removed from the list that it currently belongs to, and appended to the end of the list, given by PANAR2. This command is also used to deallocate a message object. In this case, the target list is the list of unallocated elements (PANAR2 = 0).
03_H	**Argument:** List Index **Result:** Bit 7: ERR Bit 6-0: undefined	**Result:** Message Object Number	**Dynamic Allocate** Allocate the first message object of the list of unallocated objects to the selected list. The message object is appended to the end of the list. The message number of the message object is returned in PANAR1. An ERR bit (bit 7 of PANAR2) reports the success of the operation: 0_B Success. 1_B The operation has not been performed because the list of unallocated elements was empty.
04_H	**Argument:** Destination Object Number	**Argument:** Source Object Number	**Static Insert Before** Remove a message object (source object) from the list that it currently belongs to, and insert it before a given destination object into the list structure of the destination object. The source object thus becomes the predecessor of the destination object.

Table 233 Panel Commands (continued)

PANCMD	PANAR2	PANAR1	Command Description
05_H	**Argument:** Destination Object Number **Result:** Bit 7: ERR Bit 6-0: undefined	**Result:** Object Number of inserted object	**Dynamic Insert Before** Insert a new message object before a given destination object. The new object is taken from the list of unallocated elements (the first element is chosen). The number of the new object is delivered as a result to PANAR1. An ERR bit (bit 7 of PANAR2) reports the success of the operation: 0_B Success. 1_B The operation has not been performed because the list of unallocated elements was empty.
06_H	**Argument:** Destination Object Number	**Argument:** Source Object Number	**Static Insert Behind** Remove a message object (source object) from the list that it currently belongs to, and insert it behind a given destination object into the list structure of the destination object. The source object thus becomes the successor of the destination object.
07_H	**Argument:** Destination Object Number **Result:** Bit 7: ERR Bit 6-0: undefined	**Result:** Object Number of inserted object	**Dynamic Insert Behind** Insert a new message object behind a given destination object. The new object is taken from the list of unallocated elements (the first element is chosen). The number of the new object is delivered as result to PANAR1. An ERR bit (bit 7 of PANAR2) reports the success of the operation: 0_B Success. 1_B The operation has not been performed because the list of unallocated elements was empty.
08_H - FF_H	–	–	**Reserved**

19.5.1.3 Register MCR

The Module Control Register MCR contains basic settings that determine the operation of the MulticanCAN+ module.

The write access to the lowest byte of the MCR register is possible only if the CCE bits of all CAN nodes are set (NCRx.CCE bits). The NCRx.INIT bits will be automatically set when the lowest byte of the MCR register is written, independent of the setting of the CCE bits. The INIT bits have to be reset by software in order to activate the CAN nodes.

The reconfiguration of the clock source has to be done by using two writes: first a write of zero to the CLKSEL bit field, and then a second write defining the new clock source. Between the first and the second write a delay of $4 / f_A + 2 / f_{CAN}$ number of cycles must be inserted by software, where f_A is the frequency being switched off with the first write. Exception: in case that f_{MCLK} is selected as the baud rate logic clock (MCR.CLKSEL = 1), no delay cycles between the writes are necessary. In both cases, simply using one write defining the new clock source is not allowed.

Note: If the baud rate logic is supplied from an unstable clock source, or no clock at all, the CAN functionality is not guaranteed.

MCR Address: $1C8_H$

Module Control Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPSEL				0			0	0				CLKSEL			
rw				r			rw	r				rw			

Field	Bits	Type	Description
CLKSEL	3:0	rw	**Baud Rate Logic Clock Select** 0000_B No clock supplied 0001_B f_{MCLK} 0010_B f_{OSC_HP} 0100_B hard wired to 0 1000_B hard wired to 0 $...{}_B$ not allowed
0	8	rw	**Reserved** Read as 0; should be written with 0.
MPSEL	15:12	rw	**Message Pending Selector** Bit field MPSEL makes it possible to select the bit position of the message pending bit after a message reception/transmission by a mixture of the MOIPRn register bit fields RXINP, TXINP, and MPN. Selection details are given in ***Figure 137*** on page ***547***.
0	31:16, 11:9, 7:4	r	**Reserved** Read as 0; should be written with 0.

19.5.1.4 Register MITR

The Interrupt Trigger Register ITR is used to trigger interrupt requests on each interrupt output line by software.

MITR Address: $1CC_H$

Module Interrupt Trigger Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								IT							
r								w							

Field	Bits	Type	Description
IT	7:0	w	**Interrupt Trigger** Writing a 1 to IT[m] (m = 0-7) generates an interrupt request on interrupt output line INT_O[m]. Writing a 0 to IT[m] has no effect. Bit field IT is always read as 0. Multiple interrupt requests can be generated with a single write operation to MITR by writing a 1 to several bit positions of IT. All 16 interrupts are existing, even if the interrupt request unit is not connected.
0	31:8	r	**Reserved** Read as 0; should be written with 0.

19.5.1.5 Register LISTn

List Pointer and List Register

Each CAN node has a list that determines the allocated message objects. Additionally, a list of all unallocated objects is available. Furthermore, general purpose lists are available which are not associated to a CAN node. The List Registers are assigned in the following way:

- LIST0 provides the list of all unallocated objects
- LIST1 provides the list for CAN node 0
- LIST2 provides the list for CAN node 1
- ...
- LIST2 provides the list for CAN node 1

LIST0	Address:	100_H
List Register 0	Reset Value:	$001F\ 1F00_H$
LISTn (n = 1-15)	Address:	100_H+n*4_H
List Register n	Reset Value:	$0100\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0							EMPTY	SIZE							
r							rh	rh							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END								BEGIN							
rh								rh							

Field	Bits	Type	Description
BEGIN	7:0	rh	**List Begin** BEGIN indicates the number of the first message object in list i.
END	15:8	rh	**List End** END indicates the number of the last message object in list i.

(continued)

Field	Bits	Type	Description
SIZE	23:16	rh	**List Size** SIZE indicates the number of elements in the list i. SIZE = number of list elements - 1 SIZE = 0 indicates that list i is empty.
EMPTY	24	rh	**List Empty Indication** 0_B At least one message object is allocated to list i. 1_B No message object is allocated to the list i. List i is empty.
0	31:25	r	**Reserved** Read as 0.

19.5.1.6 Message Notifications

When a message object n generates an interrupt request upon the transmission or reception of a message, then the request is routed to the interrupt output line selected by the bit field MOIPRn.TXINP or MOIPRn.RXINP of the message object n. As there are more message objects than interrupt output lines, an interrupt routine typically processes requests from more than one message object. Therefore, a priority selection mechanism is implemented in the MulticanCAN+ module to select the highest priority object within a collection of message objects.

19.5.1.6.1 Register MSPNDk

The Message Pending Register MSPNDk contains the pending interrupt notification of list i.

MSPNDk (k = 0-7) Address: 140_H+k*4_H

Message Pending Register k Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PND															
rwh															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PND															
rwh															

Field	Bits	Type	Description
PND	31:0	rwh	**Message Pending** When a message interrupt occurs, the message object sets a bit in one of the MSPND register, where the bit position is given by the MPN[4:0] field of the IPR register of the message object. The register selection n is given by the higher bits of MPN. The register bits can be cleared by software (write 0). Writing a 1 has no effect.

19.5.1.6.2 Register MSIDk

Each Message Pending Register has a Message Index Register MSIDk associated with it. The Message Index Register shows the active (set) pending bit with lowest bit position within groups of pending bits.

MSIDk (k = 0-7) Address: 180_H+k*4_H

Message Index Register k Reset Value: $0000\ 0020_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0										**INDEX**					
r										rh					

Field	Bits	Type	Description
INDEX	5:0	rh	**Message Pending Index** The value of INDEX is given by the bit position i of the pending bit of MSPNDk with the following properties: **1.** MSPNDk[i] & IM[i] = 1 **2.** i = 0 or MSPNDk[i-1:0] & IM[i-1:0] = 0 If no bit of MSPNDk satisfies these conditions then INDEX reads 100000_B. Thus INDEX shows the position of the first pending bit of MSPNDk, in which only those bits of MSPNDk that are selected in the Message Index Mask Register are taken into account.
0	31:6	r	**Reserved** Read as 0; should be written with 0.

19.5.1.6.3 Register MSIMASK

The Message Index Mask Register MSIMASK selects individual bits for the calculation of the Message Pending Index. The Message Index Mask Register is used commonly for all Message Pending registers and their associated Message Index registers.

MSIMASK Address: $1C0_H$

Message Index Mask Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IM															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IM															
rw															

Field	Bits	Type	Description
IM	31:0	rw	**Message Index Mask** Only those bits in MSPNDk for which the corresponding Index Mask bits are set contribute to the calculation of the Message Index.

19.5.2 CAN Node Registers

The CAN node registers are built in for each CAN node of the MulticanCAN+ module. They contain information that is directly related to the operation of the CAN nodes and are shared among the nodes.

19.5.2.1 Register CAN_NCRx

The Node Control Register contains basic settings that determine the operation of the CAN node.

CAN_NCRx (x = 0-1) Address: $200_H+x*100_H$

Node x Control Register Reset Value: $0000\ 0041_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0							0	CALM	CCE	TXDIS	CANDIS	ALIE	LECIE	TRIE	INIT
r							rw	rw	rw	rw	rw	rw	rw	rw	rwh

Field	Bits	Type	Description
INIT	0	rwh	**Node Initialization** 0_B Resetting bit INIT enables the participation of the node in the CAN traffic. If the CAN node is in the bus-off state, the ongoing bus-off recovery (which does not depend on the INIT bit) is continued. With the end of the bus-off recovery sequence the CAN node is allowed to take part in the CAN traffic. If the CAN node is not in the bus-off state, a sequence of 11 consecutive recessive bits must be detected before the node is allowed to take part in the CAN traffic. 1_B Setting this bit terminates the participation of this node in the CAN traffic. Any ongoing frame transfer is cancelled and the transmit line goes recessive. If the CAN node is in the bus-off state, then the running bus-off recovery sequence is continued. If the INIT bit is still set after the successful completion of the bus-off recovery sequence, i.e. after detecting 128 sequences of 11 consecutive recessive bits (11 × 1), then the CAN node leaves the bus-off state but remains inactive as long as INIT remains set. Bit INIT is automatically set when the CAN node enters the bus-off state (see page ***535***).

(continued)

Field	Bits	Type	Description
TRIE	1	rw	**Transfer Interrupt Enable** TRIE enables the transfer interrupt of CAN node x. This interrupt is generated after the successful reception or transmission of a CAN frame in node x. 0_B Transfer interrupt is disabled. 1_B Transfer interrupt is enabled. Bit field NIPRx.TRINP selects the interrupt output line which becomes activated at this type of interrupt.
LECIE	2	rw	**LEC Indicated Error Interrupt Enable** LECIE enables the last error code interrupt of CAN node x. This interrupt is generated with each hardware update of bit field NSRx.LEC with LEC > 0 (CAN protocol error). 0_B Last error code interrupt is disabled. 1_B Last error code interrupt is enabled. Bit field NIPRx.LECINP selects the interrupt output line which becomes activated at this type of interrupt.
ALIE	3	rw	**Alert Interrupt Enable** ALIE enables the alert interrupt of CAN node x. This interrupt is generated by any one of the following events: • A change of bit NSRx.BOFF • A change of bit NSRx.EWRN • A List Length Error, which also sets bit NSRx.LLE • A List Object Error, which also sets bit NSRx.LOE 0_B Alert interrupt is disabled. 1_B Alert interrupt is enabled. Bit field NIPRx.ALINP selects the interrupt output line which becomes activated at this type of interrupt.
CANDIS	4	rw	**CAN Disable** Setting this bit disables the CAN node. The CAN node first waits until it is bus-idle or bus-off. Then bit NCRx.INIT is automatically set, and an alert interrupt is generated if bit ALIE is set.
TXDIS	5	rw	**Transmit Disable** Setting this bit disables the transmission on CAN node x as soon as bus-idle is reached. Reception and bits in MOSTATn, e.g. TXRQ, will not be influenced.
CCE	6	rw	**Configuration Change Enable** 0_B The Bit Timing Register, the Port Control Register, and the Error Counter Register may only be read. All attempts to modify them are ignored. 1_B The Bit Timing Register, the Port Control Register, and the Error Counter Register may be read and written.

(continued)

Field	Bits	Type	Description
CALM	7	rw	**CAN Analyzer Mode** If this bit is set, then the CAN node operates in Analyzer Mode. This means that messages may be received, but not transmitted. No acknowledge is sent on the CAN bus upon frame reception. Active-error flags are sent recessive instead of dominant. The transmit line is continuously held at recessive (1) level. Bit CALM can be written only while bit INIT is set.
0	8	rw	**Reserved** Read as 0; should be written with 0.
0	31:9	r	**Reserved** Read as 0; should be written with 0.

19.5.2.2 Register CAN_NSRx

The Node Status Register NSRx reports errors as well as successfully transferred CAN frames.

CAN_NSRx (x = 0-1) Address: $204_H+x*100_H$

Node x Status Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0					0	LOE	LLE	BOFF	EWRN	ALERT	RXOK	TXOK	LEC		
r					rh	rwh	rwh	rh	rh	rwh	rwh	rwh	rwh		

Field	Bits	Type	Description
LEC	2:0	rwh	**Last Error Code** This bit field indicates the type of the last (most recent) CAN error. The encoding of this bit field is described in ***Table 234***.
TXOK	3	rwh	**Message Transmitted Successfully** 0_B No successful transmission since last (most recent) flag reset. 1_B A message has been transmitted successfully (error-free and acknowledged by at least another node). TXOK must be reset by software (write 0). Writing 1 has no effect.
RXOK	4	rwh	**Message Received Successfully** 0_B No successful reception since last (most recent) flag reset. 1_B A message has been received successfully. RXOK must be reset by software (write 0). Writing 1 has no effect.

(continued)

Field	Bits	Type	Description
ALERT	5	rwh	**Alert Warning** The ALERT bit is set upon the occurrence of one of the following events (the same events which also trigger an alert interrupt if ALIE is set): • A change of bit NSRx.BOFF • A change of bit NSRx.EWRN • A List Length Error, which also sets bit NSRx.LLE • A List Object Error, which also sets bit NSRx.LOE ALERT must be reset by software (write 0). Writing 1 has no effect.
EWRN	6	rh	**Error Warning Status** 0_B No warning limit exceeded. 1_B One of the error counters REC or TEC reached the warning limit EWRNLVL.
BOFF	7	rh	**Bus-off Status** 0_B CAN controller is not in the bus-off state. 1_B CAN controller is in the bus-off state.
LLE	8	rwh	**List Length Error** 0_B No List Length Error since last (most recent) flag reset. 1_B A List Length Error has been detected during message acceptance filtering. The number of elements in the list that belongs to this CAN node differs from the list SIZE given in the list termination pointer. LLE must be reset by software (write 0). Writing 1 has no effect.
LOE	9	rwh	**List Object Error** 0_B No List Object Error since last (most recent) flag reset. 1_B A List Object Error has been detected during message acceptance filtering. A message object with wrong LIST index entry in the Message Object Status Register has been detected. LOE must be reset by software (write 0). Writing 1 has no effect.
0	10	rh	**Reserved**
0	31:11	r	**Reserved** Read as 0; should be written with 0.

Encoding of the LEC Bit field

Table 234 Encoding of the LEC Bit field

LEC Value	Signification
000_B	**No Error:** No error was detected for the last (most recent) message on the CAN bus.
001_B	**Stuff Error:** More than 5 equal bits in a sequence have occurred in a part of a received message where this is not allowed.

Table 234 Encoding of the LEC Bit field (continued)

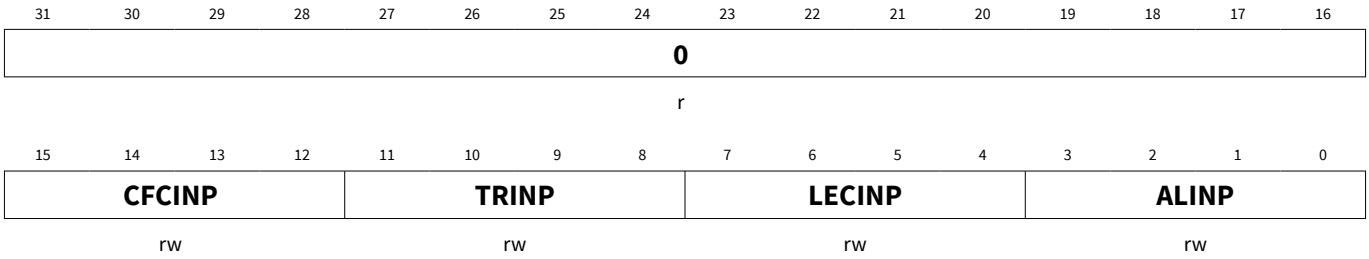
LEC Value	Signification
010_B	**Form Error:** A fixed format part of a received frame has the wrong format.
011_B	**Ack Error:** The transmitted message was not acknowledged by another node.
100_B	**Bit1 Error:** During a message transmission, the CAN node tried to send a recessive level (1) outside the arbitration field and the acknowledge slot, but the monitored bus value was dominant.
101_B	**Bit0 Error:** Two different conditions are signaled by this code: **1.** During transmission of a message (or acknowledge bit, active-error flag, overload flag), the CAN node tried to send a dominant level (0), but the monitored bus value was recessive. **2.** During bus-off recovery, this code is set each time a sequence of 11 recessive bits has been monitored. The CPU may use this code as indication that the bus is not continuously disturbed.
110_B	**CRC Error:** The CRC checksum of the received message was incorrect.
111_B	**CPU write to LEC:** Whenever the CPU writes the value 111 to LEC, it takes the value 111. Whenever the CPU writes another value to LEC, the written LEC value is ignored.

19.5.2.3 Register CAN_NIPRx

The four interrupt pointers in the Node Interrupt Pointer Register NIPRx select one out of the sixteen interrupt outputs individually for each type of CAN node interrupt. See also page ***536*** for more CAN node interrupt details.

CAN_NIPRx (x = 0-1) Address: $208_H+x*100_H$

Node x Interrupt Pointer Register Reset Value: $0000\ 0000_H$



Field	Bits	Type	Description
ALINP	3:0	rw	**Alert Interrupt Node Pointer** ALINP selects the interrupt output line INT_Om (m = 0-7) for an alert interrupt of CAN Node x. 0000_B Interrupt output line INT_O0 is selected. 0001_B Interrupt output line INT_O1 is selected. $\cdots_B$ … 1110_B Interrupt output line INT_O14 is selected. 1111_B Interrupt output line INT_O15 is selected.
LECINP	7:4	rw	**Last Error Code Interrupt Node Pointer** LECINP selects the interrupt output line INT_Om (m = 0-7) for an LEC interrupt of CAN Node x. 0000_B Interrupt output line INT_O0 is selected. 0001_B Interrupt output line INT_O1 is selected. $\cdots_B$ … 1110_B Interrupt output line INT_O14 is selected. 1111_B Interrupt output line INT_O15 is selected.
TRINP	11:8	rw	**Transfer OK Interrupt Node Pointer** TRINP selects the interrupt output line INT_Om (m = 0-7) for a transfer OK interrupt of CAN Node x. 0000_B Interrupt output line INT_O0 is selected. 0001_B Interrupt output line INT_O1 is selected. $\cdots_B$ … 1110_B Interrupt output line INT_O14 is selected. 1111_B Interrupt output line INT_O15 is selected.
CFCINP	15:12	rw	**Frame Counter Interrupt Node Pointer** CFCINP selects the interrupt output line INT_Om (m = 0-7) for a frame counter overflow interrupt of CAN Node x. 0000_B Interrupt output line INT_O0 is selected. 0001_B Interrupt output line INT_O1 is selected. $\cdots_B$ … 1110_B Interrupt output line INT_O14 is selected. 1111_B Interrupt output line INT_O15 is selected.
0	31:16	r	**Reserved** Read as 0; should be written with 0.

19.5.2.4 Register CAN_NPCRx

The Node Port Control Register NPCRx configures the CAN bus transmit/receive ports. NPCRx can be written only if bit NCRx.CCE is set.

CAN_NPCRx (x = 0-1) Address: $20C_H+x*100_H$

Node x Port Control Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0							LBM	0					RXSEL		
r							rw	r					rw		

Field	Bits	Type	Description
RXSEL	2:0	rw	**Receive Select** RXSEL selects one out of 8 possible receive inputs. The CAN receive signal is performed only through the selected input. *Note: In IMC300A, only specific combinations of RXSEL are available (see also **Node Receive Input Selection** on page 605 for description and the page before for RXSEL selections).*
LBM	8	rw	**Loop-Back Mode** 0_B Loop-Back Mode is disabled. 1_B Loop-Back Mode is enabled. This node is connected to an internal (virtual) loop-back CAN bus. All CAN nodes which are in Loop-Back Mode are connected to this virtual CAN bus so that they can communicate with each other internally. The external transmit line is forced recessive in Loop-Back Mode.
0	7:3, 31:9	r	**Reserved** Read as 0; should be written with 0.

19.5.2.5 Register CAN_NBTRx

The Node Bit Timing Register NBTRx contains all parameters to set up the bit timing for the CAN transfer. NBTRx can be written only if bit NCRx.CCE is set.

CAN_NBTRx (x = 0-1) Address: $210_H+x*100_H$

Node x Bit Timing Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIV8	TSEG2			TSEG1				SJW		BRP					
rw	rw			rw				rw		rw					

Field	Bits	Type	Description
BRP	5:0	rw	**Baud Rate Prescaler** The duration of one time quantum is given by (BRP + 1) clock cycles if DIV8 = 0. The duration of one time quantum is given by 8 × (BRP + 1) clock cycles if DIV8 = 1.
SJW	7:6	rw	**(Re) Synchronization Jump Width** (SJW + 1) time quanta are allowed for re-synchronization.
TSEG1	11:8	rw	**Time Segment Before Sample Point** (TSEG1 + 1) time quanta is the user-defined nominal time between the end of the synchronization segment and the sample point. It includes the propagation segment, which takes into account signal propagation delays. The time segment may be lengthened due to re-synchronization. Valid values for TSEG1 are 2 to 15.
TSEG2	14:12	rw	**Time Segment After Sample Point** (TSEG2 + 1) time quanta is the user-defined nominal time between the sample point and the start of the next synchronization segment. It may be shortened due to re-synchronization. Valid values for TSEG2 are 1 to 7.
DIV8	15	rw	**Divide Prescaler Clock by 8** 0_B A time quantum lasts (BRP+1) clock cycles. 1_B A time quantum lasts 8 × (BRP+1) clock cycles.
0	31:16	r	**Reserved** Read as 0; should be written with 0.

19.5.2.6 Register CAN_NECNTx

The Node Error Counter Register NECNTx contains the CAN receive and transmit error counter as well as some additional bits to ease error analysis. NECNTx can be written only if bit NCRx.CCE is set.

CAN_NECNTx (x = 0-1) Address: $214_H+x*100_H$

Node x Error Counter Register Reset Value: $0060\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0						LEINC	LETD	EWRNLVL							
r						rh	rh	rw							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEC								REC							
rwh								rwh							

Field	Bits	Type	Description
REC	7:0	rwh	**Receive Error Counter** Bit field REC contains the value of the receive error counter of CAN node x.
TEC	15:8	rwh	**Transmit Error Counter** Bit field TEC contains the value of the transmit error counter of CAN node x.
EWRNLVL	23:16	rw	**Error Warning Level** Bit field EWRNLVL determines the threshold value (warning level, default 96) to be reached in order to set the corresponding error warning bit EWRN.
LETD	24	rh	**Last Error Transfer Direction** 0_B The last error occurred while the CAN node x was receiver (REC has been incremented). 1_B The last error occurred while the CAN node x was transmitter (TEC has been incremented).
LEINC	25	rh	**Last Error Increment** 0_B The last error led to an error counter increment of 1. 1_B The last error led to an error counter increment of 8.
0	31:26	r	**Reserved** Read as 0; should be written with 0.

19.5.2.7 Register CAN_NFCRx

The Node Frame Counter Register NFCRx contains the actual value of the frame counter as well as control and status bits of the frame counter.

CAN_NFCRx (x = 0-1) Address: $218_H+x*100_H$

Node x Frame Counter Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0								CFCOV	CFCIE	0	CFMOD		CFSEL		
r								rwh	rw	r	rw		rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CFC															
rwh															

Field	Bits	Type	Description
CFC	15:0	rwh	**CAN Frame Counter** In Frame Count Mode (CFMOD = 00_B), this bit field contains the frame count value. In Time Stamp Mode (CFMOD = 01_B), this bit field contains the captured bit time count value, captured with the start of a new frame. In all Bit Timing Analysis Modes[50] (CFMOD = 10_B), CFC always displays the number of f_{CLC} clock cycles (measurement result) minus 1. Example: a CFC value of 34 in measurement mode CFSEL = 000_B means that 35 f_{CLC} clock cycles have been elapsed between the most recent two dominant edges on the receive input. In Error Count Mode (CFMOD = 11_B), this bit field contains the total amount of error frames received or error detected by the node.
CFSEL	18:16	rw	**CAN Frame Count Selection** This bit field selects the function of the frame counter for the chosen frame count mode. **Frame Count Mode** Bit 0 If Bit 0 of CFSEL is set, then CFC is incremented each time a foreign frame (i.e. a frame not matching to a message object) has been received on the CAN bus. Bit 1 If Bit 1 of CFSEL is set, then CFC is incremented each time a frame matching to a message object has been received on the CAN bus. Bit 2 If Bit 2 of CFSEL is set, then CFC is incremented each time a frame has been transmitted successfully by the node. **Time Stamp Mode** The frame counter is incremented (internally) at the beginning of a new bit time. The value is sampled during the SOF bit of a new frame. The sampled value is visible in the CFC field. **Bit Timing Mode** The available bit timing measurement modes are shown in ***Table 235***. If CFCIE is set, then an interrupt on request node x (where x is the CAN node number) is generated with a CFC update. **Error Count Mode** The frame counter is incremented when an error frame is received or an error is detected by the node. (001_B to 110_B) (see ***Table 234*** for ***Encoding of the LEC Bit field***). The configuration is don't care, in this mode.

50 The value of NFCRx.CFC is valid one module cycle later when NFCRx.CFCOV is set.

(continued)

Field	Bits	Type	Description
CFMOD	20:19	rw	**CAN Frame Counter Mode** This bit field determines the operation mode of the frame counter. 00_B Frame Count Mode: The frame counter is incremented upon the reception and transmission of frames. 01_B Time Stamp Mode: The frame counter is used to count bit times. 10_B Bit Timing Mode: The frame counter is used for analysis of the bit timing. 11_B Error Count Mode: The frame counter is used for counting when an error frame is received or an error is detected by the node.
CFCIE	22	rw	**CAN Frame Count Interrupt Enable** CFCIE enables the CAN frame counter overflow interrupt of CAN node x. 0_B CAN frame counter overflow interrupt is disabled. 1_B CAN frame counter overflow interrupt is enabled. Bit field NIPRx.CFCINP selects the interrupt output line that is activated at this type of interrupt.
CFCOV	23	rwh	**CAN Frame Counter Overflow Flag** Flag CFCOV is set upon a frame counter overflow (transition from $FFFF_H$ to 0000_H). In bit timing analysis mode, CFCOV is set upon an update of CFC. An interrupt request is generated if CFCIE = 1. 0_B No overflow has occurred since last flag reset. 1_B An overflow has occurred since last flag reset. CFCOV must be reset by software.
0	21, 31:24	r	**Reserved** Read as 0; should be written with 0.

Bit Timing Analysis Modes

Table 235 Bit Timing Analysis Modes (CFMOD = 10)

CFSEL	Measurement
000_B	Whenever a dominant edge (transition from 1 to 0) is monitored on the receive input, the time (measured in clock cycles) between this edge and the most recent dominant edge is stored in CFC.
001_B	Whenever a recessive edge (transition from 0 to 1) is monitored on the receive input the time (measured in clock cycles) between this edge and the most recent dominant edge is stored in CFC.
010_B	Whenever a dominant edge is received as a result of a transmitted dominant edge, the time (clock cycles) between both edges is stored in CFC.
011_B	Whenever a recessive edge is received as a result of a transmitted recessive edge, the time (clock cycles) between both edges is stored in CFC.
100_B	Whenever a dominant edge that qualifies for synchronization is monitored on the receive input, the time (measured in clock cycles) between this edge and the most recent sample point is stored in CFC.

Table 235 Bit Timing Analysis Modes (CFMOD = 10) (continued)

CFSEL	Measurement
101_B	With each sample point, the time (measured in clock cycles) between the start of the new bit time and the start of the previous bit time is stored in CFC[11:0]. Additional information is written to CFC[15:12] at each sample point: CFC[15]: Transmit value of actual bit time CFC[14]: Receive sample value of actual bit time CFC[13:12]: CAN bus information (see ***Table 236***)
110_B	Reserved, do not use this combination.
111_B	Reserved, do not use this combination.

Table 236 CAN Bus State Information

CFC[13:12]	CAN Bus State
00_B	**NoBit** The CAN bus is idle, performs bit (de-) stuffing or is in one of the following frame segments: SOF, SRR, CRC, delimiters, first 6 EOF bits, IFS.
01_B	**NewBit** This code represents the first bit of a new frame segment. The current bit is the first bit in one of the following frame segments: Bit 10 (MSB) of standard ID (transmit only), RTR, reserved bits, IDE, DLC(MSB), bit 7 (MSB) in each data byte and the first bit of the ID extension.
10_B	**Bit** This code represents a bit inside a frame segment with a length of more than one bit (not the first bit of those frame segments that is indicated by NewBit). The current bit is processed within one of the following frame segments: ID bits (except first bit of standard ID for transmission and first bit of ID extension), DLC (3 LSB) and bits 6-0 in each data byte.
11_B	**Done** The current bit is in one of the following frame segments: Acknowledge slot, last bit of EOF, active/passive-error frame, overload frame. Two or more directly consecutive Done codes signal an Error Frame.

19.5.3 Message Object Registers

19.5.3.1 Register CAN_MOCTRz

The Message Object Control Register MOCTRn and the Message Object Status Register MOSTATn are located at the same address offset within a message object address block (offset address $1C_H$). The MOCTRn is a write-only register that makes it possible to set/reset CAN transfer related control bits through software. Therefore the reset value is written as 0_H, even though the read part of the register has a different reset value.

CAN_MOCTRz (z = 0-30)	Address:	$101C_H+z*20_H$
Message Object z Control Register	Reset Value:	00000000_H
CAN_MOCTR31	Address:	$13FC_H$
Message Object 31 Control Register	Reset Value:	00000000H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0				SETDIR	SETTXEN1	SETTXEN0	SETTXRQ	SETRXEN	SETRTSEL	SETMSGVAL	SETMSGLST	SETNEWDAT	SETRXUPD	SETTXPND	SETRXPND
w				w	w	w	w	w	w	w	w	w	w	w	w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				RESDIR	RESTXEN1	RESTXEN0	RESTXRQ	RESRXEN	RESRTSEL	RESMSGVAL	RESMSGLST	RESNEWDAT	RESRXUPD	RESTXPND	RESRXPND
w				w	w	w	w	w	w	w	w	w	w	w	w

Field	Bits	Type	Description
RESRXPND	0	w	**Reset Receive Pending** This bit controls the reset condition for RXPND (see ***Table 237***).
RESTXPND	1	w	**Reset Transmit Pending** This bit controls the reset condition for TXPND (see ***Table 237***).
RESRXUPD	2	w	**Reset Receive Updating** This bit controls the reset condition for RXUPD (see ***Table 237***).
RESNEWDAT	3	w	**Reset New Data** This bit controls the reset condition for NEWDAT (see ***Table 237***).
RESMSGLST	4	w	**Reset Message Lost** This bit controls the reset condition for MSGLST (see ***Table 237***).
RESMSGVAL	5	w	**Reset Message Valid** This bit controls the reset condition for MSGVAL (see ***Table 237***).
RESRTSEL	6	w	**Reset Receive/Transmit Selected** This bit controls the reset condition for RTSEL (see ***Table 237***).
RESRXEN	7	w	**Reset Receive Enable** This bit controls the reset condition for RXEN (see ***Table 237***).
RESTXRQ	8	w	**Reset Transmit Request** This bit controls the reset condition for TXRQ (see ***Table 237***).
RESTXEN0	9	w	**Reset Transmit Enable 0** This bit controls the reset condition for TXEN0 (see ***Table 237***).
RESTXEN1	10	w	**Reset Transmit Enable 1** This bit controls the reset condition for TXEN1 (see ***Table 237***).
RESDIR	11	w	**Reset Message Direction** This bit controls the reset condition for DIR (see ***Table 237***).
SETRXPND	16	w	**Set Receive Pending** This bit controls the set condition for RXPND (see ***Table 237***).
SETTXPND	17	w	**Set Transmit Pending** This bit controls the set condition for TXPND (see ***Table 237***).
SETRXUPD	18	w	**Set Receive Updating** This bit controls the set condition for RXUPD (see ***Table 237***).

(continued)

Field	Bits	Type	Description
SETNEWDAT	19	w	**Set New Data** This bit controls the set condition for NEWDAT (see ***Table 237***).
SETMSGLST	20	w	**Set Message Lost** This bit controls the set condition for MSGLST (see ***Table 237***).
SETMSGVAL	21	w	**Set Message Valid** This bit controls the set condition for MSGVAL (see ***Table 237***).
SETRTSEL	22	w	**Set Receive/Transmit Selected** This bit controls the set condition for RTSEL (see ***Table 237***).
SETRXEN	23	w	**Set Receive Enable** This bit controls the set condition for RXEN (see ***Table 237***).
SETTXRQ	24	w	**Set Transmit Request** This bit controls the set condition for TXRQ (see ***Table 237***).
SETTXEN0	25	w	**Set Transmit Enable 0** This bit controls the set condition for TXEN0 (see ***Table 237***).
SETTXEN1	26	w	**Set Transmit Enable 1** This bit controls the set condition for TXEN1 (see ***Table 237***).
SETDIR	27	w	**Set Message Direction** This bit controls the set condition for DIR (see ***Table 237***).
0	15:12, 31:28	w	**Reserved** Should be written with 0.

Table 237 Reset/Set Conditions for Bits in Register MOCTRn

RESy Bit[51)]	SETy Bit	Action on Write
Write 0	Write 0	Leave element unchanged
	No write	
No write	Write 0	
Write 1	Write 1	
Write 1	Write 0	Reset element
	No write	
Write 0	Write 1	Set element
No write		

19.5.3.2 Register CAN_MOSTATn

The MOSTATn is a read-only register that indicates message object list status information such as the number of the current message object predecessor and successor message object, as well as the list number to which the message object is assigned.

51 The parameter “y” stands for the second part of the bit name (“RXPND”, “TXPND”, … up to “DIR”).

CAN_MOSTAT0 Address: $101C_H$

Message Object 0 Status Register Reset Value: $0100\ 0000_H$

CAN_MOSTATn (n = 1-30) Address: $(101C_H+n*20_H)$

Message Object n Status Register Reset Value: $((n+1)*01000000_H)+((n-1)*00010000_H)$

CAN_MOSTAT31 Address: $13FC_H$

Message Object 31 Status Register Reset Value: $1F1E0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PNEXT								PPREV							
rh								rh							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LIST				DIR	TXEN1	TXEN0	TXRQ	RXEN	RTSEL	MSGVAL	MSGLST	NEWDAT	RXUPD	TXPND	RXPND
rh				rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
RXPND	0	rh	**Receive Pending** 0_B No CAN message has been received. 1_B A CAN message has been received by the message object n, either directly or via gateway copy action. RXPND is set by hardware and must be reset by software.
TXPND	1	rh	**Transmit Pending** 0_B No CAN message has been transmitted. 1_B A CAN message from message object n has been transmitted successfully over the CAN bus. TXPND is set by hardware and must be reset by software.
RXUPD	2	rh	**Receive Updating** 0_B No receive update ongoing. 1_B Message identifier, DLC, and data of the message object are currently updated.
NEWDAT	3	rh	**New Data** 0_B No update of the message object n since last flag reset. 1_B Message object n has been updated. NEWDAT is set by hardware after a received CAN frame has been stored in message object n. NEWDAT is cleared by hardware when a CAN transmission of message object n has been started. NEWDAT should be set by software after the new transmit data has been stored in message object n to prevent the automatic reset of TXRQ at the end of an ongoing transmission.
MSGLST	4	rh	**Message Lost** 0_B No CAN message is lost. 1_B A CAN message is lost because NEWDAT has become set again when it has already been set.

(continued)

Field	Bits	Type	Description
MSGVAL	5	rh	**Message Valid** 0_B Message object n is not valid. 1_B Message object n is valid. Only a valid message object takes part in CAN transfers.
RTSEL	6	rh	**Receive/Transmit Selected** 0_B Message object n is not selected for receive or transmit operation. 1_B Message object n is selected for receive or transmit operation. **Frame Reception** RTSEL is set by hardware when message object n has been identified for storage of a CAN frame that is currently received. Before a received frame becomes finally stored in message object n, a check is performed to determine if RTSEL is set. Thus the CPU can suppress a scheduled frame delivery to this message object n by clearing RTSEL by software. **Frame Transmission** RTSEL is set by hardware when message object n has been identified to be transmitted next. A check is performed to determine if RTSEL is still set before message object n is actually set up for transmission and bit NEWDAT is cleared. It is also checked that RTSEL is still set before its message object n is verified due to the successful transmission of a frame. RTSEL needs to be checked only when the context of message object n changes, and a conflict with an ongoing frame transfer shall be avoided. In all other cases, RTSEL can be ignored. RTSEL has no impact on message acceptance filtering. RTSEL is not cleared by hardware.
RXEN	7	rh	**Receive Enable** 0_B Message object n is not enabled for frame reception. 1_B Message object n is enabled for frame reception. RXEN is evaluated for receive acceptance filtering only.
TXRQ	8	rh	**Transmit Request** 0_B No transmission of message object n is requested. 1_B Transmission of message object n on the CAN bus is requested. The transmit request becomes valid only if TXRQ, TXEN0, TXEN1 and MSGVAL are set. TXRQ is set by hardware if a matching Remote Frame has been received correctly. TXRQ is reset by hardware if message object n has been transmitted successfully and NEWDAT is not set again by software.

(continued)

Field	Bits	Type	Description
TXEN0	9	rh	**Transmit Enable 0** 0_B Message object n is not enabled for frame transmission. 1_B Message object n is enabled for frame transmission. Message object n can be transmitted only if both bits, TXEN0 and TXEN1, are set. The user may clear TXEN0 in order to inhibit the transmission of a message that is currently updated, or to disable automatic response of Remote Frames.
TXEN1	10	rh	**Transmit Enable 1** 0_B Message object n is not enabled for frame transmission. 1_B Message object n is enabled for frame transmission. Message object n can be transmitted only if both bits, TXEN0 and TXEN1, are set. TXEN1 is used by the MulticanCAN+ module for selecting the active message object in the Transmit FIFOs.
DIR	11	rh	**Message Direction** 0_B Receive Object selected: With TXRQ = 1, a Remote Frame with the identifier of message object n is scheduled for transmission. On reception of a Data Frame with matching identifier, the message is stored in message object n. 1_B Transmit Object selected: If TXRQ = 1, message object n is scheduled for transmission of a Data Frame. On reception of a Remote Frame with matching identifier, bit TXRQ is set.
LIST	15:12	rh	**List Allocation** LIST indicates the number of the message list to which message object n is allocated. LIST is updated by hardware when the list allocation of the object is modified by a panel command.
PPREV	23:16	rh	**Pointer to Previous Message Object** PPREV holds the message object number of the previous message object in a message list structure.
PNEXT	31:24	rh	**Pointer to Next Message Object** PNEXT holds the message object number of the next message object in a message list structure.

Table 238 MOSTATn Reset Values

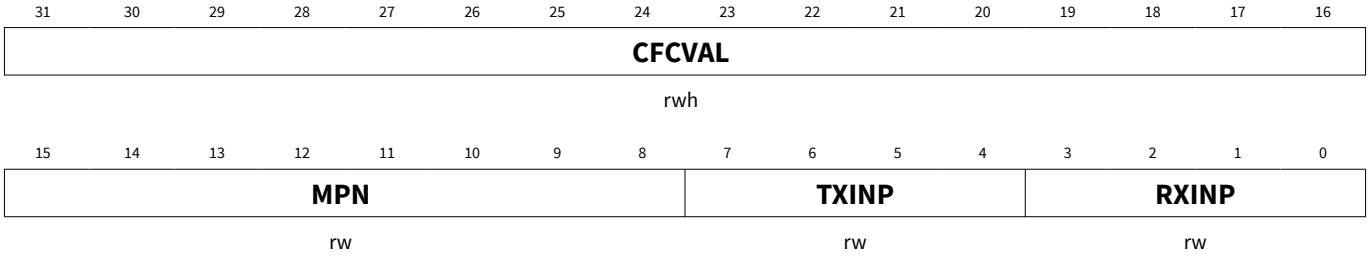
Message Object	PNEXT	PPREV	Reset Value
0	1	0	$0100\ 0000_H$
1	2	0	$0200\ 0000_H$
2	3	1	$0301\ 0000_H$
3	4	2	$0402\ 0000_H$
…	…	…	…
31	31	30	$1F1E\ 0000_H$

19.5.3.3 Register CAN_MOIPRn

The Message Object Interrupt Pointer Register MOIPRn holds the message interrupt pointers, the message pending number, and the frame counter value of message object n.

CAN_MOIPRn (n = 0-31) Address: 1008_H+n*20_H

Message Object n Interrupt Pointer Register Reset Value: $0000\ 0000_H$



Field	Bits	Type	Description
RXINP	3:0	rw	**Receive Interrupt Node Pointer** RXINP selects the interrupt output line INT_Om (m = 0-7) for a receive interrupt event of message object n. RXINP can also be taken for message pending bit selection (see page ***547***). 0000_B Interrupt output line INT_O0 is selected. 0001_B Interrupt output line INT_O1 is selected. …B … 1110_B Interrupt output line INT_O14 is selected. 1111_B Interrupt output line INT_O15 is selected.
TXINP	7:4	rw	**Transmit Interrupt Node Pointer** TXINP selects the interrupt output line INT_Om (m = 0-7) for a transmit interrupt event of message object n. TXINP can also be taken for message pending bit selection (see page ***547***). 0000_B Interrupt output line INT_O0 is selected. 0001_B Interrupt output line INT_O1 is selected. …B … 1110_B Interrupt output line INT_O14 is selected. 1111_B Interrupt output line INT_O15 is selected.
MPN	15:8	rw	**Message Pending Number** This bit field selects the bit position of the bit in the Message Pending Register that is set upon a message object n receive/ transmit interrupt.
CFCVAL	31:16	rwh	**CAN Frame Counter Value** When a message is stored in message object n or message object n has been successfully transmitted, the CAN frame counter value NFCRx.CFC is then copied to CFCVAL.

19.5.3.4 Register CAN_MOFCRn

The Message Object Function Control Register MOFCRn contains bits that select and configure the function of the message object. It also holds the CAN data length code.

CAN_MOFCRn (n = 0-31) Address: 1000_H+n*20_H

Message Object n Function Control Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0				DLC				STT	SDT	RMM	FRREN	0	OVIE	TXIE	RXIE
rw				rwh				rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				DATC	DLCC	IDC	GDFS	0	0	0	0	MMC			
rw				rw	rw	rw	rw	rw	rw	rw	rw	rw			

Field	Bits	Type	Description
MMC	3:0	rw	**Message Mode Control** MMC controls the message mode of message object n. 0000_B Standard Message Object 0001_B Receive FIFO Base Object 0010_B Transmit FIFO Base Object 0011_B Transmit FIFO Slave Object 0100_B Gateway Source Object 0101_B Do not use 0110_B Do not use $...B$ ... 1111_B Do not use
0	4	rw	**Reserved** Shall be written with 0_H.
0	5	rw	**Reserved** Shall be written with 0_H.
0	6	rw	**Reserved** Shall be written with 0_H. Setting a different value, will disable transmissions.
GDFS	8	rw	**Gateway Data Frame Send** 0_B TXRQ is unchanged in the destination object. 1_B TXRQ is set in the gateway destination object after the internal transfer from the gateway source to the gateway destination object. Applicable only to a gateway source object; ignored in other nodes.
IDC	9	rw	**Identifier Copy** 0_B The identifier of the gateway source object is not copied. 1_B The identifier of the gateway source object (after storing the received frame in the source) is copied to the gateway destination object. Applicable only to a gateway source object; ignored in other nodes.

(continued)

Field	Bits	Type	Description
DLCC	10	rw	**Data Length Code Copy** 0_B Data length code is not copied. 1_B Data length code of the gateway source object (after storing the received frame in the source) is copied to the gateway destination object. Applicable only to a gateway source object; ignored in other nodes.
DATC	11	rw	**Data Copy** 0_B Data fields are not copied. 1_B Data fields in registers MODATALn and MODATAHn of the gateway source object (after storing the received frame in the source) are copied to the gateway destination. Applicable only to a gateway source object; ignored in other nodes.
RXIE	16	rw	**Receive Interrupt Enable** RXIE enables the message receive interrupt of message object n. This interrupt is generated after reception of a CAN message (independent of whether the CAN message is received directly or indirectly via a gateway action). 0_B Message receive interrupt is disabled. 1_B Message receive interrupt is enabled. Bit field MOIPRn.RXINP selects the interrupt output line which becomes activated at this type of interrupt.
TXIE	17	rw	**Transmit Interrupt Enable** TXIE enables the message transmit interrupt of message object n. This interrupt is generated after the transmission of a CAN message. 0_B Message transmit interrupt is disabled. 1_B Message transmit interrupt is enabled. Bit field MOIPRn.TXINP selects the interrupt output line which becomes activated at this type of interrupt.
OVIE	18	rw	**Overflow Interrupt Enable** OVIE enables the FIFO full interrupt of message object n. This interrupt is generated when the pointer to the current message object (CUR) reaches the value of SEL in the FIFO/Gateway Pointer Register. 0_B FIFO full interrupt is disabled. 1_B FIFO full interrupt is enabled. If message object n is a Receive FIFO base object, bit field MOIPRn.TXINP selects the interrupt output line which becomes activated at this type of interrupt. If message object n is a Transmit FIFO base object, bit field MOIPRn.RXINP selects the interrupt output line which becomes activated at this type of interrupt. For all other message object modes, bit OVIE has no effect.

(continued)

Field	Bits	Type	Description
FRREN	20	rw	**Foreign Remote Request Enable** Specifies whether the TXRQ bit is set in message object n or in a foreign message object referenced by the pointer CUR. 0_B TXRQ of message object n is set on reception of a matching Remote Frame. 1_B TXRQ of the message object referenced by the pointer CUR is set on reception of a matching Remote Frame.
RMM	21	rw	**Transmit Object Remote Monitoring** 0_B Remote monitoring is disabled: Identifier, IDE bit, and DLC of message object n remain unchanged upon the reception of a matching Remote Frame. 1_B Remote monitoring is enabled: Identifier, IDE bit, and DLC of a matching Remote Frame are copied to transmit object n in order to monitor incoming Remote Frames. Bit RMM applies only to transmit objects and has no effect on receive objects.
SDT	22	rw	**Single Data Transfer** If SDT = 1 and message object n is not a FIFO base object, then MSGVAL is reset when this object has taken part in a successful data transfer (receive or transmit). If SDT = 1 and message object n is a FIFO base object, then MSGVAL is reset when the pointer to the current object CUR reaches the value of SEL in the FIFO/Gateway Pointer Register. With SDT = 0, bit MSGVAL is not affected.
STT	23	rw	**Single Transmit Trial** If this bit is set, then TXRQ is cleared on transmission start of message object n. Thus, no transmission retry is performed in case of transmission failure.
DLC	27:24	rwh	**Data Length Code** Bit field determines the number of data bytes for message object n. A value of DLC > 8 results in a data length of 8 data bytes. If a frame with DLC > 8 is received, the received value is stored in the message object.
0	5, 7, 15:12, 19, 31:28	rw	**Reserved** Read as 0 after reset; value last written is read back; should be written with 0.

19.5.3.5 Register CAN_MOFGPRn

The Message Object FIFO/Gateway Pointer register MOFGPRn contains a set of message object link pointers that are used for FIFO and gateway operations.

CAN_MOFGPRn (n = 0-31) Address: 1004_H+n*20_H

Message Object n FIFO/Gateway Pointer Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL								CUR							
rw								rwh							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOP								BOT							
rw								rw							

Field	Bits	Type	Description
BOT	7:0	rw	**Bottom Pointer** Bit field BOT points to the first element in a FIFO structure.
TOP	15:8	rw	**Top Pointer** Bit field TOP points to the last element in a FIFO structure.
CUR	23:16	rwh	**Current Object Pointer** Bit field CUR points to the actual target object within a FIFO/ Gateway structure. After a FIFO/gateway operation CUR is updated with the message number of the next message object in the list structure (given by PNEXT of the Message Object Status Register) until it reaches the FIFO top element (given by TOP) when it is reset to the bottom element (given by BOT).
SEL	31:24	rw	**Object Select Pointer** Bit field SEL is the second (software) pointer to complement the hardware pointer CUR in the FIFO structure. SEL is used for monitoring purposes (FIFO interrupt generation).

19.5.3.6 Register CAN_MOAMRn

Message Object n Acceptance Mask Register MOAMRn contains the mask bits for the acceptance filtering of the message object n.

CAN_MOAMRn (n = 0-31) Address: $100C_H+n*20_H$

Message Object n Acceptance Mask Register Reset Value: $3FFF\ FFFF_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0		MIDE	AM												
rw		rw	rw												

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AM															
rw															

Field	Bits	Type	Description
AM	28:0	rw	**Acceptance Mask for Message Identifier** Bit field AM is the 29-bit mask for filtering incoming messages with standard identifiers (AM[28:18]) or extended identifiers (AM[28:0]). For standard identifiers, bits AM[17:0] are “don’t care”.
MIDE	29	rw	**Acceptance Mask Bit for Message IDE Bit** 0_B Message object n accepts the reception of both, standard and extended frames. 1_B Message object n receives frames only with matching IDE bit.
0	31:30	rw	**Reserved** Read as 0 after reset; value last written is read back; should be written with 0.

19.5.3.7 Register CAN_MOARn

Message Object n Arbitration Register MOARn contains the CAN identifier of the message object.

CAN_MOARn (n = 0-31) Address: 1018_H+n*20_H

Message Object n Arbitration Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRI		**IDE**	**ID**												
rw		rwh	rwh												

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID															
rwh															

Field	Bits	Type	Description
ID	28:0	rwh	**CAN Identifier of Message Object n** Identifier of a standard message (ID[28:18]) or an extended message (ID[28:0]). For standard identifiers, bits ID[17:0] are “don’t care”.
IDE	29	rwh	**Identifier Extension Bit of Message Object n** 0_B Message object n handles standard frames with 11-bit identifier. 1_B Message object n handles extended frames with 29-bit identifier.

(continued)

Field	Bits	Type	Description
PRI	31:30	rw	**Priority Class** PRI assigns one of the four priority classes 0, 1, 2, 3 to message object n. A lower PRI number defines a higher priority. Message objects with lower PRI value always win acceptance filtering for frame reception and transmission over message objects with higher PRI value. Acceptance filtering based on identifier/mask and list position is performed only between message objects of the same priority class. PRI also determines the acceptance filtering method for transmission: 00_B Reserved. 01_B Transmit acceptance filtering is based on the list order. This means that message object n is considered for transmission only if there is no other message object with valid transmit request (MSGVAL & TXEN0 & TXEN1 = 1) somewhere before this object in the list. 10_B Transmit acceptance filtering is based on the CAN identifier. This means, message object n is considered for transmission only if there is no other message object with higher priority identifier + IDE + DIR (with respect to CAN arbitration rules) somewhere in the list (see ***Table 239***). 11_B Transmit acceptance filtering is based on the list order (as PRI = 01_B).

Table 239 Transmit Priority of Msg. Objects Based on CAN Arbitration Rules

Settings of Arbitrarily Chosen Message Objects A and B, (A has higher transmit priority than B)	Comment
A.MOAR[28:18] < B.MOAR[28:18] (11-bit standard identifier of A less than 11-bit standard identifier of B)	Messages with lower standard identifier have higher priority than messages with higher standard identifier. MOAR[28] is the most significant bit (MSB) of the standard identifier. MOAR[18] is the least significant bit of the standard identifier.
A.MOAR[28:18] = B.MOAR[28:18] A.MOAR.IDE = 0 (send Standard Frame) B.MOAR.IDE = 1 (send Extended Frame)	Standard Frames have higher transmit priority than Extended Frames with equal standard identifier.
A.MOAR[28:18] = B.MOAR[28:18] A.MOAR.IDE = B.MOAR.IDE = 0 A.MOSTAT.DIR = 1 (send Data Frame) B.MOSTAT.DIR = 0 (send Remote Fame)	Standard Data Frames have higher transmit priority than standard Remote Frames with equal identifier.
A.MOAR[28:0] = B.MOAR[28:0] A.MOAR.IDE = B.MOAR.IDE = 1 A.MOSTAT.DIR = 1 (send Data Frame) B.MOSTAT.DIR = 0 (send Remote Frame)	Extended Data Frames have higher transmit priority than Extended Remote Frames with equal identifier.

Table 239 Transmit Priority of Msg. Objects Based on CAN Arbitration Rules (continued)

Settings of Arbitrarily Chosen Message Objects A and B, (A has higher transmit priority than B)	Comment
A.MOAR[28:0] < B.MOAR[28:0] A.MOAR.IDE = B.MOAR.IDE = 1 (29-bit identifier)	Extended Frames with lower identifier have higher transmit priority than Extended Frames with higher identifier. MOAR[28] is the most significant bit (MSB) of the overall identifier (standard identifier MOAR[28:18] and identifier extension MOAR[17:0]). MOAR[0] is the least significant bit (LSB) of the overall identifier.

19.5.3.8 Register CAN_MODATALn

Message Object n Data Register Low MODATALn contains the lowest four data bytes of message object n. Unused data bytes are set to zero upon reception and ignored for transmission.

CAN_MODATALn (n = 0-31) Address: 1010_H+n*20_H

Message Object n Data Register Low Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DB3								DB2							
rwh								rwh							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DB1								DB0							
rwh								rwh							

Field	Bits	Type	Description
DB0	7:0	rwh	**Data Byte 0 of Message Object n**
DB1	15:8	rwh	**Data Byte 1 of Message Object n**
DB2	23:16	rwh	**Data Byte 2 of Message Object n**
DB3	31:24	rwh	**Data Byte 3 of Message Object n**

19.5.3.9 Register CAN_MODATAHn

Message Object n Data Register High MODATAH contains the highest four data bytes of message object n. Unused data bytes are set to zero upon reception and ignored for transmission.

CAN_MODATAHn (n = 0-31) Address: 1014_H+n*20_H

Message Object n Data Register High Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DB7								**DB6**							
rwh								rwh							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DB5								**DB4**							
rwh								rwh							

Field	Bits	Type	Description
DB4	7:0	rwh	**Data Byte 4 of Message Object n**
DB5	15:8	rwh	**Data Byte 5 of Message Object n**
DB6	23:16	rwh	**Data Byte 6 of Message Object n**
DB7	31:24	rwh	**Data Byte 7 of Message Object n**

19.6 MulticanCAN+ Module Implementation

This section describes CAN module interfaces with the clock control, port connections, interrupt control, and address decoding.

19.6.1 Interfaces of the MulticanCAN+ Module

Figure 144 shows the IMC300A specific implementation details and interconnections of the MulticanCAN+ module. The I/O lines of the MulticanCAN+ module (two I/O lines of each CAN node) are connected to the Ports listed in ***Table 241*** . The MulticanCAN+ module is also supplied by clock control, interrupt control, and address decoding logic. MulticanCAN+ interrupts can be directed to the CPU, CCU4 modules which are able to trigger CCU4, CPU operations.

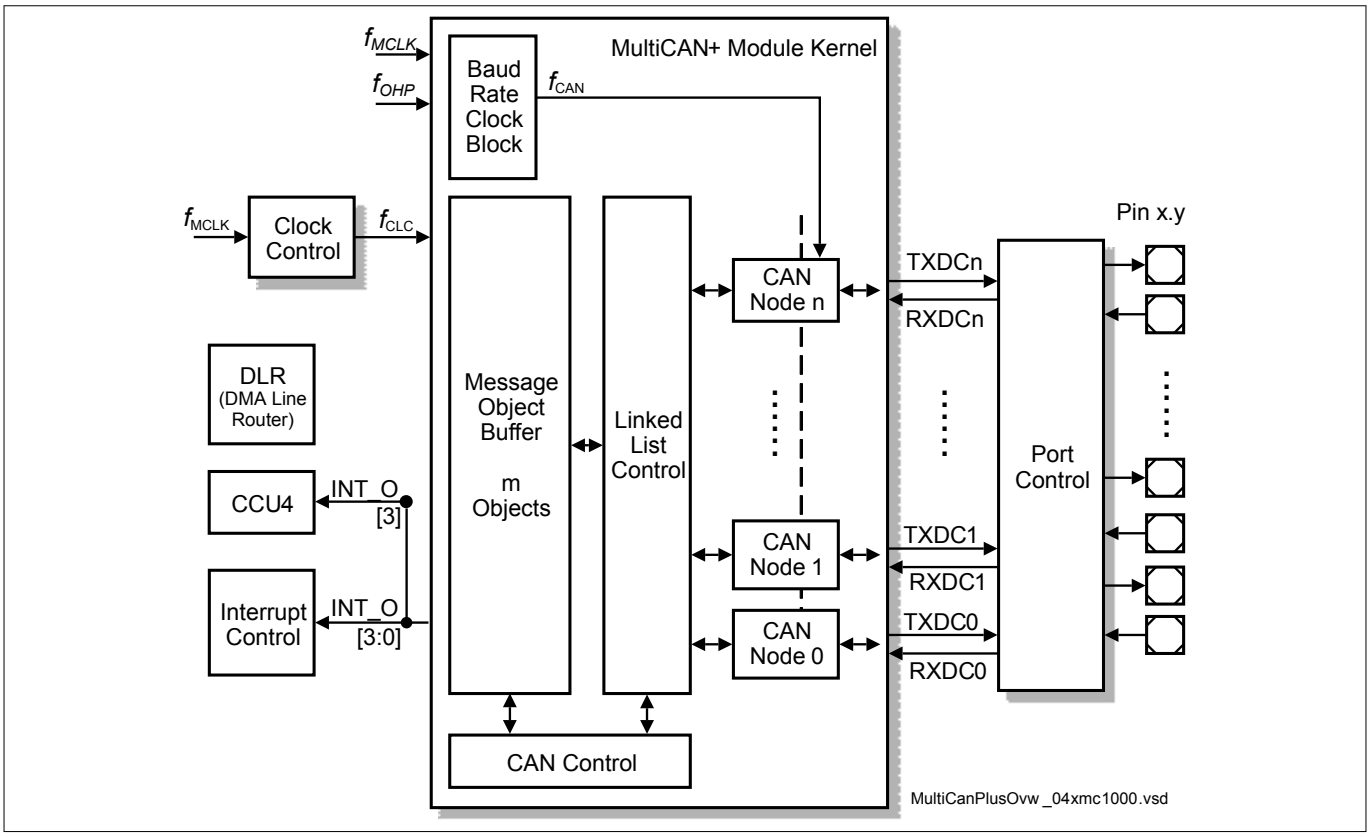


Figure 144 MultiCAN+ Module Implementation and Interconnections with n := 1 and m := 32

19.6.2 MulticanCAN+ Module External Registers

The registers listed in ***Figure 145*** are not included in the MulticanCAN+ module kernel, some registers must be programmed for proper operation of the MulticanCAN+ module.

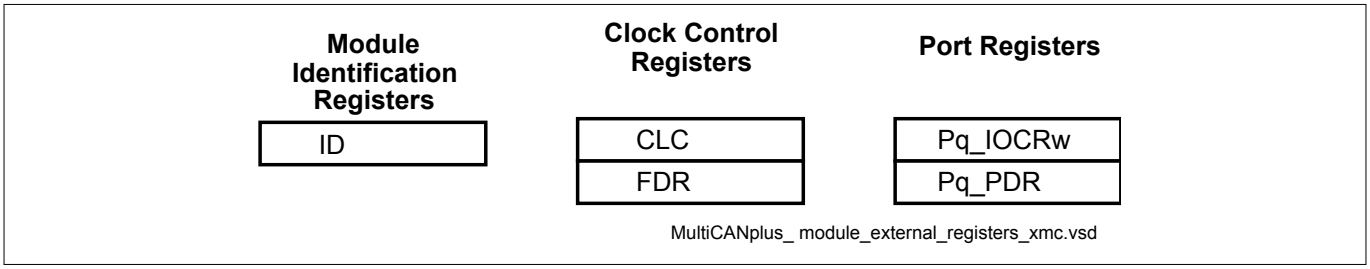


Figure 145 CAN Implementation-specific Special Function Registers

Table 240 MulticanCAN+ Module External Registers

Short Name	Description	Offset Addr	Access Mode		Reset Class	Description see
			Read	Write		
Module Identification Registers						
ID	Module Identification Register	008_H	U, PV	nBE	Application Reset	Page ***567***
Clock Control Registers						
CLC	Clock Control Register	000_H	U, PV	PV,	Application Reset	Page ***603***
FDR	Fractional Divider Register	$00C_H$	U, PV	PV,	Application Reset	Page ***604***

19.6.3 Module Clock Generation

This chapter describes the way the module get's its clock.

19.6.3.1 Clock Selection

The bit timing machine and the rest of the MulticanCAN+ module are separate frequency domains and can be driven by separate independent frequencies. The bit timing unit can be driven by the AHB bus clock or with the direct oscillator clock, and the rest of the chip is driven only by the AHB bus clock.

The purpose of supplying the bit timing unit with a direct oscillator clock is to avoid the clock jitter added by the PLL, necessary when the chip is driven by a low cost ceramic resonator instead of by high precision quartz crystal.

Selecting the clock source for the bit timing unit is done by programming the bit-field MCR.CLKSEL.

Enabling and disabling the clock of the module by using CLC.DISR affects always both frequency domains, so that when f_{CLC} is switched off, f_A is also switched off.

19.6.3.2 Fractional Divider

As shown in ***Figure 146***, the clock signals for the MulticanCAN+ module are generated and controlled by a clock control unit. This clock generation unit is responsible for the enable/disable control, the clock frequency adjustment, and the debug clock control. This unit includes two registers:

- CAN_CLC: generation of the module control clock f_{CLC}
- CAN_FDR: frequency control of the module timer clock f_{CAN}

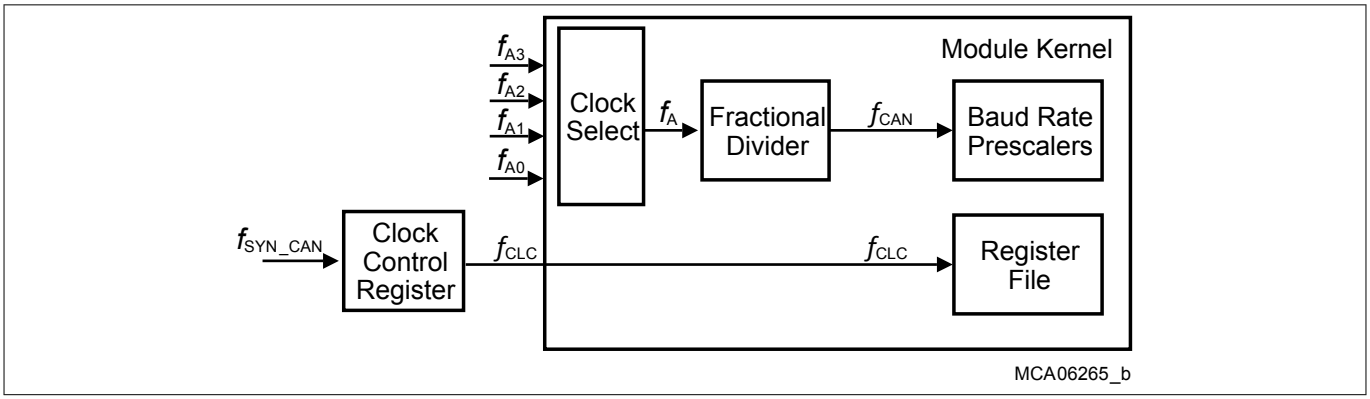


Figure 146 MulticanCAN+ Module Clock Generation

The f_{SYN_CAN} is identical to f_{MCLK}.

The module control clock f_{CLC} is used inside the MulticanCAN+ module for control purposes such as clocking of control logic and register operations. The frequency of f_{CLC} is identical to the system clock frequency f_{MCLK}. The clock control register CAN_CLC makes it possible to enable/disable f_{CLC} under certain conditions.

The module timer clock f_{CAN} is used inside the MulticanCAN+ module as input clock for all timing relevant operations (e.g. bit timing). The settings in the CAN_FDR register determine the frequency of the module timer clock f_{CAN} according the following two formulas:

$$f_{CAN} = f_A \times \frac{1}{n} \text{ with n = 1024 - CAN_FDR.STEP}$$

Equation 25

$$f_{CAN} = f_A \times \frac{n}{1024} \text{ with n = 0-1023}$$

Equation 26

Equation 25 applies to normal divider mode (CAN_FDR.DM = 01_B) of the fractional divider. ***Equation 26*** applies to fractional divider mode (CAN_FDR.DM = 10_B).

Note: The CAN module is disabled after reset. In general, after reset, the module control clock f_{CLC} must be switched on (writing to register CAN_CLC) before the frequency of the module timer clock f_{CAN} is defined (writing to register CAN_FDR).

19.6.3.2.1 Register CLC

The Clock Control Register CLC allows the programmer to adapt the functionality and power consumption of the module to the requirements of the application. The description below shows the clock control register functionality which is implemented in the BPI for the module. CLC controls the f_{CAN} module clock signal.

CLC Address: 000_H

CAN Clock Control Register Reset Value: $0000\ 0003_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0												EDIS	0	DISS	DISR
r												rw	r	rh	rw

Field	Bits	Type	Description
DISR	0	rw	**Module Disable Request Bit** Used for enable/disable control of the module. Note that no register access is possible to any register while module is disabled.
DISS	1	rh	**Module Disable Status Bit** Bit indicates the current status of the module.
EDIS	3	rw	**Sleep Mode Enable Control** Used to control module's sleep mode.
0	31:4, 2	r	**Reserved** Read as 0; should be written with 0.

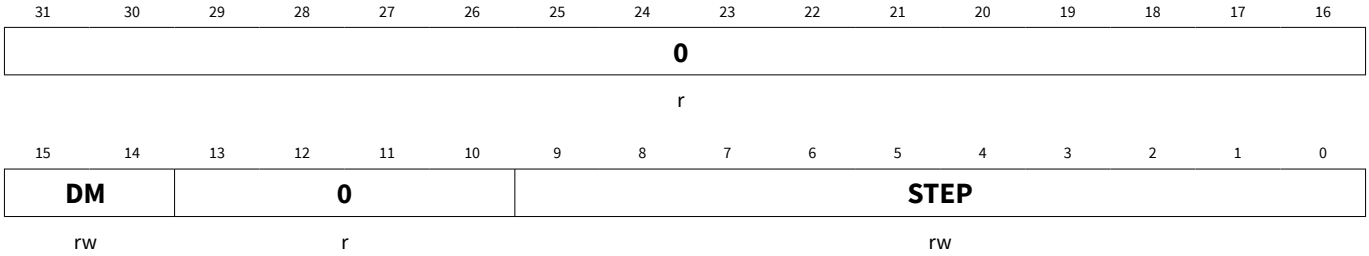
Note: The number of module clock cycles (wait states) which are required by the kernel to execute a read or write access depends on the selected CLC clock frequency.

19.6.3.2.2 Register FDR

The fractional divider register allows the programmer to control the clock rate of the module timer clock f_{CAN}.

FDR Address: $00C_H$

CAN Fractional Divider Register Reset Value: $0000\ 0000_H$



Field	Bits	Type	Description
STEP	9:0	rw	**Step Value** Reload or addition value for the result.
DM	15:14	rw	**Divider Mode** This bit field selects normal divider mode, fractional divider mode, and off-state.
0	13:10, 31:16	r	**Reserved** Read as 0; should be written with 0.

19.6.4 Port and I/O Line Control

The interconnections between the MulticanCAN+ module and the port I/O lines are controlled in the port logic. Additionally to the port input selection, the following port control operations must be executed:

- Input/output function selection (IOCR registers)
- Pad driver characteristics selection for the outputs (PDR registers)

19.6.4.1 Input/Output Function Selection in Ports

The port input/output control registers contain the bit fields that select the digital output and input driver characteristics such as pull-up/down devices, port direction (input/output), open-drain, and alternate output selections. The I/O lines for the MulticanCAN+ module are controlled by the port input/output control registers, which are described in the datasheet. In case of discrepancies between datasheet and CAN chapter, the description in the datasheet is correct.

Table 241 shows the corresponding pins, sorted by node. Even though the table is pair wise, it is possible to select a different pairing for RXD and TXD. In addition the RXSEL value to be programmed for the Receive Pins is part of this table. For more information on RXSEL please see ***Chapter 19.6.4.2***.

Table 241 MulticanCAN+ I/O Control Selection and Setup

Node	RXD	NPCRx.RXSEL	TXD
CAN0		000_B	
		001_B	
	P0.14 / RXDC	010_B	P0.15 / TXD
	P0.15 / RXDD	011_B	P0.14 / TXD

Table 241 MulticanCAN+ I/O Control Selection and Setup (continued)

Node	RXD	NPCRx.RXSEL	TXD
	P2.0 / RXDE	100_B	P2.1 / TXD
	P2.1 / RXDF	101_B	P2.0 / TXD
	P1.0 / RXDG	110_B	P1.1 / TXD
	P1.1 / RXDH	111_B	P1.0 / TXD
CAN1	P0.12 / RXDA	000_B	P0.13 / TXD
	P0.13 / RXDB	001_B	P0.12 / TXD
		010_B	
		011_B	
	P2.10 / RXDE	100_B	P2.11 / TXD
	P2.11 / RXDF	101_B	
		110_B	
		111_B	

19.6.4.2 Node Receive Input Selection

Additionally to the I/O control selection, as defined in the datasheet, the selection of a CAN node's receive input line requires that bit field RXSEL in its node port control register NPCRx must be set according to ***Table 241*** . Values for NPCRx.RXSEL other than those of the table mentioned above will result in a recessive receive input for node x. As a hint A results in 0_H, B in 1_H until H resulting in the value of 7_H.

This feature allows, for example, a CAN node which operates in analyzer mode to monitor the receive operations of its neighbor CAN node.

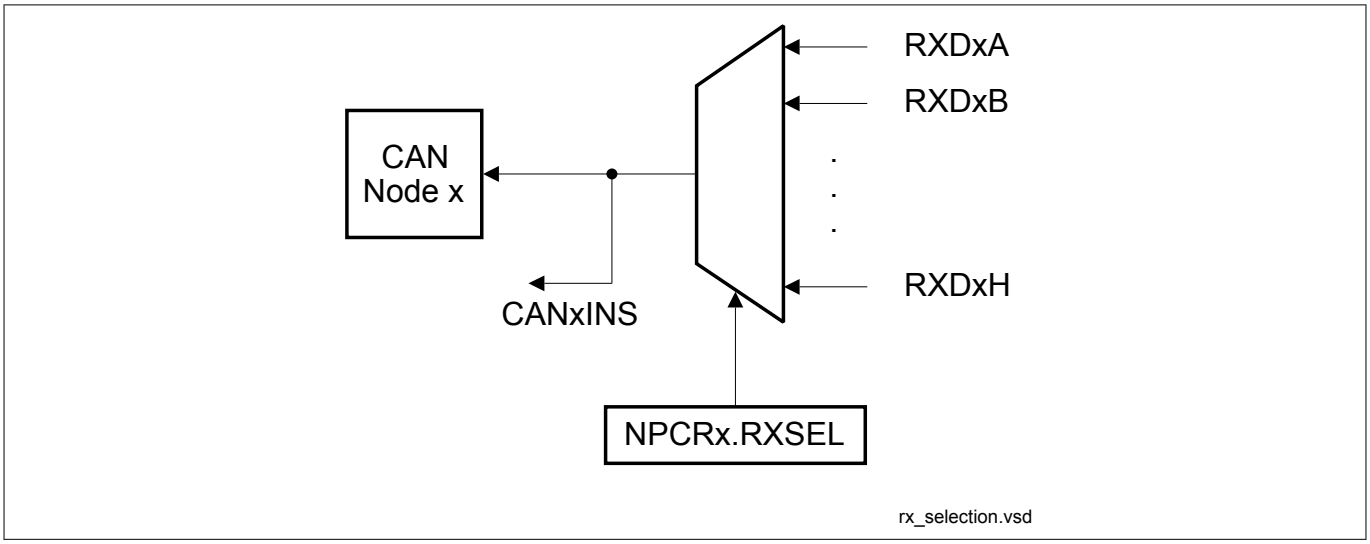


Figure 147 CAN Module Receive Input Selection

19.6.4.3 Connections to Interrupt Router Inputs

The interrupt output lines INT_O0-7 are connected to the Interrupt Router module, see ***Table 242***.

Table 242 Interrupt Router Inputs

Interrupt Router Input	Connected to CAN Interrupt Output
SRC_CANINT0	INT_O0
SRC_CANINT1	INT_O1
SRC_CANINT2	INT_O2
SRC_CANINT3	INT_O3
SRC_CANINT4	INT_O4
SRC_CANINT5	INT_O5
SRC_CANINT6	INT_O6
SRC_CANINT7	INT_O7

19.6.4.4 Connections to ERU

There are the following connections to the ERU:

Table 243 CAN0 Pin Connections

Global Input/Output	I/O	Connected To	Description
CAN0.SRC_CANINT0	O	NVIC	Service Request Output 0
CAN0.SRC_CANINT1	O	NVIC	Service Request Output 1
CAN0.SRC_CANINT2	O	NVIC	Service Request Output 2
CAN0.SRC_CANINT3	O	NVIC	Service Request Output 3
CAN0.SRC_CANINT4	O	ERU1.OGU02	Service Request Output 4
CAN0.SRC_CANINT5	O	ERU1.OGU12	Service Request Output 5
CAN0.SRC_CANINT6	O	ERU1.OGU22	Service Request Output 6
CAN0.SRC_CANINT7	O	ERU1.OGU32	Service Request Output 7

19.6.5 Interrupt Control

The interrupt control logic in the MulticanCAN+ module uses an interrupt compressing scheme that allows high flexibility in interrupt processing. There are hardware and software interrupt sources available:

- CAN node interrupts:
  - Five different interrupt sources for each of the 2 CAN nodes = 5 * 2 interrupt sources
- Message object interrupts:
  - Two interrupt source for each message object = 2 * 32 interrupt sources
- One register (MITR) to initiate 16 interrupts via software

Each of the hardware initiated interrupt sources is controlled by a 4-bit interrupt pointer that directs the interrupt source to one of the 8 interrupt outputs INT_Om (m = 0-7). This makes it possible to connect more than one interrupt source (between one and all) to one interrupt output line. The interrupt wiring matrix shown in ***Figure 148*** is built up according to the following rules:

- Each output of the 4-bit interrupt pointer demultiplexer is connected to exactly one OR-gate input of the INT_Om line. The number “m” of the corresponding selected INT_Om interrupt output line is defined by the interrupt pointer value.
- Each INT_Om output line has an input OR gate which is connected to all interrupt pointer demultiplexer outputs which are selected by an identical 4-bit pointer value.

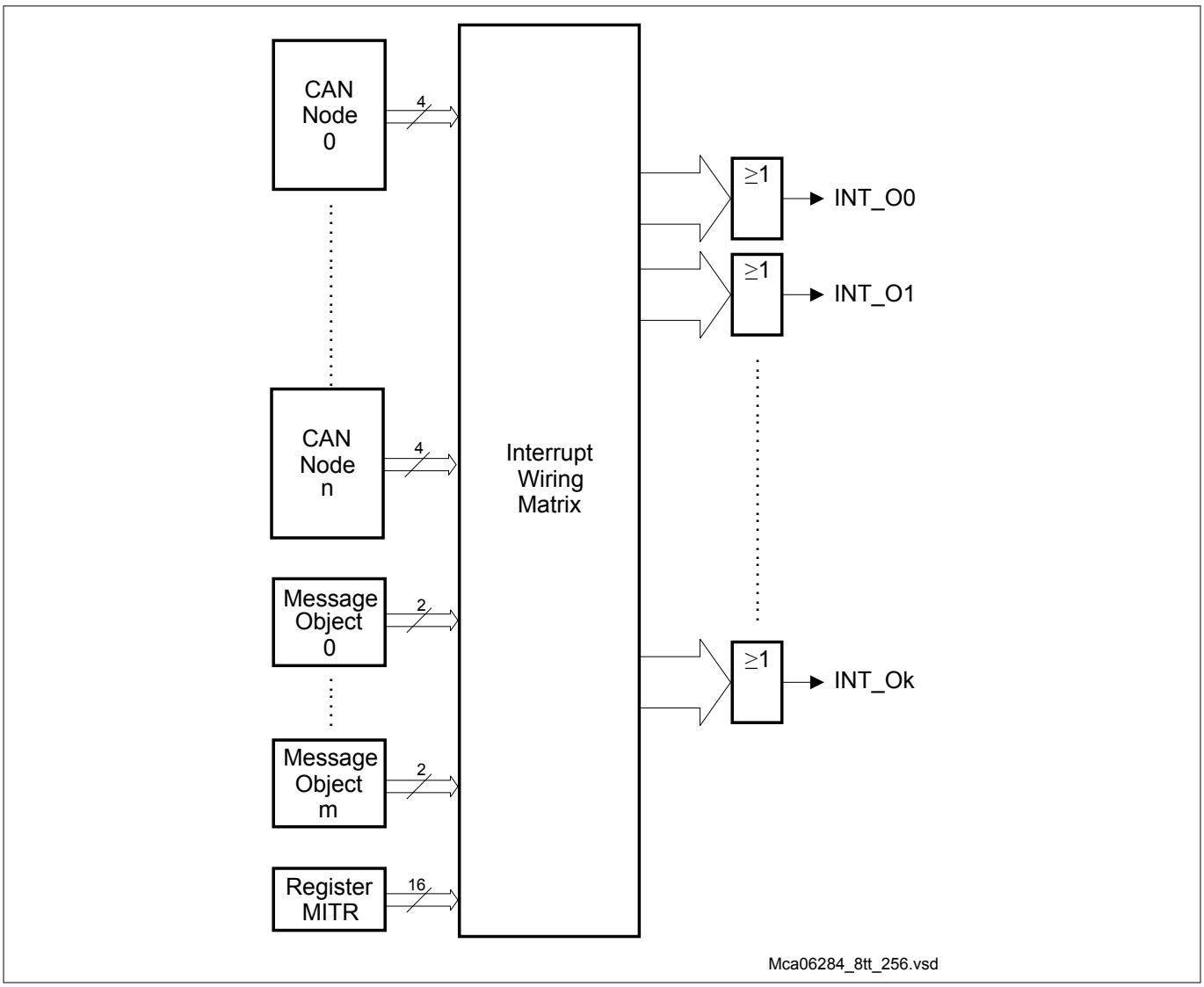


Figure 148 Interrupt Compressor n = 2, m = 32 and k = 8

19.6.6 MulticanCAN+ Module Register Address Map

The complete MulticanCAN+ module register address map of ***Figure 149*** also shows the general implementation-specific registers for clock control, module identification, interrupt service request control and the absolute address information.

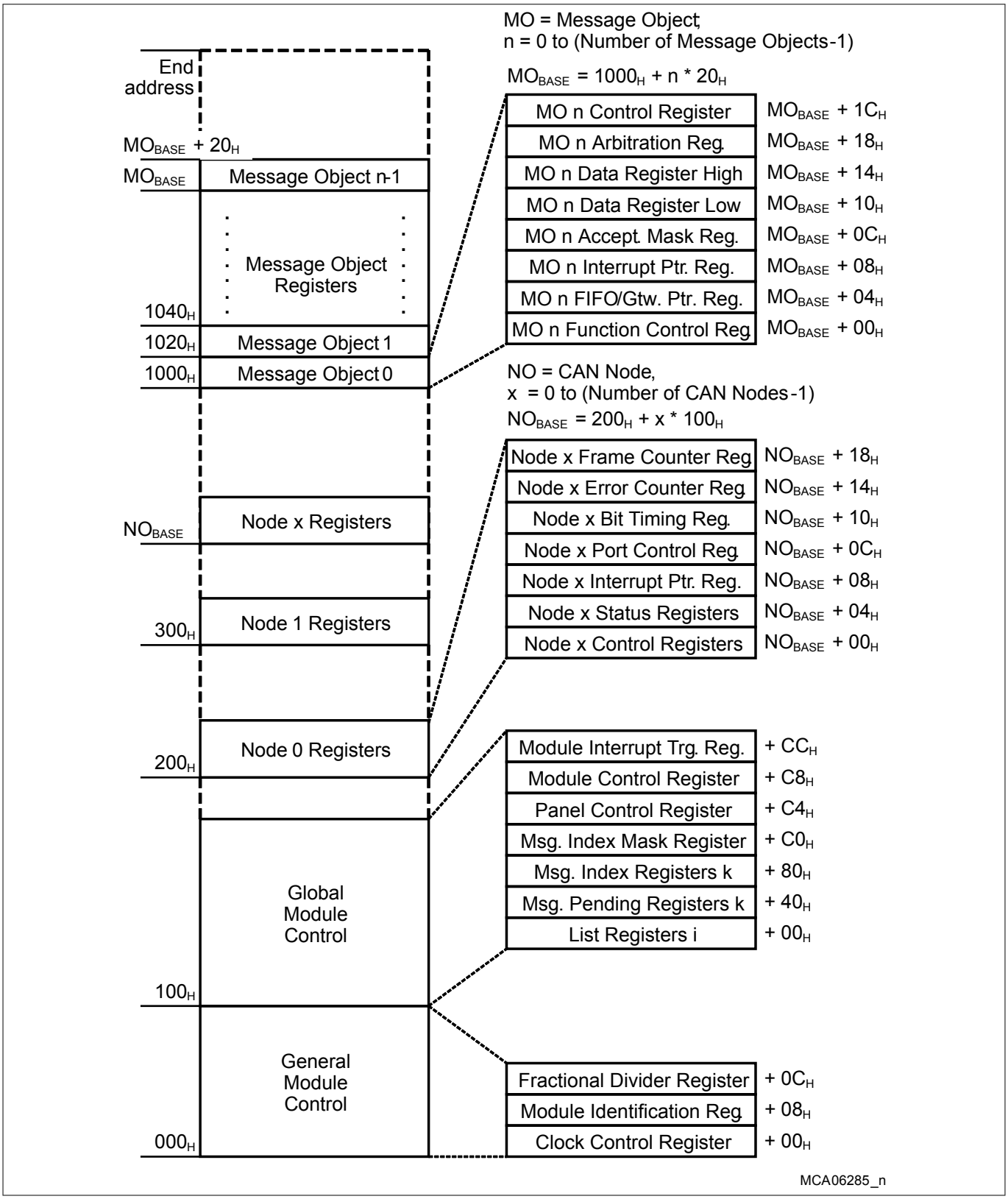


Figure 149 MulticanCAN+ Register Address Map

20 Capture/Compare Unit 4 (CCU4)

The CCU4 peripheral is a major component for systems that need general purpose timers for signal monitoring/ conditioning and Pulse Width Modulation (PWM) signal generation. Power electronic control systems like switched mode power supplies or uninterruptible power supplies, can easily be implemented with the functions inside the CCU4 peripheral.

The internal modularity of CCU4, translates into a software friendly system for fast code development and portability between applications.

Table 244 Abbreviations table

PWM	Pulse Width Modulation
CCU4x	Capture/Compare Unit 4 module instance x
CC4y	Capture/Compare Unit 4 Timer Slice instance y
ADC	Analog to Digital Converter
POSIF	Position Interface peripheral
SCU	System Control Unit
f_{ccu4}	CCU4 module clock frequency
f_{tclk}	CC4y timer clock frequency

Note: A small “y” or “x” letter in a register indicates an index

20.1 Overview

Each CCU4 module is comprised of four identical 16 bit Capture/Compare Timer slices, CC4y. Each timer slice can work in compare mode or in capture mode. In compare mode one compare channel is available while in capture mode, up to four capture registers can be used in parallel.

Each CCU4 module has four service request lines and each timer slice contains a dedicated output signal, enabling the generation of up to four independent PWM signals.

Straightforward timer slice concatenation is also possible, enabling up to 64 bit timing operations. This offers a flexible frequency measurement, frequency multiplication and pulse width modulation scheme.

A programmable function input selector for each timer slice, that offers up to nine functions, discards the need of complete resource mapping due to input ports availability.

A built-in link between the CCU4 and several other modules enable flexible digital motor control loops implementation, e.g. with Hall Sensor monitoring or direct coupling with Encoders.

20.1.1 Features

CCU4 module features

Each CCU4 represents a combination of four timer slices, that can work independently in compare or capture mode. Each timer slice has a dedicated output for PWM signal generation.

All four CCU4 timer slices, CC4y, are identical in terms of available functions and operating modes. Avoiding this way the need of implementing different software routines, depending on which resource of CCU4 is used.

A built-in link between the four timer slices is also available, enabling this way a simplified timer concatenation and sequential operations.

General Features:

- 16 bit timer cells

- capture and compare mode for each timer slice
  - four capture registers in capture mode
  - one compare channel in compare mode
- programmable low pass filter for the inputs
- built-in timer concatenation
  - 32, 48 or 64 bit width
- shadow transfer for the period and compare values
- programmable clock prescaler
- normal and gated timer mode
- three counting schemes
  - center aligned
  - edge aligned
  - single shot
- PWM generation
- TRAP function
- start/stop can be controlled by external events
- counting external events
- four dedicated service request lines per CCU4

Additional features:

- flexible coherent and non coherent update mechanism
- external modulation function
- load controlled by external events
- dithering PWM
- floating point prescaler
- output state override by an external event
- suitable and flexible connectivity to several modules:
  - motor and power conversion applications
  - high number of signal conditioning possibilities

CCU4 features vs. applications

On *Table 245* a summary of the major features of the CCU4 unit mapped with the most common applications.

Table 245 Applications summary

Feature	Applications
Four independent timer cells	Independent PWM generation: • Multiple buck/boost converter control (with independent frequencies) • Different modes of operation for each timer, increasing the resource optimization • Up to 2 Half-Bridges control • multiple Zero Voltage Switch (ZVS) converter control with easy link to the ADC channels.
Concatenated timer cells	Easy to configure timer extension up to 64 bit: • High dynamic trigger capturing • High dynamic signal measurement

Table 245 Applications summary (continued)

Feature	Applications
Dithering PWM	Generating a fractional PWM frequency or duty cycle: • To avoid big steps on frequency or duty cycle adjustment in slow control loop applications • Increase the PWM signal resolution over time
Floating prescaler	Automated control signal measurement: • decrease SW activity for monitoring signals with high or unknown dynamics • emulating more than a 16 bit timer for system control
Up to 9 functions via external signals for each timer	Flexible resource optimization: • The complete set of external functions is always available • Several arrangements can be done inside a CCU4, e.g., one timer working in capture mode and one working in compare
4 dedicated service request lines	Specially developed for: • generating interrupts for the microprocessor • flexible connectivity between peripherals, e.g. ADC triggering.
Linking with other modules	Flexible profiles for: • Hall Sensor feedback/monitoring • Motor Encoders feedback/monitoring • PWM parallel modulation • Flexible signal conditioning
Flexible coherent and non coherent update schemes	Flexible profiles that can be used for: • fuel injection control • multiple observation points for motor shaft rotation • on-the-fly compensation linked to real-time operation condition sensing • cpu load optimization for fast control loops

20.1.2 Block Diagram

Each CCU4 timer slice can operate independently from the other slices for all the available modes. Each timer slice contains a dedicated input selector for functions linked with external events and has a dedicated compare output signal, for PWM signal generation.

The built-in timer concatenation is only possible with adjacent slices, e.g. CC40/CC41. Combinations for slice concatenations like, CC40/CC42 or CC40/CC43 are not possible.

The individual service requests for each timer slice (four per slice) are multiplexed into four module service requests lines, ***Figure 150***.

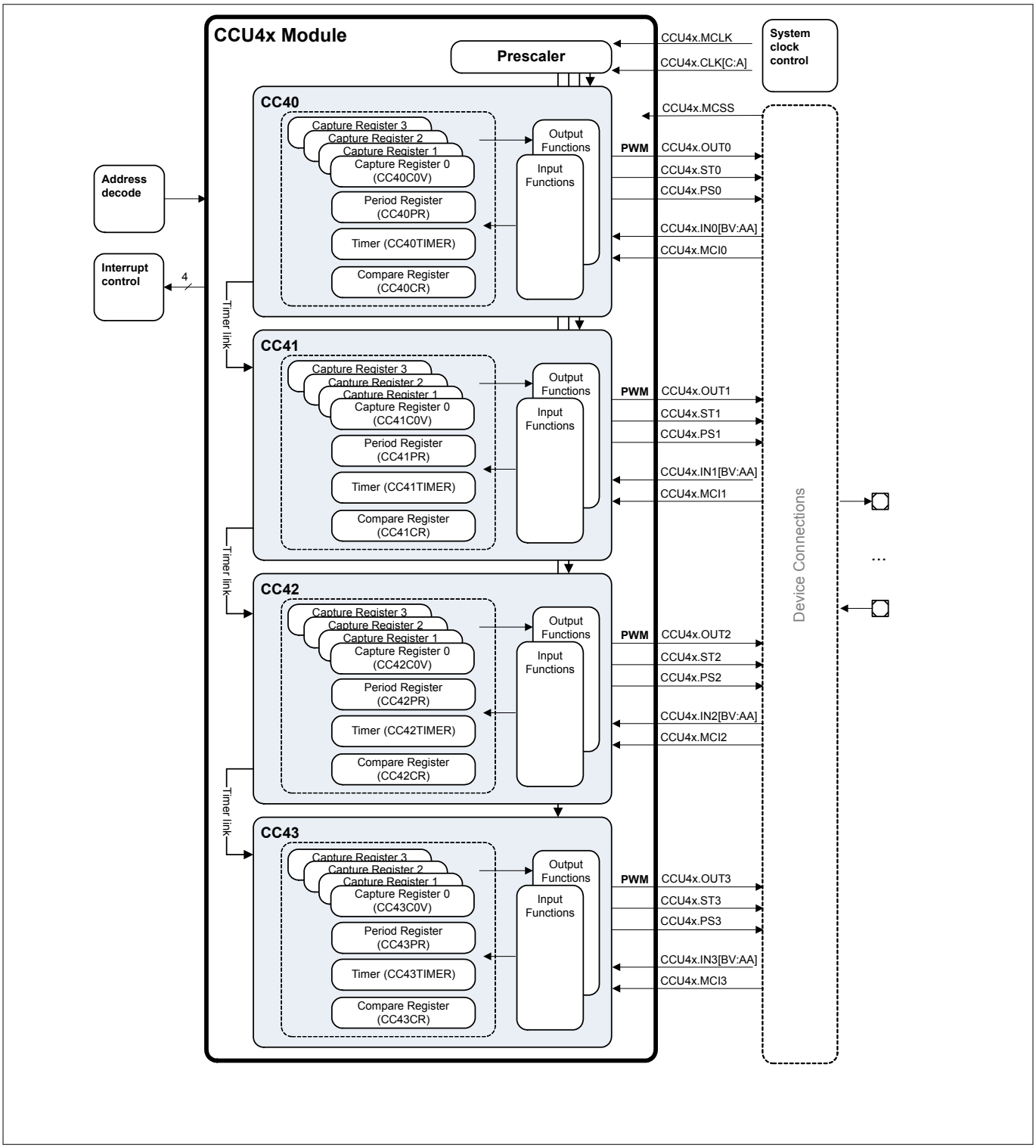


Figure 150 CCU4 block diagram

20.2 Functional Description

The following sections describe the complete set of functions and usability of the CCU4 peripheral.

In each figure several registers may be depicted to indicate controlability or configurability. These registers follow the description given in ***Figure 151***. One should also note that indexing in a register can be done via the non capital y, x or n.

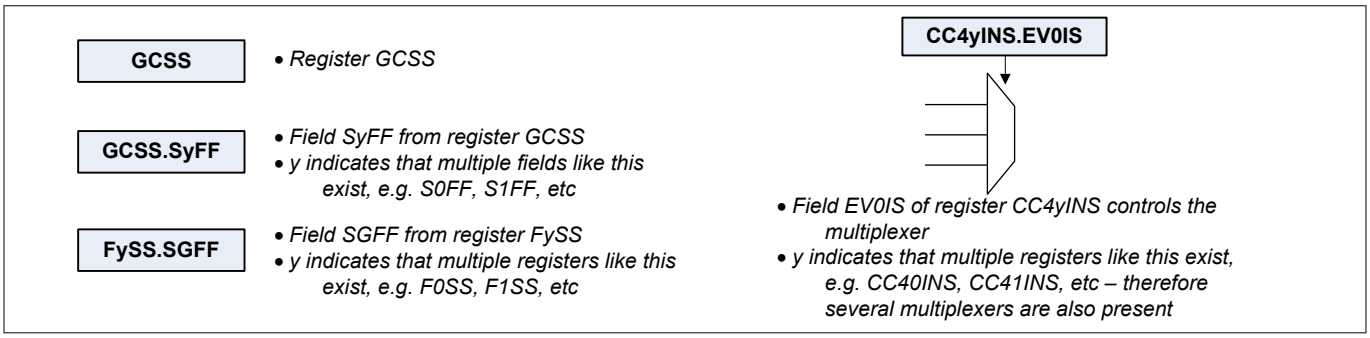


Figure 151 Register description in figures (example)

20.2.1 Timer Slice Overview

The input path of a CCU4 timer slice (a timer slice has a nomenclature of CC4y) is comprised of a selector (***Chapter 20.2.2***) and a connection matrix unit (***Chapter 20.2.3***). Via the input selector and connection matrix, the user can select several signals - that are connected to ports or peripherals - to control several available functions inside the timer kernel, e.g. start, stop, count, etc. The output path contains a service request control unit, a timer concatenation unit and two units that control directly the state of the output signal for each specific slice (for TRAP and modulation handling), see ***Figure 152***.

The timer core is built of a 16 bit counter one period and one compare register in compare mode, or up to four capture registers in capture mode.

In compare mode the period register sets the maximum counting value while the compare channel is controlling the ACTIVE/PASSIVE state of the dedicated comparison slice output.

The slice timer, can count up or down depending on the selected operating mode. A direction flag holds the actual counting direction.

The timer is connected to two stand alone comparators, one for the period match and one for a compare match. The registers used for period match and comparison match can be programmed to serve as capture registers enabling sequential capture capabilities on external events.

In normal edge aligned counting scheme, the counter is cleared to 0000_H each time that matches the period value defined in the period register. In center aligned mode, the counter direction changes from ‘up counting’ to ‘down counting’ after reaching the period value. Both period and compare registers have an aggregated shadow register, which enables the update of the PWM period and duty cycle on the fly.

A single shot mode is also available, where the counter stops after it reaches the value set in the period register.

The start and stop of the counter can be controlled via software access or by a programmable input pin.

Functions like, load, counting direction (up/down), TRAP and output modulation can also be controlled with external events, see ***Chapter 20.2.3***

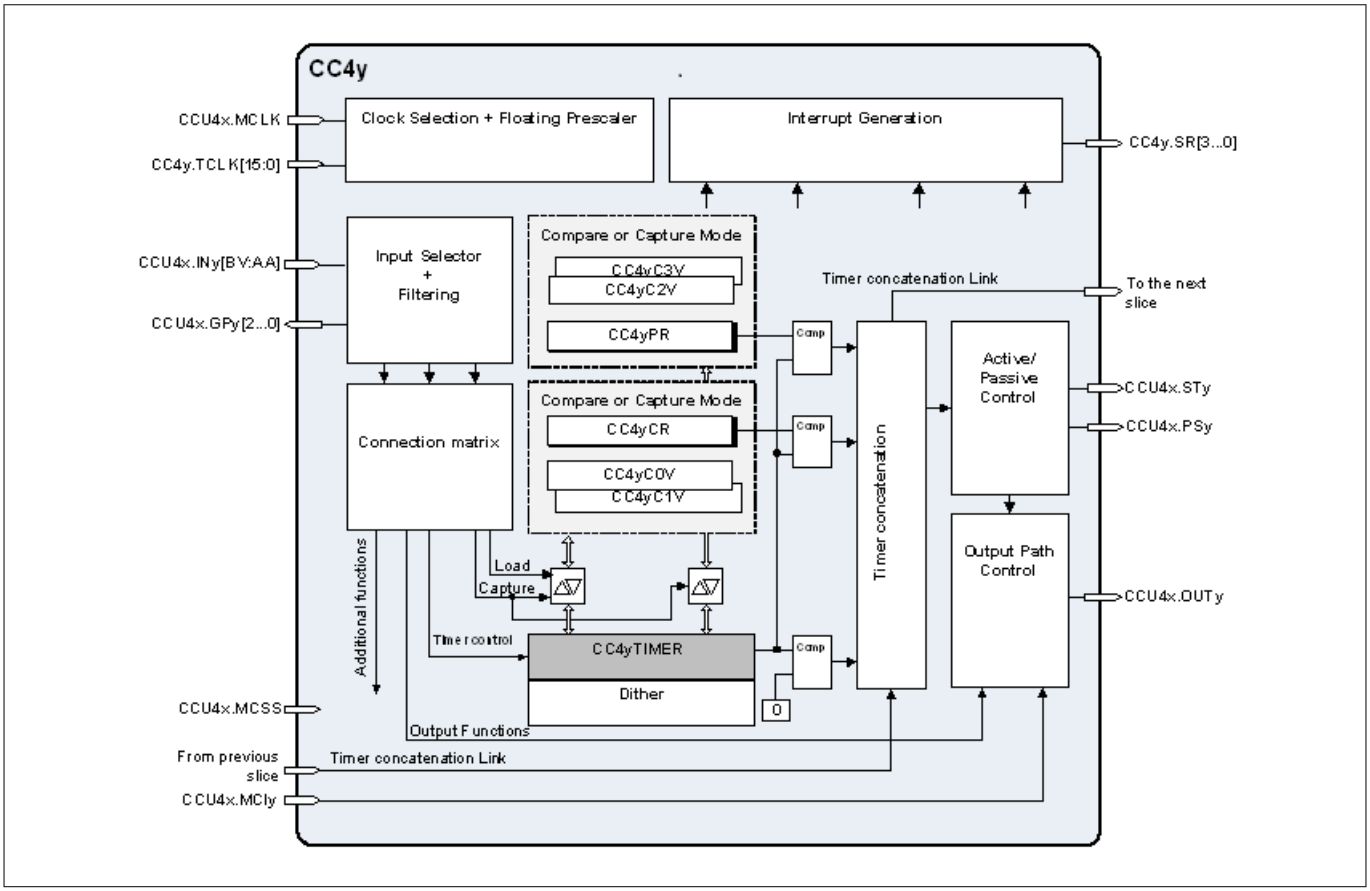


Figure 152 CCU4 slice block diagram

For more information to the functional blocks see the following links:

- ***Clock Prescaler***
- ***Service Request Generation***
- ***Timer Slice Input Selector***
- ***Timer Slice Connection Matrix***
- ***Timer Concatenation***
- ***PWM Active/Passive Rules***
- ***Output PWM Path***
- ***Timer Slice Core Functions***
- ***PWM Dither***

Each CCU4 slice, with the exception of the first, contains six dedicated inputs outputs that are used for the built-in timer concatenation functionality.

Inputs and outputs that are not seen at the CCU4 boundaries have a nomenclature of CC4y.<name>, whilst CCU4 module inputs and outputs are described as CCU4x.<signal_name>y (indicating the variable y the timer slice).

Table 246 CCU4 slice pin description

Pin	I/O	Description
CCU4x.MCLK	I	Module clock
CC4y.TCLK[15:0]	I	Clocks from the prescaler

Table 246 CCU4 slice pin description (continued)

Pin	I/O	Description
CCU4x.INy[BV:AA]	I	Slice functional inputs (used to control the functionality throughout slice external events)
CCU4x.MCIy	I	Multi-Channel mode input
CCU4x.MCSS	I	Multi-Channel shadow transfer trigger
CC4y.SR[3...0]	O	Slice service request lines
CCU4x.GPy[2...0]	O	Signals decoded from the input selector
CC4x.STy	O	Slice comparison status value
CCU4x.PSy	O	Multi-Channel pattern update trigger
CCU4x.OUTy	O	Slice dedicated output pin

Note:
- *The status bit outputs of the Kernel, CCU4x.STy, are extended for one more kernel clock cycle.*
- *The Service Request signals at the output of the kernel are extended for one more kernel clock cycle.*
- *The maximum output signal frequency of the CCU4x.STy outputs is module clock divided by 4.*

20.2.2 Timer Slice Input Selector

The first unit of the slice input path, is used to select which inputs are used to control the available external functions.

Inside this block the user also has the possibility to perform a low pass filtering of the signals and selecting the active edge(s) or level of the external event, see ***Figure 153***.

The user has the possibility of selecting any of the CCU4x.INy[BV:AA] inputs as the source of an event.

At the output of this unit we have a user selection of three events, that were configured to be active at rising, falling or both edges, or level active. These selected events can then be mapped to several functions.

Notice that each decoded event contains two outputs, one edge active and one level active, due to the fact that some functions like counting, capture or load are edge sensitive events while, timer gating or up down counting selection are level active.

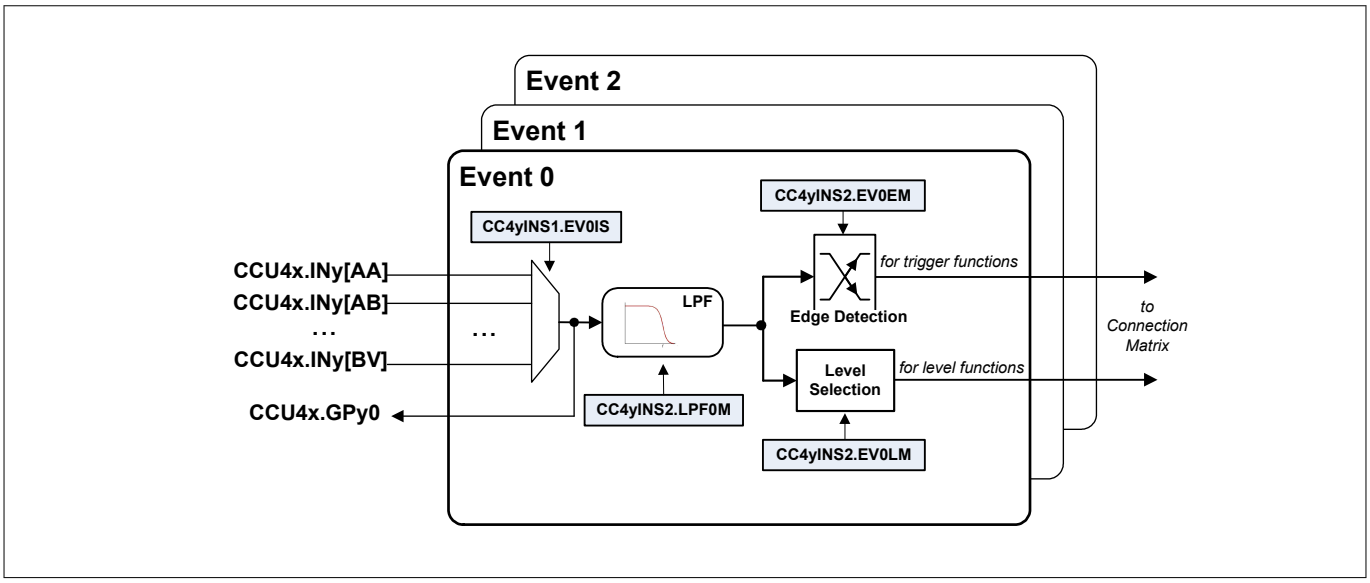


Figure 153 Slice input selector diagram

20.2.3 Timer Slice Connection Matrix

The connection matrix maps the events coming from the input selector to several user configured functions, ***Figure 154***. The following functions can be enabled on the connection matrix:

Table 247 Connection matrix available functions

Function	Brief description	Map to *Figure 154*
Start	Edge signal to start the timer	CCystrt
Stop	Edge signal to stop the timer	CCystp
Count	Edge signal used for counting events	CCycnt
Up/down	Level signal used to select up or down counting direction	CCyupd
Capture 0	Edge signal that triggers a capture into the capture registers 0 and 1	CCycapt0
Capture 1	Edge signal that triggers a capture into the capture register 2 and 3	CCycapt1
Gate	Level signal used to gate the timer clock	CCygate
Load	Edge signal that loads the timer with the value present at the compare register	CCyload
TRAP	Level signal used for fail-safe operation	CCytrap
Modulation	Level signal used to modulate/clear the output	CCymod
Status bit override	Status bit is going to be overridden with an input value	CCyoval for the value CCyoset for the trigger

Inside the connection matrix we also have a unit that performs the built-in timer concatenation. This concatenation enables a completely synchronized operation between the concatenated slices for timing operations and also for capture and load actions. The timer slice concatenation is done via the ***CC4yCMC***.TCE bitfield. For a complete description of the concatenation function, please address ***Chapter 20.2.6.2***.

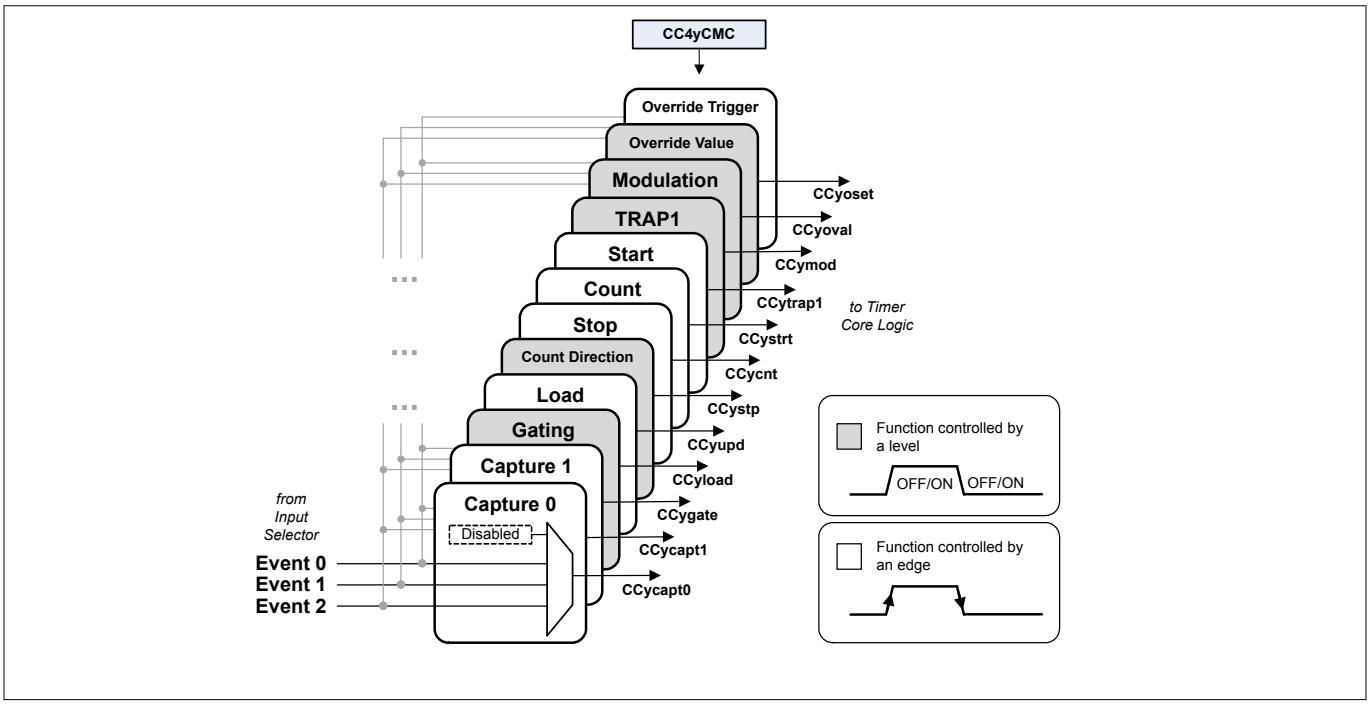


Figure 154 Slice connection matrix diagram

20.2.4 Timer Slice Core Functions

In the following sub sections one can find the description of the main functionalities of each CCU4 Timer Slice core. This functions include the different counting schemes, how to start and stop a timer or how to calculate and update the duty cycle of each Timer Slice.

Besides these functions, there are several others that can be controlled via external signals, e.g. port pins or other peripherals - these functions are described in ***Chapter 20.2.5***.

20.2.4.1 Starting/Stopping the Timer

Each timer slice contains a run bit register that indicates the actual status of the timer, ***CC4yTCST***.TRB. The start and stop of the timer can be done via software access or can be controlled directly by external events, see ***Figure 155*** .

Selecting an external signal that acts as a start trigger does not force the user to use an external stop trigger and vice versa.

Selecting the single shot mode, imposes that after the counter reaches the period value the run bit, ***CC4yTCST***.TRB, is going to be cleared and therefore the timer is stopped.

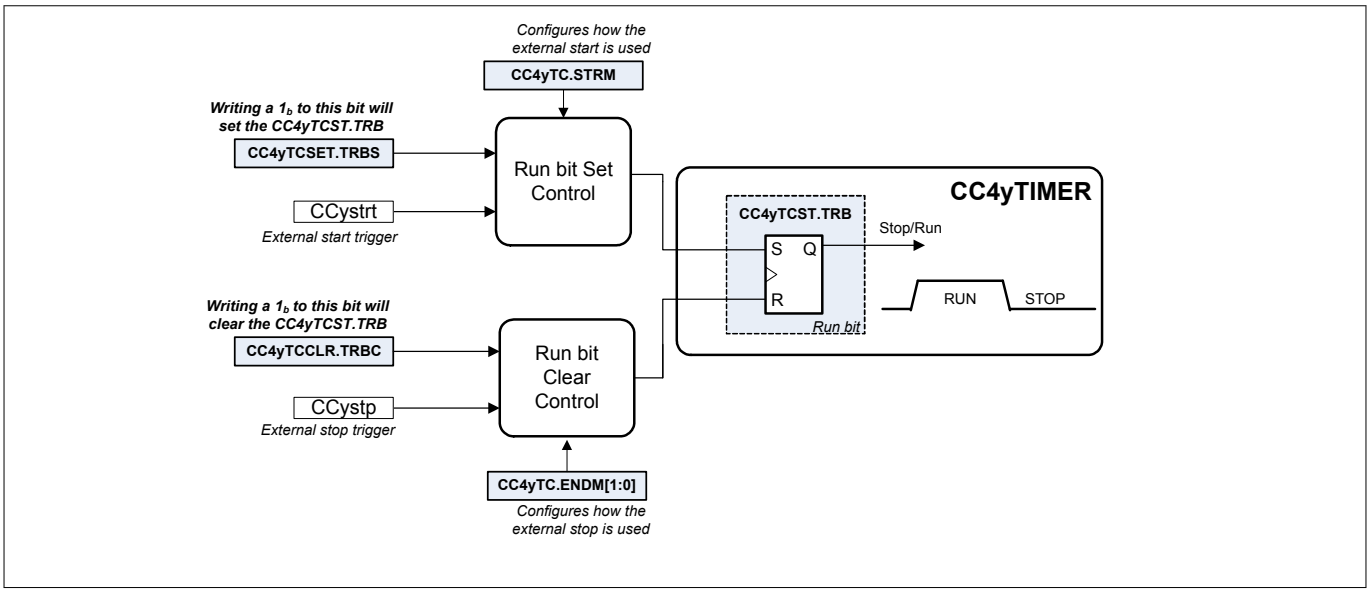


Figure 155 Timer start/stop control diagram

One can use the external stop signal to perform the following functions (configuration via ***CC4yTC***.ENDM):

- Clear the run bit (stops the timer) - default
- Clear the timer (to 0000_H) but it does not clear the run bit (timer still running)
- Clear the timer and the run bit

One can use the external start to perform the following functions (configuration via ***CC4yTC***.STRM):

- Start the timer (resume operation)
- Clear and start the timer

The set (start the timer) of the timer run bit, always has priority over a clear (stop the timer).

To start multiple CCU4 timers at the same time/synchronously one should use a dedicated input as external start (see ***Chapter 20.2.5.1*** for a description how to configure an input as start function). This input should be connected to all the Timers that need to be started synchronously (see ***Chapter 20.8*** for a complete list of module connections), ***Figure 156***.

For starting the timers synchronously via software there is a dedicated input signal, controlled by the SCU (System Control Unit), that is connected to all the CCU4 timers. This signal should then be configured as an external start signal (see ***Chapter 20.2.5.1***) and then the software must write $1_B/0_B$ (depending on the configuration of the external start function) to the specific bitfield of the CCUCON register (this register is described on the SCU chapter).

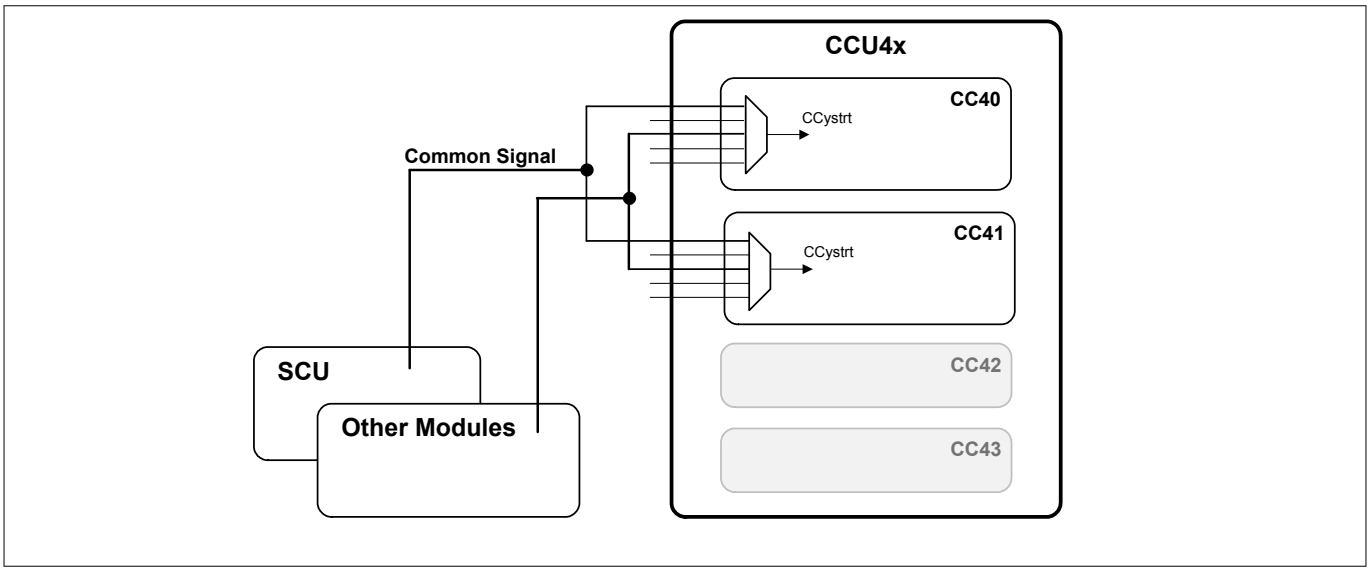


Figure 156 Starting multiple timers synchronously

20.2.4.2 Counting Modes Introduction

Each CC4y timer slice can be programmed into three different counting schemes:

- Edge aligned (default)
- Center aligned
- Single shot (can be edge or center aligned)

These three counting schemes can be used as stand alone without the need of selecting any inputs as external event sources. Nevertheless it is also possible to control the counting operation via external events like, timer gating, counting trigger, external stop, external start, etc.

For all the counting modes, it is possible to update on the fly the values for the timer period and compare channel. This enables a cycle by cycle update of the PWM frequency and duty cycle.

Each compare channel of the CC4y Timer Slice has an associated Status Bit (***GCST***.CC4yST), that indicates the active or passive state of the channel, ***Figure 157***. The set and clear of the status bit and the respective PWM signal generation is dictated by the timer period, compare value and the current counting mode. Please address the different counting mode descriptions - ***Chapter 20.2.4.3*** to ***Chapter 20.2.4.5*** - to understand how this bitfield is set and cleared, and to have a full description of the timer behavior.

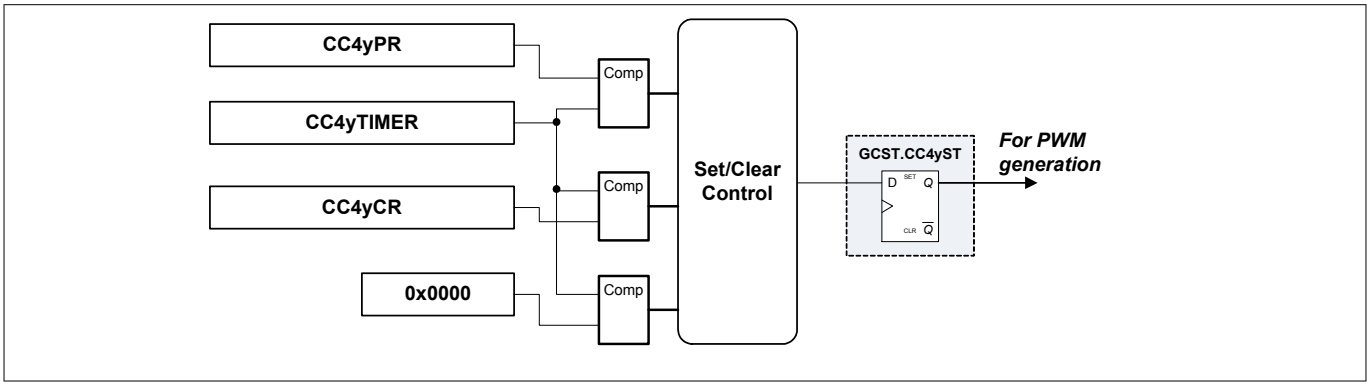


Figure 157 CC4y Status Bit

20.2.4.3 Edge Aligned Mode

Edge aligned mode is the default counting scheme. In this mode, the timer is incremented until it matches the value programmed in the period register, ***CC4yPR***. When period match is detected the timer is cleared to 0000_H and continues to be incremented - ***Figure 158***.

In edge aligned mode, the status bit of the comparison (CC4yST) is set one clock cycle after the timer hits the value programmed into the compare register. The clear of the status bit is done one clock cycle after the timer reaches 0000_H.

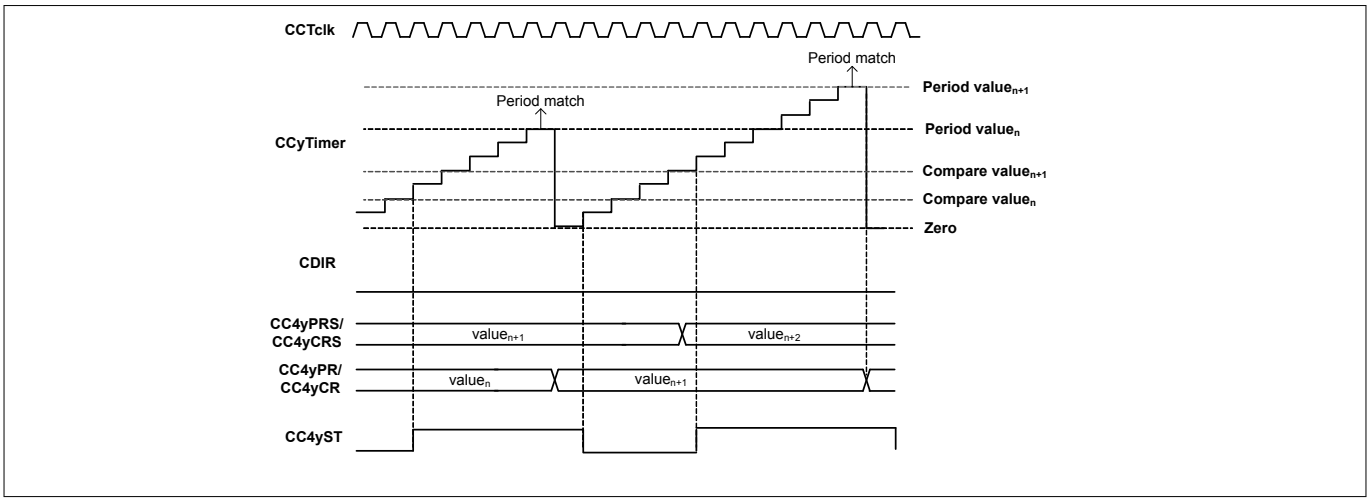


Figure 158 Edge aligned mode, *CC4yTC*.TCM = 0

In edge aligned mode, the value of the period register and compare register are updated with the value written by software into the corresponding shadow register (CC4yPRS and CC4yCRS), every time that an overflow occurs (period match) - ***Figure 158***.

If an immediate update of the compare value and/or period is needed for the application, then the ***CC4ySTC***.IRCC and ***CC4ySTC***.IRPC need to be configure to 1_B - ***Figure 159*** and ***Figure 160***.

A complete description how to update the compare and period values is given in ***Chapter 20.2.4.7***.

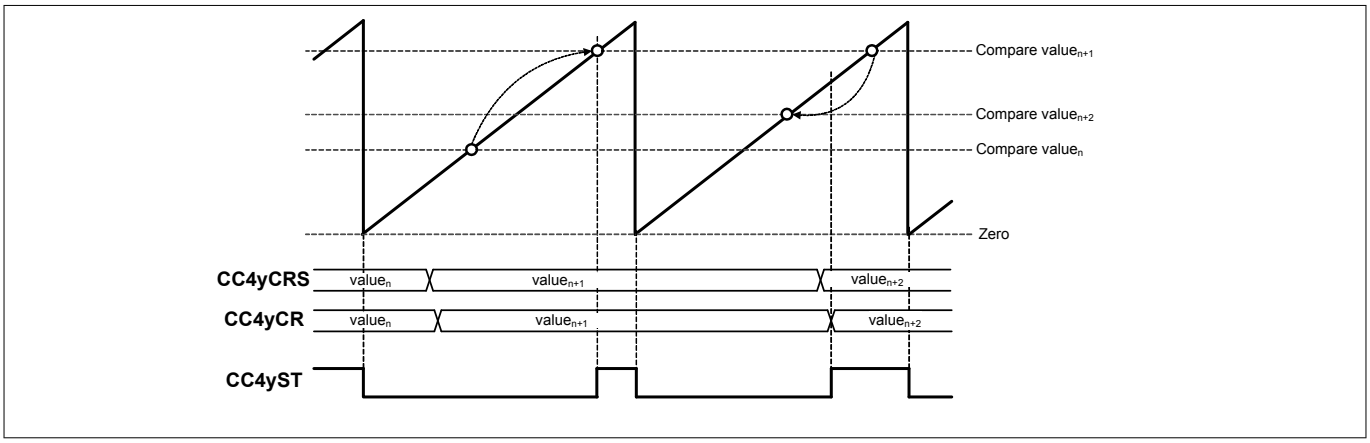


Figure 159 Edge aligned mode, immediate compare value update

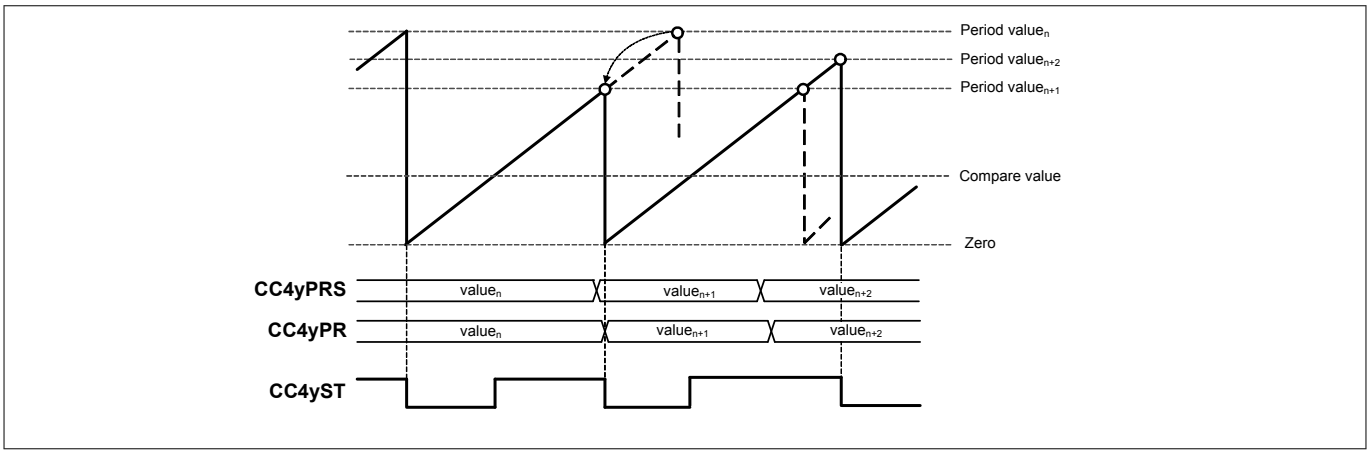


Figure 160 Edge aligned mode, immediate period value update

20.2.4.4 Center Aligned Mode

In center aligned mode, the timer is counting up or down with respect to the following rules:

- The counter counts up while ***CC4yTCST***.CDIR = 0_B and it counts down while ***CC4yTCST***.CDIR = 1_B.
- Within the next clock cycle, the count direction is set to counting up (***CC4yTCST***.CDIR = 0_B) when the counter reaches 0001_H while counting down.
- Within the next clock cycle, the count direction is set to counting down (***CC4yTCST***.CDIR = 1_B), when the period match is detected while counting up.

The status bit (CC4yST) is always 1_B when the counter value is equal or greater than the compare value and 0_B otherwise.

*Note: The bitfield **CC4yTCST**.CDIR changes within the next timer clock after the one-match or the period-match, which means that the timer continues counting in the previous direction for one more cycle before changing the direction.*

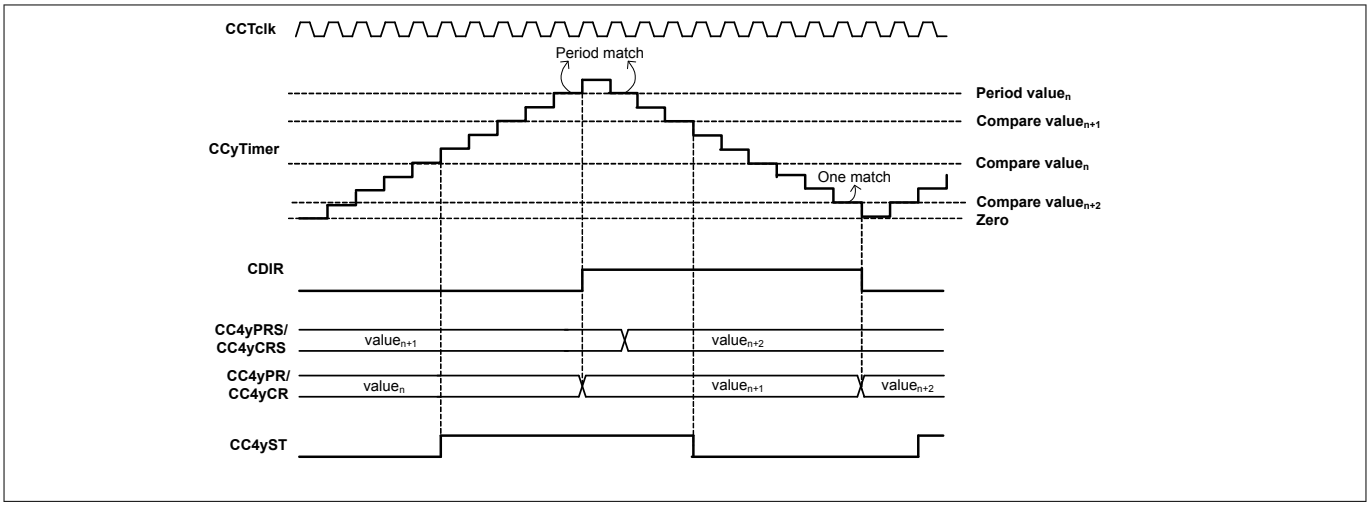


Figure 161 Center aligned mode, *CC4yTC*.TCM = 1

While in edge aligned mode, the shadow transfer for compare and period registers is executed once per switching cycle, in center aligned mode it can be executed twice:

- Within the next clock cycle after the counter reaches the period value, while counting up (***CC4yTCST***.CDIR = 0_B).
- Within the next clock cycle after the counter reaches 0001_H, while counting down (***CC4yTCST***.CDIR = 1_B).

It is also possible to select in which instant the update is done. This is done by configuring the ***CC4ySTC***.STM field accordingly.

If an immediate update of the compare value and/or period is needed for the application, then the ***CC4ySTC***.IRCC and ***CC4ySTC***.IRPC need to be configure to 1_B - ***Figure 162*** and ***Figure 163***.

A complete description how to update the compare and period values is given in ***Chapter 20.2.4.7***.

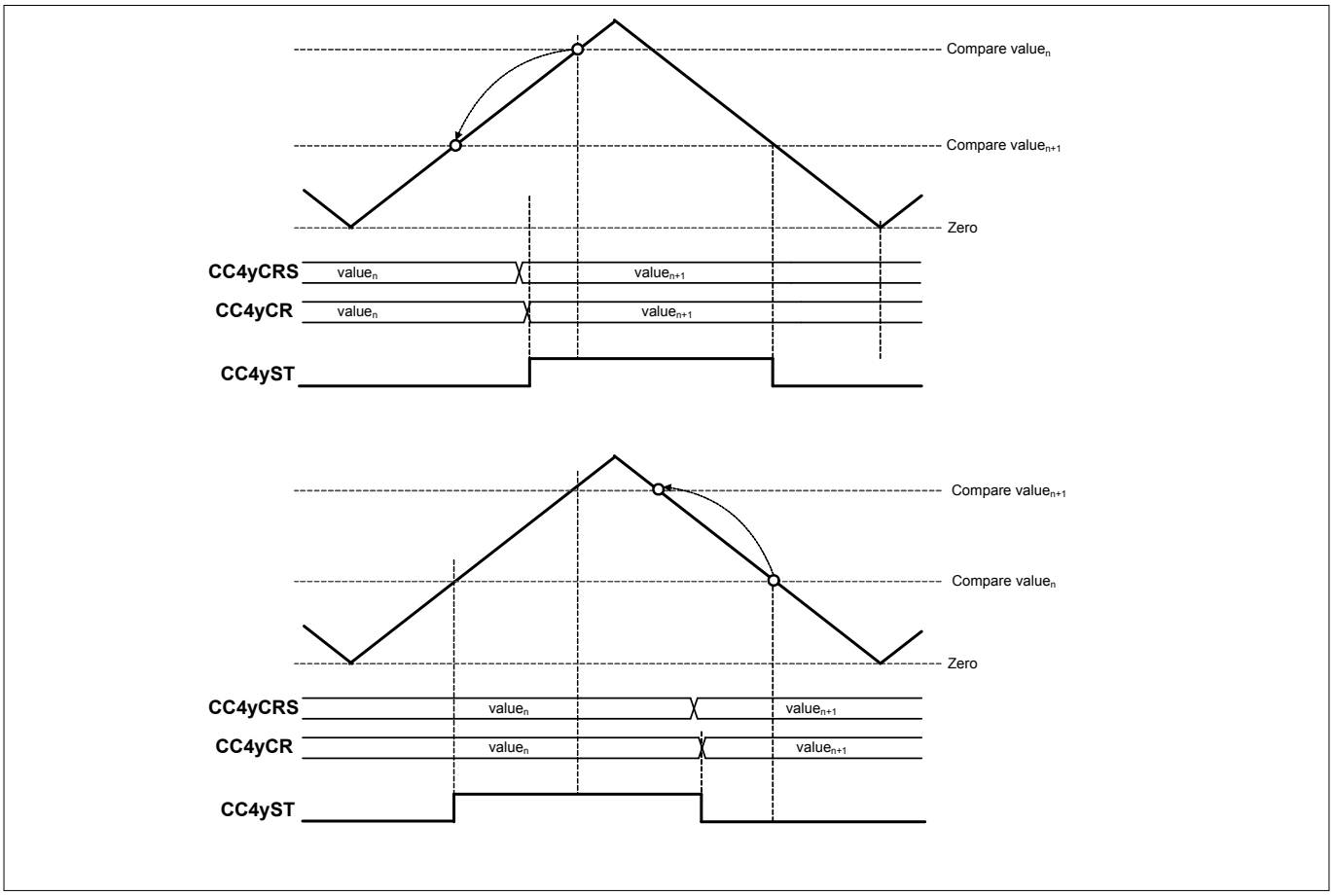


Figure 162 Center aligned mode, immediate compare value update

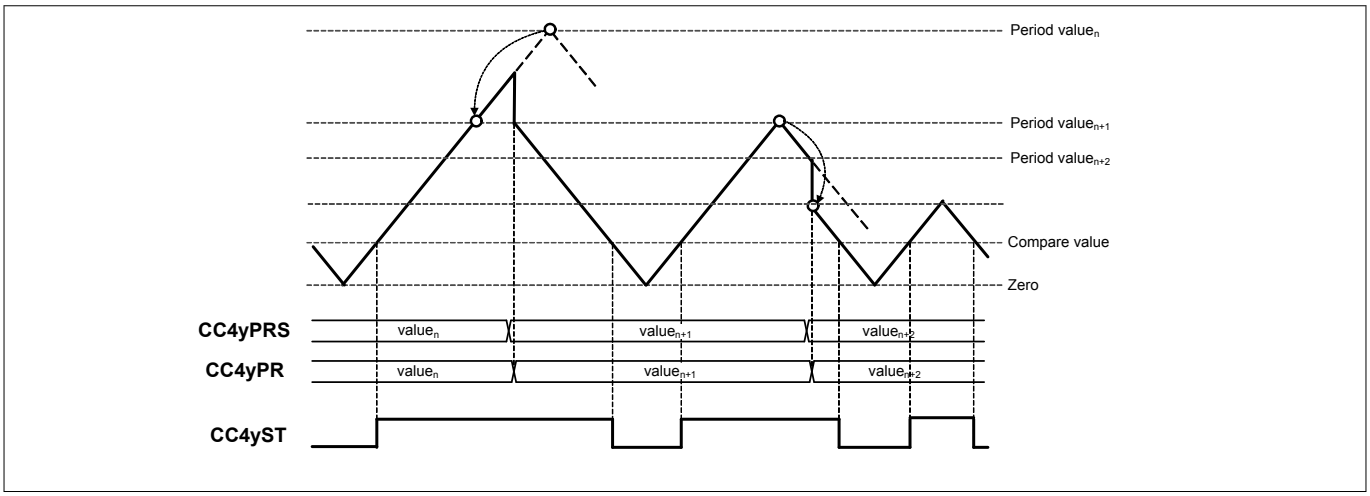


Figure 163 Center aligned mode, immediate period value update

20.2.4.5 Single Shot Mode

In single shot mode, the timer is stopped after the current timer period is finished. This mode can be used with center or edge aligned scheme.

In edge aligned mode, ***Figure 164***, the timer is stopped when it is cleared to 0000_H after having reached the period value. In center aligned mode, ***Figure 165***, the period is finished when the timer has counted down to 0000_H.

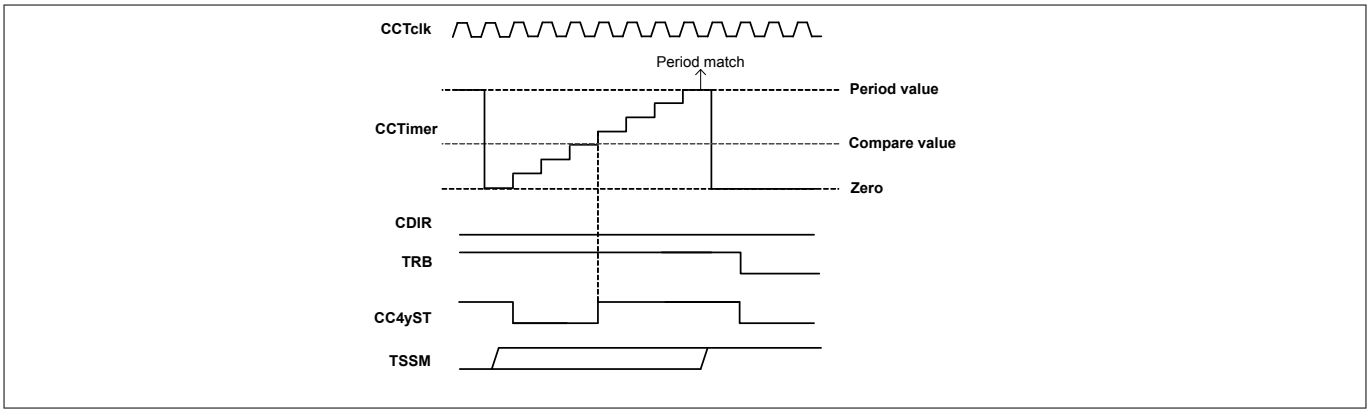


Figure 164 Single shot edge aligned - *CC4yTC*.TSSM = 1, *CC4yTC*.TCM = 0

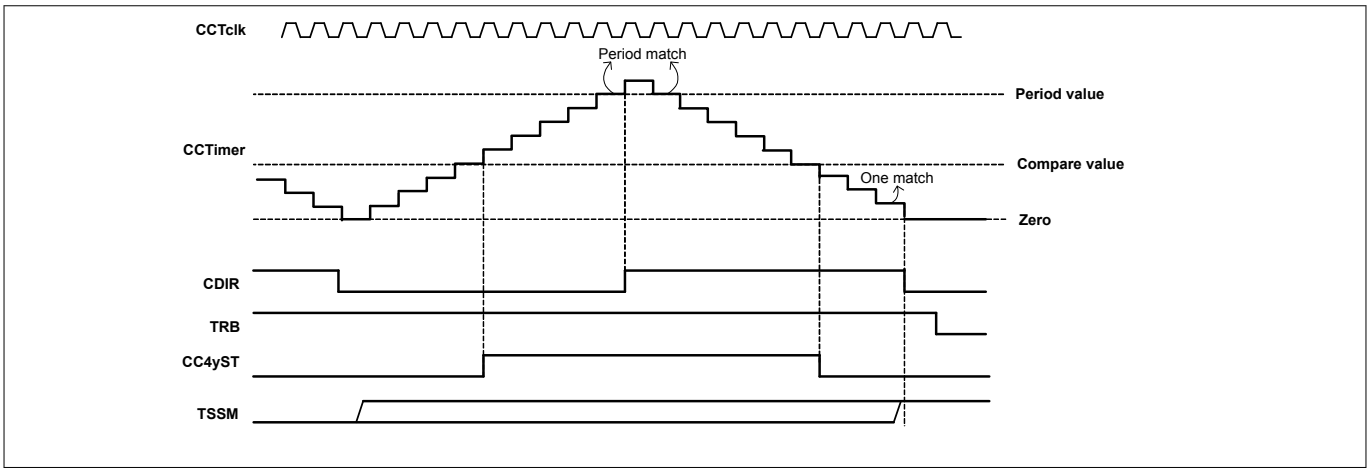


Figure 165 Single shot center aligned - *CC4yTC*.TSSM = 1, *CC4yTC*.TCM = 1

20.2.4.6 Calculating the PWM Period and Duty Cycle

The period of the timer is determined by the value in the period register, ***CC4yPR*** and by the timer mode.

The base for the PWM signal frequency and duty cycle, is always related to the clock frequency of the timer itself and not to the frequency of the module clock (due to the fact that the timer clock can be a scaled version of the module clock).

In Edge Aligned Mode, the timer period is:

$$T_{per} = \text{< Period Value >} + 1; \text{in } f_{tclk}$$

Equation 27

In Center Aligned Mode, the timer period is:

$$T_{per} = (\text{< Period Value >} + 1) \times 2; \text{in } f_{tclk}$$

Equation 28

For each of these counting schemes, the duty cycle of generated PWM signal is dictated by the value programmed into the ***CC4yCR*** register.

In Edge Aligned and Center Aligned Mode, the PWM duty cycle is:

$$DC = 1 - \text{< Compare Value >} / (\text{< Period Value >} + 1)$$

Equation 29

Both ***CC4yPR*** and ***CC4yCR*** can be updated on the fly via software, enabling a glitch free transition between different period and duty cycle values for the generated PWM signal, ***Chapter 20.2.4.7***

20.2.4.7 Updating the Period, Duty Cycle and other PWM conditions

Every CCU4 timer slice contains several registers that can be updated on-the-fly, via software, with the intent of modifying certain pwm generation conditions. The most common parameters that need to be updated on-the-fly are normally the period and compare values - that will directly control the duty cycle and switching frequency.

Besides these parameters, each timer slice also permits the user to update on-the-fly the floating prescaler, dither and even the passivel level of the PWM signal. The following text descriptions, will give an overview of the registers/parameters that can be updated on-the-fly, and also the options available to control this update.

Shadow Registers Overview

Each CCU4 timer slice provides an associated shadow register for the period and compare values. This facilitates a concurrent update by software for these two parameters, with the objective of modifying during run time the PWM signal period and duty cycle.

In addition to the shadow registers for the period and compare values, one also has available shadow registers for the floating prescaler and dither functions, ***CC4yFPCS*** and ***CC4yDITS*** respectively (please address ***Chapter 20.2.7*** and ***Chapter 20.2.6.3*** for a complete description of these functions).

The structure of the shadow registers can be seen in ***Figure 166***.

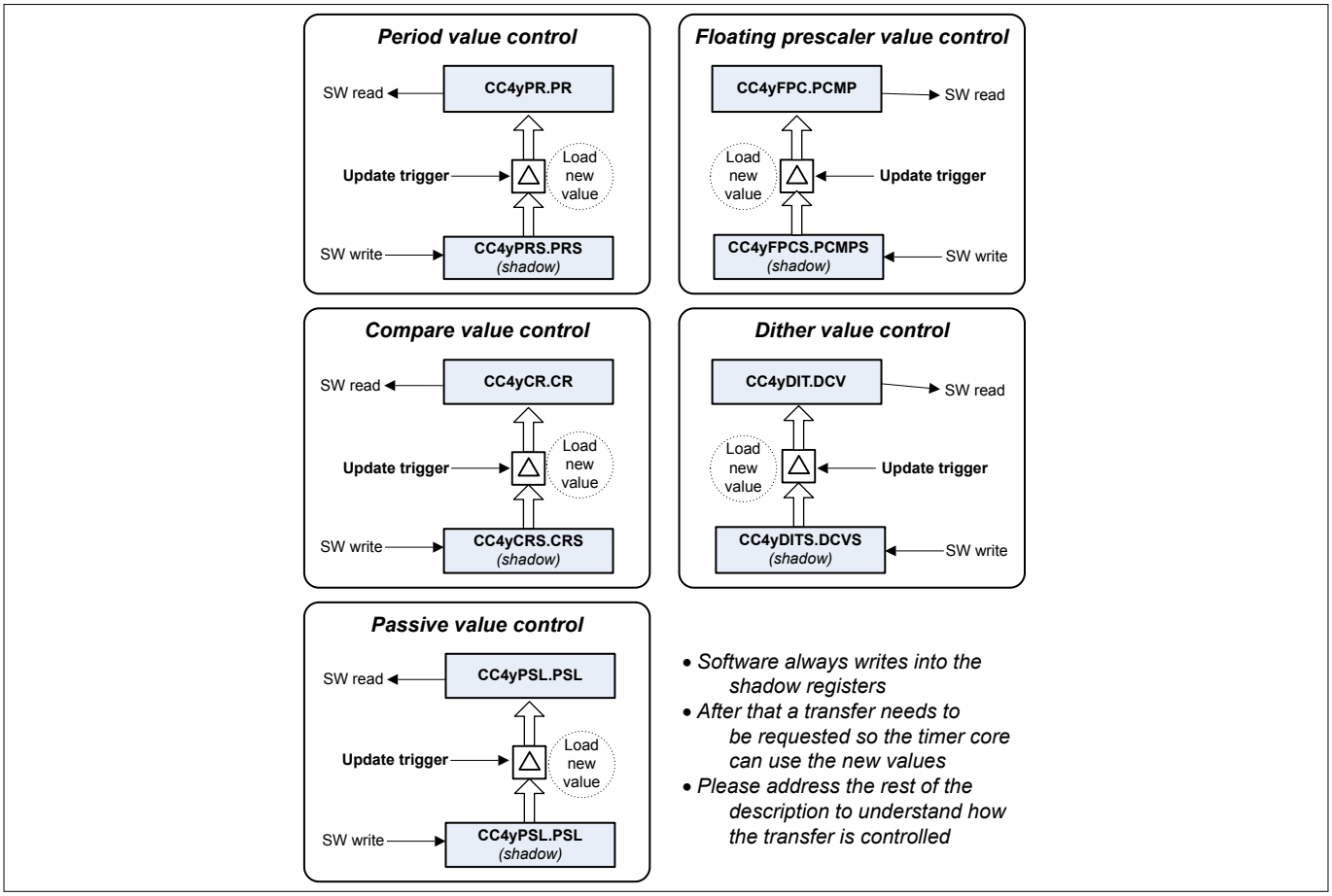


Figure 166 Shadow registers overview

The update of these registers can only be done by writing a new value into the associated shadow register and wait for a shadow transfer to occur - ***Figure 167***.

Each group of shadow registers have an individual shadow transfer enable bit. The software must set this enable bit to 1_B, whenever an update of the values is needed. These bits are automatically cleared by the hardware, when the update is done. Therefore every time that an update of the registers is needed the software must set again the specific bit(s).

Nevertheless it is also possible to clear the enable bit via software. This can be used in the case that an update of the values needs to be cancelled (after the enable bit has already been set).

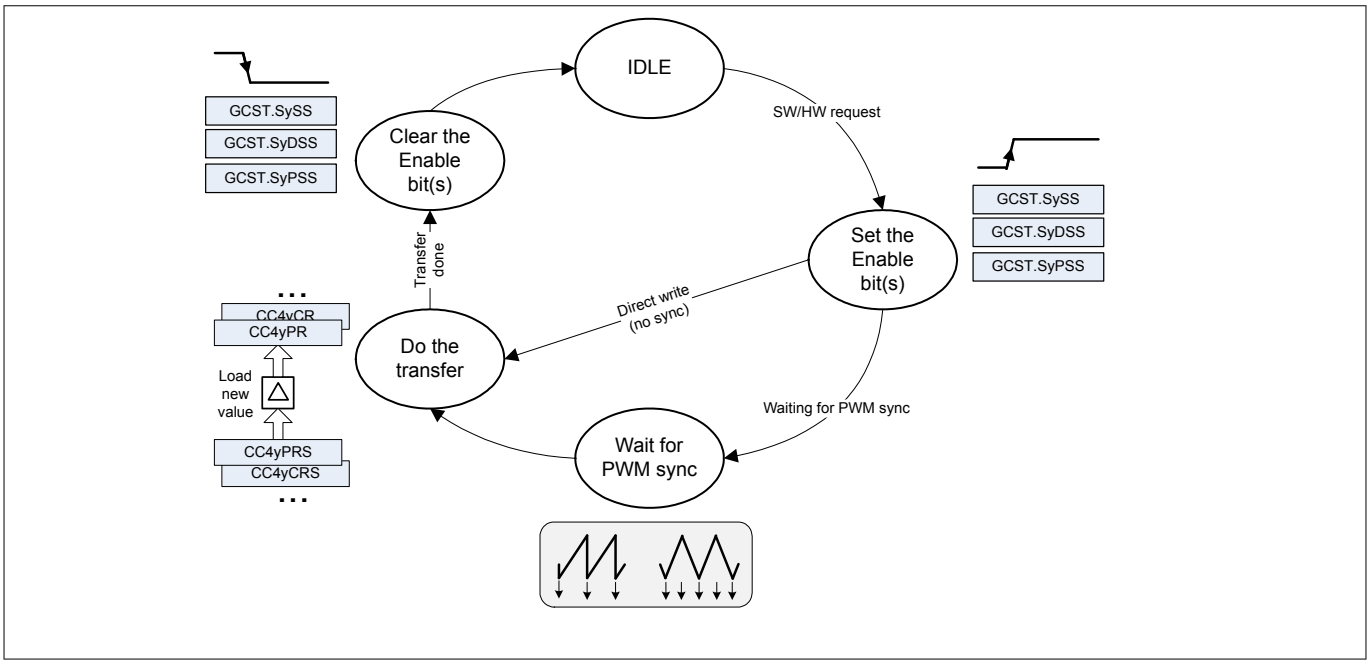


Figure 167 Shadow transfer state machine

The structure of the shadow transfer logic is depicted in ***Figure 168***. In this figure it can be seen the logic structure associated with each of the stages of the state machine - ***Figure 167***:

- In the request sources one can see that the shadow transfer can be requested by:
  - software by writing a 1_B into the specific bitfield in the GCST register
  - an automatic trigger that is configured in the ***CC4ySTC*** register, e.g. request an update every time that the period shadow register is modified
  - a hardware pin linked to the CCU4x.MCSS input (this is configured via the GCTRL.MSEy and GCTRL.MSDE fields)
- In the control logic is visible that after a shadow transfer request is issued, the associated bitfield is set, indicating that an update is pending
- There is also a stage where the user can configure how the update of the values is done (this is configured also via the ***CC4ySTC*** register):
  - synchronously with the PWM switching cycle
  - done immediately

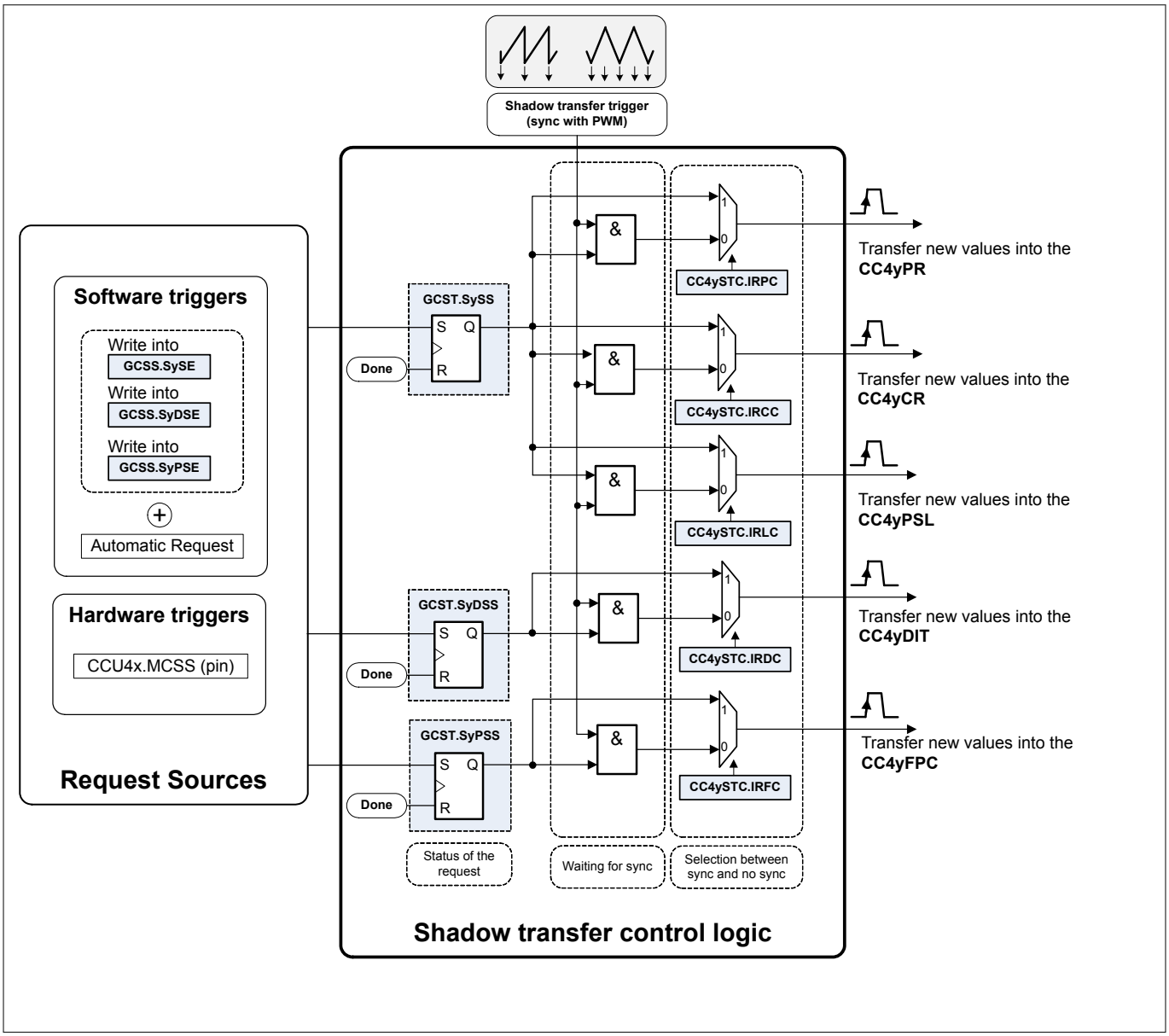


Figure 168 Shadow transfer enable logic

Updating the Shadow Registers

There are two major modes and two sub modes to update the shadow registers:

- Synchronously with the PWM switching cycle - major mode
- Immediate after an update request has been issued - major mode
- Automatic update request - sub mode
- Cascaded shadow transfer - sub mode

The following text will focus and describe each of these modes by the same order mentioned above. It is understood that the a sub mode can be used with any of the major modes.

- Synchronously with the PWM switching cycle

When the update of the registers is done synchronously with the PWM switching cycle, the shadow transfer operation is going to be done in the immediately next occurrence of a shadow transfer trigger, after the shadow transfer enable is set (***GCST***.SySS, ***GCST***.SyDSS, ***GCST***.SyPSS set to 1_B).

The occurrence of the shadow transfer trigger is imposed by the timer counting scheme (edge aligned or center aligned). Therefore the slots when the values are updated can be:

- in the next clock cycle after a Period Match while counting up - center aligned
- in the next clock cycle after an One Match while counting down - center aligned and edge aligned
- immediately, if the timer is stopped and the shadow transfer enable bit(s) is set - center aligned and edge aligned.

It is also possible to control in which slot the shadow transfer is done, via the STM field. This is only valid in Center Aligned Mode:

- ***CC4ySTC***.STM = 00_B (default) - Shadow transfer is done at the Period Match and One match slot
- ***CC4ySTC***.STM = 01_B - Shadow transfer is done only at the Period Match slot
- ***CC4ySTC***.STM = 10_B - Shadow transfer is done only at the One Match slot

Figure 169 shows an example of the shadow transfer control when the timer slice has been configured into center aligned mode. For a complete description of all the timer slice counting modes, please address ***Chapter 20.2.4.3***, ***Chapter 20.2.4.4*** and ***Chapter 20.2.4.5***.

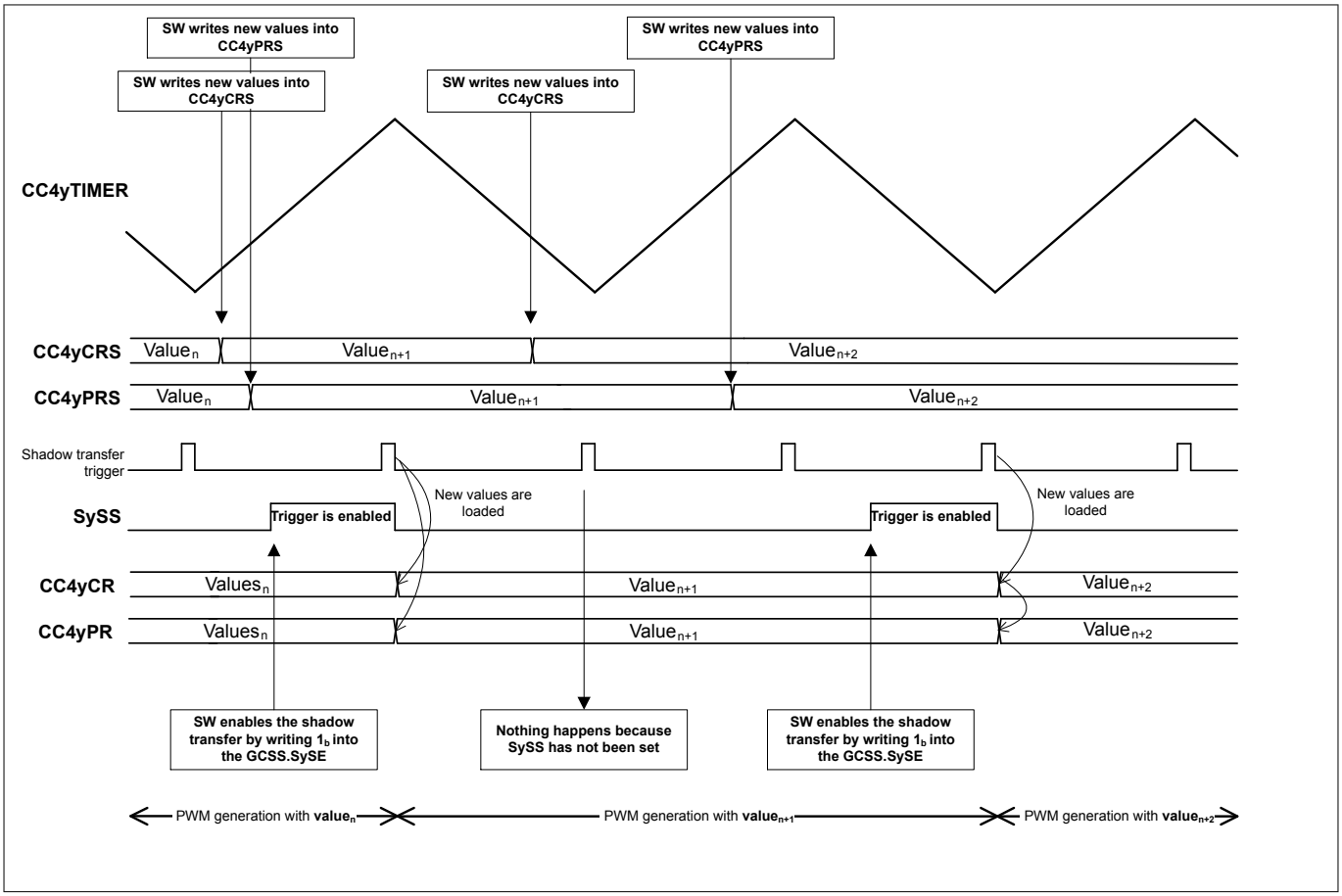


Figure 169 Shadow transfer timing example - center aligned mode with sync

- Immediate after an update request has been issued

In some applications it may be necessary to update the PWM conditions without waiting for a new switching cycle. When this is required, the user can configure via the ***CC4ySTC*** register, which fields/registers should be updated without waiting for a PWM synchronization (individual configuration fields exist for each parameter, e.g. period, compare, etc).

In ***Figure 170*** an example is depicted, of how the update of the period and compare registers can be done, without waiting for the normal switching cycle synchronization - ***CC4ySTC***.IRPC and ***CC4ySTC***.IRCC fields are both configured with 1_B.

The software writes new values into the period and compare shadow registers (CC4yPRS and CC4yCRS respectively). After doing that, the software requests an update of the current values being used by the timer kernel - by writing 1_B into the GCSS.SySE bitfield. Due to the fact that the software has configured the CC4ySTC

register to perform an immediate update, after the GCSS.SySE is written with 1_B, the hardware will automatically load and use the new values.

The request bit - SySS - is then cleared when the transfer is done. One should notice that all the depicted ***CC4ySTC*** configuration fields need to be set to 1_B for the request bit (SySS) to be cleared immediately. If one of these ***CC4ySTC*** configuration bitfields is configured with 0_B, then the associated value is updated coherently with the PWM signal - ***Figure 171***.

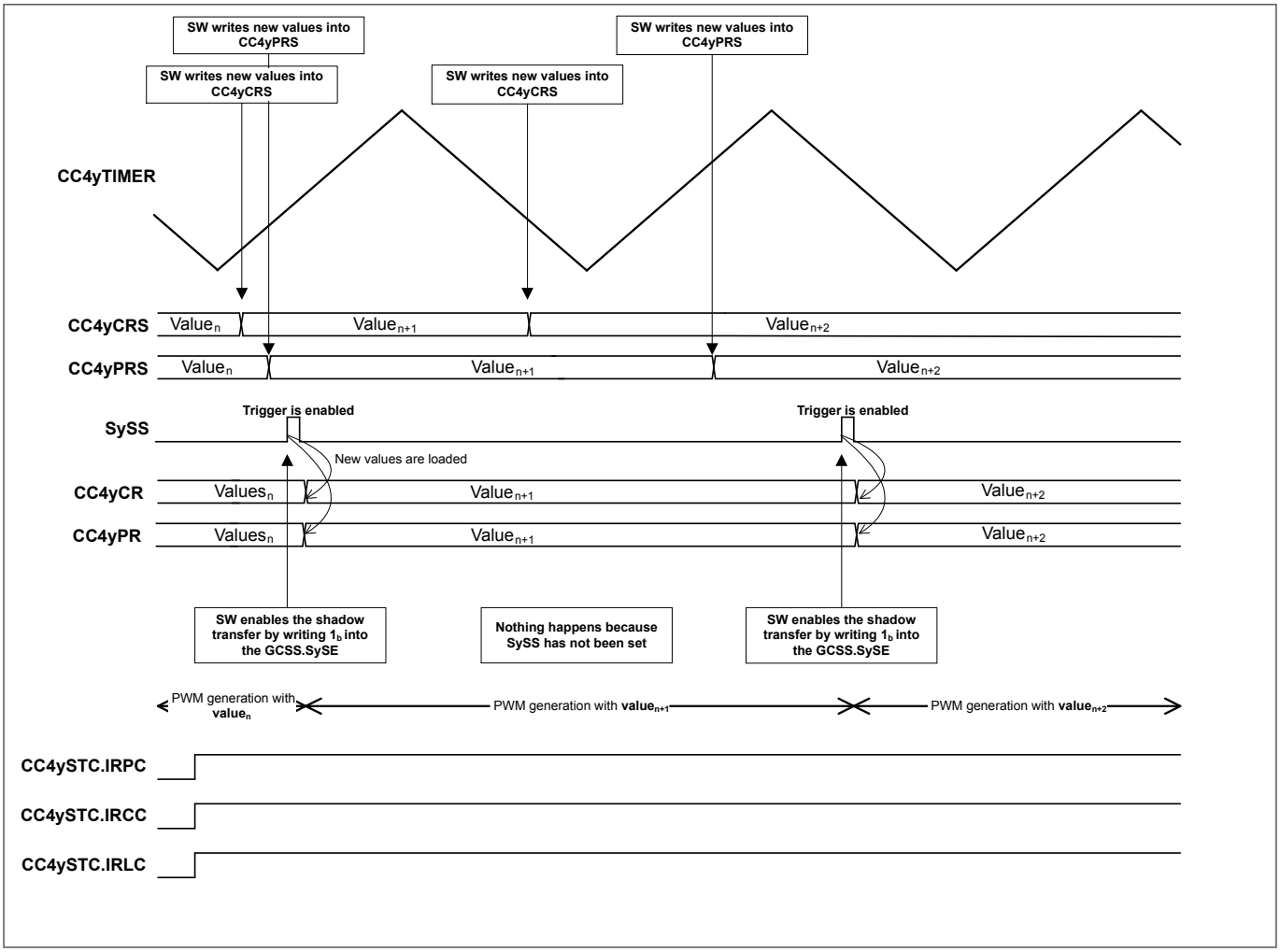


Figure 170 Shadow transfer timing example - center aligned mode without sync

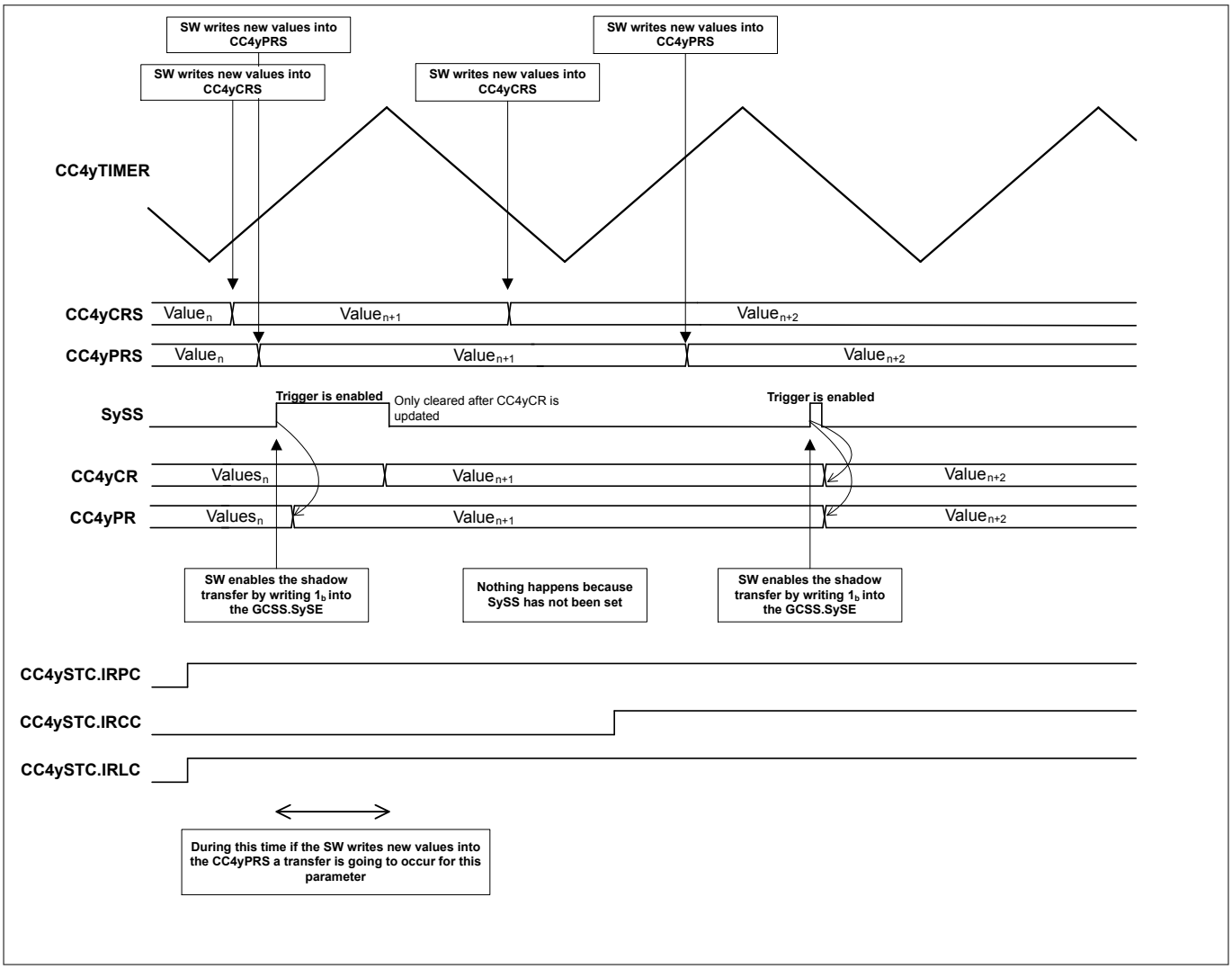


Figure 171 Shadow transfer timing example - dual configuration

- Automatic update request

Each timer slice offer also a possibility of enabling an automatic transfer request. This is configured in the ***CC4ySTC*** register (via the ASPC, ASCC, ASLC, ASDC fields). Enabling an automatic transfer request, signifies that after the software writes a value into a specific shadow register, the update of the current value is going to be automatically enabled by hardware. This means for example, that the software does not need to write a 1_B to the GCSS.SySE field after a new period value is loaded into the shadow register.

The operation of this sub mode can be seen in ***Figure 172*** - initially the software had configured the timer slice with an automatic request enable uppon the update of the period shadow register (ASPC is set to 1). One can see that after the update of the CC4yPRS (period shadow register) the SySS bitfield is automatically set by hardware, enabling a shadow transfer (in the second time slot the field ASCC is set to 1).

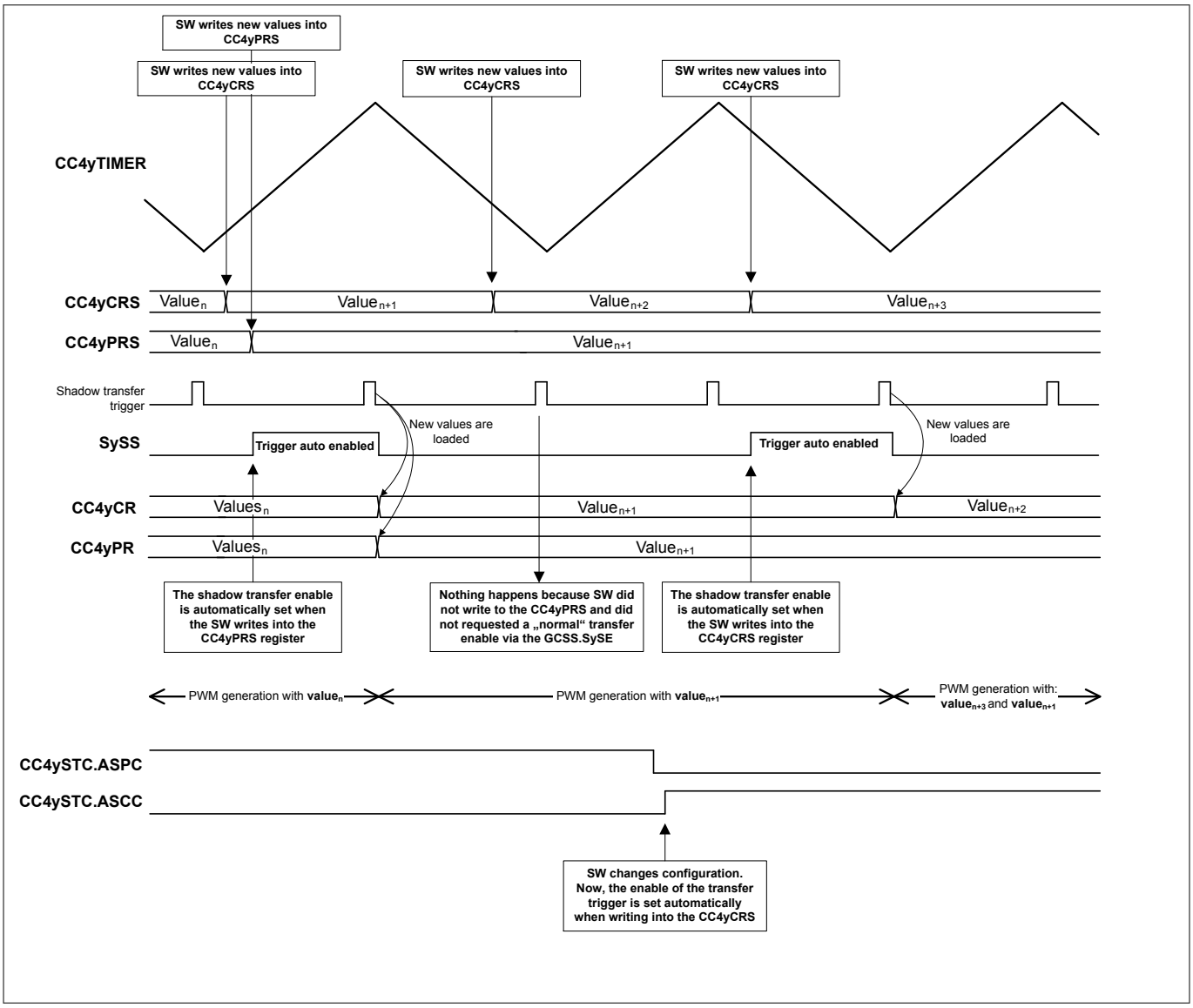


Figure 172 Shadow transfer timing example - center aligned mode with automatic request

- Cascaded Shadow Transfer

It is possible to cascade the shadow transfer operation throughout the CCU4 timer slices. The specific shadow transfer of a timer slice is cascaded with the adjacent timer slices, ***Figure 173*** .

To enable the cascaded shadow transfer function, the bitfield ***CC4ySTC***.CSE of the specific timer slice needs to be set to 1_B.

The shadow transfer enable bits, still need to be set via SW for each of the individual slices, ***Figure 174***.

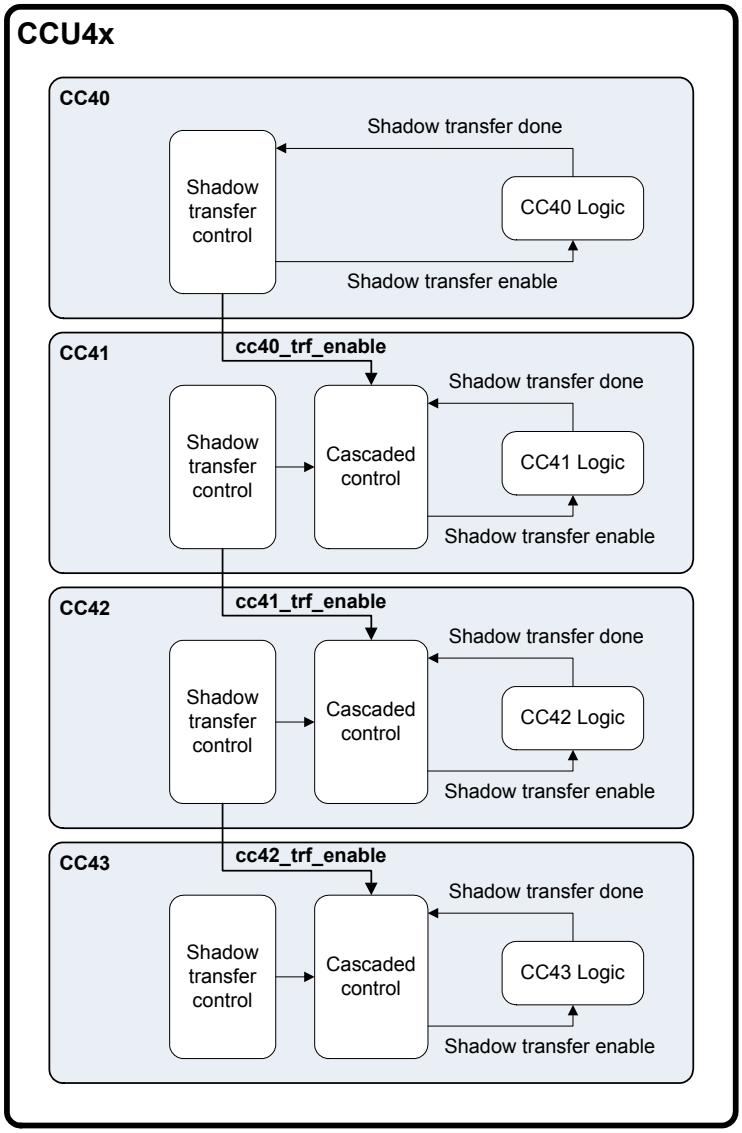


Figure 173 Cascaded shadow transfer linking

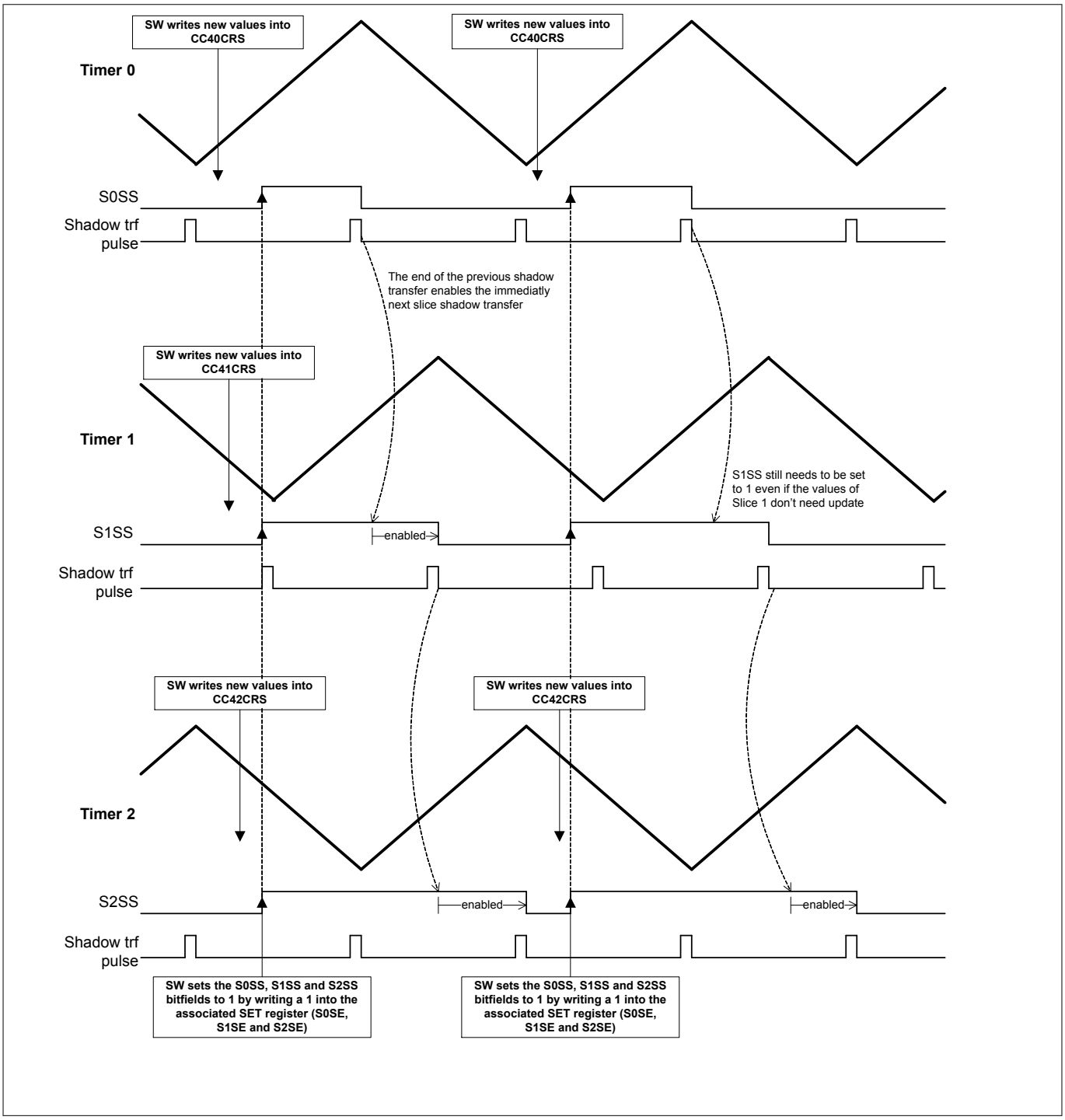


Figure 174 Cascade shadow transfer timing

Note: The shadow transfer enable bits - SySS, need to be set in all timer slices that are being used in the cascaded architecture, at the same time. The shadow transfer enable bits, also need to be set for all slices even if the shadow values of some slices were not updated.

20.2.4.8 PWM Active/Passive Rules

Like previously mentioned on ***Chapter 20.2.4.2***, each CCU4 timer slice has a status bit (CC4yST) that contains the current state of the timer comparison logic that is used to generate the output PWM signal.

The general rules that set or clear the associated timer slice status bit (CC4yST), can be generalized independently of the timer counting mode.

The following events set the Status bit (CC4yST) to Active:

- in the next f_{tclk} cycle after a compare match while counting up
- in the next f_{tclk} cycle after a zero match while counting down

The following events set the Status bit (CC4yST) to Inactive:

- in the next f_{tclk} cycle after a zero match (and not compare match) while counting up
- in the next f_{tclk} cycle after a compare match while counting down

If external events are being used to control the timer operation, these rules are still applicable.

The status bit state can only be 'override' via software or by the external status bit override function, ***Chapter 20.2.5.8***.

The software can at any time write a 1_B into the ***GCSS***.SySTS bitfield, which will set the status bit ***GCST***.CC4yST of the specific timer slice. Writing a 1_B into the ***GCSC***.SySTC bitfield will clear the specific status bit.

20.2.4.9 Output PWM Path

Each Timer Slice contains an output path, where the PWM output signal can be conditioned after the PWM status bit - CC4yST - ***Figure 175***. Inside the output path, the polarity of the PWM signal can be inverted in relation to the status bit. Each output path offers two types of outputs:

- CCU4x.OUTy - PWM signal from Timer Slice y that can be conditioning or inverted
- CCU4x.STy - PWM signal from Timer Slice y that mirrors the PWM status bit - CC4yST.

The conditioning of the output path has three sources:

- External Modulation - conditioning controlled by an external signal
- Multi-Channel Mode - conditioning controlled by a dedicated timer slice input that normally is used in Brushless DC Motor Control patterns
- TRAP State - highest level of conditioning that is controlled by an external function and is normally linked to a system fault, e.g. overcurrent protection

Each of these conditioning sources are explained in detailed in their dedicated section.

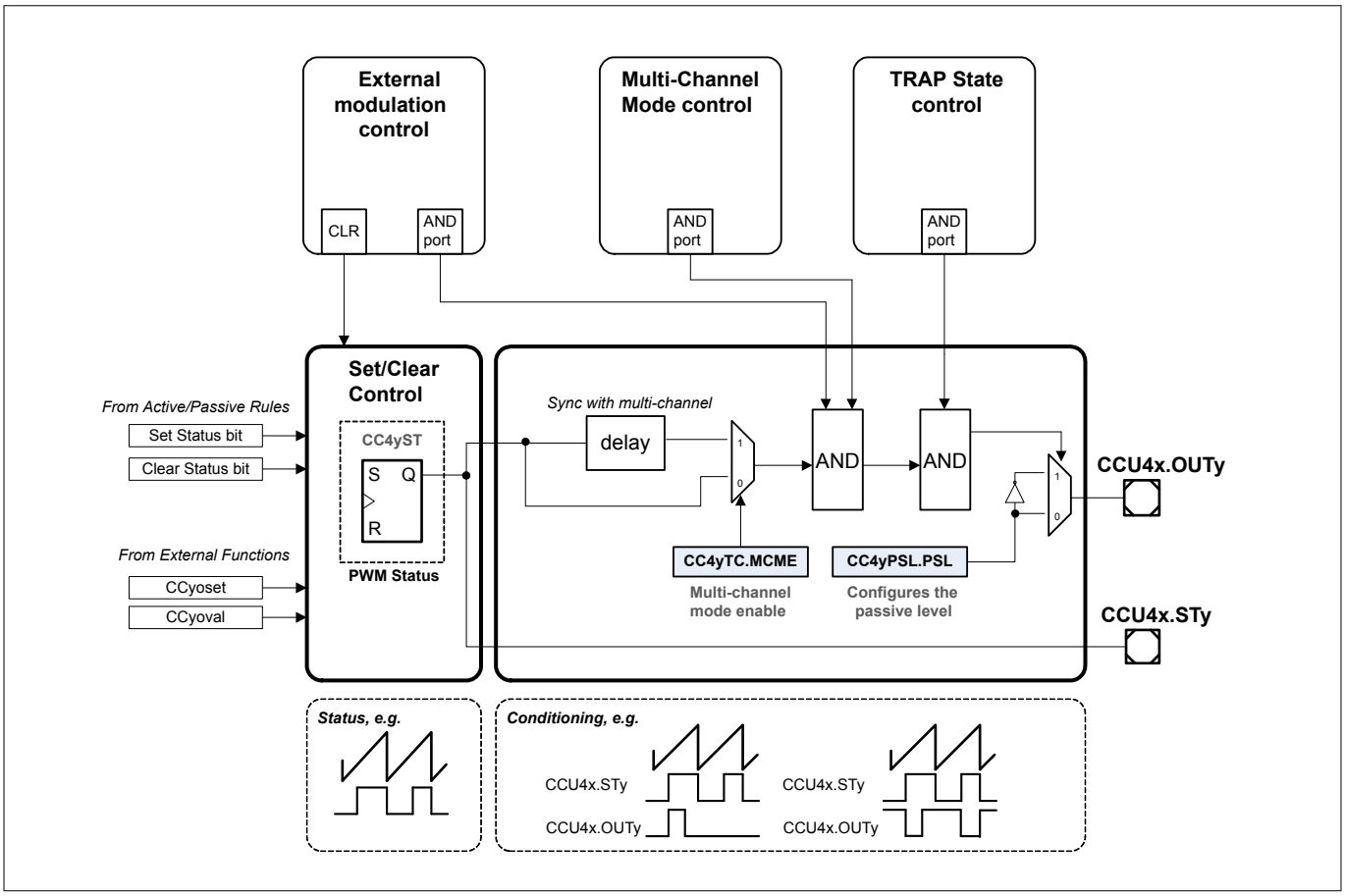


Figure 175 PWM output path

For more information to the functional blocks see the following links:

- ***External Modulation***
- ***Multi-Channel Control***
- ***TRAP Function***
- ***Status Bit Override***
- ***PWM Active/Passive Rules***

20.2.5 Timer Slice External Functions

Each CCU4 timer slice has the possibility of using up to three different input events, see ***Chapter 20.2.2***. These three events can then be mapped to Timer Slice functions (the full set of available functions is described at ***Chapter 20.2.3***)

These events can be mapped to any of the CCU4x.INy[BV:AA] inputs and there isn't any imposition that an event cannot be used to perform several functions, or that an input cannot be mapped to several events (e.g. input X triggers event 0 with rising edge and triggers event 1 with the falling edge).

20.2.5.1 External Start/Stop

To select an external start function, one should map one of the events (output of the input selector) to a specific input signal, by setting the required value in the ***CC4yINS1***.EVxIS field and indicating the active edge of the signal on the ***CC4yINS2***.EVxEM field.

This event should be then mapped to the start or stop functionality by setting the ***CC4yCMC***.STRTS (for the start) or the ***CC4yCMC***.ENDS (for the stop) with the proper value.

Notice that both start and stop functions are edge and not level active and therefore the active/passive configuration is set only by the ***CC4yINS2***.EVxEM.

The external stop by default just clears the run bit (***CC4yTCST***.TRB), while the start functions does the opposite. Nevertheless one can select an extended subset of functions for the external start and stop. This subset is controlled by the registers ***CC4yTC***.ENDM (for the stop) and ***CC4yTC***.STRM (for the start).

For the start subset (***CC4yTC***.STRM):

- sets the run bit/starts the timer (resume operation)
- clears the timer, sets the run bit/starts the timer (flush and start)

For the stop subset (***CC4yTC***.ENDM):

- clears the run/stops the timer (stop)
- clears the timer (flush)
- clears the timer, clears the run bit/stops the timer (flush and stop)

If in conjunction with an external start/stop (configured also/only as flush) and external up/down signal is used, during the flush operation the timer is going to be set to 0000_H if the actual counting direction is up or set with the value of the period register if the counting direction is down.

Figure 176 to ***Figure 179*** shows the usage of two signals to perform the start/stop functions in all the previously mentioned subsets. External Signal(1) acts as an active HIGH start signal, while External Signal(2) is used as an active HIGH stop function.

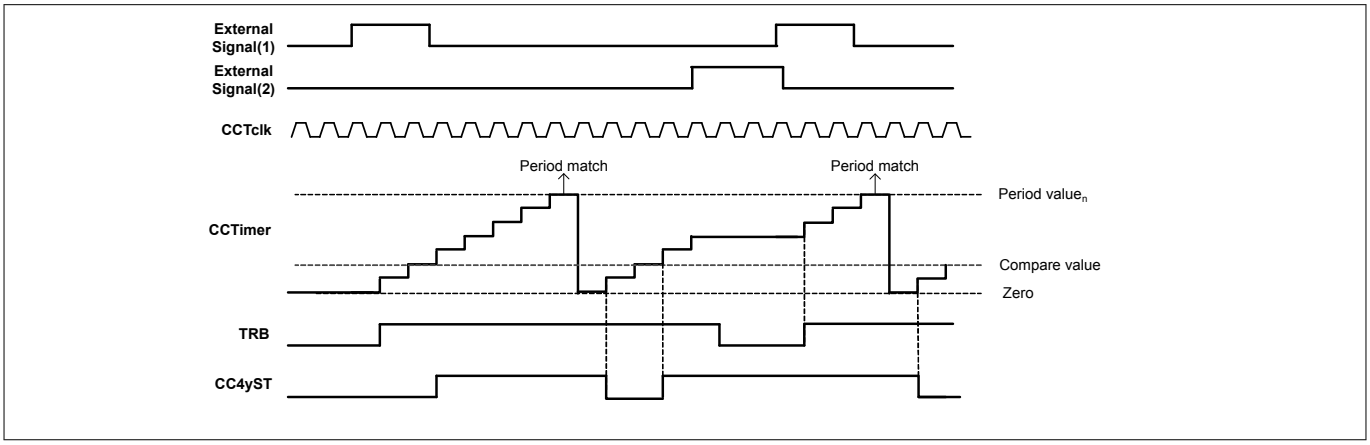


Figure 176 Start (as start)/ stop (as stop) - *CC4yTC*.STRM = 0, *CC4yTC*.ENDM = 00

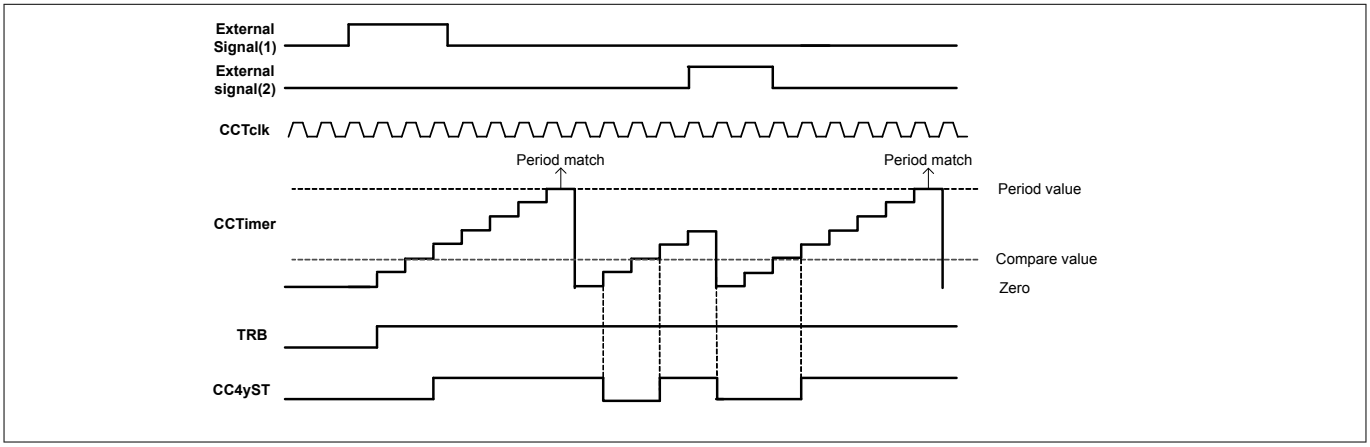


Figure 177 Start (as start)/ stop (as flush) - *CC4yTC*.STRM = 0, *CC4yTC*.ENDM = 01

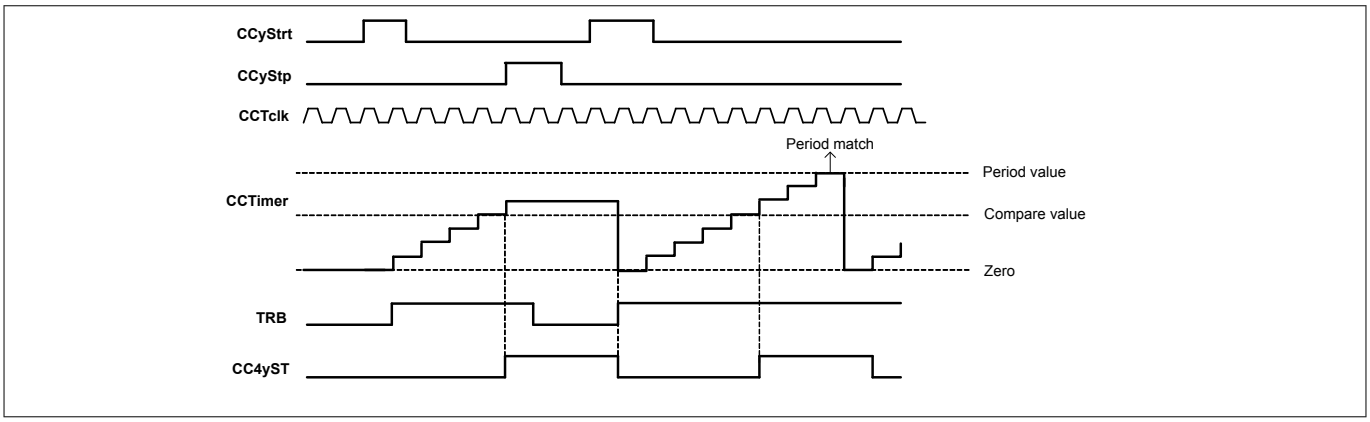


Figure 178 Start (as flush and start)/ stop (as stop) - *CC4yTC*.STRM = 1, *CC4yTC*.ENDM = 00

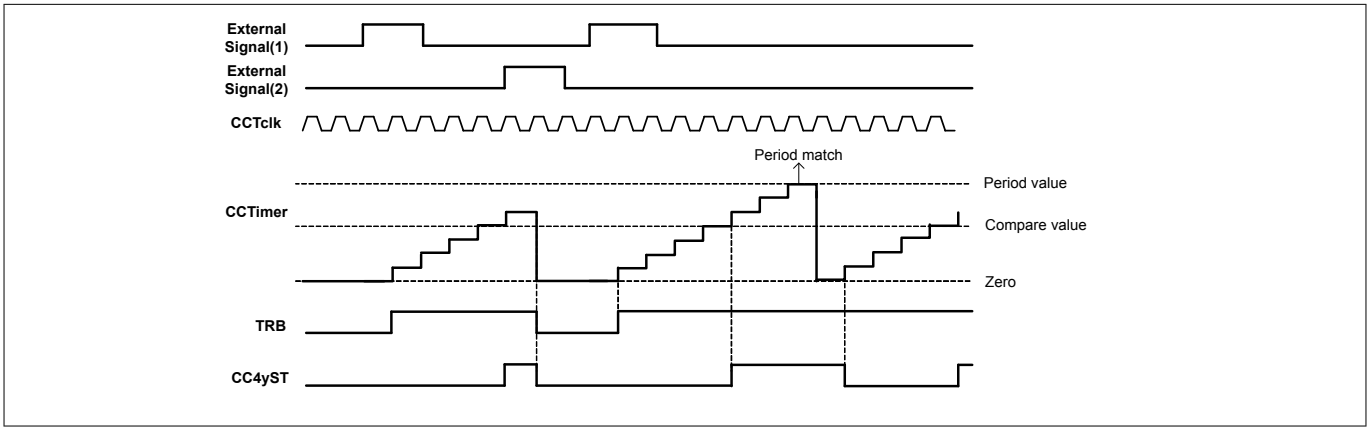


Figure 179 Start (as start)/ stop (as flush and stop) - *CC4yTC*.STRM = 0, *CC4yTC*.ENDM = 10

20.2.5.2 External Counting Direction

There is the possibility of selecting an input signal to act as increment/decrement control.

To select an external up/down control, one should map one of the events (output of the input selector) to a specific input signal, by setting the required value in the ***CC4yINS1***.EVxIS field and indicating the active level of the signal on the ***CC4yINS2***.EVxLM. This event should be then mapped to the up/down functionality by setting ***CC4yCMC***.UDS with the proper value.

Notice that the up/down function is level active and therefore the active/passive configuration is set only by the ***CC4yINS2***.EVxLM.

The status bit of the slice (CC4yST) is always set when the timer value is equal or greater than the value stored in the compare register, see ***Chapter 20.2.4.8***.

The update of the period and compare register values is done when:

- with the next clock after a period match, while counting up (***CC4yTCST***.CDIR = 0_B)
- with the next clock after a one match, while counting down (***CC4yTCST***.CDIR = 1_B)

The value of the ***CC4yTCST***.CDIR register is updated accordingly with the changes on the decoded event. Using an external signal to perform the up/down counting function and configuring the event as active LOW means that the timer is counting up when the signal is HIGH and counting down when LOW (this is to match the CDIR value).

Figure 180 shows an external signal being used to control the counting direction of the time. This signal was selected as active HIGH, which means that the timer is counting down while the signal is HIGH and counting up when the signal is LOW.

*Note: For a signal that should impose an increment when LOW and a decrement when HIGH, the user needs to set the **CC4yINS2**.EVxLM = 0_B. When the operation is switched, then the user should set **CC4yINS2**.EVxLM = 1_B.*

Note: Using an external counting direction control, sets the slice in edge aligned mode.

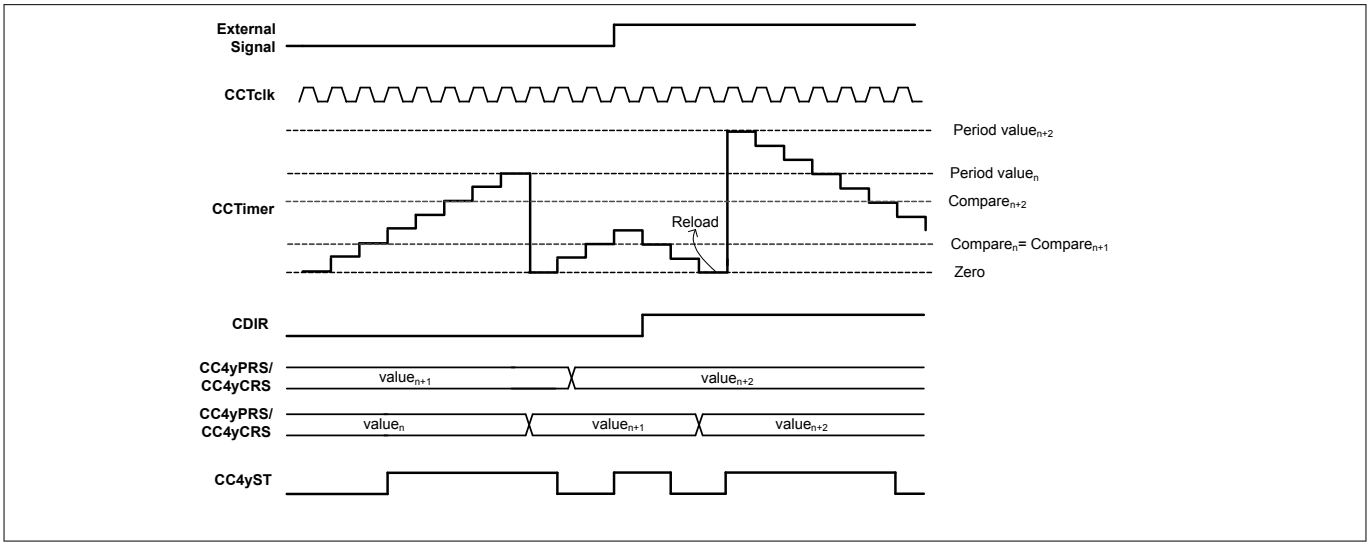


Figure 180 External counting direction

20.2.5.3 External Gating Signal

For pulse measurement, the user has the possibility of selecting an input signal that operates as counting gating.

To select an external gating control, one should map one of the events (output of the input selector) to a specific input signal, by setting the required value in the **CC4yINS1**.EVxIS register and indicating the active level of the signal on the **CC4yINS2**.EVxLM register. This event should be then mapped to the gating functionality by setting the **CC4yCMC**.GATES with the proper value.

Notice that the gating function is level active and therefore the active/passive configuration is set only by the **CC4yINS2**.EVxLM.

The status bit during an external gating signal continues to be asserted when the compare value is reached and deasserted when the counter reaches 0000_H. One should note that the counter continues to use the period register to identify the wrap around condition. ***Figure 181*** shows the usage of an external signal for gating the slice counter. The signal was set as active LOW, which means the counter gating functionality is active when the external value is zero.

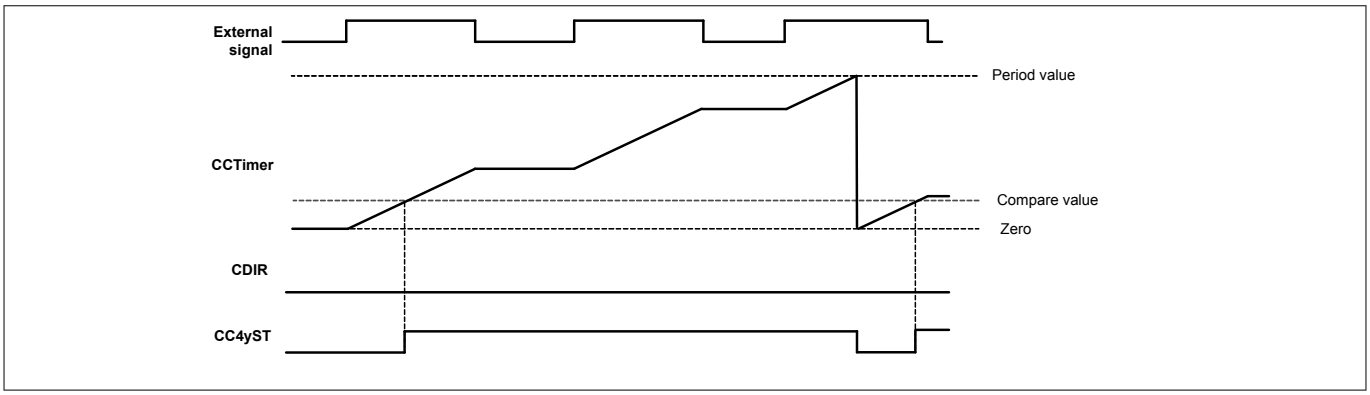


Figure 181 External gating

For any type of usage of the external gating function, the specific run bit of the Timer Slice, ***CC4yTCST***.TRB, needs to be set. This can be done via an additional external signal or directly via software.

20.2.5.4 External Count Signal

There is also the possibility of selecting an external signal to act as the counting event.

To select an external counting, one should map one of the events (output of the input selector) to a specific input signal, by setting the required value in the ***CC4yINS1***.EVxIS register and indicating the active edge of the signal on the ***CC4yINS2***.EVxEM register. This event should be then mapped to the counting functionality by setting the ***CC4yCMC***.CNTS with the proper value.

Notice that the counting function is edge active and therefore the active/passive configuration is set only by the ***CC4yINS2***.EVxEM.

One can select the rising, falling or both edges to perform a count. On ***Figure 182***, the external signal was selected as a counter event for both falling and rising edges. Wrap around condition is still applied with a comparison with the period register.

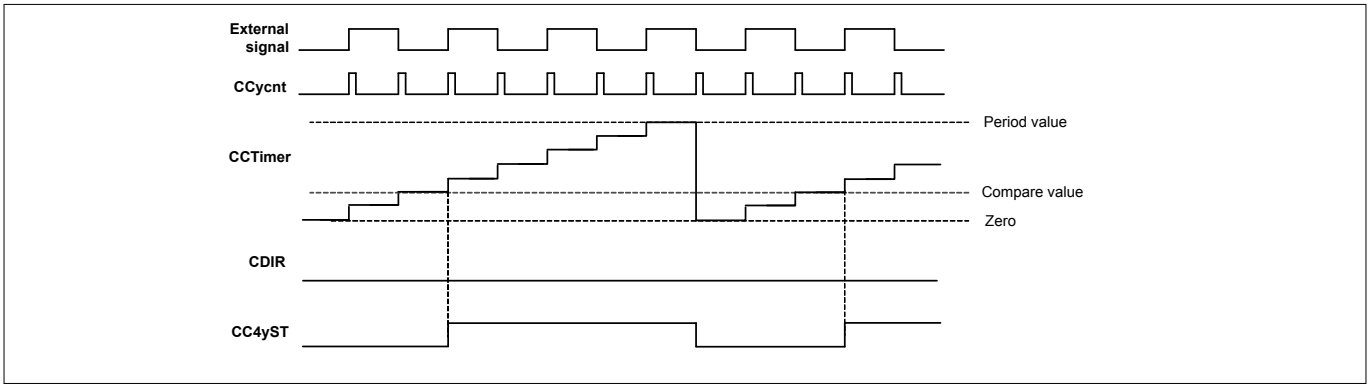


Figure 182 External count

For any type of usage of the external gating function, the specific run bit of the Timer Slice, ***CC4yTCST***.TRB, needs to be set. This can be done via an additional external signal or directly via software.

20.2.5.5 External Load

Each slice of the CCU4 also has a functionality that enables the user to select an external signal as trigger for reloading the value of the timer with the current value of the compare register (if ***CC4yTCST***.CDIR = 0) or with the value of the period register (if ***CC4yTCST***.CDIR = 1).

To select an external load signal, one should map one of the events (output of the input selector) to a specific input signal, by setting the required value in the ***CC4yINS1***.EVxIS register and indicating the active edge of the

signal on the ***CC4yINS2***.EVxEM register. This event should be then mapped to the load functionality by setting the ***CC4yCMC***.LDS with the proper value.

Notice that the load function is edge active and therefore the active/passive configuration is set only by the ***CC4yINS2*** .EVxEM.

On ***Figure 183***, the external signal (1) was used to act as a load trigger, active on the rising edge. Every time that a rising edge on external signal (1) is detected, the timer value is loaded with the value present on the compare register. If an external signal is being used to control the counting direction, up or down, the timer value can be loaded also with the value set in the period register. The External signal (2) represents the counting direction control (active HIGH). If at the moment that a load trigger is detected, the signal controlling the counting direction is imposing a decrement, then the value set in the timer is the period value.

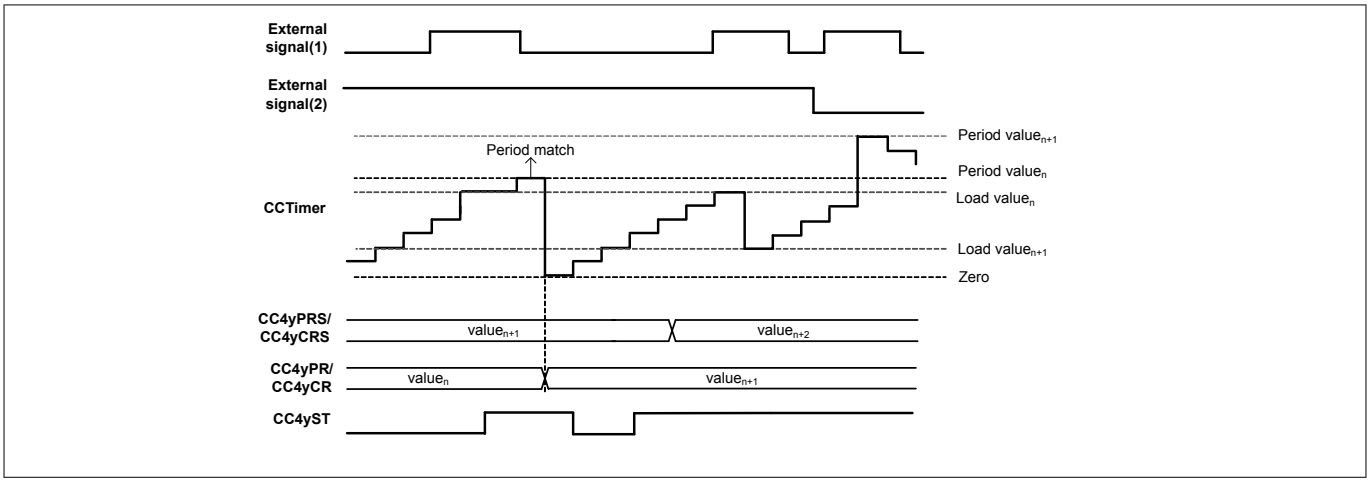


Figure 183 External load

20.2.5.6 External Capture

When selecting an external signal to be used as a capture trigger (if ***CC4yCMC***.CAP0S or ***CC4yCMC***.CAP1S are different from 0_H), the user is automatically setting the specific slice into capture mode.

In capture mode the user can have up to four capture registers, see ***Figure 186***: capture register 0 (***CC4yC0V***), capture register 1 (***CC4yC1V***), capture register 2 (***CC4yC2V***) and capture register 3 (***CC4yC3V***).

These registers are shared between compare and capture modes which imposes:

- if ***CC4yC0V*** and ***CC4yC1V*** are used for capturing, the compare registers ***CC4yCR*** and ***CC4yCRS*** are not available (no compare channel)
- if ***CC4yC2V*** and ***CC4yC3V*** are used for capturing, the period registers ***CC4yPR*** and ***CC4yPRS*** are not available (no period control)

To select an external capture signal, one should map one of the events (output of the input selector) to a specific input signal, by setting the required value in the ***CC4yINS1***.EVxIS register and indicating the active edge of the signal on the ***CC4yINS2***.EVxEM register. This event should be then mapped to the capture functionality by setting the ***CC4yCMC***.CAP0S/***CC4yCMC***.CAP1S with the proper value.

Notice that the capture function is edge active and therefore the active/passive configuration is set only by the ***CC4yINS2***.EVxEM.

The user has the possibility of selecting the following capture schemes:

- Different capture events for ***CC4yC0V***/***CC4yC1V*** and ***CC4yC2V***/***CC4yC3V***
- The same capture event for ***CC4yC0V***/***CC4yC1V*** and ***CC4yC2V***/***CC4yC3V*** with the same capture edge. For this capture scheme, only the CCcapt1 functionality needs to be programmed. To enable this scheme, the field ***CC4yTC***.SCE needs to be set to 1.

Different Capture Events (SCE = 0_B)

Every time that a capture trigger 1 occurs, CCcapt1, the actual value of the timer is captured into the capture register 3 and the previous value stored in this register is transferred into capture register 2.

Every time that a capture trigger 0 occurs, CCcapt0, the actual value of the timer is captured into the capture register 1 and the previous value stored in this register is transferred into capture register 0.

Every time that a capture procedure into one of the registers occurs, the respective full flag is set. This flag is cleared automatically by HW when the SW reads back the value of the capture register (by reading the specific capture register or by reading the extended capture read value, see ***Chapter 20.2.6.4***).

The capture of a new value into a specific capture registers is dictated by the status of the full flag as follows:

$$CC4yC1V_{capt} = NOT(CC4yC1V_{full_flag} \text{ AND } CC4yC0V_{full_flag})$$

Equation 30

$$CC4yC0V_{capt} = CC4yC1V_{full_flag} \text{ AND } NOT(CC4yC0V_{full_flag})$$

Equation 31

It is also possible to disable the effect of the full flags reset by setting the ***CC4yTC***.CCS = 1_B. This enables a continuous capturing independent if the values captured have been read or not.

*Note: When using the period registers for capturing, **CC4yCMC**.CAP1S different from 00_B, the counter always uses its full 16 bit width as period value.*

On ***Figure 184***, an external signal was selected as an event for capturing the timer value into the ***CC4yC0V***/***CC4yC1V*** registers. The status bit, CC4yST, during capture mode is asserted whenever a capture trigger is detected and deasserted when the counter matches 0000_H.

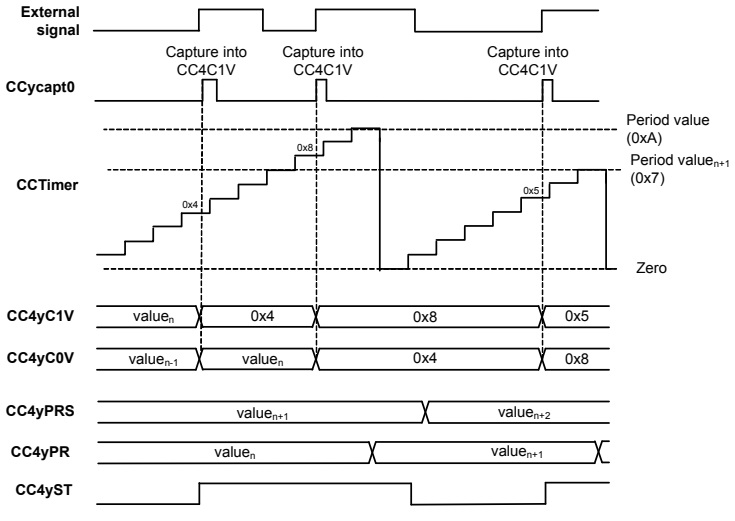


Figure 184 External capture - *CC4yCMC*.CAP0S = 00_B, *CC4yCMC*.CAP1S = 00_B

On ***Figure 185***, two different signals were used as source for capturing the timer value into the ***CC4yC0V***/***CC4yC1V*** and ***CC4yC2V***/***CC4yC3V*** registers.

External signal(1) was selected as rising edge active capture source for ***CC4yC0V***/***CC4yC1V***. External signal(2) was selected has the capture source for ***CC4yC2V***/***CC4yC3V***, but as opposite to the external signal(1), the active edge was selected has falling.

See ***Chapter 20.2.8.4***, for a capture mode usage description.

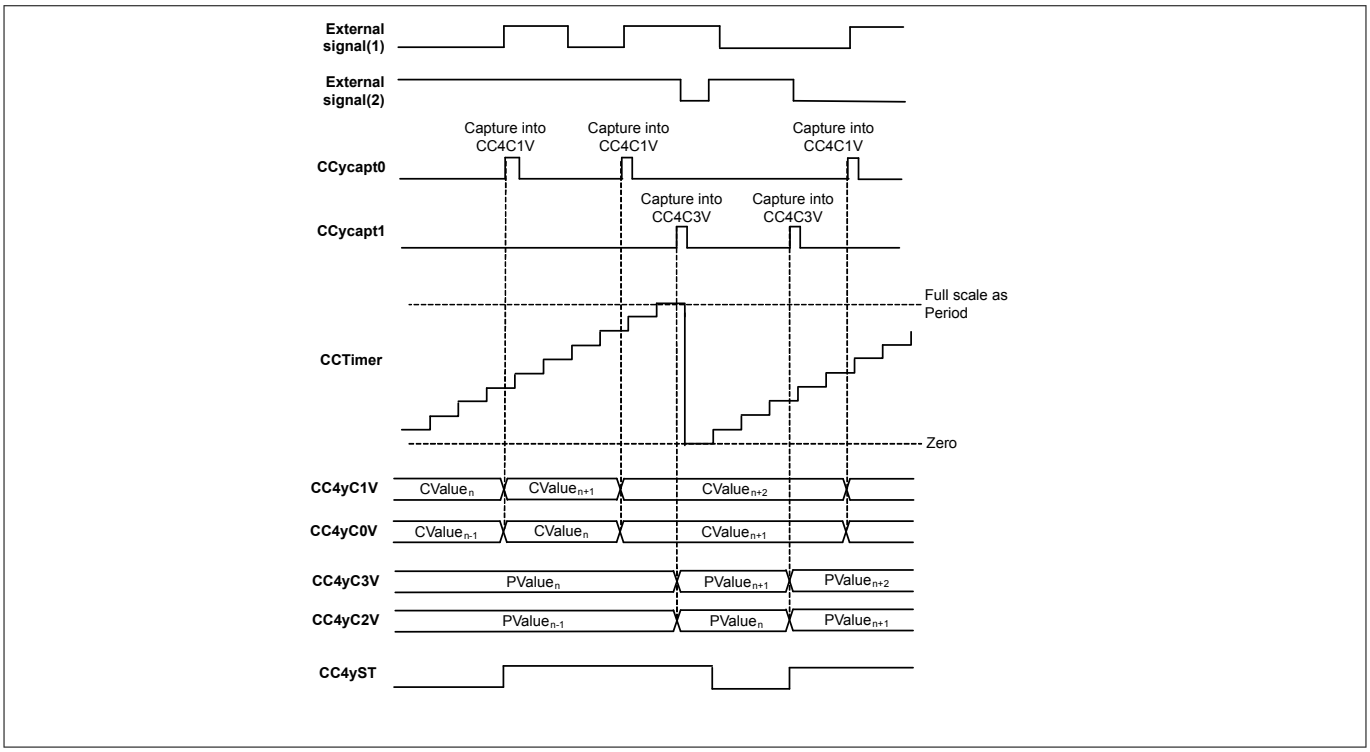


Figure 185 External capture - *CC4yCMC*.CAP0S = 00_B, *CC4yCMC*.CAP1S = 00_B

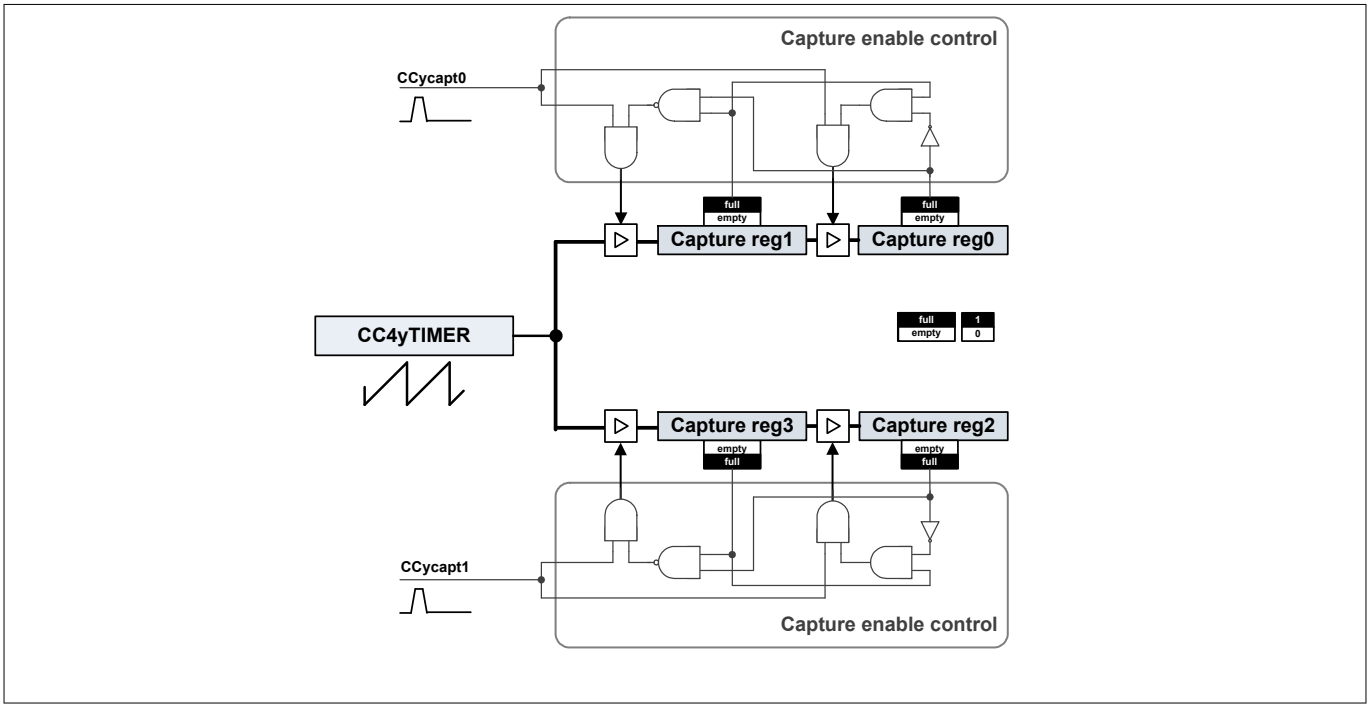


Figure 186 Slice capture logic

Same Capture Event (SCE = 1_B)

Setting the field ***CC4yTC***.SCE = 1_B, enables the possibility of having 4 capture registers linked with the same capture event, ***Figure 188***. The function that controls the capture is the CCcapt1.

The capture logic follows the same structure shown in Figure 21-37 but extended to a four register chain, see Figure 21-38. The same full flag lock rules are applied to the four register chain (it also can be disabled by setting the ***CC4yTC***.CCS = 1):

$$CC4yC3V_{capt} = NOT(CC4yC3V_{full_flag} \text{ AND } CC4yC2V_{full_flag} \text{ AND } CC4yC2V_{full_flag} \text{ AND } CC4yC1V_{full_flag})$$

Equation 32

$$CC4yC2V_{capt} = CC4yC3V_{full_flag} \text{ AND } NOT(CC4yC2V_{full_flag} \text{ AND } CC4yC1V_{full_flag} \text{ AND } CC4yC0V_{full_flag})$$

Equation 33

$$CC4yC1V_{capt} = CC4yC2V_{full_flag} \text{ AND } NOT(CC4yC1V_{full_flag} \text{ AND } CC4yC0V_{full_flag})$$

Equation 34

$$CC4yC0V_{capt} = CC4yC1V_{full_flag} \text{ AND } NOT(CC4yC0V_{full_flag})$$

Equation 35

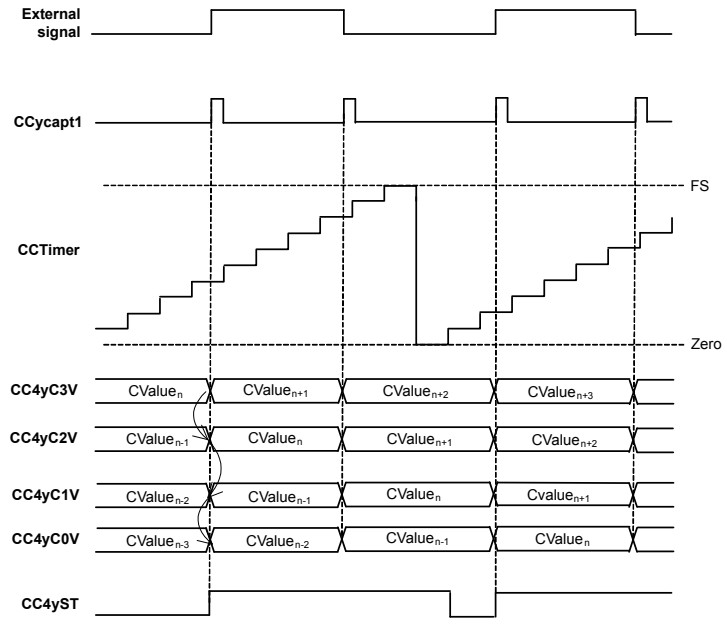


Figure 187 External Capture - *CC4yTC*.SCE = 1

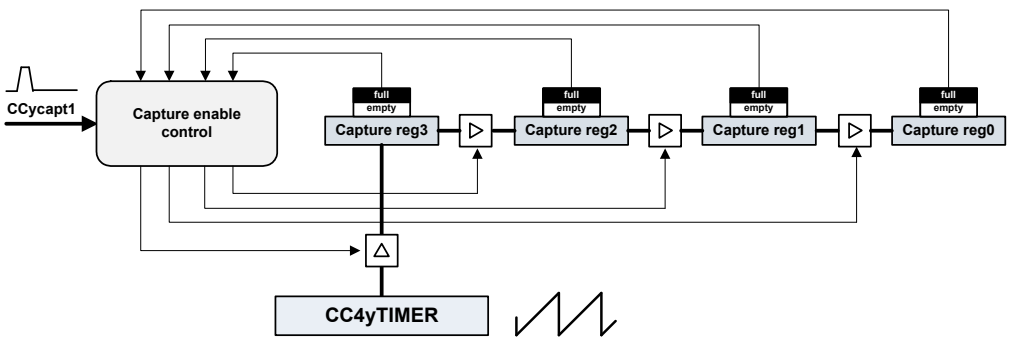


Figure 188 Slice Capture Logic - *CC4yTC*.SCE = 1

20.2.5.7 TRAP Function

The TRAP functionality allows the PWM outputs to react on the state of an input pin. This functionality can be used to switch off the power devices if the TRAP input becomes active.

To select the TRAP functionality, one should map one of the input signals to event number 2, by setting the required value in the ***CC4yINS1***.EV2IS register and indicating the active level of the signal on the ***CC4yINS2***.EV2LM register. This event should be then mapped to the trap functionality by setting the ***CC4yCMC***.TS = 1_B.

Notice that the trap function is level active and therefore the active/passive configuration is set only by the ***CC4yINTS***.EV2LM.

There are two bitfields that can be monitored via software to crosscheck the TRAP function, ***Figure 189***:

- The TRAP state bit, ***CC4yINTS***.E2AS. This bitfield if the TRAP is currently active or not. This bitfield is therefore setting the specific Timer Slice output, into ACTIVE or PASSIVE state.
- The TRAP Flag, ***CC4yINTS***.TRPF. This bitfield is used as a remainder in the case that the TRAP condition is cleared automatically via hardware. This field needs to be cleared by the software.

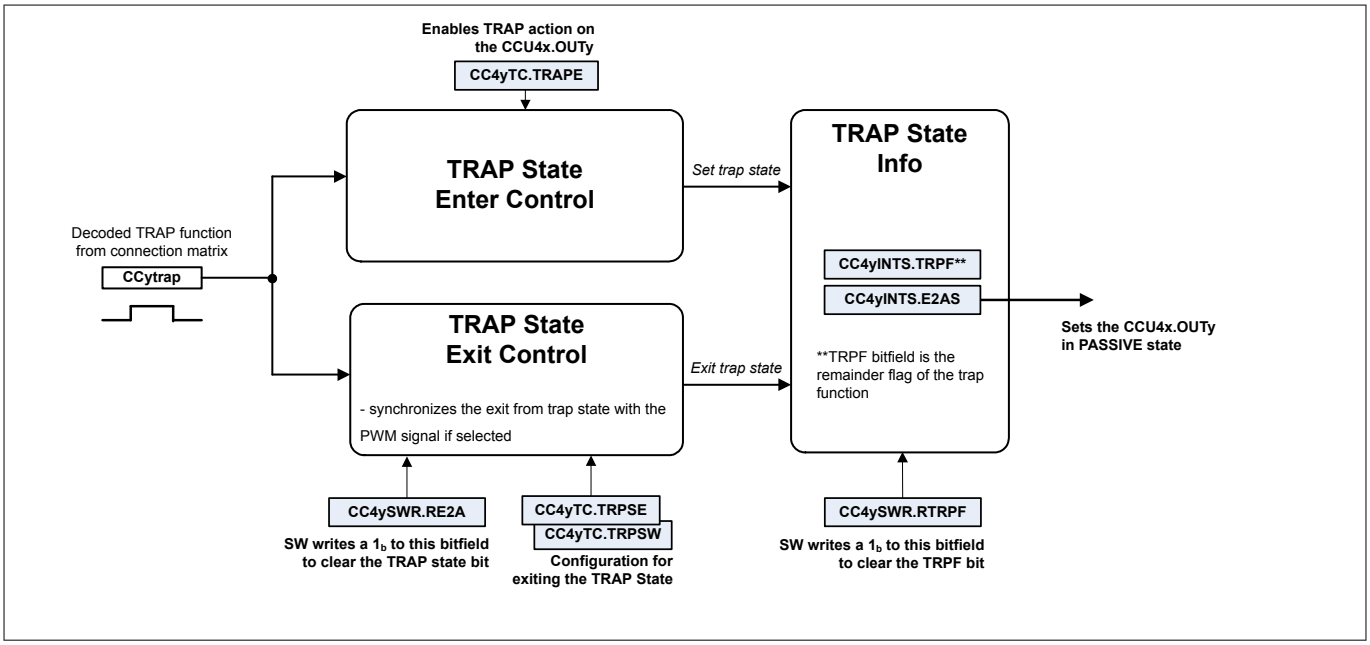


Figure 189 Trap control diagram

When a TRAP condition is detected at the selected input pin, both the Trap Flag and the Trap State bit are set to 1_B. The Trap State is entered immediately, by setting the CCU4xOUTy into the programmed PASSIVE state, ***Figure 190***.

Exiting the Trap State can be done in two ways (***CC4yTC***.TRPSW register):

- automatically via HW, when the TRAP signal becomes inactive - ***CC4yTC***.TRPSW = 0_B
- by SW only, by clearing the ***CC4yINTS***.E2AS. The clearing is only possible if the input TRAP signal is in inactive state - ***CC4yTC***.TRPSW = 1_B

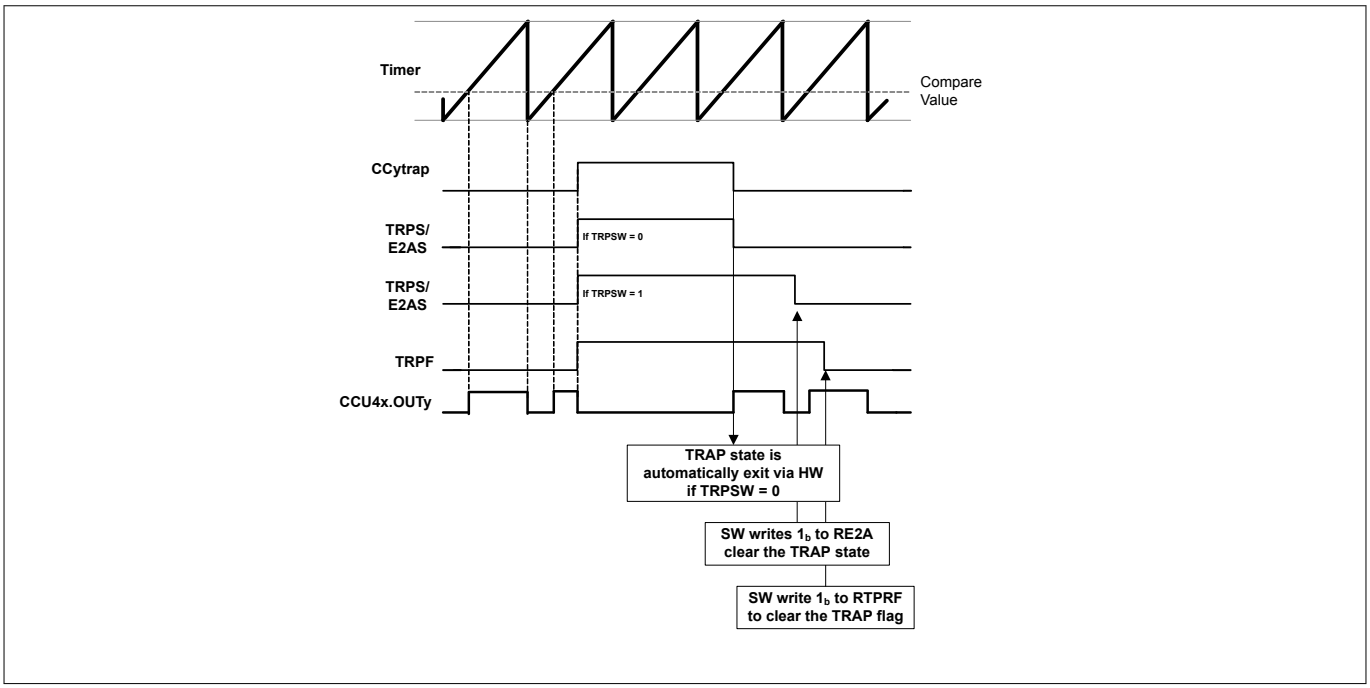


Figure 190 Trap timing diagram, *CC4yPSL*.PSL = 0_B (output passive level is 0_B)

It is also possible to synchronize the exiting of the TRAP state with the PWM signal, ***Figure 191***. This function is enabled when the bitfield ***CC4yTC***.TRPSE = 1_B.

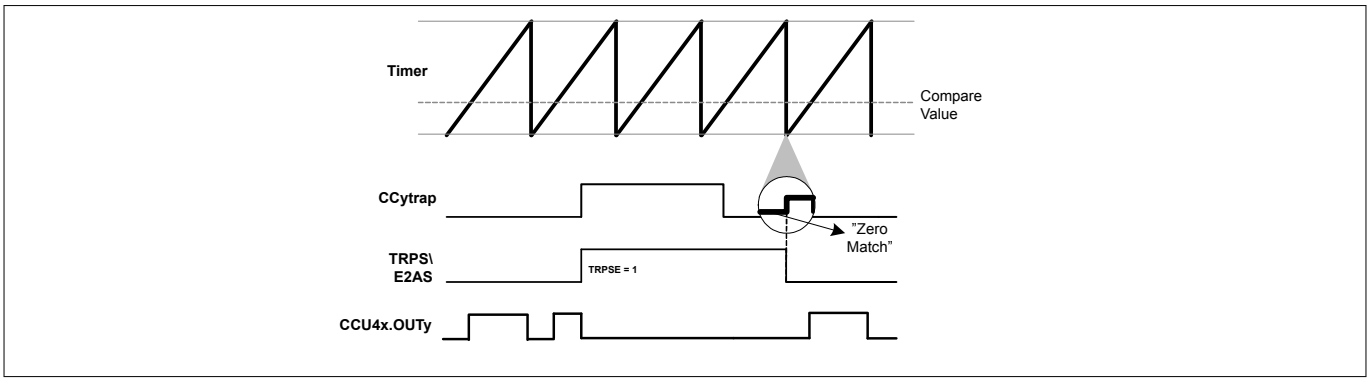


Figure 191 Trap synchronization with the PWM signal, *CC4yTC*.TRPSE = 1_B

20.2.5.8 Status Bit Override

For complex timed output control, each Timer Slice has a functionality that enables the override of the status bit (CC4yST) with a value passed trough an external signal.

The override of the status bit, can then lead to a change on the output pin, CCU4xOUTy (from inactive to active or vice versa).

To enable this functionality, two signals are needed:

- One signal that acts as a trigger to override the status bit (edge active)
- One signal that contains the value to be set in the status bit (level active)

To use the status bit override functionality, one should map the signal that acts as trigger to the event number 1, by setting the required value in the ***CC4yINS1***.EV1IS register and indicating the active edge of the signal on the ***CC4yINS2***.EV1EM register.

The signal that carries the value to be set on the status bit, needs to be mapped to the event number 2, by setting the required value in the ***CC4yINS1***.EV2IS register. The ***CC4yINS2***.EV2LM register should be set to 0_B if no inversion on the signal is needed and to 1_B otherwise.

The events should be then mapped to the status bit functionality by setting the ***CC4yCMC***.OFS = 1_B.

Figure 192 shows the functionality of the status bit override, when the external signal(1) was selected as trigger source (rising edge active) and the external signal(2) was selected as override value.

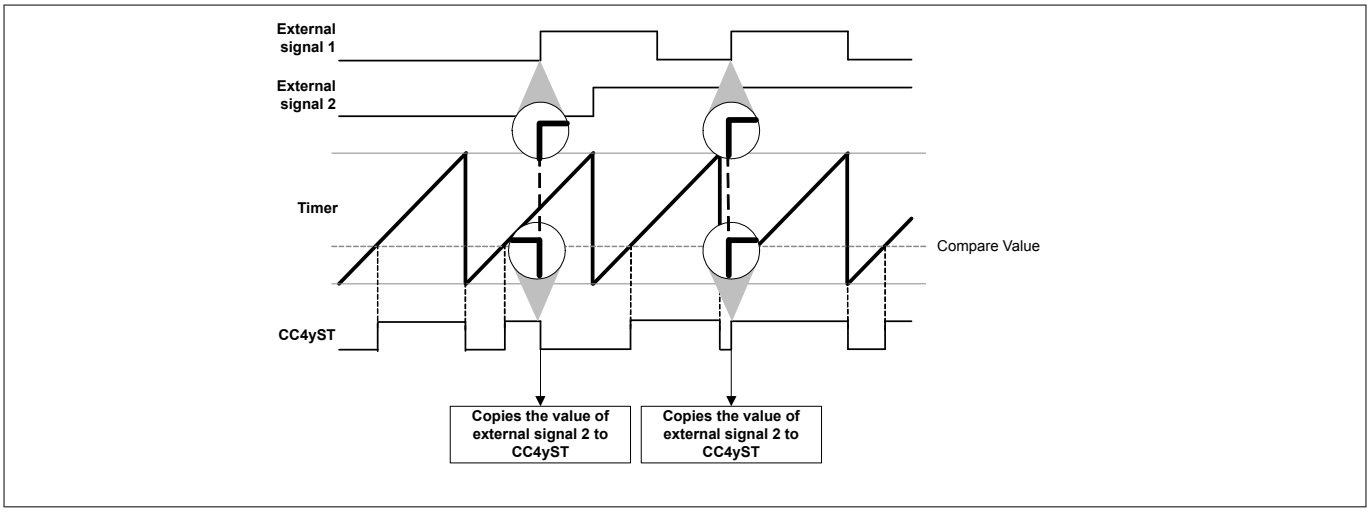


Figure 192 Status bit override

20.2.5.9 External Modulation

An external signal can be used to perform a modulation at the output of each timer slice.

To select an external modulation signal, one should map one of the input signals to one of the events, by setting the required value in the ***CC4yINS1***.EVxIS register and indicating the active level of the signal on the ***CC4yINS2***.EVxLM register. This event should be then mapped to the modulation functionality by setting the ***CC4yCMC***.MOS = 01_B if event 0 is being used, ***CC4yCMC***.MOS = 10_B if event 1 or ***CC4yCMC***.MOS = 11_B if event 2.

Notice that the modulation function is level active and therefore the active/passive configuration is set only by the ***CC4yINS2***.EVxLM.

The modulation has two modes of operation:

- modulation event is used to clear the CC4yST bit - ***CC4yTC***.EMT = 0_B
- modulation event is used to gate the outputs - ***CC4yTC***.EMT = 1_B

On ***Figure 193***, we have a external signal configured to act as modulation source that clears the CC4yST bit, ***CC4yTC***.EMT = 0_B. It was programmed to be an active LOW event and therefore, when this signal is LOW the output value follows the normal ACTIVE/PASSIVE rules.

When the signal is HIGH (inactive state), then the CC4yST bit is cleared and the output is forced into the PASSIVE state. Notice that the values of the status bit, CC4yST and the specific output CCU4x.OUTy are not linked together. One can choose for the output to be active LOW or HIGH through the PSL bit.

The exit of the external modulation inactive state is synchronized with the PWM signal due to the fact that the CC4yST bit is cleared and cannot be set while the modulation signal is inactive.

The entering into inactive state also can be synchronized with the PWM signal, by setting ***CC4yTC***.EMS = 1_B. With this all possible glitches at the output are avoided, see ***Figure 194***.

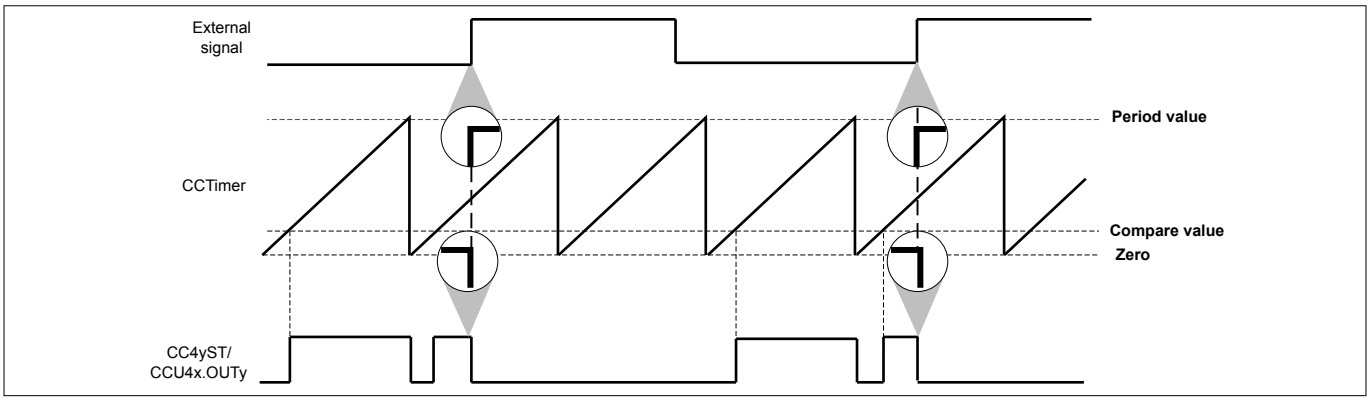


Figure 193 External modulation clearing the ST bit - *CC4yTC*.EMT = 0_B

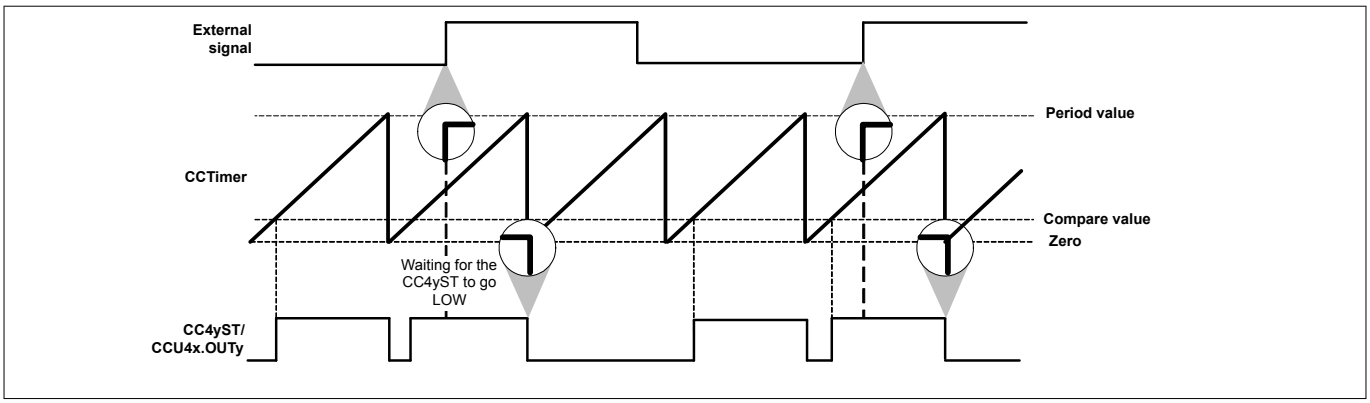


Figure 194 External modulation clearing the ST bit - *CC4yTC*.EMT = 0_B, *CC4yTC*.EMS = 1_B

On ***Figure 195***, the external modulation event was used as gating signal of the outputs, ***CC4yTC***.EMT = 1_B. The external signal was configured to be active HIGH, ***CC4yINS2***.EVxLM = 0_B, which means that when the external signal is HIGH the outputs are set to the PASSIVE state.In this mode, the gating event can also be synchronized with the PWM signal by setting the ***CC4yTC***.EMS = 1_B.

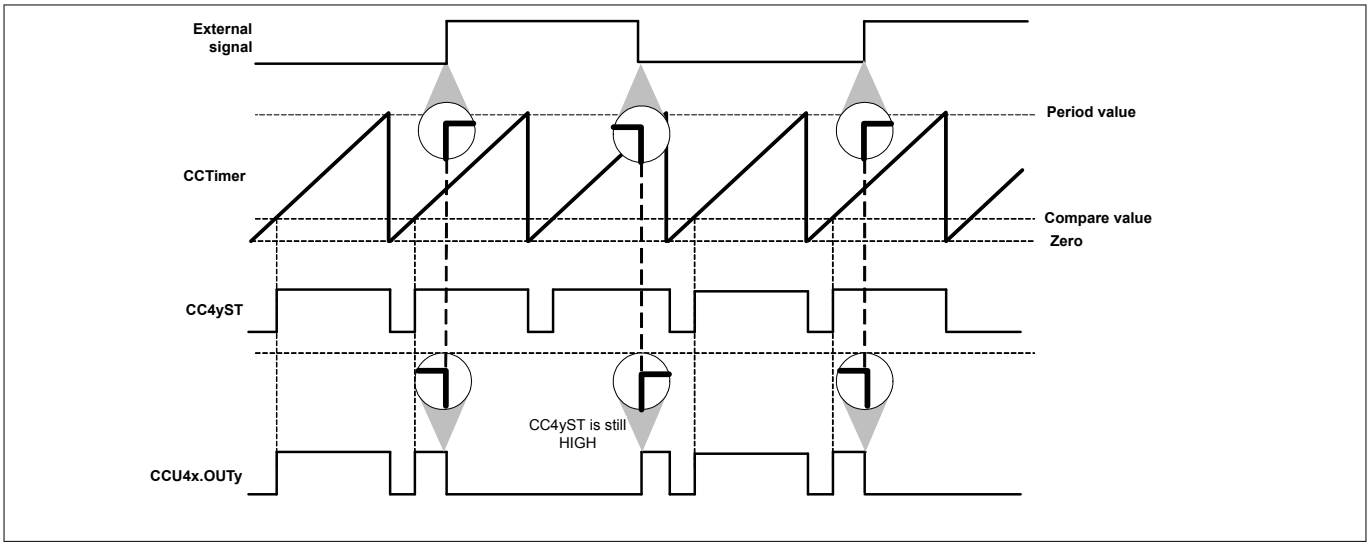


Figure 195 External modulation gating the output - *CC4yTC*.EMT = 1_B

20.2.6 Timer Slice Advanced Functions

In the following sub sections several advanced functions present in each CC4y slice are described. One should notice that each of the functions is present and works in the same manner for every CCU4 timer slice.

20.2.6.1 Multi-Channel Control

The Multi-Channel control mode is selected individually in each slice by setting the ***CC4yTC***.MCME = 1_B.

Within this mode, the output state of the Timer Slices (the ones set in Multi-Channel mode) can be controlled in parallel by a single pattern.

The pattern is controlled via the CCU4 inputs, CCU4x.MCI0, CCU4x.MCI1, CCU4x.MCI2 and CCU4x.MCI3. Each of these inputs is connected directly to the associated slice input, e.g. CCU4x.MCI0 to CC40MCI, CCU4x.MCI1 to CC41MCI.

This pattern can be controlled directly by other module. The connectivity of each device may allow different control possibilities therefore one should address ***Chapter 20.8*** to check what modules are connected to these inputs.

When using the Multi-Channel support of the CCU4, one can achieve a complete synchronicity between the output state update, CCU4x.OUTy, and the update of a new pattern,***Figure 196*** . This synchronocity feature can be enabled by using some specific modules and therefore one should address ***Chapter 20.8*** to check which module is controlling the CCU4x.MCIy inputs.

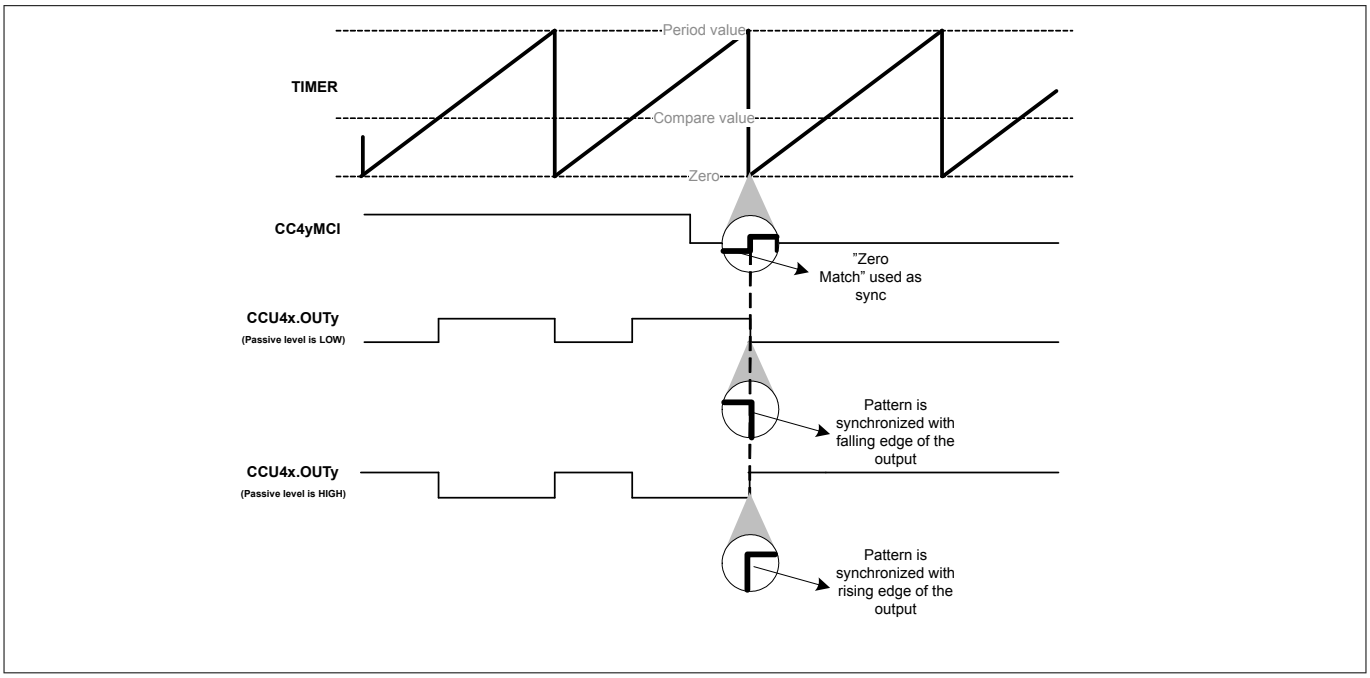


Figure 196 Multi-Channel pattern synchronization

Figure 197 shows the usage of the Multi-Channel mode in conjunction with all four Timer Slices inside the CCU4.

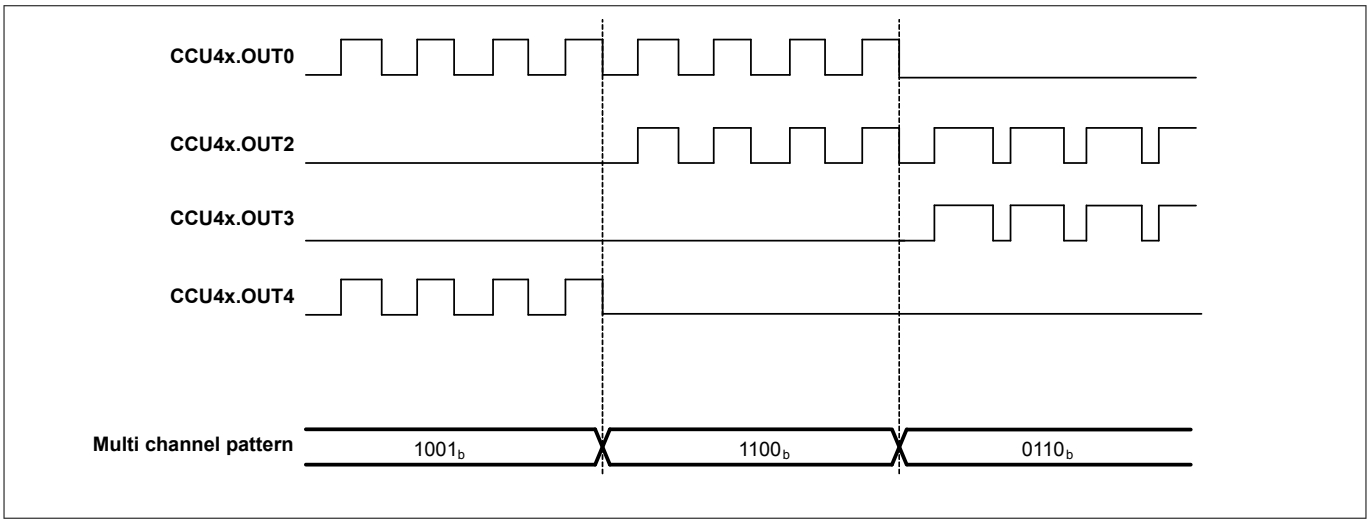


Figure 197 Multi-Channel mode for multiple Timer Slices

The synchronization between the CCU4 and the module controlling the Multi-Channel pattern is achieved, by adding a 3 cycle delay on the output path of each Timer Slice (between the status bit, CC4yST and the direct control of the output pin). This path is only selected when ***CC4yTC***.MCME = 1_B, see ***Figure 198***.

The multi pattern input synchronization can be seen on ***Figure 199***. To achieve a synchronization between the update of the status bit, the sampling of a new Multi-Channel pattern input is controlled by the period match or one match signal.

In a straightforward utilization of this synchronization feature, the module controlling the Multi-Channel pattern signals, receives a sync signal from the CCU4, the CCU4x.PSy. This signal is then used by this module to update the Multi-Channel pattern. Due to the structure of the synchronization scheme inside the CCU4, the module controlling the Multi-Channel pattern needs to update this pattern, within 4 clock cycles after the CCU4x.PSy signal is asserted, ***Figure 199***.

In a normal operation, where no external signal is used to control the counting direction, the signal used to enable the sampling of the pattern is always the period match when in edge aligned and the one match when in center aligned mode. When an external signal is used to control the counting direction, depending if the counter is counting up or counting down, the period match or the one match signal is used, respectively.

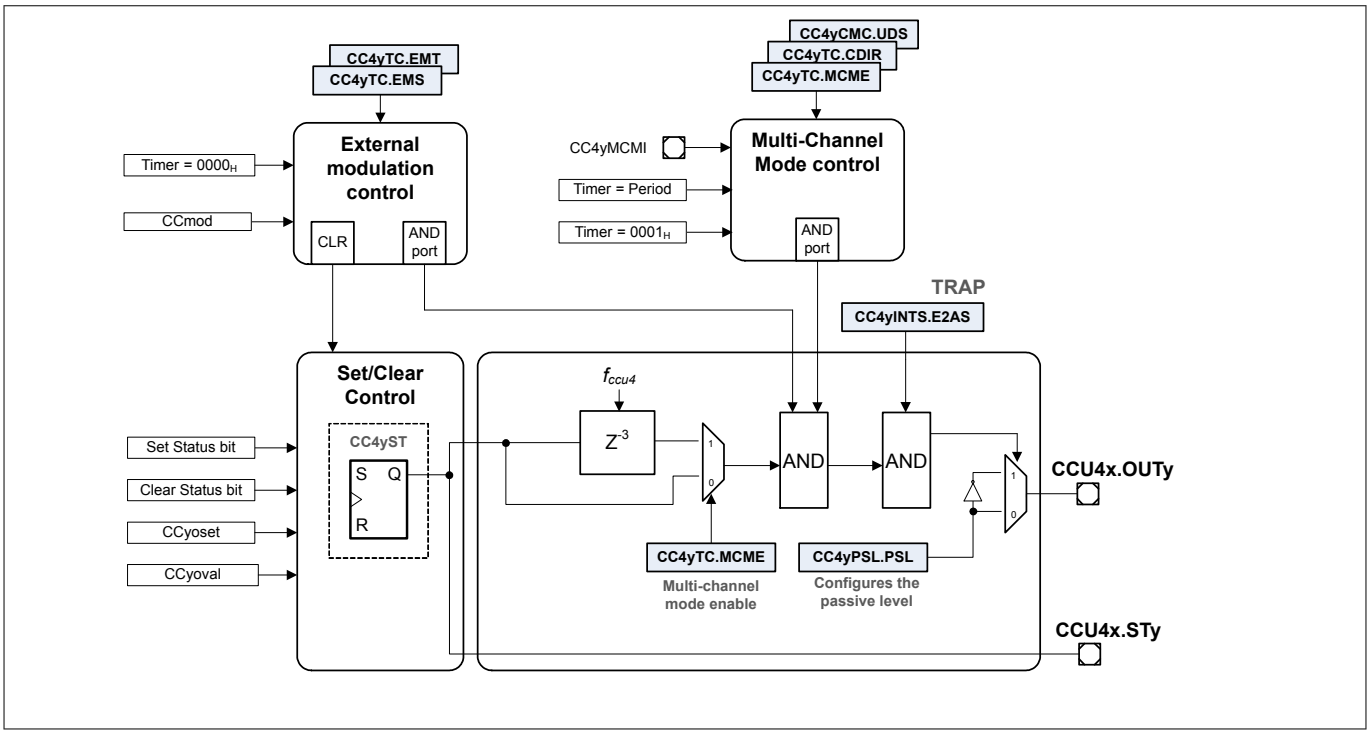


Figure 198 Multi-Channel mode output path

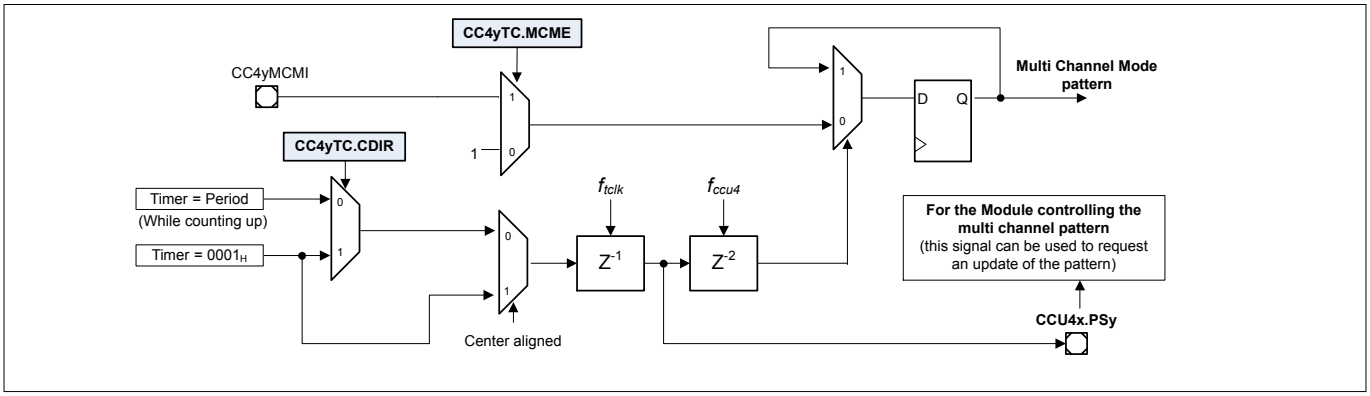


Figure 199 Multi-Channel Mode Control Logic

20.2.6.2 Timer Concatenation

The CCU4 offers a very easy mechanism to perform a synchronous timer concatenation. This functionality can be used by setting the ***CC4yCMC***.TCE = 1_B. By doing this the user is doing a concatenation of the actual CCU4 slice with the previous one, see ***Figure 200***.

Notice that is not possible to perform concatenation with non adjacent slices and that timer concatenation automatically sets the slice mode into Edge Aligned. It is not possible to perform timer concatenation in Center Aligned mode.

To enable a 64 bit timer, one should set the ***CC4yCMC***.TCE = 1_B in all the slices (with the exception of the CC40 due to the fact that it doesn't contain this control register).

To enable a 48 bit timer, one should set the ***CC4yCMC***.TCE = 1_B in two adjacent slices and to enable a 32 bit timer, the ***CC4yCMC***.TCE is set to 1_B in the slice containing the MSBs. Notice that the timer slice containing the LSBs should always have the TCE bitfield set to 0_B.

Several combinations for timer concatenation can be made inside a CCU4 module:

- one 64 bit timer
- one 48 bit timer plus a 16 timer
- two 32 bit timers
- one 32 bit timer plus two 16 bit timers

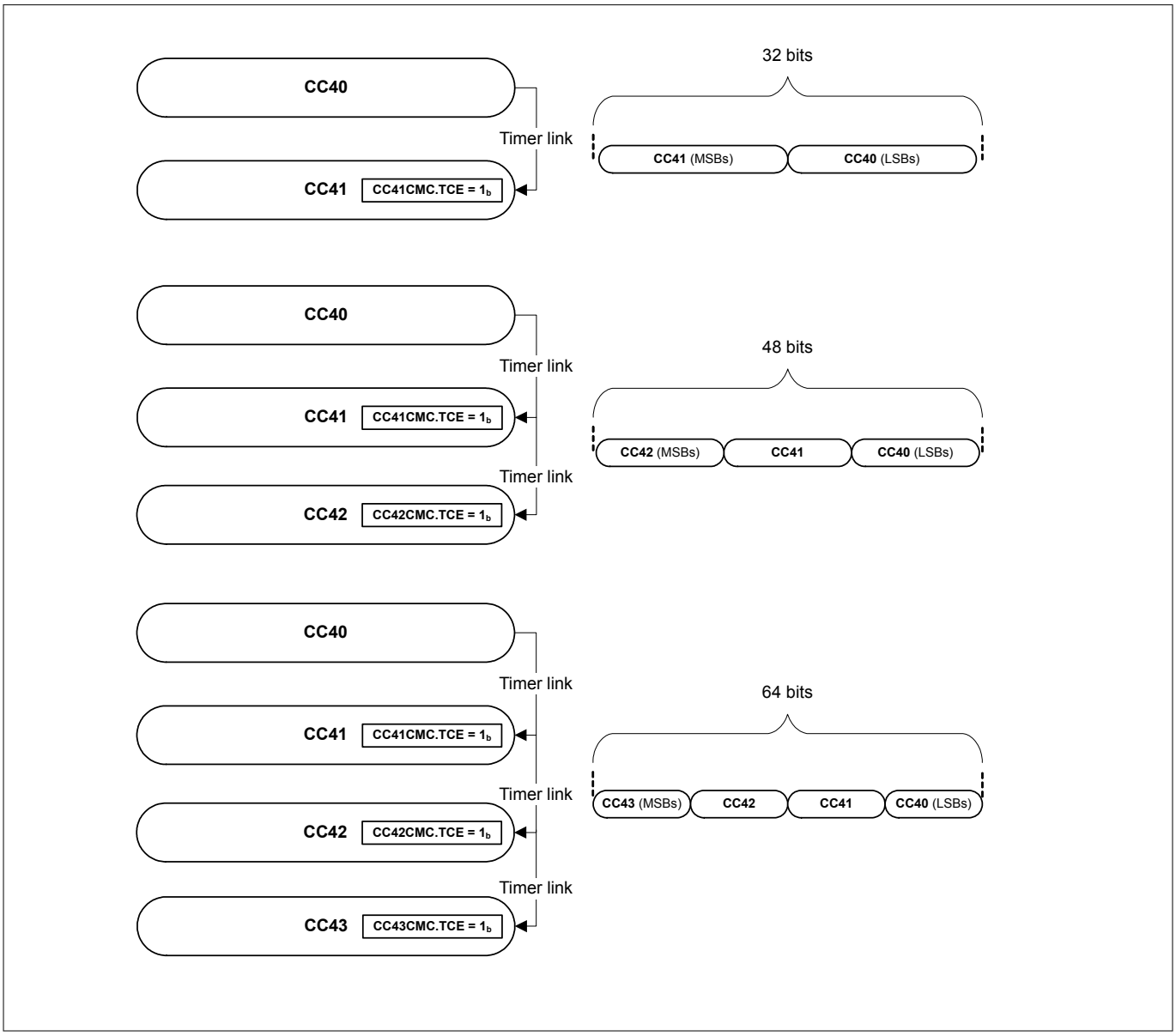


Figure 200 Timer Concatenation Example

Each Timer Slice is connected to the adjacent Timer Slices via a dedicated concatenation interface. This interface allows the concatenation of not only the Timer counting operation, but also a synchronous input trigger handling for capturing and loading operations, ***Figure 201***.

Note: For all cases CC40 and CC43 are not considered adjacent slices

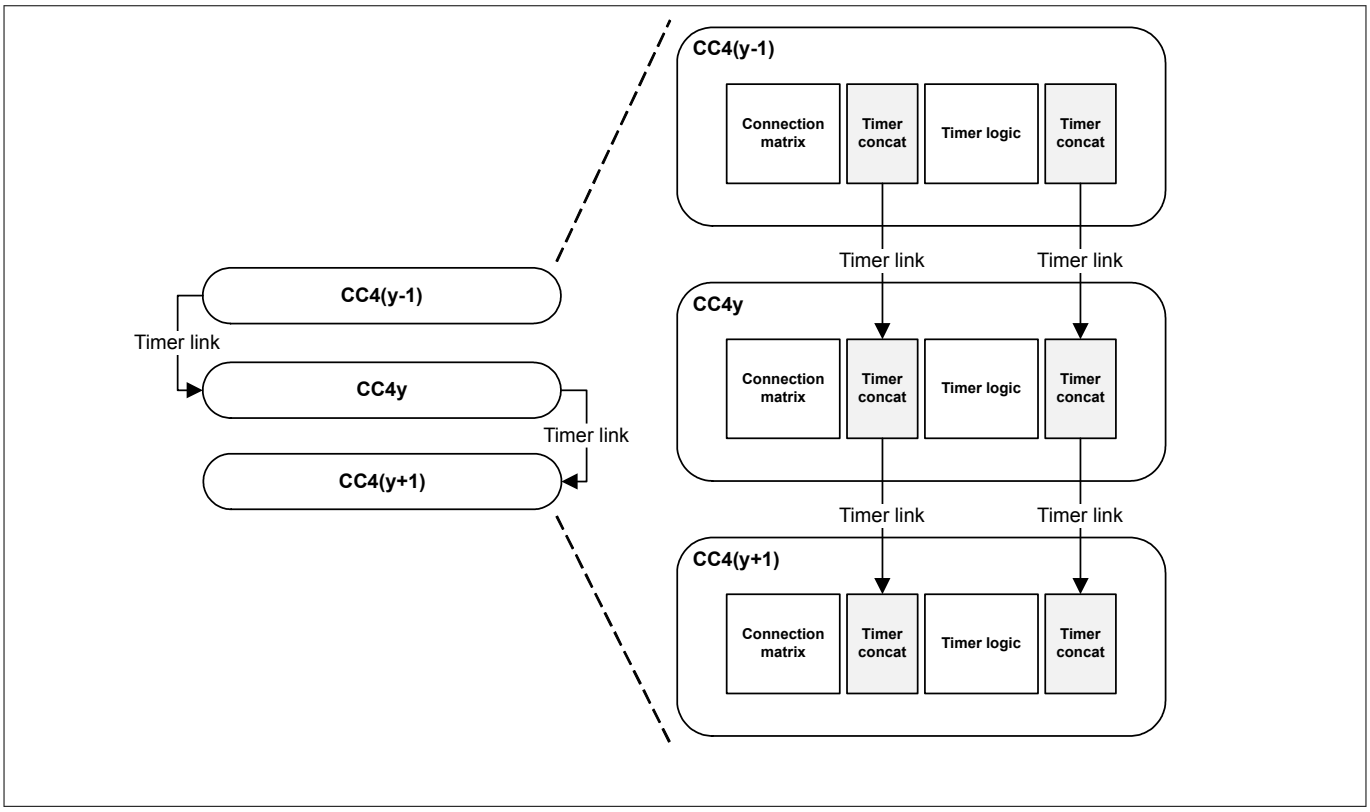


Figure 201 Timer Concatenation Link

Seven signals are present in the timer concatenation interface:

- Timer Period match (CC4yPM)
- Timer Zero match (CC4yZM)
- Timer Compare match (CC4yCM)
- Timer counting direction function (CCupd)
- Timer load function (CCload)
- Timer capture function for CC4yC0V and CC4yC1V registers (CCcap0)
- Timer capture function for CC4yC2V and CC4yC3V registers (CCcap1)

The first four signals are used to perform the synchronous timing concatenation at the output of the Timer Logic, like it is seen in ***Figure 201***. With this link, the timer length can be easily adjusted to 32, 48 or 64 bits (counting up or counting down).

The last three signals are used to perform a synchronous link between the capture and load functions, for the concatenated timer system. This means that the user can have a capture or load function programmed in the first Timer Slice, and propagate this capture or load trigger synchronously from the LSBs until the MSBs, ***Figure 202***.

The capture or load function only needs to be configured in the first Timer Slice (the one holding the LSBs). From the moment that ***CC4yCMC***.TCE is set to 1_B, in the following Timer Slices, the link between these functions is done automatically by the hardware.

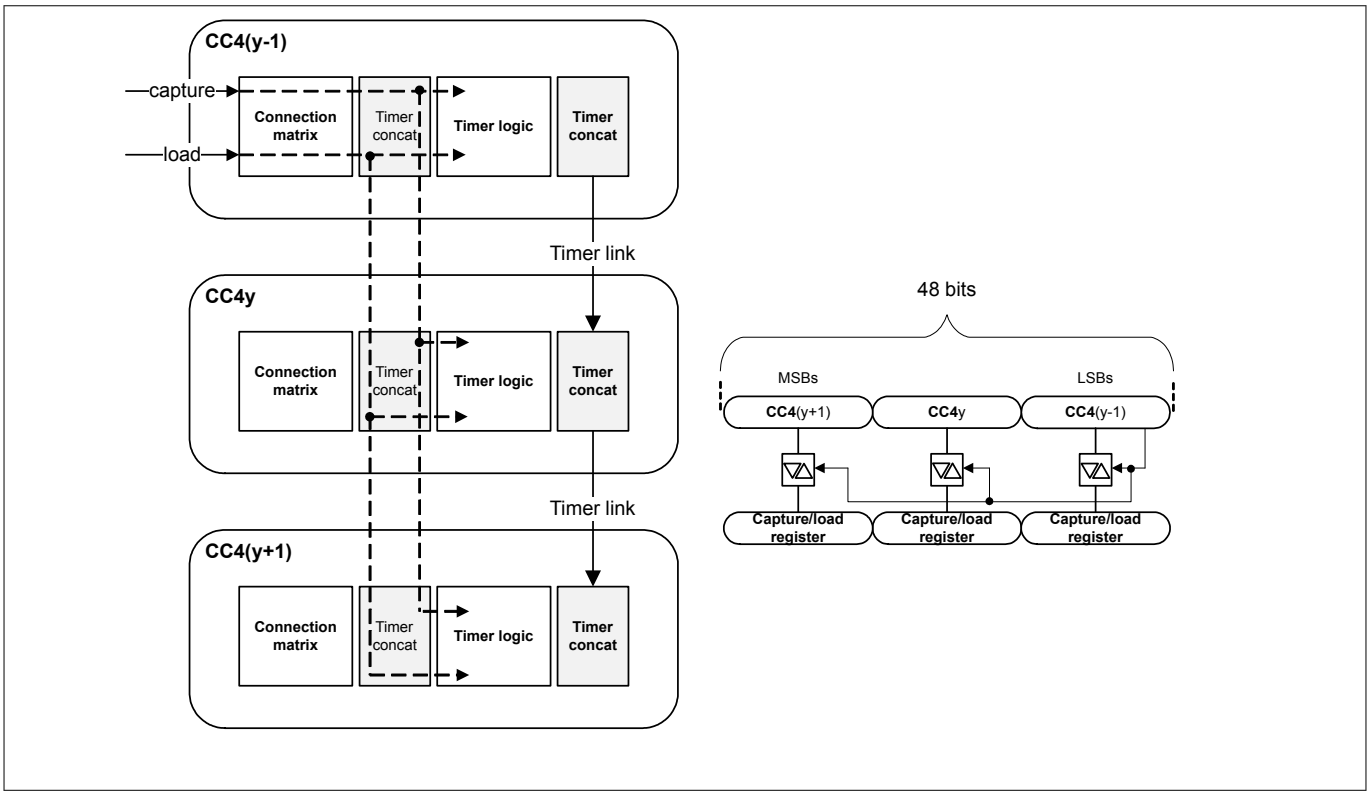


Figure 202 Capture/Load Timer Concatenation

The period match (CC4yPM) or zero match (CC4yZM) from the previous Timer Slice (with the immediately next lower index) are used in concatenated mode, as gating signal for the counter. This means that the counting operation of the MSBs only happens when a wrap around condition is detected, avoiding additional DSP operations to extract the counting value.

With the same methodology, the compare match (CC4yCM), zero match and period match are gated with the specific signals from the previous slice. This means that the timing information is propagated throughout all the slices, enabling a completely synchronous match between the LSB and MSB count, see ***Figure 203***.

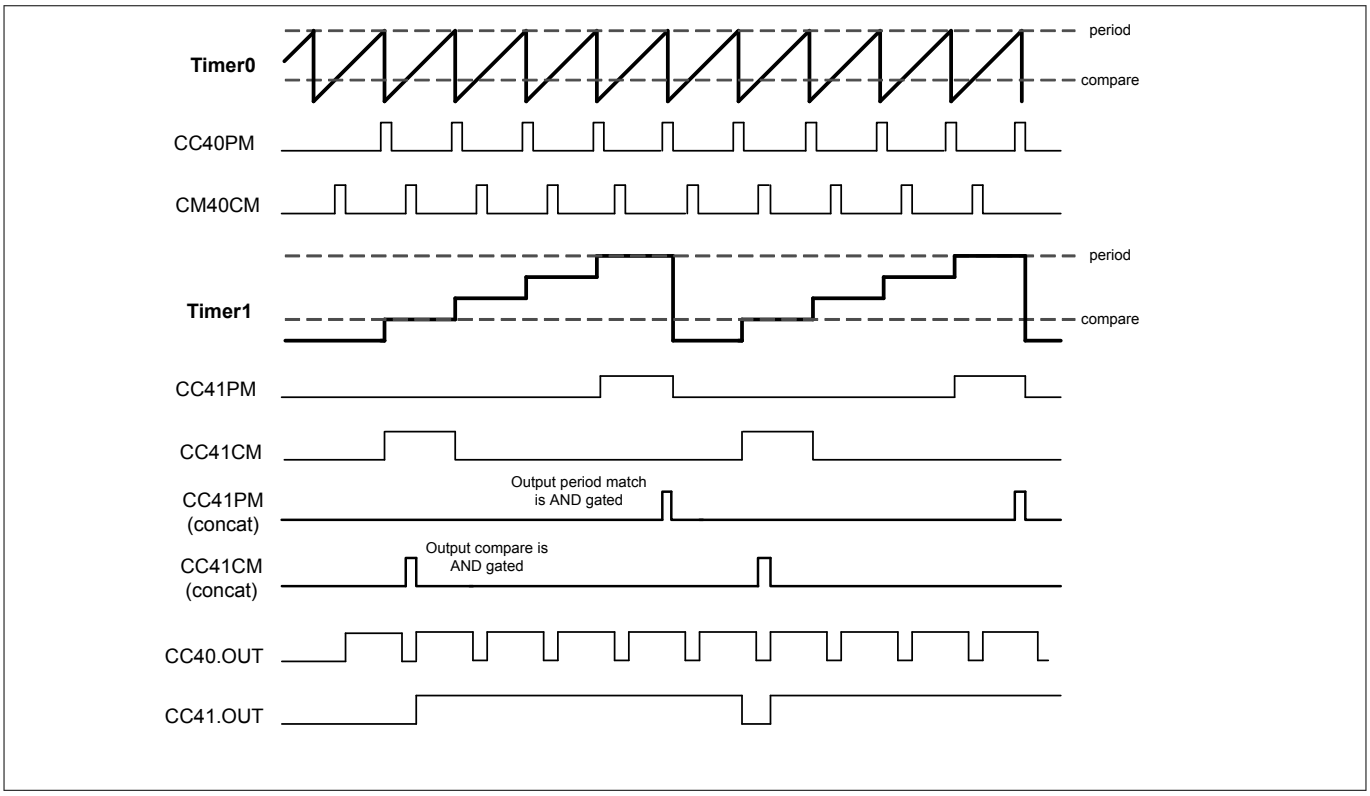


Figure 203 32 bit concatenation timing diagram

Note: The counting direction of the concatenated timer needs to be fixed. The timer can count up or count down, but the direction cannot be updated on the fly.

Figure 204 gives an overview of the timer concatenation logic. Notice that all the mechanism is controlled solely by the ***CC4yCMC***.TCE bitfield.

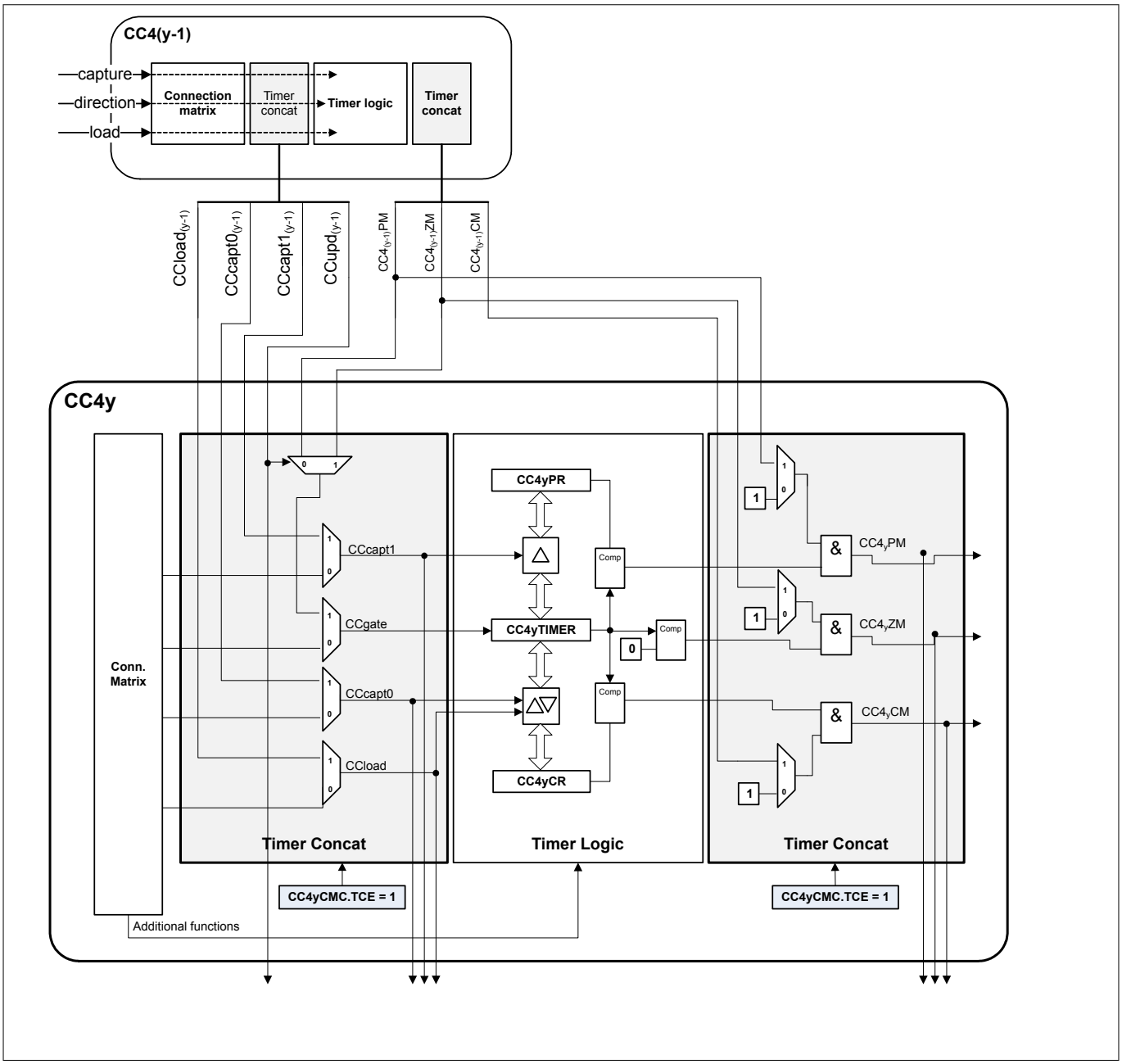


Figure 204 Timer concatenation control logic

20.2.6.3 PWM Dithering

The CCU4 has an automatic PWM dithering insertion function. This functionality can be used with very slow control loops that cannot update the period/compare values in a fast manner, and by that fact the loop can lose precision on long runs. By introducing dither on the PWM signal, the average frequency/duty cycle is then compensated against that error.

Each slice contains a dither control unit, see ***Figure 205*** .

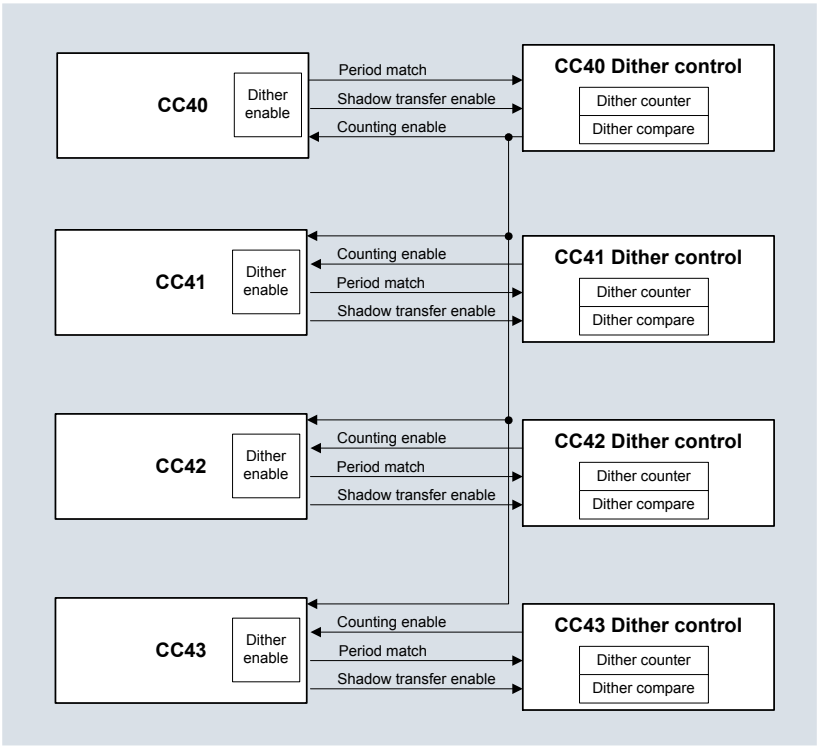


Figure 205 Dither structure overview

The dither control unit contains a 4 bit counter and a compare value. The counter works in a bit reverse mode so the distribution of increments stays uniform over 16 counter periods, see ***Table 248***.

Table 248 Dither bit reverse counter

counter[3]	counter[2]	counter[1]	counter[0]
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	0
0	0	0	1
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1

Table 248 Dither bit reverse counter (continued)

counter[3]	counter[2]	counter[1]	counter[0]
0	1	1	1
1	1	1	1

The counter is then compared against a programmed value, ***CC4yDIT***.DCV. If the counter value is smaller than the programmed value, a gating signal is generated that can be used to extend the period, to delay the compare or both (controlled by the ***CC4yTC***.DITHE field, see ***Table 249*** for one clock cycle.

Table 249 Dither modes

DITHE[1]	DITHE[0]	Mode
0	0	Dither is disabled
0	1	Period is increased by 1 cycle
1	0	Compare match is delayed by 1 cycle
1	1	Period is increased by 1 cycle and compare is delayed by 1 cycle

The dither compare value also has an associated shadow register that enables concurrent update with the period/compare register of CC4y. The control logic for the dithering unit is represented on ***Figure 206***.

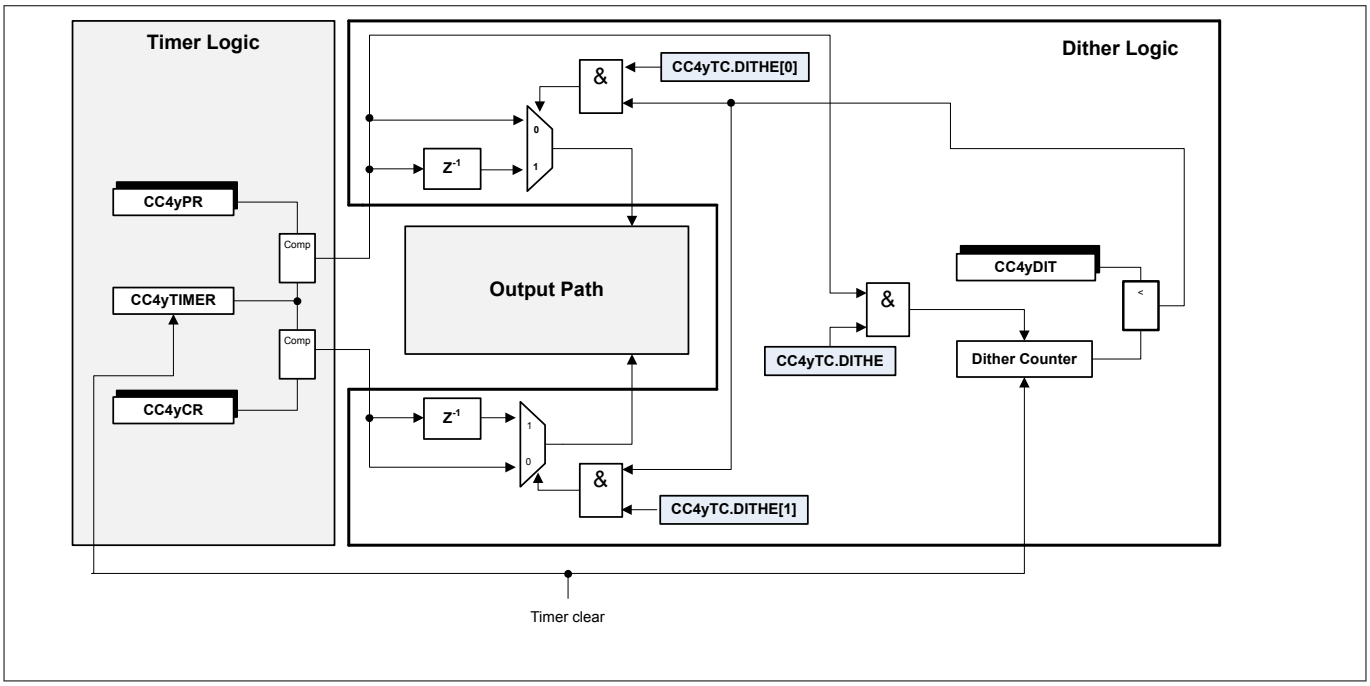


Figure 206 Dither control logic

Figure 207 to ***Figure 212*** show the effect of the different configurations for the dithering function, ***CC4yTC***.DITHE, for both counting schemes, Edge and Center Aligned mode. In each figure, the bit reverse scheme is represented for the dither counter and the compare value was programmed with the value 8_H. In each figure, the variable T, represents the period of the counter, while the variable d indicates the duty cycle (status bit is set HIGH).

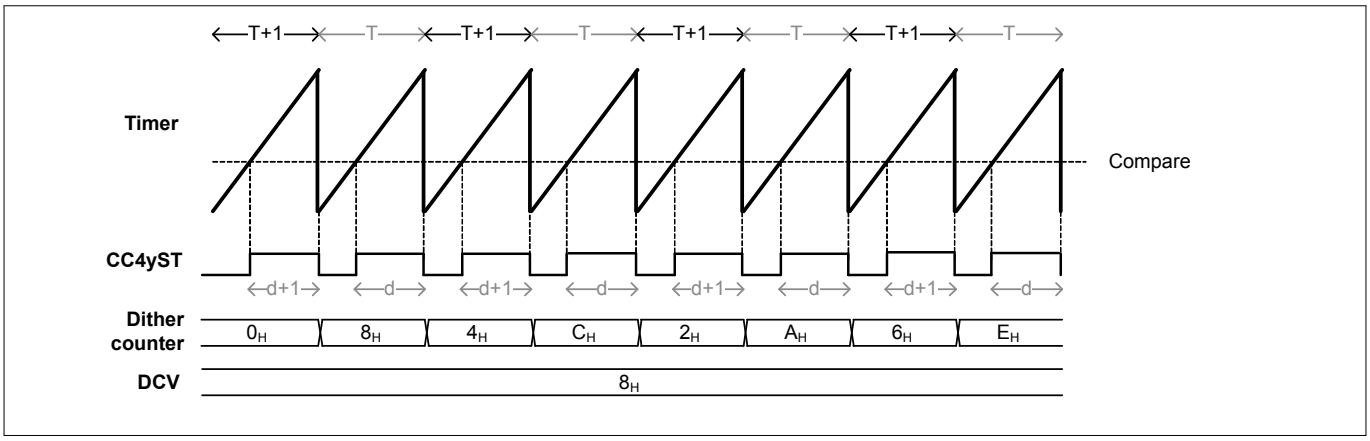


Figure 207 Dither timing diagram in edge aligned - *CC4yTC*.DITHE = 01_B

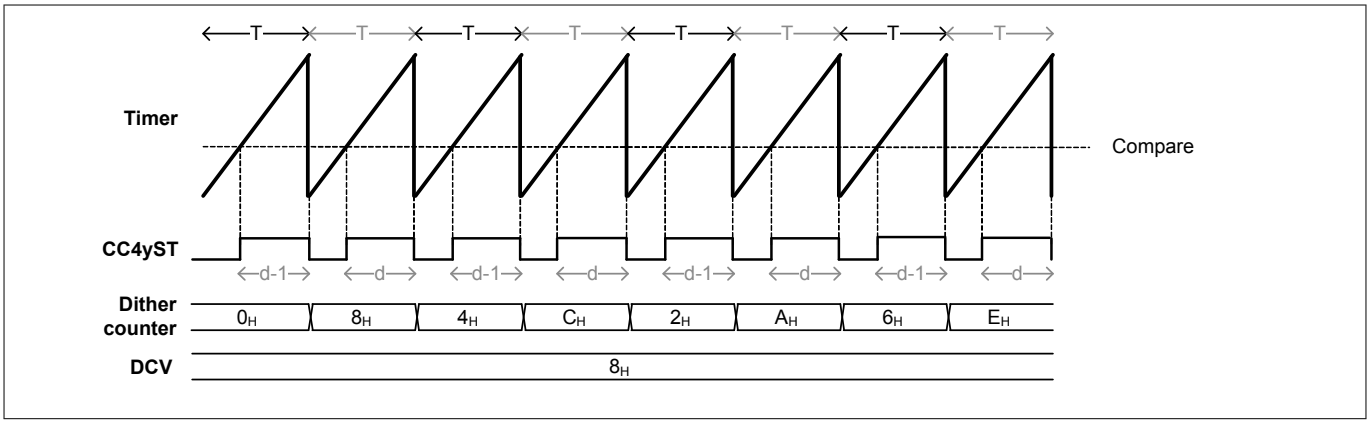


Figure 208 Dither timing diagram in edge aligned - *CC4yTC*.DITHE = 10_B

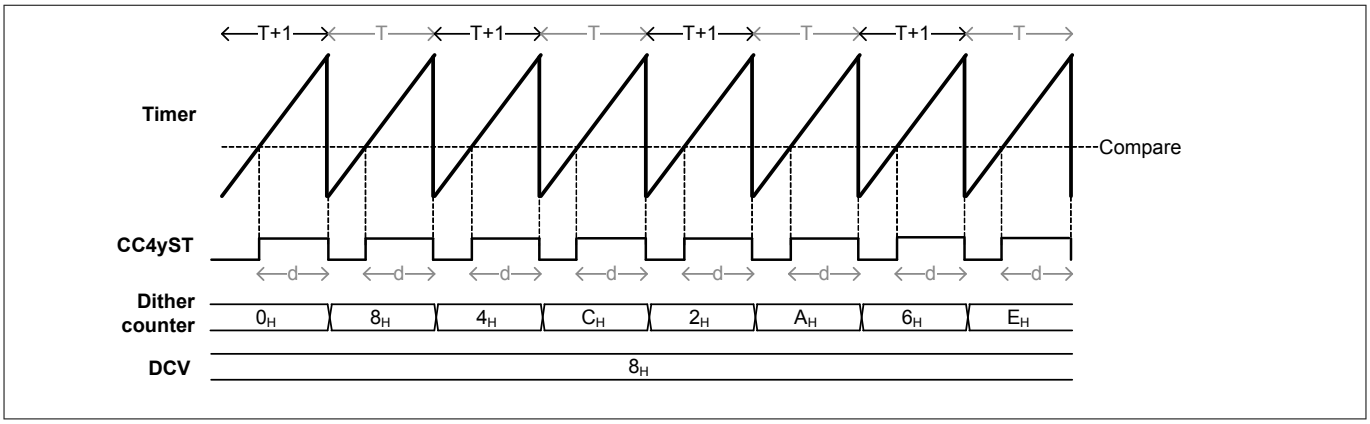


Figure 209 Dither timing diagram in edge aligned - *CC4yTC*.DITHE = 11_B

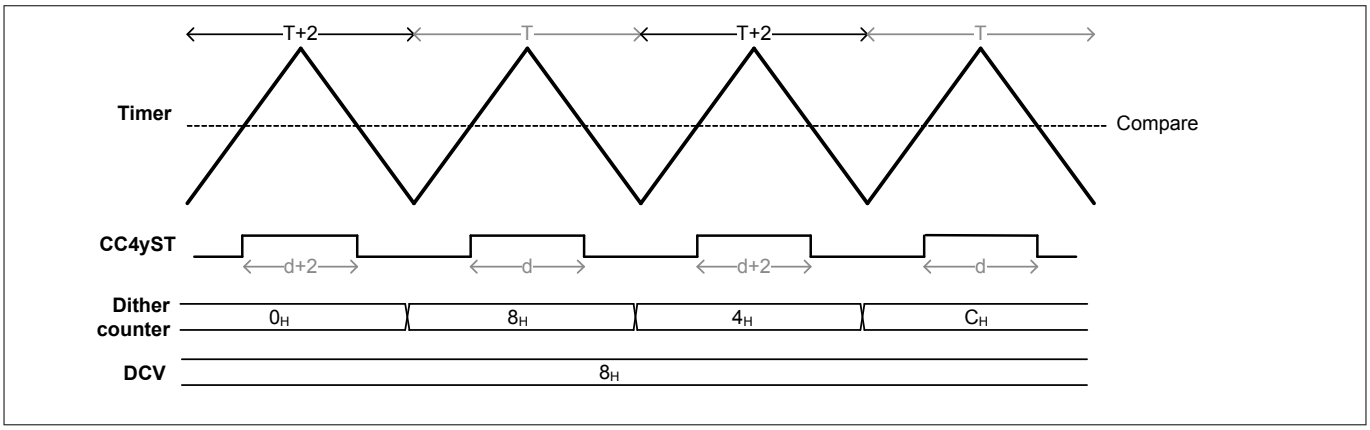


Figure 210 Dither timing diagram in center aligned - *CC4yTC*.DITHE = 01_B

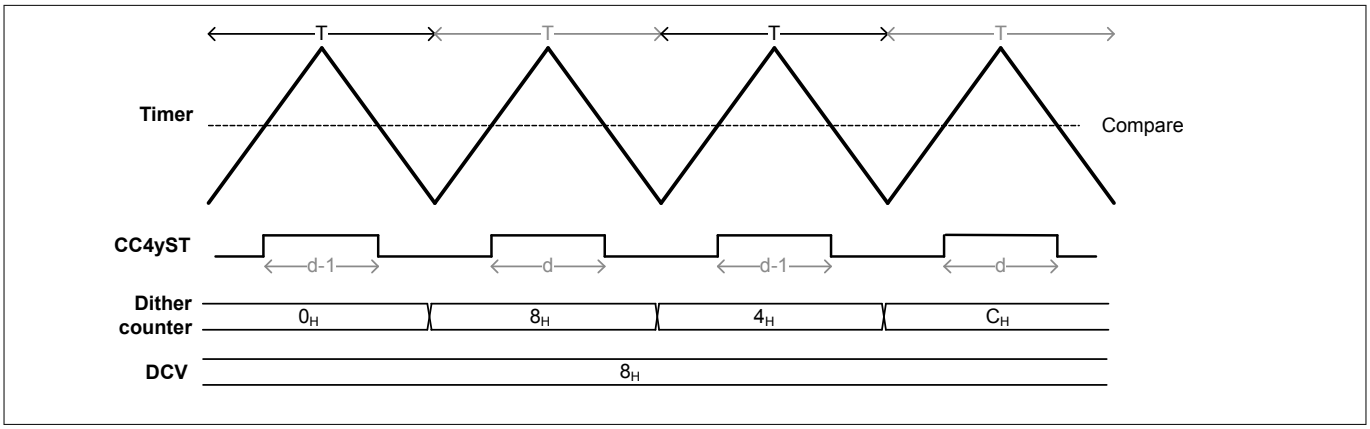


Figure 211 Dither timing diagram in center aligned - *CC4yTC*.DITHE = 10_B

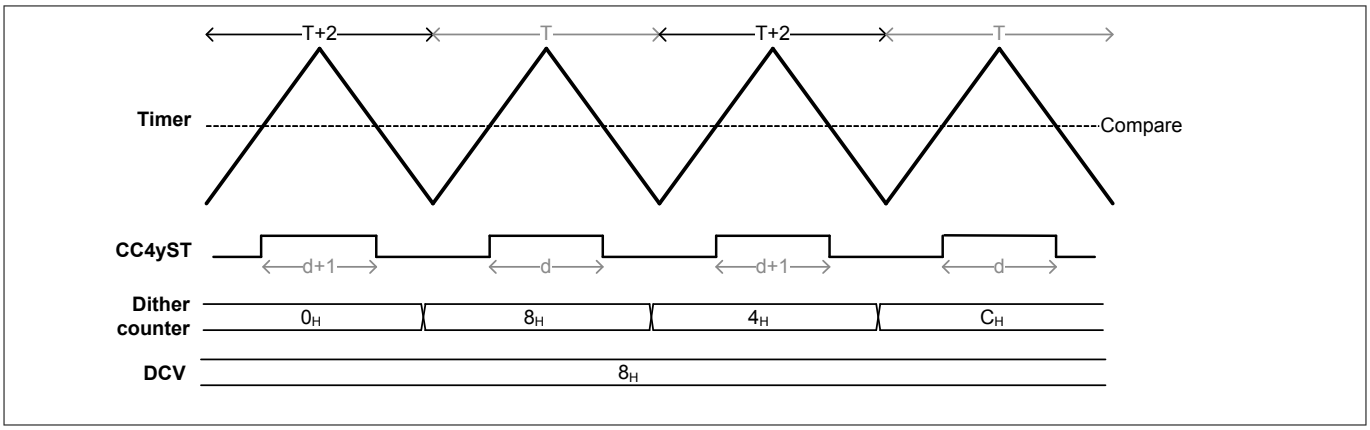


Figure 212 Dither timing diagram in center aligned - *CC4yTC*.DITHE = 11

Note: When using the dither, is not possible to select a period value of FS when in edge aligned mode. In center aligned mode, the period value must be at least FS - 2.

20.2.6.4 Capture Extended Read Back Mode

Each Timer Slice capture logic can operate in a FIFO read back mode. This mode can be enabled by setting the ***CC4yTC***.ECM = 1_B. This Extended Read back mode allows the software to read back the capture data always from the same address (***CC4yECRD0*** for the structure linked with the capture trigger 0 or ***CC4yECRD1*** for the one

linked with capture trigger 1). This read back will always return the oldest captured value, enabling an easy software routine implementation for reconstructing the capture data.

This function allows the usage of a FIFO structure for each capturing trigger. This relaxes the software read back routine when multiple capture triggers are present, and the software is not fast enough to perform a read operation in each capture event.

This FIFO read back function is present for a depth-4 and depth-2 FIFO structure.

The read back data contains also a lost value bitfield, that indicates if a capture trigger was lost due to the fact that the FIFO structure was full. This bitfield is set whenever a capture event was sensed and the FIFO was full (regardless if the continuos capture mode was enabled or not). This bitfield is cleared automatically by HW whenever the next read of the ***CC4yECRD0***/***CC4yECRD1*** register occurs. This bitfield does not indicate how many capture events were lost, it just indicates that between two ECRD reads at least a capture event was lost (this can help the SW evaluate which part of the data read, can be used for calculation).

Note: When the ECM bitfield is set, reading the individual capture registers is still possible. Nevertheless the full flags can only be cleared by the HW when a read back is done via the ***CC4yECRD0***/***CC4yECRD1*** *address.*

Depth 4 Structure

The FIFO depth-4 structure is present in the hardware when the capture trigger 1 is enabled and the ***CC4yTC***.SCE = 1_B (same capture event), ***Figure 213***.

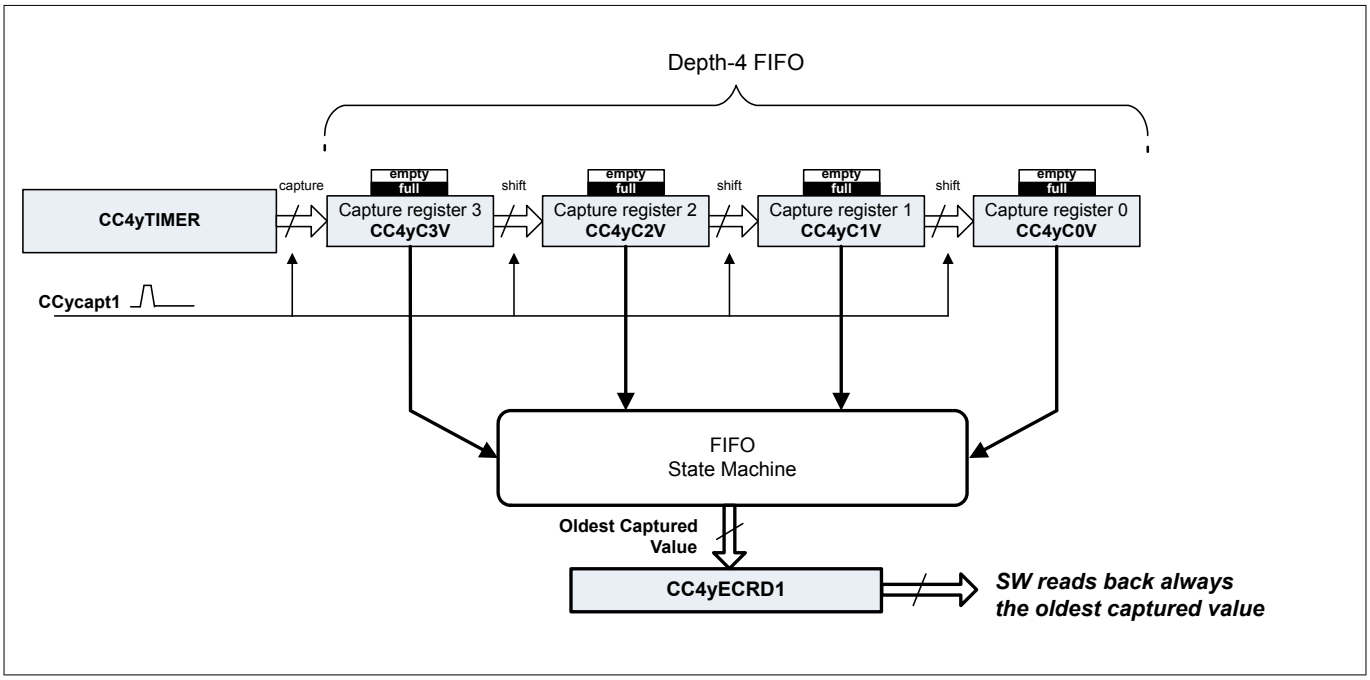


Figure 213 Capture Extended Read Back - Depth 4

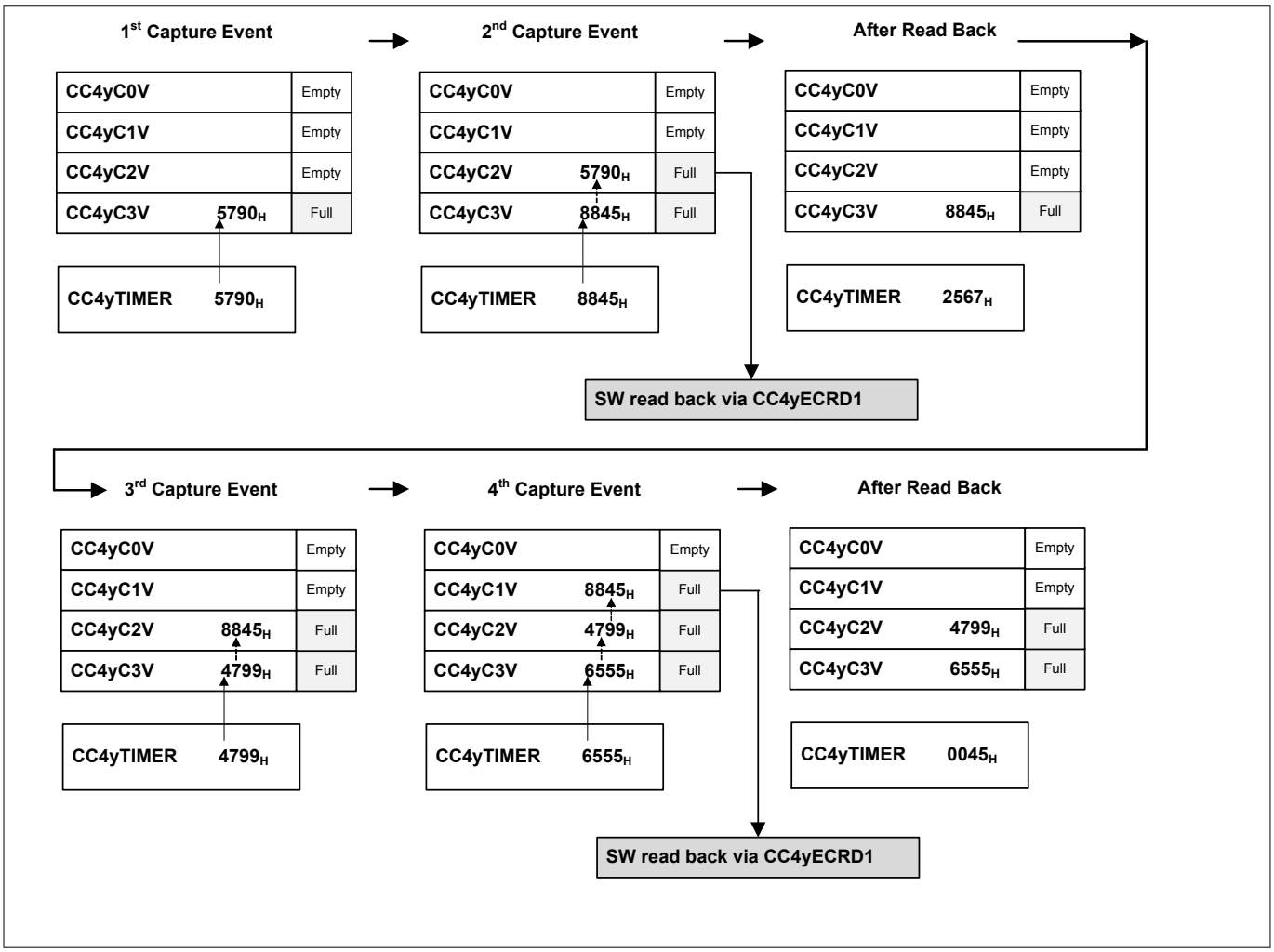


Figure 214 Depth 4 software access example

Depth 2 Structure

Each Timer Slice can have two capture structures of depth-2: one used with capture trigger 0 and another with capture trigger 1.

The one linked with capture trigger 0, is accessed via the ***CC4yECRD0*** while the one linked with the capture trigger 1 is accessed via the ***CC4yECRD1***, ***Figure 215***.

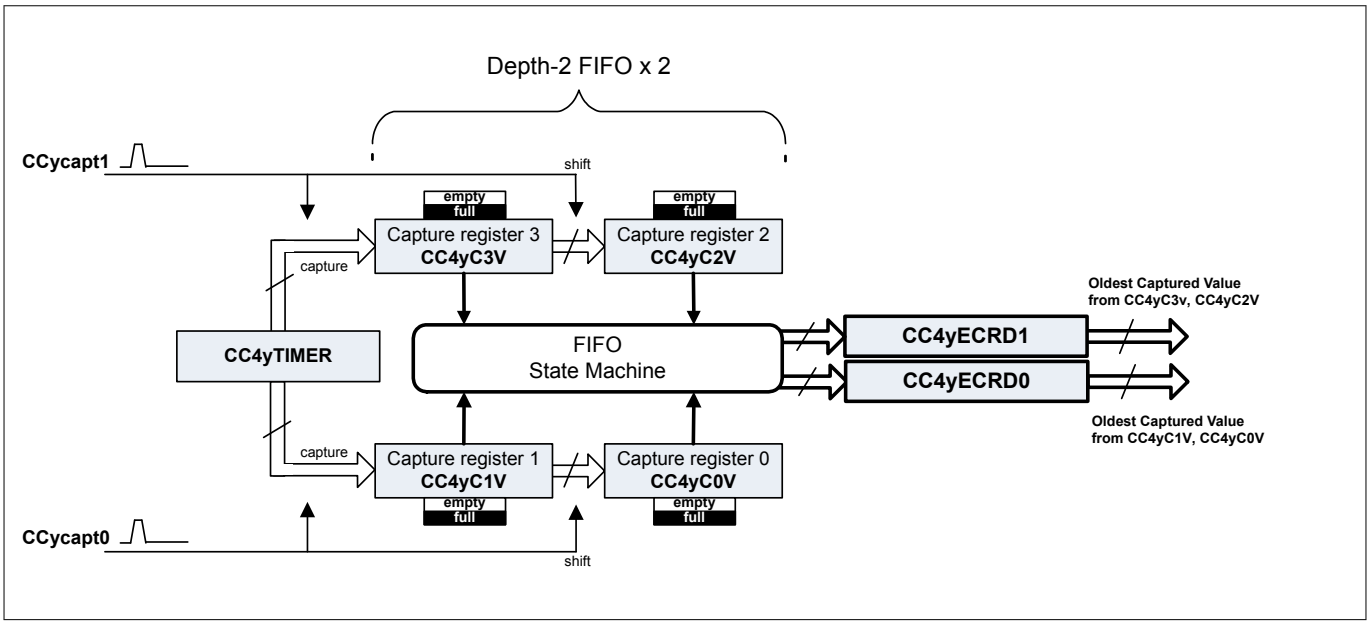


Figure 215 Capture Extended Read Back - Depth 2

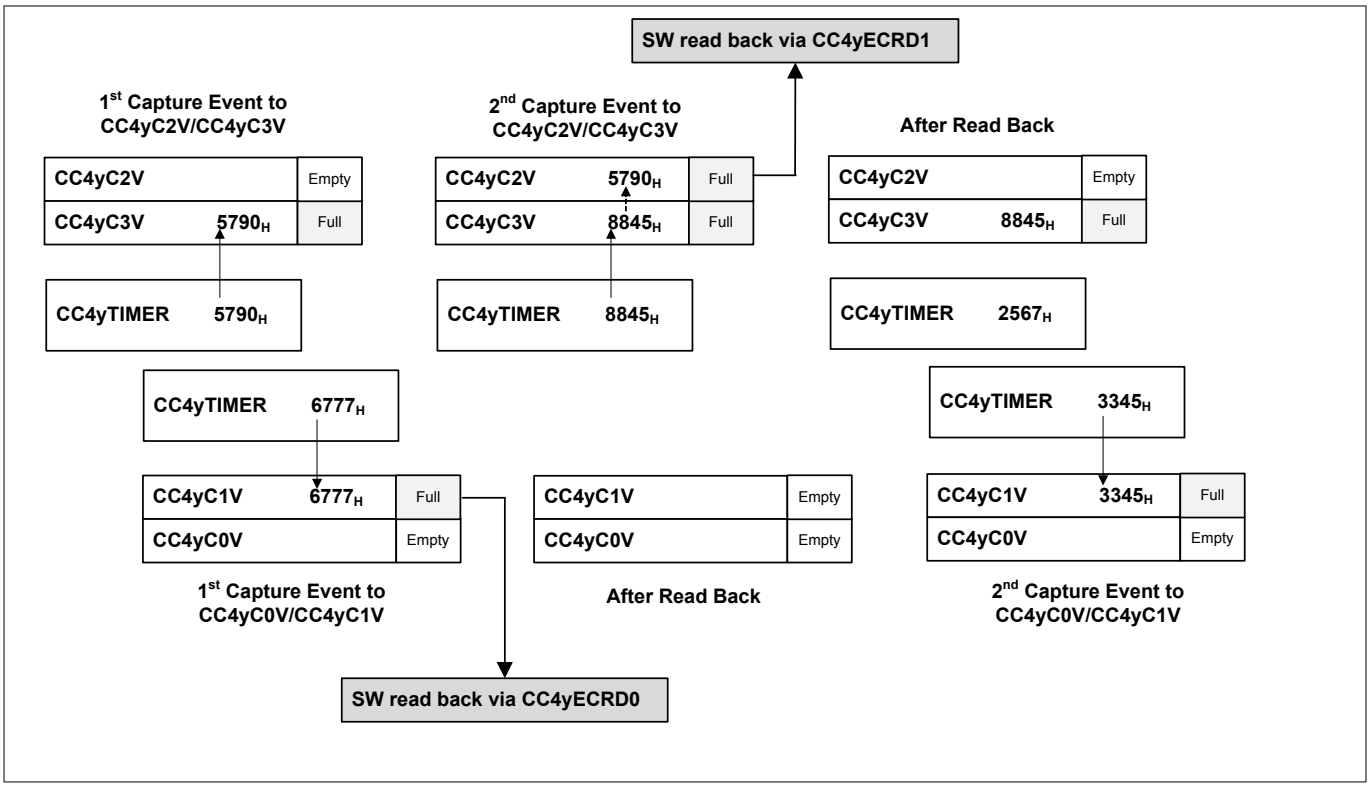


Figure 216 Depth 2 software access example

20.2.7 Clock Prescaler

The CCU4 contains a 4 bit prescaler that can be used in two operating modes for each individual slice:

- normal prescaler mode
- floating prescaler mode

The run bit of the prescaler can be set/cleared by SW by writing into the registers, ***GIDLC***.SPRB and ***GIDLS***.CPRB respectively, and it can also be cleared by the run bit of a specific slice. With the last mechanism, the run bit of

the prescaler is cleared one clock cycle after the clear of the run bit of the selected slice. To select which slice can perform this action, one should program the ***GCTRL***.PRBC register.

20.2.7.1 Normal Prescaler Mode

In Normal prescaler mode the clock fed to the CC4y counter is a normal fixed division by N, accordingly to the value set in the ***CC4yPSC***.PSIV register. The values for the possible division values are listed in ***Table 250***. The ***CC4yPSC***.PSIV value is only modified by a SW access. Notice that each slice has a dedicated prescaler value selector (***CC4yPSC***.PSIV), which means that the user can select different counter clocks for each Timer Slice (CC4y).

Table 250 Timer clock division options

***CC4yPSC*.PSIV**	**Resulting clock**
0000_B	f_{ccu4}
0001_B	$f_{ccu4}/2$
0010_B	$f_{ccu4}/4$
0011_B	$f_{ccu4}/8$
0100_B	$f_{ccu4}/16$
0101_B	$f_{ccu4}/32$
0110_B	$f_{ccu4}/64$
0111_B	$f_{ccu4}/128$
1000_B	$f_{ccu4}/256$
1001_B	$f_{ccu4}/512$
1010_B	$f_{ccu4}/1024$
1011_B	$f_{ccu4}/2048$
1100_B	$f_{ccu4}/4096$
1101_B	$f_{ccu4}/8192$
1110_B	$f_{ccu4}/16384$
1111_B	$f_{ccu4}/32768$

20.2.7.2 Floating Prescaler Mode

The floating prescaler mode can be used individually in each slice by setting the register ***CC4yTC***.FPE = 1_B. With this mode, the user can not only achieve a better precision on the counter clock for compare operations but also reduce the SW read access for the capture mode.

The floating prescaler mode contains additionally to the initial configuration value register, ***CC4yPSC***.PSIV, a compare register, ***CC4yFPC***.PCMP with an associated shadow register mechanism.

Figure 217 shows the structure of the prescaler in floating mode when the specific slice is in compare mode (no external signal is used for capture). In this mode, the value of the clock division is increment by 1_D every time that a timer overflow/underflow (overflow if in Edge Aligned Mode, underflow if in Center Aligned Mode) occurs.

In this mode, the Compare Match from the timer is AND gated with the Compare Match of the prescaler and every time that this event occurs, the value of the clock division is updated with the ***CC4yPSC***.PSIV value in the immediately next timer overflow/underflow event.

The shadow transfer of the floating prescaler compare value, ***CC4yFPC***.PCMP, is done following the same rules described on ***Chapter 20.2.4.7***.

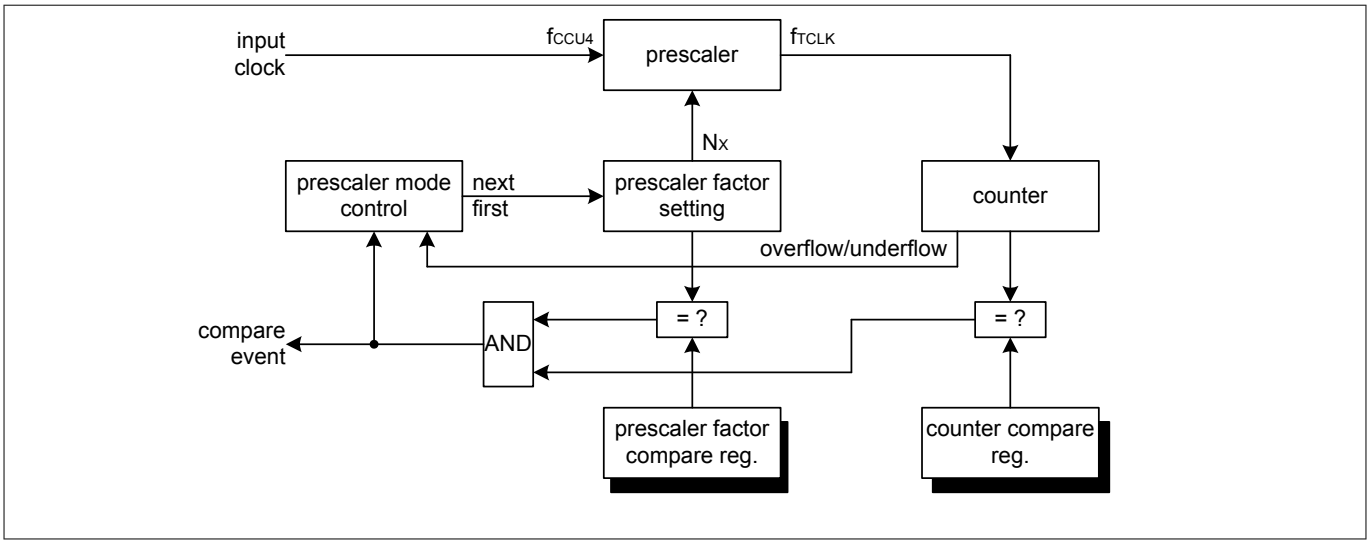


Figure 217 Floating prescaler in compare mode overview

When the specific CC4y is operating in capture mode (when at least one external signal is decoded as capture functionality), the actual value of the clock division also needs to be stored every time that a capture event occurs. The floating prescaler can have up to 4 capture registers (the maximum number of capture registers is dictated by the number of capture registers used in the specific slice).

The clock division value continues to be increment by 1_D every time that a timer overflow (in capture mode, the slice is always operating in Edge Aligned Mode) occurs and it is loaded with the PSIV value every time that a capture triggers is detected.

See the ***Chapter 20.2.8.2*** for a full description of the usage of the floating prescaler mode in conjunction with compare and capture modes.

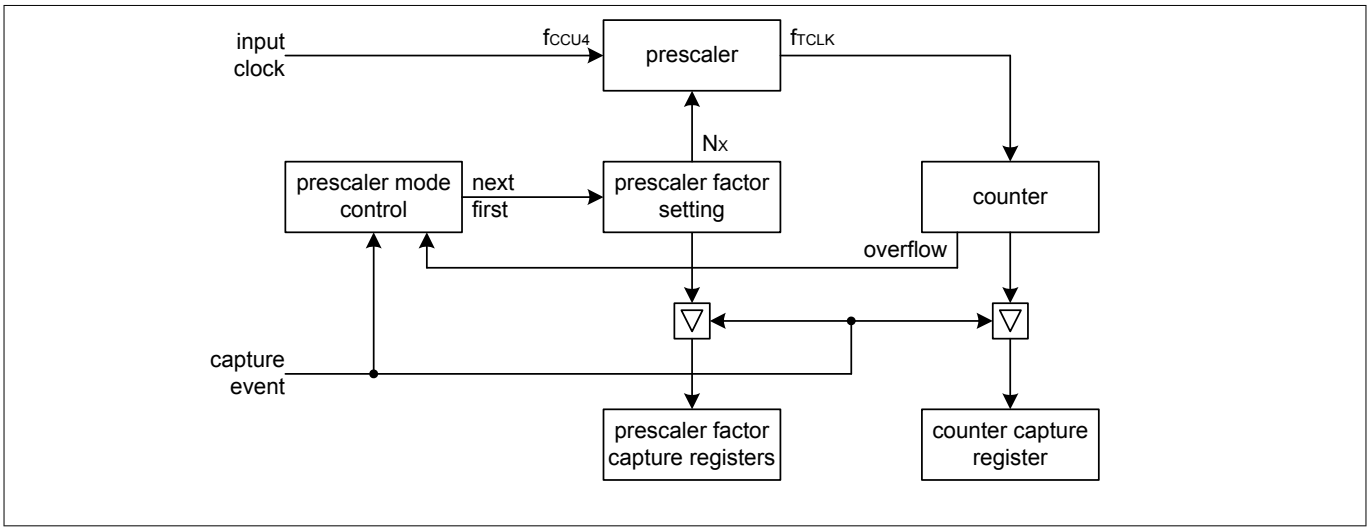


Figure 218 Floating Prescaler in capture mode overview

20.2.8 CCU4 Usage

20.2.8.1 PWM Signal Generation

The CCU4 offers a very flexible range in duty cycle configurations. This range is comprised between 0 to 100%.

To generate a PWM signal with a 100% duty cycle in Edge Aligned Mode, one should program the compare value, ***CC4yCR***.CR, to 0000_H, see ***Figure 219***.

In the same manner a 100% duty cycle signal can be generated in Center Aligned Mode, see ***Figure 220***.

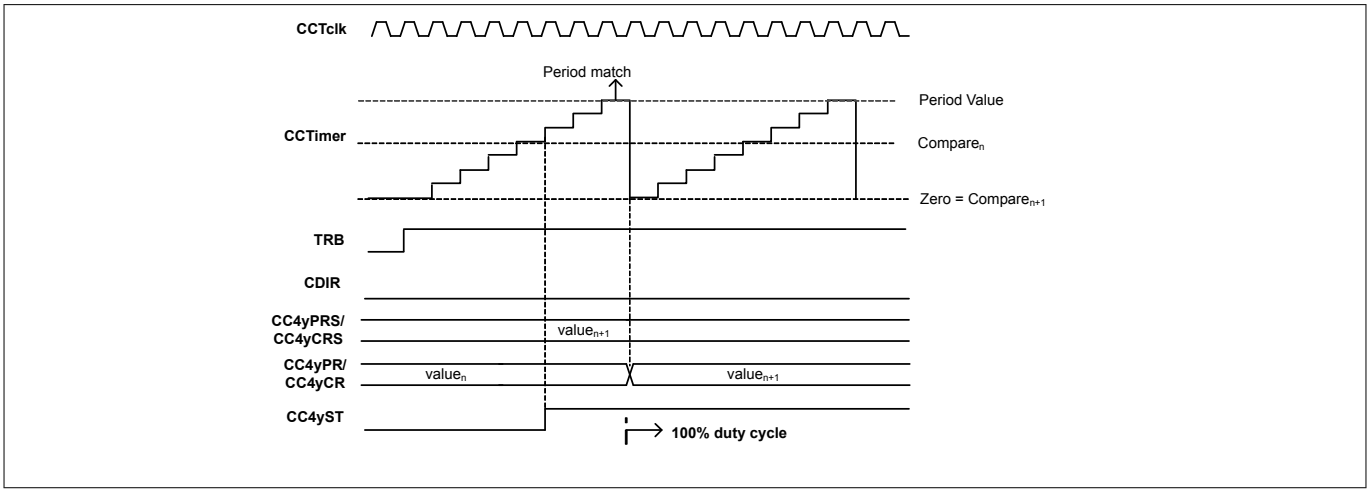


Figure 219 PWM with 100% duty cycle - Edge Aligned Mode

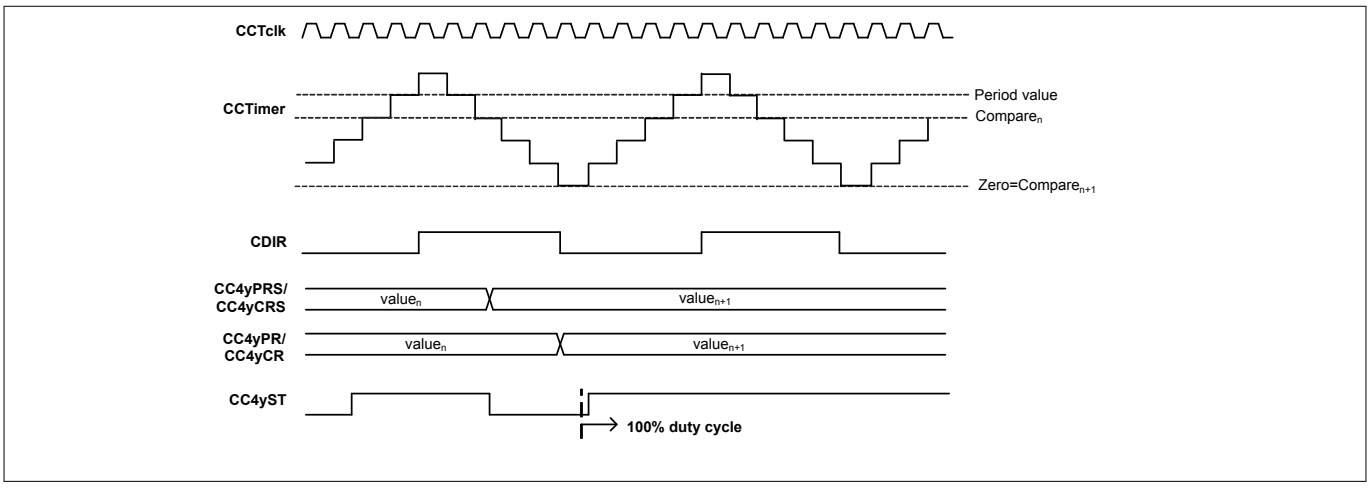


Figure 220 PWM with 100% duty cycle - Center Aligned Mode

To generate a PWM signal with 0% duty cycle in Edge Aligned Mode, the compare register should be set with the value programmed into the period value plus 1. In the case that the timer is being used with the full 16 bit capability (counting from 0 to 65535), setting a value bigger than the period value into the compare register is not possible and therefore the smallest duty cycle that can be achieved is 1/FS, see ***Figure 221***.

In Center Aligned Mode, the counter is never running from 0 to 65535_D, due to the fact that it has to overshoot for one clock cycle the value set in the period register. Therefore the user never has a FS counter, which means that generating a 0% duty cycle signal is always possible by setting a value in the compare register bigger than the one programmed into the period register, see ***Figure 222***.

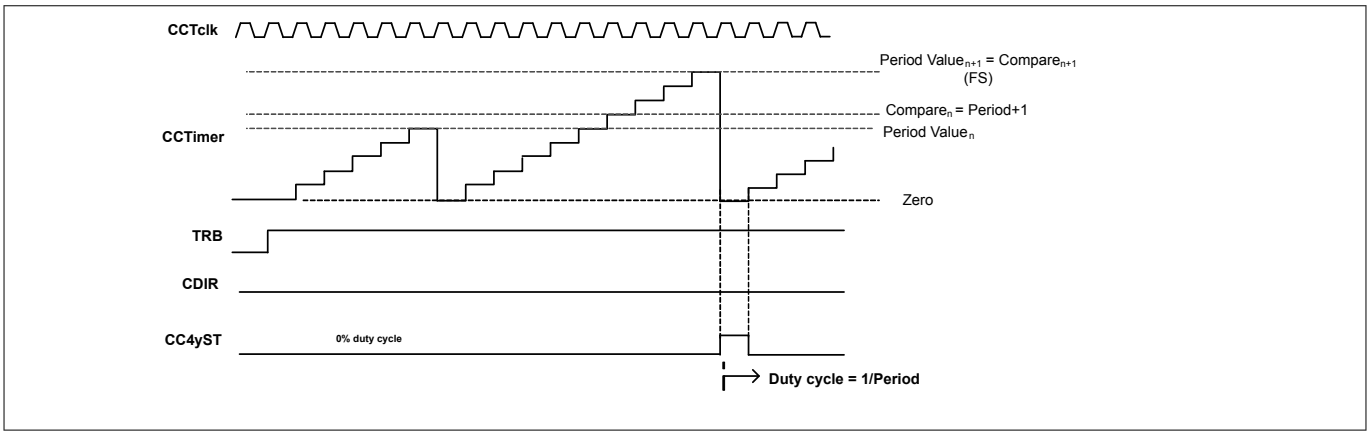


Figure 221 PWM with 0% duty cycle - Edge Aligned Mode

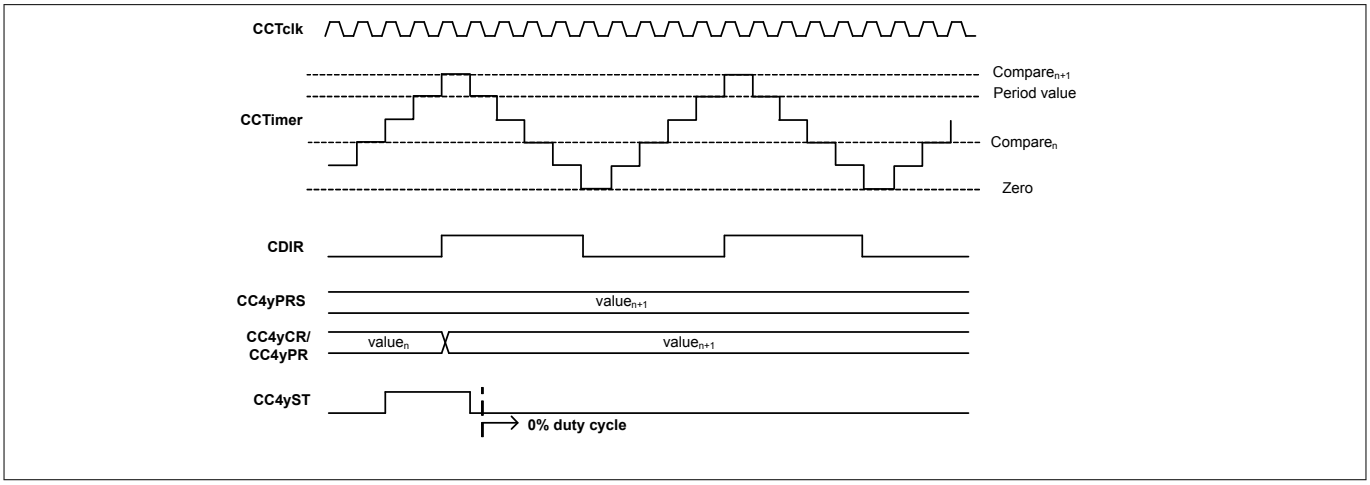


Figure 222 PWM with 0% duty cycle - Center Aligned Mode

20.2.8.2 Prescaler Usage

In Normal Prescaler Mode, the frequency of the f_{tclk} fed to the specific CC4y is chosen from the ***Table 250***, by setting the ***CC4yPSC***.PSIV with the required value.

In Floating Prescaler Mode, the frequency of the f_{tclk} can be modified over a selected timeframe, within the values specified in ***Table 250***. This mechanism is specially useful if, when in capture mode, the dynamic of the capture triggers is very slow or unknown.

In Capture Mode, the Floating Prescaler value is incremented by 1 every time that a timer overflow happens and it is set with the initial programmed value when a capture event happens, see ***Figure 223***.

When using the Floating Prescaler Mode in Capture Mode, the timer should be cleared each time that a capture event happens, ***CC4yTC***.CAPC = 11_B. By operating the Capture mode in conjunction with the Floating Prescaler, even for capture signals that have a periodicity bigger than 16 bits, it is possible to use just a single CCU4 Timer Slice without monitoring the interrupt event of the timer overflow, cycle by cycle. For this the user just needs to know what is the timer captured value and the actual prescaler configuration at the time that the capture event occurred. These values are contained in each CC4yCxV register.

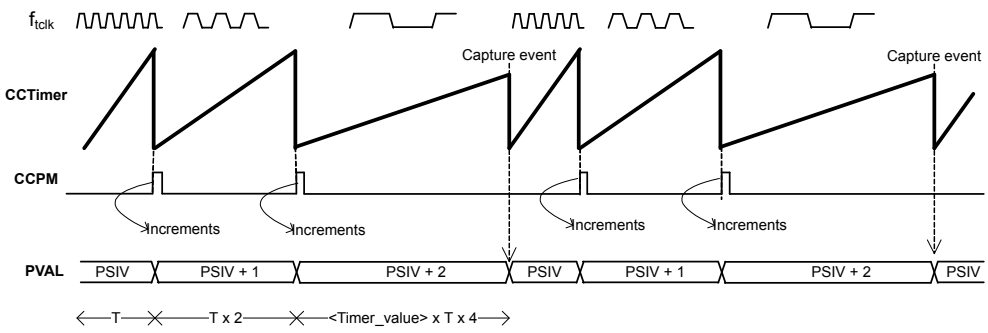


Figure 223 Floating Prescaler capture mode usage

When in Compare Mode, the Floating Prescaler function may be used to achieve a fractional PWM frequency or to perform some frequency modulation.

The same incrementing by 1_D mechanism is done every time that a overflow/underflow of the Timer occurs and the actual Prescaler value, doesn't match the one programmed into the ***CC4yFPC***.PCMP register.

When a Compare Match from the Timer occurs and the actual Prescaler value is equal to the one programmed on the ***CC4yFPC***.PCMP register, then the Prescaler value is set with the initial value, ***CC4yPSC***.PSIV, when the next occurrence of a timer overflow/underflow.

In ***Figure 224***, the Compare value of the Floating Prescaler was set to PSIV + 2. Every time that a timer overflow occurs, the value of the Prescaler is incremented by 1, which means that if we give f_{tclk} as the reference frequency for the ***CC4yPSC***.PSIV value, we have $f_{tclk}/2$ for ***CC4yPSC***.PSIV + 1 and $f_{tclk}/4$ for ***CC4yPSC***.PSIV + 2.

The period over time of the counter becomes:

$$\text{Period} = (1/f_{tclk} + 2/f_{tclk} + 4/f_{tclk})/3$$

Equation 36

The same mechanism is used in Center Aligned Mode, but to keep the rising arcade and falling arcade always symmetrical, instead of the overflow of the timer, the underflow is used, see ***Figure 225***.

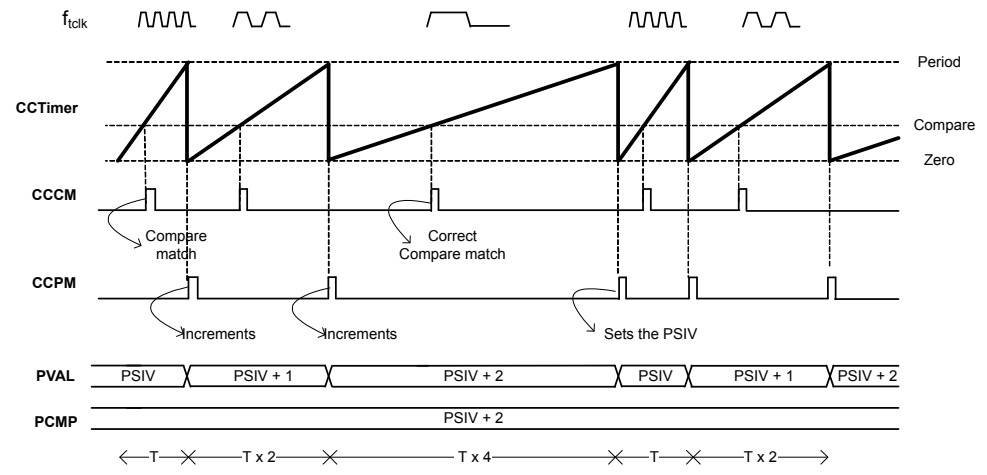


Figure 224 Floating Prescaler compare mode usage - Edge Aligned

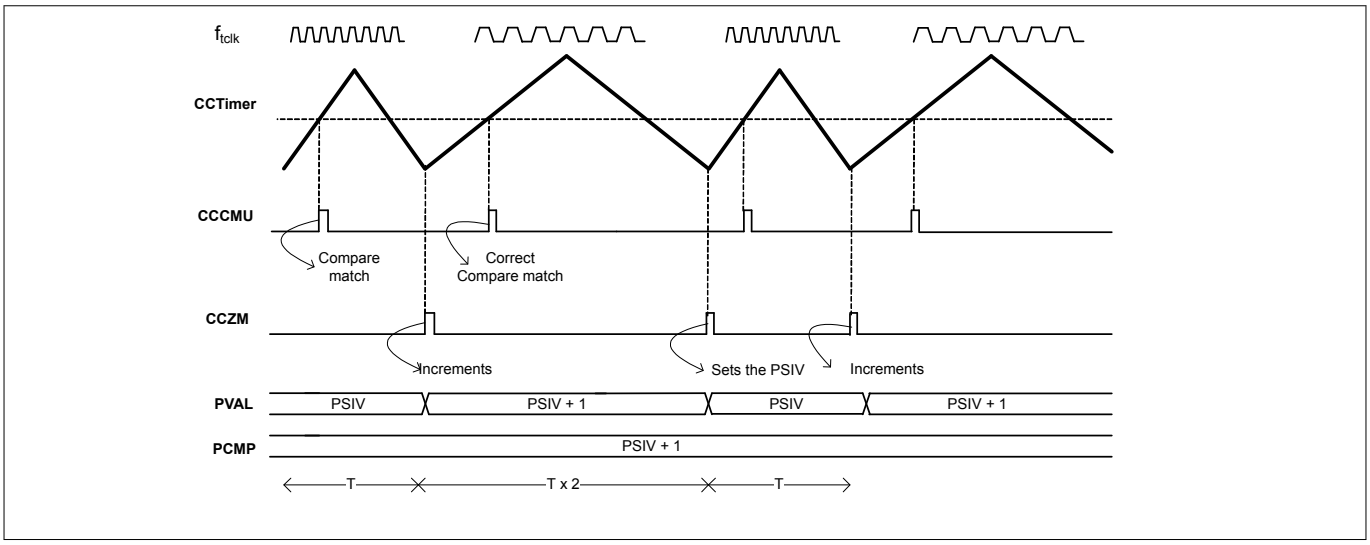


Figure 225 Floating Prescaler compare mode usage - Center Aligned

20.2.8.3 PWM Dither

The Dither functionality can be used to achieve a very fine precision on the periodicity of the output state in compare mode. The value set in the dither compare register, ***CC4yDIT***.DCV is crosschecked against the actual value of the dither counter and every time that the dither counter is smaller than the comparison value one of the follows actions is taken:

- The period is extended for 1 clock cycle - ***CC4yTC***.DITHE = 01_B; in edge aligned mode
- The period is extended for 2 clock cycles - ***CC4yTC***.DITHE = 01_B; in center aligned mode
- The comparison match while counting up (***CC4yTCST***.CDIR = 0_B) is delayed (this means that the status bit is going to stay in the SET state 1 cycle less) for 1 clock cycle - ***CC4yTC***.DITHE = 10_B;
- The period is extended for 1 clock cycle and the comparison match while counting up is delayed for 1 clock cycle - ***CC4yTC***.DITHE = 11_B; in edge aligned mode
- The period is extended for 2 clock cycles and the comparison match while counting up is delayed for 1 clock cycle; center aligned mode

The bit reverse counter distributes the number programmed in the ***CC4yDIT***.DCV throughout a window of 16 timer periods.

Table 251 describes the bit reverse distribution versus the programmed value on the ***CC4yDIT***.DCV field. The fields marked as '0' indicate that in that counter period, one of the above described actions, is going to be performed.

Table 251 Bit reverse distribution

	DCV															
Dither counter	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
4	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
C	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0
2	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
A	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0

Table 251 Bit reverse distribution (continued)

	DCV															
Dither counter	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
6	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
E	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
5	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
D	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
3	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
B	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0
7	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
F	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

The bit reverse distribution versus the programmed ***CC4yDIT***.DCV value results in the following values for the Period and duty cycle:

DITHE = 01_B

$$\text{Period} = [(16 - \text{DCV}) \times T + \text{DCV} \times (T + 1)]/16; \text{ in Edge Aligned Mode}$$

Equation 37

$$\text{Duty cycle} = [(16 - \text{DCV}) \times d/T + \text{DCV} \times (d + 1)/(T + 1)]/16; \text{ in Edge Aligned Mode}$$

Equation 38

$$\text{Period} = [(16 - \text{DCV}) \times T + \text{DCV} \times (T + 2)]/16; \text{ in Center Aligned Mode}$$

Equation 39

$$\text{Duty cycle} = [(16 - \text{DCV}) \times d/T + \text{DCV} \times (d + 2)/(T + 2)]/16; \text{ in Center Aligned Mode}$$

Equation 40

DITHE = 10

$$\text{Period} = T; \text{ in Edge Aligned Mode}$$

Equation 41

$$\text{Duty cycle} = [(16 - \text{DCV}) \times d/T + \text{DCV} \times (d - 1)/T]/16; \text{ in Edge Aligned Mode}$$

Equation 42

Period = T; in Center Aligned Mode

Equation 43

Duty cycle = $[(16 - DCV) \times d/T + DCV \times (d - 1)/T]/16$; in Center Aligned Mode

Equation 44

DITHE = 11_B

Period = $[(16 - DCV) \times T + DCV \times (T + 1)]/16$; in Edge Aligned Mode

Equation 45

Duty cycle = $[(16 - DCV) \times d/T + DCV \times d/(T + 1)]/16$; in Edge Aligned Mode

Equation 46

Period = $[(16 - DCV) \times T + DCV \times (T + 2)]/16$; in Center Aligned Mode

Equation 47

Duty cycle = $[(16 - DCV) \times d/T + DCV \times (d + 1)/(T + 2)]/16$; in Center Aligned Mode

Equation 48

where:

T - Original period of the signal, see ***Chapter 20.2.4.6***

d - Original duty cycle of the signal, see ***Chapter 20.2.4.6***

20.2.8.4 Capture Mode Usage

Each Timer Slice can make use of 2 or 4 capture registers. Using only 2 capture registers means that only 1 Event was linked to a captured trigger. To use the four capture registers, both capture triggers need to be mapped into an Event (it can be the same signal with different edges selected or two different signals) or the ***CC4yTC***.SCE field needs to be set to 1, which enables the linking of the 4 capture registers.

The internal slice mechanism for capturing is the same for the capture trigger 1 or capture trigger 0.

Different Capture Events - SCE = 0

Capture trigger 1 (CCcapt1) is appointed to the capture register 2, ***CC4yC2V*** and capture register 3, ***CC4yC3V***, while trigger 0 (CCcapt0) is appointed to capture register 1, ***CC4yC1V*** and 0, ***CC4yC0V***.

In each CCcapt0 event, the timer value is stored into ***CC4yC1V*** and the value of the ***CC4yC1V*** is transferred into the ***CC4yC0V***.

In each CCcapt1 event, the timer value is stored into capture register ***CC4yC3V*** and the value of the capture register ***CC4yC3V*** is transferred into ***CC4yC2V***.

The capture/transfer mechanism only happens if the specific register is not full. A capture register becomes full when receives a new value and becomes empty after the SW has read back the value.

The full flag is cleared every time that the SW reads back the ***CC4yC0V***, ***CC4yC1V***, ***CC4yC2V*** or ***CC4yC3V*** register. The SW can be informed of a new capture trigger by enabling the interrupt source linked to the specific Event. This means that every time that a capture is made an interrupt pulse is generated.

In the case that the Floating Prescaler Mode is being used, the actual value of the clock division is also stored in the capture register (CC4yCxV).

Figure 226 shows an example of how the capture/transfer may be used in a Timer Slice that is using a external signal as count function (to measure the velocity of a rotating device), and an equidistant capture trigger that is used to dictate the timestamp for the velocity calculation (two Timer waveforms are plotted, one that exemplifies the clearing of the timer in each capture event and another without the clearing function active).

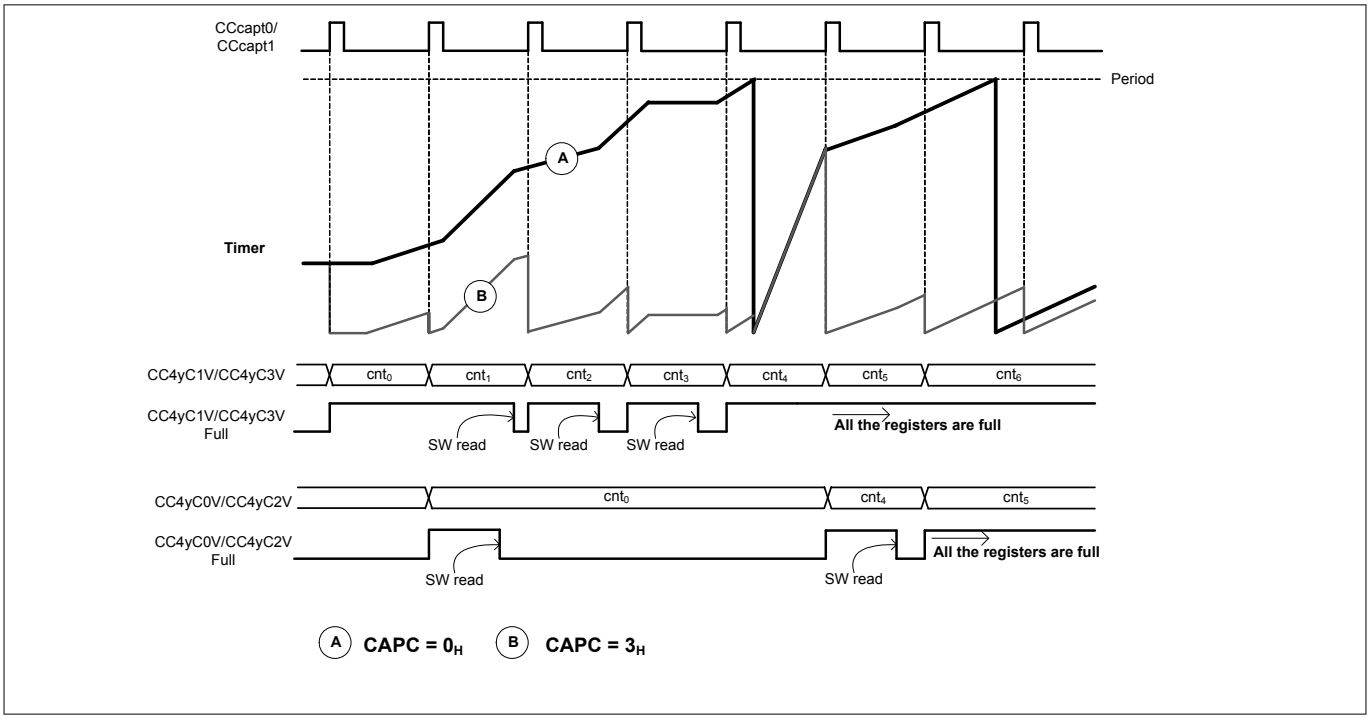


Figure 226 Capture mode usage - single channel

Same Capture Event - SCE = 1

If the ***CC4yTC***.SCE is set to 1, all the four capture registers are chained together, emulating a fifo with a depth of 4. In this case, only the capture trigger 1, CCcapt1, is used to perform a capture event.

As an example for this mode, one can consider the case where one Timer Slice is being used in capture mode with SCE = 1_B, with another external signal that controls the counting. This timer slice can be incremented at different speeds, depending on the frequency of the counting signal.

An additional Timer Slice is used to control the capture trigger, dictating the time stamp for the capturing.

A simple scheme for this can be seen in ***Figure 227***. The CC40ST output of slice 0 was used as capture trigger in the CC41 slice (active on rising and falling edge). The CC40ST output is used as known timebase marker, while the slice timer used for capture is being controlled by external events, e.g. external count.

Due to the fact that we have available 4 capture registers, every time that the SW reads back the complete set of values, 3 speed profiles can be measured.

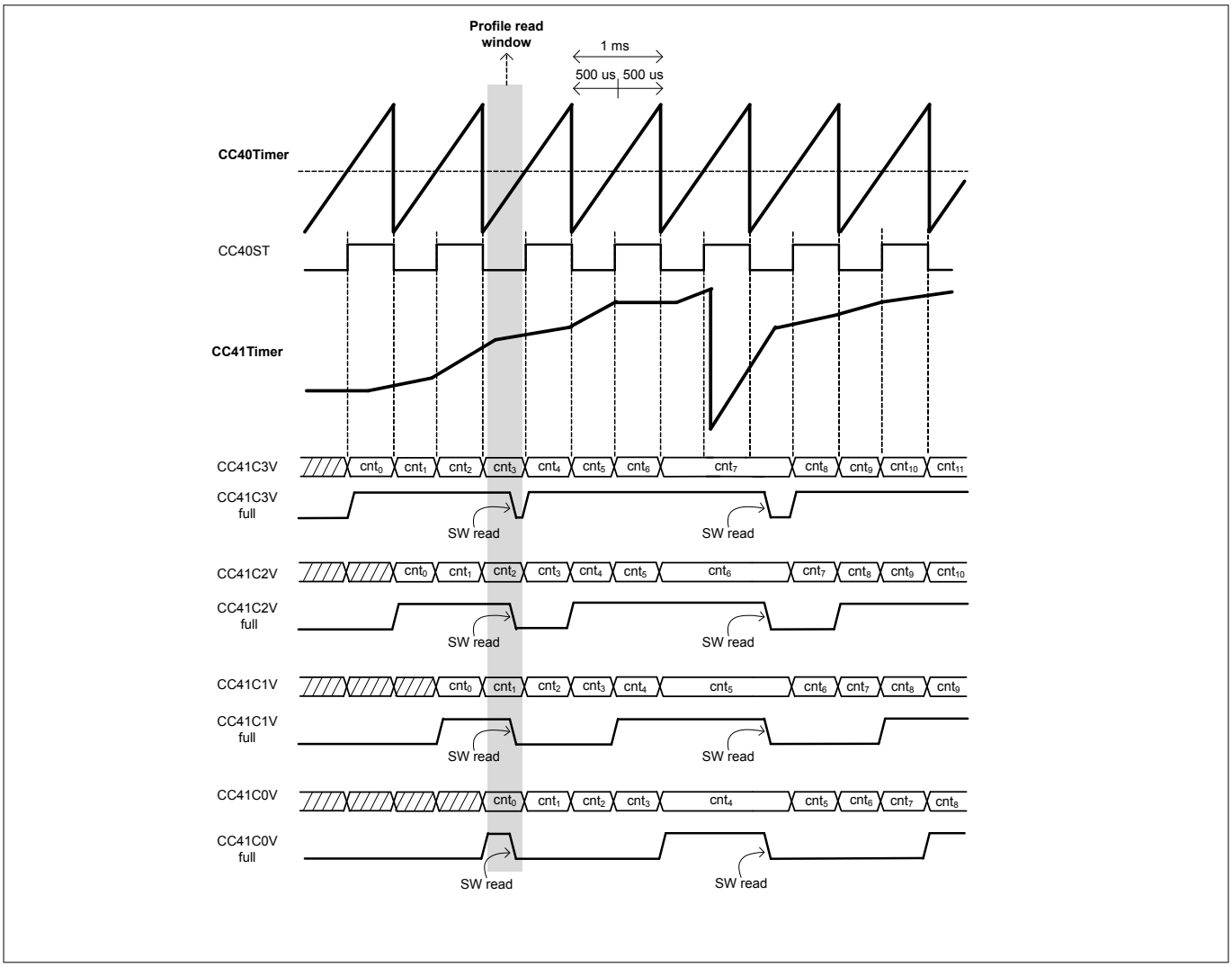


Figure 227 Three Capture profiles - *CC4yTC*.SCE = 1

To calculate the three different profiles in ***Figure 227***, the 4 capture registers need to be read during the pointed read window. After that, the profile calculation is done:

Profile 1 = $CC41C1V_{info}$ - $CC41C0V_{info}$

Profile 2 = $CC41C2V_{info}$ - $CC41C1V_{info}$

Profile 3= $CC41C3V_{info}$ - $CC41C2V_{info}$

Note: This is an example and therefore several Timer Slice configurations and software loops can be implemented.

High Dynamics Capturing

In some cases the dynamics of the capture trigger(s) may vary greatly over time. This will impose that the software needs to be prepared for the worst case scenario, where the frequency of the capture triggers may be very high. In applications where cycle-by-cycle calculation is needed (calculation in each capture trigger), then this constraints needs to be met by the software. Nevertheless for applications where a cycle-by-cycle calculation is not needed, the software can read back the FIFO data register in a periodic base and fetch all the data that has been captured so far, ***Figure 228***.

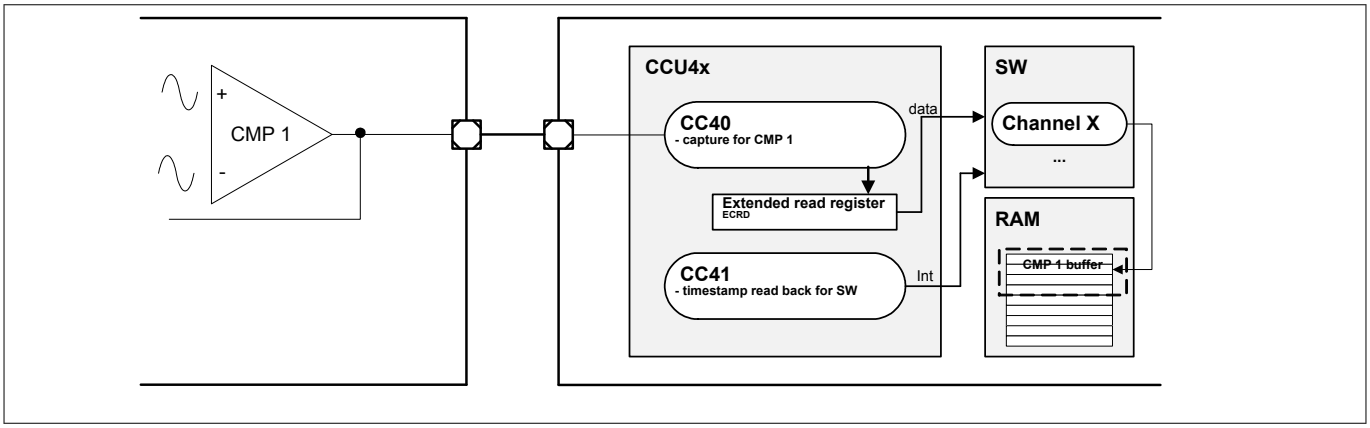


Figure 228 High dynamics capturing with software controlled timestamp

In this scenario, the software/CPU will read back the complete set of capture registers (2 or 4 depending on the chosen configuration), every time that an interrupt is triggered from the timestamp timer (the periodicity of this timer can also be adjusted on-the-fly).

Due to the fact that every capture register offers a full flag status bit, the software/CPU can always read back the complete set of registers. At the time of the data processing, this full flag is then checked, indicating if this value needs to be processed or not.

This FIFO read back functionality can also be used for applications that impose a heavy load on the system, which may not guarantee fixed access times to read back the captured data.

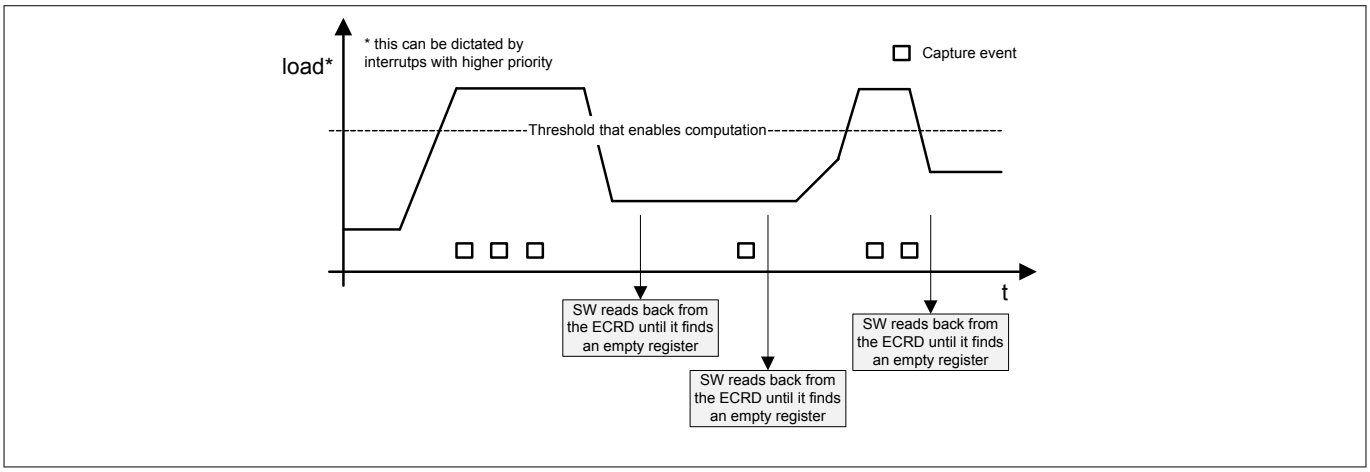


Figure 229 Extended read back during high load

Capture Grouping

In applications where multiple capture Timers are needed and the priority of the capture routines, does not imply that a cycle-by-cycle calculation needs to be done for every event, it may be suitable to group all the timers in the same CCU4x unit, ***Figure 230***.

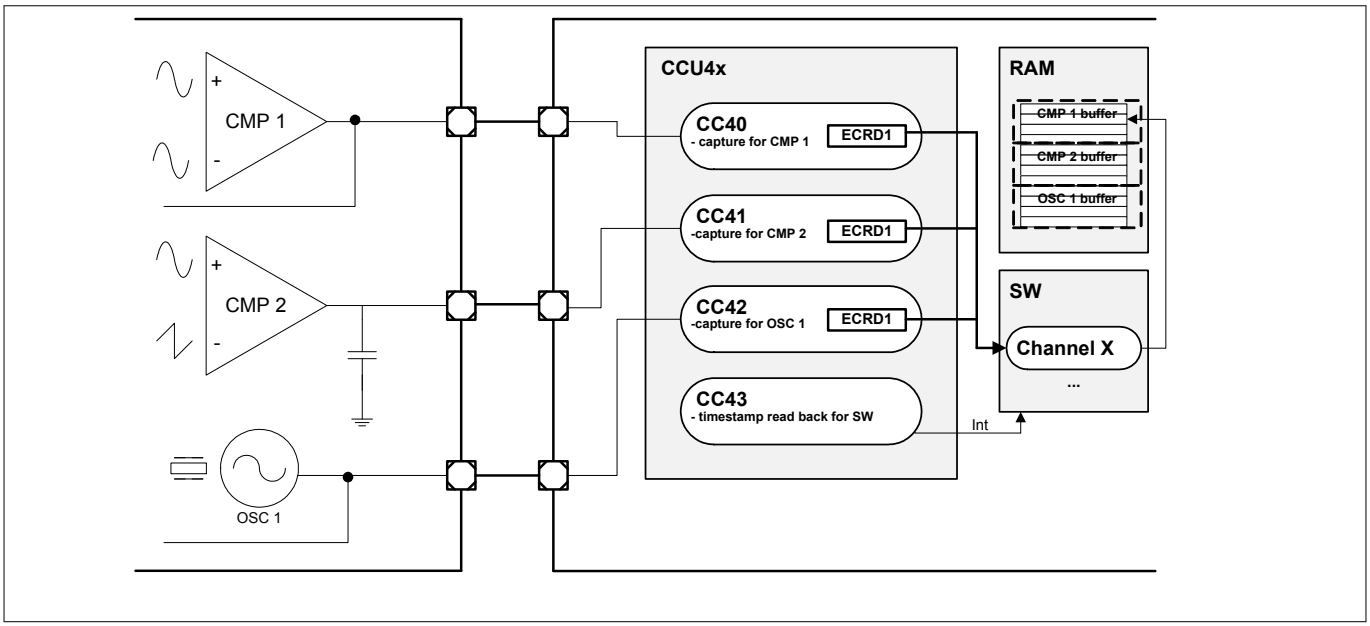


Figure 230 Capture grouping with extended read back

By setting the ECM bitfield for the TImer Slices used for capturing, the extended read back mode enables the reading back of data always in the proper capture order (from oldest to newest data). A timestamp timer is then used to trigger the Software/CPU to read back all the capture data present in the Timer Slices.

Every time that the interrupt is sensed, the Software/CPU (in this example) reads back the complete set of capture registers (via the ECRD address) for all Timer Slices. Due to the fact that each data read has a full flag indicator, the Software/CPU can read back the complete set of capture registers from all timers. This allows a fixed memory allocation that is as big as the number of captured registers, ***Figure 231*** (in this example 4 capture registers for each Timer Slice are being used).

The additional lost value bitfield (LCV) on the header of each ECRD data, will indicate if any capture trigger was lost between read operations (this can happen if the capture triggers are faster than the routine that is reading back the values).

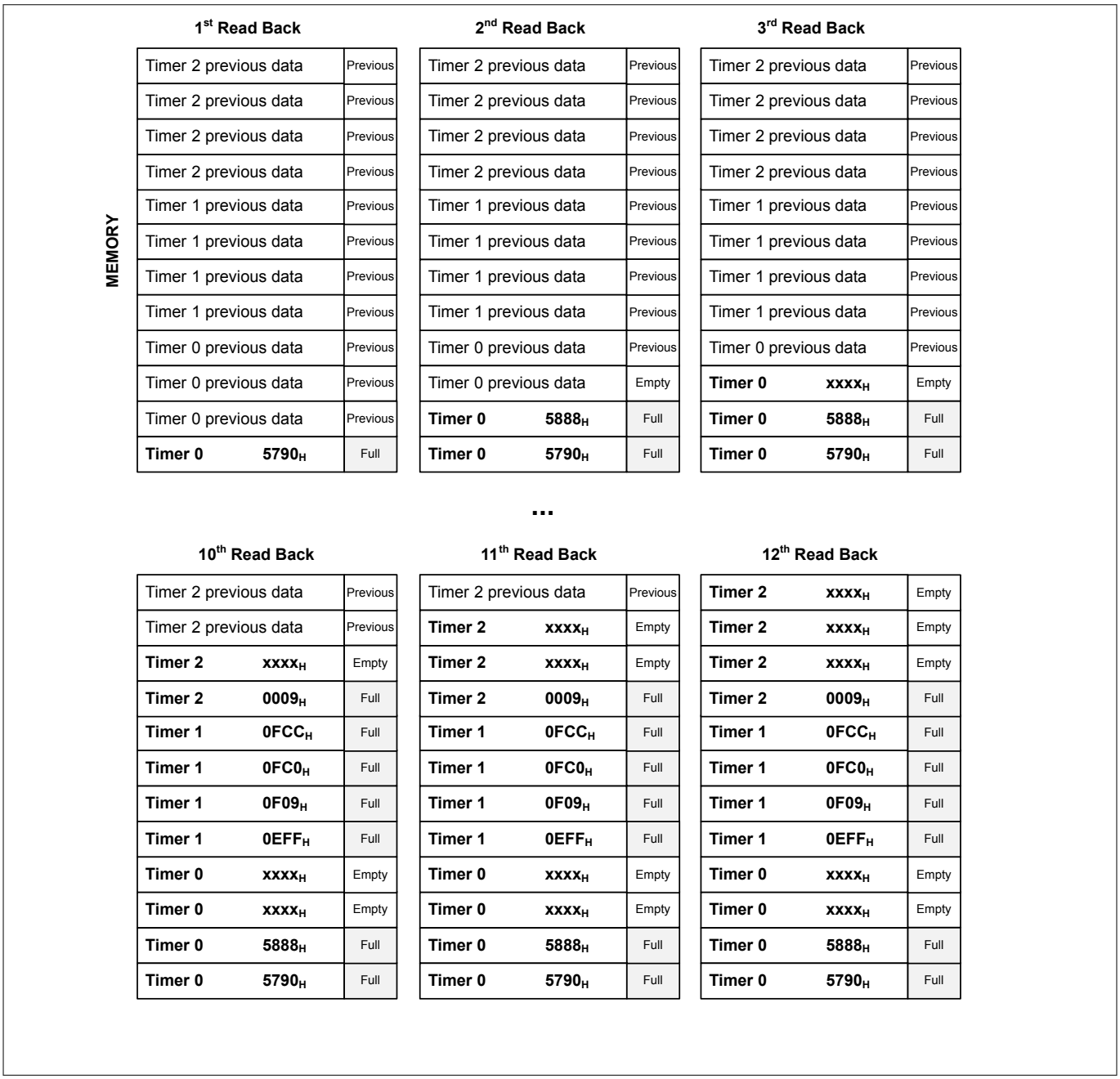


Figure 231 Memory structure for extended read back

20.3 Service Request Generation

Each CCU4 slice has an interrupt structure as the one in ***Figure 232***. The register ***CC4yINTS*** is the status register for the interrupt sources. Each dedicated interrupt source can be set or cleared by SW, by writing into the specific bit in the ***CC4ySWS*** and ***CC4ySWR*** registers respectively.

Each interrupt source can be enabled/disabled via the ***CC4yINTE*** register. An enabled interrupt source will always generate a pulse on the service request line even if the specific status bit was not cleared. ***Table 252*** describes the interrupt sources of each CCU4 slice.

The interrupt sources, Period Match while counting up and one Match while counting down are ORed together. The same mechanism is applied to the Compare Match while counting up and Compare Match while counting down.

The interrupt sources for the external events are directly linked with the configuration set on the ***CC4yINS2***.EVxEM. If an event is programmed to be active on both edges, that means that service request pulse is going to be generated when any transition on the external signal is detected. If the event is linked with a level function, the ***CC4yINS2***.EVxEM still can be programmed to enable a service request pulse. The TRAP event doesn't need any of extra configuration for generating the service request pulse when the slice enters the TRAP state.

Table 252 Interrupt sources

Signal	Description
CCINEV0_E	Event 0 edge(s) information from event selector. Used when an external signal should trigger an interrupt.
CCINEV1_E	Event 1 edge(s) information from event selector. Used when an external signal should trigger an interrupt.
CCINEV2_E	Event 2 edge(s) information from event selector. Used when an external signal should trigger an interrupt.
CCPM_U	Period Match while counting up
CCCM_U	Compare Match while counting up
CCCM_D	Compare Match while counting down
CCOM_D	One Match while counting down
Trap state set	Entering Trap State. Will set the E2AS

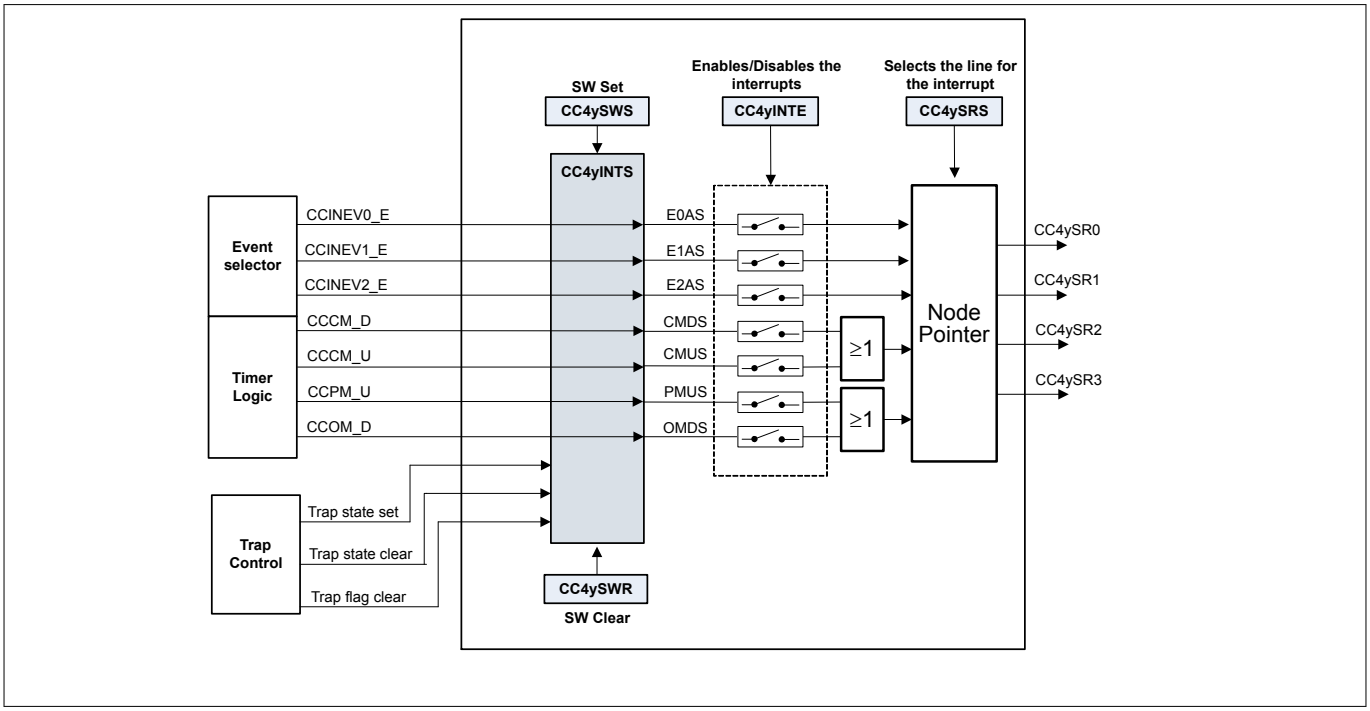


Figure 232 Slice interrupt structure overview

Each of the interrupt events can then be forwarded to one of the slice's four service request lines, ***Figure 233***. The value set on the ***CC4ySRS*** controls which interrupt event is mapped into which service request line.

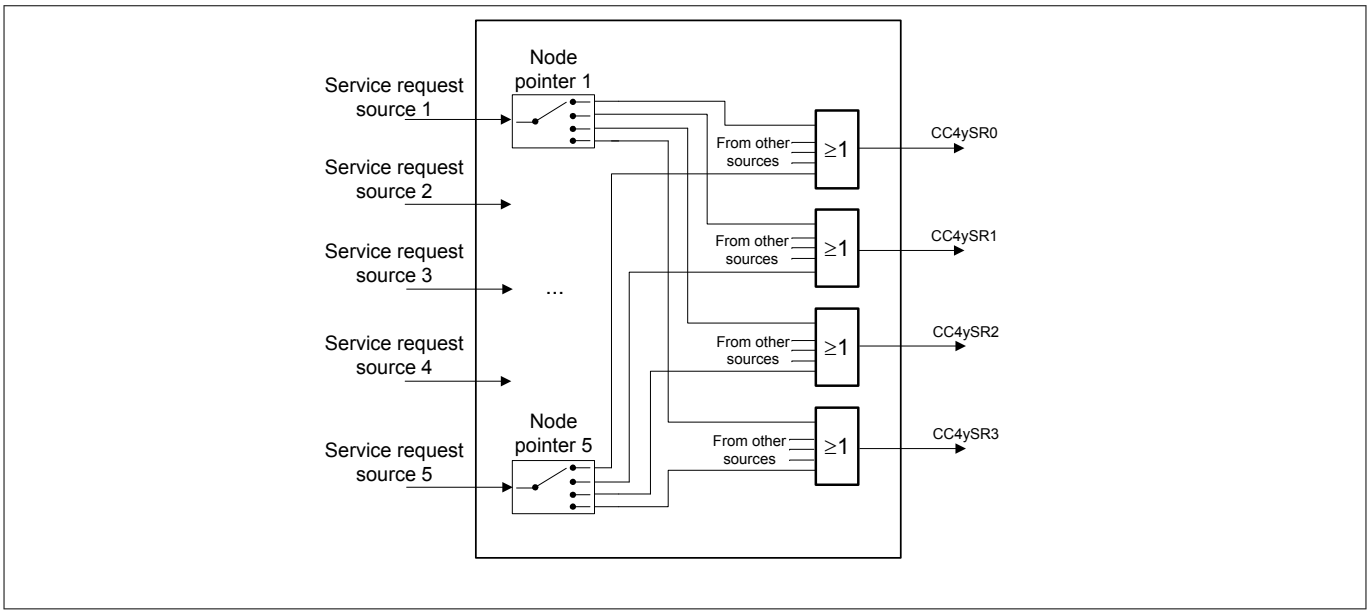


Figure 233 Slice Interrupt Node Pointer overview

The four service request lines of each slice are OR together inside the kernel of the CCU4, see ***Figure 234***. This means that there are only four service request lines per CCU4, that can have in each line interrupt requests coming from different slices.

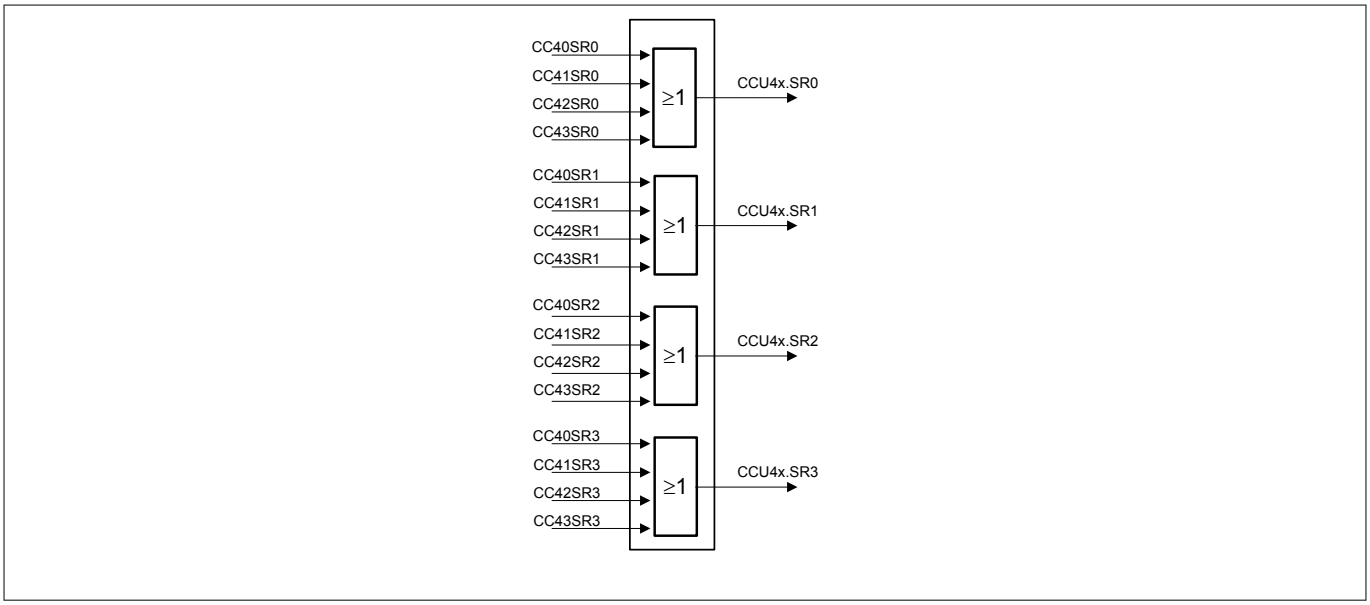


Figure 234 CCU4 service request overview

20.4 Debug Behavior

In suspend mode, the functional clocks for all slices as well the prescaler are stopped. The registers can still be accessed by the CPU (read only). This mode is useful for debugging purposes, e.g. where the current device status should be frozen in order to get a snapshot of the internal values. In suspend mode, all the slice timers are stopped. The suspend mode is non-intrusive concerning the register bits. This means register bits are not modified by hardware when entering or leaving the suspend mode.

Entry into suspend mode can be configured at the kernel level by means of the field ***GCTRL***.SUSCFG.

The module is only functional after the suspend signal becomes inactive.

20.5 Power, Reset and Clock

The following sections describe the operating conditions, characteristics and timing requirements for the CCU4. All the timing information is related to the module clock, f_{ccu4}.

20.5.1 Clocks

Module Clock

The module clock of the CCU4 module is described in the SCU chapter as f_{PCLK}.

The bus interface clock of the CCU4 module is described in the SCU chapter as f_{MCLK}.

It is possible to disable the module clock for the CCU4 via the ***GSTAT*** register, nevertheless, there may be a dependency of the f_{ccu4} through the different CCU4 instances. One should address the SCU Chapter for a complete description of the product clock scheme.

If module clock dependencies exist through different IP instances, then one can disable the module clock internally inside the specific CCU4, by disabling the prescaler (***GSTAT***.PRB = 0_B).

External Clock

It is possible to use an external clock as source for the prescaler, and consequently for all the timer Slices, CC4y. This external source can be connected to one of the CCU4x.CLK[C...A] inputs.

This external source is nevertheless synchronized against f_{ccu4}.

Table 253 External clock operating conditions

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Frequency	f_{eclk}	–	–	$f_{ccu4}/4$	MHz	
ON time	ton_{eclk}	$2T_{ccu4}$ [52)53)]	–	–	ns	
OFF time	$toff_{eclk}$	$2T_{ccu4}$ [52)53)]	–	–	ns	Only the rising edge is used

20.5.2 Power

The CCU4 is inside the power core domain, therefore no special considerations about power up or power down sequences need to be taken. For an explanation about the different power domains, please address the SCU (System Control Unit) chapter.

An internal power down mode for the CCU4, can be achieved by disabling the clock inside the CCU4 itself. For this one should set the ***GSTAT*** register with the default reset value (via the idle mode set register, ***GIDLS***).

20.6 Initialization and System Dependencies

20.6.1 Initialization Sequence

The initialization sequence for an application that is using the CCU4, should be the following:

52 Only valid if the signal was not previously synchronized/generated with the fccu4 clock (or a synchronous clock)

53 50% duty cycle is not obligatory

1st Step:

Enable the CCU4 clock via the specific SCU register, CGATCLR0.

2nd Step:

Enable the prescaler block, by writing 1_B to the ***GIDLC***.SPRB field.

3rd Step:

Configure the global CCU4 register ***GCTRL***

4th Step:

Configure all the registers related to the required Timer Slice(s) functions, including the interrupt/service request configuration.

5th Step:

If needed, configure the startup value for a specific Compare Channel Status, of a Timer Slice, by writing 1_B to the specific ***GCSS***.SyTS.

6th Step:

Enable the specific timer slice(s), CC4y, by writing 1 to the specific ***GIDLC***.CSyI.

7th Step:

For all the Timer Slices that should be started synchronously via SW, the specific system register localized in the SCU, CCUCON, that enables a synchronous timer start should be addressed. The SCU.GLCSTxx input signal needs to be configured previously as a start function, see ***Chapter 20.2.5.1***.

20.6.2 System Dependencies

Each CCU4 may have different dependencies regarding module and bus clock frequencies. This dependencies should be addressed in the SCU and System Architecture Chapters.

Dependencies between several peripherals, regarding different clock operating frequencies may also exist. This should be addressed before configuring the connectivity between the CCU4 and some other peripheral.

The following topics must be taken into consideration for good CCU4 and system operation:

- CCU4 module clock must be at maximum two times faster than the module bus interface clock
- Module input triggers for the CCU4 must not exceed the module clock frequency (if the triggers are generated internally in the device)
- Module input triggers for the CCU4 must not exceed the frequency dictated in ***Chapter 20.5.1***
- Frequency of the CCU4 outputs used as triggers/functions on other modules, must be crosschecked on the end point
- Applying and removing CCU4 from reset, can cause unwanted operations in other modules. This can occur if the modules are using CCU4 outputs as triggers/functions.

20.7 Registers

Registers Overview

The absolute register address is calculated by adding:
Module Base Address + Offset Address

Table 254 Registers Address Space

Module	Base Address	End Address	Note
CCU40	48040000_H	$48043FFF_H$	

Table 254 Registers Address Space (continued)

Module	Base Address	End Address	Note
CCU41	48044000_H	$48047FFF_H$	

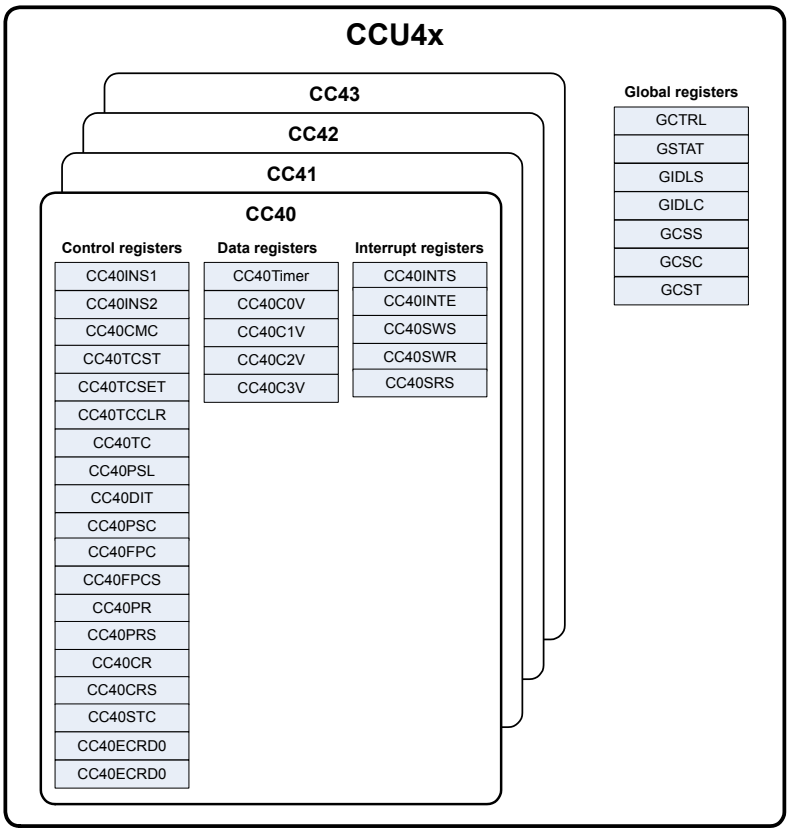


Figure 235 CCU4 registers overview

Table 255 Register Overview of CCU4

Short Name	Description	Offset Addr.[54]	Access Mode		Description see
			Read	Write	
CCU4 Global Registers					
GCTRL	Module General Control Register	0000_H	U, PV	U, PV	Page 682
GSTAT	General Slice Status Register	0004_H	U, PV	BE	Page 683
GIDLS	General Idle Enable Register	0008_H	U, PV	U, PV	Page 684
GIDLC	General Idle Disable Register	$000C_H$	U, PV	U, PV	Page 686
GCSS	General Channel Set Register	0010_H	U, PV	U, PV	Page 686
GCSC	General Channel Clear Register	0014_H	U, PV	U, PV	Page 688
GCST	General Channel Status Register	0018_H	U, PV	BE	Page 690

54 The absolute register address is calculated as follows: Module Base Address + Offset Address (shown in this column)

Table 255 Register Overview of CCU4 (continued)

Short Name	Description	Offset Addr.[54]	Access Mode		Description see
			Read	Write	
MIDR	Module Identification Register	0080_H	U, PV	BE	Page 692
CC4y Registers, y = 0...3, n = y + 1					
CC4yINS1	Input Selector Unit Configuration Register 1	$0nD8_H$	U, PV	U, PV	Page 693
CC4yINS2	Input Selector Unit Configuration Register 2	$0n00_H$	U, PV	U, PV	Page 694
CC4yCMC	Connection Matrix Configuration	$0n04_H$	U, PV	U, PV	Page 695
CC4yTST	Timer Run Status	$0n08_H$	U, PV	BE	Page 698
CC4yTCSET	Timer Run Set	$0n0C_H$	U, PV	U,PV	Page 698
CC4yTCCLR	Timer Run Clear	$0n10_H$	U, PV	U, PV	Page 699
CC4yTC	General Timer Configuration	$0n14_H$	U, PV	U, PV	Page 699
CC4yPSL	Output Passive Level Configuration	$0n18_H$	U, PV	U, PV	Page 703
CC4yDIT	Dither Configuration	$0n1C_H$	U, PV	BE	Page 703
CC4yDITS	Dither Shadow Register	$0n20_H$	U, PV	U, PV	Page 704
CC4yPSC	Prescaler Configuration	$0n24_H$	U, PV	U, PV	Page 704
CC4yFPC	Prescaler Compare Value	$0n28_H$	U, PV	U, PV	Page 705
CC4yFPCS	Prescaler Shadow Compare Value	$0n2C_H$	U, PV	U, PV	Page 706
CC4yPR	Timer Period Value	$0n30_H$	U, PV	BE	Page 706
CC4yPRS	Timer Period Shadow Value	$0n34_H$	U, PV	U, PV	Page 707
CC4yCR	Timer Compare Value	$0n38_H$	U, PV	BE	Page 707
CC4yCRS	Timer Compare Shadow Value	$0n3C_H$	U, PV	U, PV	Page 708
CC4yTIMER	Timer Current Value	$0n70_H$	U, PV	U, PV	Page 708
CC4yC0V	Capture Register 0 Value	$0n74_H$	U, PV	BE	Page 709
CC4yC1V	Capture Register 1Value	$0n78_H$	U, PV	BE	Page 710
CC4yC2V	Capture Register 2 Value	$0n7C_H$	U, PV	BE	Page 710
CC4yC3V	Capture Register 3 Value	$0n80_H$	U, PV	BE	Page 711
CC4yINTS	Interrupt Status	$0nA0_H$	U, PV	BE	Page 712
CC4yINTE	Interrupt Enable	$0nA4_H$	U, PV	U, PV	Page 713
CC4ySRS	Interrupt Configuration	$0nA8_H$	U, PV	U, PV	Page 714
CC4ySWS	Interrupt Status Set	$0nAC_H$	U, PV	U, PV	Page 716
CC4ySWR	Interrupt Status Clear	$0nB0_H$	U, PV	U, PV	Page 717
CC4ySTC	Shadow Transfer Control	$0nB4_H$	U, PV	U, PV	Page 718
CC4yECRD0	Extended Read Back 0	$0nB8_H$	U, PV	BE	Page 721
CC4yECRD1	Extended Read Back 1	$0nBC_H$	U, PV	BE	Page 722

54 The absolute register address is calculated as follows: Module Base Address + Offset Address (shown in this column)

20.7.1 Global Registers

20.7.1.1 Register GCTRL

The register contains the global configuration fields that affect all the timer slices inside CCU4.

GCTRL Address: 0000_H

Global Control Register Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSDE		MSE3	MSE2	MSE1	MSE0	SUSCFG		0		PCIS		0	PRBC		
rw		rw	rw	rw	rw	rw		r		rw		r	rw		

Field	Bits	Type	Description
PRBC	2:0	rw	**Prescaler Clear Configuration** This register controls how the prescaler Run Bit and internal registers are cleared. 000_B SW only 001_B ***GSTAT***.PRB and prescaler registers are cleared when the Run Bit of CC40 is cleared. 010_B ***GSTAT***.PRB and prescaler registers are cleared when the Run Bit of CC41 is cleared. 011_B ***GSTAT***.PRB and prescaler registers are cleared when the Run Bit of CC42 is cleared. 100_B ***GSTAT***.PRB and prescaler registers are cleared when the Run Bit of CC43 is cleared.
PCIS	5:4	rw	**Prescaler Input Clock Selection** 00_B Module clock 01_B CCU4x.ECLKA 10_B CCU4x.ECLKB 11_B CCU4x.ECLKC
SUSCFG	9:8	rw	**Suspend Mode Configuration** This field controls the entering in suspend mode for all the CAPCOM4 slices. 00_B Suspend request ignored. The module never enters in suspend 01_B Stops all the running slices immediately. Safe stop is not applied. 10_B Stops the block immediately and clamps all the outputs to PASSIVE state. Safe stop is applied. 11_B Waits for the roll over of each slice to stop and clamp the slices outputs. Safe stop is applied.

(continued)

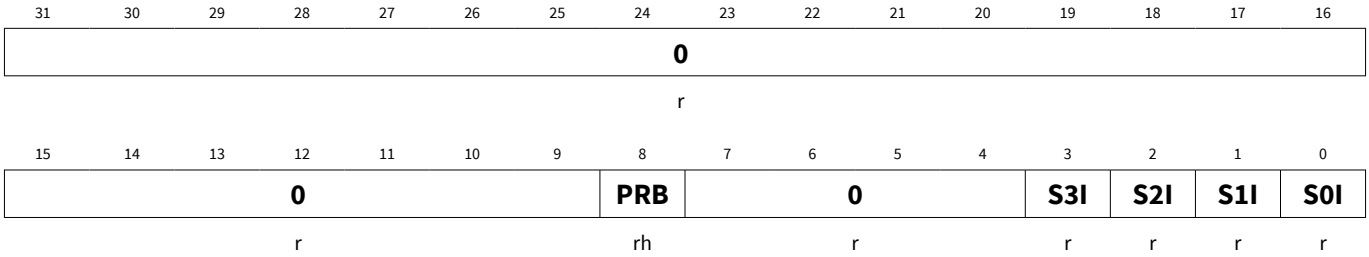
Field	Bits	Type	Description
MSE0	10	rw	**Slice 0 Multi-Channel shadow transfer enable** When this field is set, a shadow transfer of slice 0 can be requested not only by SW but also via the CCU4x.MCSS input. 0_B Shadow transfer can only be requested by SW 1_B Shadow transfer can be requested via SW and via the CCU4x.MCSS input.
MSE1	11	rw	**Slice 1 Multi-Channel shadow transfer enable** When this field is set, a shadow transfer of slice 1 can be requested not only by SW but also via the CCU4x.MCSS input. 0_B Shadow transfer can only be requested by SW 1_B Shadow transfer can be requested via SW and via the CCU4x.MCSS input.
MSE2	12	rw	**Slice 2 Multi-Channel shadow transfer enable** When this field is set, a shadow transfer of slice 2 can be requested not only by SW but also via the CCU4x.MCSS input. 0_B Shadow transfer can only be requested by SW 1_B Shadow transfer can be requested via SW and via the CCU4x.MCSS input.
MSE3	13	rw	**Slice 3 Multi-Channel shadow transfer enable** When this field is set, a shadow transfer of slice 3 can be requested not only by SW but also via the CCU4x.MCSS input. 0_B Shadow transfer can only be requested by SW 1_B Shadow transfer can be requested via SW and via the CCU4x.MCSS input.
MSDE	15:14	rw	**Multi-Channel shadow transfer request configuration** This field configures the type of shadow transfer requested via the CCU4x.MCSS input. The field ***CC4yTC***.MSEy needs to be set in order for this configuration to have any effect. 00_B Only the shadow transfer for period and compare values is requested 01_B Shadow transfer for the compare, period and prescaler compare values is requested 10_B Reserved 11_B Shadow transfer for the compare, period, prescaler and dither compare values is requested
0	3, 7:6, 31:16	r	**Reserved** A read always returns 0.

20.7.1.2 Register GSTAT

The register contains the status of the prescaler and each timer slice (idle mode or running).

GSTAT Address: 0004_H

Global Status Register Reset Value: $0000000F_H$



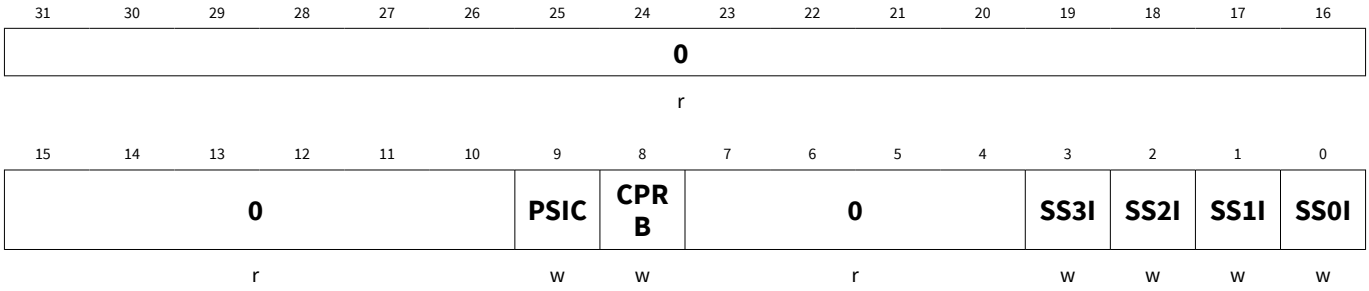
Field	Bits	Type	Description
S0I	0	r	**CC40 IDLE status** This bit indicates if the CC40 slice is in IDLE mode or not. In IDLE mode the clocks for the CC40 slice are stopped. 0_B Running 1_B Idle
S1I	1	r	**CC41 IDLE status** This bit indicates if the CC41 slice is in IDLE mode or not. In IDLE mode the clocks for the CC41 slice are stopped. 0_B Running 1_B Idle
S2I	2	r	**CC42 IDLE status** This bit indicates if the CC42 slice is in IDLE mode or not. In IDLE mode the clocks for the CC42 slice are stopped. 0_B Running 1_B Idle
S3I	3	r	**CC43 IDLE status** This bit indicates if the CC43 slice is in IDLE mode or not. In IDLE mode the clocks for the CC43 slice are stopped. 0_B Running 1_B Idle
PRB	8	rh	**Prescaler Run Bit** 0_B Prescaler is stopped 1_B Prescaler is running
0	7:4, 31:9	r	**Reserved** Read always returns 0.

20.7.1.3 Register GIDLS

Through this register one can set the prescaler and the specific timer slices into idle mode.

GIDLS Address: 0008_H

Global Idle Set Reset Value: 00000000_H



Field	Bits	Type	Description
SS0I	0	w	**CC40 IDLE mode set** Writing a 1_B to this bit sets the CC40 slice in IDLE mode. The clocks for the slice are stopped when in IDLE mode. When entering IDLE, the internal slice registers are not cleared. A read access always returns 0.
SS1I	1	w	**CC41 IDLE mode set** Writing a 1_B to this bit sets the CC41 slice in IDLE mode. The clocks for the slice are stopped when in IDLE mode. When entering IDLE, the internal slice registers are not cleared. A read access always returns 0.
SS2I	2	w	**CC42 IDLE mode set** Writing a 1_B to this bit sets the CC42 slice in IDLE mode. The clocks for the slice are stopped when in IDLE mode. When entering IDLE, the internal slice registers are not cleared. A read access always returns 0.
SS3I	3	w	**CC43 IDLE mode set** Writing a 1_B to this bit sets the CC43 slice in IDLE mode. The clocks for the slice are stopped when in IDLE mode. When entering IDLE, the internal slice registers are not cleared. A read access always returns 0.
CPRB	8	w	**Prescaler Run Bit Clear** Writing a 1_B into this register clears the Run Bit of the prescaler. Prescaler internal registers are not cleared. A read always returns 0.
PSIC	9	w	**Prescaler clear** Writing a 1_B to this register clears the prescaler counter. It also loads the PSIV into the PVAL field for all Timer Slices. This performs a re alignment of the timer clock for all Slices. The Run Bit of the prescaler is not cleared. A read always returns 0.
0	7:4, 31:10	r	**Reserved** Read always returns 0.

20.7.1.4 Register GIDLC

Through this register one can remove the prescaler and the specific timer slices from idle mode.

GIDLC Address: $000C_H$

Global Idle Clear Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0							SPRB	0				CS3I	CS2I	CS1I	CS0I
r							w	r				w	w	w	w

Field	Bits	Type	Description
CS0I	0	w	**CC40 IDLE mode clear** Writing a 1_B to this bit removes the CC40 from IDLE mode. A read access always returns 0.
CS1I	1	w	**CC41 IDLE mode clear** Writing a 1_B to this bit removes the CC41 from IDLE mode. A read access always returns 0.
CS2I	2	w	**CC42 IDLE mode clear** Writing a 1_B to this bit removes the CC42 from IDLE mode. A read access always returns 0.
CS3I	3	w	**CC43 IDLE mode clear** Writing a 1_B to this bit removes the CC43 from IDLE mode. A read access always returns 0.
SPRB	8	w	**Prescaler Run Bit Set** Writing a 1_B into this register sets the Run Bit of the prescaler. A read always returns 0.
0	7:4, 31:9	r	**Reserved** Read always returns 0.

20.7.1.5 Register GCSS

Through this register one can request a shadow transfer for the specific timer slice(s) and set the status bit for each of the compare channels.

GCSS Address: 0010_H

Global Channel Set Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0												S3STS	S2STS	S1STS	S0STS
r												w	w	w	w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	S3PSE	S3DSE	S3SE	0	S2PSE	S2DSE	S2SE	0	S1PSE	S1DSE	S1SE	0	S0PSE	S0DSE	S0SE
r	w	w	w	r	w	w	w	r	w	w	w	r	w	w	w

Field	Bits	Type	Description
S0SE	0	w	**Slice 0 shadow transfer set enable** Writing a 1_B to this bit will set the ***GCST***.S0SS field, enabling then a shadow transfer for the Period, Compare and Passive level values. A read always returns 0.
S0DSE	1	w	**Slice 0 Dither shadow transfer set enable** Writing a 1_B to this bit will set the ***GCST***.S0DSS field, enabling then a shadow transfer for the Dither compare value. A read always returns 0.
S0PSE	2	w	**Slice 0 Prescaler shadow transfer set enable** Writing a 1_B to this bit will set the ***GCST***.S0PSS field, enabling then a shadow transfer for the prescaler compare value. A read always returns 0.
S1SE	4	w	**Slice 1 shadow transfer set enable** Writing a 1_B to this bit will set the ***GCST***.S1SS field, enabling then a shadow transfer for the Period, Compare and Passive level values. A read always returns 0.
S1DSE	5	w	**Slice 1 Dither shadow transfer set enable** Writing a 1_B to this bit will set the ***GCST***.S1DSS field, enabling then a shadow transfer for the Dither compare value. A read always returns 0.
S1PSE	6	w	**Slice 1 Prescaler shadow transfer set enable** Writing a 1_B to this bit will set the ***GCST***.S1PSS field, enabling then a shadow transfer for the prescaler compare value. A read always returns 0.
S2SE	8	w	**Slice 2 shadow transfer set enable** Writing a 1_B to this bit will set the ***GCST***.S2SS field, enabling then a shadow transfer for the Period, Compare and Passive level values. A read always returns 0.
S2DSE	9	w	**Slice 2 Dither shadow transfer set enable** Writing a 1_B to this bit will set the ***GCST***.S2DSS field, enabling then a shadow transfer for the Dither compare value. A read always returns 0.

(continued)

Field	Bits	Type	Description
S2PSE	10	w	**Slice 2 Prescaler shadow transfer set enable** Writing a 1_B to this bit will set the ***GCST***.S2PSS field, enabling then a shadow transfer for the prescaler compare value. A read always returns 0.
S3SE	12	w	**Slice 3 shadow transfer set enable** Writing a 1_B to this bit will set the ***GCST***.S3SS field, enabling then a shadow transfer for the Period, Compare and Passive level values. A read always returns 0.
S3DSE	13	w	**Slice 3 Dither shadow transfer set enable** Writing a 1_B to this bit will set the ***GCST***.S3DSS field, enabling then a shadow transfer for the Dither compare value. A read always returns 0.
S3PSE	14	w	**Slice 3 Prescaler shadow transfer set enable** Writing a 1_B to this bit will set the ***GCST***.S3PSS field, enabling then a shadow transfer for the prescaler compare value. A read always returns 0.
S0STS	16	w	**Slice 0 status bit set** Writing a 1_B into this field sets the status bit of slice 0 (***GCST***.CC40ST) to 1_B. A read always returns 0.
S1STS	17	w	**Slice 1 status bit set** Writing a 1_B into this field sets the status bit of slice 1 (***GCST***.CC41ST) to 1_B. A read always returns 0.
S2STS	18	w	**Slice 2 status bit set** Writing a 1_B into this field sets the status bit of slice 2 (***GCST***.CC42ST) to 1_B. A read always returns 0.
S3STS	19	w	**Slice 3 status bit set** Writing a 1_B into this field sets the status bit of slice 3 (***GCST***.CC43ST) to 1_B. A read always returns 0.
0	3, 7, 11, 15, 31:20	r	**Reserved** Read always returns 0.

20.7.1.6 Register GCSC

Through this register one can reset a shadow transfer request for the specific timer slice and clear the status bit for each the compare channels.

GCSC Address: 0014_H

Global Channel Clear Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0												S3STC	S2STC	S1STC	S0STC
r												w	w	w	w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	S3PSC	S3DSC	S3SC	0	S2PSC	S2DSC	S2SC	0	S1PSC	S1DSC	S1SC	0	S0PSC	S0DSC	S0SC
r	w	w	w	r	w	w	w	r	w	w	w	r	w	w	w

Field	Bits	Type	Description
S0SC	0	w	**Slice 0 shadow transfer clear** Writing a 1_B to this bit will clear the ***GCST***.S0SS field, canceling any pending shadow transfer for the Period, Compare and Passive level values. A read always returns 0.
S0DSC	1	w	**Slice 0 Dither shadow transfer clear** Writing a 1_B to this bit will clear the ***GCST***.S0DSS field, canceling any pending shadow transfer for the Dither compare value. A read always returns 0.
S0PSC	2	w	**Slice 0 Prescaler shadow transfer clear** Writing a 1_B to this bit will clear the ***GCST***.S0PSS field, canceling any pending shadow transfer for the prescaler compare value. A read always returns 0.
S1SC	4	w	**Slice 1 shadow transfer clear** Writing a 1_B to this bit will clear the ***GCST***.S1SS field, canceling any pending shadow transfer for the Period, Compare and Passive level values. A read always returns 0.
S1DSC	5	w	**Slice 1 Dither shadow transfer clear** Writing a 1_B to this bit will clear the ***GCST***.S1DSS field, canceling any pending shadow transfer for the Dither compare value. A read always returns 0.
S1PSC	6	w	**Slice 1 Prescaler shadow transfer clear** Writing a 1_B to this bit will clear the ***GCST***.S1PSS field, canceling any pending shadow transfer for the prescaler compare value. A read always returns 0.
S2SC	8	w	**Slice 2 shadow transfer clear** Writing a 1_B to this bit will clear the ***GCST***.S2SS field, canceling any pending shadow transfer for the Period, Compare and Passive level values. A read always returns 0.
S2DSC	9	w	**Slice 2 Dither shadow transfer clear** Writing a 1_B to this bit will clear the ***GCST***.S2DSS field, canceling any pending shadow transfer for the Dither compare value. A read always returns 0.

(continued)

Field	Bits	Type	Description
S2PSC	10	w	**Slice 2 Prescaler shadow transfer clear** Writing a 1_B to this bit will clear the ***GCST***.S2PSS field, canceling any pending shadow transfer for the prescaler compare value. A read always returns 0.
S3SC	12	w	**Slice 3 shadow transfer clear** Writing a 1_B to this bit will clear the ***GCST***.S3SS field, canceling any pending shadow transfer for the Period, Compare and Passive level values. A read always returns 0.
S3DSC	13	w	**Slice 3 Dither shadow transfer clear** Writing a 1_B to this bit will clear the ***GCST***.S3DSS field, canceling any pending shadow transfer for the Dither compare value. A read always returns 0.
S3PSC	14	w	**Slice 3 Prescaler shadow transfer clear** Writing a 1_B to this bit will clear the ***GCST***.S3PSS field, canceling any pending shadow transfer for the prescaler compare value. A read always returns 0.
S0STC	16	w	**Slice 0 status bit clear** Writing a 1_B into this field clears the status bit of slice 0 (***GCST***.CC40ST) to 0_B. A read always returns 0.
S1STC	17	w	**Slice 1 status bit clear** Writing a 1_B into this field clears the status bit of slice 1 (***GCST***.CC41ST) to 0_B. A read always returns 0.
S2STC	18	w	**Slice 2 status bit clear** Writing a 1_B into this field clears the status bit of slice 2 (***GCST***.CC42ST) to 0_B. A read always returns 0.
S3STC	19	w	**Slice 3 status bit clear** Writing a 1_B into this field clears the status bit of slice 3 (***GCST***.CC43ST) to 0_B. A read always returns 0.
0	3, 7, 11, 15, 31:20	r	**Reserved** Read always returns 0.

20.7.1.7 Register GCST

This register holds the information of the shadow transfer requests and of each timer slice status bit.

GCST Address: 0018_H

Global Channel Status Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0												CC43ST	CC42ST	CC41ST	CC40ST
r												rh	rh	rh	rh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	S3PSS	S3DSS	S3SS	0	S2PSS	S2DSS	S2SS	0	S1PSS	S1DSS	S1SS	0	S0PSS	S0DSS	S0SS
r	rh	rh	rh	r	rh	rh	rh	r	rh	rh	rh	r	rh	rh	rh

Field	Bits	Type	Description
S0SS	0	rh	**Slice 0 shadow transfer status** 0_B Shadow transfer has not been requested 1_B Shadow transfer has been requested This field is cleared by HW after the requested shadow transfer has been executed.
S0DSS	1	rh	**Slice 0 Dither shadow transfer status** 0_B Dither shadow transfer has not been requested 1_B Dither shadow transfer has been requested This field is cleared by HW after the requested shadow transfer has been executed.
S0PSS	2	rh	**Slice 0 Prescaler shadow transfer status** 0_B Prescaler shadow transfer has not been requested 1_B Prescaler shadow transfer has been requested This field is cleared by HW after the requested shadow transfer has been executed.
S1SS	4	rh	**Slice 1 shadow transfer status** 0_B Shadow transfer has not been requested 1_B Shadow transfer has been requested This field is cleared by HW after the requested shadow transfer has been executed.
S1DSS	5	rh	**Slice 1 Dither shadow transfer status** 0_B Dither shadow transfer has not been requested 1_B Dither shadow transfer has been requested This field is cleared by HW after the requested shadow transfer has been executed.
S1PSS	6	rh	**Slice 1 Prescaler shadow transfer status** 0_B Prescaler shadow transfer has not been requested 1_B Prescaler shadow transfer has been requested This field is cleared by HW after the requested shadow transfer has been executed.

(continued)

Field	Bits	Type	Description
S2SS	8	rh	**Slice 2 shadow transfer status** 0_B Shadow transfer has not been requested 1_B Shadow transfer has been requested This field is cleared by HW after the requested shadow transfer has been executed.
S2DSS	9	rh	**Slice 2 Dither shadow transfer status** 0_B Dither shadow transfer has not been requested 1_B Dither shadow transfer has been requested This field is cleared by HW after the requested shadow transfer has been executed.
S2PSS	10	rh	**Slice 2 Prescaler shadow transfer status** 0_B Prescaler shadow transfer has not been requested 1_B Prescaler shadow transfer has been requested This field is cleared by HW after the requested shadow transfer has been executed.
S3SS	12	rh	**Slice 3 shadow transfer status** 0_B Shadow transfer has not been requested 1_B Shadow transfer has been requested This field is cleared by HW after the requested shadow transfer has been executed.
S3DSS	13	rh	**Slice 3 Dither shadow transfer status** 0_B Dither shadow transfer has not been requested 1_B Dither shadow transfer has been requested This field is cleared by HW after the requested shadow transfer has been executed.
S3PSS	14	rh	**Slice 3 Prescaler shadow transfer status** 0_B Prescaler shadow transfer has not been requested 1_B Prescaler shadow transfer has been requested This field is cleared by HW after the requested shadow transfer has been executed.
CC40ST	16	rh	**Slice 0 status bit**
CC41ST	17	rh	**Slice 1 status bit**
CC42ST	18	rh	**Slice 2 status bit**
CC43ST	19	rh	**Slice 3 status bit**
0	3, 7, 11, 15, 31:20	r	**Reserved** Read always returns 0.

20.7.1.8 Register MIDR

This register contains the module identification number.

MIDR Address: 0080_H

Module Identification Reset Value: $00B6C0XX_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MODN															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MODT								MODR							
r								r							

Field	Bits	Type	Description
MODR	7:0	r	**Module Revision** This bit field indicates the revision number of the module implementation (depending on the design step). The given value of 00_H is a placeholder for the actual number.
MODT	15:8	r	**Module Type**
MODN	31:16	r	**Module Number**

20.7.2 Slice (CC4y) Registers

20.7.2.1 Register CC4yINS1

This register configures which signals pins are used for the input selector.

CC4yINS1 (y=0-3) Address: $01D8_H + 0100_H * y$

Input Selector Configuration 1 Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0										EV2IS					
r										rw					

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		EV1IS						0		EV0IS					
r		rw						r		rw					

Field	Bits	Type	Description
EV0IS	5:0	rw	**Event 0 signal selection** This field selects which pins is used for the event 0. 000000_B CCU4x.INyAA 000001_B CCU4x.INyAB 000010_B CCU4x.INyAC 000011_B CCU4x.INyAD ... 011001_B CCU4x.INyAZ 011010_B CCU4x.INyBA 011011_B CCU4x.INyBB ... 101111_B CCU4x.INyBV $11XXXX_B$ Reserved (behaves as connected to 0)
EV1IS	13:8	rw	**Event 1 signal selection** Same as EV0IS description
EV2IS	21:16	rw	**Event 2 signal selection** Same as EV0IS description
0	7:6, 15:14, 31:22	r	**Reserved** Read always returns 0.

20.7.2.2 Register CC4yINS2

This register contains the configuration for the edge and level behavior of the input selector signals.

CC4yINS2 (y=0-3) Address: $0100_H + 0100_H * y$

Input Selector Configuration 2 Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0						LPF2M		0		LPF1M		0		LPF0M	
r						rw		r		rw		r		rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0					EV2LM	EV2EM		0	EV1LM	EV1EM		0	EV0LM	EV0EM	
r					rw	rw		r	rw	rw		r	rw	rw	

Field	Bits	Type	Description
EV0EM	1:0	rw	**Event 0 Edge Selection** 00_B No action 01_B Signal active on rising edge 10_B Signal active on falling edge 11_B Signal active on both edges

(continued)

Field	Bits	Type	Description
EV0LM	2	rw	**Event 0 Level Selection** 0_B Active on HIGH level 1_B Active on LOW level
EV1EM	5:4	rw	**Event 1 Edge Selection** Same as EV0EM description
EV1LM	6	rw	**Event 1 Level Selection** Same as EV0LM description
EV2EM	9:8	rw	**Event 2 Edge Selection** Same as EV0EM description
EV2LM	10	rw	**Event 2 Level Selection** Same as EV0LM description
LPF0M	17:16	rw	**Event 0 Low Pass Filter Configuration** This field sets the number of consecutive counts for the Low Pass Filter of Event 0. The input signal value needs to remain stable for this number of counts (f_{CCU4}), so that a level/transition is accepted. 00_B LPF is disabled 01_B 3 clock cycles of f_{CCU4} 10_B 5 clock cycles of f_{CCU4} 11_B 7 clock cycles of f_{CCU4}
LPF1M	21:20	rw	**Event 1 Low Pass Filter Configuration** Same description as LPF0M
LPF2M	25:24	rw	**Event 2 Low Pass Filter Configuration** Same description as LPF0M
0	3, 7, 15:11, 19:18, 23:22, 31:26	r	**Reserved** Read always returns 0.

20.7.2.3 Register CC4yCMC

The register contains the configuration for the connection matrix.

CC4yCMC (y=0-3) Address: $0104_H + 0100_H * y$

Connection Matrix Control Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0											TCE	MOS		TS	OFS
r											rw	rw		rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNTS		LDS		UDS		GATES		CAP1S		CAP0S		ENDS		STRTS	
rw		rw		rw		rw		rw		rw		rw		rw	

Field	Bits	Type	Description
STRTS	1:0	rw	**External Start Functionality Selector** Selects the Event that is going to be linked with the external start functionality. 00_B External Start Function deactivated 01_B External Start Function triggered by Event 0 10_B External Start Function triggered by Event 1 11_B External Start Function triggered by Event 2
ENDS	3:2	rw	**External Stop Functionality Selector** Selects the Event that is going to be linked with the external stop functionality. 00_B External Stop Function deactivated 01_B External Stop Function triggered by Event 0 10_B External Stop Function triggered by Event 1 11_B External Stop Function triggered by Event 2
CAP0S	5:4	rw	**External Capture 0 Functionality Selector** Selects the Event that is going to be linked with the external capture for capture registers number 1 and 0. 00_B External Capture 0 Function deactivated 01_B External Capture 0 Function triggered by Event 0 10_B External Capture 0 Function triggered by Event 1 11_B External Capture 0 Function triggered by Event 2
CAP1S	7:6	rw	**External Capture 1 Functionality Selector** Selects the Event that is going to be linked with the external capture for capture registers number 3 and 2. 00_B External Capture 1 Function deactivated 01_B External Capture 1 Function triggered by Event 0 10_B External Capture 1 Function triggered by Event 1 11_B External Capture 1 Function triggered by Event 2
GATES	9:8	rw	**External Gate Functionality Selector** Selects the Event that is going to be linked with the counter gating function. This function is used to gate the timer increment/ decrement procedure. 00_B External Gating Function deactivated 01_B External Gating Function triggered by Event 0 10_B External Gating Function triggered by Event 1 11_B External Gating Function triggered by Event 2
UDS	11:10	rw	**External Up/Down Functionality Selector** Selects the Event that is going to be linked with the Up/Down counting direction control. 00_B External Up/Down Function deactivated 01_B External Up/Down Function triggered by Event 0 10_B External Up/Down Function triggered by Event 1 11_B External Up/Down Function triggered by Event 2

(continued)

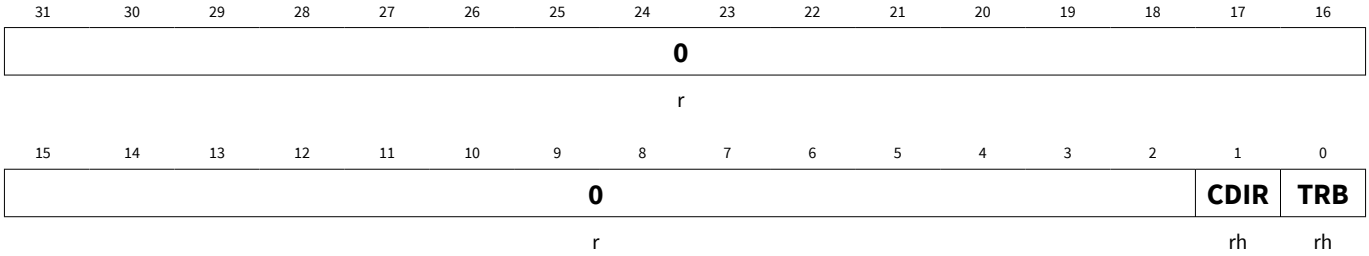
Field	Bits	Type	Description
LDS	13:12	rw	**External Timer Load Functionality Selector** Selects the Event that is going to be linked with the timer load function. 00_B - External Load Function deactivated 01_B - External Load Function triggered by Event 0 10_B - External Load Function triggered by Event 1 11_B - External Load Function triggered by Event 2
CNTS	15:14	rw	**External Count Selector** Selects the Event that is going to be linked with the count function. The counter is going to be increment/decremented each time that a specific transition on the event is detected. 00_B External Count Function deactivated 01_B External Count Function triggered by Event 0 10_B External Count Function triggered by Event 1 11_B External Count Function triggered by Event 2
OFS	16	rw	**Override Function Selector** This field enables the ST bit override functionality. 0_B Override functionality disabled 1_B Status bit trigger override connected to Event 1; Status bit value override connected to Event 2
TS	17	rw	**Trap Function Selector** This field enables the trap functionality. 0_B Trap function disabled 1_B TRAP function connected to Event 2
MOS	19:18	rw	**External Modulation Functionality Selector** Selects the Event that is going to be linked with the external modulation function. 00_B - Modulation Function deactivated 01_B - Modulation Function triggered by Event 0 10_B - Modulation Function triggered by Event 1 11_B - Modulation Function triggered by Event 2
TCE	20	rw	**Timer Concatenation Enable** This bit enables the timer concatenation with the previous slice. 0_B Timer concatenation is disabled 1_B Timer concatenation is enabled *Note: In CC40 this field doesn't exist. This is a read only reserved field. Read access always returns 0.*
0	31:21	r	**Reserved** A read always returns 0

20.7.2.4 Register CC4yTCST

The register holds the status of the timer (running/stopped) and the information about the counting direction (up/down).

CC4yTCST (y=0-3) Address: $0108_H + 0100_H * y$

Slice Timer Status Reset Value: 00000000_H



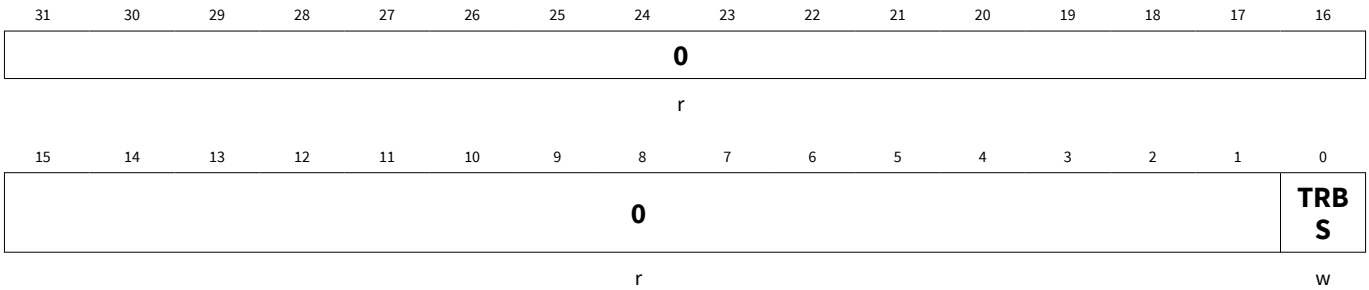
Field	Bits	Type	Description
TRB	0	rh	**Timer Run Bit** This field indicates if the timer is running. 0_B Timer is stopped 1_B Timer is running
CDIR	1	rh	**Timer Counting Direction** This filed indicates if the timer is being increment or decremented 0_B Timer is counting up 1_B Timer is counting down
0	31:2	r	**Reserved** Read always returns 0

20.7.2.5 Register CC4yTCSET

Through this register it is possible to start the timer.

CC4yTCSET (y=0-3) Address: $010C_H + 0100_H * y$

Slice Timer Run Set Reset Value: 00000000_H



Field	Bits	Type	Description
TRBS	0	w	**Timer Run Bit set** Writing a 1_B into this field sets the run bit of the timer. Read always returns 0.
0	31:1	r	**Reserved** Read always returns 0

20.7.2.6 Register CC4yTCCLR

Through this register it is possible to stop and clear the timer, and clearing also the dither counter.

CC4yTCCLR (y=0-3) Address: $0110_H + 0100_H * y$

Slice Timer Clear Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0													DITC	TCC	TRBC
r													w	w	w

Field	Bits	Type	Description
TRBC	0	w	**Timer Run Bit Clear** Writing a 1_B into this field clears the run bit of the timer. The timer is not cleared. Read always returns 0.
TCC	1	w	**Timer Clear** Writing a 1_B into this field clears the timer to 0000_H. Read always returns 0.
DITC	2	w	**Dither Counter Clear** Writing a 1_B into this field clears the dither counter to 0_H. Read always returns 0.
0	31:3	r	**Reserved** Read always returns 0

20.7.2.7 Register CC4yTC

This register holds the several possible configurations for the timer operation.

CC4yTC (y=0-3) Address: $0114_H + 0100_H * y$

Slice Timer Control Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0						MCME	EMT	EMS	TRPSW	TRPSE	0			TRAPE	FPE
r						rw	rw	rw	rw	rw	r			rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIM	DITHE		CCS	SCE	STRM	ENDM		0	CAPC		ECM	CMOD	CLST	TSSM	TCM
rw	rw		rw	rw	rw	rw		r	rw		rw	rh	rw	rw	rw

Field	Bits	Type	Description
TCM	0	rw	**Timer Counting Mode** This field controls the actual counting scheme of the timer. 0_B Edge aligned mode 1_B Center aligned mode *Note: When using an external signal to control the counting direction, the counting scheme is always edge aligned.*
TSSM	1	rw	**Timer Single Shot Mode** This field controls the single shot mode. This is applicable in edge and center aligned modes. 0_B Single shot mode is disabled 1_B Single shot mode is enabled
CLST	2	rw	**Shadow Transfer on Clear** Setting this bit to 1_B enables a shadow transfer when a timer clearing action is performed. Notice that the shadow transfer enable bitfields on the ***GCST*** register still need to be set to 1_B via software.
CMOD	3	rh	**Capture Compare Mode** This field indicates in which mode the slice is operating. The default value is compare mode. The capture mode is automatically set by the HW when an external signal is mapped to a capture trigger. 0_B Compare Mode 1_B Capture Mode
ECM	4	rw	**Extended Capture Mode** This field control the Capture mode of the specific slice. It only has effect if the CMOD bit is 1_B. 0_B Normal Capture Mode. Clear of the Full Flag of each capture register is done by accessing the registers individually only. 1_B Extended Capture Mode. Clear of the Full Flag of each capture register is done not only by accessing the individual registers but also by accessing the ECRD register. When reading the ECRD register, only the capture register register full flag pointed by the ECRD.VPTR is cleared.

(continued)

Field	Bits	Type	Description
CAPC	6:5	rw	**Clear on Capture Control** 00_B Timer is never cleared on a capture event 01_B Timer is cleared on a capture event into capture registers 2 and 3. (When SCE = 1_B, Timer is always cleared in a capture event) 10_B Timer is cleared on a capture event into capture registers 0 and 1. (When SCE = 1_B, Timer is always cleared in a capture event) 11_B Timer is always cleared in a capture event.
ENDM	9:8	rw	**Extended Stop Function Control** This field controls the extended functions of the external Stop signal. 00_B Clears the timer run bit only (default stop) 01_B Clears the timer only (flush) 10_B Clears the timer and run bit (flush/stop) 11_B Reserved *Note: When using an external up/down signal the flush operation sets the timer with zero if the counter is counting up and with the Period value if the counter is being decremented.*
STRM	10	rw	**Extended Start Function Control** This field controls the extended functions of the external Start signal. 0_B Sets run bit only (default start) 1_B Clears the timer and sets run bit (flush/start) *Note: When using an external up/down signal the flush operation sets the timer with zero if the counter is being incremented and with the Period value if the counter is being decremented.*
SCE	11	rw	**Equal Capture Event enable** 0_B Capture into ***CC4yC0V***/***CC4yC1V*** registers control by CCycapt0 and capture into ***CC4yC3V***/***CC4yC2V*** control by CCycapt1 1_B Capture into ***CC4yC0V***/***CC4yC1V*** and ***CC4yC3V***/***CC4yC2V*** control by CCycapt1
CCS	12	rw	**Continuous Capture Enable** 0_B The capture into a specific capture register is done with the rules linked with the full flags, described at ***Chapter 20.2.5.6***. 1_B The capture into the capture registers is always done regardless of the full flag status (even if the register has not been read back).

(continued)

Field	Bits	Type	Description
DITHE	14:13	rw	**Dither Enable** This field controls the dither mode for the slice. See ***Chapter 20.2.6.3***. 00_B Dither is disabled 01_B Dither is applied to the Period 10_B Dither is applied to the Compare 11_B Dither is applied to the Period and Compare
DIM	15	rw	**Dither input selector** This fields selects if the dither control signal is connected to the dither logic of the specific slice of is connected to the dither logic of slice 0. Notice that even if this field is set to 1_B, the field DITHE still needs to be programmed. 0_B Slice is using its own dither unit 1_B Slice is connected to the dither unit of slice 0.
FPE	16	rw	**Floating Prescaler enable** Setting this bit to 1_B enables the floating prescaler mode. 0_B Floating prescaler mode is disabled 1_B Floating prescaler mode is enabled
TRAPE	17	rw	**TRAP enable** Setting this bit to 1_B enables the TRAP action at the output pin. After mapping an external signal to the TRAP functionality, the user must set this field to 1_B to activate the effect of the TRAP on the output pin. Writing a 0_B into this field disables the effect of the TRAP function regardless of the state of the input signal. 0_B TRAP functionality has no effect on the output 1_B TRAP functionality affects the output
TRPSE	21	rw	**TRAP Synchronization Enable** Writing a 1_B into this bit enables a synchronous exiting with the PWM signal of the trap state. 0_B Exiting from TRAP state isn't synchronized with the PWM signal 1_B Exiting from TRAP state is synchronized with the PWM signal
TRPSW	22	rw	**TRAP State Clear Control** 0_B The slice exits the TRAP state automatically when the TRAP condition is not present 1_B The TRAP state can only be exited by a SW request.
EMS	23	rw	**External Modulation Synchronization** Setting this bit to 1_B enables the synchronization of the external modulation functionality with the PWM period. 0_B External Modulation functionality is not synchronized with the PWM signal 1_B External Modulation functionality is synchronized with the PWM signal

(continued)

Field	Bits	Type	Description
EMT	24	rw	**External Modulation Type** This field selects if the external modulation event is clearing the CC4yST bit or if is gating the outputs. 0_B External Modulation functionality is clearing the CC4yST bit. 1_B External Modulation functionality is gating the outputs.
MCME	25	rw	**Multi-Channel Mode Enable** 0_B Multi-Channel Mode is disabled 1_B Multi-Channel Mode is enabled
0	7, 20:18, 31:26	r	**Reserved** Read always returns 0

20.7.2.8 Register CC4yPSL

This register holds the configuration for the output passive level control.

CC4yPSL (y=0-3) Address: $0118_H + 0100_H * y$

Passive Level Config Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0															PSL
r															rw

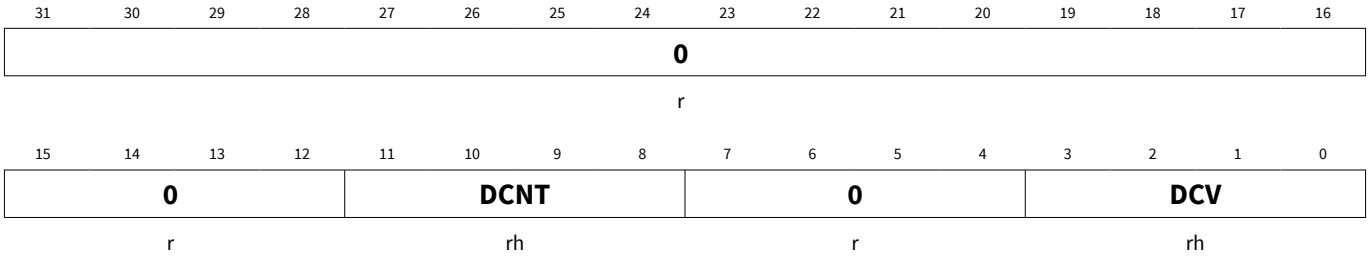
Field	Bits	Type	Description
PSL	0	rw	**Output Passive Level** This field controls the passive level of the output pin. 0_B Passive Level is LOW 1_B Passive Level is HIGH A write always addresses the shadow register, while a read always returns the current used value.
0	31:1	r	**Reserved** A read access always returns 0

20.7.2.9 Register CC4yDIT

This register holds the current dither compare and dither counter values.

CC4yDIT (y=0-3) Address: $011C_H + 0100_H * y$

Dither Config Reset Value: 00000000_H



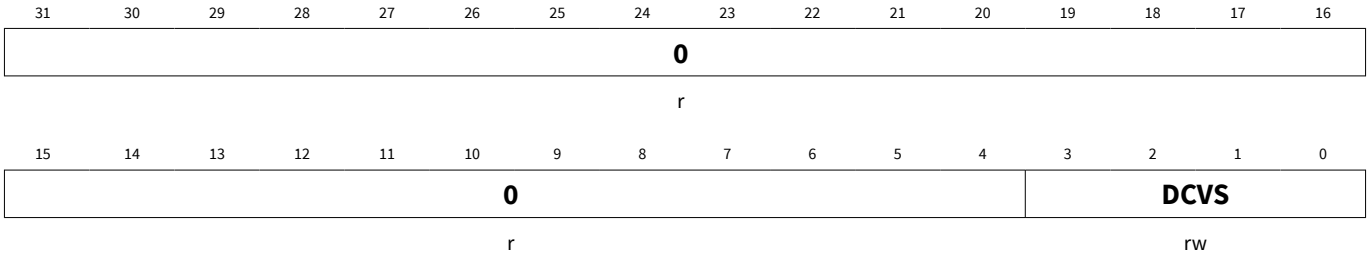
Field	Bits	Type	Description
DCV	3:0	rh	**Dither compare Value** This field contains the value used for the dither comparison. This value is updated when a shadow transfer occurs with the ***CC4yDITS***.DCVS.
DCNT	11:8	rh	**Dither counter actual value**
0	7:4, 31:12	r	**Reserved** Read always returns 0.

20.7.2.10 Register CC4yDITS

This register contains the value that is going to be loaded into the ***CC4yDIT***.DCV when the next shadow transfer occurs.

CC4yDITS (y=0-3) Address: $0120_H + 0100_H * y$

Dither Shadow Register Reset Value: 00000000_H



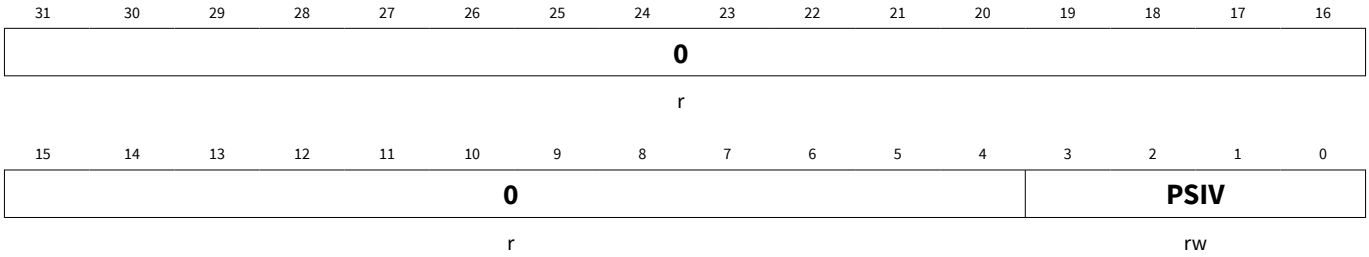
Field	Bits	Type	Description
DCVS	3:0	rw	**Dither Shadow Compare Value** This field contains the value that is going to be set on the dither compare value, ***CC4yDIT***.DCV, within the next shadow transfer.
0	31:4	r	**Reserved** Read always returns 0.

20.7.2.11 Register CC4yPSC

This register contains the value that is loaded into the prescaler during restart.

CC4yPSC (y=0-3) Address: $0124_H + 0100_H * y$

Prescaler Control Reset Value: 00000000_H



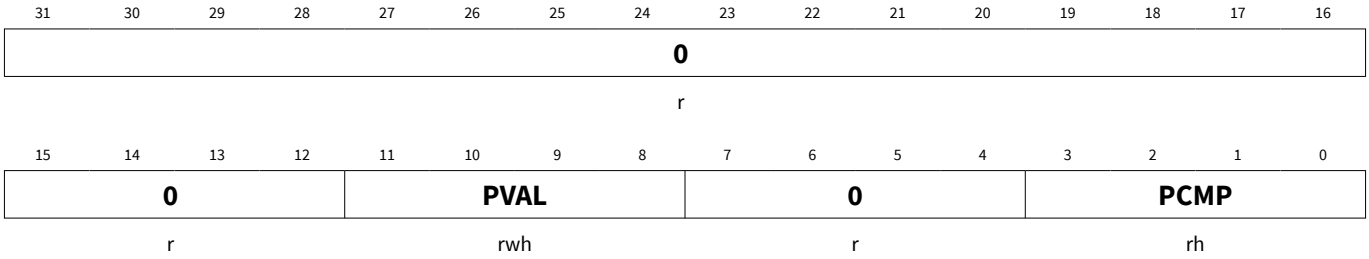
Field	Bits	Type	Description
PSIV	3:0	rw	**Prescaler Initial Value** This field contains the value that is applied to the Prescaler at startup. When floating prescaler mode is used, this value is applied when a timer compare match AND prescaler compare match occurs or when a capture event is triggered.
0	31:4	r	**Reserved** Read always returns 0.

20.7.2.12 Register CC4yFPC

This register contains the value used for the floating prescaler compare and the actual prescaler division value.

CC4yFPC (y=0-3) Address: $0128_H + 0100_H * y$

Floating Prescaler Control Reset Value: 00000000_H



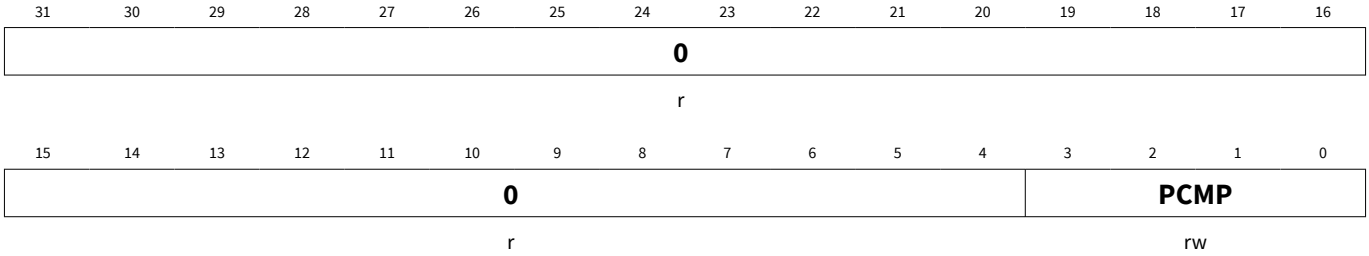
Field	Bits	Type	Description
PCMP	3:0	rh	**Floating Prescaler Compare Value** This field contains comparison value used in floating prescaler mode. The comparison is triggered by the Timer Compare match event. See ***Chapter 20.2.7.2***.
PVAL	11:8	rwh	**Actual Prescaler Value** See ***Table 250***. Writing into this register is only possible when the prescaler is stopped. When the floating prescaler mode is not used, this value is equal to the ***CC4yPSC***.PSIV.
0	7:4, 15:12, 31:16	r	**Reserved** Read always returns 0.

20.7.2.13 Register CC4yFPCS

This register contains the value that is going to be transferred to the ***CC4yFPC***. PCMP field within the next shadow transfer update.

CC4yFPCS (y=0-3) Address: $012C_H + 0100_H * y$

Floating Prescaler Shadow Reset Value: 00000000_H



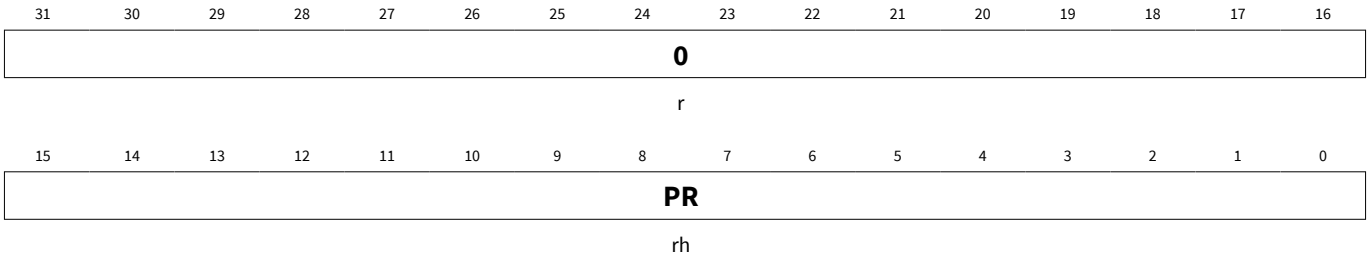
Field	Bits	Type	Description
PCMP	3:0	rw	**Floating Prescaler Shadow Compare Value** This field contains the value that is going to be set on the ***CC4yFPC***.PCMP within the next shadow transfer. See ***Table 250*** .
0	31:4	r	**Reserved** Read always returns 0.

20.7.2.14 Register CC4yPR

This register contains the actual value for the timer period.

CC4yPR (y=0-3) Address: $0130_H + 0100_H * y$

Timer Period Value Reset Value: 00000000_H



Field	Bits	Type	Description
PR	15:0	rh	**Period Register** Contains the value of the timer period. *Note: In Capture Mode when a external signal is selected for capturing the timer value into the capture registers 2 and 3, PR is not accessible for writing. A read always returns 0.*

(continued)

Field	Bits	Type	Description
0	31:16	r	**Reserved** A read always returns 0.

20.7.2.15 Register CC4yPRS

This register contains the value for the timer period that is going to be transferred into the ***CC4yPR***.PR field when the next shadow transfer occurs.

CC4yPRS (y=0-3) Address: $0134_H + 0100_H * y$

Timer Shadow Period Value Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRS															
rw															

Field	Bits	Type	Description
PRS	15:0	rw	**Period Register** Contains the value of the timer period, that is going to be passed into the ***CC4yPR***.PR field when the next shadow transfer occurs. *Note: In Capture Mode when a external signal is selected for capturing the timer value into the capture registers 2 and 3, the PRS is not accessible for writing. A read always returns 0.*
0	31:16	r	**Reserved** A read always returns 0.

20.7.2.16 Register CC4yCR

This register contains the value for the timer comparison.

CC4yCR (y=0-3) Address: $0138_H + 0100_H * y$

Timer Compare Value Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CR															
rh															

Field	Bits	Type	Description
CR	15:0	rh	**Compare Register** Contains the value for the timer comparison. *Note: In Capture Mode when a external signal is selected for capturing the timer value into the capture registers 0 and 1, a read always returns 0.*
0	31:16	r	**Reserved** A read always returns 0.

20.7.2.17 Register CC4yCRS

This register contains the value that is going to be loaded into the ***CC4yCR***. CR field when the next shadow transfer occurs.

CC4yCRS (y=0-3) Address: $013C_H + 0100_H * y$

Timer Shadow Compare Value Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRS															
rw															

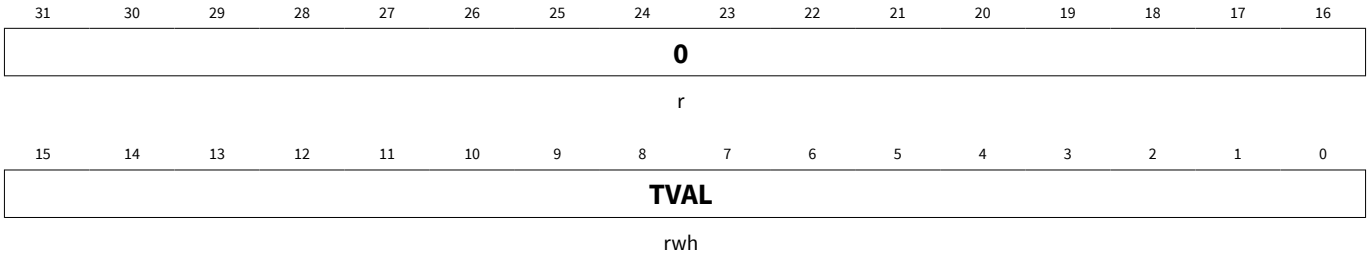
Field	Bits	Type	Description
CRS	15:0	rw	**Compare Register** Contains the value for the timer comparison, that is going to be passed into the ***CC4yCR***.CR field when the next shadow transfer occurs. *Note: In Capture Mode when a external signal is selected for capturing the timer value into the capture registers 0 and 1, a read always returns 0.*
0	31:16	r	**Reserved** A read always returns 0.

20.7.2.18 Register CC4yTIMER

This register contains the current value of the timer.

CC4yTIMER (y=0-3) Address: $0170_H + 0100_H * y$

Timer Value Reset Value: 00000000_H



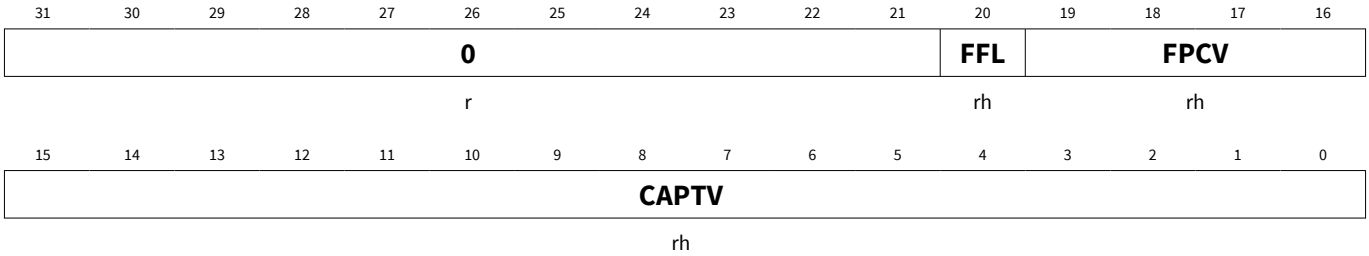
Field	Bits	Type	Description
TVAL	15:0	rwh	**Timer Value** This field contains the actual value of the timer. A write access is only possible when the timer is stopped.
0	31:16	r	**Reserved** A read access always returns 0

20.7.2.19 Register CC4yC0V

This register contains the values associated with the Capture 0 field.

CC4yC0V (y=0-3) Address: $0174_H + 0100_H * y$

Capture Register 0 Reset Value: 00000000_H



Field	Bits	Type	Description
CAPTV	15:0	rh	**Capture Value** This field contains the capture register 0 value. See ***Figure 186***. In compare mode a read access always returns 0.
FPCV	19:16	rh	**Prescaler Value** This field contains the prescaler value at the time of the capture event into the capture register 0. In compare mode a read access always returns 0.
FFL	20	rh	**Full Flag** This bit indicates if a new value was capture into the capture register 0 after the last read access. See ***Figure 186***. In compare mode a read access always returns 0. 0_B No new value was captured into the specific capture register 1_B A new value was captured into the specific register

(continued)

Field	Bits	Type	Description
0	31:21	r	**Reserved** A read always returns 0

20.7.2.20 Register CC4yC1V

This register contains the values associated with the Capture 1 field.

CC4yC1V (y=0-3) Address: $0178_H + 0100_H * y$

Capture Register 1 Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0											FFL	FPCV			
r											rh	rh			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPTV															
rh															

Field	Bits	Type	Description
CAPTV	15:0	rh	**Capture Value** This field contains the capture register 1 value. See ***Figure 186***. In compare mode a read access always returns 0.
FPCV	19:16	rh	**Prescaler Value** This field contains the prescaler value at the time of the capture event into the capture register 1. In compare mode a read access always returns 0.
FFL	20	rh	**Full Flag** This bit indicates if a new value was capture into the capture register 1 after the last read access. See ***Figure 186***. In compare mode a read access always returns 0. 0_B No new value was captured into the specific capture register 1_B A new value was captured into the specific register
0	31:21	r	**Reserved** A read always returns 0

20.7.2.21 Register CC4yC2V

This register contains the values associated with the Capture 2 field.

CC4yC2V (y=0-3) Address: $017C_H + 0100_H * y$

Capture Register 2 Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0											FFL	FPCV			
r											rh	rh			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPTV															
rh															

Field	Bits	Type	Description
CAPTV	15:0	rh	**Capture Value** This field contains the capture register 2 value. See ***Figure 188***. In compare mode a read access always returns 0.
FPCV	19:16	rh	**Prescaler Value** This field contains the prescaler value at the time of the capture event into the capture register 2. In compare mode a read access always returns 0.
FFL	20	rh	**Full Flag** This bit indicates if a new value was capture into the capture register 2 after the last read access. See ***Figure 188***. In compare mode a read access always returns 0. 0_B No new value was captured into the specific capture register 1_B A new value was captured into the specific register
0	31:21	r	**Reserved** A read always returns 0

20.7.2.22 Register CC4yC3V

This register contains the values associated with the Capture 3 field.

CC4yC3V (y=0-3) Address: $0180_H + 0100_H * y$

Capture Register 3 Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0											FFL	FPCV			
r											rh	rh			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPTV															
rh															

Field	Bits	Type	Description
CAPTV	15:0	rh	**Capture Value** This field contains the capture register 3 value. See ***Figure 188***. In compare mode a read access always returns 0.

(continued)

Field	Bits	Type	Description
FPCV	19:16	rh	**Prescaler Value** This field contains the prescaler value at the time of the capture event into the capture register 3. In compare mode a read access always returns 0.
FFL	20	rh	**Full Flag** This bit indicates if a new value was capture into the capture register 3 after the last read access. See ***Figure 188***. In compare mode a read access always returns 0. 0_B No new value was captured into the specific capture register 1_B A new value was captured into the specific register
0	31:21	r	**Reserved** A read always returns 0

20.7.2.23 Register CC4yINTS

This register contains the status of all interrupt sources.

CC4yINTS (y=0-3) Address: $01A0_H + 0100_H * y$

Interrupt Status Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				**TRPF**	**E2AS**	**E1AS**	**E0AS**	**0**				**CMDS**	**CMUS**	**OMDS**	**PMUS**
r				rh	rh	rh	rh	r				rh	rh	rh	rh

Field	Bits	Type	Description
PMUS	0	rh	**Period Match while Counting Up** 0_B Period match while counting up not detected 1_B Period match while counting up detected
OMDS	1	rh	**One Match while Counting Down** 0_B One match while counting down not detected 1_B One match while counting down detected
CMUS	2	rh	**Compare Match while Counting Up** 0_B Compare match while counting up not detected 1_B Compare match while counting up detected
CMDS	3	rh	**Compare Match while Counting Down** 0_B Compare match while counting down not detected 1_B Compare match while counting down detected

(continued)

Field	Bits	Type	Description
E0AS	8	rh	**Event 0 Detection Status** Depending on the user selection on the ***CC4yINS2***.EV0EM, this bit can be set when a rising, falling or both transitions are detected. 0_B Event 0 not detected 1_B Event 0 detected
E1AS	9	rh	**Event 1 Detection Status** Depending on the user selection on the ***CC4yINS2***.EV1EM, this bit can be set when a rising, falling or both transitions are detected. 0_B Event 1 not detected 1_B Event 1 detected
E2AS	10	rh	**Event 2 Detection Status** Depending on the user selection on the ***CC4yINS2***.EV1EM, this bit can be set when a rising, falling or both transitions are detected. 0_B Event 2 not detected 1_B Event 2 detected *Note: If this event is linked with the TRAP function, this field is automatically cleared when the slice exits the Trap State.*
TRPF	11	rh	**Trap Flag Status** This field contains the status of the Trap Flag.
0	7:4, 31:12	r	**Reserved** A read always returns 0.

20.7.2.24 Register CC4yINTE

Through this register it is possible to enable or disable the specific interrupt source(s).

CC4yINTE (y=0-3) Address: $01A4_H + 0100_H * y$

Interrupt Enable Control Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0					**E2AE**	**E1AE**	**E0AE**	**0**				**CMDE**	**CMUE**	**OME**	**PME**
r					rw	rw	rw	r				rw	rw	rw	rw

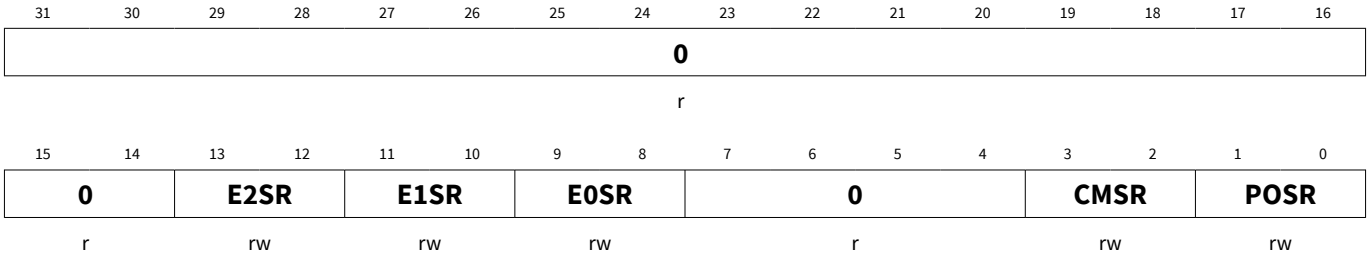
Field	Bits	Type	Description
PME	0	rw	**Period match while counting up enable** Setting this bit to 1_B enables the generation of an interrupt pulse every time a period match while counting up occurs. 0_B Period Match interrupt is disabled 1_B Period Match interrupt is enabled
OME	1	rw	**One match while counting down enable** Setting this bit to 1_B enables the generation of an interrupt pulse every time an one match while counting down occurs. 0_B One Match interrupt is disabled 1_B One Match interrupt is enabled
CMUE	2	rw	**Compare match while counting up enable** Setting this bit to 1_B enables the generation of an interrupt pulse every time a compare match while counting up occurs. 0_B Compare Match while counting up interrupt is disabled 1_B Compare Match while counting up interrupt is enabled
CMDE	3	rw	**Compare match while counting down enable** Setting this bit to 1_B enables the generation of an interrupt pulse every time a compare match while counting down occurs. 0_B Compare Match while counting down interrupt is disabled 1_B Compare Match while counting down interrupt is enabled
E0AE	8	rw	**Event 0 interrupt enable** Setting this bit to 1_B enables the generation of an interrupt pulse every time that Event 0 is detected. 0_B Event 0 detection interrupt is disabled 1_B Event 0 detection interrupt is enabled
E1AE	9	rw	**Event 1 interrupt enable** Setting this bit to 1_B enables the generation of an interrupt pulse every time that Event 1 is detected. 0_B Event 1 detection interrupt is disabled 1_B Event 1 detection interrupt is enabled
E2AE	10	rw	**Event 2 interrupt enable** Setting this bit to 1_B enables the generation of an interrupt pulse every time that Event 2 is detected. 0_B Event 2 detection interrupt is disabled 1_B Event 2 detection interrupt is enabled
0	7:4, 31:11	r	**Reserved** A read always returns 0

20.7.2.25 Register CC4ySRS

Through this register it is possible to select to which service request line each interrupt source is forwarded.

CC4ySRS (y=0-3) Address: $01A8_H + 0100_H * y$

Service Request Selector Reset Value: 00000000_H



Field	Bits	Type	Description
POSR	1:0	rw	**Period/One match Service request selector** This field selects to which slice Service request line, the interrupt(s) generated by the Period match while counting up and One match while counting down are going to be forward. 00_B Forward to CC4ySR0 01_B Forward to CC4ySR1 10_B Forward to CC4ySR2 11_B Forward to CC4ySR3
CMSR	3:2	rw	**Compare match Service request selector** This field selects to which slice Service request line, the interrupt(s) generated by the Compare match while counting up and Compare match while counting down are going to be forward. 00_B Forward to CC4ySR0 01_B Forward to CC4ySR1 10_B Forward to CC4ySR2 11_B Forward to CC4ySR3
E0SR	9:8	rw	**Event 0 Service request selector** This field selects to which slice Service request line, the interrupt generated by the Event 0 detection is going to be forward. 00_B Forward to CC4ySR0 01_B Forward to CC4ySR1 10_B Forward to CC4ySR2 11_B Forward to CC4ySR3
E1SR	11:10	rw	**Event 1 Service request selector** This field selects to which slice Service request line, the interrupt generated by the Event 1 detection is going to be forward. 00_B Forward to CC4ySR0 01_B Forward to CC4ySR1 10_B Forward to CC4ySR2 11_B Forward to CC4ySR3

(continued)

Field	Bits	Type	Description
E2SR	13:12	rw	**Event 2 Service request selector** This field selects to which slice Service request line, the interrupt generated by the Event 2 detection is going to be forward. 00_B Forward to CC4ySR0 01_B Forward to CC4ySR1 10_B Forward to CC4ySR2 11_B Forward to CC4ySR3
0	7:4, 31:14	r	**Reserved** Read always returns 0.

20.7.2.26 Register CC4ySWS

Through this register it is possible for the SW to set a specific interrupt status flag.

CC4ySWS (y=0-3) Address: $01AC_H + 0100_H * y$

Interrupt Status Set Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				STRPF	SE2A	SE1A	SE0A	0				SCMD	SCMU	SOM	SPM
r				w	w	w	w	r				w	w	w	w

Field	Bits	Type	Description
SPM	0	w	**Period match while counting up set** Writing a 1_B into this field sets the ***CC4yINTS***.PMUS bit. An interrupt pulse is generated if the source is enabled. A read always returns 0.
SOM	1	w	**One match while counting down set** Writing a 1_B into this bit sets the ***CC4yINTS***.OMDS bit. An interrupt pulse is generated if the source is enabled. A read always returns 0.
SCMU	2	w	**Compare match while counting up set** Writing a 1_B into this field sets the ***CC4yINTS***.CMUS bit. An interrupt pulse is generated if the source is enabled. A read always returns 0.
SCMD	3	w	**Compare match while counting down set** Writing a 1_B into this bit sets the ***CC4yINTS***.CMDS bit. An interrupt pulse is generated if the source is enabled. A read always returns 0.

(continued)

Field	Bits	Type	Description
SE0A	8	w	**Event 0 detection set** Writing a 1_B into this bit sets the ***CC4yINTS***.E0AS bit. An interrupt pulse is generated if the source is enabled. A read always returns 0.
SE1A	9	w	**Event 1 detection set** Writing a 1_B into this bit sets the ***CC4yINTS***.E1AS bit. An interrupt pulse is generated if the source is enabled. A read always returns 0.
SE2A	10	w	**Event 2 detection set** Writing a 1_B into this bit sets the ***CC4yINTS***.E2AS bit. An interrupt pulse is generated if the source is enabled. A read always returns 0.
STRPF	11	w	**Trap Flag status set** Writing a 1_B into this bit sets the ***CC4yINTS***.TRPF bit. A read always returns 0.
0	7:4, 31:12	r	**Reserved** Read always returns 0

20.7.2.27 Register CC4ySWR

Through this register it is possible for the SW to clear a specific interrupt status flag.

CC4ySWR (y=0-3) Address: $01B0_H + 0100_H * y$

Interrupt Status Clear Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				RTRPF	RE2A	RE1A	RE0A	0				RCMD	RCMU	ROM	RPM
r				w	w	w	w	r				w	w	w	w

Field	Bits	Type	Description
RPM	0	w	**Period match while counting up clear** Writing a 1_B into this field clears the ***CC4yINTS***.PMUS bit. A read always returns 0.
ROM	1	w	**One match while counting down clear** Writing a 1_B into this bit clears the ***CC4yINTS***.OMDS bit. A read always returns 0.
RCMU	2	w	**Compare match while counting up clear** Writing a 1_B into this field clears the ***CC4yINTS***.CMUS bit. A read always returns 0.

(continued)

Field	Bits	Type	Description
RCMD	3	w	**Compare match while counting down clear** Writing a 1_B into this bit clears the ***CC4yINTS***.CMDS bit. A read always returns 0.
RE0A	8	w	**Event 0 detection clear** Writing a 1_B into this bit clears the ***CC4yINTS***.E0AS bit. A read always returns 0.
RE1A	9	w	**Event 1 detection clear** Writing a 1_B into this bit clears the ***CC4yINTS***.E1AS bit. A read always returns 0.
RE2A	10	w	**Event 2 detection clear** Writing a 1_B into this bit clears the ***CC4yINTS***.E2AS bit. A read always returns 0.
RTRPF	11	w	**Trap Flag status clear** Writing a 1_B into this bit clears the ***CC4yINTS***.TRPF bit. Not valid if ***CC4yTC***.TRPEN = 1_B and the Trap State is still active. A read always returns 0.
0	7:4, 31:12	r	**Reserved** Read always returns 0

20.7.2.28 Register CC4ySTC

Through this register it is possible to configure the extended options for the shadow transfer mechanism.

CC4ySTC (y=0-3) Address: $01B4_H + 0100_H * y$

Shadow transfer control Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0										ASFC	ASDC	ASLC	0	ASCC	ASPC
r										rw	rw	rw	r	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0						IRFC	IRDC	IRLC	0	IRCC	IRPC	0	STM		CSE
r						rw	rw	rw	r	rw	rw	r	rw		rw

Field	Bits	Type	Description
CSE	0	rw	**Cascaded shadow transfer enable** 0_B Cascaded shadow transfer disabled 1_B Cascaded shadow transfer enabled

(continued)

Field	Bits	Type	Description
STM	2:1	rw	**Shadow transfer mode** 00_B Shadow transfer is done in Period Match and One match. 01_B Shadow transfer is done only in Period Match. 10_B Shadow transfer is done only in One Match. 11_B Reserved *Note: This field only has effect if the timer is in Center Aligned Mode and coherent update is used.*
IRPC	4	rw	**Immediate Write into Period Configuration** 0_B Update of the period value is done coherently with PWM cycle 1_B Update of the period value happens immediately after a shadow transfer is request
IRCC	5	rw	**Immediate Write into Compare Configuration** 0_B Update of the compare value is done coherently with PWM cycle 1_B Update of the compare value happens immediately after a shadow transfer is request
IRLC	7	rw	**Immediate Write into Passive Level Configuration** 0_B Update of the pwm passive level is done coherently with PWM cycle 1_B Update of the pwm passive level value happens immediately after a shadow transfer is request
IRDC	8	rw	**Immediate Write into Dither Value Configuration** 0_B Update of the dither compare value is done coherently with PWM cycle 1_B Update of the dither compare value happens immediately after a shadow transfer is request
IRFC	9	rw	**Immediate Write into Floating Prescaler Value Configuration** 0_B Update of the floating prescaler value is done coherently with PWM cycle 1_B Update of the floating prescaler value happens immediately after a shadow transfer is request
ASPC	16	rw	**Automatic Shadow Transfer request when writing into Period Shadow Register** 0_B Writing into Period Shadow register does not automatically requests a shadow transfer 1_B Writing into Period Shadow register will automatically requests a shadow transfer *Note: When enabled, the request is going to be triggered for all the shadow registers*

(continued)

Field	Bits	Type	Description
ASCC	17	rw	**Automatic Shadow transfer request when writing into Compare Shadow Register** 0_B Writing into Compare Shadow register does not automatically requests a shadow transfer 1_B Writing into Compare Shadow register automatically requests a shadow transfer *Note: When enabled, the request is going to be triggered for all the shadow registers*
ASLC	19	rw	**Automatic Shadow transfer request when writing into Passive Level register** 0_B Writing into Passivel Level register does not automatically requests a shadow transfer 1_B Writing into Passive Level register automatically requests a shadow transfer *Note: When enabled, the request is going to be triggered for all the shadow registers*
ASDC	20	rw	**Automatic Shadow transfer request when writing into Dither Shadow register** 0_B Writing into Dither Shadow register does not automatically requests a shadow transfer 1_B Writing into Dither Shadow register automatically requests a shadow transfer *Note: When enabled, the request is going to be triggered for all the shadow registers*
ASFC	21	rw	**Automatic Shadow transfer request when writing into Floating Prescaler Shadow register** 0_B Writing into Floating Prescaler Shadow register does not automatically requests a shadow transfer 1_B Writing into Floating Prescaler Shadow register automatically requests a shadow transfer *Note: When enabled, the request is going to be triggered for all the shadow registers*
0	3, 6, 15:10, 18, 31:22	r	**Reserved** Read always returns 0

20.7.2.29 Register CC4yECRD0

Through this register it is possible to read back the FIFO structure of the capture function that is linked with the capture trigger 0. The read back is only valid if the ***CC4yTC***.ECM = 1_B.

CC4yECRD0 (y=0-3) Address: $01B8_H + 0100_H * y$

Extended Read Back 0 Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0						LCV	FFL	VPTR		SPTR		FPCV			
r						rh	rh	rh		rh		rh			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPV															
rh															

Field	Bits	Type	Description
CAPV	15:0	rh	**Timer Capture Value** This field contains the timer captured value
FPCV	19:16	rh	**Prescaler Capture value** This field contains the value of the prescaler clock division associated with the specific CAPV field
SPTR	21:20	rh	**Slice pointer** This field indicates the slice index in which the value was captured. 00_B CC40 01_B CC41 10_B CC42 11_B CC43
VPTR	23:22	rh	**Capture register pointer** This field indicates the capture register index in which the value was captured. 00_B Capture register 0 01_B Capture register 1 10_B Capture register 2 11_B Capture register 3
FFL	24	rh	**Full Flag** This bit indicates if the associated capture register contains a new value. 0_B No new value was captured into this register 1_B A new value has been captured into this register
LCV	25	rh	**Lost Capture Value** This field indicates if between two reads of the ECRD0 a capture trigger occured while the FIFO structure was full. If a capture trigger occured between two reads than a capture value was lost. This field is automatically cleared by the HW whenever a read to the ECRD occurs. 0_B No capture was lost 1_B A capture was lost

(continued)

Field	Bits	Type	Description
0	31:26	r	**Reserved** Read always returns 0

20.7.2.30 Register CC4yECRD1

Through this register it is possible to read back the FIFO structure of the capture function that is linked with the capture trigger 1. The read back is only valid if the ***CC4yTC***.ECM = 1_B.

CC4yECRD1 (y=0-3) Address: $01BC_H + 0100_H * y$

Extended Read Back 1 Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0						**LCV**	**FFL**	**VPTR**		**SPTR**		**FPCV**			
r						rh	rh	rh		rh		rh			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPV															
rh															

Field	Bits	Type	Description
CAPV	15:0	rh	**Timer Capture Value** This field contains the timer captured value
FPCV	19:16	rh	**Prescaler Capture value** This field contains the value of the prescaler clock division associated with the specific CAPV field
SPTR	21:20	rh	**Slice pointer** This field indicates the slice index in which the value was captured. 00_B CC40 01_B CC41 10_B CC42 11_B CC43
VPTR	23:22	rh	**Capture register pointer** This field indicates the capture register index in which the value was captured. 00_B Capture register 0 01_B Capture register 1 10_B Capture register 2 11_B Capture register 3
FFL	24	rh	**Full Flag** This bit indicates if the associated capture register contains a new value. 0_B No new value was captured into this register 1_B A new value has been captured into this register

(continued)

Field	Bits	Type	Description
LCV	25	rh	**Lost Capture Value** This field indicates if between two reads of the ECRD0 a capture trigger occured while the FIFO structure was full. If a capture trigger occured between two reads than a capture value was lost. This field is automatically cleared by the HW whenever a read to the ECRD occurs. 0_B No capture was lost 1_B A capture was lost
0	31:26	r	**Reserved** Read always returns 0

20.8 Interconnects

The tables that refer to the “global pins” are the ones that contain the inputs/outputs of each module that are common to all slices.

The GPIO connections are available at the Ports chapter.

20.8.1 CCU40 Pins

Table 256 CCU40 Pin Connections

Global Input/Output	I/O	Connected To	Description
CCU40.MCLK	I	PCLK	
CCU40.CLKA	I	ERU1.IOUT0	
CCU40.CLKB	I	ERU0.IOUT0	
CCU40.CLKC	I	ERU0.IOUT1	
CCU40.MCSS	I		
CCU40.SR0	O	NVIC; ; ERU0.OGU01; CCU40.IN0BB;	
CCU40.SR1	O	NVIC; ERU0.OGU11; CCU40.IN2AT; CCU40.IN3AT; CCU40.IN1BB;	
CCU40.SR2	O	NVIC; ; ; ERU0.OGU21; CCU40.IN0AT; CCU40.IN1AT; CCU40.IN2BB;	
CCU40.SR3	O	NVIC; ; ; ; ERU0.OGU31; CCU40.IN3BB;	

Table 257 CCU40 - CC40 Pin Connections

Input/Output	I/O	Connected To	Description
CCU40.IN0AA	I	P0.12	General purpose function
CCU40.IN0AB	I		General purpose function

Table 257 CCU40 - CC40 Pin Connections (continued)

Input/Output	I/O	Connected To	Description
CCU40.IN0AC	I		General purpose function
CCU40.IN0AD	I	ERU0.PDOUT1	General purpose function
CCU40.IN0AE	I		General purpose function
CCU40.IN0AF	I		General purpose function
CCU40.IN0AG	I		General purpose function
CCU40.IN0AH	I	CCU80.ST3	General purpose function
CCU40.IN0AI	I	SCU.GSC40	General purpose function
CCU40.IN0AJ	I	ERU0.PDOUT0	General purpose function
CCU40.IN0AK	I	ERU0.IOUT0	General purpose function
CCU40.IN0AL	I	USIC0_CH0.DX2INS	General purpose function
CCU40.IN0AM	I	CCU40.GP10	General purpose function
CCU40.IN0AN	I	CCU40.ST1	General purpose function
CCU40.IN0AO	I	CCU40.ST2	General purpose function
CCU40.IN0AP	I	CCU40.ST3	General purpose function
CCU40.IN0AQ	I	DAC0.OUT0	General purpose function
CCU40.IN0AR	I	ACMP1.OUT	General purpose function
CCU40.IN0AS	I	ACMP0.OUT	General purpose function
CCU40.IN0AT	I	CCU40.SR2	General purpose function
CCU40.IN0AU	I	CCU40.ST0	General purpose function
CCU40.IN0AV	I		General purpose function
CCU40.IN0AW	I	ERU1.PDOUT0	General purpose function
CCU40.IN0AX	I	ERU1.IOUT0	General purpose function
CCU40.IN0AY	I	ERU1.PDOUT1	General purpose function
CCU40.IN0AZ	I	DAC0.OUT6	General purpose function
CCU40.IN0BA	I	P4.0	General purpose function
CCU40.IN0BB	I	CCU40.SR0	General purpose function
CCU40.IN0BC	I	0	Reserved
CCU40.IN0BD	I	0	Reserved
CCU40.IN0BE	I	0	Reserved
CCU40.IN0BF	I	0	Reserved
CCU40.IN0BG	I	0	Reserved
CCU40.IN0BH	I	0	Reserved
CCU40.IN0BI	I	0	Reserved
CCU40.IN0BJ	I	0	Reserved

Table 257 CCU40 - CC40 Pin Connections (continued)

Input/Output	I/O	Connected To	Description
CCU40.IN0BK	I	0	Reserved
CCU40.IN0BL	I	0	Reserved
CCU40.IN0BM	I	0	Reserved
CCU40.IN0BN	I	0	Reserved
CCU40.IN0BO	I	0	Reserved
CCU40.IN0BP	I	0	Reserved
CCU40.IN0BQ	I	0	Reserved
CCU40.IN0BR	I	0	Reserved
CCU40.IN0BS	I	0	Reserved
CCU40.IN0BT	I	0	Reserved
CCU40.IN0BU	I	0	Reserved
CCU40.IN0BV	I	0	Reserved
CCU40.MCI0	I	DAC0.OUT2	Multi Channel pattern input
CCU40.OUT0	O	P1.0; P2.0; P4.0; P2.0.HW1 direction control;	Slice compare output
CCU40.GP00	O	CCU40.IN3AM	Selected signal for event 0
CCU40.GP01	O	not connected	Selected signal for event 1
CCU40.GP02	O		Selected signal for event 2
CCU40.ST0	O	CCU40.IN0AU; CCU40.IN1AN; CCU40.IN2AN; CCU40.IN3AN; CCU41.IN0AL; ; ERU1.0B0;	Slice status bit
CCU40.PS0	O	not connected	Multi channel pattern sync trigger: PM when counting UP (edge aligned) or OM when counting DOWN (center aligned)

Table 258 CCU40 - CC41 Pin Connections

Input/Output	I/O	Connected To	Description
CCU40.IN1AA	I	P0.12	General purpose function
CCU40.IN1AB	I	P0.7	General purpose function
CCU40.IN1AC	I		General purpose function
CCU40.IN1AD	I	ERU0.PDOUT0	General purpose function
CCU40.IN1AE	I		General purpose function
CCU40.IN1AF	I		General purpose function
CCU40.IN1AG	I		General purpose function
CCU40.IN1AH	I		General purpose function
CCU40.IN1AI	I	SCU.GSC40	General purpose function

Table 258 CCU40 - CC41 Pin Connections (continued)

Input/Output	I/O	Connected To	Description
CCU40.IN1AJ	I	ERU0.PDOUT1	General purpose function
CCU40.IN1AK	I	ERU0.IOUT1	General purpose function
CCU40.IN1AL	I	USIC0_CH1.DX2INS	General purpose function
CCU40.IN1AM	I	CCU40.GP20	General purpose function
CCU40.IN1AN	I	CCU40.ST0	General purpose function
CCU40.IN1AO	I	CCU40.ST2	General purpose function
CCU40.IN1AP	I	CCU40.ST3	General purpose function
CCU40.IN1AQ	I	DAC0.OUT8	
CCU40.IN1AR	I	ACMP3.OUT	
CCU40.IN1AS	I	ACMP2.OUT	
CCU40.IN1AT	I	CCU40.SR2	
CCU40.IN1AU	I	CCU40.ST1	
CCU40.IN1AV	I		
CCU40.IN1AW	I	ERU1.PDOUT1	
CCU40.IN1AX	I	ERU1.IOUT1	
CCU40.IN1AY	I	ERU1.PDOUT0	
CCU40.IN1AZ	I	DAC0.OUT3	
CCU40.IN1BA	I	P4.1	
CCU40.IN1BB	I	CCU40.SR1	
CCU40.IN1BC	I	0	Reserved
CCU40.IN1BD	I	0	Reserved
CCU40.IN1BE	I	0	Reserved
CCU40.IN1BF	I	0	Reserved
CCU40.IN1BG	I	0	Reserved
CCU40.IN1BH	I	0	Reserved
CCU40.IN1BI	I	0	Reserved
CCU40.IN1BJ	I	0	Reserved
CCU40.IN1BK	I	0	Reserved
CCU40.IN1BL	I	0	Reserved
CCU40.IN1BM	I	0	Reserved
CCU40.IN1BN	I	0	Reserved
CCU40.IN1BO	I	0	Reserved
CCU40.IN1BP	I	0	Reserved
CCU40.IN1BQ	I	0	Reserved

Table 258 CCU40 - CC41 Pin Connections (continued)

Input/Output	I/O	Connected To	Description
CCU40.IN1BR	I	0	Reserved
CCU40.IN1BS	I	0	Reserved
CCU40.IN1BT	I	0	Reserved
CCU40.IN1BU	I	0	Reserved
CCU40.IN1BV	I	0	Reserved
CCU40.MCI1	I	DAC0.OUT3	Multi Channel pattern input
CCU40.OUT1	O	P1.1; P2.1; P4.1; P2.1.HW1 direction control;	Slice compare output
CCU40.GP10	O	CCU40.IN0AM	Selected signal for event 0
CCU40.GP11	O	not connected	Selected signal for event 1
CCU40.GP12	O		Selected signal for event 2
CCU40.ST1	O	CCU40.IN0AN; CCU40.IN1AU; CCU40.IN2AO; CCU40.IN3AO; CCU41.IN1AL; ERU1.1B0;	Slice status bit
CCU40.PS1	O		Multi channel pattern sync trigger: PM when counting UP (edge aligned) or OM when counting DOWN (center aligned)

Table 259 CCU40 - CC42 Pin Connections

Input/Output	I/O	Connected To	Description
CCU40.IN2AA	I	P0.12	General purpose function
CCU40.IN2AB	I	P0.8	General purpose function
CCU40.IN2AC	I		General purpose function
CCU40.IN2AD	I	ERU0.PDOUT3	General purpose function
CCU40.IN2AE	I		General purpose function
CCU40.IN2AF	I		General purpose function
CCU40.IN2AG	I		General purpose function
CCU40.IN2AH	I		General purpose function
CCU40.IN2AI	I	SCU.GSC40	General purpose function
CCU40.IN2AJ	I	ERU0.PDOUT2	General purpose function
CCU40.IN2AK	I	ERU0.IOUT2	General purpose function
CCU40.IN2AL	I	0	General purpose function
CCU40.IN2AM	I	CCU40.GP30	General purpose function
CCU40.IN2AN	I	CCU40.ST0	General purpose function
CCU40.IN2AO	I	CCU40.ST1	General purpose function
CCU40.IN2AP	I	CCU40.ST3	General purpose function

Table 259 CCU40 - CC42 Pin Connections (continued)

Input/Output	I/O	Connected To	Description
CCU40.IN2AQ	I	DAC0.OUT4	General purpose function
CCU40.IN2AR	I	ACMP2.OUT	General purpose function
CCU40.IN2AS	I	ACMP1.OUT	General purpose function
CCU40.IN2AT	I	CCU40.SR1	General purpose function
CCU40.IN2AU	I	CCU40.ST2	General purpose function
CCU40.IN2AV	I		General purpose function
CCU40.IN2AW	I	ERU1.PDOUT2	General purpose function
CCU40.IN2AX	I	ERU1.IOUT2	General purpose function
CCU40.IN2AY	I	ERU1.PDOUT3	General purpose function
CCU40.IN2AZ	I	DAC0.OUT7	General purpose function
CCU40.IN2BA	I	P4.2	General purpose function
CCU40.IN2BB	I	CCU40.SR2	General purpose function
CCU40.IN2BC	I		General purpose function
CCU40.IN2BD	I	0	Reserved
CCU40.IN2BE	I	0	Reserved
CCU40.IN2BF	I	0	Reserved
CCU40.IN2BG	I	0	Reserved
CCU40.IN2BH	I	0	Reserved
CCU40.IN2BI	I	0	Reserved
CCU40.IN2BJ	I	0	Reserved
CCU40.IN2BK	I	0	Reserved
CCU40.IN2BL	I	0	Reserved
CCU40.IN2BM	I	0	Reserved
CCU40.IN2BN	I	0	Reserved
CCU40.IN2BO	I	0	Reserved
CCU40.IN2BP	I	0	Reserved
CCU40.IN2BQ	I	0	Reserved
CCU40.IN2BR	I	0	Reserved
CCU40.IN2BS	I	0	Reserved
CCU40.IN2BT	I	0	Reserved
CCU40.IN2BU	I	0	Reserved
CCU40.IN2BV	I	0	Reserved
CCU40.MCI2	I	DAC0.OUT4	Multi Channel pattern input

Table 259 CCU40 - CC42 Pin Connections (continued)

Input/Output	I/O	Connected To	Description
CCU40.OUT2	O	P0.8; P2.10; P4.2; P2.8.HW1 pull control; P2.10.HW1 direction control;	Slice compare output
CCU40.GP20	O	CCU40.IN1AM	Selected signal for event 0
CCU40.GP21	O	not connected	Selected signal for event 1
CCU40.GP22	O		Selected signal for event 2
CCU40.ST2	O	CCU40.IN0AO; CCU40.IN1AO; CCU40.IN2AU; CCU40.IN3AP; CCU41.IN2AL; ERU1.2B0;	Slice status bit
CCU40.PS0	O	not connected	Multi channel pattern sync trigger: PM when counting UP (edge aligned) or OM when counting DOWN (center aligned)

Table 260 CCU40 - CC43 Pin Connections

Input/Output	I/O	Connected To	Description
CCU40.IN3AA	I	P0.12	General purpose function
CCU40.IN3AB	I	P0.9	General purpose function
CCU40.IN3AC	I		General purpose function
CCU40.IN3AD	I	ERU0.PDOUT2	General purpose function
CCU40.IN3AE	I		General purpose function
CCU40.IN3AF	I		General purpose function
CCU40.IN3AG	I	VADC0.G0ARBCNT	General purpose function
CCU40.IN3AH	I		General purpose function
CCU40.IN3AI	I	SCU.GSC40	General purpose function
CCU40.IN3AJ	I	ERU0.PDOUT3	General purpose function
CCU40.IN3AK	I	ERU0.IOUT3	General purpose function
CCU40.IN3AL	I	0	General purpose function
CCU40.IN3AM	I	CCU40.GP00	General purpose function
CCU40.IN3AN	I	CCU40.ST0	General purpose function
CCU40.IN3AO	I	CCU40.ST1	General purpose function
CCU40.IN3AP	I	CCU40.ST2	General purpose function
CCU40.IN3AQ	I	DAC0.OUT5	General purpose function
CCU40.IN3AR	I	ACMP0.OUT	General purpose function
CCU40.IN3AS	I	ACMP3.OUT	General purpose function
CCU40.IN3AT	I	CCU40.SR1	General purpose function
CCU40.IN3AU	I	CCU40.ST3	General purpose function

Table 260 CCU40 - CC43 Pin Connections (continued)

Input/Output	I/O	Connected To	Description
CCU40.IN3AV	I		General purpose function
CCU40.IN3AW	I	ERU1.PDOUT3	General purpose function
CCU40.IN3AX	I	ERU1.IOUT3	General purpose function
CCU40.IN3AY	I	ERU1.PDOUT2	General purpose function
CCU40.IN3AZ	I	DAC0.OUT1	General purpose function
CCU40.IN3BA	I	P4.3	General purpose function
CCU40.IN3BB	I	CCU40.SR3	General purpose function
CCU40.IN3BC	I		General purpose function
CCU40.IN3BD	I		General purpose function
CCU40.IN3BE	I	0	Reserved
CCU40.IN3BF	I	0	Reserved
CCU40.IN3BG	I	0	Reserved
CCU40.IN3BH	I	0	Reserved
CCU40.IN3BI	I	0	Reserved
CCU40.IN3BJ	I	0	Reserved
CCU40.IN3BK	I	0	Reserved
CCU40.IN3BL	I	0	Reserved
CCU40.IN3BM	I	0	Reserved
CCU40.IN3BN	I	0	Reserved
CCU40.IN3BO	I	0	Reserved
CCU40.IN3BP	I	0	Reserved
CCU40.IN3BQ	I	0	Reserved
CCU40.IN3BR	I	0	Reserved
CCU40.IN3BS	I	0	Reserved
CCU40.IN3BT	I	0	Reserved
CCU40.IN3BU	I	0	Reserved
CCU40.IN3BV	I	0	Reserved
CCU40.MCI3	I	DAC0.OUT5	Multi Channel pattern input
CCU40.OUT3	O	P0.9; P2.11; P4.3; P2.2.HW1 pull control; P2.6.HW1 pull control; P2.11.HW1 direction control;	Slice compare output
CCU40.GP30	O	CCU40.IN2AM	Selected signal for event 0
CCU40.GP31	O	not connected	Selected signal for event 1
CCU40.GP32	O		Selected signal for event 2

Table 260 CCU40 - CC43 Pin Connections (continued)

Input/Output	I/O	Connected To	Description
CCU40.ST3	O	CCU40.IN0AP; CCU40.IN1AP; CCU40.IN2AP; CCU40.IN3AU; CCU41.IN3AL; ; ERU1.3B0;	Slice status bit
CCU40.PS3	O	not connected	Multi channel pattern sync trigger: PM when counting UP (edge aligned) or OM when counting DOWN (center aligned)

20.8.2 CCU41 Pins

Table 261 CCU41 Pin Connections

Global Input/Output	I/O	Connected To	Description
CCU41.MCLK	I	PCLK	
CCU41.CLKA	I	ERU0.IOUT0	
CCU41.CLKB	I	ERU1.IOUT0	
CCU41.CLKC	I	ERU1.IOUT1	
CCU41.MCSS	I	POSIF1.OUT6	
CCU41.SR0	O	NVIC; ; POSIF1.MSETA; ERU1.OGU01; CCU41.IN0BB;	
CCU41.SR1	O	NVIC; ERU1.OGU11; CCU41.IN2AT; CCU41.IN3AT; CCU41.IN1BB;	
CCU41.SR2	O	NVIC; ; ; ; ; ; ERU1.OGU21; CCU41.IN0AT; CCU41.IN1AT; CCU41.IN2BB;	
CCU41.SR3	O	NVIC; ; ; ; ; ; ; ERU1.OGU31; CCU41.IN3BB;	

Table 262 CCU41 - CC40 Pin Connections

Input/Output	I/O	Connected To	Description
CCU41.IN0AA	I		General purpose function
CCU41.IN0AB	I		General purpose function
CCU41.IN0AC	I	P4.0	General purpose function
CCU41.IN0AD	I	ERU0.PDOUT1	General purpose function
CCU41.IN0AE	I	POSIF1.OUT0	General purpose function
CCU41.IN0AF	I	POSIF1.OUT1	General purpose function
CCU41.IN0AG	I	POSIF1.OUT3	General purpose function
CCU41.IN0AH	I	;	General purpose function
CCU41.IN0AI	I	SCU.GSC41	General purpose function

Table 262 CCU41 - CC40 Pin Connections (continued)

Input/Output	I/O	Connected To	Description
CCU41.IN0AJ	I	ERU0.PDOUT0	General purpose function
CCU41.IN0AK	I	ERU0.IOUT0	General purpose function
CCU41.IN0AL	I	CCU40.ST0	General purpose function
CCU41.IN0AM	I	CCU41.GP10	General purpose function
CCU41.IN0AN	I	CCU41.ST1	General purpose function
CCU41.IN0AO	I	CCU41.ST2	General purpose function
CCU41.IN0AP	I	CCU41.ST3	General purpose function
CCU41.IN0AQ	I	DAC0.OUT0	General purpose function
CCU41.IN0AR	I	ACMP1.OUT	General purpose function
CCU41.IN0AS	I	ACMP0.OUT	General purpose function
CCU41.IN0AT	I	CCU41.SR2	General purpose function
CCU41.IN0AU	I	CCU41.ST0	General purpose function
CCU41.IN0AV	I	P4.4	General purpose function
CCU41.IN0AW	I	ERU1.PDOUT0	General purpose function
CCU41.IN0AX	I	ERU1.IOUT0	General purpose function
CCU41.IN0AY	I	ERU1.PDOUT1	General purpose function
CCU41.IN0AZ	I	DAC0.OUT6	General purpose function
CCU41.IN0BA	I		General purpose function
CCU41.IN0BB	I	CCU41.SR0	General purpose function
CCU41.IN0BC	I	USIC1_CH0.DX2INS	General purpose function
CCU41.IN0BD	I	0	Reserved
CCU41.IN0BE	I	0	Reserved
CCU41.IN0BF	I	0	Reserved
CCU41.IN0BG	I	0	Reserved
CCU41.IN0BH	I	0	Reserved
CCU41.IN0BI	I	0	Reserved
CCU41.IN0BJ	I	0	Reserved
CCU41.IN0BK	I	0	Reserved
CCU41.IN0BL	I	0	Reserved
CCU41.IN0BM	I	0	Reserved
CCU41.IN0BN	I	0	Reserved
CCU41.IN0BO	I	0	Reserved
CCU41.IN0BP	I	0	Reserved
CCU41.IN0BQ	I	0	Reserved

Table 262 CCU41 - CC40 Pin Connections (continued)

Input/Output	I/O	Connected To	Description
CCU41.IN0BR	I	0	Reserved
CCU41.IN0BS	I	0	Reserved
CCU41.IN0BT	I	0	Reserved
CCU41.IN0BU	I	0	Reserved
CCU41.IN0BV	I	0	Reserved
CCU41.MCI0	I	DAC0.OUT0	Multi Channel pattern input
CCU41.OUT0	O	P4.0; P4.4;	Slice compare output
CCU41.GP00	O	CCU41.IN3AM	Selected signal for event 0
CCU41.GP01	O	not connected	Selected signal for event 1
CCU41.GP02	O		Selected signal for event 2
CCU41.ST0	O	CCU41.IN0AU; CCU41.IN1AN; CCU41.IN2AN; CCU41.IN3AN; ; POSIF1.HSDA; ERU1.0B1; ; ; ;	Slice status bit
CCU41.PS0	O	not connected	Multi channel pattern sync trigger: PM when counting UP (edge aligned) or OM when counting DOWN (center aligned)

Table 263 CCU41 - CC41 Pin Connections

Input/Output	I/O	Connected To	Description
CCU41.IN1AA	I		General purpose function
CCU41.IN1AB	I		General purpose function
CCU41.IN1AC	I	P4.1	General purpose function
CCU41.IN1AD	I	ERU0.PDOUT0	General purpose function
CCU41.IN1AE	I	POSIF1.OUT0	General purpose function
CCU41.IN1AF	I	POSIF1.OUT1	General purpose function
CCU41.IN1AG	I	POSIF1.OUT3	General purpose function
CCU41.IN1AH	I	POSIF1.OUT4	General purpose function
CCU41.IN1AI	I	SCU.GSC41	General purpose function
CCU41.IN1AJ	I	ERU0.PDOUT1	General purpose function
CCU41.IN1AK	I	ERU0.IOUT1	General purpose function
CCU41.IN1AL	I	CCU40.ST1	General purpose function
CCU41.IN1AM	I	CCU41.GP20	General purpose function
CCU41.IN1AN	I	CCU41.ST0	General purpose function
CCU41.IN1AO	I	CCU41.ST2	General purpose function
CCU41.IN1AP	I	CCU41.ST3	General purpose function

Table 263 CCU41 - CC41 Pin Connections (continued)

Input/Output	I/O	Connected To	Description
CCU41.IN1AQ	I	DAC0.OUT1	General purpose function
CCU41.IN1AR	I	ACMP3.>ACMP3.OUT	General purpose function
CCU41.IN1AS	I	ACMP2.OUT	General purpose function
CCU41.IN1AT	I	CCU41.SR2	General purpose function
CCU41.IN1AU	I	CCU41.ST1	General purpose function
CCU41.IN1AV	I	P4.5	General purpose function
CCU41.IN1AW	I	ERU1.PDOUT1	General purpose function
CCU41.IN1AX	I	ERU1.IOUT1	General purpose function
CCU41.IN1AY	I	ERU1.PDOUT0	General purpose function
CCU41.IN1AZ	I	DAC0.OUT3	General purpose function
CCU41.IN1BA	I		General purpose function
CCU41.IN1BB	I	CCU41.SR1	General purpose function
CCU41.IN1BC	I		General purpose function
CCU41.IN1BD	I	0	Reserved
CCU41.IN1BE	I	0	Reserved
CCU41.IN1BF	I	0	Reserved
CCU41.IN1BG	I	0	Reserved
CCU41.IN1BH	I	0	Reserved
CCU41.IN1BI	I	0	Reserved
CCU41.IN1BJ	I	0	Reserved
CCU41.IN1BK	I	0	Reserved
CCU41.IN1BL	I	0	Reserved
CCU41.IN1BM	I	0	Reserved
CCU41.IN1BN	I	0	Reserved
CCU41.IN1BO	I	0	Reserved
CCU41.IN1BP	I	0	Reserved
CCU41.IN1BQ	I	0	Reserved
CCU41.IN1BR	I	0	Reserved
CCU41.IN1BS	I	0	Reserved
CCU41.IN1BT	I	0	Reserved
CCU41.IN1BU	I	0	Reserved
CCU41.IN1BV	I	0	Reserved
CCU41.MCI1	I	DAC0.OUT1	Multi Channel pattern input
CCU41.OUT1	O	P4.1; P4.5;	Slice compare output

Table 263 CCU41 - CC41 Pin Connections (continued)

Input/Output	I/O	Connected To	Description
CCU41.GP10	O	CCU41.IN0AM	Selected signal for event 0
CCU41.GP11	O	not connected	Selected signal for event 1
CCU41.GP12	O		Selected signal for event 2
CCU41.ST1	O	CCU41.IN0AN; CCU41.IN1AU; CCU41.IN2AO; CCU41.IN3AO; POSIF1.MSETB; ERU1.1B1;	Slice status bit
CCU41.PS1	O	POSIF1.MSYNCC	Multi channel pattern sync trigger: PM when counting UP (edge aligned) or OM when counting DOWN (center aligned)

Table 264 CCU41 - CC42 Pin Connections

Input/Output	I/O	Connected To	Description
CCU41.IN2AA	I		General purpose function
CCU41.IN2AB	I		General purpose function
CCU41.IN2AC	I	P4.2	General purpose function
CCU41.IN2AD	I	ERU0.PDOUT3	General purpose function
CCU41.IN2AE	I	POSIF1.OUT1	General purpose function
CCU41.IN2AF	I	POSIF1.OUT2	General purpose function
CCU41.IN2AG	I	POSIF1.OUT3	General purpose function
CCU41.IN2AH	I	POSIF1.OUT4	General purpose function
CCU41.IN2AI	I	SCU.GSC41	General purpose function
CCU41.IN2AJ	I	ERU0.PDOUT2	General purpose function
CCU41.IN2AK	I	ERU0.IOUT2	General purpose function
CCU41.IN2AL	I	CCU40.ST2	General purpose function
CCU41.IN2AM	I	CCU41.GP30	General purpose function
CCU41.IN2AN	I	CCU41.ST0	General purpose function
CCU41.IN2AO	I	CCU41.ST1	General purpose function
CCU41.IN2AP	I	CCU41.ST3	General purpose function
CCU41.IN2AQ	I	DAC0.OUT2	General purpose function
CCU41.IN2AR	I	ACMP2.OUT	General purpose function
CCU41.IN2AS	I	ACMP1.OUT	General purpose function
CCU41.IN2AT	I	CCU41.SR1	General purpose function
CCU41.IN2AU	I	CCU41.ST2	General purpose function
CCU41.IN2AV	I	P4.6	General purpose function
CCU41.IN2AW	I	ERU1.PDOUT2	General purpose function

Table 264 CCU41 - CC42 Pin Connections (continued)

Input/Output	I/O	Connected To	Description
CCU41.IN2AX	I	ERU1.IOUT2	General purpose function
CCU41.IN2AY	I	ERU1.PDOUT3	General purpose function
CCU41.IN2AZ	I	DAC0.OUT7	General purpose function
CCU41.IN2BA	I		General purpose function
CCU41.IN2BB	I	CCU41.SR2	General purpose function
CCU41.IN2BC	I	POSIF1.OUT0	General purpose function
CCU41.IN2BD	I	0	Reserved
CCU41.IN2BE	I	0	Reserved
CCU41.IN2BF	I	0	Reserved
CCU41.IN2BG	I	0	Reserved
CCU41.IN2BH	I	0	Reserved
CCU41.IN2BI	I	0	Reserved
CCU41.IN2BJ	I	0	Reserved
CCU41.IN2BK	I	0	Reserved
CCU41.IN2BL	I	0	Reserved
CCU41.IN2BM	I	0	Reserved
CCU41.IN2BN	I	0	Reserved
CCU41.IN2BO	I	0	Reserved
CCU41.IN2BP	I	0	Reserved
CCU41.IN2BQ	I	0	Reserved
CCU41.IN2BR	I	0	Reserved
CCU41.IN2BS	I	0	Reserved
CCU41.IN2BT	I	0	Reserved
CCU41.IN2BU	I	0	Reserved
CCU41.IN2BV	I	0	Reserved
CCU41.MCI2	I	DAC0.OUT2	Multi Channel pattern input
CCU41.OUT2	O	P0.8; P4.2; P4.6;	Slice compare output
CCU41.GP20	O	CCU41.IN1AM	Selected signal for event 0
CCU41.GP21	O	not connected	Selected signal for event 1
CCU41.GP22	O		Selected signal for event 2
CCU41.ST2	O	CCU41.IN0AO; CCU41.IN1AO; CCU41.IN2AU; CCU41.IN3AP; POSIF1.MSETC; ERU1.2B1;	Slice status bit

Table 264 CCU41 - CC42 Pin Connections (continued)

Input/Output	I/O	Connected To	Description
CCU41.PS0	O	not connected	Multi channel pattern sync trigger: PM when counting UP (edge aligned) or OM when counting DOWN (center aligned)

Table 265 CCU41 - CC43 Pin Connections

Input/Output	I/O	Connected To	Description
CCU41.IN3AA	I		General purpose function
CCU41.IN3AB	I		General purpose function
CCU41.IN3AC	I	P4.3	General purpose function
CCU41.IN3AD	I	ERU0.PDOUT2	General purpose function
CCU41.IN3AE	I	POSIF1.OUT3	General purpose function
CCU41.IN3AF	I	POSIF1.OUT5	General purpose function
CCU41.IN3AG	I		General purpose function
CCU41.IN3AH	I		General purpose function
CCU41.IN3AI	I	SCU.GSC41	General purpose function
CCU41.IN3AJ	I	ERU0.PDOUT3	General purpose function
CCU41.IN3AK	I	ERU0.IOUT3	General purpose function
CCU41.IN3AL	I	CCU40.ST3	General purpose function
CCU41.IN3AM	I	CCU41.GP00	General purpose function
CCU41.IN3AN	I	CCU41.ST0	General purpose function
CCU41.IN3AO	I	CCU41.ST1	General purpose function
CCU41.IN3AP	I	CCU41.ST2	General purpose function
CCU41.IN3AQ	I	DAC0.OUT5	General purpose function
CCU41.IN3AR	I	ACMP0.OUT	General purpose function
CCU41.IN3AS	I	ACMP3.>ACMP3.OUT	General purpose function
CCU41.IN3AT	I	CCU41.SR1	General purpose function
CCU41.IN3AU	I	CCU41.ST3	General purpose function
CCU41.IN3AV	I	P4.7	General purpose function
CCU41.IN3AW	I	ERU1.PDOUT3	General purpose function
CCU41.IN3AX	I	ERU1.IOUT3	General purpose function
CCU41.IN3AY	I	ERU1.PDOUT2	General purpose function
CCU41.IN3AZ	I	DAC0.OUT8	General purpose function
CCU41.IN3BA	I		General purpose function
CCU41.IN3BB	I	CCU41.SR3	General purpose function
CCU41.IN3BC	I	POSIF1.OUT0	General purpose function

Table 265 CCU41 - CC43 Pin Connections (continued)

Input/Output	I/O	Connected To	Description
CCU41.IN3BD	I	POSIF1.OUT1	General purpose function
CCU41.IN3BE	I	0	Reserved
CCU41.IN3BF	I	0	Reserved
CCU41.IN3BG	I	0	Reserved
CCU41.IN3BH	I	0	Reserved
CCU41.IN3BI	I	0	Reserved
CCU41.IN3BJ	I	0	Reserved
CCU41.IN3BK	I	0	Reserved
CCU41.IN3BL	I	0	Reserved
CCU41.IN3BM	I	0	Reserved
CCU41.IN3BN	I	0	Reserved
CCU41.IN3BO	I	0	Reserved
CCU41.IN3BP	I	0	Reserved
CCU41.IN3BQ	I	0	Reserved
CCU41.IN3BR	I	0	Reserved
CCU41.IN3BS	I	0	Reserved
CCU41.IN3BT	I	0	Reserved
CCU41.IN3BU	I	0	Reserved
CCU41.IN3BV	I	0	Reserved
CCU41.MCI3	I	DAC0.OUT5	Multi Channel pattern input
CCU41.OUT3	O	P0.9; P4.3; P4.7;	Slice compare output
CCU41.GP30	O	CCU41.IN2AM	Selected signal for event 0
CCU41.GP31	O	not connected	Selected signal for event 1
CCU41.GP32	O		Selected signal for event 2
CCU41.ST3	O	CCU41.IN0AP; CCU41.IN1AP; CCU41.IN2AP; CCU41.IN3AU; ; POSIF1.MSETD; ERU1.3B1;	Slice status bit
CCU41.PS3	O	not connected	Multi channel pattern sync trigger: PM when counting UP (edge aligned) or OM when counting DOWN (center aligned)

21 Position Interface Unit (POSIF)

The POSIF unit is a flexible and powerful component for motor control systems that use Rotary Encoders or Hall Sensors as feedback loop. The several configuration schemes of the module, target a very large universe of motor control application requirements. This enables the build of simple and complex control feedback loops, for industrial and automotive motor applications, targeting high performance motion and position monitoring.

Table 266 Abbreviations table

PWM	Pulse Width Modulation
POSIFx	Position Interface module instance x
CCU8x	Capture/Compare Unit 8 module instance x
CCU4x	Capture/Compare Unit 4 module instance x
CC8y	Capture/Compare Unit 8 Timer Slice instance y
CC4y	Capture/Compare Unit 4 Timer Slice instance y
SCU	System Control Unit
f_{posif}	POSIF module clock frequency

Note: A small “y” or “x” letter in a register indicates an index

21.1 Overview

The POSIF module is comprised of three major sub units, the Quadrature Decoder unit, the Hall Sensor Control unit and the Multi-Channel Mode unit.

The Quadrature Decoder Unit is used for position control linked with a rotary incremental encoder.

The Hall Sensor Control Unit is used for direct control of brushless DC motors.

The Multi-Channel Mode unit is used in conjunction with the Hall Sensor mode to output the wanted motor control pattern but also can be used in a stand-alone manner to perform a simple multi-channel control of several control units.

The POSIF module is used in conjunction with a CCU4 or CCU8 which enables a very flexible resource arrangement and optimization for any type of application.

21.1.1 Features

POSIF module features

The POSIF is built of three dedicated control units that can operate in a stand-alone manner.

The Quadrature Decoder Unit contains an output interface that enables position and velocity measurements when linked with a CCU4 module. The Hall Sensor Unit enables the control of a multi-channel pattern, that can be linked with up 8 output control sources. The Multi-Channel unit offers a complete built-in interaction with the Hall Sensor Mode and an easy stand-alone control loop.

General Features

- Quadrature Decoder
  - interface for position measurement
  - interface for motor revolution measurement
  - interface for velocity measurement
  - interrupt sources for phase error, motor revolution, direction change and error on phase decoding

- Hall Sensor Mode
  - Simple build-in mode for brushless DC motor control
  - Shadow register for the multi-channel pattern
  - Complete synchronization with the PWM signals and the multi-channel pattern update
  - interrupt sources for Correct Hall Event detection, Wrong Hall Event Detection
- Multi-Channel Mode
  - Simple usage with Hall Sensor Mode
  - stand-alone Multi-Channel mode
  - Shadow register for the multi-channel pattern

Additional features

- Quadrature Decoder mode can be used in parallel with the stand-alone Multi-Channel mode
- Several profiles (via CCU4) to perform position and velocity measurement for the Quadrature Decoder mode
- Programmable delay times (via CCU4) for input pattern evaluation and new pattern value for the Hall Sensor Mode

POSIF features vs. applications

On *Table 267* a summary of the major features of the POSIF unit mapped with the most common applications.

Table 267 Applications summary

Feature	Applications
Quadrature Decoder Mode	Easy plug-in for rotary encoders: • with or without index/top marker signal • gear-slip or shaft winding compensation • separate outputs for position, velocity and revolution control - matching different system requirements • extended profile for position tracking - with revolution measurement and multiple position triggers for each revolution • support for high dynamic speed changes due to tick-to-tick and tick-to-sync capturing method
Hall Sensor Mode	Easy plug-in for Motor control using Hall Sensors: • 2 or 3 Hall sensor topologies • extended input filtering to avoid unwanted pattern switch due to noisy input signals • synchronization with the PWM signals of the Capture/Compare Unit • Active freewheeling/synchronous rectification with dead time support (link with Capture/Compare Unit 8) • easy velocity measurement function by using a Capture/Compare unit Timer Slice
Multi-Channel Mode	Modulating multiple PWM signals: • parallel modulation controlled via SW for N PWM signals - for systems with multiple power converters • generating proprietary PWM modulations • parallel and synchronous shut down of N PWM signals due to system feedback

21.1.2 Block Diagram

Each POSIF module can operate in three different modes, Quadrature Decoder, Hall Sensor and stand-alone Multi-channel Mode. To complete the control/measurement loop of all these three modes, the POSIF needs to be linked with a CCU4/CCU8 module. In the case of the Quadrature Decoder mode, one CCU4 unit is needed, for the Hall Sensor Mode, one needs one slice of one CCU4 and a CCU8 unit. The connectivity between the stand-alone Multi-Channel mode and CCU4/CCU8 module(s) does not follow any usage constraints.

Each POSIF module contains 30 inputs and 25 outputs (including service requests), ***Figure 236***, that are going to be mapped to available functions of the module, depending in which configuration it was selected by the user: Quadrature Decoder, Hall Sensor or stand-alone Multi-Channel.

The module also has two dedicated Service request Lines, see ***Chapter 21.3***.

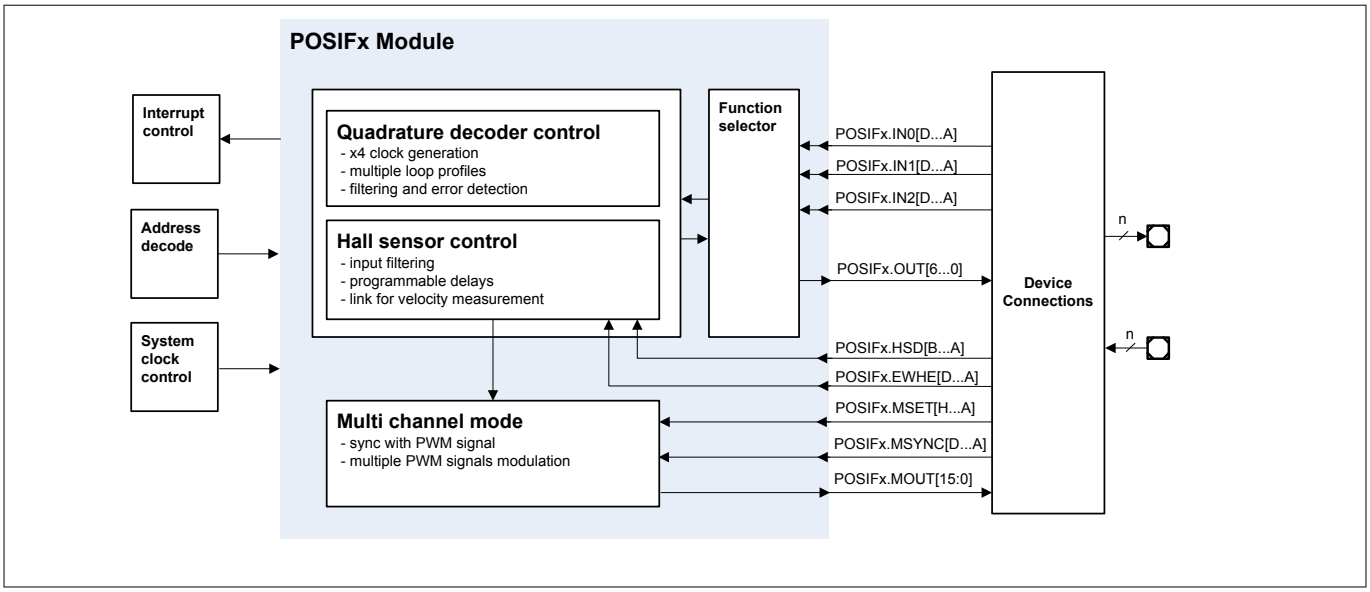


Figure 236 POSIF block diagram

21.2 Functional Description

The following sections describe the complete set of functions and usability of the POSIF peripheral.

In each figure several registers may be depicted to indicate controlability or configurability. These registers follow the description given in ***Figure 237*** . One should also note that indexing in a register can be done via the non capital y, x or n.

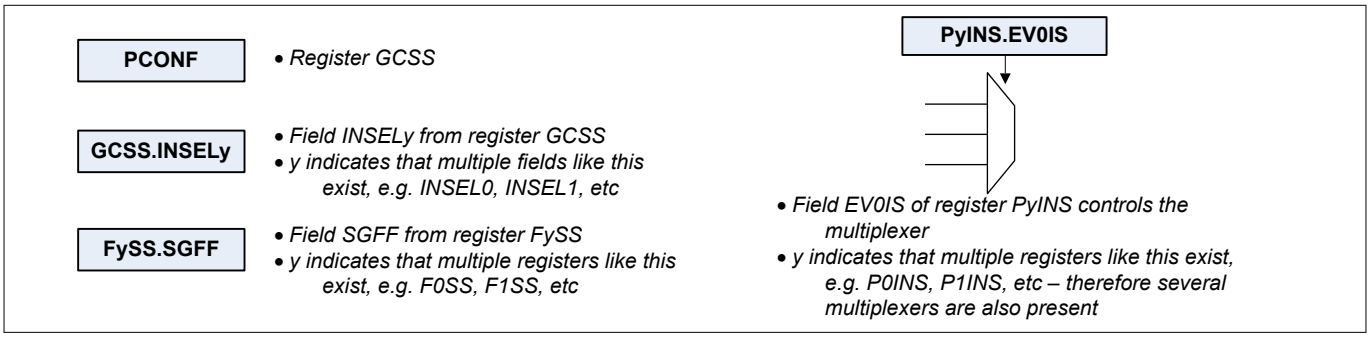


Figure 237 Register description in figures (example)

21.2.1 Overview

The POSIF module contains a function selector unit, that is used in parallel by both Quadrature Decoder and Hall Sensor Control units. This block selects which input signals should be decoded for each control unit. The function selector is also decoding the outputs coming from these two modes (Quadrature and Hall Sensor Mode).

The POSIF module also contains a subset of inputs that are only used in Hall Sensor/Multi-Channel Mode. These inputs are connected to a timer structure (CCU4/CCU8) and are used to control the delays between pattern sampling, multi-channel pattern update and synchronization, etc.

The Multi-Channel unit contains 16 dedicated outputs, that contain the current multi-channel pattern and that can be connected to a CCU8/CCU4.

The POSIF control unit contain a dedicated Run bit, that can be set/clear by SW. It can also generate a Sync start signal that can be connected to the timer units (CCU4/CCU8).

For the Quadrature Decoder Mode, there is the possibility to define which of the signals is the leading phase and also the active level for each one.

The Quadrature Decoder Mode can also receive the clock and direction signals directly from an external source.

The Multi-Channel offers a shadow register, for the Multi-Channel pattern, enabling this way an update on the fly of these parameter. A write access always addresses the shadow register while a read, always returns the actual value of the Multi-Channel pattern.

Table 268 POSIF slice pin description

Pin	I/O	Hall Sensor Mode	Quadrature Decoder Mode	Multi-Channel Mode (stand-alone)
POSIFx.IN0[D...A]	I	Hall Input 1	Encoder Phase A or Clock	Not used
POSIFx.IN1[D...A]	I	Hall Input 2	Encoder Phase B or Direction	Not used
POSIFx.IN2[D...A]	I	Hall Input 3	Index/Zero marker	Not used
POSIFx.HSD[B...A]	I	Hall pattern sample delay	Not used	Not used
POSIFx.EWHE[D...A]	I	Wrong hall event emulation	Not used	Wrong hall event emulation
POSIFx.MSET[H...A]	I	Multi-Channel next pattern update set	Not used	Multi-Channel next pattern update set
POSIFx.MSYNC[D...A]	I	Multi-Channel pattern update synchronization	Not used	Multi-Channel pattern update synchronization
POSIFx.OUT0	O	Hall inputs edge detection trigger	Quadrature clock	Not used
POSIFx.OUT1	O	Hall Correct event	Direction	Not used
POSIFx.OUT2	O	Idle/ wrong hall event	Period clock	Not used
POSIFx.OUT3	O	Stop	Clear/capt	Not used
POSIFx.OUT4	O	Multi-Channel pattern update	Index	Not used
POSIFx.OUT5	O	Sync start	Sync start	Not used

Table 268 POSIF slice pin description (continued)

Pin	I/O	Hall Sensor Mode	Quadrature Decoder Mode	Multi-Channel Mode (stand-alone)
POSIFx.OUT6	O	Multi Pattern sync trigger	Not used	Multi Pattern sync trigger
POSIFx.MOUT[15:0]	O	Multi-Channel pattern	Not used	Multi-Channel pattern
POSIFx.SR0	O	Service request line 0	Service request line 0	Service request line 0
POSIFx.SR1	O	Service request line 1	Service request line 1	Service request line 1

Note: The Service Request signals at the output of the kernel are extended for one more kernel clock cycle.

21.2.2 Function Selector

The Function selector maps the input function signals to the selected operating mode, whether Quadrature or Hall Sensor Mode, ***Figure 238***. The outputs are also decoded throughout this unit.

For each function input, POSI0, POSI1 and POSI2, the user can select one of the 4 input pins via the fields ***PCONF***.INSEL0, ***PCONF***.INSEL1 and ***PCONF***.INSEL2. It is also possible to perform a low pass filtering on the three inputs, the field ***PCONF***.LPC controls the low pass filters cut frequency.

The Hall Sensor Mode is the default function, ***PCONF***.FSEL = 00_B. In this mode, the Function selector maps the POSI0 to the Hall Input 1, the POSI1 to the Hall input 2 and the POSI2 to the Hall input 3.

When the Quadrature Decoder mode is selected, ***PCONF***.FSEL = 01_B, POSI0 is mapped to Phase A or Clock, POSI1 to the Phase B or Direction and POSI2 to the Index signals coming from the rotary motor encoder. Notice that it is also possible to select the Quadrature Decoder and stand-alone Multi-Channel mode, by setting ***PCONF***.FSEL = 11_B.

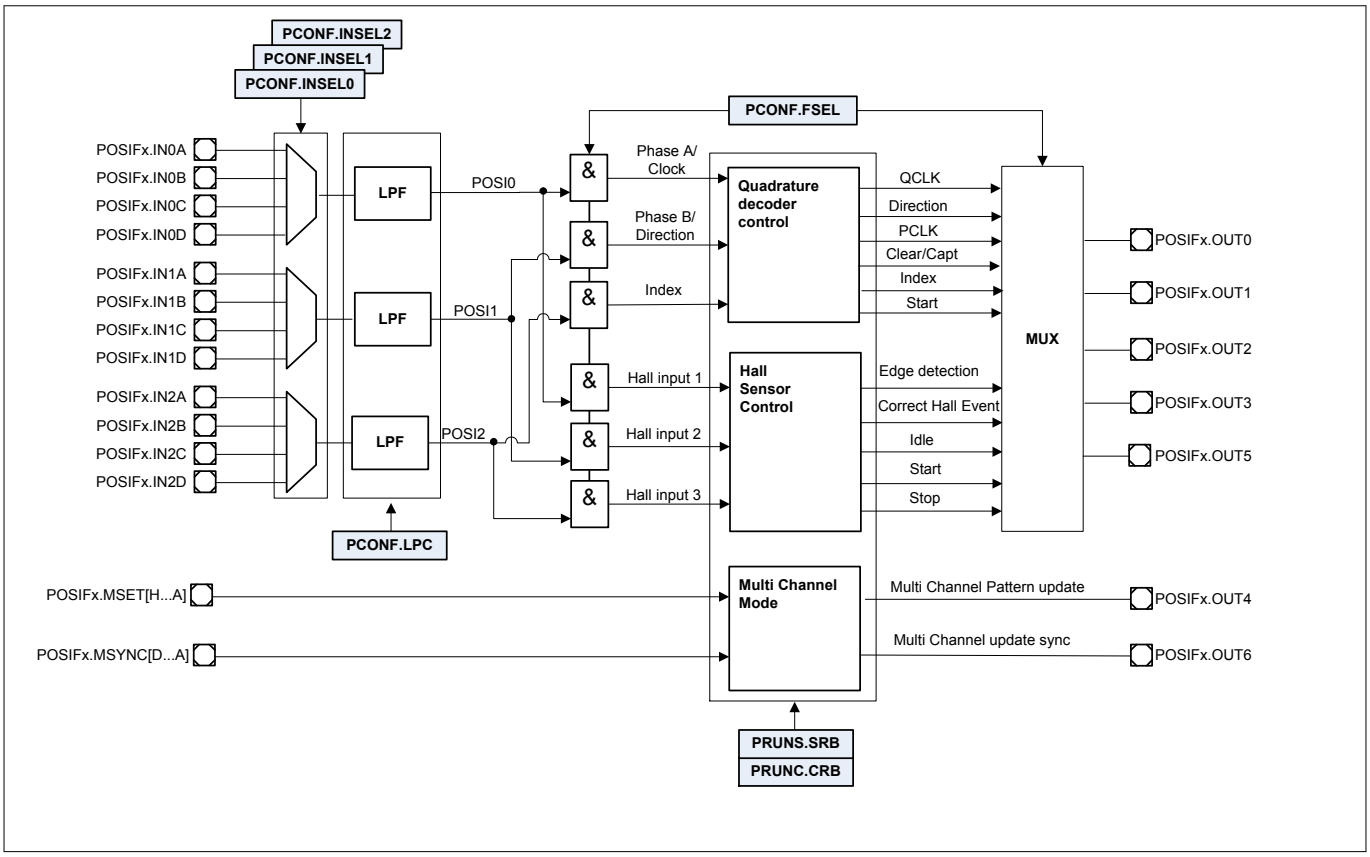


Figure 238 Function selector diagram

21.2.3 Hall Sensor Control

The Hall Sensor mode is divided in three major loops: detection of any update in the Hall inputs, delay between the detection and the sampling of the Hall inputs for comparison against the expected Hall Pattern and the update of the Multi-Channel pattern.

The Hall inputs are directly connected to an edge detection circuitry and with any modification in any of these three inputs, a signal is generated on the POSIFx.OUT0 pin, see ***Figure 239***. This pin can be connected to one CCU4 slice that is controlling the delay between the edge detection and the next step on the Hall sensor mode, the sampling of the Hall Inputs.

The signal used to trigger the sample of the Hall inputs is selected via the ***PCONF***.DSEL field, and this trigger can be active at the rising or falling edge (***PCONF***.SPES).

When the sampling trigger is sensed, the Hall inputs are sampled and compared against the Current Pattern, ***HALP***.HCP and the Expected Hall Pattern, ***HALP***.HEP (to evaluate if the input pattern match the HEP or HCP values).

The edge detection circuit generates an enable signal for sampling the hall inputs, PIFHSP and the sample logic generates a pulse every time that new values are captured, PIFHRDY, that is used inside the pattern compare logic.

When the sampled value matches the Expected Hall Pattern, a pulse is generated in the POSIFx.OUT1 pin to indicate a correct hall event. At the same time the next values programmed into the shadow registers are loaded. The ***HALP***.HCP[LSB] is linked to the Hall input 1, and the ***HALP***.HCP[MSB] is linked to the Hall input 3 (the same is applicable for the ***HALP***.HEP register).

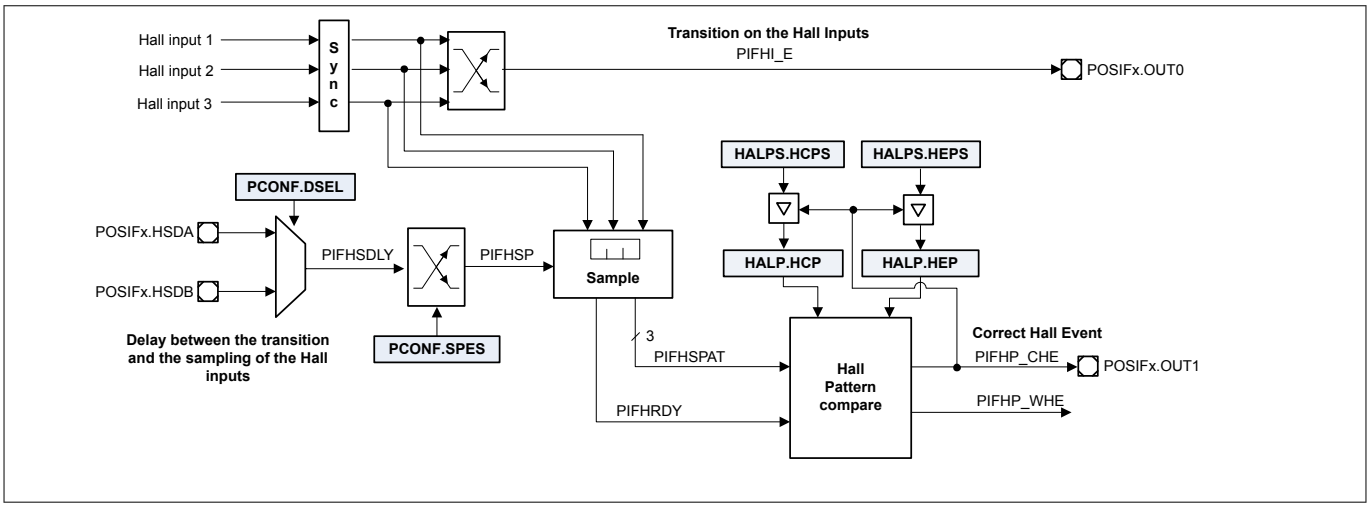


Figure 239 Hall Sensor Control Diagram

When the sampled value matches the Current Hall Pattern, a line glitch deemed to have occurred and no action is taken. When the sampled value does not match any of the values (the current and the expected pattern), a major error is deemed to have occurred and the Wrong Hall Event signal is generated. Every time that a sampled pattern leads to a wrong hall event or when it matches the current pattern a stop signal is generated throughout the POSIFx.OUT3 pin, ***Figure 240***.

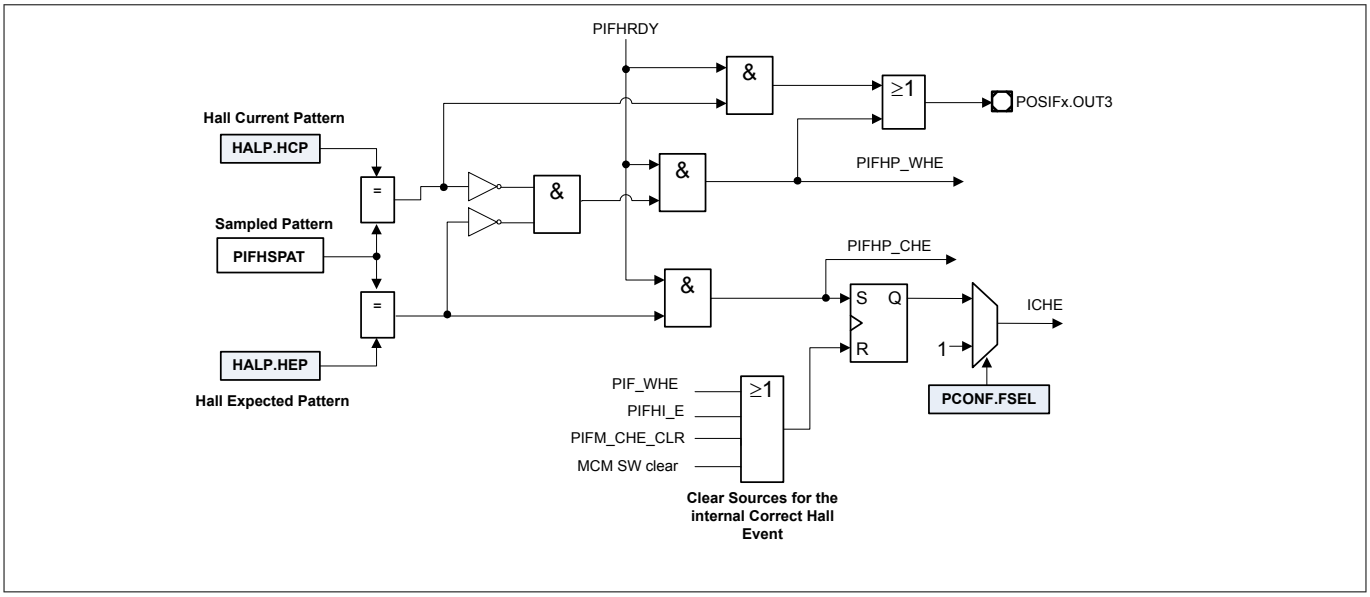


Figure 240 Hall Sensor Compare logic

A wrong hall event can generate an IDLE signal that is connected to the POSIFx.OUT2 and can be used to clear the run bit of the Hall Sensor Control unit.

The IDLE signal can also be connected to the PWM unit to perform a forced stop operation,***Figure 241*** . The wrong hall event/idle function can also be controlled via a pin.

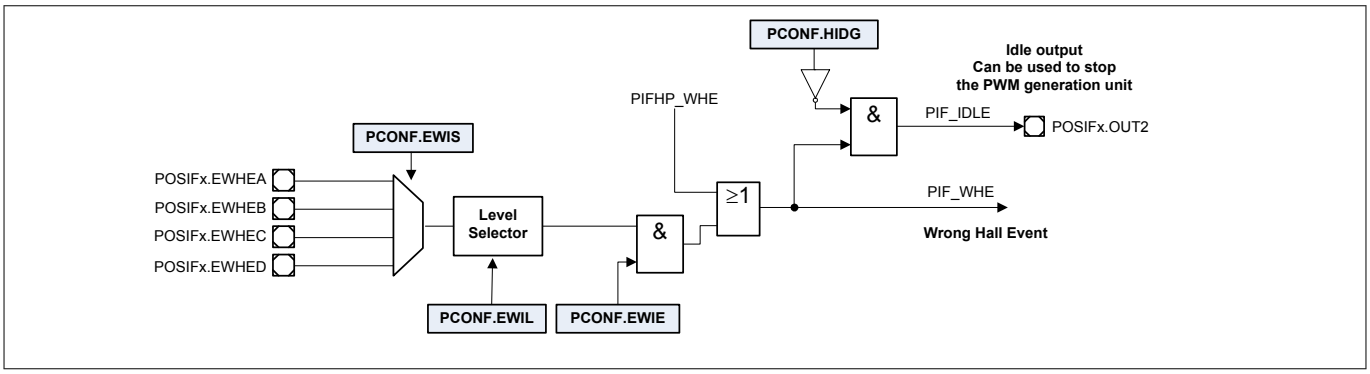


Figure 241 Wrong Hall Event/Idle logic

After the Correct Hall Event is detected, a delay can be generated between this detection and the update of the Multi-Channel pattern. On ***Figure 242*** it is demonstrated the control logic of the Multi-Channel mode.

The delay for the update of the Multi-Channel pattern can be controlled directly by a CCU4 slice. The trigger that indicates that the delay is finished, can be mapped to one of the input signals POSIFx.MSET[H...A] (***PCONF***.MSETS selects the input signal used for this purpose). One can also select the active edge for the trigger via ***PCONF***.MSES.

The ***PCONF***.MCUE field selects the source that enables an update of the Multi-Channel pattern. When set to 1_B, the Multi-Channel pattern can only be updated after the SW has written a 1_B into the ***MCMS***.MNPS field.

After the update delay, the Multi-Channel pattern still needs to be synchronized with the PWM signal. For this, the user selects a signal from the POSIFx.MSYNC[D...A] inputs via ***PCONF***.MSYNS field. When a falling edge is detected in this signal, then the new multi pattern is applied at the POSIFx.MOUT[15:0] outputs, with the ***MCM***.MCMP[15] linked to the POSIFx.MOUT[15] and ***MCM***.MCMP[0] to POSIFx.MOUT[0].

The POSIFxOUT6 pin is connected to the ***MCMF***.MSS register field. This register field is enabling the Multi-Channel pattern update (that is done upon receiving the sync signal, PIFMSYNC) and can be used in conjunction with a CAPCOM module to perform a synchronous update of the Multi-Channel pattern and the compare values used inside of the CAPCOM.

When a wrong hall event is configured to set the Hall Sensor Control into IDLE, the Multi-Channel pattern is also cleared.

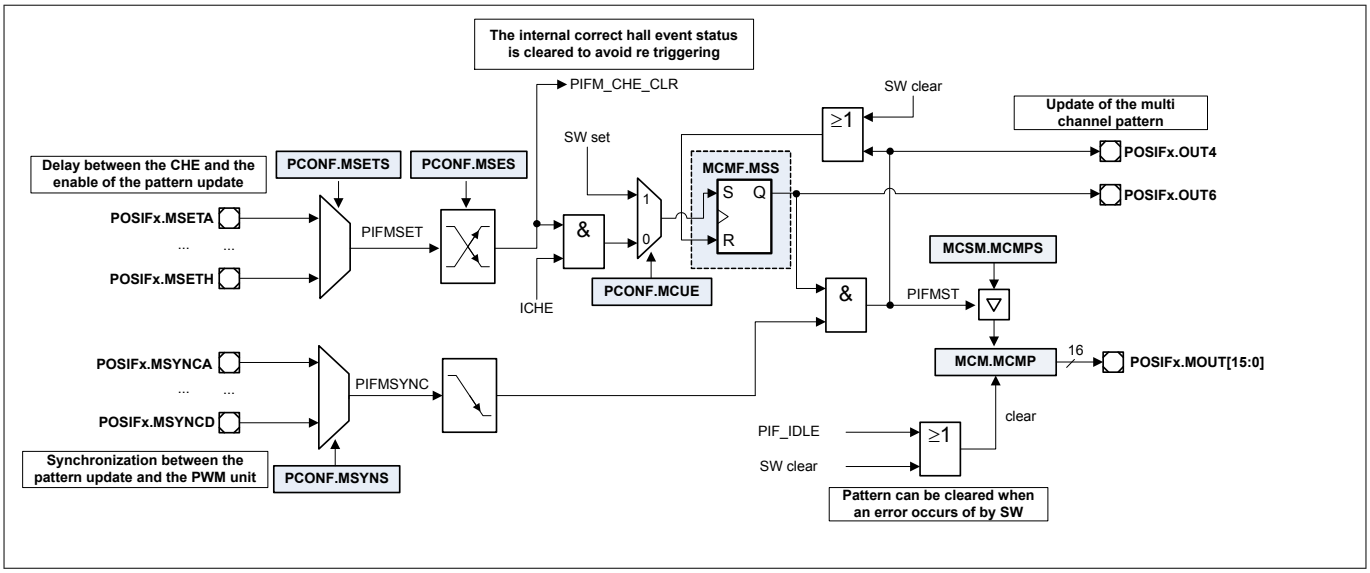


Figure 242 Multi-Channel Mode Diagram

Figure 243 shows all the previous described steps in the Hall Sensor Mode. Every time that a transition on a Hall input is detected, the pin POSIFx.OUT0 is asserted. This signal is used to start the timing delay between the transition detection and the sampling of the hall inputs.

In this scenario the status output (ST in ***Figure 243***) of a timer cell was used to control the timing 1 (delay between the transition and the sampling of the hall inputs). With the rising edge of the ST signal, the hall inputs are sampled and if they match the expected pattern, signal POSIFx.OUT1 is asserted.

A service request line (SR signal) mapped to the same timer cell is used to control the delay between a correct Hall Event and the update of the Multi-Channel pattern. This service request is asserted when a period match is detected.

Another timer cell is used to measure the time between each correct hall event. This timer cell is represented by the Timing 2 on ***Figure 243*** (the CR symbolizes the capture register of the timer cell).

After the delay controlled by the Timing 1 (SR signal) is over, the update of the Multi-Channel pattern needs to be synchronized with the PWM signal. This is done by using one of the pattern synchronization outputs of the Capture/Compare Unit that is used to generate the PWM signals (as an example a CCU8 was used).

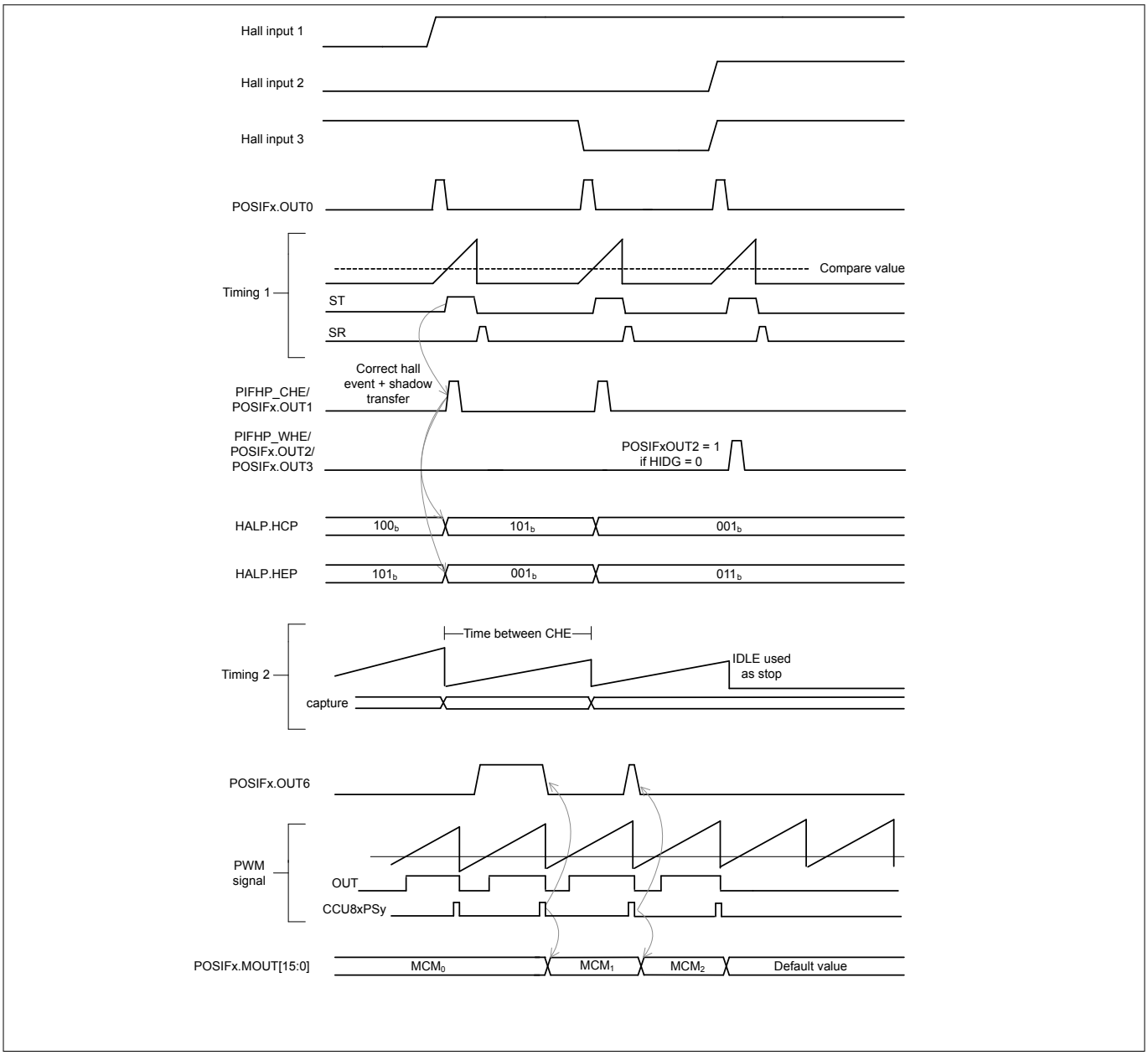


Figure 243 Hall Sensor timing diagram

21.2.4 Quadrature Decoder Control

The Quadrature Decoder Mode is selected by setting ***PCONF***.FSEL = 01_B or ***PCONF***.FSEL = 11_B (in this case the Multi-Channel mode is also enabled).

Inside the Quadrature Decoder Mode, two different subsets are available:

- standard Quadrature Mode
- Direction Count Mode

The standard mode is used when the external rotary encoder provides two phase signals and additionally and index/marker signal that is generated once per shaft revolution. The Direction Count Mode is used when the external encoder only provides a clock and a direction signal, ***Figure 244***.

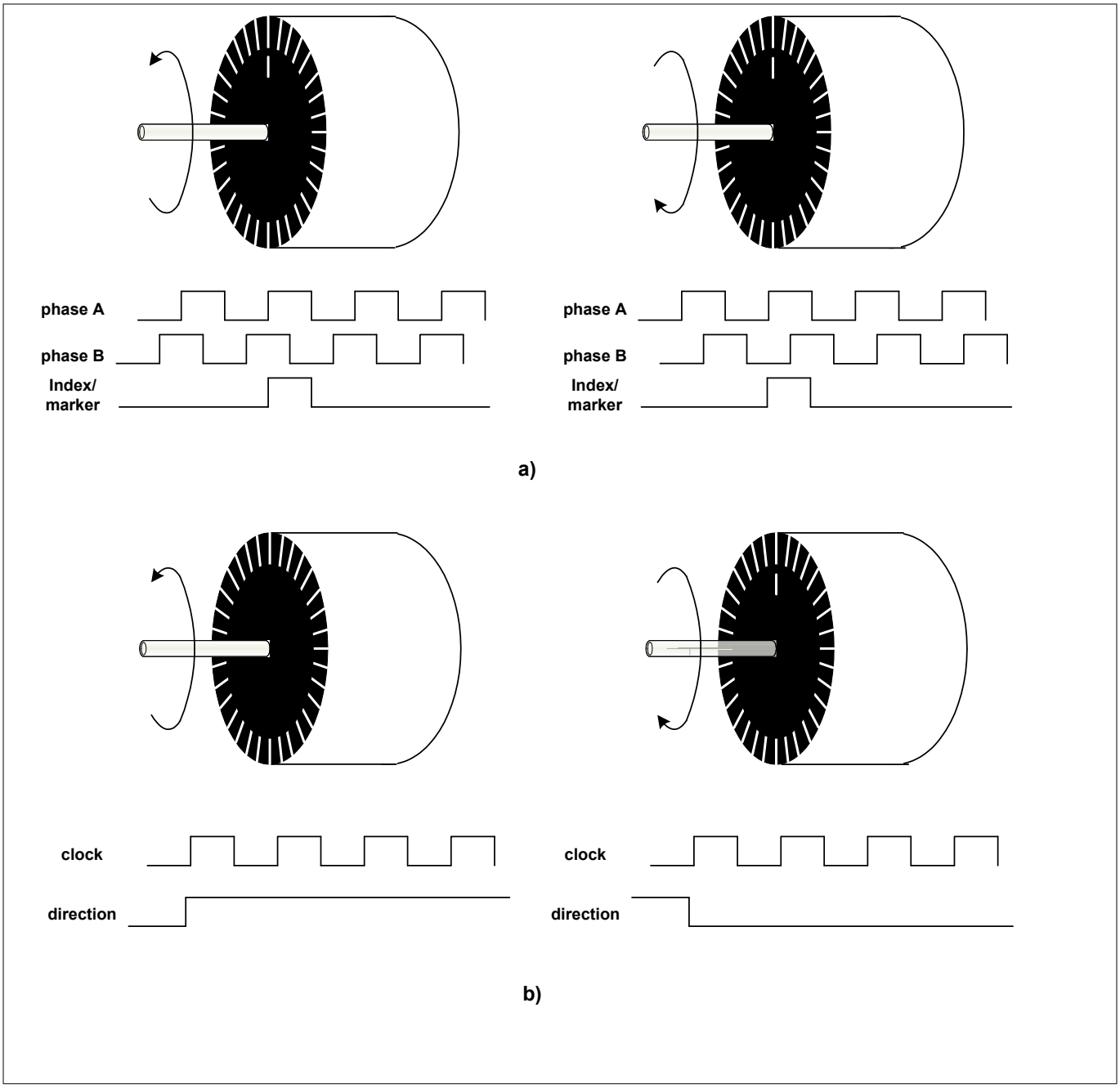


Figure 244 Rotary encoder types - a) standard two phase plus index signal; b) clock plus direction

Standard Quadrature Mode

The Quadrature Decoder unit offers a very flexible PhaseA/PhaseB configuration stage. Normally for a clockwise motor shaft rotation, Phase A should precede Phase B but nevertheless, the user can configure the leading phase as well the specific active state for each signal, ***Figure 245***.

There are two major blocks that build the Quadrature Decoder Control unit: the block that decodes the quadrature clock and motor shaft direction and the block that handles the index (motor revolution) control.

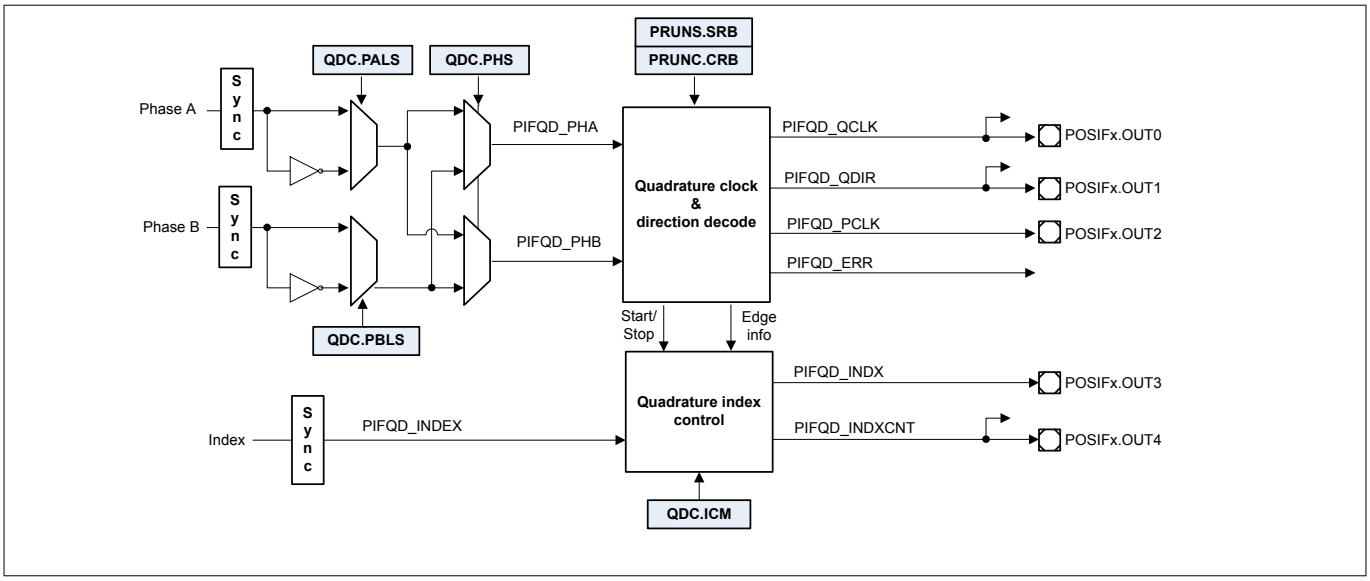


Figure 245 Quadrature Decoder Control Overview

The quadrature clock is connected to pin POSIFx.OUT0 and is used for position measurement. This clock is decoded from every edge of the phase signals and therefore there are 4 clock pulses per phase period.

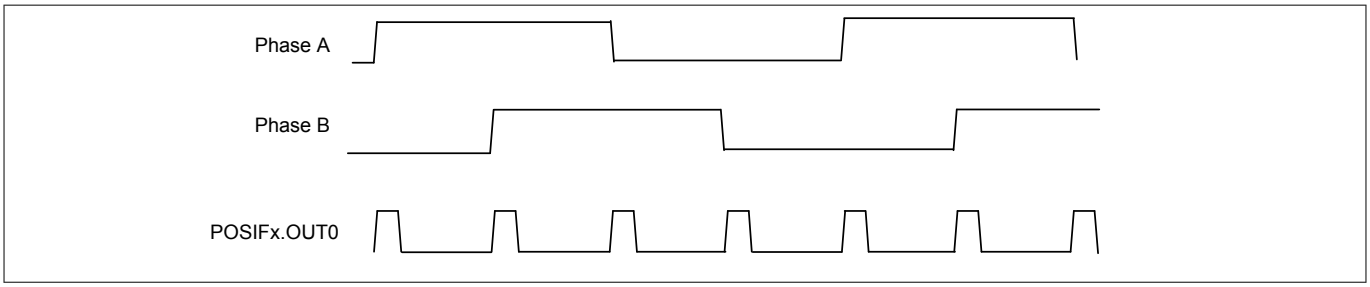


Figure 246 Quadrature clock generation

A period clock is also generated for velocity measurement operations.

The direction of the motor rotation is connected to the POSIFx.OUT1 pin and is asserted HIGH when the motor is rotating clockwise and LOW when it is turning in the counterclockwise direction.

The index control logic, memorizes which was the first edge after the assertion of the index signal, so the same quadrature transition is used for index event operations. It also memorizes the direction of the first index, so that it can control when the revolution increment signal should be asserted.

An error signal, connected to a flag (and if enable an interrupt can be generated) also can be generated when a wrong phase pair is detected.

The Quadrature Decoder Control, uses the information of the current and previous phase pair to decode the direction and clocks. Both phase signals pass through a edge detection logic, from which the outputs are going to be used against the valid/invalid transitions stages, see ***Figure 247***. There is the possibility to reset the decoder state machine (but not the flags and static configuration) by writing a 1_B into the ***PRUNC***.CSM field.

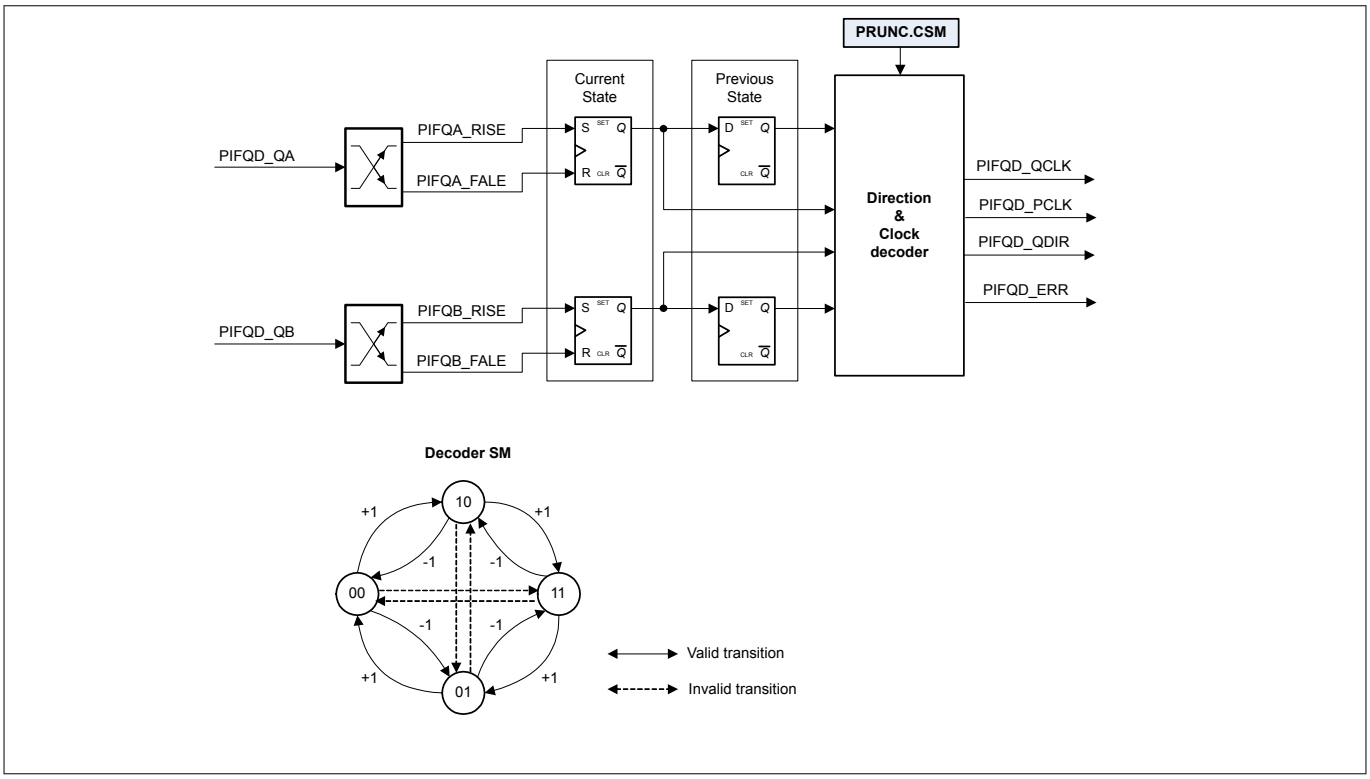


Figure 247 Quadrature Decoder States

Direction Count Mode

Some position encoders do not have the phase signals as outputs, instead, they provide two signals that contain the clock and direction information. This is know as the Direct Count Mode.

When using a position encoder of this type, the user should set the ***PCONF***.QDCM bit field to 1_B (enabling the direction count mode). In this case, the signal selected from the POSIFx.IN0[D...A] is used as clock and the selected signal from the POSIFx.IN1[D...A] contains the direction information.

The input signals are synchronized with the POSIF module clock and sent to the respective outputs. In this case the inputs and outputs linked with the index/zero marker are not used. The POSIFx.OUT2 output is also inactive.

21.2.4.1 Quadrature Clock and Direction decoding

The Quadrature Decoder unit outputs two clocks. One clock is used for position control and therefore is generated in each edge transition of the phase signals. The second clock is used for velocity measurements and is immune to possible glitches on the phase signals that can be present at very slow rotation speeds. These glitches are not normal line noise, but are due to the slow movement of the engine.

The decoding of the direction signal is done following the rules on ***Figure 247***. ***Figure 248*** shows all the valid transitions of Phase A and Phase B signals.

Figure 249 shows the difference between the two clock signals in the case that some glitches are present in the phase signals.

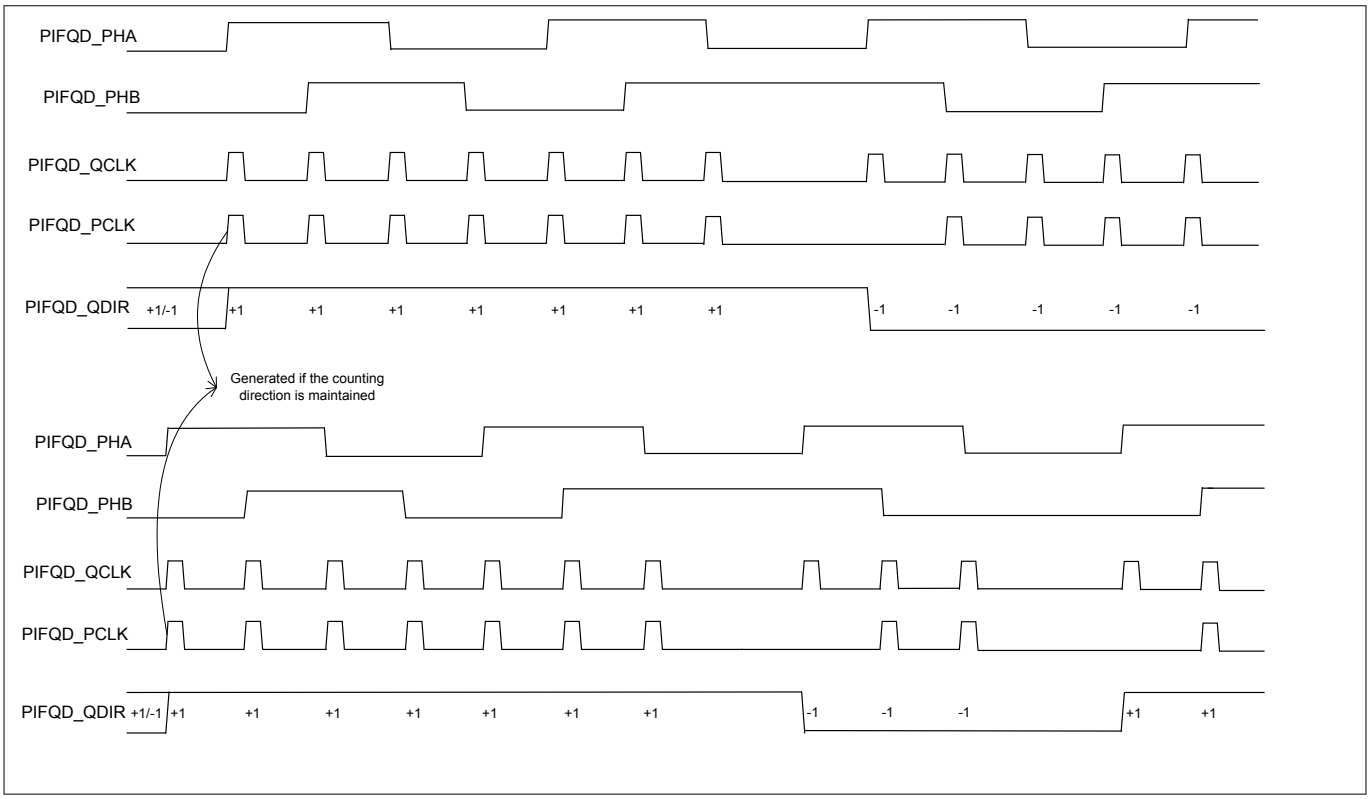


Figure 248 Quadrature clock and direction timings

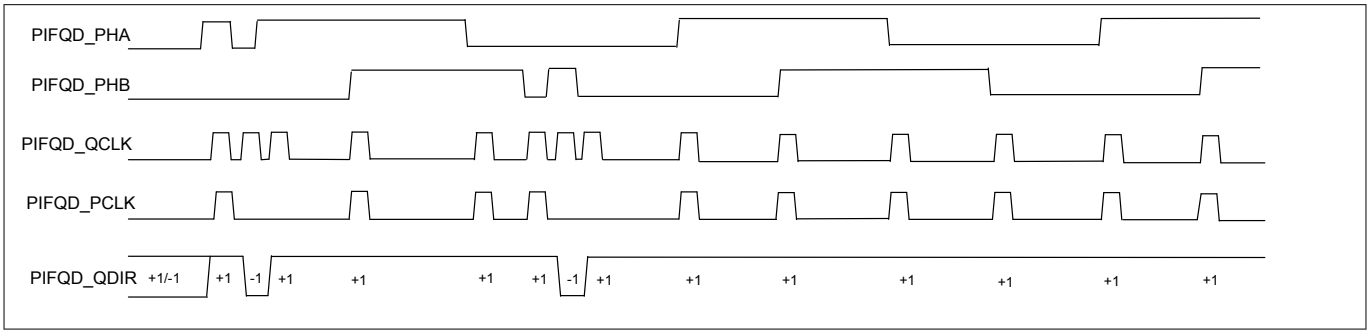


Figure 249 Quadrature clock with jitter

21.2.4.2 Index Control

The Index Control logic has two different outputs. One is asserted every time that an index signal is detected (and the motor shaft rotation is the same), POSIFx.OUT4, and therefore it can be used in a revolution counter. With this, the SW can monitor not only the position of the shaft but also the total number of revolutions that have occurred.

The activity of the other output, POSIFx.OUT3, can be programmed via the ***QDC***.ICM field. Depending on the value set in the ***QDC***.ICM, this signal can be generated:

- in every index signal occurrence
- only on the first index signal occurrence
- disabled - this outputs is never asserted

This is useful for applications that need to reset the counters on every index event or only at the first one.

The Index Control logic memorizes the immediately next phase edge that follows a index so the generated signals have always the same reference. If the first phase edge after the index is the rising edge of Phase B

signal, then the index signals are going to be generated in the next index event with the rising edge of the Phase B signal if the direction is kept or with the falling edge of Phase B signal if the direction has changed.

Figure 250 shows the timing diagram for the generation of the index signals. In this case the ***QDC***.ICM = 10_B, which means that the POSIFx.OUT3 index signal is going to be generated in every occurrence of the input index.

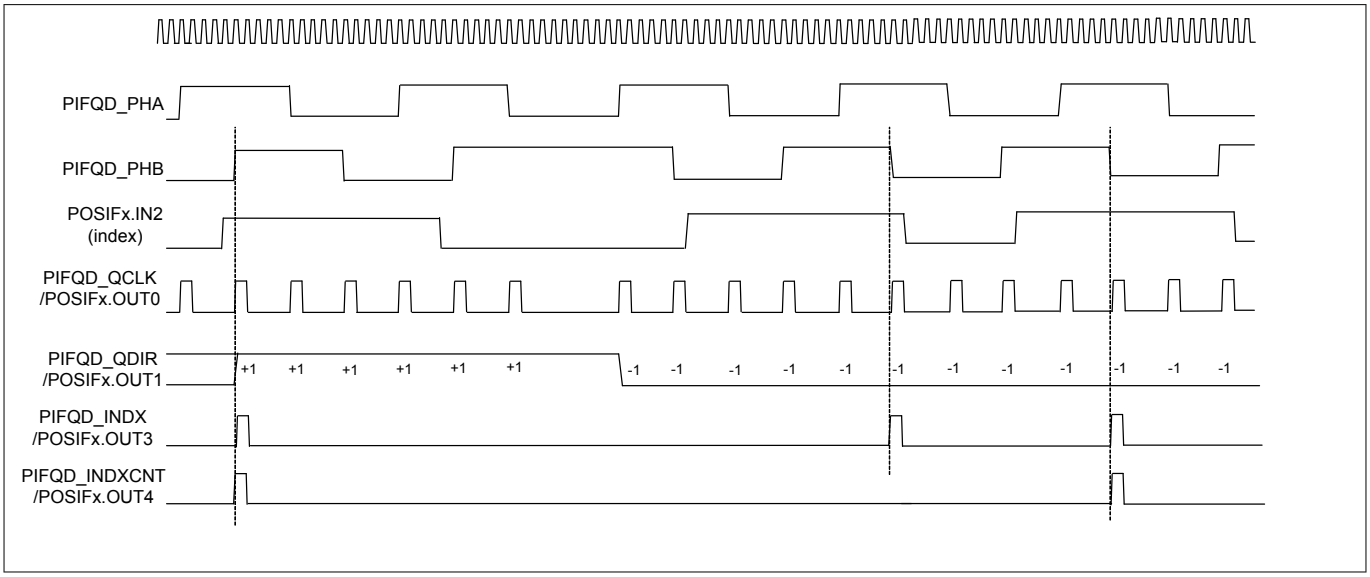


Figure 250 Index signals timing

21.2.5 Stand-Alone Multi-Channel Mode

The Multi-Channel mode (Multi-Channel Mode logic can be see on ***Figure 242***) can be used without the Hall Sensor Control, by setting the ***PCONF***.FSEL = 10_B or if the Quadrature Decoder Mode is also needed, by setting ***PCONF***.FSEL = 11_B.

In stand-alone Multi-Channel Mode, the mechanism to update the multi-channel pattern is the same as the one described in ***Chapter 21.2.3***.

The trigger for a pattern update can come from the SW, by writing 1_B to ***MCMS***.MNPS, or it can come from an external signal like in Hall sensor Mode. This external signal should then be mapped to the PIFMSET function by selecting the appropriate value in the ***PCONF***.MSETS field.

The synchronization between the update of the new Multi-Channel pattern and control signal still needs to be done. The user needs to map one input signal of the POSIFx.MSYNC[D...A] range to this function.

The SW has the possibility of clearing the actual Multi-Channel pattern, by writing 1 into the ***MCMC***.MPC field.

21.2.6 Synchronous Start

The POSIF module has a synchronous start output, POSIFx.OUT5, that can be used together with the CAPCOM for a complete synchronous start of both modules. The synchronous start is linked with the run bit of the POSIF module, which means that every time that the run bit is set, a pulse is generated throughout the POSIFx.OUT5 pin.

By using the synchronous start output, the SW does not perform two independent accesses to start the POSIF and the CCU4/CCU8 and therefore is guaranteed that both modules start their operation at the exact same time.

21.2.7 Using the POSIF

The POSIF module needs to be linked with a CCU4/CCU8 module to perform the full set of functions in each of the possible modes (due to the fact that doesn’t contain built-in counters/timers).

To operate the POSIF in the Quadrature Decoder Mode, one CCU4 module is needed. The Hall Sensor Mode, needs a CCU8 (at least 3 slices are need to control a brushless DC motor) and also (at least) two CCU4 or CCU8 slices. The stand-alone Multi-Channel Mode linking configuration depends heavily on the use cases and therefore the number of slices of CCU4 or CCU8 used is freely chosen by the user.

21.2.7.1 Hall Sensor Mode Usage

When using the Hall Sensor Mode of the POSIF, the Multi-Channel Mode is also working. Due to that fact, the CCU8 module used to perform the Multi-Channel Modulation, needs to be configured in Multi-Channel Mode.

Standard Hall Sensor Mode Usage

On ***Figure 251***, the Hall Sensor Mode is used in conjunction with two CCU4 slices and one CCU8 module. The first slice of CCU4, slice 0 is being used to control the delays between the edge detection of the Hall Inputs and the actual sampling, and also to control the delay between a Correct Hall Event and the Multi-Channel Pattern update enable.

The rising edge of the CCU4x.ST0 is used as finish trigger for the first delay, while the Service request line is used for triggering the update of a new pattern after a Correct Hall Event. The service request is configured to be active on each period match hit of the specific slice.

Slice 0 is configured in single shot mode, so that the time delay can be re triggered every time that a request from the POSIF occurs.

The second slice of the CCU4 unit, Slice 1, is being used in Capture Mode, to capture the time between Correct Hall Events (storing this way the motor speed between two correct hall events). The POSIFx.OUT1 of the POSIF is used as capture trigger for the slice while the POSIFx.OUT3 is used as stop. The capture and stop triggers are configured in the specific timer slices as active on the rising edge.

The CCU8 is the module that is generating the PWM signals to control the motor and therefore, the Multi-Channel Pattern outputs POSIFx.MOUT[7:0] are linked to this unit.

To close the Multi-Channel loop, an output of the CCU8 needs to be connected to the POSIF module (one of the CCU8x.PSy signals), so that the Multi-Channel Pattern is updated synchronously with the PWM period.

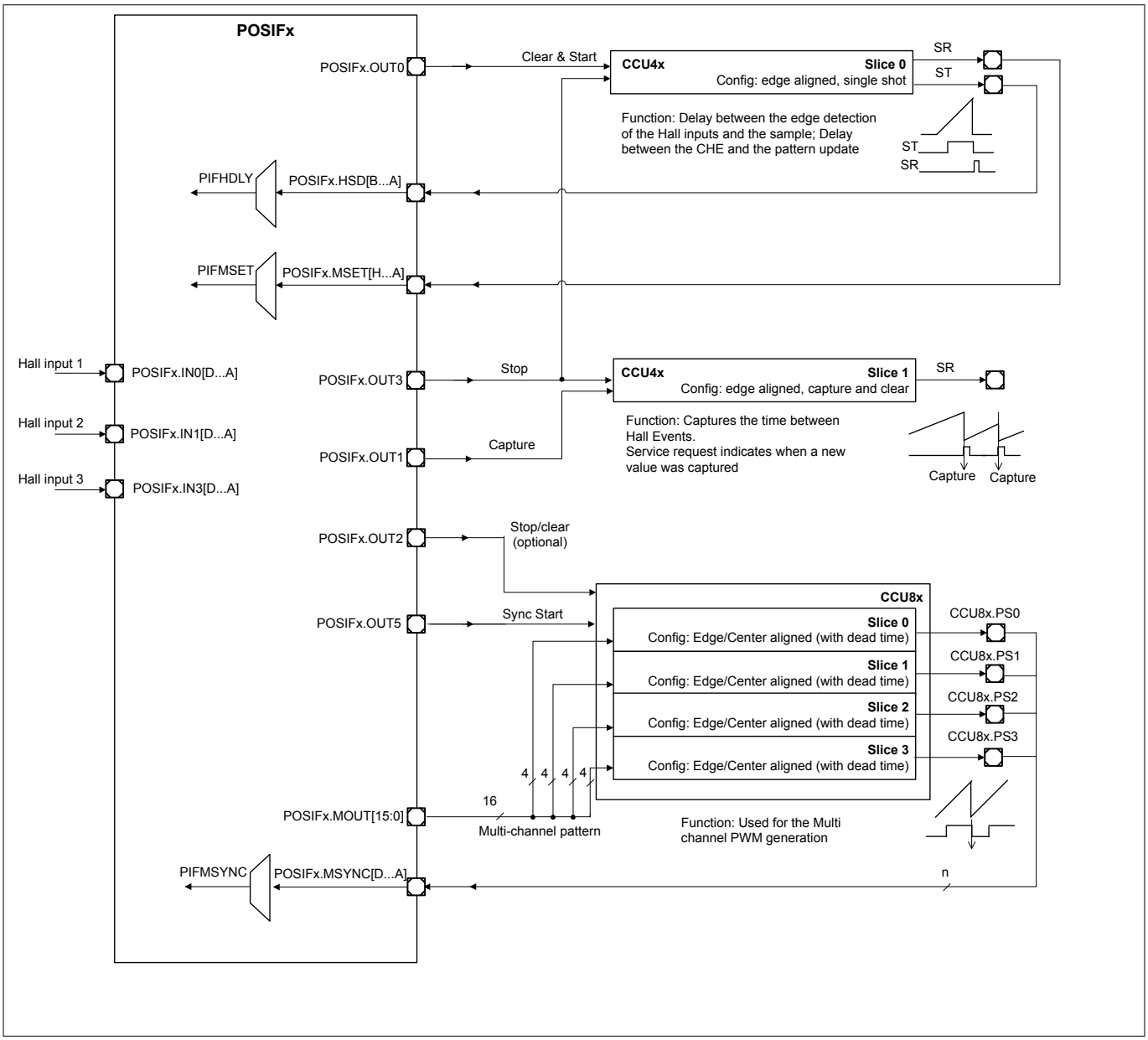


Figure 251 Hall Sensor Mode usage - profile 1

Hall Sensor Mode Usage - Flexible Time Control

On ***Figure 252***, another profile is demonstrated. In this case instead of 2 CCU4 slices, the Hall Sensor Mode is using 3 CCU4 slices. This profile gives more flexibility in terms of delay configuration. It uses two timer slices to control independently the delay between the transition of the hall inputs and sampling, and the delay between a Correct Hall Event and the update of the Multi-Channel pattern. At the same time it also removes the need of using a service request to control the pattern update delay.

Slice 0 is used to control the delay between a transition at the hall inputs and the actual sampling. Slice 2 is used to control the delay between a Correct Hall Event and the update of the Multi-Channel pattern.

Slice 1 is used as keeper of the time stamp between Correct Hall events (the same function as Slice 1 in profile 1).

The synchronism between the PWM signal and the update of the Multi-Channel pattern is again done with one of the CCU8x.PSy outputs.

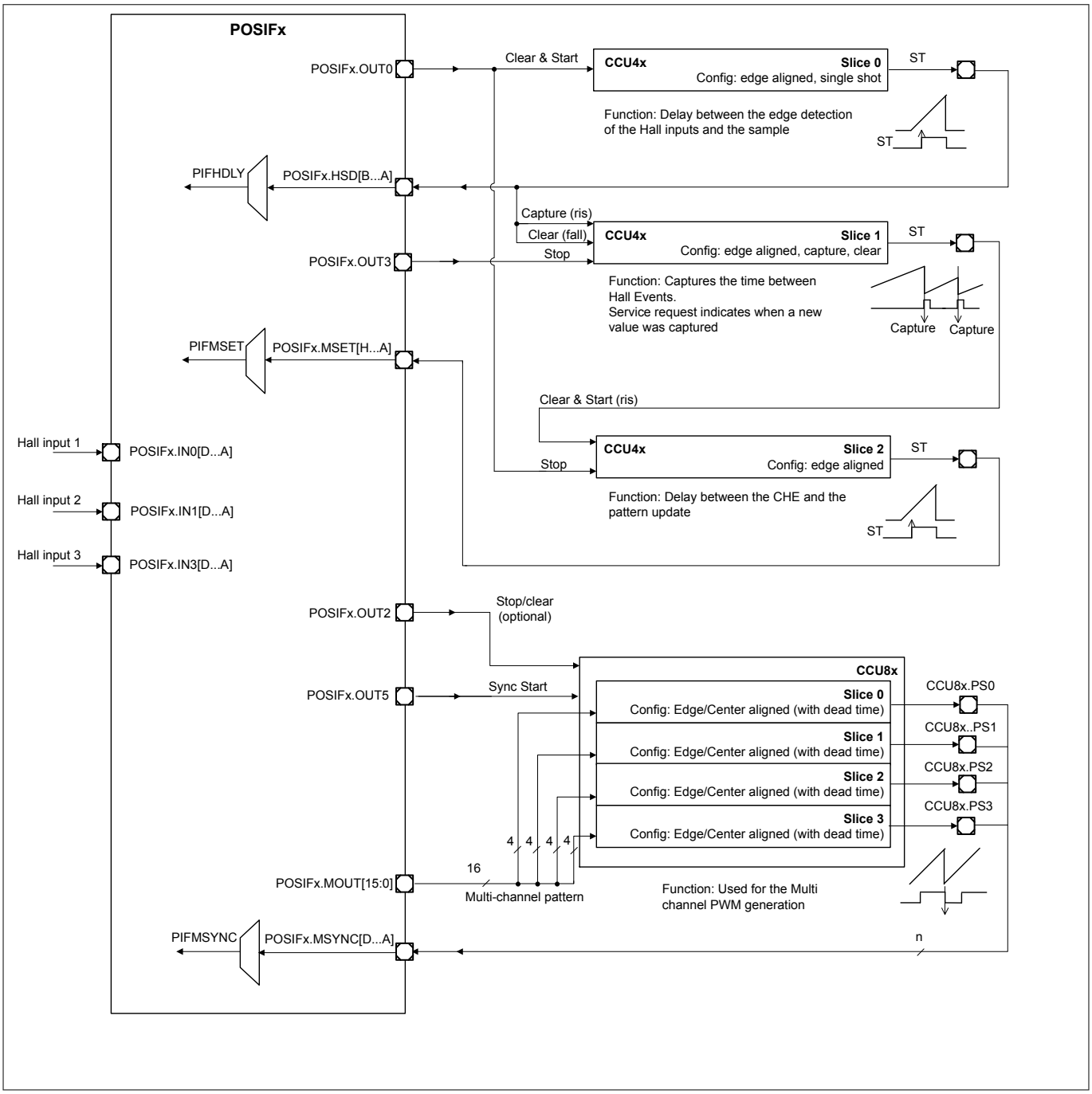


Figure 252 Hall Sensor Mode usage - profile 2

21.2.7.2 Quadrature Decoder Mode usage

The Quadrature Decoder Mode can be used in a very flexible way when connected with a CCU4 unit. The connection profile depends on the amount of functions that the user wants to perform in parallel: position control, revolution control and velocity measurement.

Quadrature Decoder Usage - Tick and Revolution Compare plus Velocity Between N Ticks

On ***Figure 253***, the POSIF is linked with a CCU4, using all the module timer slices. In this profile, the user in Quadrature Decoder Mode has a slice being used for position control (comparison), one for revolutions counter and two aggregated slices used for velocity measurement.

Slice 0 is connected to the POSIFx.OUT0 and POSIFx.OUT1 outputs, which means that one has to configure POSIFx.OUT0 as counting functionality and POSIFx.OUT1 as Up/Down counting function. This slice is then used to track the actual position of the system and the compare channel can be configured to trigger the required actions, when the position reaches a certain value.

Slice 1 is connected to POSIFx.OUT4 pin, which means that it is used as a motor revolution counter. The compare channel can be programmed to trigger an interrupt every time that the motor performs N revolutions.

Slice 2 and Slice 3 are used to perform velocity measurements. Slice 2 receives the Quadrature Decoder period clock via POSIFx.OUT2, that is mapped to a counting functionality. The compare channel of this slice is then used to trigger a capture event in Slice3. The last one is using the module clock and therefore in every capture event, the actual system ticks are captured. This way the user knows how much time has elapsed between N phase periods and can calculate the corresponding velocity profiles.

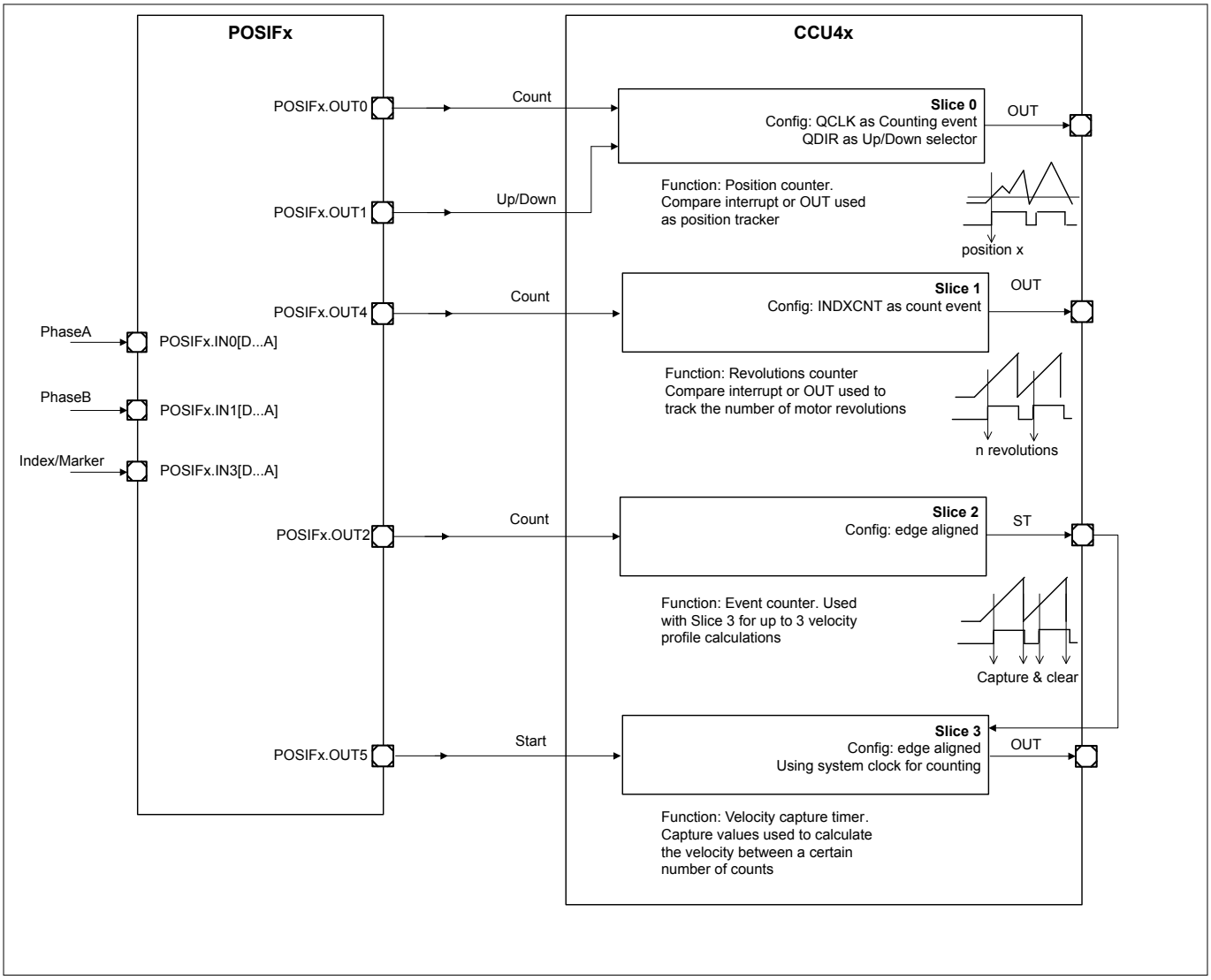


Figure 253 Quadrature Decoder Mode usage - profile 1

Quadrature Decoder Usage - Extended Tick Comparison plus Velocity Between N Ticks

The profile demonstrated in ***Figure 254*** enables the usage of 2 compare channels for the position control. This profile is especially useful for multi operations during just one motor revolution.

Slice 0 and Slice 1 are using the POSIFx.OUT0 as counting function and the POSIFxOUT1 as up/down control. The compare channels in each slice are then programmed with different compare values.

Slice 2 and Slice 3 are used in the same manner as profile 1, ***Figure 254***.

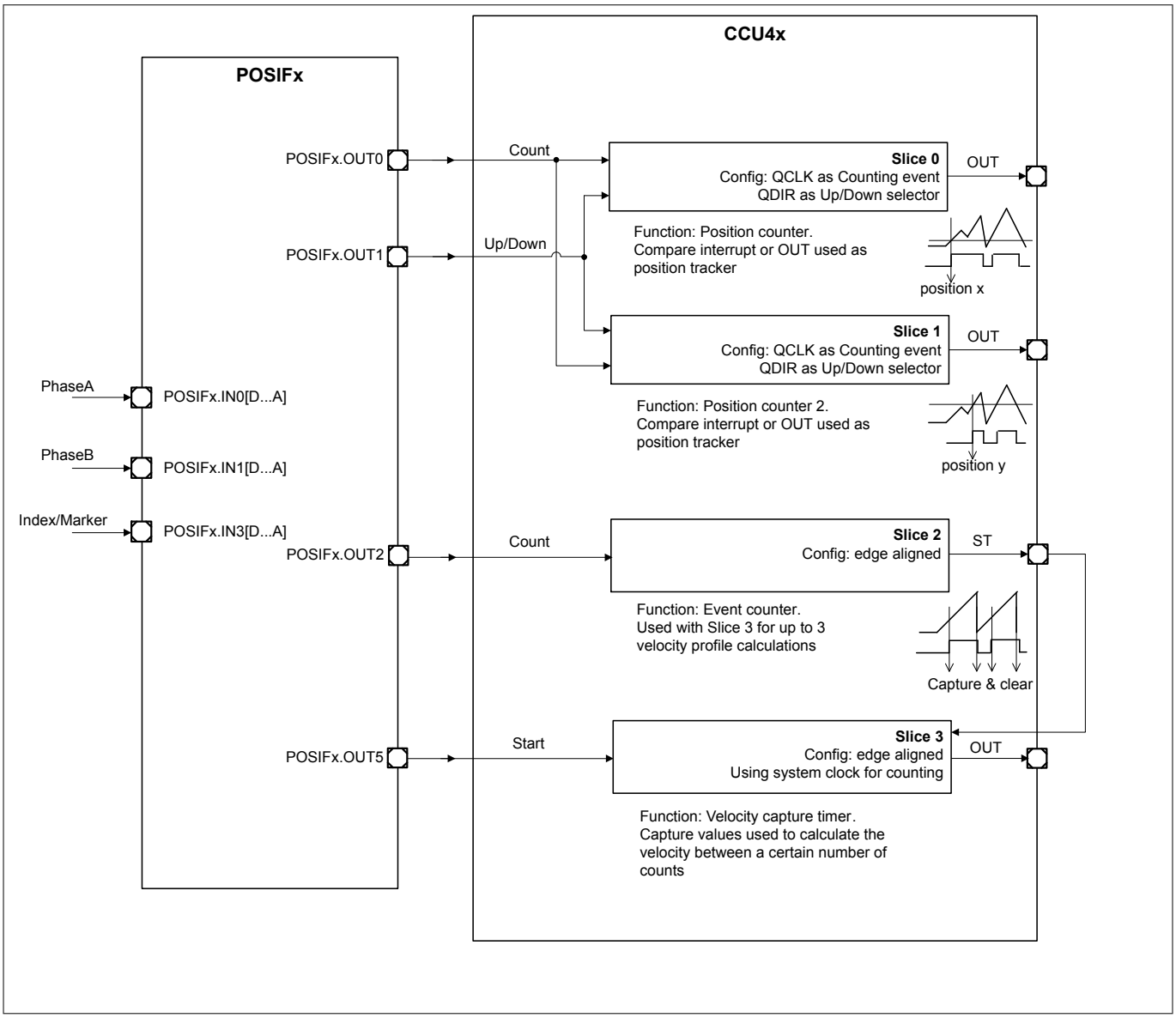


Figure 254 Quadrature Decoder Mode usage - profile 2

Quadrature Decoder Usage - Tick and Revolution Comparison with Index Clear plus Velocity Between N Ticks

In some applications it is useful to use the index marker as a clear signal for the position and velocity control. This clear action is linked with the POSIFx.OUT3 pin, that can be programmed to be asserted only at the first index marker or at all maker hits. This pin is then connected to the specific CCU4 slices and used as clear functionality. ***Figure 255*** shows the adaptation of profile 1 with the index marker signal used as clear signal.

The same procedure can be used in profile 2, so that we can have the 2 compare channels plus the velocity measurement and the index used as clear signal.

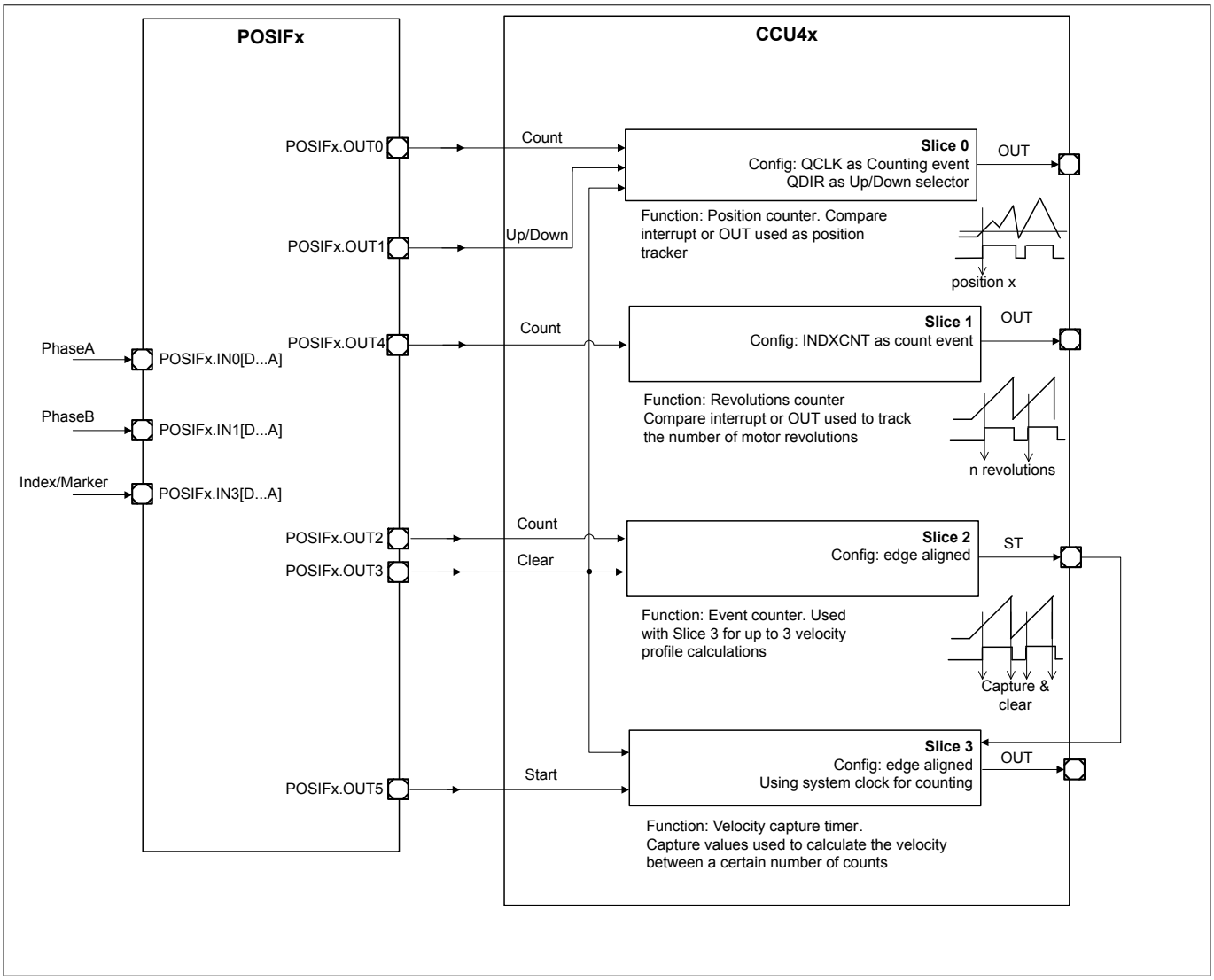


Figure 255 Quadrature Decoder Mode usage - profile 3

Quadrature Decoder Usage - Tick Comparison plus Micro Tick Velocity for Slow Rotating Speeds

When the motor rotating speed is slow, it may not be suitable to discard the time between each occurrence of a rotary encoder tick.

In a fast rotating system, the time between ticks is normally discarded and the velocity calculation can be done, by taking into account the number of ticks that have been elapsed since the last ISR. But in a slow rotating system, taking into account the number of ticks may not be enough (because of the associated error), and the software needs also to take into consideration, the time between the last tick and the actual ISR trigger.

Figure 256 shows a slow rotating system, where the ISR for the velocity calculation is triggered in a periodic way. In this case, because of the small amount of ticks between each ISR trigger, the software needs to know not only the amount of elapsed ticks but also the elapsed time between the last tick and the ISR occurrence.

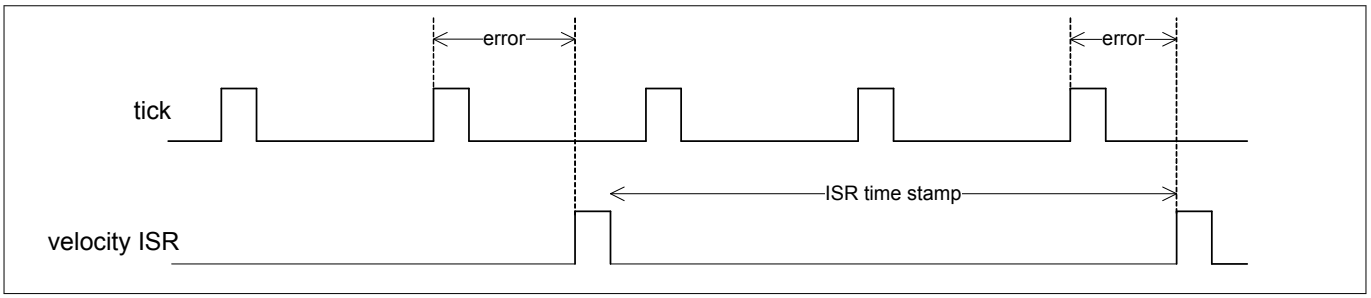


Figure 256 Slow rotating system example

It is possible to built a profile with the POSIF and one CCU4 module to perform a control loop that is immune to this slow velocity calculation pitfalls. The resource usage is exemplified on ***Figure 257***.

One timer slice of a CCU4 module, Slice 0, is used to monitor the current position of the motor shaft.

Three additional timer slices are needed to built the slow velocity calculation loop: Slice 1, Slice 2 and Slice 3.

Timer Slice 1, is counting the number of ticks (PCLK) that are elapsed between each velocity ISR occurrence.

Timer Slice 2, is counting the time between each tick (PCLK) occurrence. This timer slice is cleared and started within every tick and therefore it always keeps the timing info between the last and the current tick.

Timer Slice 3, is controlling the periodicity of the velocity ISR. Every time that a velocity ISR is triggered, Slice 3 also triggers a capture in Slice 2 and a capture & clear in Slice 1.

With this mechanism, every time that the software reads back the captured values from Slice 1 and Slice 2, it can calculate the speed based on:

- the amount of ticks elapsed since the last ISR
- plus the amount of time elapsed between the last tick and the ISR

This control loop offers therefore a very accurate way to calculate the motor speed within systems with low velocity.

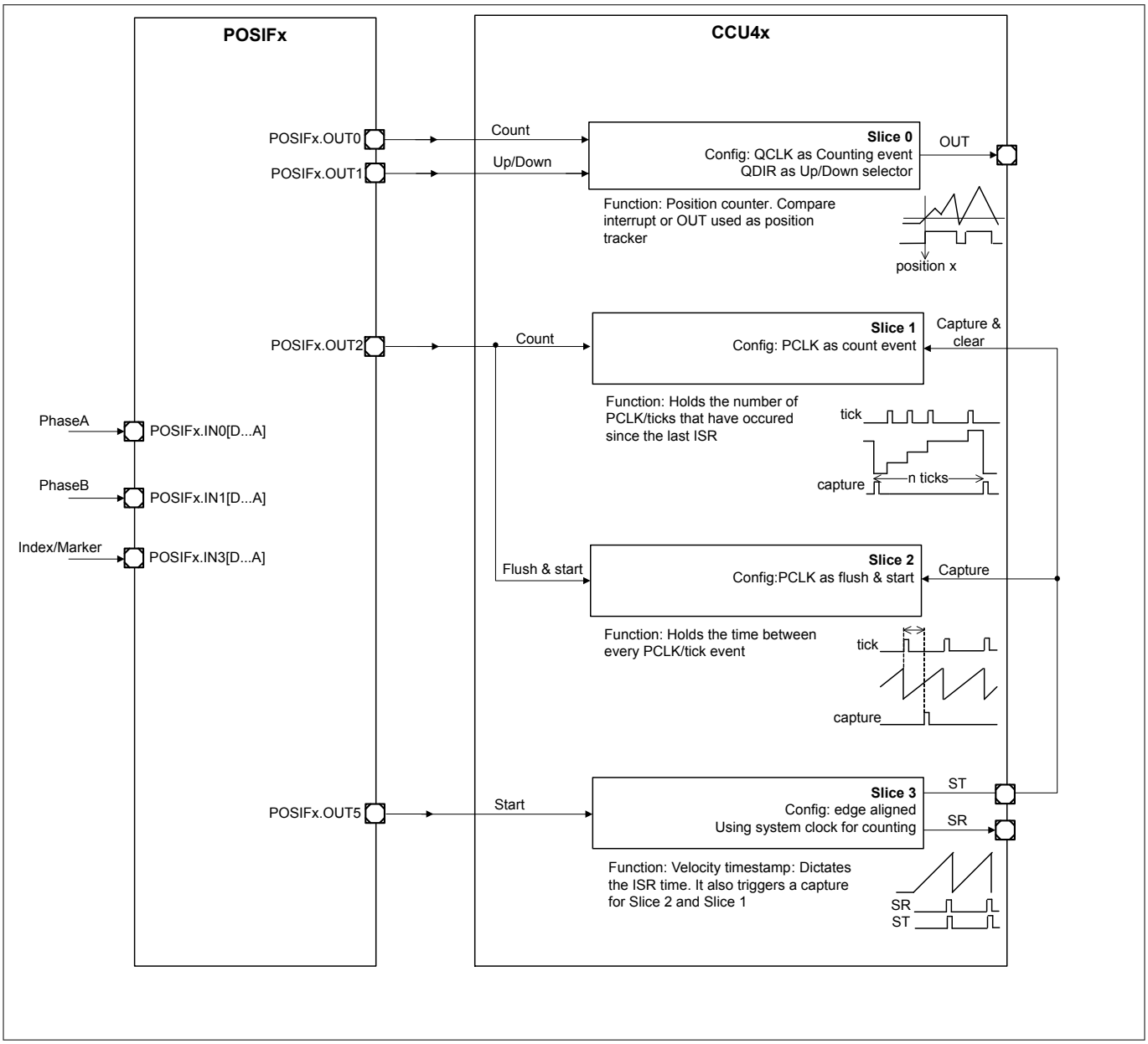


Figure 257 Quadrature Decoder Mode usage - profile 4

21.2.7.3 Stand-alone Multi-Channel Mode

The Multi-Channel Mode can be used in the POSIF module without being linked with the Hall Sensor Mode. This is especially useful for performing generic control loops that need to be perfectly synchronized.

The stand-alone Multi-Channel Mode is very generic and depends very much on the control loop specified by the user. A generic profile for the Multi-Channel mode is to use a CCU4/CCU8 module to perform the signal generation and a slice from a CCU4 module linked with an external pin that is used as trigger for updating the Multi-Channel pattern.

On ***Figure 258***, a slice from a CCU4 unit is used to control the delay between the update of an external signal (e.g. external sensor) and the update of the Multi-Channel Pattern. Notice that this external signal can also be connected to the POSIF module if no timing delay is needed or it can be just controlled by SW, by writing an one into the ***MCMS***.MNPS field.

One output can then be chosen from the CCU4/CCU8 unit that is generating the PWM signals, to act as synchronization trigger between the generated signal and the update of the Multi-Channel pattern (CCU4x.PSy in case of CCU4 and CCU8x.PSy in case of CCU8).

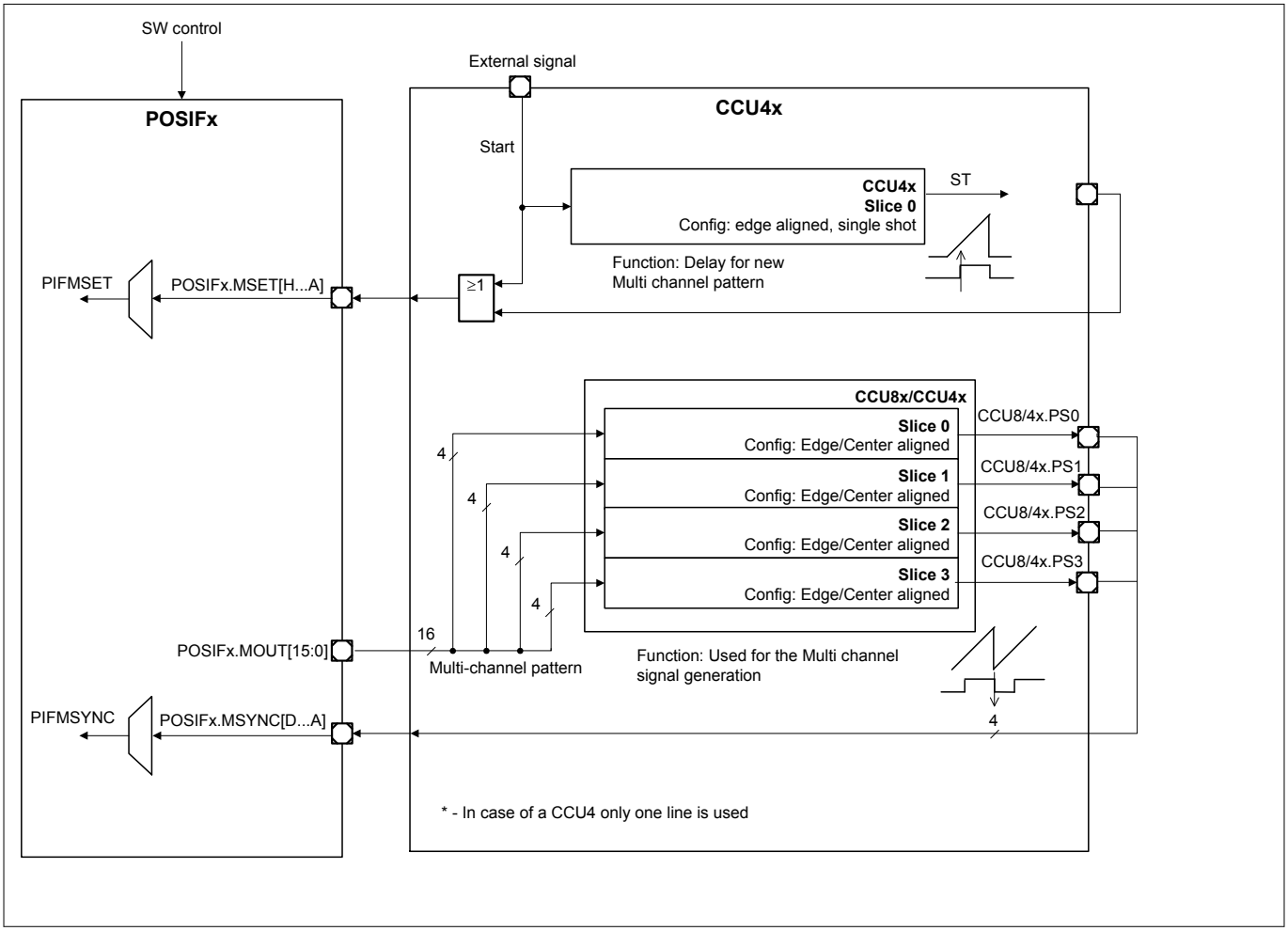


Figure 258 Stand-alone Multi-Channel Mode usage

21.3 Service Request Generation

The POSIF has several interrupt sources that are linked to the different operation modes: Hall Sensor Mode, Quadrature Decoder Mode and stand-alone Multi-Channel Mode.

The interrupt flags for the Hall Sensor Mode are described in ***Chapter 21.3.1*** while the interrupt flags of the Quadrature Decoder Mode are described in ***Chapter 21.3.2*** .

The flags associated with the Multi-Channel function are available in all the modes. This is due to the fact that the Multi-Channel Mode can operate in parallel with the Quadrature Decoder Mode and is needed whenever the Hall Sensor Mode is activated.

Each of the interrupt sources, can be routed to the POSIFx.SR0 or POSIFx.SR1 output, depending on the value programmed in the ***PFLGE*** register.

21.3.1 Hall Sensor Mode flags

The Hall Sensor Control contains four flags that can be configured to generate an interrupt request pulse, see ***Figure 259***.

The four interrupt sources are:

- Transition at the Hall Inputs (***PFLG***.HIES)
- occurrence of a correct hall event (***PFLG***.CHES)
- occurrence of a wrong hall event (***PFLG***.WHES)
- shadow transfer of the Multi-Channel pattern (***PFLG***.MSTS)

The last one is triggered every time the Multi-Channel pattern is updated (PIFMST), which means that the POSIFx.MOUT[15:0] output was updated with a new value (see also ***Figure 242***).

Each of this interrupt sources can be enabled/disabled individually. The SW also has the possibility to set and clear the specific flags by writing a 1_B into the specific fields of ***SPFLG*** and ***RPFLG*** registers. By enabling an interrupt source, an interrupt pulse is generated every time that a flag set operation occurs, independently if the flag is already set or not.

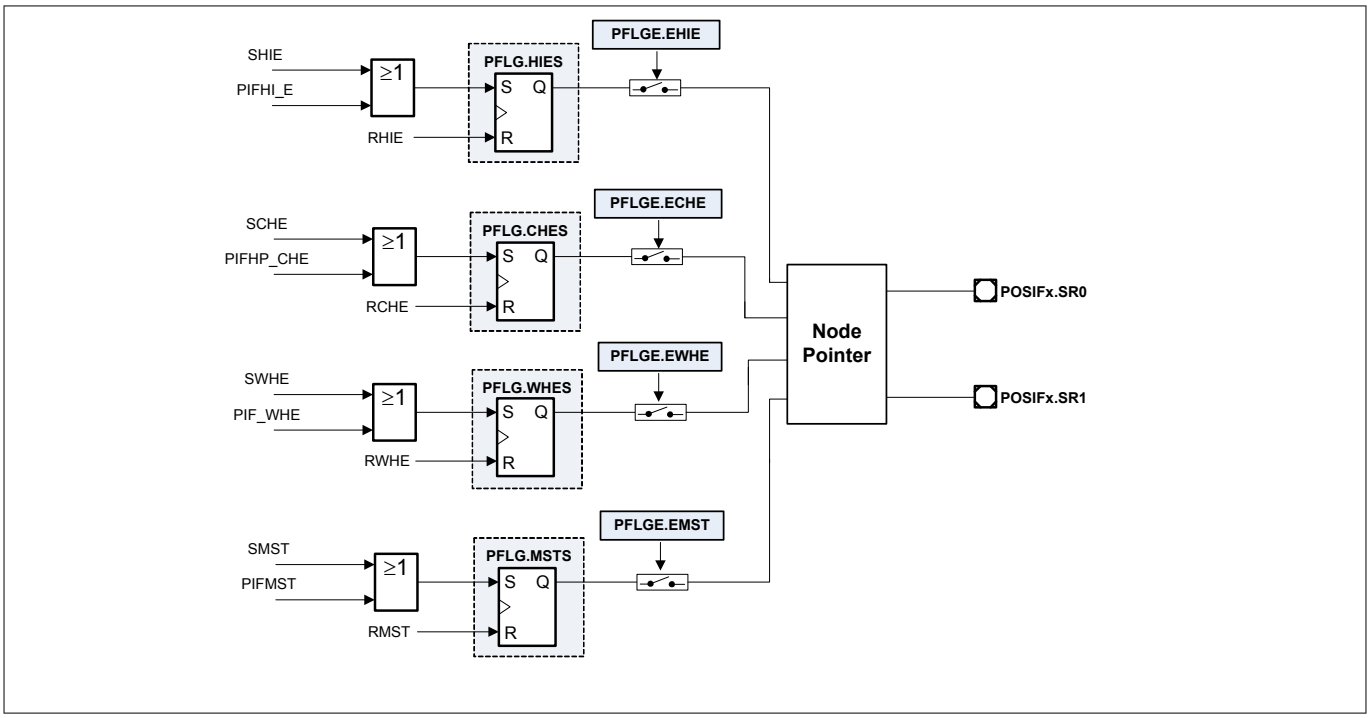


Figure 259 Hall Sensor Mode flags

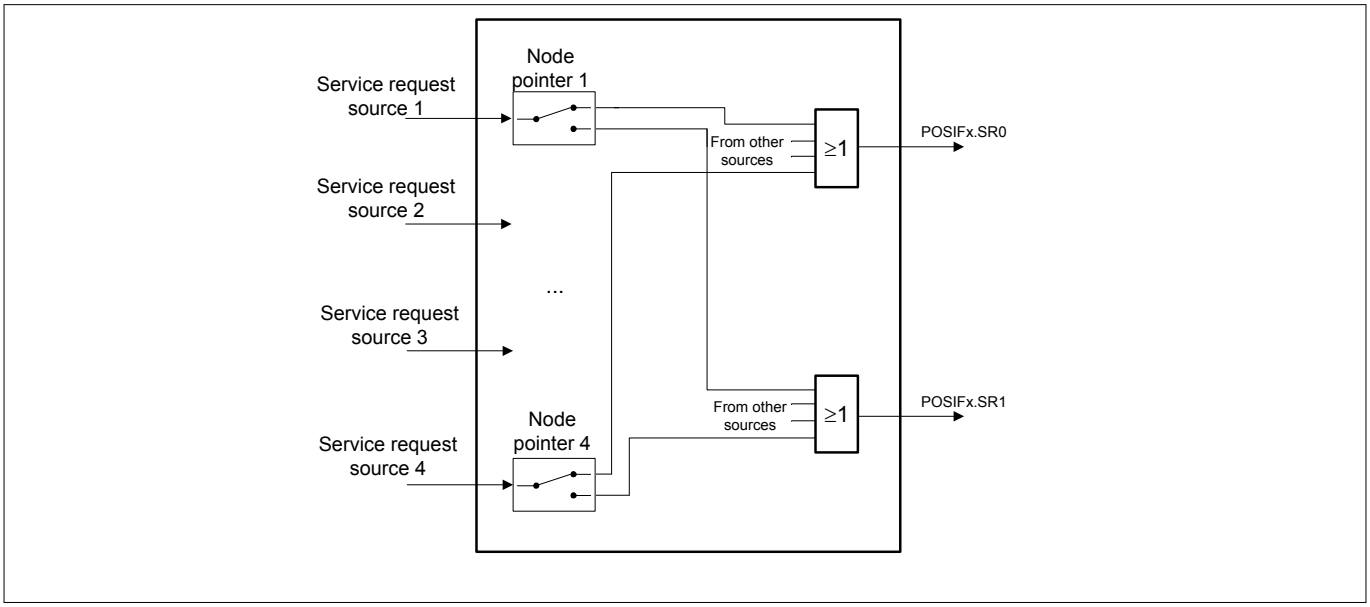


Figure 260 Interrupt node pointer overview - hall sensor mode

21.3.2 Quadrature Decoder Flags

The Quadrature Decoder Mode has five flags that can be enabled individually as interrupt sources (besides these five flags, the ones that are linked to the usage of Multi-Channel mode are also available: Multi-Channel Pattern update (***PFLG***.MSTS) and Wrong Hall event (***PFLG***.WHES). This can be useful if one selects the Quadrature Mode and the Multi-Channel stand-alone functionality.

These five flags are:

- Index event detection (***PFLG***.INDXS)
- phase detection error (***PFLG***.ERRS)
- quadrature clock generation (***PFLG***.CNTS)
- period clock generation (***PFLG***.PCLKS)
- direction change (***PFLG***.DIRS)

By enabling an interrupt source, an interrupt pulse is generated every time that a flag set operation occurs, independently if the flag is already set or not.

The index event detection flag is set every time that a index is detected.

The phase error flag is set when one invalid transition on the phase signals is detected, see ***Figure 247***.

The quadrature clock and period clock flags are generated accordingly with the timings shown in ***Figure 248***.

The direction change flag is set, every time that an inversion of the motor rotation happens.

Each flag can be set/cleared individually by SW, by writing into the specific field on the registers ***SPFLG*** and ***RPFLG***, see ***Figure 261***.

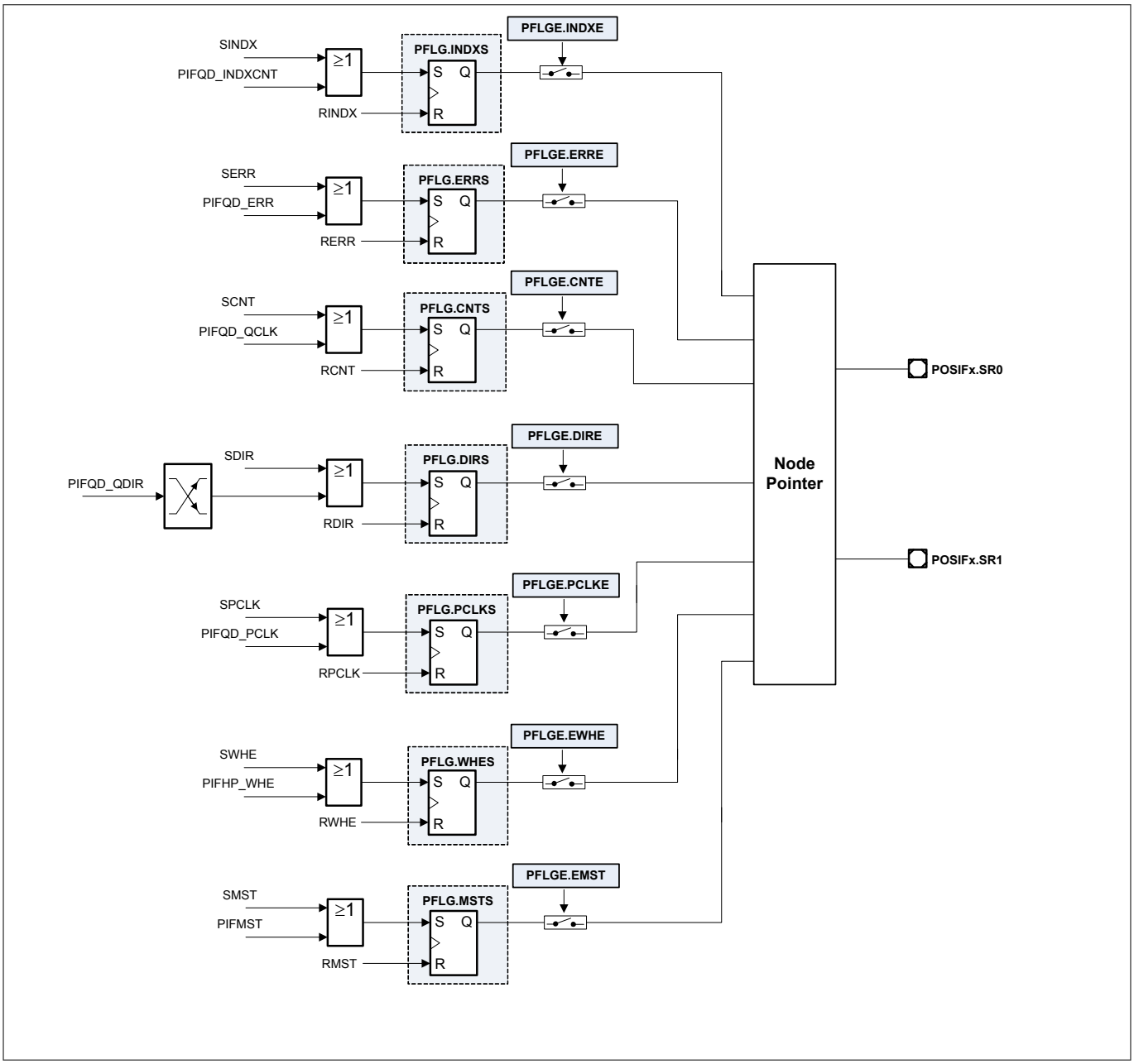


Figure 261 Quadrature Decoder flags

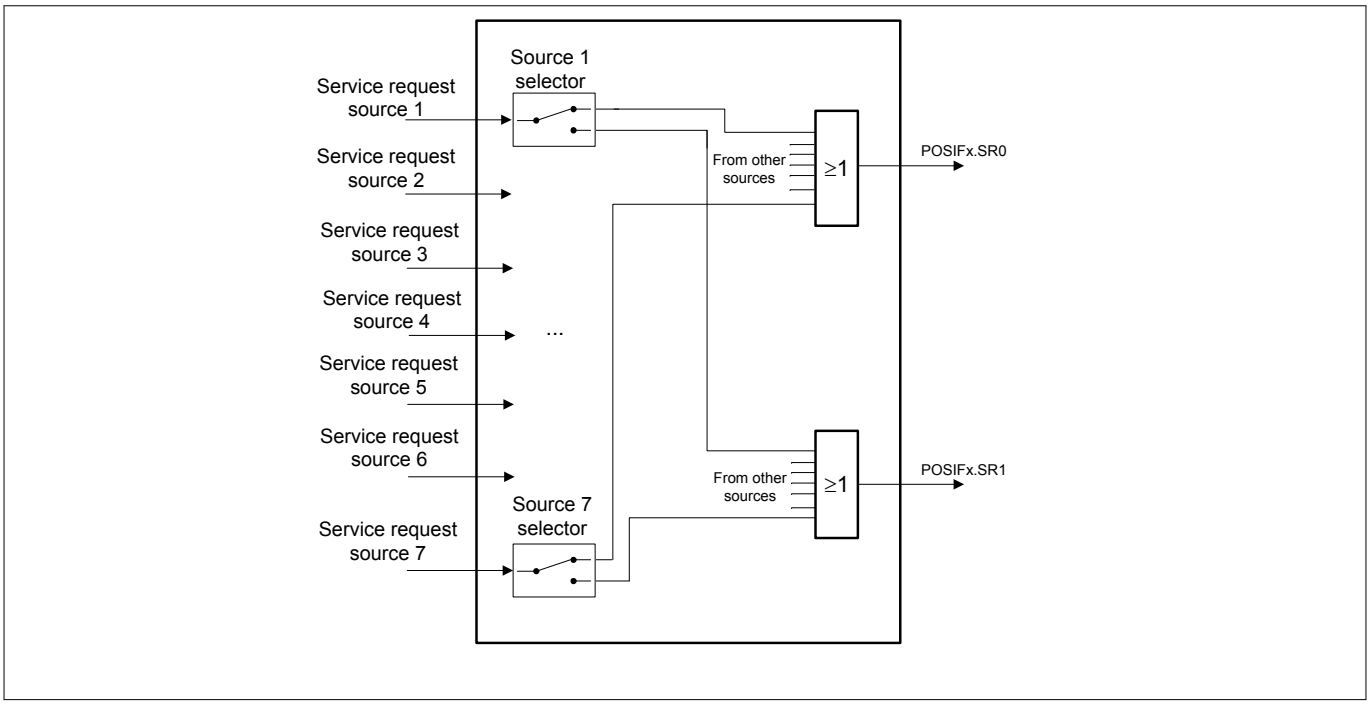


Figure 262 Interrupt node pointer overview - quadrature decoder mode

21.4 Debug Behavior

In suspend mode, the entire block is halted. The registers can still be accessed by the CPU (read only). This mode is useful for debugging purposes, e.g., where the current device status should be frozen in order to get a snapshot of the internal values. In suspend mode, all counters are stopped. The suspend mode is non-intrusive concerning the register bits. This means register bits are not modified by hardware when entering or leaving the suspend mode.

Entry into suspend mode can be configured at the kernel level by means of the register ***PSUS***.

The module is only functional after the suspend signal becomes inactive.

21.5 Power, Reset and Clock

The following sections describe the operating conditions, characteristics and timing requirements for the POSIF. All the timing information is related to the module clock, f_{posif}.

21.5.1 Clocks

Module Clock

It is possible to disable the module clock for the POSIF, via a specific system control bit, nevertheless, there may be a dependency on the f_{posif} through the different POSIF instances or Capture/Compare Units. One should address the SCU Chapter for a complete description of the product clock scheme.

External Signals

The maximum frequency for the external signals, linked with the Hall Sensor and Rotary Encoder inputs can be seen in ***Table 269***.

Table 269 External Hall/Rotary signals operating conditions

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Frequency	f_{esig}	–	–	$f_{posif}/4$	MHz	
ON time	ton_{esig}	$2T_{posif}$	–	–	ns	
OFF time	$toff_{esig}$	$2T_{posif}$	–	–	ns	

21.5.2 Power

The POSIF is inside the power core domain, therefore no special considerations about power up or power down sequences need to be taken. For a explanation about the different power domains, please address the SCU (System Control Unit) chapter.

21.6 Initialization and System Dependencies

21.6.1 Initialization

The initialization sequence for an application that is using the POSIF, should be the following:

Note: Due to different startup conditions of the motor system itself (as well SW control loop implementation) it is possible to receive some erroneous interrupt triggers before the SW and HW loop are completely locked. To overcome this, the SW can ignore the interrupts during start up or the interrupt sources can be enabled only after a proper lock between HW and SW has been sensed.

21.6.2 System Dependencies

Each POSIF may have different dependencies regarding module and bus clock frequencies. This dependencies should be addressed in the SCU and System Architecture Chapters.

Dependencies between several peripherals, regarding different clock operating frequencies may also exist. This should be addressed before configuring the connectivity between the POSIF and some other peripheral.

The following topics must be taken into consideration for good POSIF and system operation:

- POSIF module clock must be at maximum two times faster than the module bus interface clock
- Module input triggers for the POSIF must not exceed the module clock frequency (if the triggers are generated internally in the device)
- Module input triggers for the POSIF must not exceed the frequency dictated in ***Chapter 21.5.1***
- Frequency of the POSIF outputs used as triggers/functions on other modules, must be crosschecked on the end point
- Applying and removing POSIF from reset, can cause unwanted operations in other modules. This can occur if the modules are using POSIF outputs as triggers/functions.

21.7 Registers

Registers Overview

The absolute register address is calculated by adding:
Module Base Address + Offset Address

Table 270 Registers Address Space

Module	Base Address	End Address	Note
POSIF0	50010000_H	$50013FFF_H$	
POSIF1	50014000_H	$50017FFF_H$	

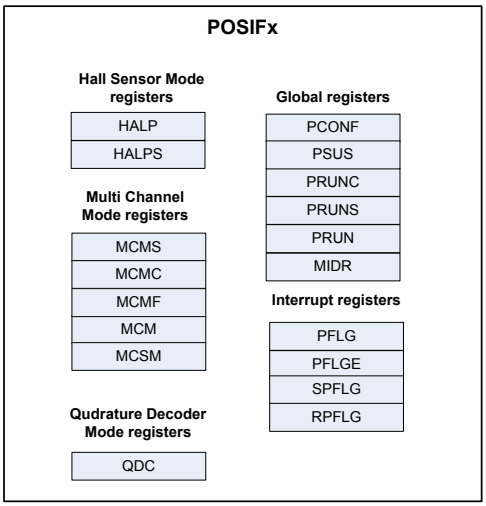


Figure 263 POSIF registers overview

Table 271 Register Overview of POSIF

Short Name	Description	Offset Addr.[55]	Access Mode		Description see
			Read	Write	
POSIF Kernel Registers					
PCONF	Global control register	0000_H	U, PV	U, PV	Page 768
PSUS	Suspend Configuration	0004_H	U, PV	U, PV	Page 771
PRUNS	POSIF run bit set	0008_H	U, PV	U, PV	Page 772
PRUNC	POSIF run bit clear	$000C_H$	U, PV	U, PV	Page 772
PRUN	POSIF run bit status	0010_H	U, PV	BE	Page 773
PDBG	Debug Design Register	0100_H	U, PV	BE	Page 774
MIDR	Module Identification register	0020_H	U, PV	BE	Page 774
Hall Sensor Mode Registers					
HALP	Hall Current and Expected patterns	0030_H	U, PV	BE	Page 775
HALPS	Hall Current and Expected shadow patterns	0034_H	U, PV	U, PV	Page 776
Multi-Channel Mode Register					
MCM	Multi-Channel Mode Pattern	0040_H	U, PV	BE	Page 777

55 The absolute register address is calculated as follows: Module Base Address + Offset Address (shown in this column)

Table 271 Register Overview of POSIF (continued)

Short Name	Description	Offset Addr.[55]	Access Mode		Description see
			Read	Write	
MCSM	Multi-Channel Mode shadow Pattern	0044_H	U, PV	U, PV	Page 777
MCMS	Multi-Channel Mode Control set	0048_H	U, PV	U, PV	Page 778
MCMC	Multi-Channel Mode Control clear	$004C_H$	U, PV	U, PV	Page 778
MCMF	Multi-Channel Mode flag status	0050_H	U, PV	BE	Page 779
Quadrature Decoder Mode Register					
QDC	Quadrature Decoder Configuration	0060_H	U, PV	U, PV	Page 780
Interrupt Registers					
PFLG	POSIF interrupt status	0070_H	U, PV	BE	Page 781
PFLGE	POSIF interrupt enable	0074_H	U, PV	U, PV	Page 782
SPFLG	Interrupt set register	0078_H	U, PV	U, PV	Page 784
RPFLG	Interrupt clear register	$007C_H$	U, PV	U, PV	Page 785

21.7.1 Global registers

21.7.1.1 Register PCONF

The register contains the global configuration for the POSIF operation: operation mode, input selection, filter configuration.

PCONF Address: 0000_H

POSIF configuration Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0		LPC		EWIL	EWIE	EWIS		MSYNS		MSES	MSETS			SPES	DSEL
r		rw		rw	rw	rw		rw		rw	rw			rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		INSEL2		INSEL1		INSEL0		0		MCUE	HIDG	0	QDCM	FSEL	
r		rw		rw		rw		r		rw	rw	r	rw	rw	

55 The absolute register address is calculated as follows: Module Base Address + Offset Address (shown in this column)

Field	Bits	Type	Description
FSEL	1:0	rw	**Function Selector** 00_B Hall Sensor Mode enabled 01_B Quadrature Decoder Mode enabled 10_B stand-alone Multi-Channel Mode enabled 11_B Quadrature Decoder and stand-alone Multi-Channel Mode enabled
QDCM	2	rw	**Position Decoder Mode selection** This field selects if the Position Decoder block is in Quadrature Mode or Direction Count Mode. In Quadrature mode, the position encoder is providing the phase signals, while in Direction Count Mode is providing a clock and a direction signal. 0_B Position encoder is in Quadrature Mode 1_B Position encoder is in Direction Count Mode.
HIDG	4	rw	**Idle generation enable** Setting this field to 1_B disables the generation of the IDLE signal that forces a clear on the Multi-Channel pattern and run bit.
MCUE	5	rw	**Multi-Channel Pattern SW update enable** 0_B Multi-Channel pattern update is controlled via HW 1_B Multi-Channel pattern update is controlled via SW
INSEL0	9:8	rw	**PhaseA/Hal input 1 selector** This fields selects which input is used for the Phase A or Hall input 1 function (dependent if the module is set for Quadrature Decoder or Hall Sensor Mode): 00_B POSIFx.IN0A 01_B POSIFx.IN0B 10_B POSIFx.IN0C 11_B POSIFx.IN0D
INSEL1	11:10	rw	**PhaseB/Hall input 2 selector** This fields selects which input is used for the Phase B or Hall input 2 function (dependent if the module is set for Quadrature Decoder or Hall Sensor Mode): 00_B POSIFx.IN1A 01_B POSIFx.IN1B 10_B POSIFx.IN1C 11_B POSIFx.IN1D
INSEL2	13:12	rw	**Index/Hall input 3 selector** This fields selects which input is used for the Index or Hall input 3 function (dependent if the module is set for Quadrature Decoder or Hall Sensor Mode): 00_B POSIFx.IN2A 01_B POSIFx.IN2B 10_B POSIFx.IN2C 11_B POSIFx.IN2D

(continued)

Field	Bits	Type	Description
DSEL	16	rw	**Delay Pin selector** This field selects which input is used to trigger the end of the delay between the detection of an edge in the Hall inputs and the actual sample of the Hall inputs. 0_B POSIFx.HSDA 1_B POSIFx.HSDB
SPES	17	rw	**Edge selector for the sampling trigger** This field selects which edge is used of the selected POSIFx.HSD[B...A] signal to trigger a sample of the Hall inputs. 0_B Rising edge 1_B Falling edge
MSETS	20:18	rw	**Pattern update signal select** Selects the input signal that is used to enable a Multi-Channel pattern update. 000_B POSIFx.MSETA 001_B POSIFx.MSETB 010_B POSIFx.MSETC 011_B POSIFx.MSETD 100_B POSIFx.MSETE 101_B POSIFx.MSETF 110_B POSIFx.MSETG 111_B POSIFx.MSETH
MSES	21	rw	**Multi-Channel pattern update trigger edge** 0_B The signal used to enable a pattern update is active on the rising edge 1_B The signal used to enable a pattern update is active on the falling edge
MSYNS	23:22	rw	**PWM synchronization signal selector** This fields selects which input is used as trigger for Multi-Channel pattern update (synchronization with the PWM signal). 00_B POSIFx.MSYNCA 01_B POSIFx.MSYNCB 10_B POSIFx.MSYNCC 11_B POSIFx.MSYNCD
EWIS	25:24	rw	**Wrong Hall Event selection** 00_B POSIFx.EWHEA 01_B POSIFx.EWHEB 10_B POSIFx.EWHEC 11_B POSIFx.EWHED
EWIE	26	rw	**External Wrong Hall Event enable** 0_B External wrong hall event emulation signal, POSIFx.EWHE[D...A], is disabled 1_B External wrong hall event emulation signal, POSIFx.EWHE[D...A], is enabled.

(continued)

Field	Bits	Type	Description
EWIL	27	rw	**External Wrong Hall Event active level** 0_B POSIFx.EWHE[D...A] signal is active HIGH 1_B POSIFx.EWHE[D...A] signal is active LOW
LPC	30:28	rw	**Low Pass Filters Configuration** 000_B Low pass filter disabled 001_B Low pass of 1 clock cycle 010_B Low pass of 2 clock cycles 011_B Low pass of 4 clock cycles 100_B Low pass of 8 clock cycles 101_B Low pass of 16 clock cycles 110_B Low pass of 32 clock cycles 111_B Low pass of 64 clock cycles
0	3, 7:6, 15:14, 31	r	**Reserved** Read always returns 0

21.7.1.2 Register PSUS

The register contains the suspend configuration for the POSIF.

PSUS Address: 0004_H

POSIF Suspend Config Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0												MSUS		QSUS	
r												rw		rw	

Field	Bits	Type	Description
QSUS	1:0	rw	**Quadrature Mode Suspend Config** This field controls the entering in suspend for the quadrature decoder mode. 00_B Suspend request ignored 01_B Stop immediately 10_B Suspend in the next index occurrence 11_B Suspend in the next phase (PhaseA or PhaseB) occurrence

(continued)

Field	Bits	Type	Description
MSUS	3:2	rw	**Multi-Channel Mode Suspend Config** This field controls the entering in suspend for the Multi-Channel mode. The Hall sensor mode is also covered by this configuration. 00_B Suspend request ignored 01_B Stop immediately. Multi-Channel pattern is not set to the reset value. 10_B Stop immediately. Multi-Channel pattern is set to the reset value. 11_B Suspend with the synchronization of the PWM signal. Multi-Channel pattern is set to the reset value at the same time of the synchronization.
0	31:4	r	**Reserved** Read always returns 0

21.7.1.3 Register PRUNS

Via this register it is possible to set the run bit of the module.

PRUNS Address: 0008_H

POSIF Run Bit Set Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0															SRB
r															w

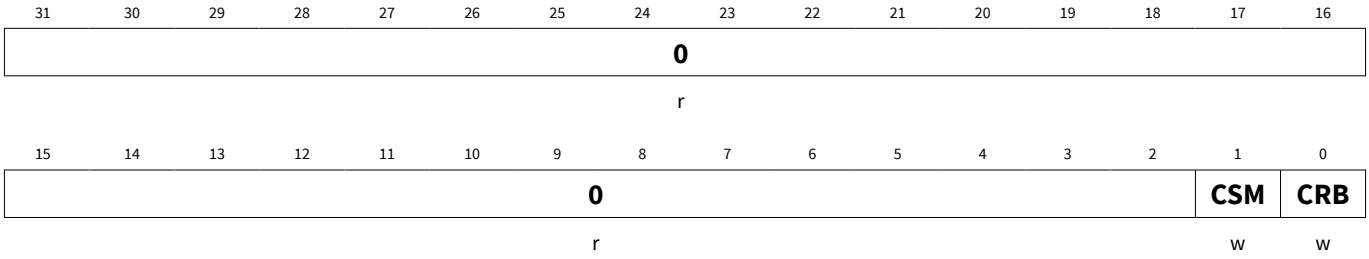
Field	Bits	Type	Description
SRB	0	w	**Set Run bit** Writing an 1_B into this bit sets the run bit of the module. Read always returns 0.
0	31:1	r	**Reserved** Read always returns 0

21.7.1.4 Register PRUNC

Via this register it is possible to clear the run bit and the internal state machines of the module.

PRUNC Address: $000C_H$

POSIF Run Bit Clear Reset Value: 00000000_H



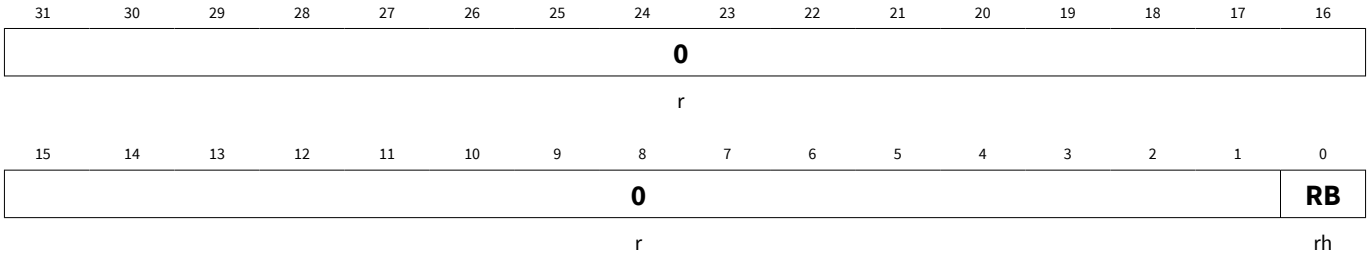
Field	Bits	Type	Description
CRB	0	w	**Clear Run bit** Writing an 1_B into this bit clears the run bit of the module. The module is stopped. Read always returns 0.
CSM	1	w	**Clear Current internal status** Writing an 1_B into this bit resets the state machine of the quadrature decoder and the current status of the Hall sensor and Multi-Channel mode registers. The flags and static configuration bit fields are not cleared. Read always returns 0.
0	31:2	r	**Reserved** Read always returns 0

21.7.1.5 Register PRUN

The register contains the run bit status of the POSIF.

PRUN Address: 0010_H

POSIF Run Bit Status Reset Value: 00000000_H



Field	Bits	Type	Description
RB	0	rh	**Run Bit** This field indicates if the module is in running or IDLE state. 0_B IDLE 1_B Running
0	31:1	r	**Reserved** Read always returns 0

21.7.1.6 Register PDBG

Debug register for current state of the POSIF state machines and Hall Sampled values.

PDBG Address: 0100_H

POSIF Debug register Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0				**LPP2**						**LPP1**					
r				rh						rh					

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		**LPP0**						**HSP**			**IVAL**	**QPSV**		**QCSV**	
r		rh						rh			rh	rh		rh	

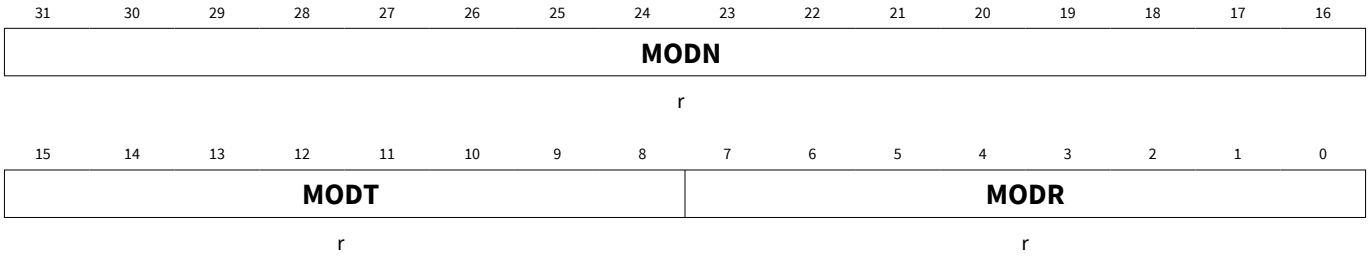
Field	Bits	Type	Description
QCSV	1:0	rh	**Quadrature Decoder Current state** QCSV[0] - Phase A QCSV[1] - Phase B
QPSV	3:2	rh	**Quadrature Decoder Previous state** QPSV[0] - Phase A QPSV[1] - Phase B
IVAL	4	rh	**Current Index Value**
HSP	7:5	rh	**Hall Current Sampled Pattern** HSP[0] - Hall Input 1 HSP[1] - Hall Input 2 HSP[2] - Hall Input 3
LPP0	13:8	rh	**Actual count of the Low Pass Filter for POSI0**
LPP1	21:16	rh	**Actual count of the Low Pass Filter for POSI1**
LPP2	27:22	rh	**Actual count of the Low Pass Filter for POSI2**
0	31:28, 15:14	r	**Reserved** A read always returns 0.

21.7.1.7 Register MIDR

This register contains the module identification number.

MIDR Address: 0020_H

Module Identification register Reset Value: $00A8C0XX_H$



Field	Bits	Type	Description
MODR	7:0	r	**Module Revision** This bit field indicates the revision number of the module implementation (depending on the design step).
MODT	15:8	r	**Module Type**
MODN	31:16	r	**Module Number**

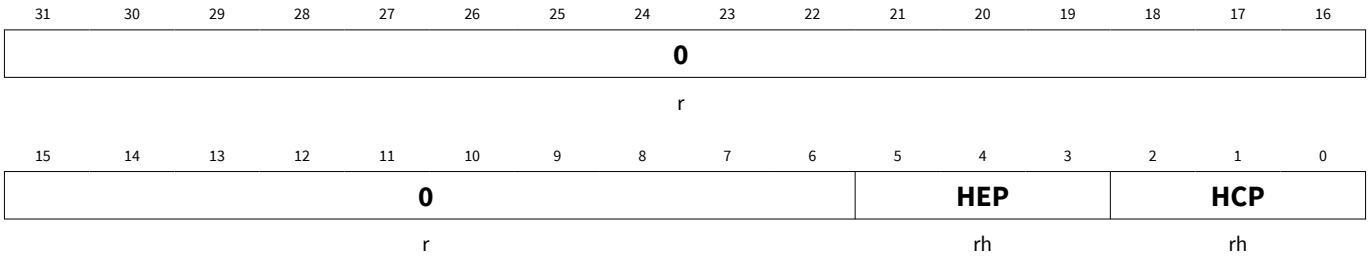
21.7.2 Hall Sensor Mode Registers

21.7.2.1 Register HALP

The register contains the values for the Hall Expected Pattern and Hall Current Pattern.

HALP Address: 0030_H

Hall Sensor Patterns Reset Value: 00000000_H



Field	Bits	Type	Description
HCP	2:0	rh	**Hall Current Pattern** This field contains the Hall Current pattern. This field is updated with the ***HALPS***.HCPS value every time that a correct hall event occurs. HCP[0] - Hall Input 1 HCP[1] - Hall Input 2 HCP[2] - Hall Input 3

(continued)

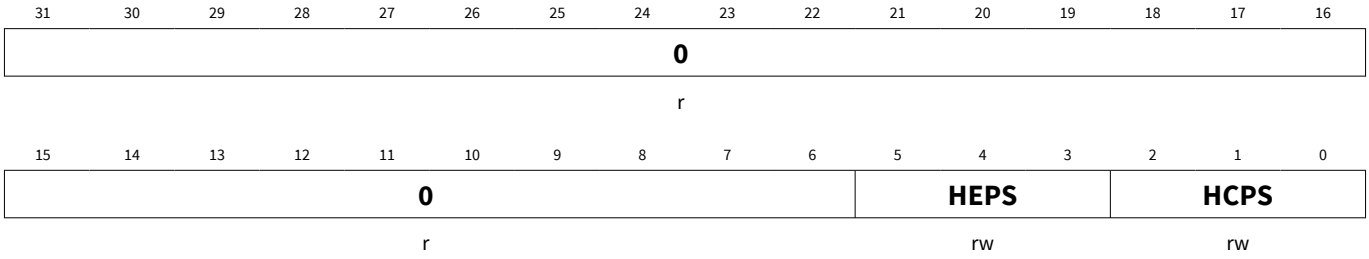
Field	Bits	Type	Description
HEP	5:3	rh	**Hall Expected Pattern** This field contains the Hall Expected pattern. This field is updated with the ***HALPS***.HEPS values every time that a correct hall event occurs. HEP[0] - Hall Input 1 HEP[1] - Hall Input 2 HEP[2] - Hall Input 3
0	31:6	r	**Reserved** Read always returns 0

21.7.2.2 Register HALPS

The register contains the values that are going to be loaded into the ***HALP*** register when the next correct hall event occurs.

HALPS Address: 0034_H

Hall Sensor Shadow Patterns Reset Value: 00000000_H



Field	Bits	Type	Description
HCPS	2:0	rw	**Shadow Hall Current Pattern** This field contains the next Hall Current pattern value. This field is set on the ***HALP***.HCP field every time that a correct hall event occurs. HCPS[0] - Hall Input 1 HCPS[1] - Hall Input 2 HCPS[2] - Hall Input 3
HEPS	5:3	rw	**Shadow Hall expected Pattern** This field contains the next Hall Expected pattern. This field is set on the ***HALP***.HEP field every time that a correct hall event occurs. HEPS[0] - Hall Input 1 HEPS[1] - Hall Input 2 HEPS[2] - Hall Input 3
0	31:6	r	**Reserved** Read always returns 0

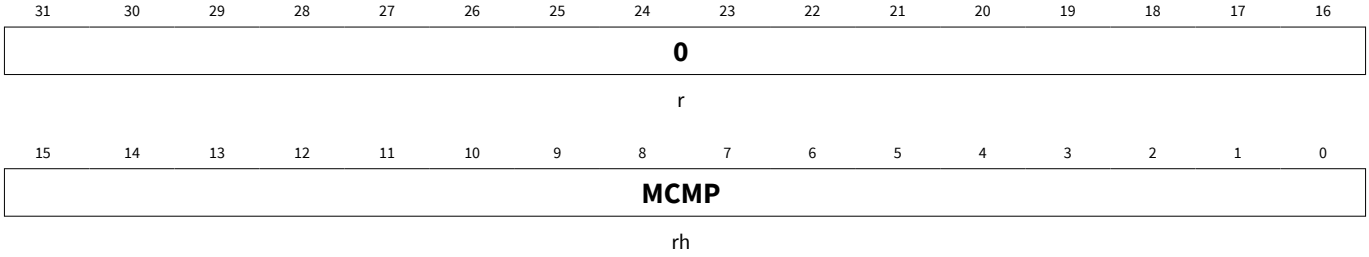
21.7.3 Multi-Channel Mode Registers

21.7.3.1 Register MCM

The register contains the value of the Multi-Channel pattern that is applied to the outputs POSIFx.OUT[15:0].

MCM Address: 0040_H

Multi-Channel Pattern Reset Value: 00000000_H



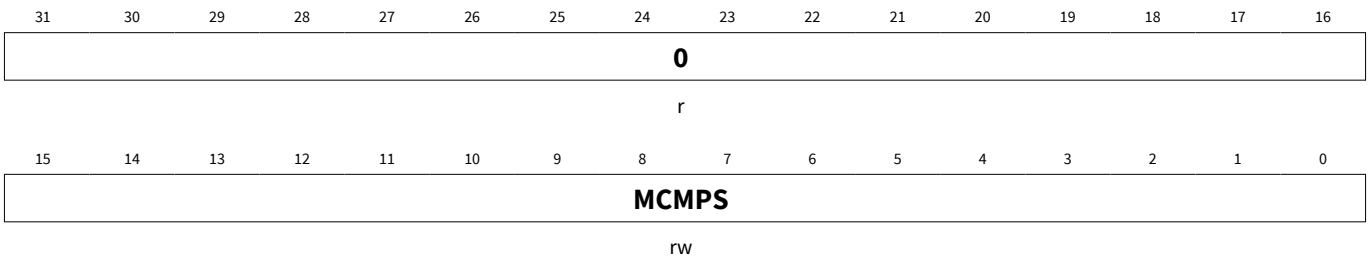
Field	Bits	Type	Description
MCMP	15:0	rh	**Multi-Channel Pattern** This field contains the Multi-Channel Pattern that is going to be applied to the Multi-Channel outputs, POSIFx.MOUT[15:0]. This field is updated with the value of the ***MCSM***.MCMPS every time that a Multi-Channel pattern update is triggered.
0	31:16	r	**Reserved** Read always returns 0

21.7.3.2 Register MCSM

The register contains the value that is going to be loaded into the ***MCM*** register when the next Multi-Channel update trigger occurs.

MCSM Address: 0044_H

Multi-Channel Shadow Pattern Reset Value: 00000000_H



Field	Bits	Type	Description
MCMPS	15:0	rw	**Shadow Multi-Channel Pattern** This field contains the next Multi-Channel Pattern. Every time that a Multi-Channel pattern transfer is triggered, this value is passed into the field ***MCM***.MCMP.

(continued)

Field	Bits	Type	Description
0	31:16	r	**Reserved** Read always returns 0

21.7.3.3 Register MCMS

Through this register it is possible to request a Multi-Channel pattern update. It is also possible through this register to request an immediate update of the Multi-Channel and Hall Sensor patterns without waiting for the hardware trigger.

MCMS Address: 0048_H

Multi-Channel Pattern Control set Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0													STMR	STHR	MNPS
r													w	w	w

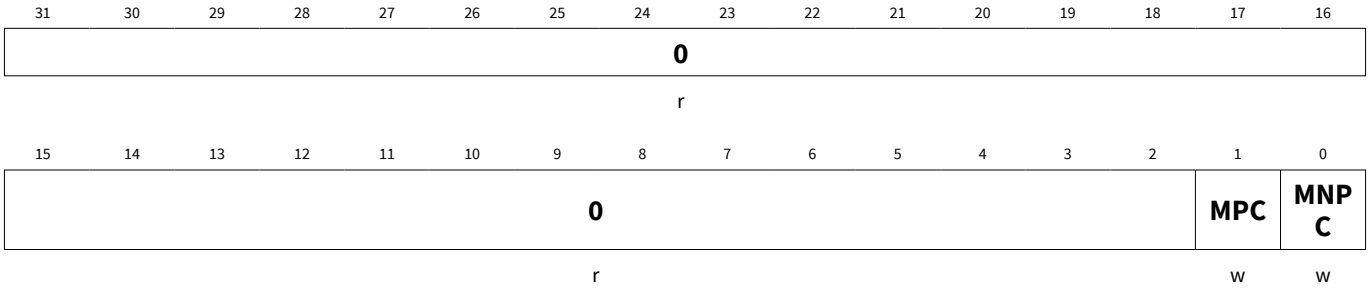
Field	Bits	Type	Description
MNPS	0	w	**Multi-Channel Pattern Update Enable Set** Writing a 1_B into this field enables the Multi-Channel pattern update (sets the ***MCMF***.MSS bit). The update is not done immediately due to the fact that the trigger that synchronizes the update with the PWM is still needed. A read always returns 0.
STHR	1	w	**Hall Pattern Shadow Transfer Request** Writing a 1_B into this field leads to an immediate update of the fields ***HALP***.HCP and ***HALP***.HEP. A read always returns 0.
STMR	2	w	**Multi-Channel Shadow Transfer Request** Writing a 1_B into this field leads to an immediate update of the field ***MCM***.MCMP. A read always returns 0.
0	31:3	r	**Reserved** Read always returns 0

21.7.3.4 Register MCMC

Through this register is possible to cancel a Multi-Channel pattern update and to clear the Multi-Channel pattern to the default value.

MCMC Address: $004C_H$

Multi-Channel Pattern Control clear Reset Value: 00000000_H



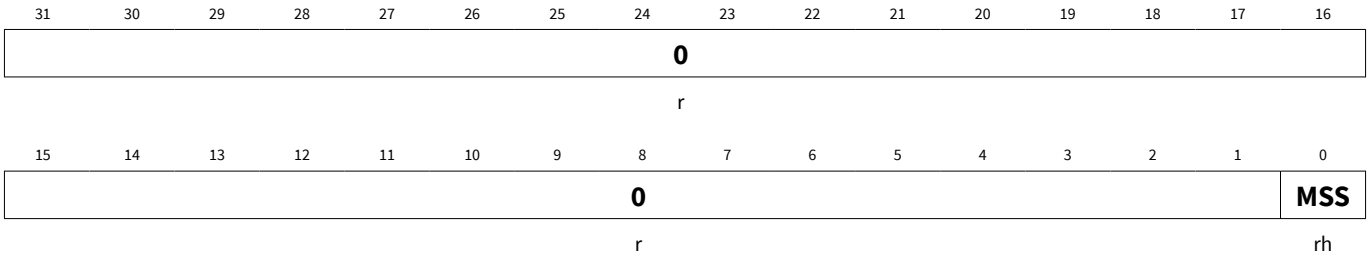
Field	Bits	Type	Description
MNPC	0	w	**Multi-Channel Pattern Update Enable Clear** Writing a 1_B into this field clears the ***MCMF***.MSS bit. A read always returns 0.
MPC	1	w	**Multi-Channel Pattern clear** Writing a 1_B into this field clears the Multi-Channel Pattern value to 0000_H. A read always returns 0.
0	31:2	r	**Reserved** Read always returns 0

21.7.3.5 Register MCMF

The register contains the status of the Multi-Channel update request.

MCMF Address: 0050_H

Multi-Channel Pattern Control flag Reset Value: 00000000_H



Field	Bits	Type	Description
MSS	0	rh	**Multi-Channel Pattern update status** This field indicates if the Multi-Channel pattern is ready to be updated or not. When this field is set, the Multi-Channel pattern is updated when the triggering signal, selected from the POSIFx.MSYNC[D...A], becomes active. 0_B Update of the Multi-Channel pattern is set 1_B Update of the Multi-Channel pattern is not set
0	31:1	r	**Reserved** Read always returns 0

21.7.4 Quadrature Decoder Registers

21.7.4.1 Register QDC

The register contains the configuration for the operation of the Quadrature Decoder Mode.

QDC Address: 0060_H

Quadrature Decoder Control Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0							**DVAL**	**0**		**ICM**		**0**	**PHS**	**PBLS**	**PALS**
r							rh	r		rw		r	rw	rw	rw

Field	Bits	Type	Description
PALS	0	rw	**Phase A Level selector** 0_B Phase A is active HIGH 1_B Phase A is active LOW
PBLS	1	rw	**Phase B Level selector** 0_B Phase B is active HIGH 1_B Phase B is active LOW
PHS	2	rw	**Phase signals swap** 0_B Phase A is the leading signal for clockwise rotation 1_B Phase B is the leading signal for clockwise rotation
ICM	5:4	rw	**Index Marker generations control** This field controls the generation of the index marker that is linked to the output pin POSIFx.OUT3. 00_B No index marker generation on POSIFx.OUT3 01_B Only first index occurrence generated on POSIFx.OUT3 10_B All index occurrences generated on POSIFx.OUT3 11_B Reserved
DVAL	8	rh	**Current rotation direction** 0_B Counterclockwise rotation 1_B Clockwise rotation
0	3, 7:6, 31:9	r	**Reserved** Read always returns 0

21.7.5 Interrupt Registers

21.7.5.1 Register PFLG

The register contains the status of all the interrupt flags of the module.

PFLG Address: 0070_H

POSIF Interrupt Flags Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0			PCLKS	DIRS	CNTS	ERRS	INDXS	0			MSTS	0	HIES	WHES	CHES
r			rh	rh	rh	rh	rh	r			rh	r	rh	rh	rh

Field	Bits	Type	Description
CHES	0	rh	**Correct Hall Event Status** 0_B Correct Hall Event not detected 1_B Correct Hall Event detected
WHES	1	rh	**Wrong Hall Event Status** 0_B Wrong Hall Event not detected 1_B Wrong Hall Event detected
HIES	2	rh	**Hall Inputs Update Status** 0_B Transition on the Hall Inputs not detected 1_B Transition on the Hall Inputs detected
MSTS	4	rh	**Multi-Channel pattern shadow transfer status** 0_B Shadow transfer not done 1_B Shadow transfer done
INDXS	8	rh	**Quadrature Index Status** 0_B Index event not detected 1_B Index event detected
ERRS	9	rh	**Quadrature Phase Error Status** 0_B Phase Error event not detected 1_B Phase Error event detected
CNTS	10	rh	**Quadrature CLK Status** 0_B Quadrature clock not generated 1_B Quadrature clock generated
DIRS	11	rh	**Quadrature Direction Change** 0_B Change on direction not detected 1_B Change on direction detected
PCLKS	12	rh	**Quadrature Period Clk Status** 0_B Period clock not generated 1_B Period clock generated
0	3, 7:5, 31:13	r	**Reserved** Read always returns 0

21.7.5.2 Register PFLGE

Through this register it is possible to enable or disable each of the available interrupt sources. It is also possible to select to which service request line an interrupt is forward.

PFLGE Address: 0074_H

POSIF Interrupt Enable Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0			PCLSEL	DIRSEL	CNTSEL	ERRSEL	INDSEL	0			MSTSEL	0	HIESEL	WHESEL	CHESEL
r			rw	rw	rw	rw	rw	r			rw	r	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0			EPCLK	EDIR	ECNT	EERR	EINDX	0			EMST	0	EHIE	EWHE	ECHE
r			rw	rw	rw	rw	rw	r			rw	r	rw	rw	rw

Field	Bits	Type	Description
ECHE	0	rw	**Correct Hall Event Enable** 0_B Correct Hall Event interrupt disabled 1_B Correct Hall Event interrupt enabled
EWHE	1	rw	**Wrong Hall Event Enable** 0_B Wrong Hall Event interrupt disabled 1_B Wrong Hall Event interrupt enabled
EHIE	2	rw	**Hall Input Update Enable** 0_B Update of the Hall Inputs interrupt is disabled 1_B Update of the Hall Inputs interrupt is enabled
EMST	4	rw	**Multi-Channel pattern shadow transfer enable** 0_B Shadow transfer event interrupt disabled 1_B Shadow transfer event interrupt enabled
EINDX	8	rw	**Quadrature Index Event Enable** 0_B Index event interrupt disabled 1_B Index event interrupt enabled
EERR	9	rw	**Quadrature Phase Error Enable** 0_B Phase error event interrupt disabled 1_B Phase error event interrupt enabled
ECNT	10	rw	**Quadrature CLK interrupt Enable** 0_B Quadrature CLK event interrupt disabled 1_B Quadrature CLK event interrupt enabled
EDIR	11	rw	**Quadrature direction change interrupt Enable** 0_B Direction change event interrupt disabled 1_B Direction change event interrupt enabled

(continued)

Field	Bits	Type	Description
EPCLK	12	rw	**Quadrature Period CLK interrupt Enable** 0_B Quadrature Period CLK event interrupt disabled 1_B Quadrature Period CLK event interrupt enabled
CHESEL	16	rw	**Correct Hall Event Service Request Selector** 0_B Correct Hall Event interrupt forward to POSIFx.SR0 1_B Correct Hall Event interrupt forward to POSIFx.SR1
WHESEL	17	rw	**Wrong Hall Event Service Request Selector** 0_B Wrong Hall Event interrupt forward to POSIFx.SR0 1_B Wrong Hall Event interrupt forward to POSIFx.SR1
HIESEL	18	rw	**Hall Inputs Update Event Service Request Selector** 0_B Hall Inputs Update Event interrupt forward to POSIFx.SR0 1_B Hall Inputs Update Event interrupt forward to POSIFx.SR1
MSTSEL	20	rw	**Multi-Channel pattern Update Event Service Request Selector** 0_B Multi-Channel pattern Update Event interrupt forward to POSIFx.SR0 1_B Multi-Channel pattern Update Event interrupt forward to POSIFx.SR1
INDSEL	24	rw	**Quadrature Index Event Service Request Selector** 0_B Quadrature Index Event interrupt forward to POSIFx.SR0 1_B Quadrature Index Event interrupt forward to POSIFx.SR1
ERRSEL	25	rw	**Quadrature Phase Error Event Service Request Selector** 0_B Quadrature Phase error Event interrupt forward to POSIFx.SR0 1_B Quadrature Phase error Event interrupt forward to POSIFx.SR1
CNTSEL	26	rw	**Quadrature Clock Event Service Request Selector** 0_B Quadrature Clock Event interrupt forward to POSIFx.SR0 1_B Quadrature Clock Event interrupt forward to POSIFx.SR1
DIRSEL	27	rw	**Quadrature Direction Update Event Service Request Selector** 0_B Quadrature Direction Update Event interrupt forward to POSIFx.SR0 1_B Quadrature Direction Update Event interrupt forward to POSIFx.SR1
PCLSEL	28	rw	**Quadrature Period clock Event Service Request Selector** 0_B Quadrature Period clock Event interrupt forward to POSIFx.SR0 1_B Quadrature Period clock Event interrupt forward to POSIFx.SR1
0	3, 7:5, 15:13, 19, 23:21, 31:29	r	**Reserved** Read always returns 0

21.7.5.3 Register SPFLG

Through this register it is possible for the SW to set a specific interrupt status flag.

SPFLG Address: 0078_H

POSIF Interrupt Set Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0			SPCLK	SDIR	SCNT	SERR	SINDX	0			SMST	0	SHIE	SWHE	SCHE
r			w	w	w	w	w	r			w	r	w	w	w

Field	Bits	Type	Description
SCHE	0	w	**Correct Hall Event flag set** Writing a 1_B to this field sets the ***PFLG***.CHES bit field. An interrupt pulse is generated. A read always returns 0.
SWHE	1	w	**Wrong Hall Event flag set** Writing a 1_B to this field sets the ***PFLG***.WHES bit field. An interrupt pulse is generated. A read always returns 0.
SHIE	2	w	**Hall Inputs Update Event flag set** Writing a 1 to this field sets the ***PFLG***.HIES bit field. An interrupt pulse is generated. A read always returns 0.
SMST	4	w	**Multi-Channel Pattern shadow transfer flag set** Writing a 1_B to this field sets the ***PFLG***.MSTS bit field. An interrupt pulse is generated. A read always returns 0.
SINDX	8	w	**Quadrature Index flag set** Writing a 1_B to this field sets the ***PFLG***.INDXS bit field. An interrupt pulse is generated. A read always returns 0.
SERR	9	w	**Quadrature Phase Error flag set** Writing a 1_B to this field sets the ***PFLG***.ERRS bit field. An interrupt pulse is generated. A read always returns 0.
SCNT	10	w	**Quadrature CLK flag set** Writing a 1 to this field sets the ***PFLG***.CNTS bit field. An interrupt pulse is generated. A read always returns 0.

(continued)

Field	Bits	Type	Description
SDIR	11	w	**Quadrature Direction flag set** Writing a 1_B to this field sets the ***PFLG***.DIRS bit field. An interrupt pulse is generated. A read always returns 0.
SPCLK	12	w	**Quadrature period clock flag set** Writing a 1_B to this field sets the ***PFLG***.PCLKS bit field. An interrupt pulse is generated. A read always returns 0.
0	3, 7:5, 31:13	r	**Reserved** Read always returns 0

21.7.5.4 Register RPFLG

Through this register it is possible for the SW to reset/clear a specific interrupt status flag.

RPFLG Address: $007C_H$

POSIF Interrupt Clear Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0			RPCLK	RDIR	RCNT	RERR	RINDX	0			RMST	0	RHIE	RWHE	RCHE
r			w	w	w	w	w	r			w	r	w	w	w

Field	Bits	Type	Description
RCHE	0	w	**Correct Hall Event flag clear** Writing a 1_B to this field clears the ***PFLG***.CHES bit field. A read always returns 0.
RWHE	1	w	**Wrong Hall Event flag clear** Writing a 1_B to this field clears the ***PFLG***.WHES bit field. A read always returns 0.
RHIE	2	w	**Hall Inputs Update Event flag clear** Writing a 1_B to this field clears the ***PFLG***.HIES bit field. A read always returns 0.
RMST	4	w	**Multi-Channel Pattern shadow transfer flag clear** Writing a 1_B to this field clears the ***PFLG***.MSTS bit field. A read always returns 0.
RINDX	8	w	**Quadrature Index flag clear** Writing a 1_B to this field clears the ***PFLG***.INDXS bit field. A read always returns 0.

(continued)

Field	Bits	Type	Description
RERR	9	w	**Quadrature Phase Error flag clear** Writing a 1_B to this field clears the ***PFLG***.ERRS bit field. A read always returns 0.
RCNT	10	w	**Quadrature CLK flag clear** Writing a 1_B to this field clears the ***PFLG***.CNTS bit field. A read always returns 0.
RDIR	11	w	**Quadrature Direction flag clear** Writing a 1_B to this field clears the ***PFLG***.DIRS bit field. A read always returns 0.
RPCLK	12	w	**Quadrature period clock flag clear** Writing a 1_B to this field clears the ***PFLG***.PCLKS bit field. A read always returns 0.
0	3, 7:5, 31:13	r	**Reserved** Read always returns 0

21.8 Interconnects

The following tables, describe the connectivity present on the device for each POSIF module.
The GPIO connections are available at the Ports chapter.

21.8.1 POSIF0 Pins

Table 272 POSIF0 Pin Connections

Global Input/Output	I/O	Connected To	Description
POSIF0.CLK	I	PCLK	Module clock is the same one used by the capcoms
POSIF0.IN0A	I		Shared connection for rotary encoder and hall sensor
POSIF0.IN0B	I	P0.13	Shared connection for rotary encoder and hall sensor
POSIF0.IN0C	I	VADC0.CBFLOUT0	Shared connection for rotary encoder and hall sensor
POSIF0.IN0D	I	ERU0.PDOUT0	Shared connection for rotary encoder and hall sensor
POSIF0.IN1A	I	P1.1	Shared connection for rotary encoder and hall sensor
POSIF0.IN1B	I	P0.14	Shared connection for rotary encoder and hall sensor
POSIF0.IN1C	I	VADC0.CBFLOUT1	Shared connection for rotary encoder and hall sensor

Table 272 POSIF0 Pin Connections (continued)

Global Input/Output	I/O	Connected To	Description
POSIF0.IN1D	I	ERU0.PDOUT1	Shared connection for rotary encoder and hall sensor
POSIF0.IN2A	I	P1.0	Shared connection for rotary encoder and hall sensor
POSIF0.IN2B	I	P0.15	Shared connection for rotary encoder and hall sensor
POSIF0.IN2C	I	VADC0.CBFLOUT2	Shared connection for rotary encoder and hall sensor
POSIF0.IN2D	I	ERU0.PDOUT2	Shared connection for rotary encoder and hall sensor
POSIF0.HSDA	I	CCU40.ST0	Used for the Hall pattern sample delay. Like the dead time counter in capcom6
POSIF0.HSDB	I	POSIF0.OUT0	Used for the Hall pattern sample delay. Like the dead time counter in capcom6
POSIF0.EWHEA	I	VADC0.CBFLOUT3	Wrong Hall event emulation, Trap, etc
POSIF0.EWHEB	I	ERU0.IOUT0	Wrong Hall event emulation, Trap, etc
POSIF0.EWHEC	I	ERU0.IOUT3	Wrong Hall event emulation, Trap, etc
POSIF0.EWHED	I	ERU1.IOUT3	Wrong Hall event emulation, Trap, etc
POSIF0.MSETA	I	CCU40.SR0	Multi Pattern updated set. Requests a new shadow transfer
POSIF0.MSETB	I	CCU40.ST1	Multi Pattern updated set. Requests a new shadow transfer
POSIF0.MSETC	I	CCU40.ST2	Multi Pattern updated set. Requests a new shadow transfer
POSIF0.MSETD	I	CCU40.ST3	Multi Pattern updated set. Requests a new shadow transfer
POSIF0.MSETE	I	CCU80.SR1	Multi Pattern updated set. Requests a new shadow transfer
POSIF0.MSETF	I	ERU0.IOUT2	Multi Pattern updated set. Requests a new shadow transfer
POSIF0.MSETG	I	ERU0.IOUT3	Multi Pattern updated set. Requests a new shadow transfer
POSIF0.MSETH	I	POSIF0.OUT1	Multi Pattern updated set. Requests a new shadow transfer
POSIF0.MSYNCA	I	CCU80.PS1	Sync for updating the multi channel pattern with the shadow transfer
POSIF0.MSYNCB	I	CCU80.PS3	Sync for updating the multi channel pattern with the shadow transfer

Table 272 POSIF0 Pin Connections (continued)

Global Input/Output	I/O	Connected To	Description
POSIF0.MSYNCC	I	CCU40.PS1	Sync for updating the multi channel pattern with the shadow transfer
POSIF0.MSYNCD	I	POSIF0.OUT6	Sync for updating the multi channel pattern with the shadow transfer
POSIF0.OUT0	O	CCU40.IN0AE; CCU40.IN1AE; CCU40.IN2BC; CCU40.IN3BC; POSIF0.HSDB;	Quadrature mode: Quadrature clock; Hall sensor mode: Hall input edge detection
POSIF0.OUT1	O	CCU40.IN0AF; CCU40.IN1AF; CCU40.IN2AE; CCU40.IN3BD; POSIF0.MSETH;	Quadrature mode: Shaft direction; Hall sensor mode: Correct Hall Event
POSIF0.OUT2	O	CCU40.IN2AF; CCU80.IN0AD; CCU80.IN1AD; CCU80.IN2AD; CCU80.IN3AD;	Quadrature mode: Pclk for velocity; Hall sensor mode: Idle/wrong hall event
POSIF0.OUT3	O	CCU40.IN0AG; CCU40.IN1AG; CCU40.IN2AG; CCU40.IN3AE;	Quadrature mode: Index event used for Clear/capt; Hall sensor mode: stop in Hall sensor mode
POSIF0.OUT4	O	CCU40.IN1AH; CCU40.IN2AH;	Quadrature mode:Index event; Hall sensor mode: Multi channel pattern update done
POSIF0.OUT5	O	CCU40.IN3AF; CCU80.IN0AE; CCU80.IN1AE; CCU80.IN2AE; CCU80.IN3AE;	Sync start
POSIF0.OUT6	O	CCU40.MCSS; CCU80.MCSS; POSIF0.MSYNCD;	Multi channel pattern update request
POSIF0.MOUT[0]	O	CCU80.MCI00;	Multi channel pattern
POSIF0.MOUT[1]	O	CCU80.MCI01;	Multi channel pattern
POSIF0.MOUT[2]	O	CCU80.MCI02;	Multi channel pattern
POSIF0.MOUT[3]	O	CCU80.MCI03;	Multi channel pattern
POSIF0.MOUT[4]	O	CCU80.MCI10;	Multi channel pattern
POSIF0.MOUT[5]	O	CCU80.MCI11;	Multi channel pattern
POSIF0.MOUT[6]	O	CCU80.MCI12;	Multi channel pattern
POSIF0.MOUT[7]	O	CCU80.MCI13;	Multi channel pattern
POSIF0.MOUT[8]	O	CCU80.MCI20;	Multi channel pattern
POSIF0.MOUT[9]	O	CCU80.MCI21;	Multi channel pattern
POSIF0.MOUT[10]	O	CCU80.MCI22;	Multi channel pattern
POSIF0.MOUT[11]	O	CCU80.MCI23;	Multi channel pattern
POSIF0.MOUT[12]	O	CCU80.MCI30;	Multi channel pattern
POSIF0.MOUT[13]	O	CCU80.MCI31;	Multi channel pattern
POSIF0.MOUT[14]	O	CCU80.MCI32;	Multi channel pattern

Table 272 POSIF0 Pin Connections (continued)

Global Input/Output	I/O	Connected To	Description
POSIF0.MOUT[15]	O	CCU80.MCI33;	Multi channel pattern
POSIF0.SR0	O	NVIC	Service request line 0
POSIF0.SR1	O	NVIC; VADC0.BGREQTRO; VADC0.G0REQTRO; VADC0.G1REQTRO;	Service request line 1

21.8.2 POSIF1 Pins

Table 273 POSIF1 Pin Connections

Global Input/Output	I/O	Connected To	Description
POSIF1.CLK	I	PCLK	Module clock is the same one used by the capcoms
POSIF1.IN0A	I		Shared connection for rotary encoder and hall sensor
POSIF1.IN0B	I	P4.1	Shared connection for rotary encoder and hall sensor
POSIF1.IN0C	I	VADC0.CBFLOUT0	Shared connection for rotary encoder and hall sensor
POSIF1.IN0D	I	ERU1.PDOUT0	Shared connection for rotary encoder and hall sensor
POSIF1.IN1A	I		Shared connection for rotary encoder and hall sensor
POSIF1.IN1B	I	P4.2	Shared connection for rotary encoder and hall sensor
POSIF1.IN1C	I	VADC0.CBFLOUT1	Shared connection for rotary encoder and hall sensor
POSIF1.IN1D	I	ERU1.PDOUT1	Shared connection for rotary encoder and hall sensor
POSIF1.IN2A	I		Shared connection for rotary encoder and hall sensor
POSIF1.IN2B	I	P4.3	Shared connection for rotary encoder and hall sensor
POSIF1.IN2C	I	VADC0.CBFLOUT2	Shared connection for rotary encoder and hall sensor
POSIF1.IN2D	I	ERU1.PDOUT2	Shared connection for rotary encoder and hall sensor
POSIF1.HSDA	I	CCU41.ST0	Used for the Hall pattern sample delay. Like the dead time counter in capcom6

Table 273 POSIF1 Pin Connections (continued)

Global Input/Output	I/O	Connected To	Description
POSIF1.HSDB	I	POSIF1.OUT0	Used for the Hall pattern sample delay. Like the dead time counter in capcom6
POSIF1.EWHEA	I	VADC0.CBFLOUT3	Wrong Hall event emulation, Trap, etc
POSIF1.EWHEB	I	ERU1.IOUT0	Wrong Hall event emulation, Trap, etc
POSIF1.EWHEC	I	ERU1.IOUT3	Wrong Hall event emulation, Trap, etc
POSIF1.EWHED	I	ERU0.IOUT3	Wrong Hall event emulation, Trap, etc
POSIF1.MSETA	I	CCU41.SR0	Multi Pattern updated set. Requests a new shadow transfer
POSIF1.MSETB	I	CCU41.ST1	Multi Pattern updated set. Requests a new shadow transfer
POSIF1.MSETC	I	CCU41.ST2	Multi Pattern updated set. Requests a new shadow transfer
POSIF1.MSETD	I	CCU41.ST3	Multi Pattern updated set. Requests a new shadow transfer
POSIF1.MSETE	I	CCU81.SR1	Multi Pattern updated set. Requests a new shadow transfer
POSIF1.MSETF	I	ERU1.IOUT2	Multi Pattern updated set. Requests a new shadow transfer
POSIF1.MSETG	I	ERU1.IOUT3	Multi Pattern updated set. Requests a new shadow transfer
POSIF1.MSETH	I	POSIF1.OUT1	Multi Pattern updated set. Requests a new shadow transfer
POSIF1.MSYNCA	I	CCU81.PS1	Sync for updating the multi channel pattern with the shadow transfer
POSIF1.MSYNCB	I	CCU81.PS3	Sync for updating the multi channel pattern with the shadow transfer
POSIF1.MSYNCC	I	CCU41.PS1	Sync for updating the multi channel pattern with the shadow transfer
POSIF1.MSYNCD	I	POSIF1.OUT6	Sync for updating the multi channel pattern with the shadow transfer
POSIF1.OUT0	O	CCU41.IN0AE; CCU41.IN1AE; CCU41.IN2BC; CCU41.IN3BC; POSIF1.HSDB;	Quadrature mode: Quadrature clock; Hall sensor mode: Hall input edge detection
POSIF1.OUT1	O	CCU41.IN0AF; CCU41.IN1AF; CCU41.IN2AE; CCU41.IN3BD; POSIF1.MSETH;	Quadrature mode: Shaft direction; Hall sensor mode: Correct Hall Event
POSIF1.OUT2	O	CCU41.IN2AF; CCU81.IN0AD; CCU81.IN1AD; CCU81.IN2AD; CCU81.IN3AD;	Quadrature mode: Pclk for velocity; Hall sensor mode: Idle/wrong hall event

Table 273 POSIF1 Pin Connections (continued)

Global Input/Output	I/O	Connected To	Description
POSIF1.OUT3	O	CCU41.IN0AG; CCU41.IN1AG; CCU41.IN2AG; CCU41.IN3AE;	Quadrature mode: Index event used for Clear/capt; Hall sensor mode: stop in Hall sensor mode
POSIF1.OUT4	O	CCU41.IN1AH; CCU41.IN2AH;	Quadrature mode:Index event; Hall sensor mode: Multi channel pattern update done
POSIF1.OUT5	O	CCU41.IN3AF; CCU81.IN0AE; CCU81.IN1AE; CCU81.IN2AE; CCU81.IN3AE;	Sync start
POSIF1.OUT6	O	CCU41.MCSS; CCU81.MCSS; POSIF1.MSYNCD;	Multi channel pattern update request
POSIF1.MOUT[0]	O	CCU81.MCI00;	Multi channel pattern
POSIF1.MOUT[1]	O	CCU81.MCI01;	Multi channel pattern
POSIF1.MOUT[2]	O	CCU81.MCI02;	Multi channel pattern
POSIF1.MOUT[3]	O	CCU81.MCI03;	Multi channel pattern
POSIF1.MOUT[4]	O	CCU81.MCI10;	Multi channel pattern
POSIF1.MOUT[5]	O	CCU81.MCI11;	Multi channel pattern
POSIF1.MOUT[6]	O	CCU81.MCI12;	Multi channel pattern
POSIF1.MOUT[7]	O	CCU81.MCI13;	Multi channel pattern
POSIF1.MOUT[8]	O	CCU81.MCI20;	Multi channel pattern
POSIF1.MOUT[9]	O	CCU81.MCI21;	Multi channel pattern
POSIF1.MOUT[10]	O	CCU81.MCI22;	Multi channel pattern
POSIF1.MOUT[11]	O	CCU81.MCI23;	Multi channel pattern
POSIF1.MOUT[12]	O	CCU81.MCI30;	Multi channel pattern
POSIF1.MOUT[13]	O	CCU81.MCI31;	Multi channel pattern
POSIF1.MOUT[14]	O	CCU81.MCI32;	Multi channel pattern
POSIF1.MOUT[15]	O	CCU81.MCI33;	Multi channel pattern
POSIF1.SR0	O	NVIC	Service request line 0
POSIF1.SR1	O	NVIC; ERU1.3A1;	Service request line 1

22 Analog-to-Digital Converter (ADC)

The analog-to-digital converter of IMC300A provides up to 7 analog input channels. It is based on a high-speed 12-Bit converter clocked at 32 MHz using the successive approximation register (SAR) principle to convert analog input values (voltages) to discrete digital values. Each analog input channel can be configured to be amplified by an adjustable gain factor. Conversion mode and sampling time can be configured in order to meet the requirements of the application.

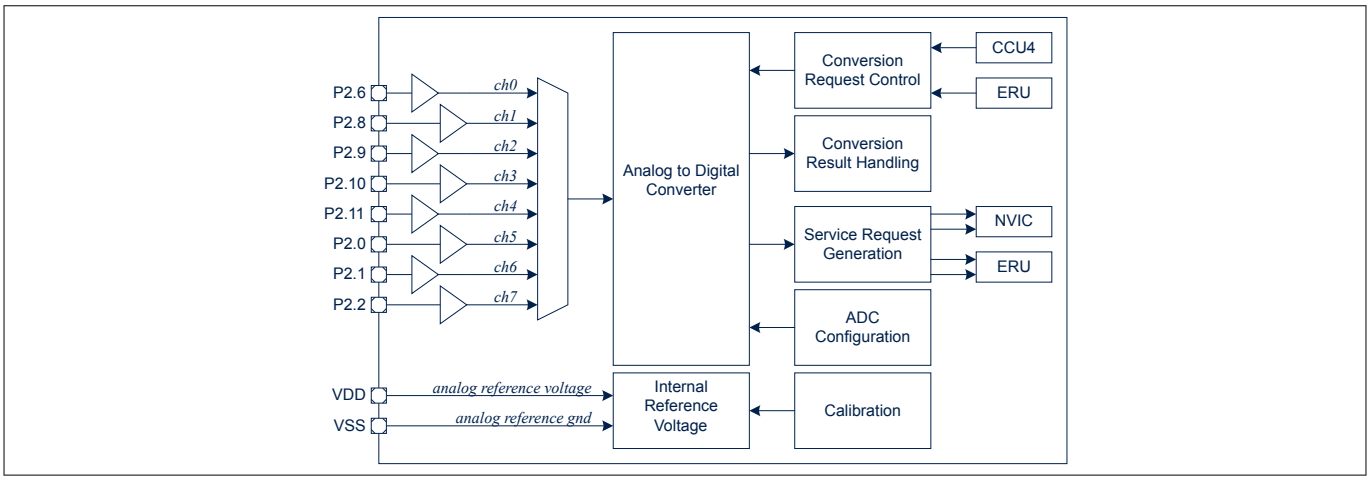


Figure 264 Block Diagram

The reference voltage of the ADC is internally generated and can be automatically calibrated to the supply voltage of the device. If required, additional calibration steps can be automatically performed after each conversion.

The ADC offers two first-order sigma-delta loops which can be assigned to any of the input channels (***Chapter 22.1.3***). They hold the quantization error of the previous conversion in order to automatically consider this tiny amount of charge in the next conversion. This will increase the Effective Number Of Bits (ENOB) while implementing oversampling algorithms.

The Conversion Request Control Unit (***Chapter 22.2***) controls the sampling and conversion of the analog input signal. Conversions of single channels as well as a scan of selected channels can be configured. The start of the conversion sequence is either a software command or a hardware trigger from an interconnected peripheral or a signal at a port pin.

The conversion result is provided in a result register with a wait-for-read option. The wait-for-read mode avoids data loss due to premature result overwrite, by blocking a conversion until the previous result has been read. Automatic accumulation of consecutive measurements can be performed by the data reduction filter which is described in ***Chapter 22.4.4***.

Flexible service request generation is based on selectable events which can be routed to two interrupts.

- Source events indicate the completion of a conversion sequence in the corresponding request source. This event can be used to trigger the setup of a new sequence
- Result events indicate the availability of new result data in the corresponding result register. If data reduction mode is active, events are generated only after a complete accumulation sequence

Each event can be assigned to one of four service request nodes. This allows grouping the requests according to the requirements of the application.

22.1 Analog Module Activation and Control

The analog converter of the ADC is the functional block that generates the digital result values from the selected input voltage. It draws a permanent current during its operation and can be deactivated between conversions to reduce the consumed overall energy.

Note: After reset, the analog converters are off. They must be enabled before triggering any action involving the converter.

22.1.1 Analog Converter Control

Bit ANOFF in register ***SHS0_SHSCFG*** forces the analog part into power-down mode, without changing the configuration of the associated groups. While ANOFF = 0, the analog part is enabled.

Wakeup Time from Analog Powerdown

When the converter is activated (ANOFF = 0), it needs a certain wakeup time to settle before a conversion can be properly executed. This wakeup time can be established by waiting the required period before starting a conversion.

22.1.2 Calibration

Calibration compensates deviations caused by process, temperature, and voltage variations. This ensures accurate results throughout the operation time.

Several different calibration cycles are executed for offset and gain calibration. These calibration cycles are executed alternating after a conversion.

An initial startup calibration is required once after a reset. First, the converter must be enabled (ANOFF = 0_B), then the startup calibration can be initiated by setting bit SUCAL in register ***GLOBCFG***. Conversions may be started after the initial calibration sequence. This is indicated by parameter ***SHS0_SHSCFG***.STATE which can be polled by software.

The start-up calibration phase takes 1920 cycles (1920 × 31.25 ns = 60 µs).

Note: Since the ADC error depends on the temperature, the calibration can be repeated periodically.

22.1.3 Sigma-Delta-Loop Function

Each standard analog-to-digital conversion incurs a quantization error due to the limited number of steps i.e. discrete result values. By activating the sigma-delta-loop function this residual quantization error can be forwarded to the next conversion. The residual charge is stored and added to the next sampled charge. Averaging successive conversion results (with the loop enabled) can, therefore, reduce the quantization error.

*Note: The data accumulation function (see **Chapter 22.4.4**) supports this averaging.*

The loop control bitfields are available in pairs in register ***SHS0_LOOP***.

22.2 Conversion Request Generation

The conversion request unit of a group autonomously handles the generation of conversion requests.

- Software triggers directly activate the request source and request a conversion
- External triggers: An external signal can act as conversion trigger request. As a result it synchronizes the request source activation with external events, such as a trigger pulse from a timer generating a PWM signal, or from a port pin
- External gating: An external signal can block a conversion request

Application software selects the trigger type and source (***BRSCTRL***), the gating mechanism (***BRSMR***) and the channel(s) to be converted (***BRSSEL***). The request source can also be activated directly by software (***BRSMR***.LDEV = 1) without requiring an external trigger. The conversion request is then forwarded to the converter to start the sampling and conversion of the requested channel(s). ***Figure 265*** gives an overview to the conversion request source.

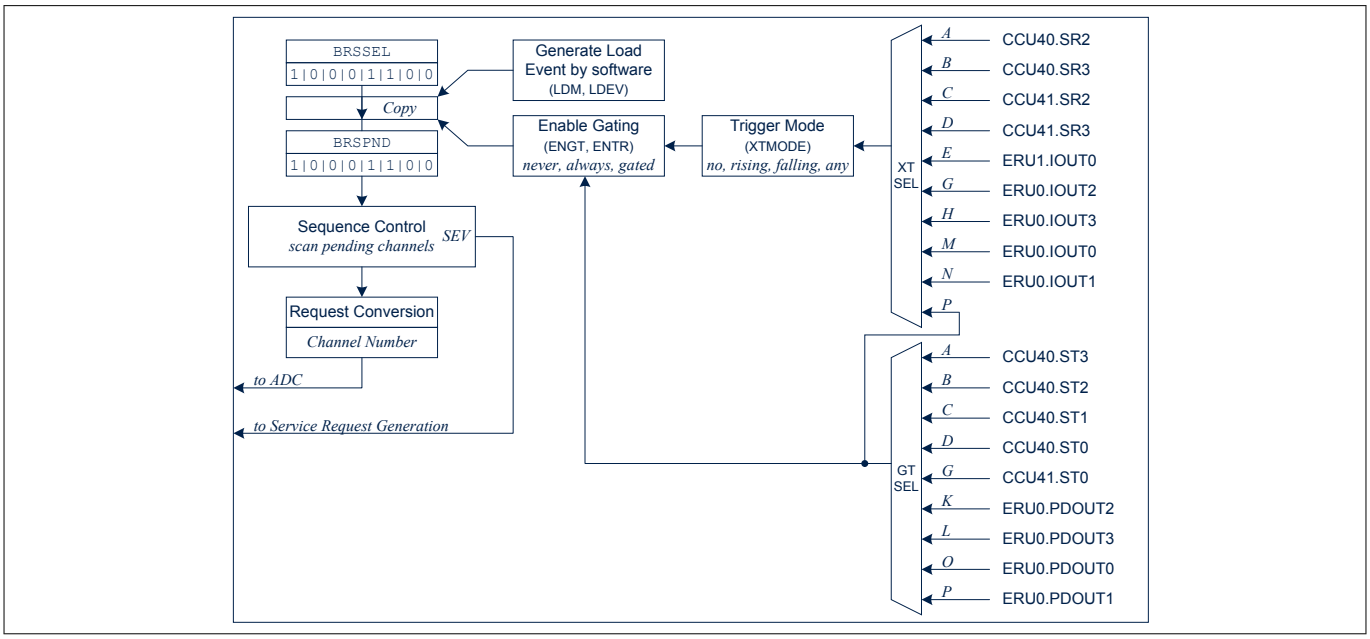


Figure 265 Conversion Request Source

The request source can operate in single-shot (scan mode) or in continuous mode (autoscan mode):

- In single-shot mode, the programmed conversion (sequence) is requested once after being triggered. A subsequent conversion (sequence) must be triggered again
- In continuous mode, the programmed conversion (sequence) is automatically requested repeatedly after being triggered once

External triggers are generated from one of 15 selectable trigger inputs (REQTRx[P:A]) and from one of 16 selectable gating inputs (REQGTx[P:A]). The available trigger signals for the IMC300A are listed in ***Chapter 22.7.3***.

22.2.1 Channel Scan Request Source Handling

Each analog input channel can be included in or excluded from the scan sequence by setting or clearing the corresponding channel select bit in register ***BRSSEL***. The programmed register value remains unchanged by an ongoing scan sequence. The scan sequence starts with the highest enabled channel number and continues towards lower channel numbers.

Upon a load event which is triggered by hardware signals or software, the request pattern is transferred to the pending bits in register ***BRSPND***. The pending conversion requests indicate which input channels are to be

converted in an ongoing scan sequence. Each conversion start that was triggered by the scan request source, automatically clears the corresponding pending bit. If the last conversion triggered by the scan source is finished and all pending bits are cleared, the current scan sequence is considered finished and a request source event (REV) is generated.

The trigger and gating unit generates load events from the selected external (outside the ADC) trigger and gating signals. For example, a timer unit can issue a request signal to synchronize conversions to PWM events.

Load events start a scan sequence and can be generated either via software or via the selected hardware triggers. The request source event can also generate an automatic load event, so the programmed sequence is automatically repeated.

Scan Source Operation

Configure the scan request source by executing the following actions:

- Select the input channels for the sequence by programming ***BRSSEL***
- If hardware trigger or gating is desired, select the appropriate trigger and gating inputs and the proper signal transitions by programming ***BRSCTRL***. Enable the trigger and select the gating mode by programming ***BRSMR***[56)]
- Define the load event operation (handling of pending bits, autoscan mode) by programming ***BRSMR***. A load event with bit LDM = 0 copies the content of ***BRSSEL*** to ***BRSPND*** (overwrite mode). This starts a new scan sequence and aborts any pending conversions from a previous scan sequence. A load event with bit LDM = 1 OR-combines the content of ***BRSSEL*** to ***BRSPND*** (combine mode). This starts a scan sequence that includes pending conversions from a previous scan sequence

Start a channel scan sequence by generating a load event:

- If a hardware trigger is selected and enabled, generate the configured transition at the selected input signal, e.g. from a timer or an input pin
- or: Generate a software load event by setting LDEV = 1 (***BRSMR***)
- or: Generate a load event by writing the scan pattern directly to the pending bits in ***BRSPND***. The pattern is copied to ***BRSSEL*** and a load event is generated automatically. In this case, a scan sequence can be defined and started with a single data write action (provided that the pattern fits into one register)

Note: If autoscan is enabled, a load event is generated automatically each time a request source event occurs when the scan sequence has finished. This permanently repeats the defined scan sequence (autoscan).

Stop or abort an ongoing scan sequence by executing one of the following actions:

- If external gating is enabled, switch the gating signal to the defined inactive level. This does not modify the conversion pending bits, but only prevents issuing conversion requests to the ADC
- Disable the channel scan source by clearing bitfield ENGT = 00_B. Clear the pending request bits by setting bit CLRPND = 1 (***BRSMR***)

Scan Request Source Events and Interrupt Service Requests

A request source event of a scan source occurs when the last conversion of a scan sequence is finished (all pending bits = 0). A request source event interrupt can be generated based on a request source event. If a request source event is detected, it sets the corresponding indication flag in register ***GLOBEFLAG***. This flag can also be set by writing 1 to the corresponding bit position, whereas writing 0 has no effect.

The service request output SRx that is selected by the request source event interrupt node pointer bitfields in register ***GLOBEVNP*** becomes activated each time the related request source event is detected (and enabled by ENSI) or the related bit position in register ***GLOBEFLAG*** is written with 1 (this write action simulates a request source event).

56 If PDOUT signals from the ERU are used, initialize the ERU accordingly before enabling the gate inputs to avoid unexpected signal transitions.

The indication flags can be cleared by SW by writing 1 to the corresponding bit position in register ***GLOBEFLAG***.[57)]

22.3 Analog Input Channel Configuration

The analog input channels are assigned to one multiplexer. A number of parameters can be configured in register ***GLOBICLASS*** that control the conversion of the channels.

22.3.1 Conversion Modes

A conversion can be executed in several ways. The conversion mode is selected according to the requested resolution of the digital result and according to the acceptable conversion time (***Chapter 22.3.2***). Use bitfield CMS in register ***GLOBICLASS*** to select a mode.

Standard Conversions

A standard conversion returns a result value with a predefined resolution. 8-bit, 10-bit, and 12-bit resolution can be selected.

These result values can be accumulated.

Fast Compare Mode

In Fast Compare Mode, the selected input voltage is directly compared with a digital value that is stored in the result register. This compare operation returns a binary result indicating the compared input voltage is above or below the given reference value. This result is generated quickly and thus supports monitoring of boundary values.

Fast Compare Mode uses a 10-bit compare value stored left-aligned at bit position 11.

57 Please refer to ***Service Request Generation*** on page 801.

22.3.2 Conversion Timing

The total time required for a conversion comprises the time from the start of the sample phase[58] until the availability of the result.

The timing basis are the module clock f_{ADC} (derived from MCLK) and the converter clock f_{SH} (typically 32 MHz).

The sample rate at which consecutive conversions are triggered also depends on several configurable factors:

- The conversion time, according to the selected conversion mode
- The frequency of external trigger signals, if enabled

The sample time can be adjusted according to the application requirements. Use bitfield STC in register ***GLOBICLASS*** to adjust the sample time.

The total conversion time is the sum of sample time and converter time. It can be computed for an N-bit (N: 8, 10 or 12) conversion with the following formula:

$t_{CN} = (2 + STC) \times 2 \times t_{ADC} + 4 \times t_{SH} + (N + 8) \times t_{SH} + 5 \times t_{ADC}$

A conversion round comprises a conversion and a calibration step. Calibration steps are executed after each conversion (up to $12 \times t_{SH}$)[59], so the maximum complete conversion round will take:

$t_{CR} = (2 + STC) \times 2 \times t_{ADC} + 4 \times t_{SH} + (N + 8) \times t_{SH} + 5 \times t_{ADC} + 12 \times t_{SH}$[59]

Timing Examples

System assumptions: $f_{ADC} = f_{SH} = 32$ MHz i.e. $t_{ADC} = t_{SH} = 31.25$ ns

According to the given formula the following minimum conversion times can be achieved:

12-bit conversion: $t_{CN12C} = 2 \times 2 \times t_{ADC} + 4 \times t_{SH} + (12 + 8) \times t_{SH} + 5 \times t_{ADC} = 33 \times 31.25$ ns = 1 032 ns

10-bit conversion: $t_{CN10C} = 2 \times 2 \times t_{ADC} + 4 \times t_{SH} + (10 + 8) \times t_{SH} + 5 \times t_{ADC} = 31 \times 31.25$ ns = 969 ns

The maximum time for an isolated conversion will take up to: t_{C1} = 1 032 ns + 12 × 31.25 ns = 1 407 ns (12-bit conversion)[60]

58 The time from the trigger event that requests the corresponding conversion until the start of the sample phase depends on propagation delays of the selected trigger signal.

59 Offset and gain calibration steps are executed alternating, where gain calibration takes more time than offset calibration (9 cycles).

60 12 calibration clock cycles are the maximum resulting from a gain calibration step.

22.4 Conversion Result Handling

The A/D converter can preprocess the conversion result data to a certain extent before storing them for retrieval by the CPU. This supports the subsequent handling of result data by the application software.

Conversion result handling comprises the following functions:

- ***Storage of Conversion Results*** and ***Data Alignment***
- ***Wait-for-Read Mode*** to avoid loss of data
- ***Result Event Generation***
- ***Data Modification***

22.4.1 Storage of Conversion Results

The conversion result values are stored in the result register (***GLOBRES***).

The result register has an individual data valid flag (VF) associated with it. This flag indicates when “new” valid data has been stored in the result register and can be read out.

For standard conversions, result values are available in bitfield RESULT. Conversions in Fast Compare Mode use bitfield RESULT for the reference value, so the result of the operation is stored in bit FCR.

The result register can be read via two different views. These views use different addresses but access the same register data:

- When the result register is read via the application view (***GLOBRES***), the corresponding valid flag is automatically cleared when the result is read. This provides an easy handshake between result generation and retrieval. This also supports wait-for-read mode
- When the result register is read via the debug view (***GLOBRESD***), the corresponding valid flag remains unchanged when the result is read. This supports debugging by delivering the result value without disturbing the handshake with the application

22.4.1.1 Data Alignment

The position of a conversion result value within the selected result register depends on two configurations:

- The selected result width (12/10/8 bits, see ***Chapter 22.3.1***)
- The selected data accumulation mode (data reduction, see ***Chapter 22.4.4***)

These options provide the conversion results in a way that minimizes data handling for the application software.

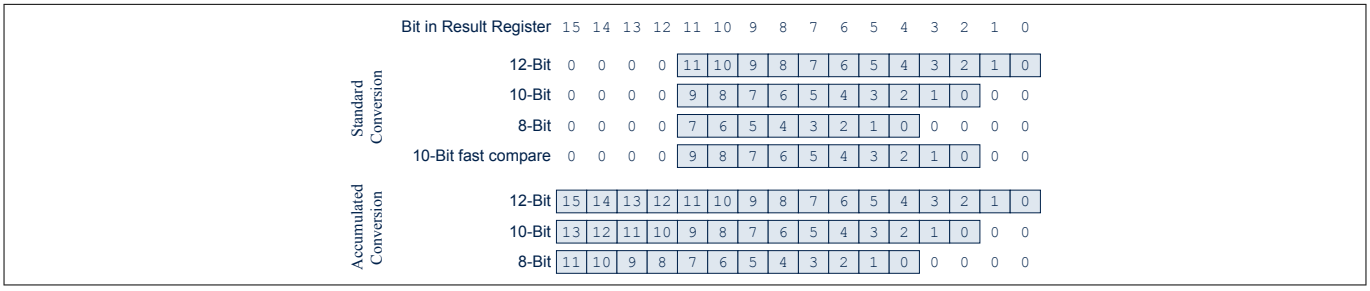


Figure 266 Result Register Data Alignment

Bitfield RESULT of register ***GLOBRES*** must be written by SW with the wanted reference comparison value for Fast Compare Mode. In this mode, bits 11-2 are evaluated, the other bits are ignored.

22.4.2 Wait-for-Read Mode

The wait-for-read mode (***GLOBRCR***.WFR = 1) prevents data loss due to overwriting the result register with a new conversion result before the CPU has read the previous data. Since the results come from different input channels, an overwrite may destroy the result from the previous conversion.

Wait-for-read mode automatically suspends the start of a conversion until the current result has been read. As a result, a conversion or a conversion sequence can be requested by a hardware or software trigger, while each conversion is only started after the result of the previous one has been read. This automatically aligns the conversion sequence with the CPU capability to read the formerly converted result (latency).

22.4.3 Result Event Generation

A result event can be generated when a new value is stored in the result register. Result events can be restricted due to data accumulation and can be generated only if the accumulation is complete.

Result events can also be suppressed completely.

22.4.4 Data Modification

The data resulting from conversions can be automatically modified before being used by an application.

The data reduction mode can be used as a digital filter for anti-aliasing or decimation purposes. It accumulates a maximum of 4 conversion values to generate a final result.

The result register can be configured for data reduction, controlled by bitfield ***GLOBRCR***.DRCTR.

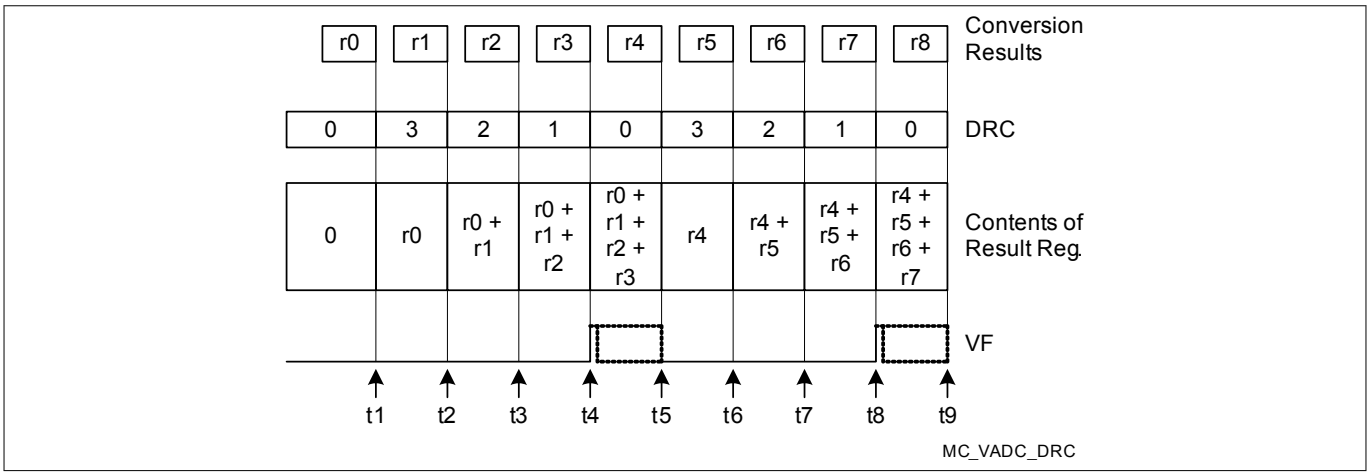


Figure 267 Standard Data Reduction Filter

This example shows a data reduction sequence of 4 accumulated conversion results. Eight conversion results (r0 … r7) are accumulated and produce 2 final results.

When a conversion is complete, data is stored in the result register with data reduction mode enabled, and the data handling is controlled by the data reduction counter DRC:

- If DRC = 0 (t1, t5, t9 in the example), the conversion result is stored to the result register. DRC is loaded with the contents of bitfield DRCTR (i.e. the accumulation begins)
- If DRC > 0 (t2, t3, t4 and t6, t7, t8 in the example), the conversion result is added to the value in the result register. DRC is decremented by 1
- If DRC becomes 0, either decremented from 1 (t4 and t8 in the example) or loaded from DRCTR, the valid bit for the respective result register is set and a result register event occurs. The final result must be read before the next data reduction sequence starts (before t5 or t9 in the example). This automatically clears the valid flag

Note: The data reduction filter may be used with a single channel only unless averaging of several channels is intended.

22.5 Service Request Generation

The A/D Converter can activate service request output signals. 2 request signals can issue an interrupt, see ***Table 278*** on page 820.

Several events can be assigned to each service request output. Service requests can be generated by three types of events:

- Request source events (SEV): indicate that the request source completed the requested conversion sequence and the application software can initiate further actions. The event is generated when the complete defined set of channels (pending bits) has been converted
- Result events (REV): indicate a new valid result in the result register. Usually, this triggers a read action by the CPU. Optionally, result events can be generated only at a reduced rate if data reduction is active

Each ADC event is indicated by a dedicated flag that can be cleared by software. If a service request is enabled for a certain event, the service request is generated for each event, independent of the status of the corresponding event indication flag. This ensures that the ADC event can generate a service request without the need to clear the indication flag.

Event flag registers indicate all types of events that occur during the ADC's operation. Software can set/clear each flag by writing a 1 to the respective position in register ***GLOBEFLAG*** to trigger/clear an event. If enabled, service requests are generated for each occurrence of an event, even if the associated flag remains set.

Node Pointer Registers

Requests from each event source can be directed to a set of service request nodes via associated node pointers. Requests from several sources can be directed to the same node; in this case, they are OR'ed to the service request output signal.

22.6 Registers

The register map of the ADC is built from two blocks, the VADC0 and the SHS0. The corresponding registers, therefore, have an individual offset assigned (see ***Table 275***). The exact register location is obtained by adding the respective register offset to the base address (see ***Table 274***) of the corresponding block.

Table 274 Registers Address Space

Module	Base Address	End Address	Note
VADC0	$4803\ 0000_H$	$4803\ 03FF_H$	
SHS0	$4803\ 4000_H$	$4803\ 41FF_H$	

Table 275 Registers Overview

Register Short Name	Register Long Name	Offset Addr.	Access Mode		Page Num.
			Read	Write	
VADC0 Register					
ID	Module Identification Register	0008_H	U, PV	BE	***803***
CLC	Clock Control Register	0000_H	U, PV	PV	***804***
OCS	OCDS Control and Status Register	0028_H	U, PV	PV	***805***
GLOBCFG	Global Configuration Register	0080_H	U, PV	U, PV	***806***
BRSCTRL	Request Source Control Register	0200_H	U, PV	U, PV	***808***
BRSMR	Request Source Mode Register	0204_H	U, PV	U, PV	***809***
BRSSEL	Request Source Channel Select Register	0180_H	U, PV	U, PV	***810***

Table 275 Registers Overview (continued)

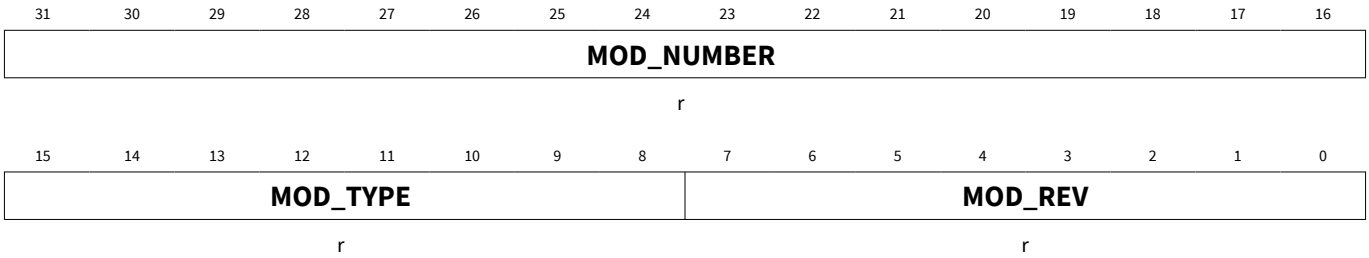
Register Short Name	Register Long Name	Offset Addr.	Access Mode		Page Num.
			Read	Write	
BRSPND	Request Source Channel Pending Register	$01C0_H$	U, PV	U, PV	811
GLOBICLASS	Input Class Register	$00A0_H$	U, PV	U, PV	812
GLOBRCR	Result Control Register	0280_H	U, PV	U, PV	813
GLOBRES	Result Register	0300_H	U, PV	U, PV	813
GLOBRESD	Result Register (debug view)	0380_H	U, PV	U, PV	813
GLOBEFLAG	Event Flag Register	$00E0_H$	U, PV	U, PV	817
GLOBEVNP	Event Node Pointer Register	0140_H	U, PV	U, PV	818
SHS0 Register					
SHS0_ID	SHS Module Identification Register	0008_H	U, SV	U, SV	803
SHSCFG	SHS Configuration Register	0040_H	U, SV	U, SV	807
GNCTR	Gain Control Register	0180_H	U, SV	U, SV	814
LOOP	SD Loop Control Register	0050_H	U, SV	U, SV	816

22.6.1 Module Identification

The module identification register indicates the version of the ADC module that is used in the IMC300A.

22.6.1.1 Register ID

ID	Address:	0008_H
Module Identification Register	Reset Value:	$00C5\ C0XX_H$
SHS0_ID	Address:	$4803\ 4008_H$
Module Identification Register	Reset Value:	$0099\ C0XX_H$



Field	Bits	Type	Description
MOD_REV	7:0	r	**Module Revision** Indicates the revision number of the implementation. This information depends on the design step.
MOD_TYPE	15:8	r	**Module Type** This internal marker is fixed toC0.
MOD_NUMBER	31:16	r	**Module Number** Indicates the module identification number (00C5= SARADC,0099= SHS).

22.6.2 System Registers

A set of standardized registers provides general access to the module and controls basic system functions.

22.6.2.1 Register CLC

The Clock Control Register ***CLC*** allows the programmer to adapt the functionality and power consumption of the module to the requirements of the application. Register ***CLC*** controls the module clock signal and the reactivity to the sleep mode signal.

CLC Address: 0000_H

Clock Control Register Reset Value: $0000\ 0003_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0												**EDIS**	**0**	**DISS**	**DISR**
r												rw	r	r	rw

Field	Bits	Type	Description
DISR	0	rw	**Module Disable Request Bit** Used for enable/disable control of the module. Also the analog section is disabled by clearing ANONS. 0_B On request: enable the module clock 1_B Off request: stop the module clock
DISS	1	r	**Module Disable Status Bit** 0_B Module clock is enabled 1_B Off: module is not clocked
0	2	r	**Reserved, write 0, read as 0**
EDIS	3	rw	**Sleep Mode Enable Control** Used to control module's reaction to sleep mode. 0_B Sleep mode request is enabled and functional 1_B Module disregards the sleep mode control signal
0	31:4	r	**Reserved, write 0, read as 0**

22.6.2.2 Register OCS

The OCDS control and status register OCS controls the module's behavior in suspend mode (used for debugging).

The OCDS Control and Status (OCS) register is cleared by Debug Reset. The OCS register can only be written when the OCDS is enabled. If OCDS is being disabled, the OCS register value will not change. When OCDS is disabled the OCS suspend control is ineffective. Write access is 32 bit wide only and requires Supervisor Mode.

OCS Address: 0028_H

OCDS Control and Status Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0		**SUSSTA**	**SUS_P**	**SUS**				**0**							
r		rh	w	rw				r							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0															
r															

Field	Bits	Type	Description
0	23:0	r	**Reserved, write 0, read as 0**
SUS	27:24	rw	**OCDS Suspend Control** Controls the sensitivity to the suspend signal coming from the OCDS Trigger Switch (OTGS) 0000_B Will not suspend 0001_B Hard suspend: Clock is switched off immediately. 0010_B Soft suspend mode 0: Stop conversions after the currently running one is completed and its result has been stored. No change for the arbiter. 0011_B Soft suspend mode 1: Stop conversions after the currently running one is completed and its result has been stored. Stop arbiter after the current arbitration round. others: Reserved
SUS_P	28	w	**SUS Write Protection** SUS is only written when SUS_P is 1, otherwise unchanged. Read as 0.
SUSSTA	29	rh	**Suspend State** 0_B Module is not (yet) suspended 1_B Module is suspended
0	31:30	r	**Reserved, write 0, read as 0**

22.6.3 General Registers

22.6.3.1 Register GLOBCFG

The global configuration register provides global control and configuration options that are valid for all converters of the cluster.

GLOBCFG Address: 0080_H

Global Configuration Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SUCAL	**0**														**DPCAL**
w	r														rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0															
r															

Field	Bits	Type	Description
0	15:0	r	**Reserved, write 0, read as 0**
DPCAL	16	rw	**Disable Post-Calibration** 0_B Automatic post-calibration after each conversion 1_B No post-calibration
0	30:17	r	**Reserved, write 0, read as 0**
SUCAL	31	w	**Start-Up Calibration** The 0-1 transition of bit SUCAL initiates the start-up calibration phase of all calibrated analog converters. 0_B No action 1_B Initiate the start-up calibration phase (indication in SHS0_SHSCFG.STATE)

22.6.3.2 Register SHS0_SHSCFG

SHS0_SHSCFG Address: $4803\ 4040_H$

SHS Configuration Register Reset Value: $0000\ 1000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
STATE				**0**											**SP**
rh				r											rh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCWC	**ANRDY**	**0**	**ANOFF**	**AREF**		**0**									
w	rh	r	rw	rw		r									

Field	Bits	Type	Description
0	9:0	r	**Reserved, write 0, read as 0**
AREF	11:10	rw	**Analog Reference Voltage Selection** 00_B External reference, upper supply range 01_B Reserved 10_B Internal reference, upper supply range 11_B Internal reference, lower supply range
ANOFF	12	rw	**Analog Converter Power Down Force**[61)] 0_B Converter controlled by bitfields ANONS (digital control block) 1_B Converter is permanently off
0	13	r	**Reserved, write 0, read as 0**
ANRDY	14	rh	**Analog Converter Ready** 0_B Converter is in power-down mode 1_B Converter is operable
SCWC	15	w	**Write Control for SHS Configuration** 0_B No write access to SHS configuration 1_B Bitfields ANOFF, AREF can be written
SP	16	rh	**Sample Pending on Group x** 0_B No sample pending 1_B Group x has finished the sample phase
0	27:17	r	**Reserved, write 0, read as 0**
STATE	31:28	rh	**Current State of Sequencer** 0000_B Idle 0001_B Offset calibration active 0010_B Gain calibration active 0011_B Startup calibration active Others: Normal operation

61 See also ***Analog Converter Control*** on page 793.

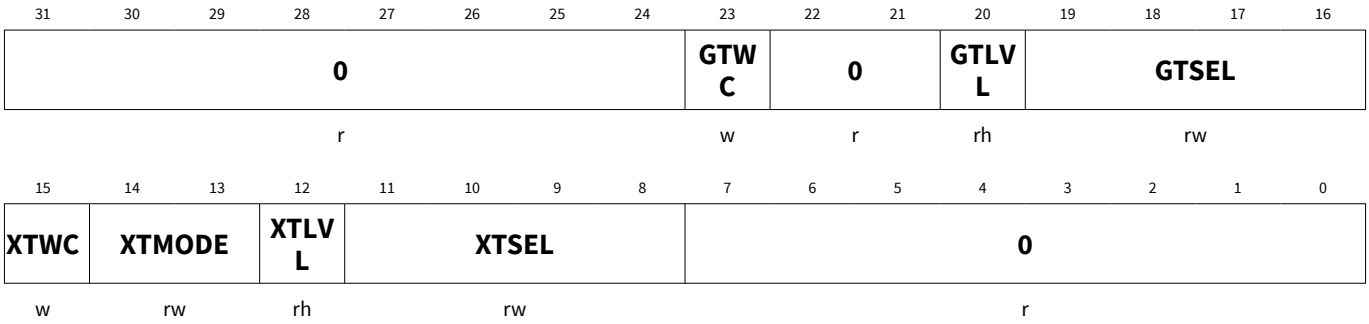
22.6.4 Conversion Request Source Registers

22.6.4.1 Register BRSCTRL

The control register of the request source selects the external gate and/or trigger signals. Write control bits allow separate control of each function with a simple write access.

BRSCTRL Address: 0200_H

Request Source Control Register Reset Value: $0000\ 0000_H$



Field	Bits	Type	Description
0	7:0	r	**Reserved, write 0, read as 0**
XTSEL	11:8	rw	**External Trigger Input Selection** The connected trigger input signals are listed in ***Table 278*** on page 820 *Note: $XTSEL = 1111_B$ uses the selected gate input as trigger source (ENGT must be $0X_B$).*
XTLVL	12	rh	**External Trigger Level** Current level of the selected trigger input
XTMODE	14:13	rw	**Trigger Operating Mode** 00_B No external trigger 01_B Trigger event upon a falling edge 10_B Trigger event upon a rising edge 11_B Trigger event upon any edge
XTWC	15	w	**Write Control for Trigger Configuration** 0_B No write access to trigger configuration 1_B Bitfields XTMODE and XTSEL can be written
GTSEL	19:16	rw	**Gate Input Selection** The connected gate input signals are listed in ***Table 278*** on page 820
GTLVL	20	rh	**Gate Input Level** Current level of the selected gate input
0	22:21	r	**Reserved, write 0, read as 0**

(continued)

Field	Bits	Type	Description
GTWC	23	w	**Write Control for Gate Configuration** 0_B No write access to gate configuration 1_B Bitfield GTSEL can be written
0	31:24	r	**Reserved, write 0, read as 0**

22.6.4.2 Register BRSMR

The Conversion Request Mode Register configures the operating mode of the background request source.

BRSMR Address: 0204_H

Request Source Mode Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0						LDEV	CLRPND	REQGT	0	LDM	SCAN	ENSI	ENTR	ENGT	
r						w	w	rh	r	rw	rw	rw	rw	rw	

Field	Bits	Type	Description
ENGT	1:0	rw	**Enable Gate** Selects the gating functionality for source 1. 00_B No conversion requests are issued 01_B Conversion requests are issued if at least one pending bit is set 10_B Conversion requests are issued if at least one pending bit is set and REQGTx = 1. 11_B Conversion requests are issued if at least one pending bit is set and REQGTx = 0. *Note: REQGTx is the selected gating signal.*
ENTR	2	rw	**Enable External Trigger** 0_B External trigger disabled 1_B The selected edge at the selected trigger input signal REQTR generates the load event
ENSI	3	rw	**Enable Source Interrupt** 0_B No request source interrupt 1_B A request source interrupt is generated upon a request source event (last pending conversion is finished)

(continued)

Field	Bits	Type	Description
SCAN	4	rw	**Autoscan Enable** 0_B No autoscan 1_B Autoscan functionality enabled: a request source event automatically generates a load event
LDM	5	rw	**Autoscan Source Load Event Mode** 0_B Overwrite mode: Copy all bits from the select registers to the pending registers upon a load event 1_B Combine mode: Set all pending bits that are set in the select registers upon a load event (logic OR)
0	6	r	**Reserved, write 0, read as 0**
REQGT	7	rh	**Request Gate Level** Monitors the level at the selected REQGT input. 0_B The gate input is low 1_B The gate input is high
CLRPND	8	w	**Clear Pending Bits** 0_B No action 1_B The bits in registers BRSPNDx are cleared
LDEV	9	w	**Generate Load Event** 0_B No action 1_B A load event is generated
0	31:10	r	**Reserved, write 0, read as 0**

22.6.4.3 Register BRSSEL

The Channel Select Registers select the channels to be converted by the request source. Its bits are used to update the pending registers, when a load event occurs.

The number of valid channel bits depends on the channels available in the respective product type (please refer to ***Product-Specific Configuration*** on page 819).

BRSSEL Address: 0180_H

Request Source Channel Select Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								CHSELGy (y=0-7)							
r								rwh							

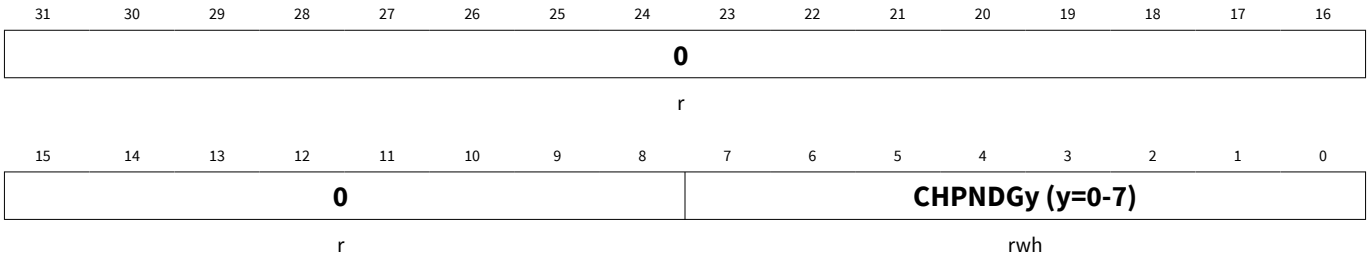
Field	Bits	Type	Description
CHSELGy (y=0-7)	y	rwh	**Channel Selection** Each bit (when set) enables the corresponding input channel to take part in the background scan sequence. 0_B Ignore this channel 1_B This channel is part of the scan sequence
0	31:8	r	**Reserved, write 0, read as 0**

22.6.4.4 Register BRSPND

The Channel Pending Registers indicate the channels to be converted in the current conversion sequence. They are updated from the select registers, when a load event occurs.

BRSPND Address: $01C0_H$

Request Source Pending Register Reset Value: $0000\ 0000_H$



Field	Bits	Type	Description
CHPNDGy (y=0-7)	y	rwh	**Channels Pending** Each bit (when set) request the conversion of the corresponding input channel. 0_B Ignore this channel 1_B Request conversion of this channel
0	31:8	r	**Reserved, write 0, read as 0**

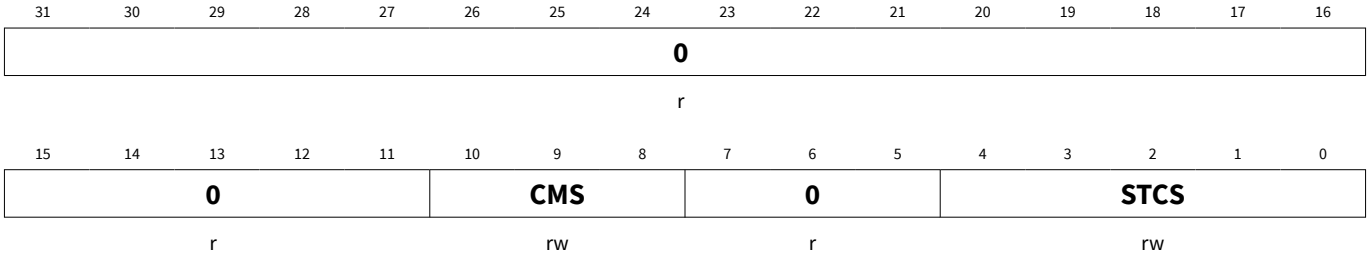
Note: Writing to any of registers BRSPND automatically updates the corresponding register BRSSEL and generates a load event that copies all bits from all registers BRSSEL to BRSPND. Use this shortcut only when writing the last word of the request pattern.

22.6.5 Channel Control Registers

22.6.5.1 Register GLOBICLASS

GLOBICLASS Address: $00A0_H$

Input Class Register Reset Value: $0000\ 0000_H$



Field	Bits	Type	Description
STCS	4:0	rw	**Sample Time Control for Standard Conversions** Number of additional clock cycles to be added to the minimum sample phase of 2 analog clock cycles: Coding and resulting sample time see ***Table 276***.
0	7:5	r	**Reserved, write 0, read as 0**
CMS	10:8	rw	**Conversion Mode for Standard Conversions** 000_B 12-bit conversion 001_B 10-bit conversion 010_B 8-bit conversion 011_B Reserved 100_B Reserved 101_B 10-bit fast compare mode 110_B Reserved 111_B Reserved
0	31:11	r	**Reserved, write 0, read as 0**

Table 276 Sample Time Coding

STCS	Additional Clock Cycles	Sample Time
$0\ 0000_B$	0	2 / f_{ADCI}
$0\ 0001_B$	1	3 / f_{ADCI}
…	…	…
$0\ 1111_B$	15	17 / f_{ADCI}
$1\ 0000_B$	16	18 / f_{ADCI}
$1\ 0001_B$	32	34 / f_{ADCI}
…	…	…
$1\ 1110_B$	240	242 / f_{ADCI}
$1\ 1111_B$	256	258 / f_{ADCI}

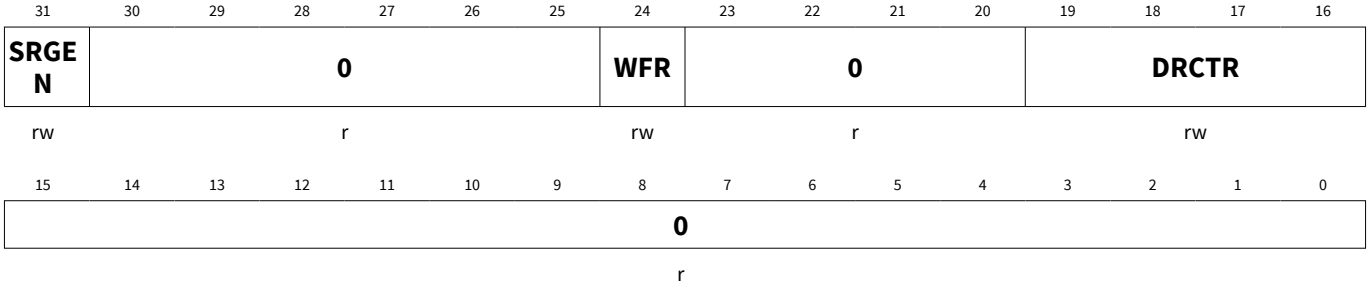
22.6.6 Result Register

22.6.6.1 Register GLOBRCR

The result control register selects the behavior of the result register.

GLOBRCR Address: 0280_H

Result Control Register Reset Value: $0100\ 0000_H$



Field	Bits	Type	Description
0	15:0	r	**Reserved, write 0, read as 0**
DRCTR	19:16	rw	**Data Reduction Control** Defines how result values are stored/accumulated in this register for the final result. The data reduction counter DRC can be loaded from this bitfield. 0000_B Data reduction disabled 0001_B Accumulate 2 result values 0010_B Accumulate 3 result values 0011_B Accumulate 4 result values others: Reserved
0	23:20	r	**Reserved, write 0, read as 0**
WFR	24	rw	**Wait-for-Read Mode Enable** 0_B Overwrite mode 1_B Wait-for-read mode enabled for this register
0	30:25	r	**Reserved, write 0, read as 0**
SRGEN	31	rw	**Service Request Generation Enable** 0_B No service request 1_B Service request after a result event

22.6.6.2 Register GLOBRES

The result register provides a common storage location for all channels of all groups.

GLOBRES Address: 0300_H

Result Register, Application view Reset Value: $0000\ 0000_H$

GLOBRESD Address: 0380_H

Result Register, Debug view Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VF	**FCR**	**1**	**0**				**CHNR**					**0**			
rwh	rh	r	r				rh					r			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESULT															
rwh															

Field	Bits	Type	Description
RESULT	15:0	rwh	**Result of most recent conversion** The position of the result bits within this bitfield depends on the configured operating mode.[62] Please, refer to ***Chapter 22.4.1.1***.
0	19:16	r	Reserved, read as 0
CHNR	24:20	rh	**Channel Number** Indicates the channel number corresponding to the value in bitfield RESULT.
0	28:25	r	**Reserved, read as 0**
1	29	r	**Reserved, read as 1**
FCR	30	rh	**Fast Compare Result** Indicates the result of an operation in Fast Compare Mode. 0_B Signal level was below compare value 1_B Signal level was above compare value
VF	31	rwh	**Valid Flag** Indicates a new result in bitfield RESULT or bit FCR. 0_B Read access: No new valid data available Write access: No effect 1_B Read access: Bitfield RESULT contains valid data and has not yet been read, or bit FCR has been updated Write access: Clear this valid flag and the data reduction counter (overrides a hardware set action)[62]

22.6.7 Gain Control Register

22.6.7.1 Register SHS0_GNCTR

The gain control register GNCTR selects the gain level for each input.

SHS0_GNCTR Address: $4803\ 4180_H$

Gain Control Register Reset Value: $0000\ 0000_H$

62 Only writable in register GLOBRES, not in register GLOBRESD.

22 Analog-to-Digital Converter (ADC)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GAIN7				**GAIN6**				**GAIN5**				**GAIN4**			
rw				rw				rw				rw			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GAIN3				**GAIN2**				**GAIN1**				**GAIN0**			
rw				rw				rw				rw			

Field	Bits	Type	Description
GAINx (x=0-7)	x*4+3:x*4	rw	**Gain Control Channel x** 0000_B Gain factor = 1 0001_B Gain factor = 3 0010_B Gain factor = 6 0011_B Gain factor = 12 Others: Reserved

22.6.8 Miscellaneous Registers

22.6.8.1 Register SHS0_LOOP

The sigma-delta-loop control register LOOP configures the functionality of the sigma-delta-loop(s).

SHS0_LOOP Address: $4803\ 4050_H$

Loop Control Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LPEN1	**0**										**LPCH1**				
rw	r										rw				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LPEN0	**0**										**LPCH0**				
rw	r										rw				

Field	Bits	Type	Description
LPCH0	4:0	rw	**Loop 0 Channel** Selects the input channel, for which this sigma-delta-loop function shall be enabled.
0	14:5	r	**Reserved, write 0, read as 0**
LPEN0	15	rw	**Loop 0 Enable** 0_H Off: standard operation 1_H ON: sigma-delta-loop is active
LPCH1	20:16	rw	**Loop 1 Channel** Selects the input channel, for which this sigma-delta-loop function shall be enabled.
0	30:21	r	**Reserved, write 0, read as 0**
LPEN1	31	rw	**Loop 1 Enable** 0_H Off: standard operation 1_H ON: sigma-delta-loop is active

22.6.9 Service Request Registers

22.6.9.1 Register GLOBEFLAG

GLOBEFLAG Address: $00E0_H$

Event Flag Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0							**REVGLBCLR**	**0**							**SEVGLBCLR**
r							w	r							w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0							**REVGLB**	**0**							**SEVGLB**
r							rwh	r							rwh

Field	Bits	Type	Description
SEVGLB	0	rwh	**Source Event** 0_B No source event 1_B A source event has occurred
0	7:1	r	**Reserved, write 0, read as 0**
REVGLB	8	rwh	**Result Event** 0_B No result event 1_B New result was stored in register GLOBRES
0	15:9	r	**Reserved, write 0, read as 0**
SEVGLBCLR	16	w	**Clear Source Event** 0_B No action 1_B Clear the source event flag SEVGLB
0	23:17	r	**Reserved, write 0, read as 0**
REVGLBCLR	24	w	**Clear Result Event** 0_B No action 1_B Clear the result event flag REVGLB
0	31:25	r	**Reserved, write 0, read as 0**

Note: Software can set flags REVGLB and SEVGLB and trigger the corresponding event by writing 1 to the respective bit. Writing 0 has no effect. Software can clear these flags by writing 1 to bit REVGLBCLR and SECGLBCLR, respectively. Setting both bits (e.g. SEVGLB and SEVGLBCLR) simultaneously clears the corresponding flag (e.g. SEVGLB).

22.6.9.2 Register GLOBEVNP

GLOBEVNP Address: 0140_H

Event Node Pointer Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0												**REV0NP**			
r												rw			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0												**SEV0NP**			
r												rw			

Field	Bits	Type	Description
SEV0NP	3:0	rw	**Service Request Node Pointer Source Event** Routes the corresponding event trigger to one of the service request lines (nodes). 0000_B Select shared service request line 0 of common service request group 0 0011_B Select shared service request line 3 of common service request group 0 …others: Reserved *Note: For shared service request lines see **Table 278**.*
0	15:4	r	**Reserved, write 0, read as 0**
REV0NP	19:16	rw	**Service Request Node Pointer Result Event** Routes the corresponding event trigger to one of the service request lines (nodes). 0000_B Select shared service request line 0 of common service request group 0 0011_B Select shared service request line 3 of common service request group 0 …others: Reserved *Note: For shared service request lines see **Table 278**.*
0	31:20	r	**Reserved, write 0, read as 0**

22.7 Interconnects

This section describes the actual implementation of the VADC module into the IMC300A, i.e. the incorporation into the microcontroller system.

22.7.1 Product-Specific Configuration

The functional description describes the features and operating modes of the A/D Converters in a general way. This section summarizes the configuration that is available in this product (IMC300A).

22.7.2 Analog Module Connections in the IMC300A

The VADC module accepts a number of analog input signals. The analog input multiplexers select the input channels from the signals available in this product.

The exact number of analog input channels and the available connection to port pins depend on the employed product type. A summary of channels enclosing all versions of the IMC300A can be found in ***Table 277***.

Table 277 Analog Connections in the IMC300A

Signal	Dir.	Source/Destin.	Description
Reference Voltage Pins			
V_{AREF}	I	VDD	positive analog reference
V_{AGND}	I	VSS	negative analog reference
Analog Input Channels			
CH0	I	P2.6	analog input channel 0
CH1	I	P2.8	analog input channel 1
CH3	I	P2.10	analog input channel 3
CH4	I	P2.11	analog input channel 4
CH5	I	P2.0	analog input channel 5
CH6	I	P2.1	analog input channel 6
CH7	I	P2.2	analog input channel 7

22.7.3 Digital Module Connections in the IMC300A

The VADC module accepts a number of digital input signals and generates a number of output signals. This section summarizes the connection of these signals to other on-chip modules or to external resources via port pins.

Note: The control bitfields for triggers and gates select the corresponding multiplexer input. Values 0000_B … 1111_B select inputs with suffix -A … -P.

Table 278 Digital Connections in the IMC300A

Signal	Dir.	Source/Destination	Description
Gate Inputs			
BGREQGTA	I	CCU40.ST3	Gating input A (GTSEL = 0000_B)
BGREQGTB	I	CCU40.ST2	Gating input B (GTSEL = 0001_B)
BGREQGTC	I	CCU40.ST1	Gating input C (GTSEL = 0010_B)
BGREQGTD	I	CCU40.ST0	Gating input D (GTSEL = 0011_B)
BGREQGTE	I	0	Gating input E (GTSEL = 0100_B)
BGREQGTF	I	0	Gating input F (GTSEL = 0101_B)
BGREQGTG	I	CCU41.ST0	Gating input G (GTSEL = 0110_B)
BGREQGTH	I	0	Gating input H (GTSEL = 0111_B)
BGREQGTI	I	0	Gating input I (GTSEL = 1000_B)
BGREQGTJ	I	0	Gating input J (GTSEL = 1001_B)
BGREQGTK	I	ERU0.PDOUT2	Gating input K (GTSEL = 1010_B)
BGREQGTL	I	ERU0.PDOUT3	Gating input L (GTSEL = 1011_B)
BGREQGTM	I	0	Gating input M (GTSEL = 1100_B)
BGREQGTN	I	0	Gating input N (GTSEL = 1101_B)
BGREQGTO	I	ERU0.PDOUT0	Gating input O (GTSEL = 1110_B)
BGREQGTP	I	ERU0.PDOUT1	Gating input P (GTSEL = 1111_B)
BGREQGTSEL	O	BGREQTRP[63]	Selected gating signal
Trigger Inputs			
BGREQTRA	I	CCU40.SR2	Trigger input A (XTSEL = 0000_B)
BGREQTRB	I	CCU40.SR3	Trigger input B (XTSEL = 0001_B)
BGREQTRC	I	CCU41.SR2	Trigger input C (XTSEL = 0010_B)
BGREQTRD	I	CCU41.SR3	Trigger input D (XTSEL = 0011_B)
BGREQTRE	I	ERU1.IOUT0	Trigger input E (XTSEL = 0100_B)
BGREQTRF	I	0	Trigger input F (XTSEL = 0101_B)
BGREQTRG	I	ERU0.IOUT2	Trigger input G (XTSEL = 0110_B)
BGREQTRH	I	ERU0.IOUT3	Trigger input H (XTSEL = 0111_B)

63 Internal signal connection.

Table 278 Digital Connections in the IMC300A (continued)

Signal	Dir.	Source/Destination	Description
BGREQTRI	I	0	Trigger input I (XTSEL = 1000_B)
BGREQTRJ	I	0	Trigger input J (XTSEL = 1001_B)
BGREQTRK	I	0	Trigger input K (XTSEL = 1010_B)
BGREQTRL	I	0	Trigger input L (XTSEL = 1011_B)
BGREQTRM	I	ERU0.IOUT0	Trigger input M (XTSEL = 1100_B)
BGREQTRN	I	ERU0.IOUT1	Trigger input N (XTSEL = 1101_B)
BGREQTRO	I	0	Trigger input O (XTSEL = 1110_B)
BGREQTRP	I	BGREQGTSEL[63]	Extend triggers to selected gating input (XTSEL = 1111_B)
System-Internal Connections			
SR0	O	NVIC (15)	Service request 0
SR1	O	NVIC (16)	Service request 1
SR2	O	ERU0.OGU02 ERU0.OGU12	Service request 2
SR3	O	ERU0.OGU22 ERU0.OGU32	Service request 3

63 Internal signal connection.

23 Analog Comparator (ACMP) and Out of Range Comparator (ORC)

This chapter describes the controls for analog comparator (ACMP) and out of range comparator (ORC).

23.1 Overview

This section gives an overview about the feature set of the Analog comparator and the Out of Range Comparator. In IMC300A, there are multiple Analog Comparators (ACMPx [x=1 and 2]) and Out of Range Comparators (ORCx [x=0,4,6,7]).

23.1.1 Features

The following features are provided:

- Out of Range Comparator (ORC)
  - Over-voltage monitoring for the analog input pins of the ADC module
- Analog Comparator (ACMP)
  - Monitor external voltage level
  - Selectable low power mode
  - Inverted ouput option

23.2 Analog Comparator (ACMP)

Figure 268 shows the block diagram of a Analog Comparator unit.

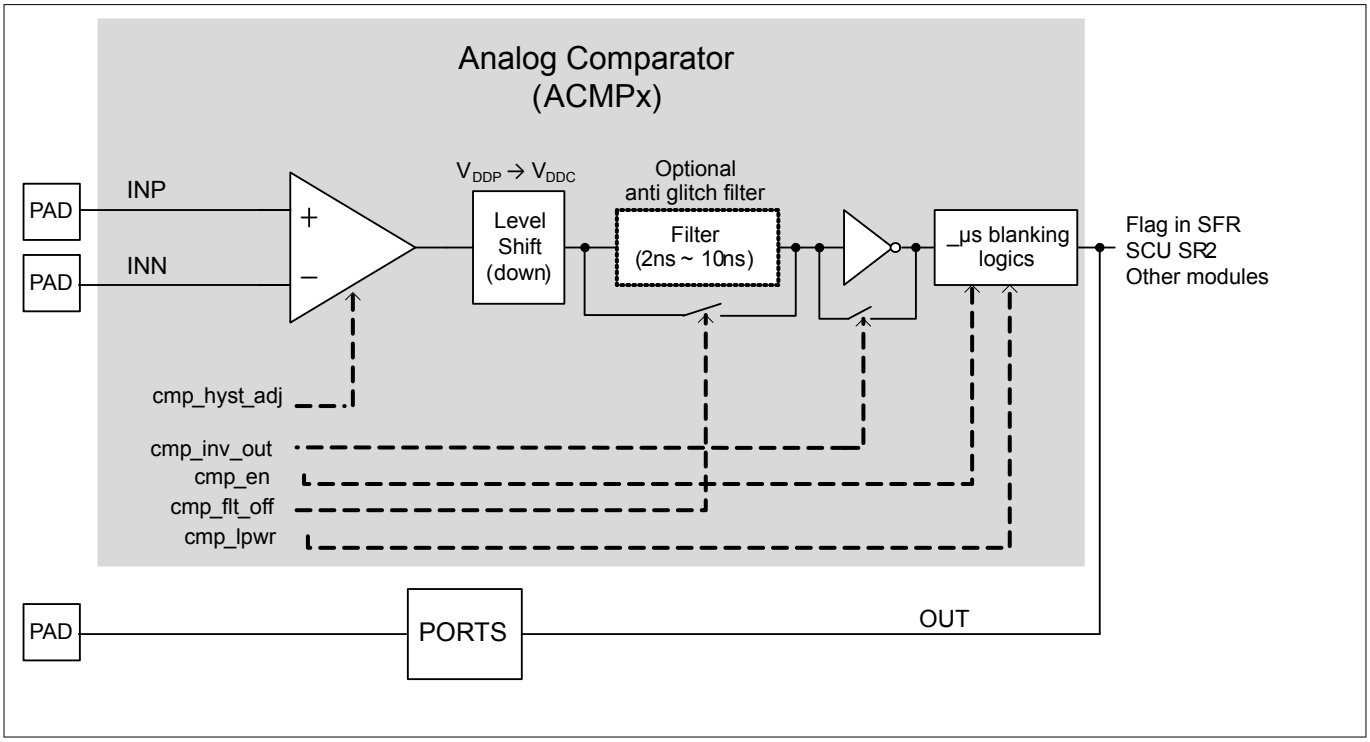


Figure 268 Block diagram of Analog Comparator

Input INP is compared with input INN in the pad voltage domain. The digital comparator output signal is shifted down from V_{DDP} power supply voltage level to V_{DDC} core voltage level. A filter (if enabled) absorbs generated spikes and can be controlled via bit ANACMPx.CMP_FLT_OFF. To prevent undefined states immediately after comparator enabling, a blanking module is added to ensure a stable output during transition state. The

blanking time is in a range of few usec. With the help of bit ANACMPx.CMP_INV_OUT, the comparator output is inverted. The output of the comparator could be used to wake-up the system from power save mode. It can also be observed from a pin.

The analog comparator can be switched off via bit CMP_EN bit in the ANACMPx register to save power.

Divided Reference Voltage

A resistor chain (in the order of 500kOhm) divides the reference voltage value from ACMP.REF input if bit ANACMP1.REF_DIV_EN is set. According to ***Figure 269***, the divided voltage is delivered to pin ACMP1.INP. With bit ANACMP0.ACMP0_SEL , ANACMP2.ACMP2_SEL and ANACMP3.ACMP3_SEL all other comparators can be supplied by this divided reference voltage.

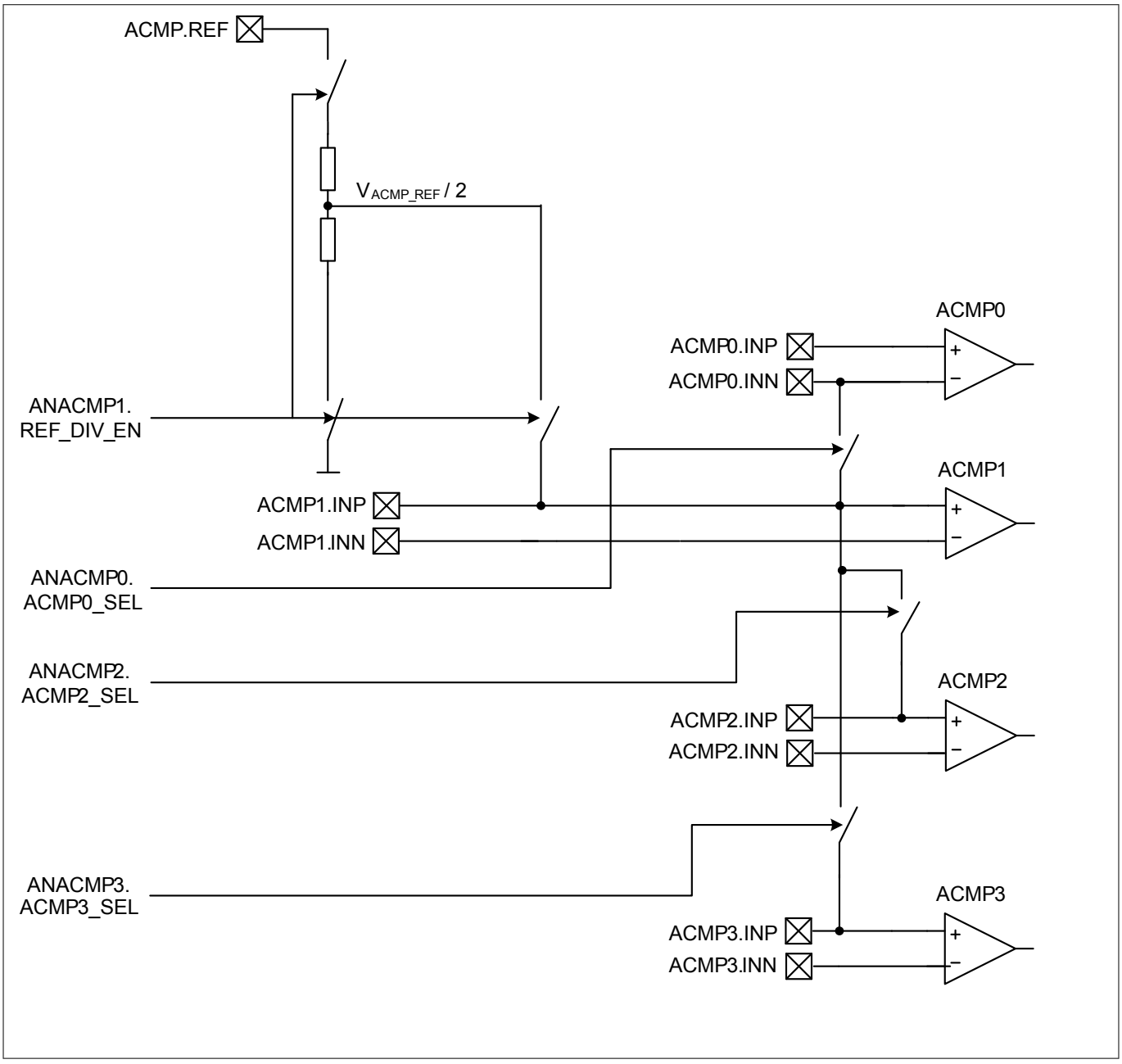


Figure 269 Analog Comparator Reference Divider Function

Low Power Mode

A low power state helps to reduce the total power consumption e.g. during sleep mode. It can be enabled by setting ANACMPx.LPWR to HIGH. In this mode, the analog comparators may shows a reduced performance. When switching back to normal mode, the blanking time applies to ensure a stable output.

23.3 Out of Range Comparator (ORC)

Out of range comparator (ORC) is build into every ADC channel which will trigger other modules or an interrupt when voltage out of range condition occurs. This happens when voltage at the input channel rises to above V_{DDP} level or when the input channel falls to a voltage below V_{DDP} level.

The out of range comparator is connected to ERU0 modules. All out of range comparator events is assigned to one interrupt node.

Before using the out of range comparator, it has to be enabled by setting the bits at ***ORCCTRL***.ENORCx and configuring it to detect voltage higher or lower than V_{DDP} by setting bits ***ORCCTRL***.CNFx (See ***Figure 270***).

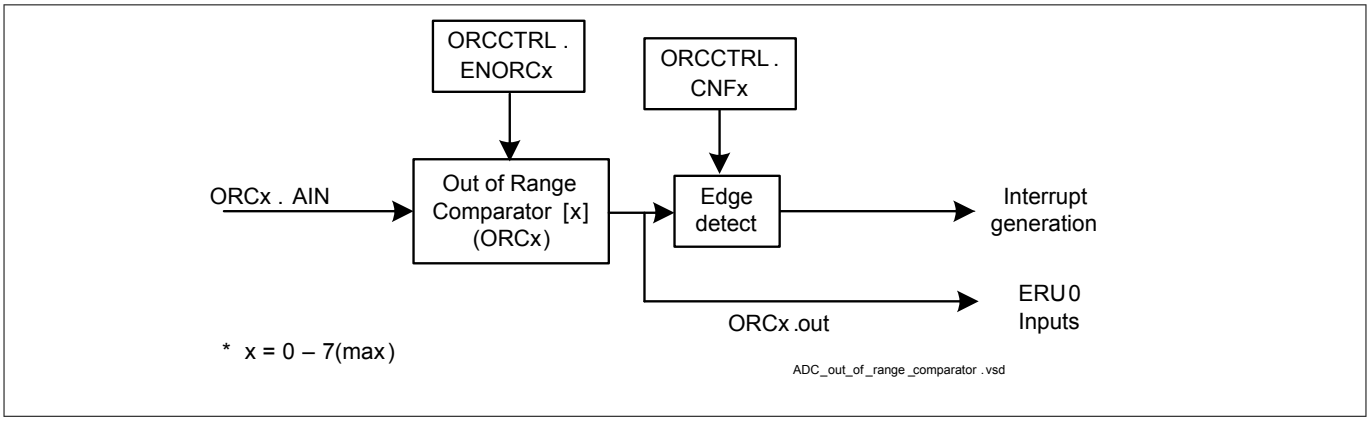


Figure 270 Out of range comparator

When a voltage out of range event occurs, the event sets an interrupt request through SCU.SR2 and triggers ERU0 through output of ORC (ORCx.out).

In IMC300A, ORCx.AIN[x=0,4,6,7] are connected to ports in the range of P2.2 - P2.9 respectively.

23.4 Service Request Generation

Both the ACMP and ORC has a service request output each. They are combined into a single output and connected to one of the interrupt node in the Nested Vectored Interrupt Controller (NVIC) via SCU.SR2.

The service request handling is part of the GCU block in SCU module. Refer to the “Service Request” description in the GCU section which is part of the SCU chapter for more details.

23.5 Debug Behavior

ACMPx and ORCx are not affected by the debug activities performed using external debug probe.

23.6 Registers

ACMP registers are accessible via the APB bus. ORC registers are accessible via the AHB bus. The absolute register address is calculated by adding:

Module Base Address + Offset Address

Following access to ACMP/ORC SFRs result in an AHB/APB error response:

- Read or write access to undefined address
- Write access to read-only registers

Table 279 Registers Address Space

Module	Base Address	End Address	Note
COMPARATOR	$4001\ 0000_H$	$4001\ FFFF_H$	System Control Unit Registers

Table 280 Registers Overview

Short Name	Description	Offset Addr.[64]	Access Mode		Description See
			Read	Write	
ORCx Registers					
ORCCTRL	Out of Range Comparator Control Register	0500_H	U, PV 32	U, PV 32	Page 825
ACMPx Registers					
ANACMP0	Analog Comparator 0 Control Register	$105C_H$	U, PV	U, PV	Page 826
ANACMP1	Analog Comparator 1 Control Register	1060_H	U, PV	U, PV	Page 827
ANACMP2	Analog Comparator 2 Control Register	1064_H	U, PV	U, PV	Page 828
ANACMP3	Analog Comparator 3 Control Register	1068_H	U, PV	U, PV	Page 829

23.6.1 ORC Register

23.6.1.1 Register ORCCTRL

This register enables the out of range comparator and selects the rising edge trigger or falling edge trigger for the flag register.

ORCCTRL Address: 0500_H

Out Of Range Comparator Control Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0								0	CNF6	0	CNF4	0	0	0	CNF0
r								r	rw	r	rw	r	r	r	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								0	ENORC6	0	ENORC4	0	0	0	ENORC0
r								r	rw	r	rw	r	r	r	rw

64 The absolute register address is calculated as follows: Module Base Address + Offset Address (shown in this column)

Field	Bits	Type	Description
ENORCx (x=0,4,6,7)	x	rw	**Enable Out of Range Comparator x** This bit defines if the out of range comparator is enabled in the corresponding analog input channel. 0_B Out of range comparator disabled. 1_B Out of range comparator enabled.
CNFx (x=0,4,6,7)	x+16	rw	**Out of Range Comparator Flag x** This bit selects CHx rising edge trigger or falling edge trigger for out of range comparator flag register. 0_B Falling edge trigger out of range event register. 1_B Rising edge trigger out of range event register.
0	15:8, 31:24	r	**Reserved** Read as 0; should be written with 0.

23.6.2 ACMP Registers

23.6.2.1 Register ANACMP0

ANACMP0 Address: $105C_H$

Analog Comparator 0 Control Register Reset Value: 0020_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP_OUT	**0**						**CMP_LPWR**	**0**	**ACMP0_SEL**	**CMP_HYST_ADJ**		**CMP_INV_OUT**	**0**	**CMP_FLT_OFF**	**CMP_EN**
rh	r						rw	r	rw	rw		rw	r	rw	rw

Field	Bits	Type	Description
CMP_EN	0	rw	**Comparator enable** 0_B CMP_DIS, Comparator is disabled 1_B CMP_EN, Comparator is enabled
CMP_FLT_OFF	1	rw	**Disables comparator filter** If set, the comparator glitch-filter is switched off 0_B FIL_ON, filter is active 1_B FIL_OFF, filter is switched off (to prevent a filter delay)
CMP_INV_OUT	3	rw	**Inverted Comparator output** The comparator output is simply inverted 0_B INV_OFF, no inversion of comparator signal 1_B INV_ON, comparator signal is inverted

(continued)

Field	Bits	Type	Description
CMP_HYST_ADJ	5:4	rw	**Comparator hysteresis adjust** To reduce noise sensitivity a hysteresis voltage can be chosen. It can be switched off with writing 00_B HYS_OFF, Comparator hysteresis is switched off 01_B HYS1, Hysteresis_typ = 10mV 10_B HYS2, Hysteresis_typ = 15mV 11_B HYS3, Hysteresis_typ = 20mV
ACMP0_SEL	6	rw	**Connect ACMP0.INN to ACMP1.INP** An internal switch connects comparator pad ACMP0.INN with pad ACMP1.INP together. Only one of both input pad shall be driven by a voltage source. The time delay between both pads is caused by the impedance of the switch. When bit ANACMP1.REF_DIV_EN is set, the divided reference voltage is applied not ony to ACMP1.INP, but also to ACMP0.INN 0_B OFF, ACMP0.INN is not connected 1_B ON, ACMP0.INN is connected to ACMP1.INP
CMP_LPWR	8	rw	**Low Power Mode** If enabled, all three analog comparator units are set into low power mode. If the logic level of this bit is changed, the core has to blank the comparator output information a certain time. 0_B HPM, High Power Mode 1_B LPM, Low Power Mode
CMP_OUT	15	rh	**Comparator output monitor bit** This bit corresponds to the comparator output status 0_B OUT0, state “Vminus > Vplus” 1_B OUT1, state “Vminus < Vplus”
0	2, 7, 14:9	r	**Reserved** Read as 0; should be written with 0.

23.6.2.2 Register ANACMP1

ANACMP1 Address: 1060_H

Analog Comparator 1 Control Register Reset Value: 0020_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP_OUT	0								REF_DIV_EN	CMP_HYST_ADJ		CMP_INV_OUT	0	CMP_FLT_OFF	CMP_EN
rh	r								rw	rw		rw	r	rw	rw

Field	Bits	Type	Description
CMP_EN	0	rw	**Comparator enable** 0_B CMP_DIS, Comparator is disabled 1_B CMP_EN, Comparator is enabled
CMP_FLT_OFF	1	rw	**Disables comparator filter** If set, the comparator glitch-filter is switched off 0_B FIL_ON, filter is active 1_B FIL_OFF, filter is switched off (to prevent a filter delay)
CMP_INV_OUT	3	rw	**Inverted Comparator output** The comparator output is simply inverted 0_B INV_OFF, no inversion of comparator signal 1_B INV_ON, comparator signal is inverted
CMP_HYST_ADJ	5:4	rw	**Comparator hysteresis adjust** To reduce noise sensitivity a hysteresis voltage can be chosen. It can be switched off with writing 00_B HYS_OFF, Comparator hysteresis is switched off 01_B HYS1, Hysteresis_typ = 10mV 10_B HYS2, Hysteresis_typ = 15mV 11_B HYS3, Hysteresis_typ = 20mV
REF_DIV_EN	6	rw	**Resistor Divider is enabled and Reference Voltage is applied to ACMP1** The divider reference voltage is applied to the positive ACMP1 input 0_B OFF, no resistor is connected 1_B ON, the divider resistor is enabled and the voltage is applied to ACMP1.INP
CMP_OUT	15	rh	**Comparator output monitor bit** This bit corresponds to the comparator output status 0_B OUT0, state “Vminus > Vplus” 1_B OUT1, state “Vminus < Vplus”
0	2, 14:7	r	**Reserved** Read as 0; should be written with 0.

23.6.2.3 Register ANACMP2

ANACMP2 Address: 1064_H

Analog Comparator 2 Control Register Reset Value: 0020_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP_OUT	0								ACMP2_SEL	CMP_HYST_ADJ		CMP_INV_OUT	0	CMP_FLT_OFF	CMP_EN
rh	r								rw	rw		rw	r	rw	rw

Field	Bits	Type	Description
CMP_EN	0	rw	**Comparator enable** 0_B CMP_DIS, Comparator is disabled 1_B CMP_EN, Comparator is enabled
CMP_FLT_OFF	1	rw	**Disables comparator filter** If set, the comparator glitch-filter is switched off 0_B FIL_ON, filter is active 1_B FIL_OFF, filter is switched off (to prevent a filter delay)
CMP_INV_OUT	3	rw	**Inverted Comparator output** The comparator output is simply inverted 0_B INV_OFF, no inversion of comparator signal 1_B INV_ON, comparator signal is inverted
CMP_HYST_ADJ	5:4	rw	**Comparator hysteresis adjust** To reduce noise sensitivity a hysteresis voltage can be chosen. It can be switched off with writing 00_B HYS_OFF, Comparator hysteresis is switched off 01_B HYS1, Hysteresis_typ = 10mV 10_B HYS2, Hysteresis_typ = 15mV 11_B HYS3, Hysteresis_typ = 20mV
ACMP2_SEL	6	rw	**Connect ACMP2.INP to ACMP1.INP** An internal switch connects comparator pad ACMP2.INP with pad ACMP1.INP together. Only one of both input pad shall be driven by a voltage source. The time delay between both pads is caused by the impedance of the switch. When bit ANACMP1.REF_DIV_EN is set, the divided reference voltage is applied not ony to ACMP1.INP, but also to ACMP2.INP 0_B OFF, ACMP2.INP is not connected 1_B ON, ACMP2.INP is connected to ACMP1.INP
CMP_OUT	15	rh	**Comparator output monitor bit** This bit corresponds to the comparator output status 0_B OUT0, state “Vminus > Vplus” 1_B OUT1, state “Vminus < Vplus”
0	2, 14:7	r	**Reserved** Read as 0; should be written with 0.

23.6.2.4 Register ANACMP3

ANACMP3 Address: 1068_H

Analog Comparator 3 Control Register Reset Value: 0020_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP_OUT	0								ACMP3_SEL	CMP_HYST_ADJ		CMP_INV_OUT	0	CMP_FLT_OFF	CMP_EN
rh	r								rw	rw		rw	r	rw	rw

Field	Bits	Type	Description
CMP_EN	0	rw	**Comparator enable** 0_B CMP_DIS, Comparator is disabled 1_B CMP_EN, Comparator is enabled
CMP_FLT_OFF	1	rw	**Disables comparator filter** If set, the comparator glitch-filter is switched off 0_B FIL_ON, filter is active 1_B FIL_OFF, filter is switched off (to prevent a filter delay)
CMP_INV_OUT	3	rw	**Inverted Comparator output** The comparator output is simply inverted 0_B INV_OFF, no inversion of comparator signal 1_B INV_ON, comparator signal is inverted
CMP_HYST_ADJ	5:4	rw	**Comparator hysteresis adjust** To reduce noise sensitivity a hysteresis voltage can be chosen. It can be switched off with writing 00_B HYS_OFF, Comparator hysteresis is switched off 01_B HYS1, Hysteresis_typ = 10mV 10_B HYS2, Hysteresis_typ = 15mV 11_B HYS3, Hysteresis_typ = 20mV
ACMP3_SEL	6	rw	**Connect ACMP3.INP to ACMP1.INP** An internal switch connects comparator pad ACMP3.INP with pad ACMP1.INP together. Only one of both input pad shall be driven by a voltage source. The time delay between both pads is caused by the impedance of the switch. When bit ANACMP1.REF_DIV_EN is set, the divided reference voltage is applied not only to ACMP1.INP, but also to ACMP3.INP 0_B OFF, ACMP3.INP is not connected 1_B ON, ACMP3.INP is connected to ACMP1.INP
CMP_OUT	15	rh	**Comparator output monitor bit** This bit corresponds to the comparator output status 0_B OUT0, state “Vminus > Vplus” 1_B OUT1, state “Vminus < Vplus”
0	2, 14:7	r	**Reserved** Read as 0; should be written with 0.

23.7 Interconnects

ACMP and ORC are connected to the port pins, the ERU0, ERU1, CCH40, CCH41, , , and DAC0.

Table 281 Analog Comparator Pin Connections

Input/Output	I/O	Connected To	Description
ACMP0.INN	I	P2.8	“-” input of ACMP0
ACMP0.INP	I	P2.9	“+” input of ACMP0
ACMP1.INN	I	P2.6	“-” input of ACMP1
ACMP1.INP	I	P2.7	“+” input of ACMP1
ACMP2.INN	I	P2.2	“-” input of ACMP2
ACMP2.INP	I	P2.1	“+” input of ACMP2
ACMP3.INN	I	P2.12	“-” input of ACMP3
ACMP3.INP	I	P2.13	“+” input of ACMP3
ACMP.REF	I	P2.11	Reference input of ACMP
ACMP0.OUT	O	P0.10 P2.10 P4.3 ERU0.0A0 CCU40.IN0AS CCU40.IN3AR ERU1.3A0 CCU41.IN0AS CCU41.IN3AR	output of ACMP0
ACMP1.OUT	O	P1.0 P4.0 ERU0.1A0 CCU40.IN0AR CCU40.IN2AS ERU1.0A0 CCU41.IN0AR CCU41.IN2AS	output of ACMP1
ACMP2.OUT	O	P4.2 ERU0.2A0 DAC0.IN4 CCU40.IN1AS CCU40.IN2AR ERU1.2A0 CCU41.IN1AS CCU41.IN2AR	output of ACMP2

Table 281 Analog Comparator Pin Connections (continued)

Input/Output	I/O	Connected To	Description
ACMP3.OUT	O	P4.1 CCU40.IN1AR CCU40.IN3AS ERU1.1A0 CCU41.IN1AR CCU41.IN3AS	output of ACMP3

Table 282 Out of Range Comparator Pin Connections

Input/Output	I/O	Connected To	Description
ORC0.AIN	I	P2.2	analog input of ORC0
ORC4.AIN	I	P2.6	analog input of ORC4
ORC6.AIN	I	P2.8	analog input of ORC6
ORC0.OUT	O	ERU0.0B2	output of ORC0
ORC4.OUT	O	ERU0.2A2	output of ORC4
ORC6.OUT	O	ERU0.3B2	output of ORC6

24 Digital to Analog Converter (DAC)

The DAC of IMC300A is a sigma delta digital to analog converter that is capable of controlling multiple channels. A one-bit sigma-delta bit stream is provided for every channel that determines the output level. The module supports automatic control of the output level by adjusting the relative data value of selected channels using a linear ramp function.

24.1 Overview

The DAC in IMC300A contains 9 identical channels. Each channel can generate a one-bit flexible sigma-delta bit stream with a user-adjustable 12-bit average value. The bit stream is generated by a 12-bit sigma-delta modulator which requires low-pass filter on the outputs.

24.1.1 Features

The DAC provides the following functionality:

- 9 independent channels generating a 1-bit on-off signal each
- 12-bit channel data values
- Individual ramp function for each channel

24.2 Functional Description

Each channel can operate independently from the others. The target value can be processed by a ramp function which provides the set value for the sigma-delta modulator of each channel.

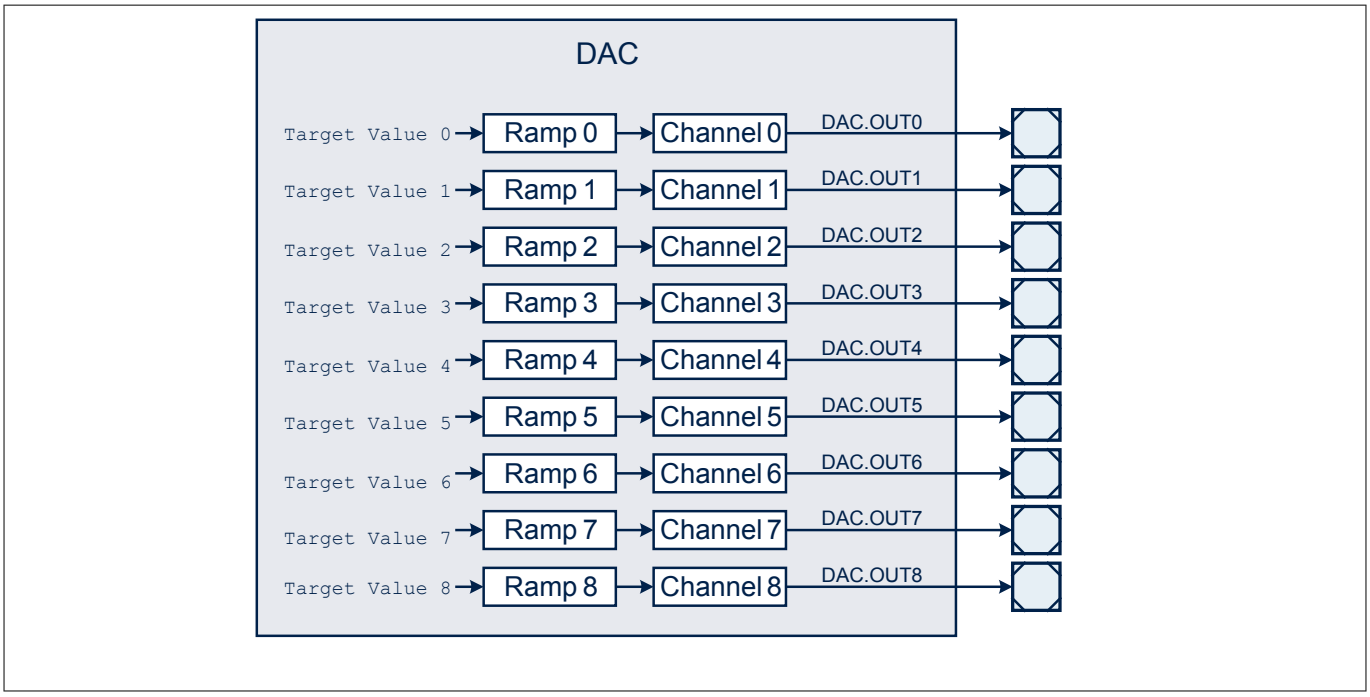


Figure 271 DAC Kernel Block Diagram

Every active channel has a 12-bit data value (DAC_***DATAy***.CHDATA) which represents the average level of the output bit stream.

It is recommended to select a high bit clock frequency by setting the fast clock prescaler (DAC_***GLOBCLK***.FCLK_PS) to a low value and by selecting fast mode (DAC_***GLOBCLK***.BCS to 1). The data values of the selected DAC channels must be enabled (DAC_***CHCONFIGy***.DEN is 1) and the flicker watchdog should be disabled (DAC_***CHCONFIGy***.WEN to 0).

24.2.1 RC Low-Pass Filter

Thesigma-delta bitstream must be averaged by an external low-pass filter. The DAC.OUTy signals of the port pins in push-pull configuration can directly drive the RC-filter. The output voltage can be used across the capacitor.

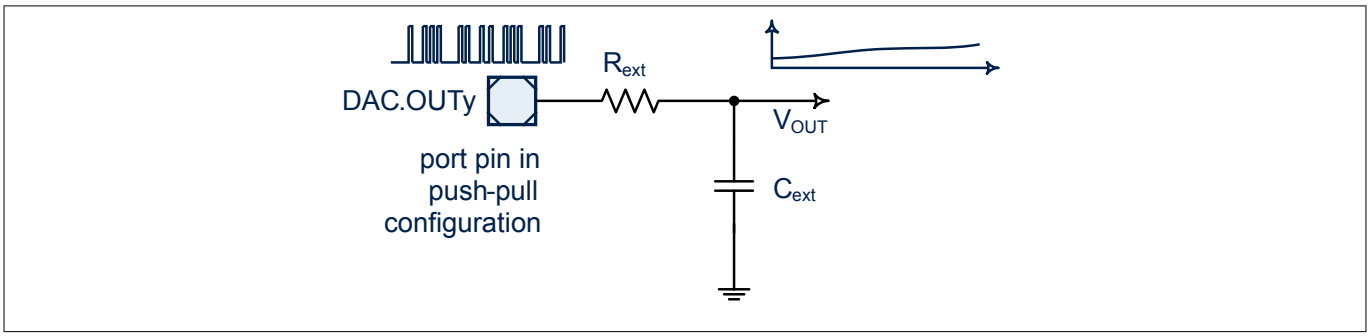


Figure 272 RC low-pass filter

24.2.2 Simple Low-Pass Filter

The pull devices of the pads can be used in combination with an external capacitor as a simple low-pass filter. The DAC.OUTy signals can control the pull devices of certain port pins. The ADC can be used to measure the voltage and compensate non-linearities of the pull devices by adjusting the data value accordingly.

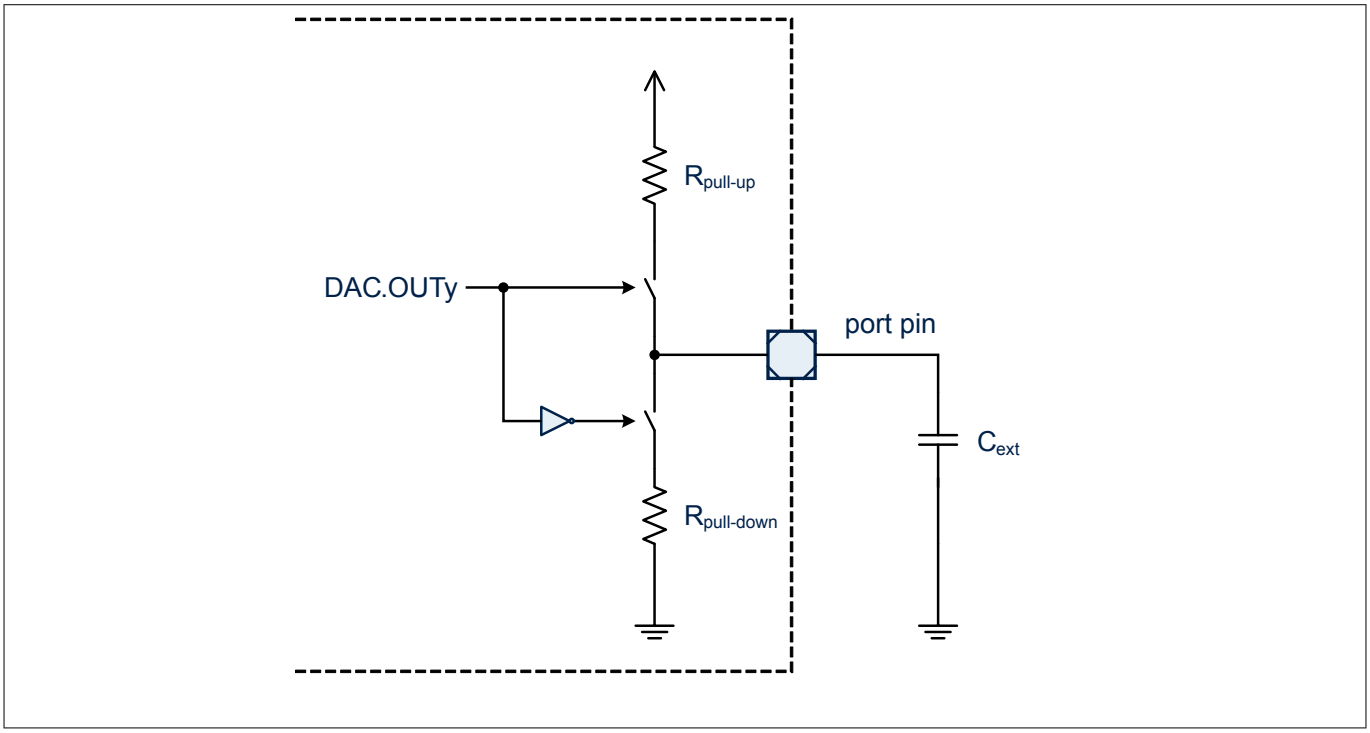


Figure 273 Simple low-pass filter on one pin

In this configuration, the user must ensure that the HW0 control path is selected for the port pins used. This can be done by setting the selected Pn_HWSEL.HWx bitfields to 01_B. Additionally, the used pads need to be enabled by resetting the respective bits in register P2_PDISC. This will configure the port pins as digital input pins and can still be used by other modules. One example is generating an analog voltage reference for the in-built analog comparator.

24.2.3 Sigma-Delta Modulator

The sigma-delta modulator oversamples the slowly changing 12-bit data signal and changes it into a high bitrate single-bit signal. The average analog value of the single-bit signal is directly proportional to the 12-bit data value. Low-pass filtering is required by an external analog filter.

The modulator contains a flicker watchdog which, if enabled, limits the number of consecutive off-bits (0) at the output. The maximum number of off-bits allowed is determined by DAC_***GLOBCON***.WDMBN. If the number of consecutive off-bits reaches this threshold, one on-bit (1) is inserted into the bitstream.

The minimum frequency of on bits is defined by the following formula:

$$f_{min} = \frac{1}{WDMBN} \times f_{DACbclk}$$

Equation 49

24.2.4 Ramp Function

The data value (DAC_***DATAy***.CHINT) can be changed using a ramp function. The transition time, aka ramp time, is user adjustable by programming the (DAC_***CHCONFIGy***.RAMP_PS) bitfield. Reaching the target data value (DAC_***DATASy***.TCHDATA) after shadow transfer (setting DAC_***CHSTRCON***.CHyS) will take the selected transition time which can be calculated by the following formula:

$$RAMPTIME = \frac{RAMP_PS \times 2^{13}}{f_{DACfclk}}$$

Equation 50

Once the ramping is done, DAC_***CHSTRCON***.CHyS is cleared by hardware. Setting DAC_***CHSTRCON***.CHyA will abort the ramp function and will clear DAC_***CHSTRCON***.CHyS.

DAC_***DATASy***.TCHDATA cannot be written while the ramp function is ongoing (DAC_***CHSTRCON***.CHyS is set). During this time, write accesses are ignored. The user either has to first wait until the ramp is finished or has to manually abort the ramp by setting DAC_***CHSTRCON***.CHyA.

If a ramp function was previously aborted, the subsequent ramp starts with a miniscule delay. The maximum delay is one linear clock (RAMP_PS * 1 fclk cycle).

If DAC_***CHCONFIGy***.RAMP_PS is 0, the data value will be the same as the target data value on shadow transfer, which means that the ramp function is effectively bypassed.

24.3 Power, Reset and Clock

DAC is located in the core power domain. The module, including all registers other than the bit field DAC_***GLOBCON***.SUSCFG, can be reset to its default state by a system reset. The bit field DAC_***GLOBCON***.SUSCFG is reset to its default value only by a debug reset.

*Note: In IMC300A, as there is no separate debug reset, the bit field DAC_**GLOBCON**.SUSCFG will be reset to its default state by a system reset.*

The DAC kernel is clocked (DAC_clk) and accessible on the peripheral bus frequency (PCLK). Two main clocks are generated for the different blocks in the module:

- DAC_bclk (bit clock) is the clock that determines the sampling rate of the sigma-delta converter and the bit time of the signal it generates. Depending on DAC_***GLOBCLK***.BCS, DAC_bclk is generated from DAC_fclk via a 4 divider or it is the same as DAC_fclk.
- DAC_fclk (fast clock) is used by the Trigger Control block to generate the trigger delay. It is generated from DAC_clk by a prescaler. The frequency can be set by DAC_***GLOBCLK***.FCLK_PS.

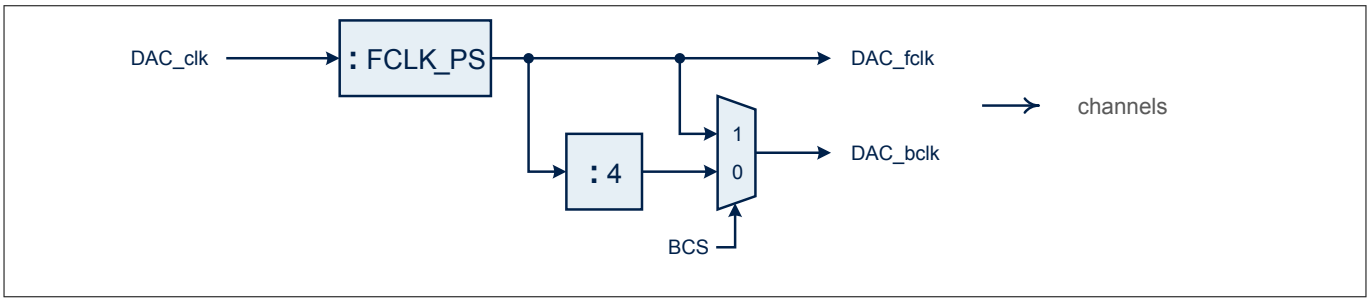


Figure 274 DAC clocks

The clock frequencies in normal mode can be calculated with the following formulas:

$$f_{fclk} = \frac{1}{FCLKPS} \times f_{clk}$$

Equation 51

$$f_{bclk} = \frac{1}{FCLKPS \times 4} \times f_{clk}$$

Equation 52

The kernel is only in operation in active mode.

24.4 Debug Behaviour

The clocks to all channels and other functional blocks are stopped in suspend mode. The registers can still be accessed by the CPU as read-only. This mode is useful for debugging purposes as the current device status is frozen to get a snapshot of the internal values. As the clocks are stopped, all counters and timers are stopped and frozen.

Mode of entry into suspend mode can be configured by changing the DAC_***GLOBCON***.SUSCFG bitfield.

When debug suspend is revoked, the kernel resumes operation according to latest SFR settings.

*Note: In IMC300A, bit field DAC_**GLOBCON**.SUSCFG is reset to its default value by any reset. If the suspend function is required during debugging, it is recommended that it is enabled in the user initialization code. Before programming the bit field, the module clock has to be enabled and special care needs to be taken while enabling the module clock as described in the CCU (Clock Gating Control) section of the SCU chapter.*

24.5 Initialization

The DAC registers are recommended to be programmed in a specific sequence.

1. Program Global Registers

- DAC_***GLOBCLK*** to set up the clocks
- DAC_***GLOBCON*** for general configuration

2. Program Channel Registers

- DAC_***CHCONFIGy*** for general channel configuration
- DAC_***CHEN*** to enable channels

3. Set target data values and start ramp function

- DAC_***CHCONFIGy***.RAMP_PS to set the ramp time
- DAC_***DATASy*** to set the target intensities
- DAC_***CHSTRCON*** to start ramp function
- When the rampings are finished, DAC_***CHSTRCON***.CHyS are cleared by hardware

24.6 Registers

All DAC registers (except bit field DAC_***GLOBCON***.SUSCFG) are reset by a system reset. Bit field DAC_***GLOBCON***.SUSCFG is reset by a debug reset.

Registers Overview

The absolute register address is calculated by adding:
Module Base Address + Offset Address

Table 283 Registers Address Space

Module	Base Address	End Address	Note
DAC	5003 0000$_H$	5003 FFFF$_H$	

Table 284 Register Overview

Short Name	Description	Offset Addr.	Access Mode		Description See
			Read	Write	
DAC Global Registers					
GLOBCON	Global Control Register	0000$_H$	U, PV, 32	U, PV, 32	Page ***837***
GLOBCLK	Global Clock Register	0004$_H$	U, PV, 32	U, PV, 32	Page ***838***
ID	Module Identification Register	0008$_H$	U, PV, 32	BE	Page ***839***
CHEN	Channel Enable Register	000C$_H$	U, PV, 32	U, PV, 32	Page ***840***
CHSTRCON	Channel Shadow Transfer Control Register	0018$_H$	U, PV, 32	U, PV, 32	Page ***840***
DAC Channel Registers					
DATASy	Channel Data Value Shadow Register y	003C$_H$+ y*0014$_H$	U, PV, 32	U, PV, 32	Page ***841***
DATAy	Channel Data Value Register y	0040$_H$+ y*0014$_H$	U, PV, 32	BE	Page ***841***
CHCONFIGy	Channel Configuration Register y	0044$_H$+ y*0014$_H$	U, PV, 32	U, PV, 32	Page ***842***

24.6.1 Global Registers

24.6.1.1 Register GLOBCON

GLOBCON Address: 0000$_H$
Global Control Reset Value: 0320 0000$_H$

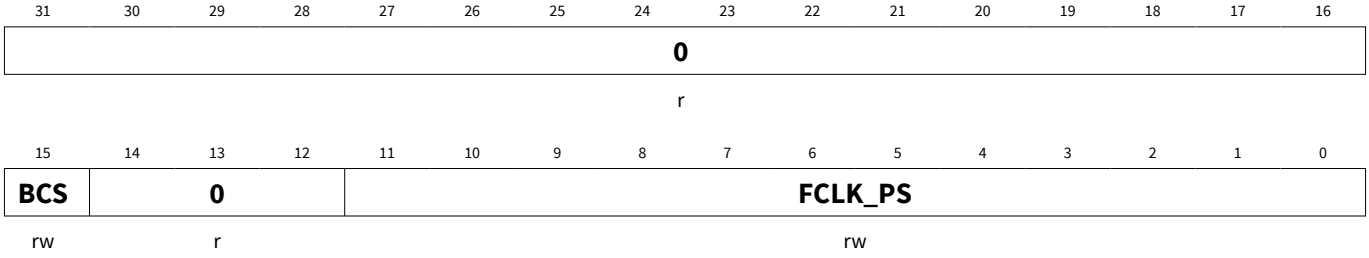


Field	Bits	Type	Description
0	3:0	r	**Reserved** Read as 0; should be written with 0.
SUSCFG	5:4	rw	**Suspend Mode Configuration** This bitfield determines how the DAC channels enter suspend mode. 00_B Suspend request is ignored and the module cannot get suspended 01_B All channels stop running immediately and freeze in the last state without any safe stop 10_B All channels stop running immediately and freeze in the last state; all outputs go to passive state to achieve safe stop 11_B Reserved
0	15:6	r	**Reserved** Read as 0; should be written with 0.
WDMBN	27:16	rw	**Watchdog Maximum Bitnumber** The maximum number of consecutive zeroes allowed at the output of the sigma-delta modulators
0	31:28	r	**Reserved** Read as 0; should be written with 0.

24.6.1.2 Register GLOBCLK

GLOBCLK Address: 0004_H

Global Clock Reset Value: $00DB\ 0190_H$



Field	Bits	Type	Description
FCLK_PS	11:0	rw	**Fast Clock Prescaler Factor** The constant clock input to the DAC is prescaled according to this value to generate DAC_fclk. DAC_bclk is generated from DAC_fclk by a division of 4. DAC_bclk determines the bit-time at the output of the sigma-delta modulators. 0_D No clock 1_D Divide by 1 ...
0	14:12	r	**Reserved** Read as 0; should be written with 0.
BCS	15	rw	**Bit-Clock Selector** 0_B Normal Mode: DAC_bclk is generated from DAC_fclk by a division of 4 1_B Fast Mode: DAC_bclk is the same as DAC_fclk
0	31:16	r	**Reserved** Read as 0; should be written with 0.

24.6.1.3 Register ID

ID Address: 0008_H

Module Identification Reset Value: $00F3\ C0XX_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MOD_NUMBER															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOD_TYPE0								MOD_REV							
r								r							

Field	Bits	Type	Description
MOD_REV	7:0	r	**Module Revision Number** MOD_REV defines the revision number. The value of a module revision starts with 01_H (first revision).
MOD_TYPE0	15:8	r	**Module Type** This bit field is $C0_H$. It defines the module as a 32-bit module.
MOD_NUMBER	31:16	r	**Module Number Value** This bit field defines the module identification number.

24.6.1.4 Register CHEN

CHEN Address: $000C_H$

Channel Enable Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0							ECH8	ECH7	ECH6	ECH5	ECH4	ECH3	ECH2	ECH1	ECH0
r							rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
ECHy (y=0-8)	y	rw	**Channel y Enable** 0_B Channel is disabled, the output level is passive; the ramp function and the Sigma-Delta Modulator are reset; all internal logic and DATAy are reset when the channel gets disabled 1_B Channel is enabled
0	31:9	r	**Reserved** Read as 0; should be written with 0.

24.6.1.5 Register CHSTRCON

CHSTRCON Address: 0018_H

Channel Shadow Transfer Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0							CH8A	CH7A	CH6A	CH5A	CH4A	CH3A	CH2A	CH1A	CH0A
r							w	w	w	w	w	w	w	w	w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0							CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
r							rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
CHyS (y=0-8)	y	rwh	**Channel y Shadow Transfer** 0_B No action 1_B Initiate channel y target data value shadow transfer. The ramping will start and channel y data value will start to change towards the target. Cleared by hardware when the ramping is complete and the target has been reached.
0	15:9	r	**Reserved** Read as 0; should be written with 0.

(continued)

Field	Bits	Type	Description
CHyA (y=0-8)	y+16	w	**Channel y Ramp Function Abort** 0_B No action 1_B Abort ramp function; CHyS is cleared, channel y data value stops changing Always read as 0
0	31:25	r	**Reserved** Read as 0; should be written with 0.

24.6.2 Channel Registers

There are 9 channels available on IMC300A. y denotes channel 0 through 8.

24.6.2.1 Register DATASy

DATASy (y=0-8) Address: $003C_H + y*0014_H$

Channel Data Shadow Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

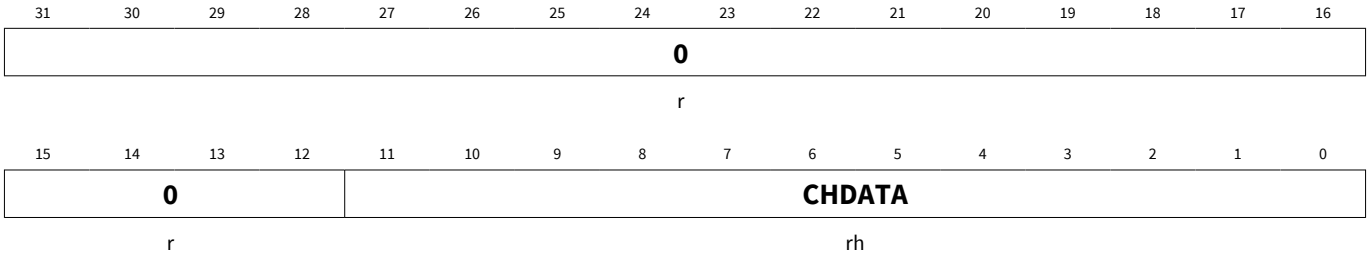
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				**TCHDATA**											
r				rw											

Field	Bits	Type	Description
TCHDATA	11:0	rw	**Target Channel Data Value** Can only be written if CHSTRCON.CHyS is not set, otherwise the new value will be ignored.
0	31:12	r	**Reserved** Read as 0; should be written with 0.

24.6.2.2 Register DATAy

DATAy (y=0-8) Address: $0040_H + y*0014_H$

Channel Data Value Reset Value: $0000\ 0000_H$

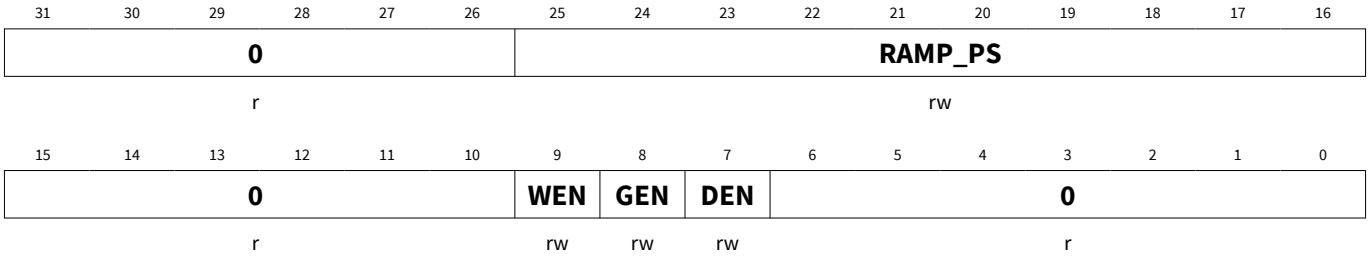


Field	Bits	Type	Description
CHDATA	11:0	rh	**Channel Data Value** Actual channel intensity.
0	31:12	r	**Reserved** Read as 0; should be written with 0.

24.6.2.3 Register CHCONFIGy

CHCONFIGy (y=0-8) Address: $0044_H + y*0014_H$

Channel Configuration Reset Value: $0000\ 0002_H$



Field	Bits	Type	Description
0	6:0	r	**Reserved** Read as 0; should be written with 0.
DEN	7	rw	**Data Value Enable** 0_B Channel data values are irgnored 1_B Channel data values are processed
GEN	8	rw	**Gating Enable** 0_B Gating function is disabled, the input signal (DAC.INy) has no effect 1_B Gating function is enabled, the output gating signal is DAC.INy
WEN	9	rw	**Flicker Watchdog Enable** 0_B The flicker watchdog is not used 1_B The flicker watchdog is active and limits the number of consecutive zeroes at the sigma-delta modulator output according to GLOBCON.WDMBN

(continued)

Field	Bits	Type	Description
0	15:10	r	**Reserved** Read as 0; should be written with 0.
RAMP_PS	25:16	rw	**Ramp Clock Prescaler** Determines how long it takes for the Channel Data Value to reach the Target Channel Data Value after shadow transfer (after CHSTRCON.CHyS is set). If this value is 0, then the data value will become the same as the target data value on shadow transfer.
0	31:26	r	**Reserved** Read as 0; should be written with 0.

24.7 Interconnects

DAC0 is connected to the ports, the ER, the analog comparator, the ADC, the NVIC, CCU4, the suspend signal and the kernel clock.

Table 285 DAC0 Pin Connections

Global Input/Output	I/O	Connected To	Description
DAC0.clk	I	PCLK	DAC kernel clock
DAC0.SUSPEND	I	CPU Halted	Suspend signal
DAC0.OUT0	O	P1.0; P4.0; P4.4; CCU40.IN0AQ; CCU80.IN0AI; CCU41.MCI0; CCU41.IN0AQ; P2.2.HW0 pull control;	Output of channel 0
DAC0.OUT1	O	CCU40.IN3AZ; CCU41.MCI1; CCU41.IN1AQ; P2.0.HW0 pull control; P2.8.HW0 pull control;	Output of channel 1
DAC0.OUT2	O	P4.6; CCU40.MCI0; CCU41.MCI2; CCU41.IN2AQ; P1.0.HW0 pull control; P2.6.HW0 pull control;	Output of channel 2

Table 285 DAC0 Pin Connections (continued)

Global Input/Output	I/O	Connected To	Description
DAC0.OUT3	O	CCU40.MCI1; CCU40.IN1AZ; CCU41.IN1AZ; P1.1.HW0 pull control;	Output of channel 3
DAC0.OUT4	O	P0.8; P4.2; CCU40.MCI2; CCU40.IN2AQ; P2.10.HW0 pull control;	Output of channel 4
DAC0.OUT5	O	P0.9; P4.3; P4.7; CCU40.MCI3; CCU40.IN3AQ; CCU41.MCI3; CCU41.IN3AQ; P2.11.HW0 pull control;	Output of channel 5
DAC0.OUT6	O	P0.10; P0.12; CCU40.IN0AZ; CCU41.IN0AZ; P1.4.HW0 pull control; P2.1.HW0 pull control;	Output of channel 6
DAC0.OUT7	O	P0.11; P0.14; CCU40.IN2AZ; CCU41.IN2AZ;	Output of channel 7
DAC0.OUT8	O	P0.15; P1.7; P4.1; P4.5; CCU40.IN1AQ; CCU41.IN3AZ;	Output of channel 8

25 Temperature Sensor (DTS)

This chapter describes the controls for Temperature Sensor (DTS).

25.1 General Description

The Temperature Sensor (DTS) generates a measurement result that represents the current temperature. The result of the measurement is displayed via bit field ANATSEMON.TSE_MON. The temperature sensor has to be enabled before it can be used via bit ANATSECTRL.TSE_EN.

The measurement result is ready when the SRRAW.TSE_DONE flag is set. An interrupt can be triggered when it is enabled via SRMSK.TSE_DONE bit. After the measurement is completed and result is stored in TSE_MON, temperature sensor continue with next measurement. Measurement are disabled when TSE_EN is cleared to 0. Hence, reading the TSE_MON value will provide you the latest temperature.

The temperature sensor is capable of generating interrupt requests when DTS temperature measurement in result crosses upper and/or lower threshold value configured in bit ANATSEIH.TSE_IH and ANATSEIL.TSE_IL respectively. Digital comparators are implemented to compare the actual measurement result against configured limits and triggers interrupt if the value fall outside of valid range. Result of comparison is shown as the SRRAW.TSE_HIGH and TSE_LOW flag.

25.2 Service Request Generation

The temperature sensor has a service request output for the TSE_DONE, TSE_HIGH and TSE_LOW event. They are combined with events from other modules into a single output and connected to one of the interrupt node in the Nested Vectored Interrupt Controller (NVIC) via SCU.SR1.

The service request handling is part of the GCU block in SCU module. Refer to the “Service Request” description in the GCU section which is part of the SCU chapter for more details.

25.3 Registers

DTS registers are accessible via the APB bus. The absolute register address is calculated by adding:

Module Base Address + Offset Address

Following access to DTS SFRs result in an AHB/APB error response:

- Read or write access to undefined address
- Write access to read-only registers

Table 286 Registers Address Space

Module	Base Address	End Address	Note
DTS	$4001\ 0000_H$	$4001\ FFFF_H$	System Control Unit Registers

Table 287 Registers Overview

Short Name	Description	Offset Addr.[65]	Access Mode		Description See
			Read	Write	
ANATSECTRL	Temperature Sensor Control Register	0024_H	U, PV	U, PV	Page 846

65 The absolute register address is calculated as follows: Module Base Address + Offset Address (shown in this column)

Table 287 Registers Overview (continued)

Short Name	Description	Offset Addr.[65]	Access Mode		Description See
			Read	Write	
ANATSEIH	Temperature Sensor High Interrupt Register	0030_H	U, PV	U, PV	Page 846
ANATSEIL	Temperature Sensor Low Interrupt Register	0034_H	U, PV	U, PV	Page 847
ANATSEMON	Temperature Sensor Counter2 Monitor Register	0040_H	U, PV	U, PV	Page 847

25.3.1 Register ANATSECTRL

ANATSECTRL Address: 1024_H

Temperature Sensor Control Register Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0															TSE_EN
r															rw

Field	Bits	Type	Description
TSE_EN	0	rw	**Temperature sensor enable** 0_B Temperature sensor is disabled 1_B Temperature sensor is switched on
0	15:1	r	**Reserved** Read as 0; should be written with 0.

25.3.2 Register ANATSEIH

ANATSEIH Address: 1030_H

Temperature Sensor High Temperature Interrupt Register Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSE_IH															
rw															

65 The absolute register address is calculated as follows: Module Base Address + Offset Address (shown in this column)

Field	Bits	Type	Description
TSE_IH	15:0	rw	**Counter value for high temperature interrupt** ANATSEIH value is compared with ANATSEMON (with the counter value) An high temperature interrupt is triggered if: ANATSE_MON < ANATSEIH The comparison result can be observed from SCU_SRRAW.TSE_HIGH

25.3.3 Register ANATSEIL

ANATSEIL Address: 1034_H

Temperature Sensor Low Temperature Interrupt Register Reset Value: $FFFF_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSE_IL															
rw															

Field	Bits	Type	Description
TSE_IL	15:0	rw	**Counter value for low temperature interrupt** ANATSEIL value is compared with ANATSEMON An low interrupt is triggered if: ANATSEMON > ANATSEIL The comparison result can be observed from SCU_SRRAW.TSE_LOW

25.3.4 Register ANATSEMON

ANATSEMON Address: 1040_H

Temperature Sensor Counter2 Monitor Register Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSE_MON															
rh															

Field	Bits	Type	Description
TSE_MON	15:0	rh	**Result values; loaded by TSE_DONE** After each measurement done event (indicated by a set in SCU_SRRAW.TSE_DONE bit), the result is stored in this register.

26 General Purpose I/O Ports (Ports)

The IMC300A has up to 56 digital General Purpose Input/Output (GPIO) port lines which are connected to the on-chip peripheral units.

26.1 Overview

The Ports provide a generic and very flexible software and hardware interface for all standard digital I/Os. Each Port slice has individual interfaces for the operation as General Purpose I/O and it further provides the connectivity to the on-chip periphery and the control for the pad characteristics. ***Table 288*** gives an overview of the available PORTS and other pins in the different packages of the IMC300A:

Table 288 Port/Pin Overview

Port	Note
P0	Standard bi-directional pad
P1	High current and Standard bi-directional pad
P2	Analog/Digital input and bi-directional pad
P3	Standard bi-directional pad
P4	Standard bi-directional pad
Supply VDD, ADC / ORC Reference Voltage	VDD
Supply GND, ADC Reference Ground	VSSP/VSS
I/O Port Supply	VDDP
I/O Port Ground	VSSP
Exposed Die Pad	Must be connected to common V_{SS}

26.1.1 Features

This is a list of the main features of the Ports:

- same generic register interface for each port pin, ***Chapter 26.8***
- simple and robust software access for general purpose I/O functionality, ***Chapter 26.2***
- direct input connections to on-chip peripherals, ***Chapter 26.2.1***
- dedicated hardware interface for DAC, CCU4, ACMP and USIC with select option, ***Chapter 26.3***
- defined power-up/power-fail behavior, ***Chapter 26.6***.
- up to nine alternate output paths from peripherals selectable, ***Chapter 26.8.1***
- programmable open-drain or push-pull output driver stage, ***Chapter 26.8.1***
- programmable weak pull-up and pull-down devices, ***Chapter 26.8.1***
- programmable input inverter, ***Chapter 26.8.1***
- programmable pad hysteresis, ***Chapter 26.8.2***
- disabling of digital input stage on shared analog inputs, ***Chapter 26.8.3***
- separate set and clear output control to avoid read-modify-write operations, ***Chapter 26.8.5***
- programmable power-save behavior in Deep-Sleep mode, ***Chapter 26.8.7***
- Privileged Mode restricted access to configuration registers to avoid accidential modification

26.1.2 Block Diagram

Below is a figure with the generic structure of a digital port pin, split into the port slice with the control logic and the pad with the pull devices and the input and output stages, ***Figure 275***.

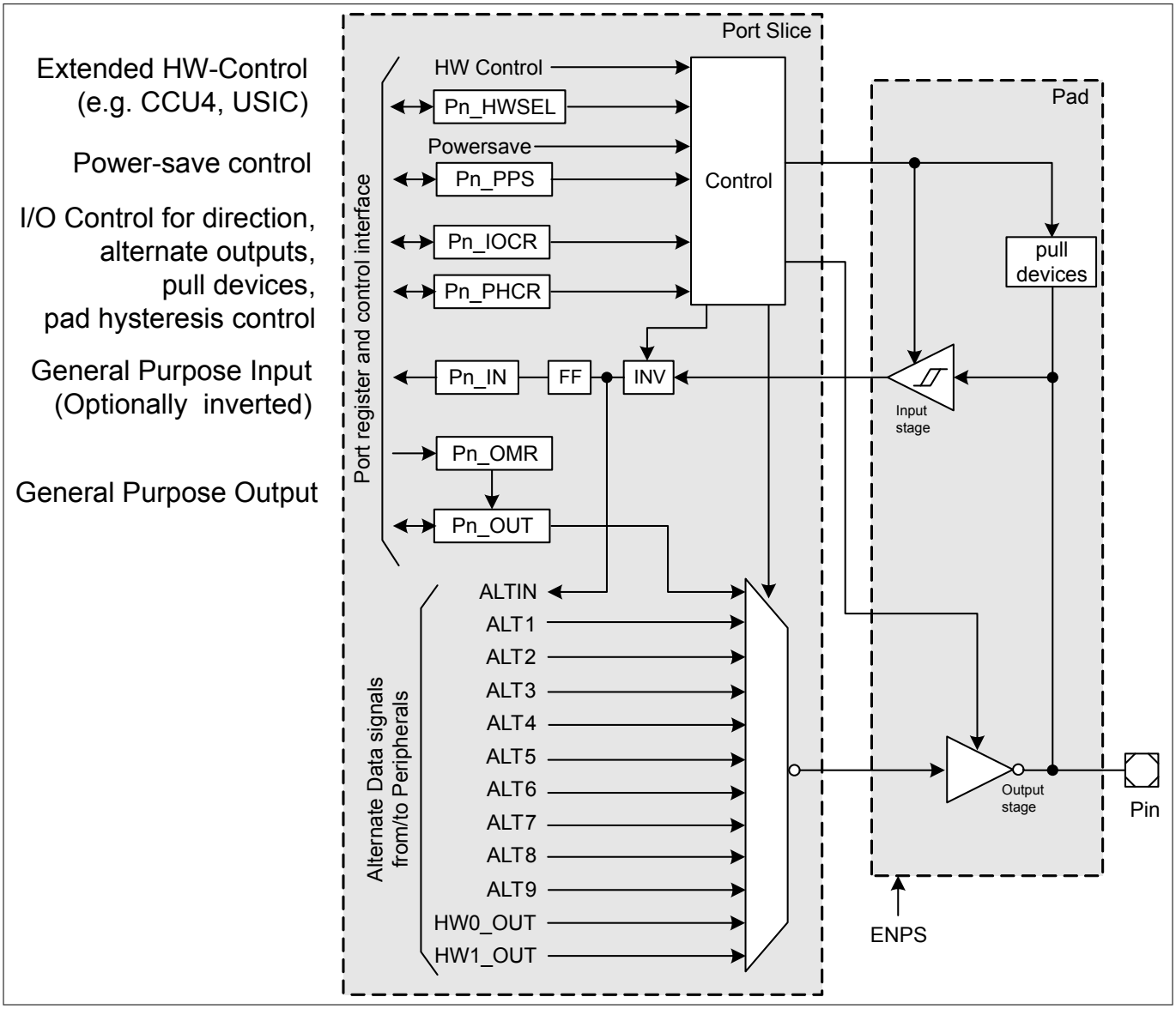


Figure 275 General Structure of a digital Port Pin

26.1.3 Definition of Terms

Some specific terms are used throughout this chapter:

Pin/Ball

External connection of the device to the PCB.

Dedicated Pin

A Pin with a dedicated function that is not under the control of the port logic (i.e. supply pins).

Port Pin

A pin under the control of the port logic (P0.1).

Port

A group of up to 16 Port Pins sharing the same generic register set (P0).

Port Slice

The “sum” of register bits and control logic used to control a port pin.

Pad

Analog component containing the output driver, pull devices and input Schmitt-Trigger. Also interfaces the internal logic operating on V_{DDC} to the pad supply domain V_{DDP}.

GPIO

General Purpose Input/Output. A port pin with the input and/or output function controlled by the application software.

Alternate Function

Direct connection of a port pin with an on-chip peripheral.

26.2 GPIO and Alternate Functions

The Ports can be operated as General Purpose Input/Output (GPIO) and with Alternate Functions of the on-chip periphery, configured by the Port Input/Output Control Register (Pn_IOCR, ***Chapter 26.8.1***). It selects between

- Direct or Inverted Input
  - with or without pull device
- Push-pull or Open-Drain Output driven by
  - Pn_OUT (GPIO)
  - selected peripheral output connections.

As GPIO the port pin is controlled by the application software, reading the input value by the Port Input register Pn_IN (***Chapter 26.8.6***) and/or defining the output value by the Output Modification Register Pn_OMR (***Chapter 26.8.5***). Output modification by Pn_OMR is preferred over the direct change of the output value with the Output register Pn_OUT (***Chapter 26.8.4***), as Pn_OMR allows the manipulation of individual port pins in a single access without “disturbing” other pins controlled by the same Pn_OUT register. If an application uses a GPIO as a bi-directional I/O line, register Pn_IOCR has to be written to switch between input and output functionality.

For the operation with Alternate Functions, the port pins are directly connected to input or output functions of the on-chip periphery. This allows the peripheral to directly evaluate the input value or drive the output value of the port pin without further application software interaction after the initial configuration. The connection of alternate functions is used for control and communication interfaces, like a PWM from a CAPCOM unit or a SPI communication of a USIC channel. A detailed connectivity list of the peripherals to the port pins is given in the ***Port I/O Function Description*** chapter. For specific functions, certain peripherals may also take direct control of “their” port pins, see ***Hardware Controlled I/Os***.

26.2.1 Input Operation

As an input, the actual voltage level at the port pin is translated into a logical 0_B or 1_B via a Schmitt-Trigger device within the pad. The resulting input value can be optionally inverted. As general purpose input, the signal is synchronized and can be read with the Input register (Pn_IN, ***Chapter 26.8.6***). Alternatively, the input can be connected to the multiple on-chip peripherals via the ALTIN signal. Where neccessary, these peripherals have internal controls to select the appropriate port pin with an input multiplexer stage, and will take care of synchronization and further processing of the input signals. (See respective peripheral chapters for more details on the input selection and handling). With the Pn_IOCR register (***Chapter 26.8.1***), it is also possible to activate an internal weak pull-up or pull-down device in the pad.

The input register Pn_IN and ALTIN signal always represent the state of the input, independent whether the port pin is configured as input or output. This means that even if the port is in output mode, the level of the pin can be read by software via Pn_IN and/or a peripheral can use the pin level as an input.

Pad Hysteresis Control

The pad hysteresis can be configured according to the application needs via the Pad Hysteresis Control register (Pn_PHCR, ***Chapter 26.8.2***). Selecting the appropriate pad hysteresis allows optimized pad oscillation behaviour for touch-sensing applications.

26.2.2 Output Operation

In output mode, the output driver is activated and drives the value supplied through the multiplexer to the port pin. Switching between input and output mode is accomplished through the Pn_IOCR register (***Chapter 26.8.1***), which

- enables or disables the output driver,
- selects between open-drain and push-pull mode,
- selects the general purpose or alternate function outputs.

The output multiplexer selects the signal source of the output with

- Pn_IOCR
  - general purpose output (Pn_OUT, ***Chapter 26.8.4***)
  - alternate peripheral functions, ALT1...ALT9
- hardware control, Pn_HWSEL
  - HW0_OUT
  - HW1_OUT

Note: It is recommended to complete the Port and peripheral configuration with respect to operating mode and initial values before the port pin is switched to output mode.

The output function is exclusive, meaning that only one peripheral has control of the output path at any one time.

Used as general purpose output, software can directly modify the content of Pn_OUT to define the output value on the pin. A write operation to Pn_OUT updates all port pins of that port (e.g. P0) that are configured as general purpose output. Updating just one or a selected few general purpose output pins via Pn_OUT requires a masked read-modify-write operation to avoid disturbing pins that shall not be changed. Direct writes to Pn_OUT will also affect Pn_OUT bits configured for use with the Pin Power-save function, ***Chapter 26.4***.

Because of that, it is preferred to modify Pn_OUT bits by the Output Modification Register Pn_OMR (***Chapter 26.8.5***). The bits in Pn_OMR allow to individually set, clear or toggle the bits in the Pn_OUT register and only update the “addressed” Pn_OUT bits.

The data written by software into the output register Pn_OUT can also be used as input data to an on-chip peripheral. This enables, for example, peripheral tests and simulation via software without external circuitry.

Output lines of on-chip peripherals can directly control the output value of the output driver if selected via ALT1 to ALT9 as well as HW0_OUT and HW1_OUT. After initialization, this allows the connected peripherals to directly drive complex control and communication patterns without further software interaction with the ports.

The actual logic level at the pin can be examined through reading Pn_IN and compared against the applied output level (either applied by the output register Pn_OUT, or via an alternate output function of a peripheral unit). This can be used to detect some electrical failures at the pin caused by external circuitry. In addition, software-supported arbitration schemes between different “masters” can be implemented in this way, using the open-drain configuration and an external wired-AND circuitry. Collisions on the external communication lines can be detected when a high level (1_B) is output, but a low level (0_B) is seen when reading the pin value via the input register Pn_IN or directly by a peripheral (via ALTIN, for example a USIC channel in IIC mode).

There are three pad types in IMC300A providing different drive strength or with oscillator function:

- Standard pad (with oscillator function)

- Standard pad (without oscillator function)
- High Current pad

The assignment of each port pin to one of these pad types is listed in the Package Pin Summary table. Further details about pad properties are summarized in the Data Sheet. Oscillator functions and controls are described in the Clock Control Unit (CCU) of SCU chapter.

26.3 Hardware Controlled I/Os

Some ports pins are overlaid with peripheral functions for which the connected peripheral needs direct hardware control, e.g. for the direction of a bi-directional data bus. There is a dedicated hardware control interface for these functions. As multiple peripherals need access to this interface, the Pn_HWSEL register (***Chapter 26.8.8***) allows to select between the hardware "masters".

Depending on the operating mode, the peripheral can take control of various functions:

- Pin direction, input or output, e.g. for bi-directional signals
- Driver type, open-drain or push-pull
- Pull devices under peripheral control or under standard control via Pn_IOCR

Some configurations remain under control by the standard configuration interface, the pad hysteresis by Pn_PHCR and the direct or inverted input path by Pn_IOCR.

Pn_HWSEL.HWx just pre-assigns the hardware-control of the pin to a certain peripheral, but the peripheral itself decides when to take control over it. As long as the peripheral does not take control of a given pin via HWx_EN, the configuration of this pin is still defined by the configuration registers and it is available as GPIO or for other alternate functions. This might be because the selected peripheral has controls to just activate a subset of its pins, or because the peripheral is not active at all.

This mechanism can also be used to prohibit the hardware control of certain pins to a peripheral, in case the application does not need the respective functionality and the peripheral has no controls to disable the hardware control selectively.

The default hardware input configuration and the pull devices are controlled by Pn_IOCR.

The outputs of DAC, CCU4 and ACMP modules can be used to control the internal pull devices via direct hardware control. A detailed connectivity list of the hardware I/O and pull control of the peripherals to the port pins is given in the ***Hardware Controlled I/O Function Description*** chapter.

Note: Do not enable the Pin Power Save function for pins configured for Hardware Control (Pn_HWSEL.HWx != 00_B). Doing so may result in an undefined behavior of the pin when the device enters the Deep Sleep state.

26.4 Power Saving Mode Operation

In Deep-Sleep mode, the behavior of a pin depends on the setting of the Pin Power save register (Pn_PPS, ***Chapter 26.8.7***). Basically, each pin can be configured to react to the Power Save Mode Request or to ignore it. In case a pin is configured to react to a Power Save Mode Request, the output driver is switched to tri-state, the input Schmitt-Trigger and the pull devices are switched off (see ***Figure 276***). The input signal to the the on-chip peripherals is optionally driven statically high or low, software-defined by a value stored in Pn_OUT or by the last input value sampled to the Pn_OUT register during normal operation. The actual reaction is configured with the Pn_IOCR register under power save conditions, see ***Table 295***.

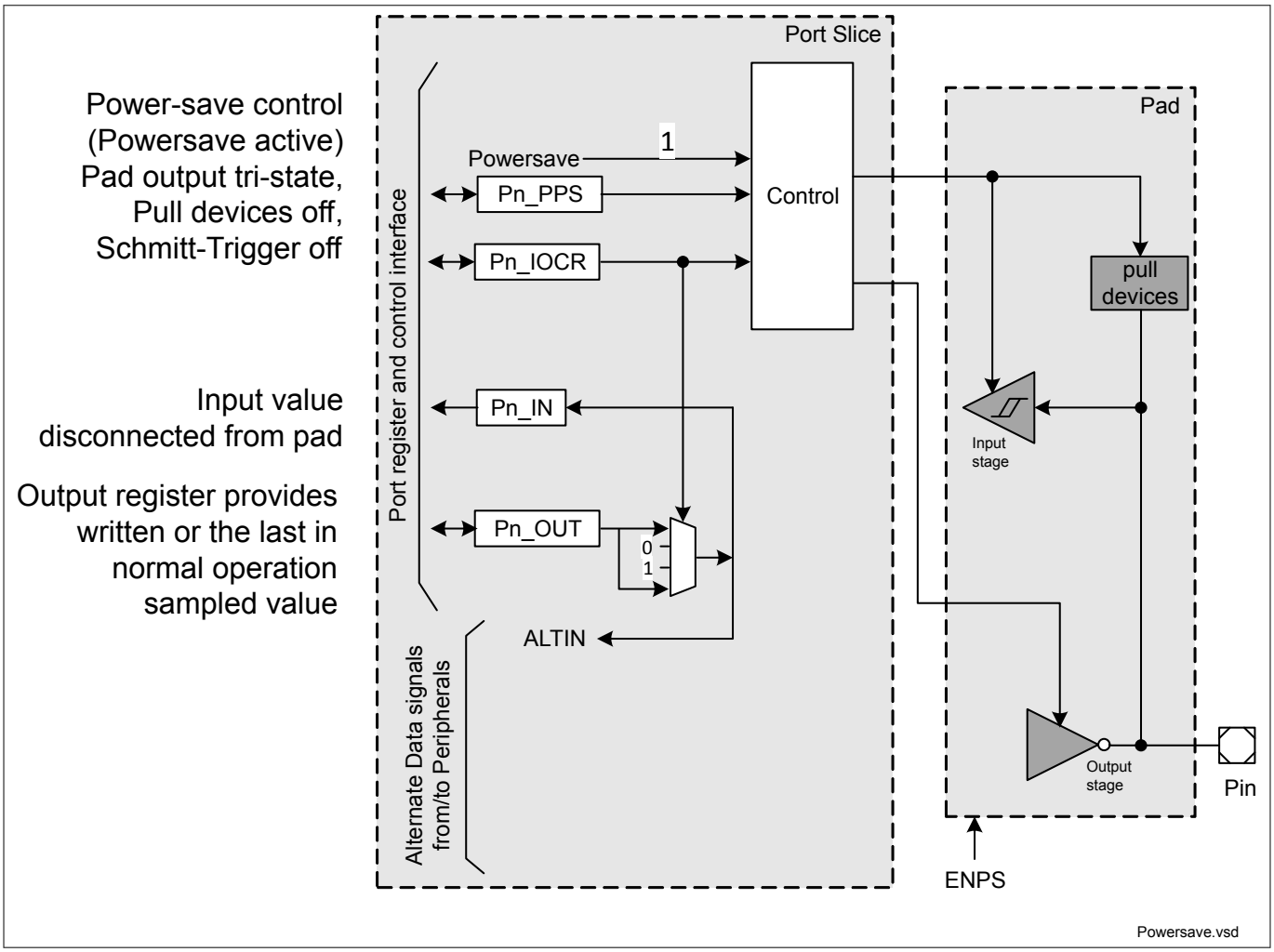


Figure 276 Port Pin in Power Save State

Note: Do not enable the Pin Power Save function for pins configured for Hardware Control (Pn_HWSEL.HWx != 00_B). Doing so may result in an undefined behavior of the pin when the device enters the Deep Sleep state.

26.5 Analog Ports

P2.2 - P2.9 is the analog and digital input port with a simplified port and pad structure, see ***Figure 277***. The analog pads have no output drivers and the digital input Schmitt-Trigger can be controlled by the Pn_PDISC (***Chapter 26.8.3***) register. Accordingly, the port control interface is reduced in its functionality. The Pn_IOCR register controls the pull devices, the optional input inversion and the input source in power-save mode. The Pn_OUT has only its power-save functionality, as described in ***Chapter 26.4***.

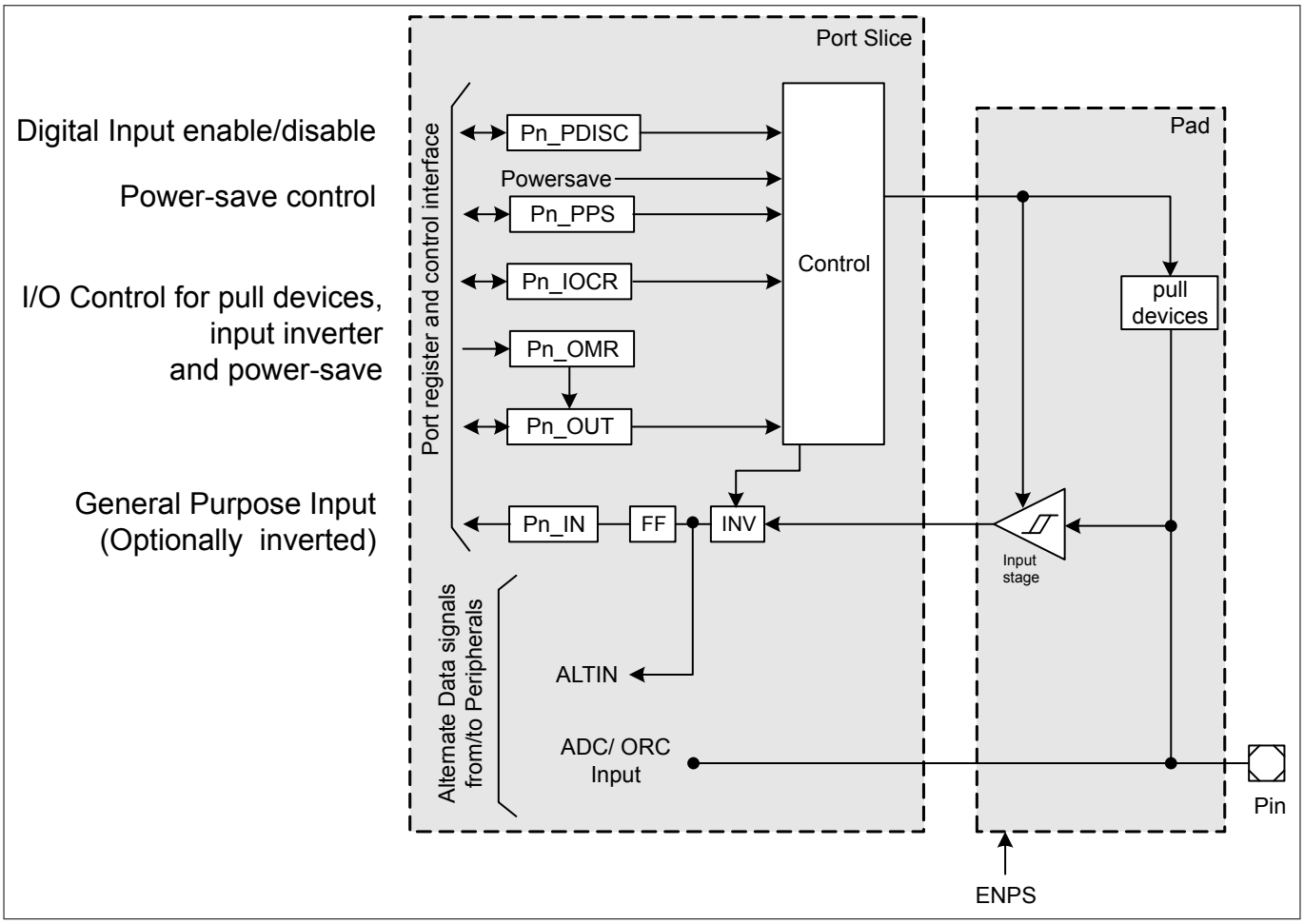


Figure 277 Analog Port Structure

26.6 Power, Reset and Clock

All digital I/O pads are held in a defined state, tristate, with output driver disabled and no pull devices active when one of the following occurs:

- During power-up, until V_{DDC} and V_{DDP} voltage levels are stable and within limits
- During power-fail, one or more voltage levels are outside the limits

Refer to the EVR section in the SCU chapter and Data Sheet for details on the power-up, supply monitoring and voltage limits.

All Port registers are reset with the System Reset (see Reset Control Unit chapter in the System Control Unit). The standard reset values are defined such that the port pins are configured as tri-state inputs, output driver disabled and no pull devices active. Exceptions from these standard values are related to special interfaces or the analog input channels.

All registers of the Ports are clocked with f_{MCLK}.

26.7 Initialization and System Dependencies

It is recommended to follow pre-defined routines for the initialization of the port pins.

Input

When a peripheral shall use a port pin as input, the actual pin levels may immediately trigger an unexpected peripheral event (e.g. clock edge at SPI). This can be avoided by forcing the "passive" level via pull-up/down programming.

The following steps are required to configure a port pin as an input:

- Pn_IOCR
  input configuration with pull device and/or power-save mode configuration
- Pn_PHCR
  pad hysteresis configuration (if applicable)
- Hardware Control (if applicable)
  - Pn_HWSEL
    switch hardware control to peripheral
- Pin Power Save (if applicable)
  - Pn_OMR/Pn_OUT
    default value in power save mode (if applicable)
  - Pn_PPS
    enable power save control

Output

When a port pin is configured as output for an on-chip peripheral, it is important that the peripheral is configured before the port switches the control to the peripheral in order to avoid spikes on the output.

The following steps are required to configure a port pin as an output:

- Pn_OMR/Pn_OUT
  Initial output value (as general purpose output)
- GPIO or Alternate Output
  - Pn_IOCR
    Output multiplexer select
    Push-pull or open-drain output driver mode
    Activates the output driver!
- Hardware Control
  - Pn_IOCR
    depending on the hardware function Pn_IOCR can enable the internal pull devices
  - Pn_HWSEL
    Switch hardware control to peripheral

Transitions

If a port pin is used for different functions that require a reconfiguration of the port registers, it is recommended to do this transition via an intermediate “neutral” tri-state input configuration.

- Pn_HWSEL
  disable hardware selection; can be omitted if no hardware control is used on the port pin
- Pn_PPS
  disable power save mode control of the pin; can be ommited if no power save configuration is used on the port pin
- Pn_IOCR
  tri-state input and no pull device active

26.8 Registers

Registers Overview

The absolute register address is calculated by adding:
Module Base Address + Offset Address

Table 289 Registers Address Space

Module	Base Address	End Address	Note
P0	$4004\ 0000_H$	$4004\ 00FF_H$	4 standard pads can be disabled for external oscillator function
P1	$4004\ 0100_H$	$4004\ 01FF_H$	High current bi-directional pad
P2	$4004\ 0200_H$	$4004\ 02FF_H$	Analog/Digital input and bi-directional pad
P3	$4004\ 0300_H$	$4004\ 03FF_H$	
P4	$4004\ 0400_H$	$4004\ 04FF_H$	

Table 290 Register Overview

Short Name	Description	Offset Addr.	Access Mode		Description See
			Read	Write	
Pn_OUT	Port n Output Register	0000_H	U, PV	U, PV	Page *871*
Pn_OMR	Port n Output Modification Register	0004_H	U, PV	U, PV	Page *874*
–	Reserved	0008_H - $000C_H$	BE	BE	–
Pn_IOCR0	Port n Input/Output Control Register 0	0010_H	U, PV	PV	Page *859*
Pn_IOCR4	Port n Input/Output Control Register 4	0014_H	U, PV	PV	Page *860*
Pn_IOCR8	Port n Input/Output Control Register 8	0018_H	U, PV	PV	Page *861*
Pn_IOCR12	Port n Input/Output Control Register 12	$001C_H$	U, PV	PV	Page *862*
–	Reserved	0020_H	BE	BE	–
Pn_IN	Port n Input Register	0024_H	U, PV	R	Page *877*
–	Reserved	0028_H - $003C_H$	BE	BE	–
Pn_PHCR0	Port n Pad Hysteresis Control Register 0	0040_H	U, PV	PV	Page *864*
Pn_PHCR1	Port n Pad Hysteresis Control Register 1	0044_H	U, PV	PV	Page *866*
–	Reserved	0048_H - $005C_H$	BE	BE	–
P0_PDISC P1_PDISC	Port n Pin Function Decision Control Register (non-ADC/ACMP ports)	0060_H	U, PV	BE	Page *868*
P2_PDISC	Port n Pin Function Decision Control Register (ADC/ACMP ports)	0060_H	U, PV	PV	Page *869*

Table 290 Register Overview (continued)

Short Name	Description	Offset Addr.	Access Mode		Description See
			Read	Write	
P3_PDISC P4_PDISC	Port n Pin Function Decision Control Register (non-ADC/ACMP ports)	0060_H	U, PV	BE	Page 870
–	Reserved	0064_H - $006C_H$	BE	BE	–
Pn_PPS	Port n Pin Power Save Register	0070_H	U, PV	PV	Page 880
Pn_HWSEL	Port n Hardware Select Register	0074_H	U, PV	PV	Page 883
–	Reserved	0078_H - $00FC_H$	BE	BE	–

Table 291 Registers Access Rights and Reset Classes

Register Short Name	Access Rights		Reset Class
	Read	Write	
Pn_IN	U, PV	R	System Reset
Pn_OUT		U, PV	
Pn_OMR			
Pn_IOCR0		PV	
Pn_IOCR4			
Pn_IOCR8			
Pn_IOCR12			
Pn_PDISC (ADC/ACMP ports)			
Pn_PH0			
Pn_PH1			
Pn_PPS			
Pn_PDISC (non-ADC/ACMP ports)		BE	

26.8.1 Port Input/Output Control Registers

The port input/output control registers select the digital output and input driver functionality and characteristics of a GPIO port pin. Port direction (input or output), pull-up or pull-down devices for inputs, and push-pull or open-drain functionality for outputs can be selected by the corresponding bit fields PCx (x = 0-15). Each 32-bit wide port input/output control register controls four GPIO port lines:

Register Pn_IOCR0 controls the Pn.[3:0] port lines

Register Pn_IOCR4 controls the Pn.[7:4] port lines

Register Pn_IOCR8 controls the Pn.[11:8] port lines

Register Pn_IOCR12 controls the Pn.[15:12] port lines

The diagrams below show the register layouts of the port input/output control registers with the PCx bit fields. One PCx bit field controls exactly one port line Pn.x.

Depending on the GPIO port functionality (number of GPIO lines of a port), not all of the port input/output control registers are implemented.

The structure with one control bit field for each port pin located in different register bytes offers the possibility to configure the port pin functionality of a single pin with byte-oriented accesses without accessing the other PCx bit fields.

Port Control Coding

Table 292 describes the coding of the PCx bit fields that determine the port line functionality.

The Pn_IOCRy PCx bit field is also used to contol the pin behavior in Deep-Sleep mode if the Pin Power Save option is enabled, see *Chapter 26.8.7*.

Table 292 Standard PCx Coding[66)]

PCx[5:0]	I/O	Output Characteristics	Selected Pull-up / Pull-down / Selected Output Function
$0XX000_B$	Direct Input	–	No internal pull device active
$0XX001_B$			Internal pull-down device active
$0XX010_B$			Internal pull-up device active
$0XX011_B$			No internal pull device active; Pn_OUTx continuously samples the input value
$0XX100_B$	Inverted Input	–	No internal pull device active
$0XX101_B$			Internal pull-down device active
$0XX110_B$			Internal pull-up device active
$0XX111_B$			No internal pull device active; Pn_OUTx continuously samples the input value
100000_B	Output (Direct Input)	Push-pull	General-purpose output
100001_B			Alternate output function 1
100010_B			Alternate output function 2
100011_B			Alternate output function 3
100100_B			Alternate output function 4
100101_B			Alternate output function 5
100110_B			Alternate output function 6
100111_B			Alternate output function 7
101000_B			Alternate output function 8
101001_B			Alternate output function 9
101010_B			Reserved
101011_B			Reserved
101100_B			Reserved
101101_B			Reserved
101110_B			Reserved
101111_B			Reserved

66 For the analog and digital input port P2.2 - P2.9, the combinations with PCx[5]=1_B is reserved.

Table 292 Standard PCx Coding[66] (continued)

PCx[5:0]	I/O	Output Characteristics	Selected Pull-up / Pull-down / Selected Output Function
110000_B	Output (Direct Input)	Open-drain	General-purpose output
110001_B			Alternate output function 1
110010_B			Alternate output function 2
110011_B			Alternate output function 3
110100_B			Alternate output function 4
110101_B			Alternate output function 5
110110_B			Alternate output function 6
110111_B			Alternate output function 7
111000_B			Alternate output function 8
111001_B			Alternate output function 9
111010_B			Reserved
111011_B			Reserved
111100_B			Reserved
111101_B			Reserved
111110_B			Reserved
111111_B			Reserved

26.8.1.1 Register Pn_IOCR0 (n=0-4)

Pn_IOCR0 (n=0-4) Address: $4004\ 0010_H + n*100_H$

Port n Input/Output Control Register 0 Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PC3						0		PC2						0	
rw						r		rw						r	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PC1						0		PC0						0	
rw						r		rw						r	

Field	Bits	Type	Description
PC0	7:2	rw	**Port Control for Port n Pin 0** This bit field determines the Port n line x functionality (x = 0) according to the coding table (see ***Table 292***).
PC1	15:10	rw	**Port Control for Port n Pin 1** This bit field determines the Port n line x functionality (x = 1) according to the coding table (see ***Table 292***).

66 For the analog and digital input port P2.2 - P2.9, the combinations with PCx[5]=1_B is reserved.

(continued)

Field	Bits	Type	Description
PC2	23:18	rw	**Port Control for Port n Pin 2** This bit field determines the Port n line x functionality (x = 2) according to the coding table (see ***Table 292***).
PC3	31:26	rw	**Port Control for Port n Pin 3** This bit field determines the Port n line x functionality (x = 3) according to the coding table (see ***Table 292***).
0	1:0, 9:8, 17:16, 25:24	r	**Reserved** Read as 0; should be written with 0.

26.8.1.2 Register Pn_IOCR4 (n=0-2) / P4_IOCR4

Pn_IOCR4 (n=0-2) Address: $4004\ 0014_H + n*100_H$

Port n Input/Output Control Register 4 Reset Value: $0000\ 0000_H$

P4_IOCR4 Address: 0014_H

Port 4 Input/Output Control Register 4 Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PC7						**0**		**PC6**						**0**	
rw						r		rw						r	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PC5						**0**		**PC4**						**0**	
rw						r		rw						r	

Field	Bits	Type	Description
PC4	7:2	rw	**Port Control for Port n Pin 4** This bit field determines the Port n line x functionality (x = 4) according to the coding table (see ***Table 292***).
PC5	15:10	rw	**Port Control for Port n Pin 5** This bit field determines the Port n line x functionality (x = 5) according to the coding table (see ***Table 292***).
PC6	23:18	rw	**Port Control for Port n Pin 6** This bit field determines the Port n line x functionality (x = 6) according to the coding table (see ***Table 292***).
PC7	31:26	rw	**Port Control for Port n Pin 7** This bit field determines the Port n line x functionality (x = 7) according to the coding table (see ***Table 292***).
0	1:0, 9:8, 17:16, 25:24	r	**Reserved** Read as 0; should be written with 0.

26.8.1.3 Register P3_IOCR4

P3_IOCR4 Address: 0014_H

Port 3 Input/Output Control Register 4 Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								PC4						0	
r								rw						r	

Field	Bits	Type	Description
PC4	7:2	rw	**Port Control for Port 3 Pin 4** This bit field determines the Port 3 line x functionality (x = 4) according to the coding table (see ***Table 292***).
0	1:0, 31:8	r	**Reserved** Read as 0; should be written with 0.

26.8.1.4 Register P0_IOCR8 / P2_IOCR8 / P4_IOCR8

P0_IOCR8 Address: 0018_H

Port 0 Input/Output Control Register 8 Reset Value: $0000\ 0000_H$

P2_IOCR8 Address: 0018_H

Port 2 Input/Output Control Register 8 Reset Value: $0000\ 0000_H$

P4_IOCR8 Address: 0018_H

Port 4 Input/Output Control Register 8 Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PC11						0		PC10						0	
rw						r		rw						r	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PC9						0		PC8						0	
rw						r		rw						r	

Field	Bits	Type	Description
PC8	7:2	rw	**Port Control for Port n Pin 8** This bit field determines the Port n line x functionality (x = 8) according to the coding table (see ***Table 292***).
PC9	15:10	rw	**Port Control for Port n Pin 9** This bit field determines the Port n line x functionality (x = 9) according to the coding table (see ***Table 292***).

(continued)

Field	Bits	Type	Description
PC10	23:18	rw	**Port Control for Port n Pin 10** This bit field determines the Port n line x functionality (x = 10) according to the coding table (see ***Table 292***).
PC11	31:26	rw	**Port Control for Port n Pin 11** This bit field determines the Port n line x functionality (x = 11) according to the coding table (see ***Table 292***).
0	1:0, 9:8, 17:16, 25:24	r	**Reserved** Read as 0; should be written with 0.

26.8.1.5 Register P1_IOCR8

P1_IOCR8 Address: 0018_H

Port 1 Input/Output Control Register 8 Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								PC8						0	
r								rw						r	

Field	Bits	Type	Description
PC8	7:2	rw	**Port Control for Port 1 Pin 8** This bit field determines the Port 1 line x functionality (x = 8) according to the coding table (see ***Table 292***).
0	1:0, 31:8	r	**Reserved** Read as 0; should be written with 0.

26.8.1.6 Register P0_IOCR12

P0_IOCR12 Address: $001C_H$

Port 0 Input/Output Control Register 12 Reset Value: $0000\ 0000_H$ [67)]

67 Upon reset, the value of PC14 (P0.14) is 000000_B. The Startup Software (SSW) will change the PC14 value to input pull-up device active, 000100_B. Refer to the Startup chapter for more information.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PC15						0		PC14						0	
rw						r		rw						r	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PC13						0		PC12						0	
rw						r		rw						r	

Field	Bits	Type	Description
PC12	7:2	rw	**Port Control for Port 0 Pin 12** This bit field determines the Port 0 line x functionality (x = 12) according to the coding table (see ***Table 292***).
PC13	15:10	rw	**Port Control for Port 0 Pin 13** This bit field determines the Port 0 line x functionality (x = 13) according to the coding table (see ***Table 292***).
PC14	23:18	rw	**Port Control for Port 0 Pin 14** This bit field determines the Port 0 line x functionality (x = 14) according to the coding table (see ***Table 292***).
PC15	31:26	rw	**Port Control for Port 0 Pin 15** This bit field determines the Port 0 line x functionality (x = 15) according to the coding table (see ***Table 292***).
0	1:0, 9:8, 17:16, 25:24	r	**Reserved** Read as 0; should be written with 0.

26.8.1.7 Register P2_IOCR12

P2_IOCR12 Address: $001C_H$

Port 2 Input/Output Control Register 12 Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PC13						0		PC12						0	
rw						r		rw						r	

Field	Bits	Type	Description
PC12	7:2	rw	**Port Control for Port 2 Pin 12** This bit field determines the Port 2 line x functionality (x = 12) according to the coding table (see ***Table 292***).

(continued)

Field	Bits	Type	Description
PC13	15:10	rw	**Port Control for Port 2 Pin 13** This bit field determines the Port 2 line x functionality (x = 13) according to the coding table (see ***Table 292***).
0	1:0, 9:8, 31:16	r	**Reserved** Read as 0; should be written with 0.

26.8.2 Pad Hysteresis Control Register

The pad structure of the IMC300A GPIO lines offers the possibility to select the pad hysteresis. These two parameters are controlled by the bit fields in the pad hysteresis control registers Pn_PHCR0/1, independently from input/output and pull-up/pull-down control functionality as programmed in the Pn_IOCR register. Pn_PHCR0 and Pn_PHCR1 registers are assigned to each port.

The 1-bit pad hysteresis selection bit field PHx in the pad hysteresis control registers Pn_PHCR make it possible to select the port line functionality as shown in ***Table 293***. Note that the pad hysteresis control registers are specific for each port.

Table 293 Pad Hysteresis Selection

PHx	Functionality
0	Standard hysteresis
1	Large hysteresis

Note: Refer to Input/Output Characteristics table in the IMC300A Data Sheet for hysteresis parameter values.

26.8.2.1 Register Pn_PHCR0 (n=0-2) / P4_PHCR0

Pn_PHCR0 (n=0-2) Address: $4004\ 0040_H + n*100_H$

Port n Pad Hysteresis Control Register 0 Reset Value: $0000\ 0000_H$

P4_PHCR0 Address: 0040_H

Port 4 Pad Hysteresis Control Register 0 Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**PH7**	**0**			**PH6**	**0**			**PH5**	**0**			**PH4**	**0**	
r	rw	r			rw	r			rw	r			rw	r	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**PH3**	**0**			**PH2**	**0**			**PH1**	**0**			**PH0**	**0**	
r	rw	r			rw	r			rw	r			rw	r	

Field	Bits	Type	Description
PH0	2	rw	**Pad Hysteresis for Pn.0**

(continued)

Field	Bits	Type	Description
PH1	6	rw	**Pad Hysteresis for Pn.1**
PH2	10	rw	**Pad Hysteresis for Pn.2**
PH3	14	rw	**Pad Hysteresis for Pn.3**
PH4	18	rw	**Pad Hysteresis for Pn.4**
PH5	22	rw	**Pad Hysteresis for Pn.5**
PH6	26	rw	**Pad Hysteresis for Pn.6**
PH7	30	rw	**Pad Hysteresis for Pn.7**
0	1:0, 5:3, 9:7, 13:11, 17:15, 21:19, 25:23, 29:27, 31	r	**Reserved** Read as 0; should be written with 0.

26.8.2.2 Register P3_PHCR0

P3_PHCR0 Address: 0040_H

Port 3 Pad Hysteresis Control Register 0 Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0													PH4	0	
r													rw	r	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	PH3	0			PH2	0			PH1	0			PH0	0	
r	rw	r			rw	r			rw	r			rw	r	

Field	Bits	Type	Description
PH0	2	rw	**Pad Hysteresis for P3.0**
PH1	6	rw	**Pad Hysteresis for P3.1**
PH2	10	rw	**Pad Hysteresis for P3.2**
PH3	14	rw	**Pad Hysteresis for P3.3**
PH4	18	rw	**Pad Hysteresis for P3.4**
0	1:0, 5:3, 9:7, 13:11, 17:15, 31:19	r	**Reserved** Read as 0; should be written with 0.

26.8.2.3 Register P0_PHCR1

P0_PHCR1 Address: 0044_H

Port 0 Pad Hysteresis Control Register 1 Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**PH15**	**0**			**PH14**	**0**			**PH13**	**0**			**PH12**	**0**	
r	rw	r			rw	r			rw	r			rw	r	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**PH11**	**0**			**PH10**	**0**			**PH9**	**0**			**PH8**	**0**	
r	rw	r			rw	r			rw	r			rw	r	

Field	Bits	Type	Description
PH8	2	rw	**Pad Hysteresis for P0.8**
PH9	6	rw	**Pad Hysteresis for P0.9**
PH10	10	rw	**Pad Hysteresis for P0.10**
PH11	14	rw	**Pad Hysteresis for P0.11**
PH12	18	rw	**Pad Hysteresis for P0.12**
PH13	22	rw	**Pad Hysteresis for P0.13**
PH14	26	rw	**Pad Hysteresis for P0.14**
PH15	30	rw	**Pad Hysteresis for P0.15**
0	1:0, 5:3, 9:7, 13:11, 17:15, 21:19, 25:23, 29:27, 31	r	**Reserved** Read as 0; should be written with 0.

26.8.2.4 Register P1_PHCR1

P1_PHCR1 Address: 0044_H

Port 1 Pad Hysteresis Control Register 1 Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0													**PH8**	**0**	
r													rw	r	

Field	Bits	Type	Description
PH8	2	rw	**Pad Hysteresis for P1.8**

(continued)

Field	Bits	Type	Description
0	1:0, 31:3	r	**Reserved** Read as 0; should be written with 0.

26.8.2.5 Register P2_PHCR1

P2_PHCR1 Address: 0044_H

Port 2 Pad Hysteresis Control Register 1 Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0									PH13	0			PH12	0	
r									rw	r			rw	r	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	PH11	0			PH10	0			PH9	0			PH8	0	
r	rw	r			rw	r			rw	r			rw	r	

Field	Bits	Type	Description
PH8	2	rw	**Pad Hysteresis for P2.8**
PH9	6	rw	**Pad Hysteresis for P2.9**
PH10	10	rw	**Pad Hysteresis for P2.10**
PH11	14	rw	**Pad Hysteresis for P2.11**
PH12	18	rw	**Pad Hysteresis for P2.12**
PH13	22	rw	**Pad Hysteresis for P2.13**
0	1:0, 5:3, 9:7, 13:11, 17:15, 21:19, 31:23	r	**Reserved** Read as 0; should be written with 0.

26.8.2.6 Register P4_PHCR1

P4_PHCR1 Address: 0044_H

Port 4 Pad Hysteresis Control Register 1 Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	PH11	0			PH10	0			PH9	0			PH8	0	
r	rw	r			rw	r			rw	r			rw	r	

Field	Bits	Type	Description
PH8	2	rw	**Pad Hysteresis for P4.8**
PH9	6	rw	**Pad Hysteresis for P4.9**
PH10	10	rw	**Pad Hysteresis for P4.10**
PH11	14	rw	**Pad Hysteresis for P4.11**
0	1:0, 5:3, 9:7, 13:11, 31:15	r	**Reserved** Read as 0; should be written with 0.

26.8.3 Pin Function Decision Control Register

The primary use for this register is to disable/enable the digital pad structure in shared analog and digital ports, see the dedicated description for ***P2_PDISC***.

For “normal” digital I/O ports (P0-P1, P3-P4) this register is read-only and the read value corresponds to the available pins in the given package.

26.8.3.1 Register P0_PDISC

P0_PDISC Address: 0060_H

Port 0 Pin Function Decision Control Register Reset Value: $0000\ XXXX_H$ [68]

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PDIS 15	**PDIS 14**	**PDIS 13**	**PDIS 12**	**PDIS 11**	**PDIS 10**	**PDIS 9**	**PDIS 8**	**PDIS 7**	**PDIS 6**	**PDIS 5**	**PDIS 4**	**PDIS 3**	**PDIS 2**	**PDIS 1**	**PDIS 0**
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Field	Bits	Type	Description
PDISx (x=0-15)	x	r	**Pad Disable for Port 0 Pin x** 0_B Pad P0.x is enabled. 1_B Pad P0.x is disabled.
0	31:16	r	**Reserved** Read as 0; should be written with 0.

26.8.3.2 Register P1_PDISC

P1_PDISC Address: 0060_H

Port 1 Pin Function Decision Control Register Reset Value: $0000\ 0XXX_H$ [69]

68 The reset value is package dependent.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0							**PDIS 8**	**PDIS 7**	**PDIS 6**	**PDIS 5**	**PDIS 4**	**PDIS 3**	**PDIS 2**	**PDIS 1**	**PDIS 0**
r							r	r	r	r	r	r	r	r	r

Field	Bits	Type	Description
PDISx (x=0-8)	x	r	**Pad Disable for Port 1 Pin x** 0_B Pad P1.x is enabled. 1_B Pad P1.x is disabled.
0	31:9	r	**Reserved** Read as 0; should be written with 0.

26.8.3.3 Register P2_PDISC

P2_PDISC Address: 0060_H

Port 2 Pin Function Decision Control Register Reset Value: 0000 XXXX$_H$ [70)]

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		**PDIS 13**	**PDIS 12**	**PDIS 11**	**PDIS 10**	**PDIS 9**	**PDIS 8**	**PDIS 7**	**PDIS 6**	**PDIS 5**	**PDIS 4**	**PDIS 3**	**PDIS 2**	**PDIS 1**	**PDIS 0**
r		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
PDISx (x=0-1)	x	rw	**Pad Disable for Port 2 Pin 0 to 1** This bit disables or enables the digital pad function. 0_B Digital Pad input is enabled. Analog and digital input/output path active. 1_B Digital Pad input is disabled. Analog input path active. (default)

69 The reset value is package dependent.
70 The reset value is package dependent.

(continued)

Field	Bits	Type	Description
PDISx (x=2-9)	x	rw	**Pad Disable for Port 2 Pin 2 to 9** This bit disables or enables the digital pad function. 0_B Digital Pad input is enabled. Analog and digital input path active. 1_B Digital Pad is disabled. Analog input path active. (default)
PDISx (x=10-13)	x	rw	**Pad Disable for Port 2 Pin 10 to 13** This bit disables or enables the digital pad function. 0_B Digital Pad input is enabled. Analog and digital input/output path active. 1_B Digital Pad input is disabled. Analog input path active. (default)
0	31:14	r	**Reserved** Read as 0; should be written with 0.

26.8.3.4 Register P3_PDISC

P3_PDISC Address: 0060_H

Port 3 Pin Function Decision Control Register Reset Value: $0000\ 00XX_H$ [71)]

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0											PDIS4	PDIS3	PDIS2	PDIS1	PDIS0
r											r	r	r	r	r

Field	Bits	Type	Description
PDISx (x=0-4)	x	r	**Pad Disable for Port 3 Pin x** 0_B Pad P3.x is enabled. 1_B Pad P3.x is disabled.
0	31:5	r	**Reserved** Read as 0; should be written with 0.

26.8.3.5 Register P4_PDISC

P4_PDISC Address: 0060_H

Port 4 Pin Function Decision Control Register Reset Value: $0000\ 0XXX_H$ [72)]

71 The reset value is package dependent.
72 The reset value is package dependent.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				PDIS 11	PDIS 10	PDIS 9	PDIS 8	PDIS 7	PDIS 6	PDIS 5	PDIS 4	PDIS 3	PDIS 2	PDIS 1	PDIS 0
r				r	r	r	r	r	r	r	r	r	r	r	r

Field	Bits	Type	Description
PDISx (x=0-11)	x	r	**Pad Disable for Port 4 Pin x** 0_B Pad P4.x is enabled. 1_B Pad P4.x is disabled.
0	31:12	r	**Reserved** Read as 0; should be written with 0.

26.8.4 Port Output Register

The port output register determines the value of a GPIO pin when it is selected by Pn_IOCRx as output. Writing a 0 to a Pn_OUT.Px (x = 0-15) bit position delivers a low level at the corresponding output pin. A high level is output when the corresponding bit is written with a 1. Note that the bits of Pn_OUT.Px can be individually set/ reset by writing appropriate values into the port output modification register Pn_OMR, avoiding read-modify-write operations on the Pn_OUT, which might affect other pins of the port.

The Pn_OUT is also used to store/drive a defined value for the input in Deep-Sleep mode. For details on this, see the ***Port Pin Power Save Register***. That is also the only use of the Pn_OUT register in the analog and digital input port P2.2 - P2.9.

26.8.4.1 Register P0_OUT

P0_OUT Address: 0000_H

Port 0 Output Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
Px (x=0-15)	x	rwh	**Port 0 Output Bit x** This bit determines the level at the output pin P0.x if the output is selected as GPIO output. 0_B The output level of P0.x is 0. 1_B The output level of P0.x is 1. P0.x can also be set/reset by control bits of the P0_OMR register.
0	31:16	r	**Reserved** Read as 0; should be written with 0.

26.8.4.2 Register P1_OUT

P1_OUT Address: 0000_H

Port 1 Output Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0							**P8**	**P7**	**P6**	**P5**	**P4**	**P3**	**P2**	**P1**	**P0**
r							rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
Px (x=0-8)	x	rwh	**Port 1 Output Bit x** This bit determines the level at the output pin P1.x if the output is selected as GPIO output. 0_B The output level of P1.x is 0. 1_B The output level of P1.x is 1. P1.x can also be set/reset by control bits of the P1_OMR register.
0	31:9	r	**Reserved** Read as 0; should be written with 0.

26.8.4.3 Register P2_OUT

P2_OUT Address: 0000_H

Port 2 Output Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0
r		rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
Px (x=0-13)	x	rwh	**Port 2 Output Bit x** This bit determines the level at the output pin P2.x if the output is selected as GPIO output. 0_B The output level of P2.x is 0. 1_B The output level of P2.x is 1. P2.x can also be set/reset by control bits of the P2_OMR register.
0	31:14	r	**Reserved** Read as 0; should be written with 0.

26.8.4.4 Register P3_OUT

P3_OUT Address: 0000_H

Port 3 Output Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0											P4	P3	P2	P1	P0
r											rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
Px (x=0-4)	x	rwh	**Port 3 Output Bit x** This bit determines the level at the output pin P3.x if the output is selected as GPIO output. 0_B The output level of P3.x is 0. 1_B The output level of P3.x is 1. P3.x can also be set/reset by control bits of the P3_OMR register.
0	31:5	r	**Reserved** Read as 0; should be written with 0.

26.8.4.5 Register P4_OUT

P4_OUT Address: 0000_H

Port 4 Output Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				**P11**	**P10**	**P9**	**P8**	**P7**	**P6**	**P5**	**P4**	**P3**	**P2**	**P1**	**P0**
r				rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
Px (x=0-11)	x	rwh	**Port 4 Output Bit x** This bit determines the level at the output pin P4.x if the output is selected as GPIO output. 0_B The output level of P4.x is 0. 1_B The output level of P4.x is 1. P4.x can also be set/reset by control bits of the P4_OMR register.
0	31:12	r	**Reserved** Read as 0; should be written with 0.

26.8.5 Port Output Modification Register

The port output modification register contains control bits that make it possible to individually set, reset, or toggle the logic state of a single port line by manipulating the output register.

Table 294 Function of the Bits PRx and PSx

PRx	PSx	Function
0	0	Bit Pn_OUT.Px is not changed.
0	1	Bit Pn_OUT.Px is set.
1	0	Bit Pn_OUT.Px is reset.
1	1	Bit Pn_OUT.Px is toggled.

26.8.5.1 Register P0_OMR

P0_OMR Address: 0004_H

Port 0 Output Modification Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PR15	**PR14**	**PR13**	**PR12**	**PR11**	**PR10**	**PR9**	**PR8**	**PR7**	**PR6**	**PR5**	**PR4**	**PR3**	**PR2**	**PR1**	**PR0**
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PS15	**PS14**	**PS13**	**PS12**	**PS11**	**PS10**	**PS9**	**PS8**	**PS7**	**PS6**	**PS5**	**PS4**	**PS3**	**PS2**	**PS1**	**PS0**
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

Field	Bits	Type	Description
PSx (x=0-15)	x	w	**Port 0 Set Bit x** Setting this bit will set or toggle the corresponding bit in the port output register P0_OUT. The function of this bit is shown in ***Table 294***.
PRx (x=0-15)	x+16	w	**Port 0 Reset Bit x** Setting this bit will reset or toggle the corresponding bit in the port output register P0_OUT. The function of this bit is shown in ***Table 294***.

26.8.5.2 Register P1_OMR

P1_OMR Address: 0004_H

Port 1 Output Modification Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
			0				**PR8**	**PR7**	**PR6**	**PR5**	**PR4**	**PR3**	**PR2**	**PR1**	**PR0**
			r				w	w	w	w	w	w	w	w	w
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			0				**PS8**	**PS7**	**PS6**	**PS5**	**PS4**	**PS3**	**PS2**	**PS1**	**PS0**
			r				w	w	w	w	w	w	w	w	w

Field	Bits	Type	Description
PSx (x=0-8)	x	w	**Port 1 Set Bit x** Setting this bit will set or toggle the corresponding bit in the port output register P1_OUT. The function of this bit is shown in ***Table 294***.
PRx (x=0-8)	x+16	w	**Port 1 Reset Bit x** Setting this bit will reset or toggle the corresponding bit in the port output register P1_OUT. The function of this bit is shown in ***Table 294***.
0	15:9, 31:25	r	**Reserved** Read as 0; should be written with 0.

26.8.5.3 Register P2_OMR

P2_OMR Address: 0004_H

Port 2 Output Modification Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0		**PR13**	**PR12**	**PR11**	**PR10**	**PR9**	**PR8**	**PR7**	**PR6**	**PR5**	**PR4**	**PR3**	**PR2**	**PR1**	**PR0**
r		w	w	w	w	w	w	w	w	w	w	w	w	w	w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		**PS13**	**PS12**	**PS11**	**PS10**	**PS9**	**PS8**	**PS7**	**PS6**	**PS5**	**PS4**	**PS3**	**PS2**	**PS1**	**PS0**
r		w	w	w	w	w	w	w	w	w	w	w	w	w	w

Field	Bits	Type	Description
PSx (x=0-13)	x	w	**Port 2 Set Bit x** Setting this bit will set or toggle the corresponding bit in the port output register P2_OUT. The function of this bit is shown in ***Table 294***.
PRx (x=0-13)	x+16	w	**Port 2 Reset Bit x** Setting this bit will reset or toggle the corresponding bit in the port output register P2_OUT. The function of this bit is shown in ***Table 294***.
0	15:14, 31:30	r	**Reserved** Read as 0; should be written with 0.

26.8.5.4 Register P3_OMR

P3_OMR Address: 0004_H

Port 3 Output Modification Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0											**PR4**	**PR3**	**PR2**	**PR1**	**PR0**
r											w	w	w	w	w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0											**PS4**	**PS3**	**PS2**	**PS1**	**PS0**
r											w	w	w	w	w

Field	Bits	Type	Description
PSx (x=0-4)	x	w	**Port 3 Set Bit x** Setting this bit will set or toggle the corresponding bit in the port output register P3_OUT. The function of this bit is shown in ***Table 294***.

(continued)

Field	Bits	Type	Description
PRx (x=0-4)	x+16	w	**Port 3 Reset Bit x** Setting this bit will reset or toggle the corresponding bit in the port output register P3_OUT. The function of this bit is shown in ***Table 294***.
0	15:5, 31:21	r	**Reserved** Read as 0; should be written with 0.

26.8.5.5 Register P4_OMR

P4_OMR Address: 0004_H

Port 4 Output Modification Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0				PR11	PR10	PR9	PR8	PR7	PR6	PR5	PR4	PR3	PR2	PR1	PR0
r				w	w	w	w	w	w	w	w	w	w	w	w
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				PS11	PS10	PS9	PS8	PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0
r				w	w	w	w	w	w	w	w	w	w	w	w

Field	Bits	Type	Description
PSx (x=0-11)	x	w	**Port 4 Set Bit x** Setting this bit will set or toggle the corresponding bit in the port output register P4_OUT. The function of this bit is shown in ***Table 294***.
PRx (x=0-11)	x+16	w	**Port 4 Reset Bit x** Setting this bit will reset or toggle the corresponding bit in the port output register P4_OUT. The function of this bit is shown in***Table 294***.
0	15:12, 31:28	r	**Reserved** Read as 0; should be written with 0.

26.8.6 Port Input Register

The logic level of a GPIO pin can be read via the read-only port input register Pn_IN. Reading the Pn_IN register always returns the current logical value at the GPIO pin, synchronized to avoid meta-stabilities, independently whether the pin is selected as input or output.

26.8.6.1 Register P0_IN

P0_IN Address: 0024_H

Port 0 Input Register Reset Value: $0000\ XXXX_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
Px (x=0-15)	x	rh	**Port 0 Input Bit x** This bit indicates the level at the input pin P0.x. 0_B The input level of P0.x is 0. 1_B The input level of P0.x is 1.
0	31:16	r	**Reserved** Read as 0.

26.8.6.2 Register P1_IN

P1_IN Address: 0024_H

Port 1 Input Register Reset Value: $0000\ 0XXX_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0							P8	P7	P6	P5	P4	P3	P2	P1	P0
r							rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
Px (x=0-8)	x	rh	**Port 1 Input Bit x** This bit indicates the level at the input pin P1.x. 0_B The input level of P1.x is 0. 1_B The input level of P1.x is 1.
0	31:9	r	**Reserved** Read as 0.

26.8.6.3 Register P2_IN

P2_IN Address: 0024_H

Port 2 Input Register Reset Value: $0000\ XXXX_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0
r		rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
Px (x=0-13)	x	rh	**Port 2 Input Bit x** This bit indicates the level at the input pin P2.x. 0_B The input level of P2.x is 0. 1_B The input level of P2.x is 1.
0	31:14	r	**Reserved** Read as 0.

26.8.6.4 Register P3_IN

P3_IN Address: 0024_H

Port 3 Input Register Reset Value: $0000\ 00XX_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0											P4	P3	P2	P1	P0
r											rh	rh	rh	rh	rh

Field	Bits	Type	Description
Px (x=0-4)	x	rh	**Port 3 Input Bit x** This bit indicates the level at the input pin P3.x. 0_B The input level of P3.x is 0. 1_B The input level of P3.x is 1.
0	31:5	r	**Reserved** Read as 0.

26.8.6.5 Register P4_IN

P4_IN Address: 0024_H

Port 4 Input Register Reset Value: $0000\ 0XXX_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0
r				rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
Px (x=0-11)	x	rh	**Port 4 Input Bit x** This bit indicates the level at the input pin P4.x. 0_B The input level of P4.x is 0. 1_B The input level of P4.x is 1.
0	31:12	r	**Reserved** Read as 0.

26.8.7 Port Pin Power Save Register

When the IMC300A enters Deep-Sleep mode, pins with enabled Pin Power Save option are set to a defined state and the input Schmitt-Trigger as well as the output driver stage are switched off.

Note: Do not enable the Pin Power Save function for pins configured for Hardware Control (Pn_HWSEL.HWx != 00_B). Doing so may result in an undefined behavior of the pin when the device enters the Deep Sleep state.

Deep-Sleep Pin Power Save behavior

The actual behavior in Deep-Sleep mode with enabled Pin Power Save is controlled by the Pn_IOCRy.PCx bit field (***Port Input/Output Control Registers*** on page 857) of the respective pin. ***Table 295*** shows the coding.

Table 295 PCx Coding in Deep-Sleep mode

PCx[5:0]	I/O	Normal Operation or PPSx=0_B	Deep-Sleep mode and PPSx=1_B
$0XX000_B$	Direct Input	See ***Table 292***	Input value=Pn_OUTx
$0XX001_B$			Input value=0_B; pull-down deactivated
$0XX010_B$			Input value=1_B; pull-up deactivated
$0XX011_B$			Input value=Pn_OUTx, storing the last sampled input value
$0XX100_B$	Inverted Input	See ***Table 292***	Input value=$\overline{Pn_OUTx}$
$0XX101_B$			Input value=1_B; pull-down deactivated
$0XX110_B$			Input value=0_B; pull-up deactivated
$0XX111_B$			Input value=$\overline{Pn_OUTx}$, storing the last sampled input value
$1XXXXX_B$	Output	See ***Table 292***	Output driver off, Input Schmitt-Trigger off,

Table 295 PCx Coding in Deep-Sleep mode (continued)

PCx[5:0]	I/O	Normal Operation or PPSx=0_B	Deep-Sleep mode and PPSx=1_B
			no pull device active, Input value=Pn_OUTx

26.8.7.1 Register P0_PPS

P0_PPS Address: 0070_H

Port 0 Pin Power Save Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPS15	PPS14	PPS13	PPS12	PPS11	PPS10	PPS9	PPS8	PPS7	PPS6	PPS5	PPS4	PPS3	PPS2	PPS1	PPS0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
PPSx (x=0-15)	x	rw	**Port 0 Pin Power Save Bit x** 0_B Pin Power Save of P0.x is disabled. 1_B Pin Power Save of P0.x is enabled.
0	31:16	r	**Reserved** Read as 0.

26.8.7.2 Register P1_PPS

P1_PPS Address: 0070_H

Port 1 Pin Power Save Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0							PPS8	PPS7	PPS6	PPS5	PPS4	PPS3	PPS2	PPS1	PPS0
r							rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
PPSx (x=0-8)	x	rw	**Port 1 Pin Power Save Bit x** 0_B Pin Power Save of P1.x is disabled. 1_B Pin Power Save of P1.x is enabled.
0	31:9	r	**Reserved** Read as 0.

26.8.7.3 Register P2_PPS

P2_PPS Address: 0070_H

Port 2 Pin Power Save Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		**PPS13**	**PPS12**	**PPS11**	**PPS10**	**PPS9**	**PPS8**	**PPS7**	**PPS6**	**PPS5**	**PPS4**	**PPS3**	**PPS2**	**PPS1**	**PPS0**
r		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
PPSx (x=0-13)	x	rw	**Port 2 Pin Power Save Bit x** 0_B Pin Power Save of P2.x is disabled. 1_B Pin Power Save of P2.x is enabled.
0	31:14	r	**Reserved** Read as 0.

26.8.7.4 Register P3_PPS

P3_PPS Address: 0070_H

Port 3 Pin Power Save Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0											**PPS4**	**PPS3**	**PPS2**	**PPS1**	**PPS0**
r											rw	rw	rw	rw	rw

Field	Bits	Type	Description
PPSx (x=0-4)	x	rw	**Port 3 Pin Power Save Bit x** 0_B Pin Power Save of P3.x is disabled. 1_B Pin Power Save of P3.x is enabled.
0	31:5	r	**Reserved** Read as 0.

26.8.7.5 Register P4_PPS

P4_PPS Address: 0070_H

Port 4 Pin Power Save Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				**PPS11**	**PPS10**	**PPS9**	**PPS8**	**PPS7**	**PPS6**	**PPS5**	**PPS4**	**PPS3**	**PPS2**	**PPS1**	**PPS0**
r				rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
PPSx (x=0-11)	x	rw	**Port 4 Pin Power Save Bit x** 0_B Pin Power Save of P4.x is disabled. 1_B Pin Power Save of P4.x is enabled.
0	31:12	r	**Reserved** Read as 0.

26.8.8 Port Pin Hardware Select Register

Some peripherals require direct hardware control of their I/Os. As multiple such peripheral I/Os are mapped on some pins, the register Pn_HWSEL is used to select which peripheral has the control over the pin.

Note: Pn_HWSEL.HWx just pre-assigns the hardware-control of the pin to a certain peripheral, but the peripheral itself decides when to take control over it. As long as the peripheral does not take control of a given pin via HWx_EN, the configuration of this pin is still defined by the configuration registers and it is available as GPIO or for other alternate functions. This might be because the selected peripheral has provisions to just activate a subset of its pins, or because the peripheral is not active at all.

This mechanism can also be used to prohibit the hardware control of certain pins to a peripheral, in case the application does not need the respective functionality and the peripheral has no provisions to disable the hardware control selectively.

26.8.8.1 Register P0_HWSEL

P0_HWSEL Address: 0074_H

Port 0 Pin Hardware Select Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW15		**HW14**		**HW13**		**HW12**		**HW11**		**HW10**		**HW9**		**HW8**	
rw		rw		rw		rw		rw		rw		rw		rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW7		**HW6**		**HW5**		**HW4**		**HW3**		**HW2**		**HW1**		**HW0**	
rw		rw		rw		rw		rw		rw		rw		rw	

Field	Bits	Type	Description
HWx (x=0-15)	2*x+1:2*x	rw	**Port 0 Pin Hardware Select Bit x** 00_B Software control only. 01_B HW0 control path can override the software configuration. 10_B HW1 control path can override the software configuration. 11_B Reserved.

26.8.8.2 Register P1_HWSEL

P1_HWSEL Address: 0074_H

Port 1 Pin Hardware Select Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0														**HW8**	
r														rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW7		**HW6**		**HW5**		**HW4**		**HW3**		**HW2**		**HW1**		**HW0**	
rw		rw		rw		rw		rw		rw		rw		rw	

Field	Bits	Type	Description
HWx (x=0-8)	2*x+1:2*x	rw	**Port 1 Pin Hardware Select Bit x** 00_B Software control only. 01_B HW0 control path can override the software configuration. 10_B HW1 control path can override the software configuration. 11_B Reserved.
0	31:18	r	**Reserved** Read as 0; should be written with 0.

26.8.8.3 Register P2_HWSEL

P2_HWSEL Address: 0074_H

Port 2 Pin Hardware Select Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0				HW13		HW12		HW11		HW10		HW9		HW8	
r				rw		rw		rw		rw		rw		rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW7		HW6		HW5		HW4		HW3		HW2		HW1		HW0	
rw		rw		rw		rw		rw		rw		rw		rw	

Field	Bits	Type	Description
HWx (x=0-13)	2*x+1:2*x	rw	**Port 2 Pin Hardware Select Bit x** 00_B Software control only. 01_B HW0 control path can override the software configuration. 10_B HW1 control path can override the software configuration. 11_B Reserved.
0	31:28	r	**Reserved** Read as 0; should be written with 0.

26.8.8.4 Register P3_HWSEL

P3_HWSEL Address: 0074_H

Port 3 Pin Hardware Select Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0						HW4		HW3		HW2		HW1		HW0	
r						rw		rw		rw		rw		rw	

Field	Bits	Type	Description
HWx (x=0-4)	2*x+1:2*x	rw	**Port 3 Pin Hardware Select Bit x** 00_B Software control only. 01_B HW0 control path can override the software configuration. 10_B HW1 control path can override the software configuration. 11_B Reserved.
0	31:10	r	**Reserved** Read as 0; should be written with 0.

26.8.8.5 Register P4_HWSEL

P4_HWSEL Address: 0074_H

Port 4 Pin Hardware Select Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0								HW11		HW10		HW9		HW8	
r								rw		rw		rw		rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW7		HW6		HW5		HW4		HW3		HW2		HW1		HW0	
rw		rw		rw		rw		rw		rw		rw		rw	

Field	Bits	Type	Description
HWx (x=0-11)	2*x+1:2*x	rw	**Port 4 Pin Hardware Select Bit x** 00_B Software control only. 01_B HW0 control path can override the software configuration. 10_B HW1 control path can override the software configuration. 11_B Reserved.
0	31:24	r	**Reserved** Read as 0; should be written with 0.

26.9 Port I/O Functions

26.9.1 Port Pin for Boot Modes

Port functions can be overruled by the boot mode selected. The type of boot mode is selected via BMI. ***Table 296*** shows the port pins used for the various boot modes.

Table 296 Port Pin for Boot Modes

Boot	Boot Description
Pin: P0.13	
CS(O)	SSC BSL mode
Pin: P0.14	
SWDIO_0	Debug mode (SWD)
SPD_0	Debug mode (SPD)
RX/TX	ASC BSL half-duplex mode
RX	ASC BSL full-duplex mode
RX	CAN BSL mode
SCLK(O)	SSC BSL mode
Pin: P0.15	
SWDCLK_0	Debug mode (SWD)
TX	ASC BSL full-duplex mode

Table 296 Port Pin for Boot Modes (continued)

Boot	Boot Description
TX	CAN BSL mode
DATA(I/O)	SSC BSL mode
Pin: P4.6	
HWCON0	Boot Pins (Boot-from-pins mode must be selected)
Pin: P4.7	
HWCON1	Boot Pins (Boot-from-pins mode must be selected)

26.9.2 Port I/O Function Description

The following general building blocks ares used to describe the I/O functions of each PORT pin:

Table 297 Port Input Function Description

Pin	Functions	Functions
P0.0	MODC.INA	
Pn.y	MODA.INA	MODC.INB

Table 298 Port Output Function Description

Pin	ALT1	ALTn
P0.0		MODA.OUT
Pn.y	MODA.OUT	

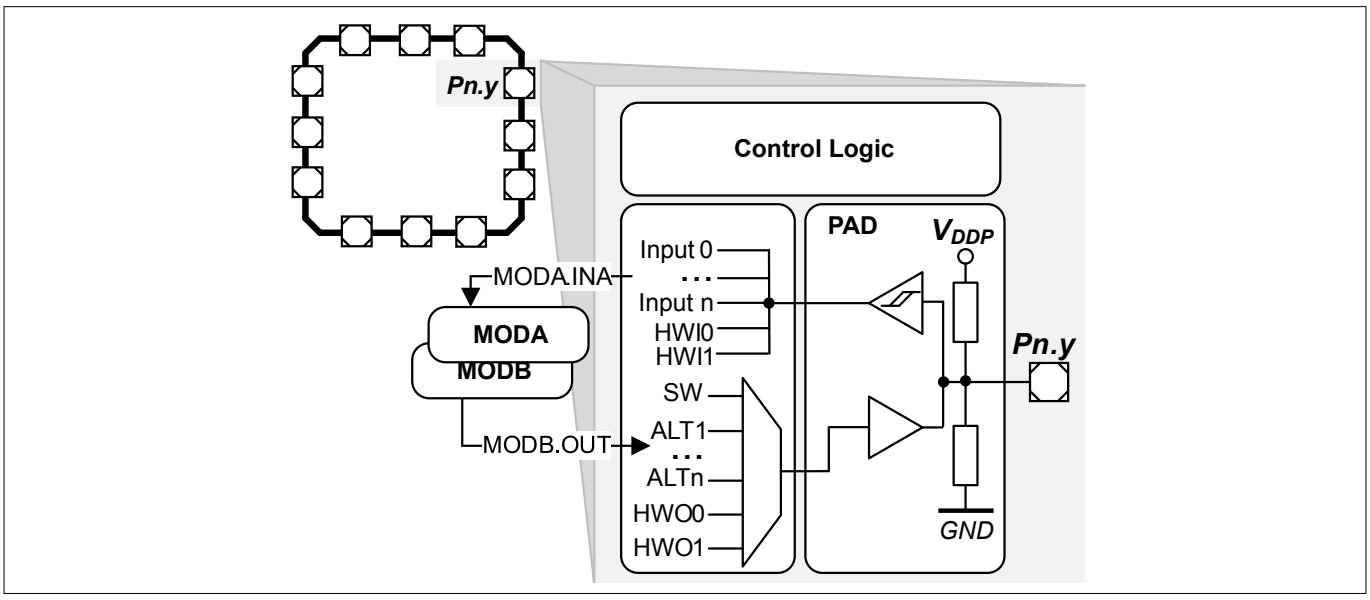


Figure 278 Simplified Port Structure

Pn.y is the port pin name, defining the control and data bits/registers associated with it. As GPIO, the port is under software control. Its input value is read via Pn_IN.y, Pn_OUT defines the output value.

Up to nine alternate output functions (ALT1 to ALT9) can be mapped to a single port pin, selected by Pn_IOCR.PC. The output value is directly driven by the respective module, with the pin characteristics controlled by the port registers (within the limits of the connected pad).

The input path is also active while the pin is configured as output. This allows to feedback an output to on-chip resources without wasting an additional external pin.

The port pin input can be connected to multiple peripherals. Most peripherals have an input multiplexer to select between different possible input sources.

Table 299 Port Input Functions

Pin	Func-tions	Func-tions	Func-tions	Func-tions	Func-tions	Func-tions	Func-tions	Func-tions	Func-tions	Func-tions	Func-tions	Func-tions
P0.8/ RTC_XTAL1		CCU40.IN2AB						USIC0_CH0.DX1B		USIC0_CH1.DX1B		
P0.9/ RTC_XTAL2		CCU40.IN3AB						USIC0_CH0.DX2B		USIC0_CH1.DX2B		
P0.10/ XTAL1								USIC0_CH0.DX2C		USIC0_CH1.DX2C		
P0.11/ XTAL2								USIC0_CH0.DX2D		USIC0_CH1.DX2D		
P0.12		CCU40.IN0AA	CCU40.IN1AA	CCU40.IN2AA		CCU40.IN3AA		USIC0_CH0.DX2E			CAN.N1_RXDA	
P0.13								USIC0_CH0.DX2F			CAN.N1_RXDB	
P0.14							USIC0_CH0.DX0A	USIC0_CH0.DX1A			CAN.N0_RXDC	
P0.15							USIC0_CH0.DX0B				CAN.N0_RXDD	
P1.0							USIC0_CH0.DX0C				CAN.N0_RXDG	
P1.1							USIC0_CH0.DX0D	USIC0_CH0.DX1D		USIC0_CH1.DX2E	CAN.N0_RXDH	
P2.0		VADC0.CH5					USIC0_CH0.DX0E	USIC0_CH0.DX1E		USIC0_CH1.DX2F	CAN.N0_RXDE	ERU0.0B0

Table 299 Port Input Functions (continued)

Pin	Func-tions	Func-tions	Func-tions	Func-tions	Func-tions	Func-tions	Func-tions	Func-tions	Func-tions	Func-tions	Func-tions	Func-tions
P2.1	ACMP2.INP	VADC0.CH6					USIC0_CH0.DX0F		USIC0_CH1.DX3A	USIC0_CH1.DX4A	CAN.N0_RXDF	ERU0.1B0
P2.2	ACMP2.INN	VADC0.CH7		ORC0.AIN	USIC1_CH0.DX5E		USIC0_CH0.DX3A	USIC0_CH0.DX4A	USIC0_CH1.DX5A			ERU0.0B1
P2.6	ACMP1.INN	VADC0.CH0		ORC4.AIN			USIC0_CH0.DX3E	USIC0_CH0.DX4E	USIC0_CH1.DX5D			ERU0.2A1
P2.8	ACMP0.INN	VADC0.CH1		ORC6.AIN			USIC0_CH0.DX3D	USIC0_CH0.DX4D	USIC0_CH1.DX5C			ERU0.3B1
P2.10		VADC0.CH3					USIC0_CH0.DX3C	USIC0_CH0.DX4C	USIC0_CH1.DX0F		CAN.N1_RXDE	ERU0.2B0
P2.11	ACMP.REF	VADC0.CH4							USIC0_CH1.DX0E	USIC0_CH1.DX1E	CAN.N1_RXDF	ERU0.2B1
P4.0		CCU40.IN0BA	CCU41.IN0AC				USIC1_CH0.DX3D	USIC1_CH0.DX4D				
P4.1		CCU40.IN1BA	CCU41.IN1AC			POSIF1.IN0B	USIC1_CH0.DX5C					
P4.2		CCU40.IN2BA	CCU41.IN2AC			POSIF1.IN1B	USIC1_CH0.DX5D					
P4.3		CCU40.IN3BA	CCU41.IN3AC			POSIF1.IN2B		USIC1_CH0.DX1B				
P4.4			CCU41.IN0AV				USIC1_CH0.DX0C					ERU1.0A2
P4.5			CCU41.IN1AV				USIC1_CH0.DX0D	USIC1_CH0.DX1C				ERU1.1A2
P4.6			CCU41.IN2AV					USIC1_CH0.DX1D				ERU1.2A2
P4.7			CCU41.IN3AV					USIC1_CH0.DX2A				ERU1.0A3

Table 300 Port Output Functions

Non-listed pins have no port output functions.

Pin	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
P0.8/ RTC_XTAL1	DAC0.OUT4			CCU40.OUT2		USIC0_CH0.SCLKOUT	USIC0_CH1.SCLKOUT		CCU41.OUT2
P0.9/ RTC_XTAL2	DAC0.OUT5			CCU40.OUT3		USIC0_CH0.SELO0	USIC0_CH1.SELO0		CCU41.OUT3
P0.10/ XTAL1	DAC0.OUT6			ACMP0.OUT		USIC0_CH0.SELO1	USIC0_CH1.SELO1		
P0.11/ XTAL2	DAC0.OUT7			USIC0_CH0.MCLKOUT		USIC0_CH0.SELO2	USIC0_CH1.SELO2		
P0.12	DAC0.OUT6					USIC0_CH0.SELO3			CAN.N1_TXD
P0.13	WWDT.SERVICE_OUT					USIC0_CH0.SELO4			CAN.N1_TXD
P0.14	DAC0.OUT7					USIC0_CH0.DOUT0	USIC0_CH0.SCLKOUT		CAN.N0_TXD
P0.15	DAC0.OUT8					USIC0_CH0.DOUT0	USIC0_CH1.MCLKOUT		CAN.N0_TXD
P1.0	DAC0.OUT0	CCU40.OUT0				ACMP1.OUT	USIC0_CH0.DOUT0		CAN.N0_TXD
P1.1	ERU1.PDOUT1	CCU40.OUT1				USIC0_CH0.DOUT0	USIC0_CH1.SELO0		CAN.N0_TXD
P2.0	ERU0.PDOUT3	CCU40.OUT0	ERU0.GOUT3			USIC0_CH0.DOUT0	USIC0_CH0.SCLKOUT		CAN.N0_TXD
P2.1	ERU0.PDOUT2	CCU40.OUT1	ERU0.GOUT2			USIC0_CH0.DOUT0	USIC0_CH1.SCLKOUT		CAN.N0_TXD
P2.10	ERU0.PDOUT1	CCU40.OUT2	ERU0.GOUT1			ACMP0.OUT	USIC0_CH1.DOUT0		CAN.N1_TXD
P2.11	ERU0.PDOUT0	CCU40.OUT3	ERU0.GOUT0			USIC0_CH1.SCLKOUT	USIC0_CH1.DOUT0		CAN.N1_TXD

Table 300 Port Output Functions (continued)

Non-listed pins have no port output functions.

Pin	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
P4.0	DAC0.OUT0	ERU1.PDOUT0		ERU1.GOUT0	CCU40.OUT0	ACMP1.OUT			CCU41.OUT0
P4.1	DAC0.OUT8	ERU1.PDOUT1		ERU1.GOUT1	CCU40.OUT1	ACMP3.OUT			CCU41.OUT1
P4.2	DAC0.OUT4	ERU1.PDOUT2		ERU1.GOUT2	CCU40.OUT2	ACMP2.OUT			CCU41.OUT2
P4.3	DAC0.OUT5	ERU1.PDOUT3		ERU1.GOUT3	CCU40.OUT3	ACMP0.OUT	USIC1_CH0.SCLKOUT		CCU41.OUT3
P4.4	DAC0.OUT0					USIC1_CH0.DOUT0			CCU41.OUT0
P4.5	DAC0.OUT8					USIC1_CH0.DOUT0	USIC1_CH0.SCLKOUT		CCU41.OUT1
P4.6	DAC0.OUT2						USIC1_CH0.SCLKOUT		CCU41.OUT2
P4.7	DAC0.OUT5						USIC1_CH0.SELO0		CCU41.OUT3

26.9.3 Hardware Controlled I/O Function Description

The following general building block is used to describe the hardware I/O and pull control functions of each PORT pin:

Table 301 Hardware Controlled I/O Function Description

Function	Outputs	Inputs	Pull Control	
	HWO0	HWI0	HW0_PD	HW0_PU
P0.0	MODB.OUT	MODB.INA		
Pn.y			$\overline{\text{MODC.OUT}}$	MODC.OUT

By Pn_HWSEL (*Chapter 26.8.8*) it is possible to select between different hardware “masters” (HWO0/HWI0, HWO1/HWI1). The selected peripheral can take control of the pin(s). Hardware control overrules settings in the respective port pin registers. Additional hardware signals HW0_PD/HW1_PD and HW0_PU/HW1_PU controlled by the peripherals can be used to control the pull devices of the pin.

Table 302 Hardware Controlled I/O Functions

Non-listed pins have no hardware controlled I/O and pull control function.

Pin	Outputs		Inputs		Pull Control			
	HWO0	HWO1	HWI0	HWI1	HW0_PD	HW0_PU	HW1_PD	HW1_PU
P1.0		USIC0_CH0.DOUT0		USIC0_CH0.HWIN0	$\overline{\text{DAC0.OUT2}}$	DAC0.OUT2		
P1.1		USIC0_CH0.DOUT1		USIC0_CH0.HWIN1	$\overline{\text{DAC0.OUT3}}$	DAC0.OUT3		
P2.0					$\overline{\text{DAC0.OUT1}}$	DAC0.OUT1		
P2.1					$\overline{\text{DAC0.OUT6}}$	DAC0.OUT6		
P2.2					$\overline{\text{DAC0.OUT0}}$	DAC0.OUT0	$\overline{\text{CCU40.OUT3}}$	CCU40.OUT3
P2.6					$\overline{\text{DAC0.OUT2}}$	DAC0.OUT2	$\overline{\text{CCU40.OUT3}}$	CCU40.OUT3
P2.8					$\overline{\text{DAC0.OUT1}}$	DAC0.OUT1	$\overline{\text{CCU40.OUT2}}$	CCU40.OUT2
P2.10					$\overline{\text{DAC0.OUT4}}$	DAC0.OUT4		
P2.11					$\overline{\text{DAC0.OUT5}}$	DAC0.OUT5		

26.10 Pad Characteristics

This section provides a general overview of the pad characteristics.

26.10.1 Input and Output Voltage

Figure 279 explains the input voltage ranges of V_{IN} and V_{AIN} and its dependency to the supply level of V_{DDP}. The input voltage must not exceed 6.0 V, and it must not be more than 0.5 V above V_{DDP}. For the range up to V_{DDP} + 0.5 V also see the definition of the overload conditions in ***Chapter 26.10.4***.

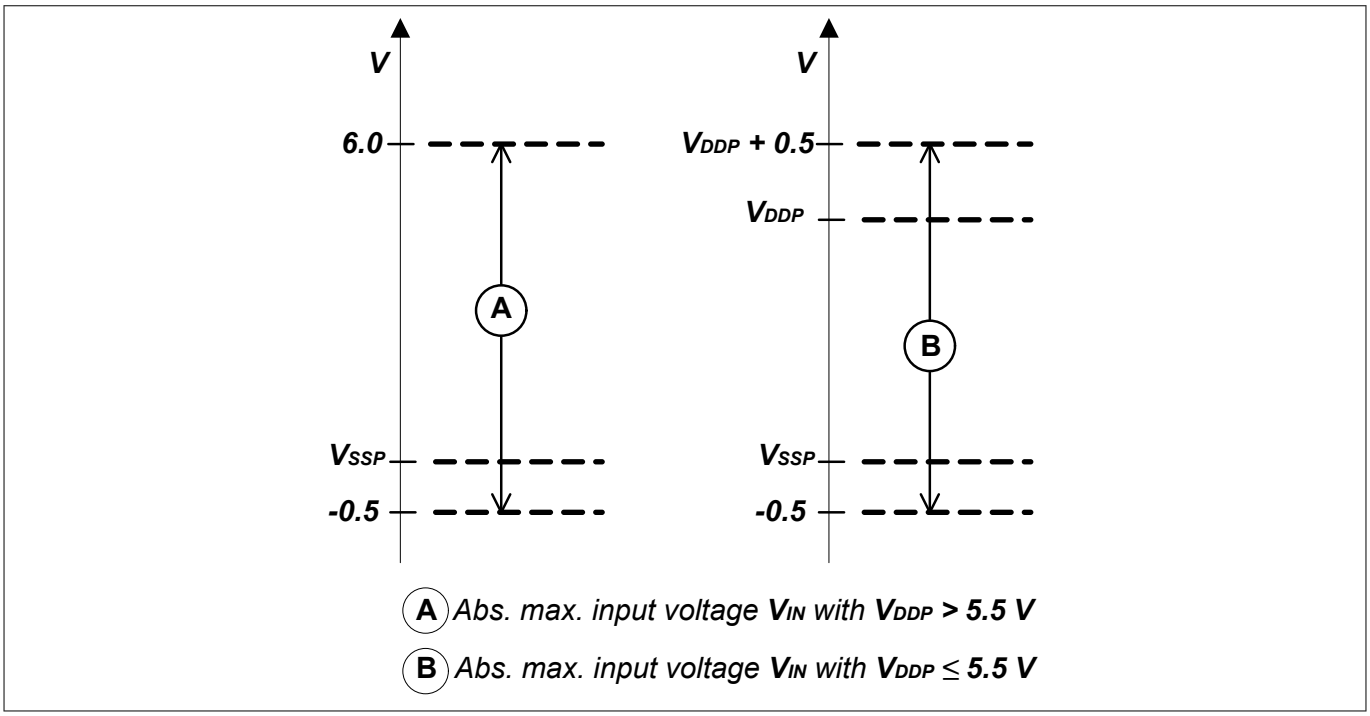


Figure 279 Absolute Maximum Input Voltage Ranges

26.10.2 Input Low and Input High Voltage

Figure 280 explains the Input Low Voltage, V_{ILPS}/V_{ILPL} and Input High Voltage, V_{IHPS}/V_{ILPL} and their ranges in Standard Hysteresis mode (S) and Large Hysteresis mode (L).

V_{ILPx} defines the maximum voltage level that will be interpreted as a '0' by a digital input.V_{IHPx} defines the minimum voltage level that will be interpreted as a '1' by a digital input.

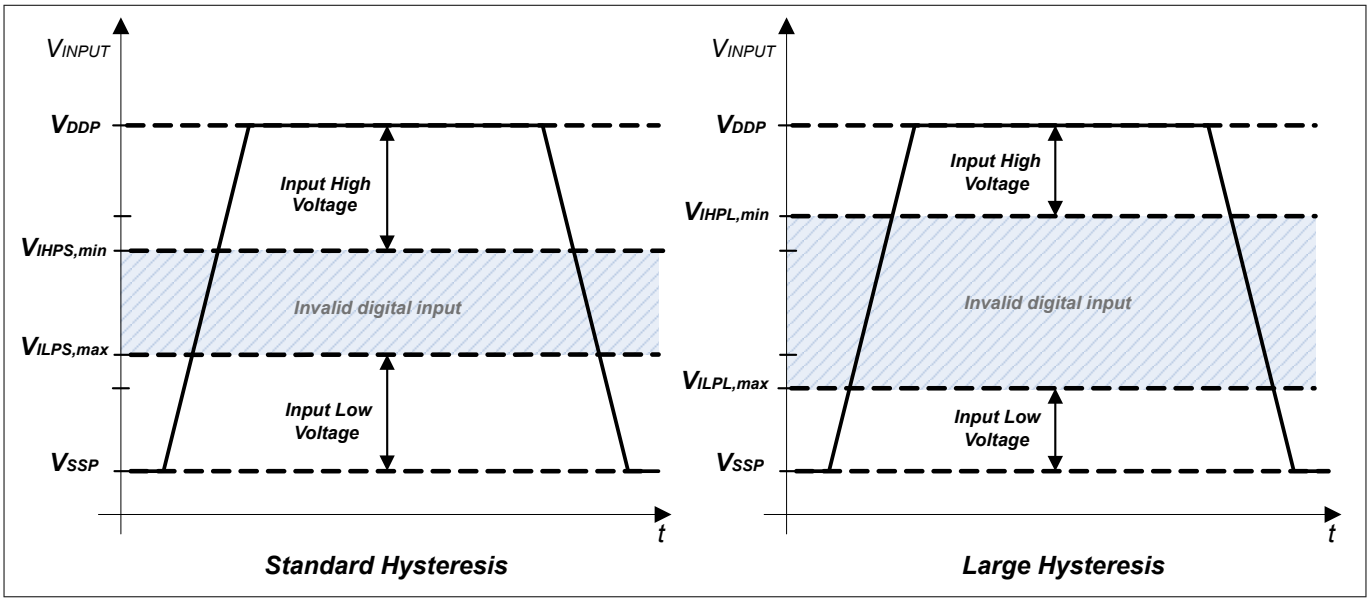


Figure 280 Input Low Voltage and Input High Voltage

A voltage level between V_{ILPx} and V_{IHPx} will result in an undefined logic state. It could be interpreted as either '0' or '1' by the circuit that received these inputs. In addition, most CMOS inputs will draw excessive current if an undefined voltage level is applied.

26.10.3 Output Low and Output High Voltage

V_{OLP} defines the maximum voltage level that will appear on a digital output set to '0'. V_{OHP} defines the minimum voltage level that will appear on a digital output set to '1'.

The output parameters are usually given for a specified I_{OL}, as the output levels are dependant on the load impedance applied to the logic output.

Figure 281 and ***Figure 282*** explain the Output Low Voltage, V_{OLP} and Output High Voltage, V_{OHP} and its depenency to the 2 different output load current, I_{OL_Lx} / I_{OH_Lx}.

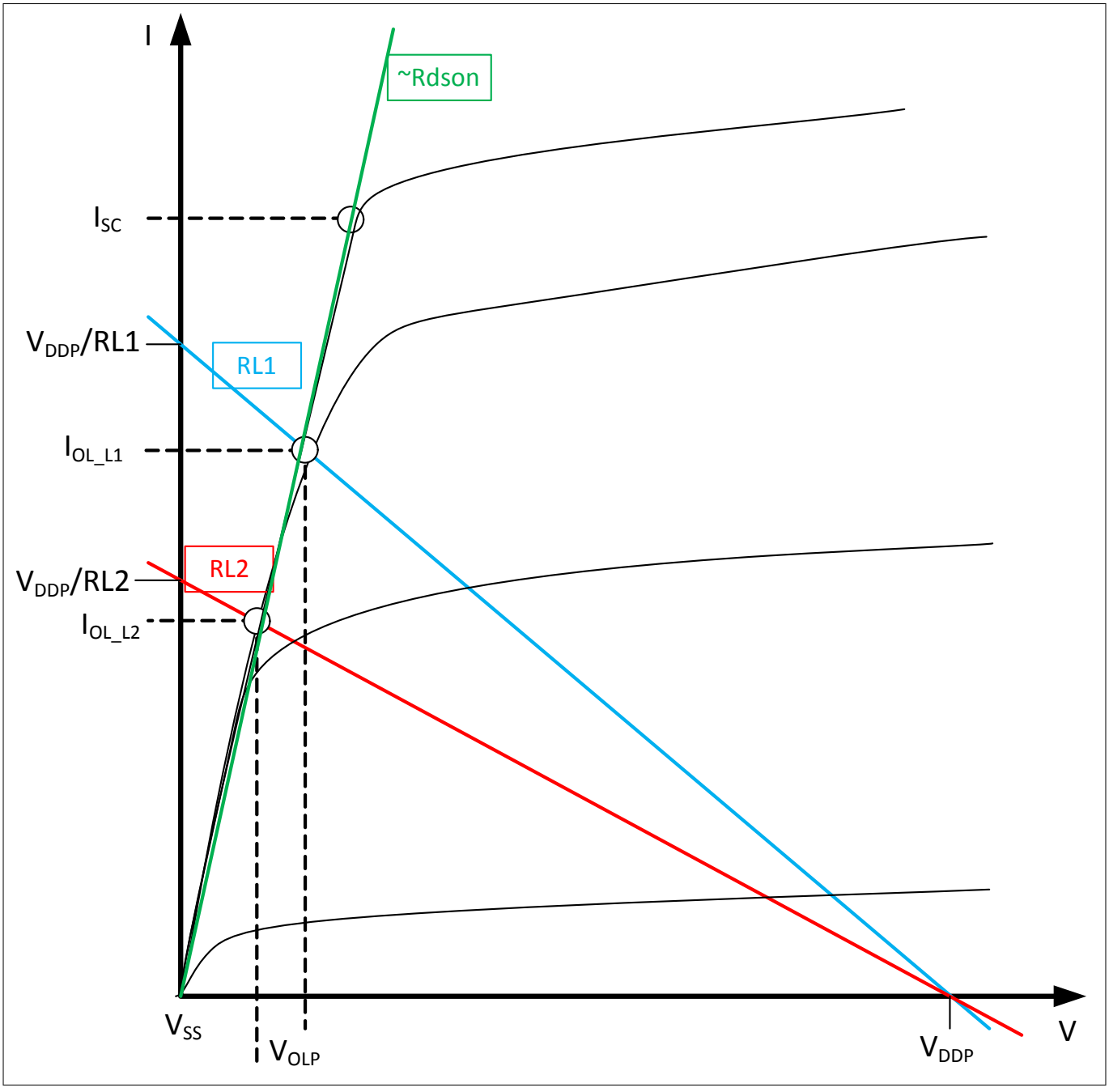


Figure 281 Output Low Voltage

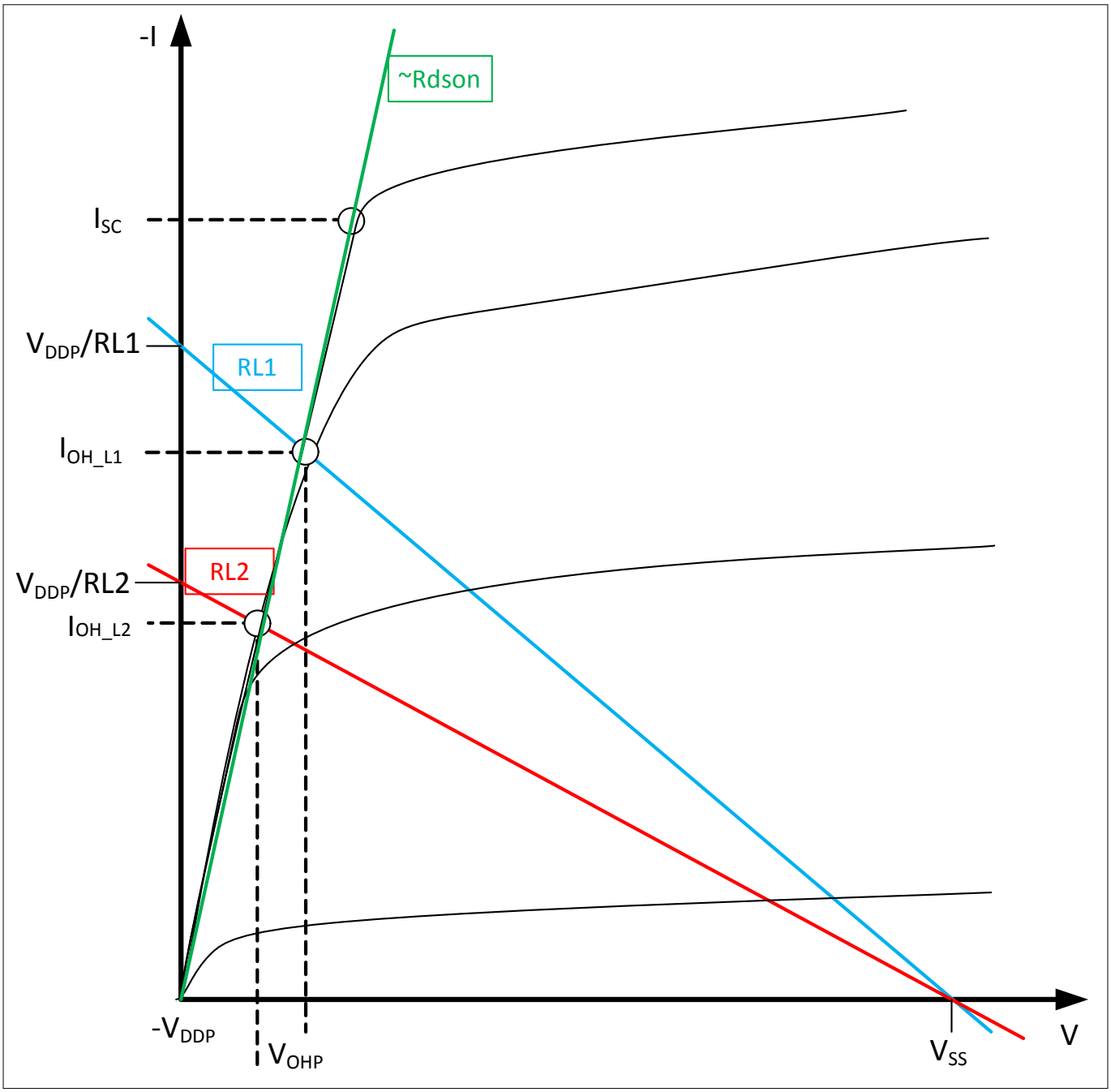


Figure 282 Output High Voltage

26.10.4 Pin Reliability in Overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

If a pin current is outside of the operating conditions but within the overload conditions, then the parameters of this pin as stated in the operating conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

Note: An overload condition on one or more pins does not require a reset.

Note: A series resistor at the pin to limit the current to the maximum permitted overload current is sufficient to handle failure situations like short to battery.

Figure 283 shows the path of the input currents during overload via the ESD protection structures. The diodes against V_{DDP} and ground are a simplified representation of these ESD protection structures.

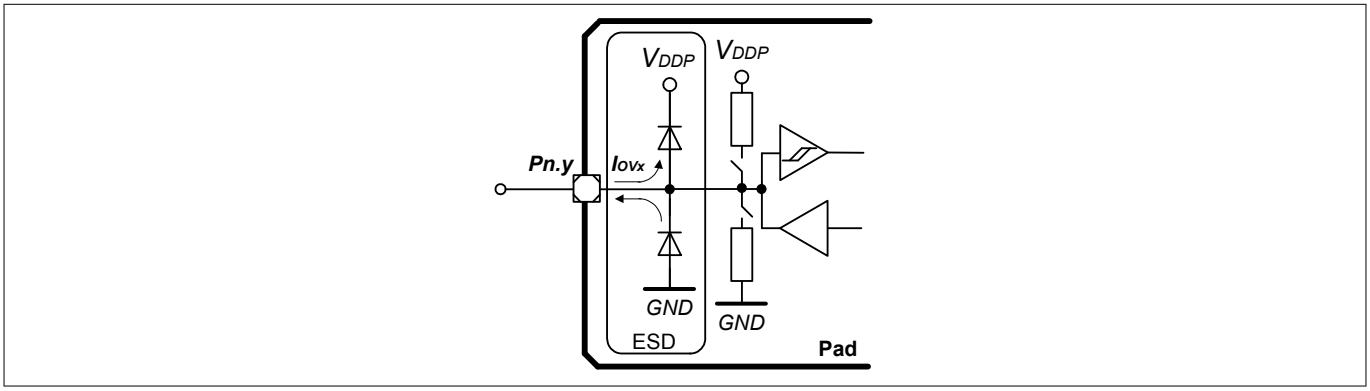


Figure 283 Input Overload Current via ESD structures

Refer to the Datasheet for the overload conditions and limits that will not cause any negative reliability impact .

26.10.5 Internal Pull Device

Figure 284 visualizes the input characteristics with an active internal pull device:

- in the cases “A” the internal pull device is overridden by a strong external driver;
- in the cases “B” the internal pull device defines the input logical state against a weak external load.

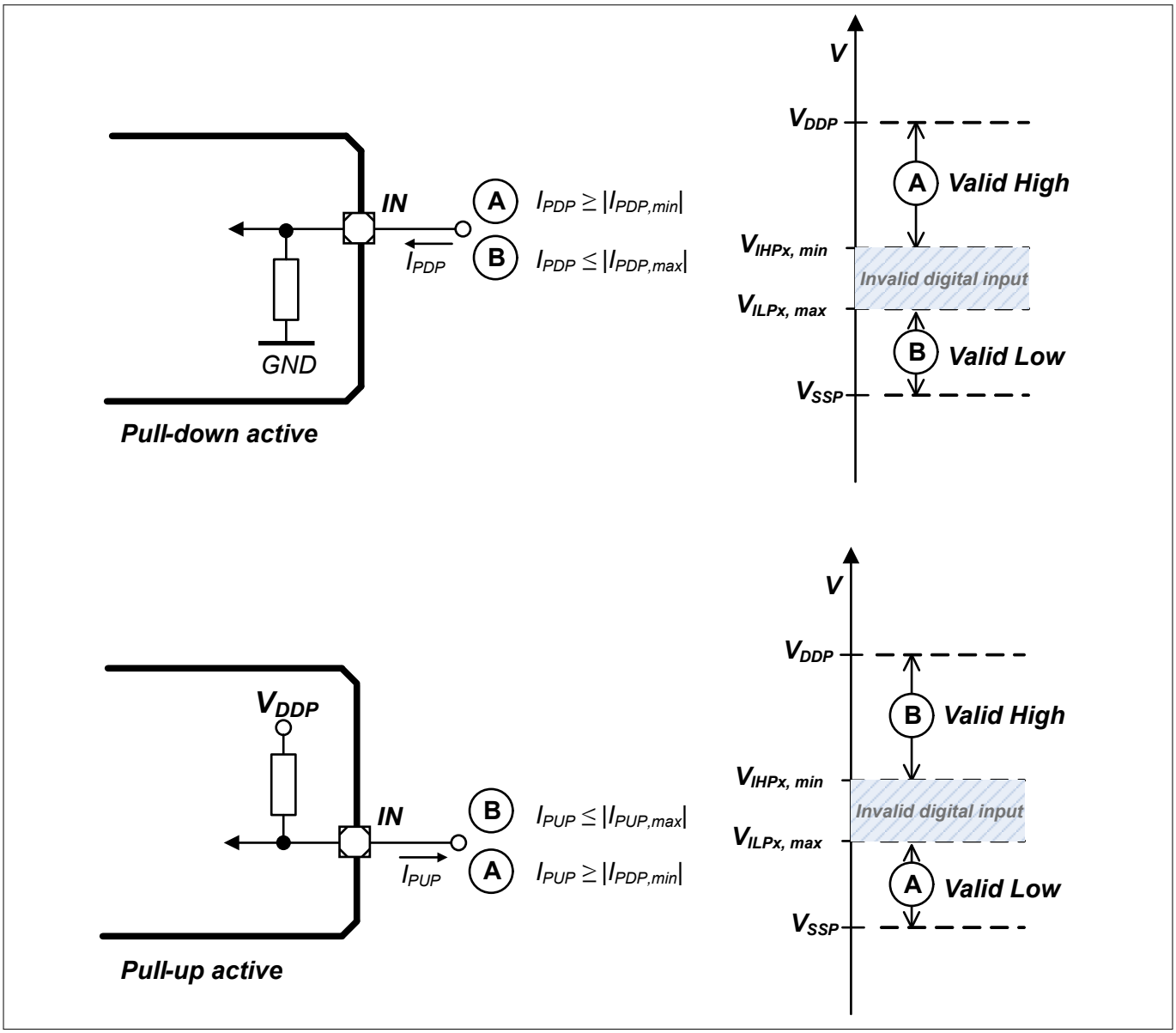


Figure 284 Pull Device Input Characteristics

27 Boot and Startup

The startup sequence of the IMC300A is a process taking place before user application software takes control of the system and is comprising of two major phases (see ***Figure 285***), split in several distinctive steps:

Hardware Controlled Startup Phase

The hardware controlled startup phase gets performed automatically after power up of the microcontroller. This part is generic and it ensures basic configuration common to most applications. The hardware setup needs to ensure fulfillment of requirements specified in Data Sheet in order to enable reliable start up of the microcontroller before control is handed over to the user software. The sequence where boot code gets executed is considered a part of the hardware controlled phase of the startup sequence.

For details of the setup requirements, please refer to Data Sheet.

Software Controlled Startup Phase

The software controlled startup phase is the part where the application specific configuration gets applied with user software. It involves several steps that are critical for proper operation of the microcontroller in the application context and may also involve some optional configuration actions in order to improve system performance and stability in the application context.

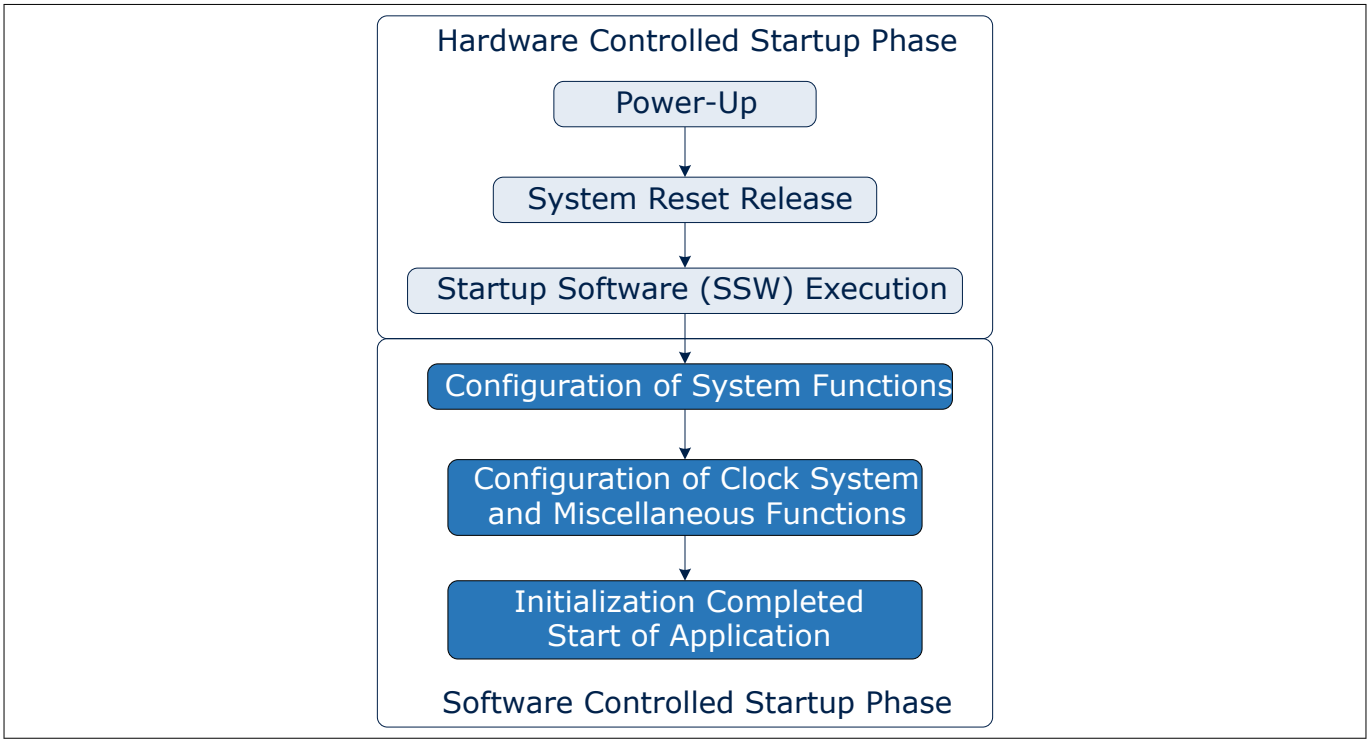


Figure 285 Startup sequence

27.1 Startup Sequence and System Dependencies

A more detailed description of the startup sequence is available in the following sub-chapters.

27.1.1 Power-Up

Power up of the microcontroller gets performed by applying V_{DDP} supply (for details of the supply requirements, please refer to Data Sheet). Once V_{DDP} reaches a threshold, the internal core voltage, V_{DDC}, is generated automatically by the EVR.

27.1.2 System Reset Release

The internal power-on reset generation is based on the supply and core voltage validation. When V_{DDP} and V_{DDC} reaches a stable threshold level, the power-on reset is released. Next, after the on-chip oscillators generate a stable clock output, the system reset is released automatically and the SSW code starts to run.

The system reset can be triggered from various sources like software controlled CPU reset register or a watchdog time-out-triggered reset. For more details on reset control details, please refer to the Reset Control Unit (RCU) section in the SCU chapter.

The cause of the last reset gets automatically stored in the SCU_RSTSTAT register and can be checked by user software to determine the state of the system and for debug purpose. The reset status in the SCU_RSTSTAT register shall be reset with SCU_RSTCLR register after each startup in order to ensure consistent source indication after the next reset.

After reset release, MCLK and PCLK are running at 8MHz and most of the peripherals' clocks are disabled except for CPU, memories and PORT. It is recommended to disable the clock of the unused modules in order to reduce power consumption.

27.1.3 Startup Software (SSW) Execution

After the reset is deasserted, CPU starts to execute the SSW code from the ROM memory. To indicate the start of the SSW execution, the pullup device in P0.14 is enabled. Pullup device is disabled during reset.

SSW reads the Boot Mode Index (BMI) stored in Flash and decide the startup mode selected by the user. For more details about the various startup modes and handling of BMI, please refer to ***Chapter 27.2***.

To handle the initial hardfault error during the SSW execution, SSW installs "jump to itself" instruction at SRAM location $2000'000C_H$ as temporary HardFault handler - until the user code installs its own. It is installed upon master reset only.

During SSW execution, the SRAM area between $2000'00C0_H$ and $2000'0200_H$ is reserved for usage by IMC300A SSW, therefore the user software should not store in this area data which must be preserved throughout (non-power) resets.

The MCLK and PCLK frequency that is used to execute the SSW and to start the user code can be configured by user. In addition, some of the peripheral clock can also be enabled (default disabled) by the SSW. Detailed description can be found in the ***Chapter 27.1.3.1***.

27.1.3.1 Clock system handling by SSW

IMC300A SSW is able to change device clock settings to allow flexibility of device performance e.g. speed vs. power consumption optimization during start-up.

The clock handling by SSW is user configurable by installing values in Flash. For this purpose two word locations - CLK_VAL1 and CLK_VAL2 - are assigned in Flash (refer to ***Table 305***), the values from these locations are processed by SSW as follows:

- if CLK_VAL1[31]=0 - CLK_VAL1[21:10], [7:0] bits are installed into SCU_CLKCR bit fields [19:8], [7:0] register, respectively and CLK_VAL1[9:8] into SCU_CLKCR1.[1:0]- this configures clock dividers and selection
- if CLK_VAL2[31]=0 - CLK_VAL2[21:16],[10:0] bits are installed into SCU_CGATCLR0 bit fields [21:16] and [10:0], respectively - this enables the clock of the selected peripherals

In case some CLK_VALx location is not programmed by the user - like in device delivery state - its bit[31]=1 and no installation is done into the respective register(s).

Limited device frequency change

To avoid big jumps/drops in power consumption, the user-configurable value to be installed during start-up from CLK_VAL1 into CLKCR.IDIV is limited to the range 1..16, resulting in possible range of MCLK after re-

configuration 3..48 MHz from initial 8MHz - i.e. MCLK frequency can be increased or decreased no more than 4 times (rounded, ignoring potential FDIV influence).

In case CLK_VAL1 (refer to ***Table 305***) contains IDIV value out of the 1..16 range:

- if IDIV=0 - SSW installs IDIV=1 instead
- if IDIV>16 - SSW install IDIV=16 instead

27.1.4 Configuration of Special System Functions as part of User code initialization

Special system functions are may be required to perform actions that improve system stability and robustness. The following special system functions or modules require initialization as part of the User code initialization before the actual user application starts:

- Start Address and Initial Stack Pointer Value
- Setup the Interrupt handler
- Supply Voltage Brown-out Detection
- Watchdog Timer (WDT)

Start Address and Initial Stack Pointer Value

The start address and the inital stack pointer values in ***Table 305*** need to be defined by the user. It can be done together with the downloading of the user code into the flash memory.

Setup the Interrupt Handler

The vector table is remapped to the SRAM based on the remapped vector table in CPU chapter. The interrupt service routine can be placed in these SRAM address or user can also have a branch instruction to the routine that is placed in other memory location. For details, please refer to CPU chapter.

V_{DDP} Brown Out Detection

V_{DDP} brown out detection mechanism allow active monitoring of the supply voltage and a corrective reaction in case the voltage level is below a programmed threshold. An interrupt request will be flagged if a programmed condition is detected. For details, please refer to the Power Control Unit (PCU) section in the SCU chapter.

Watchdog Timer

The Watchdog Timer requires a clock source selection and activation. It is highly recommended to use reliable clock source, preferably independent from the system clock source in order to ensure corrective action in case of a system failure which will bring the microcontroller into a safe operation state. In IMC300A, the default WDT clock is the standby clock. For more details, please refer to WDT chapter. For details of the WDT module configuration please refer to the “Initialization and Control Sequence” section of the WDT chapter.

27.1.5 Configuration of Clock System and Miscellaneous Functions

The following functions are available and may require configuration in the user code:

- Clock System Configuration
- System Reset Configuration
- Debug Suspend Configuration

Clock System Configuration

MCLK and PCLK frequency can be configured to be different from the user settings during SSW execution as described in ***Chapter 27.1.3.1***. The SCU_CRCLK.IDIV/FDIV bits are used to program the target clock frequency. The ratio between MCLK and PCLK is also selectable via bit SCU_CRCLK.PCLKSEL. In addition, some of the

peripheral clocks can be enable/disable via the SCU_CGATCLR0/SCU_CGATSET0 register respectively. It is also recommended to enable the oscillator watchdog for loss of clock detection.

System Reset Configuration

Several events such as Flash ECC error or SRAM parity error can be used to trigger a system reset using the SCU_RSTCON register. For details, please refer to the reset control unit (RCU) section in the SCU chapter.

Debug Suspend Configuration

The IMC300A device supports a suspend capability for peripherals, if the program execution of the CPU is stopped by the debugger, e.g. with a breakpoint, or with the C_HALT. This allows the debugging of critical states of the whole microcontroller. The suspend function has to be enabled or disabled locally at the peripheral based on the application and the debugging approach. Refer to Debug System chapter for details.

27.2 Start-up Modes

Startup Software (short name SSW) is the first software executed by CPU after any device leaves reset state.

SSW is stored in the ROM memory, but nevertheless its flow is influenced by other “flexible” factors as:

- type of the event triggering SSW execution
- start-up configuration as selected by the user in Boot Mode Index (short notation BMI)

27.2.1 Start-up modes in IMC300A

Start-up mode selection in IMC300A is done by the SSW after reset. For the first start-up, it is based on ***Boot Mode Index (BMI)*** stored in flash configuration sector 0 (CS0). Subsequently, there is also an option to boot via pins by programming BMI.PINDIS with 0. Upon master reset, the value at the boot pins P4.6 (STSTAT.HWCON[0]) and P4.7 (STSTAT.HWCON[1]) is latched in.

Table 303 shows the boot pin encoding and the boot modes.

Table 303 Boot pin modes

HWCON[1]	HWCON[0]	Boot Mode
0	0	User Productive Mode
0	1	ASC BSL
1	0	Alternate Boot Mode
1	1	CAN BSL[73)]

To program a new BMI, user need to call the user function “Request BMI installation” as described in the BSL and User Routines chapter. The selection and handling of BMI by SSW is described in ***Chapter 27.2.3***. The default start-up mode in device delivery state is the ASC BSL mode.

A summary of the supported start-up modes follows.

27.2.1.1 User productive mode

User code is started from Flash memory, no debugging is possible in this mode.

The address of the first user instruction - to where SSW jumps at its end - is taken from Flash location $1000'1004_H$.

73 A programmed value of BMI.BSLTO results in a time-out duration defined by the bit field. If time-out duration is not intended, BMI.BSLTO shall be configured with 0.

SSW does not check either the target address is inside user Flash. Therefore HardFault will be generated if it's outside and the execution will jump to exception handler in SRAM (upon master reset an endless loop is installed by SSW).

27.2.1.2 User mode with debug enabled

User code is started from Flash memory, the first address is determined as in ***User productive mode*** (see ***Chapter 27.2.1.1***).

Debug interface is configured according to ***Boot Mode Index (BMI)*** value and enabled.

27.2.1.3 User mode with debug enabled and Halt After Reset (HAR)

User code is started from Flash memory as in the two modes above.

Debug interface is configured according to BMI value and enabled, the CPU is stalled upon exit from SSW and before the first user instruction (for the handling refer to ***Chapter 27.2.3.2***).

27.2.1.4 Alternate Boot Mode (ABM)

In this mode, user defined bootloader (application) which resides in the user-defined flash address has to be first downloaded via standard bootstrap loader or SWD. This must be followed by a change in the BMI to boot via pins and the selection of ABM boot mode. For new boot mode to take effect, a master reset must be performed.

SSW branches to the user defined bootloader only with a matching magic key, defined in ***Table 304***.

The ABM header is placed at the last 32 bytes of the user flash area, start address at $1000\ 0000_H$ + (FLSIZE.ADDR<<12-20_H).

Table 304 Alternate Boot Mode Header (ABMHD) structure

Offset Address	Size (Byte)	Field Name	Description
00_H	4	MAGICKEY	Magic Key = $A5C3E10F_H$
04_H	4	STADDABM	Start address of the User Code of ABM
08_H	4	CODELENGTH	Length of the User Code of ABM

27.2.1.5 Standard Bootstrap Loader modes

In this mode (short notation Standard BSL):

- user code is downloaded into SRAM
- at the SSW end the execution jumps to SRAM
- no debugging is possible

The Standard BSL mode supported in IMC300A uses USIC0 module for communication with the host:

- ASC - using channel 0 or 1 (auto-detection by firmware) of USIC0 module and ASC (UART) protocol for download

  This is the default start-up mode - selected by BMI value in device delivery state.
- SSC - using USIC0 channel 0 and SSC (SPI) standard protocol for download

  In this mode SPI-compatible serial EEPROM is supposed to be connected as slave device to IMC300A.

The functionality of standard BSL routines is described in the BSL chapter.

27.2.1.6 Bootstrap Loader modes with time-out

These modes are using the Standard BSL routines for downloading, but the functionality is different:

- SSW first checks either an external device is connected/active, meaning SSW waits to receive Start and Header Bytes from the host - either via USIC channel 0 or 1 - for time-out which duration is taken from BMI.BLSTO (refer to ***Chapter 27.2.2***):
  - if yes
    - user code is downloaded into SRAM
    - at the SSW end the execution jumps to SRAM
  - if not
    - at the SSW end the execution jumps to Flash as in ***User productive mode***
- no debugging is possible in this mode, independently either code execution starts from Flash or SRAM

Three BSL modes with time-out are supported in IMC300A, using USIC0 module or CAN for communication with the host. Besides the difference in interface selection, also the check performed as part from the above sequence is different:

- ASC mode
  - SSW configures USIC0 channels 0 and 1 in ASC (UART) mode
  - SSW waits to receive Start and Header Bytes from the host - either via channel 0 or 1 - for time-out which duration is taken from BMI.BLSTO (refer to ***Chapter 27.2.2***)
  - if Start+Header Bytes are received - Standard ASC BSL is further executed for downloading and starting user code from SRAM; otherwise execution from Flash will be taken
- CAN mode
  - SSW configures the clock selection based on BMI.CANCLK as the system clock.
  - SSW configures CAN node 0 in bit timing node.
  - SSW waits to receive the initialisation frame. If the frame is received within the time-out, CAN BSL is further executed for downloading and starting user code from SRAM; otherwise execution from Flash will be taken for BMI.BSLTO > 0. If BMI.BSLTO = 0, endless loop is executed.
- SSC mode
  - SSW configures USIC0 channel 0 as Master in SSC (SPI) mode
  - SSW initiates communication with SPI-compatible serial EEPROM supposed to be connected as slave device
  - if data received upon Read Command sent by SSW corresponds to the expected (serial EEPROM) protocol - Standard SSC BSL is further executed for downloading and starting user code from SRAM; otherwise execution from Flash will be taken

Note: If BSLTO=0 is configured in BMI - SSW at all does not perform any BSL check but directly takes User Productive Mode for ASC BSL with time-out mode.

27.2.2 Boot Mode Index (BMI)

The Boot Mode Index is 2 Byte value stored in Flash (refer to ***Table 305***) and holding information about start-up mode and debug configuration of the device. Additionally to BMI at $1000'0E00_H$ its inverse value is stored at $1000'0E10_H$ for check purposes.

27.2.2.1 Register BMI

BMI Address: $1000'0E00_H$

Boot Mode Index Delivery State: $F8C3_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BSLTO				CAN CLK	DAPDIS		DAP TYP	PIND IS	HWCFG						
r				r	r		r	r	r						

Field	Bits	Type	Description
HWCFG	6:0	r	**Start-up Mode Selection:** 0000000_B CAN Bootstrap Loader mode (CAN_BSL) 0010000_B CAN BSL mode with time-out (CAN_BSLTO) 0100000_B Secure Bootstrap Loader mode over CANopen (SBSL CANopen) 1000000_B ASC Bootstrap Loader mode (ASC_BSL) 1000001_B User productive Mode (UPM) 1000011_B User mode with debug enabled (UMD) 1000111_B User mode with debug enabled and HAR (UMHAR) 1001000_B SSC Bootstrap Loader mode (SSC_BSL) 1010000_B ASC BSL mode with time-out (ASC_BSLTO) 1011000_B SSC BSL mode with time-out (SSC_BSLTO) 1111010_B Secure Bootstrap Loader mode over ASC (SBSL ASC) else Reserved [74]
PINDIS	7	r	**Boot Configuration Type Selection** 0_B Boot from pins is selected 1_B Boot from BMI is selected
DAPTYP	8	r	**DAP Type Selection** 0_B Serial wire debug interface is selected 1_B Single pin debug interface is selected
DAPDIS	10:9	r	**SWD/SPD Input/Output Selection** 00_B SWD/SPD_0 pin is selected 01_B SWD/SPD_1 pin is selected 10_B Reserved 11_B Reserved
CANCLK	11	r	**CAN Clock Source for CAN BSL Mode** 0_B Synchronous CAN clock via internal oscillator (DCO1) with enabled trimming via external reference is selected 1_B Synchronous CAN clock via external oscillator (OSC_HP) is selected
BSLTO	15:12	r	**ASC BSL Time-out value** The time-out duration is BSLTO*2664000 MCLK cycles, the supported time-out range is 0.3-5s (333...4995ms)

74 ATTENTION: Installing a reserved BMI value will cause device delivery state to be restored upon the next reset - refer to ***Chapter 27.2.3***

27.2.3 Start-up mode selection

The start-up modes in IMC300A are selected and handled according to Boot Mode Index (BMI) value read from Flash - refer to ***Chapter 27.2.1***.

The BMI evaluation can lead to:

- taking User mode - SSW will jump at its end into User Flash and start execution from the location which address is stored at $1000'1004_H$ if:
  - a kind of User Mode is selected in BMI
  - ASC BSL with time-out is selected but no valid Start+Header Bytes are received within the selected time frame
- taking Bootstrap Loader mode - executing ASC/SSC or CAN BSL[75] then jumping into SRAM at $2000'0200_H$
- taking Secure Bootstrap Loader (SBSL) mode [75]
- taking Alternate Boot Mode - SSW jumps to User Flash address defined in STADDABM in the Alternate Boot Mode Header
- executing (endless) loop - waiting for valid data to be received via SSC upon SSC BSL mode without time-out, or valid initialization frame via CAN BSL mode without time-out
- erasing the complete user Flash and installing ASC BSL (or SBSL if supported) mode as new BMI value - upon invalid BMI value or if Secure BSL or CAN BSL is selected but not supported for the device. Afterwards master reset is triggered and device is started in a mode according to the new BMI.

27.2.3.1 BMI handling by SSW

This SSW part is intended to be executed after the user function (in ROM) “Request BMI installation” (described in the BSL and User Routines chapter) has been called and has triggered a system reset. Therefore the conditions under which this handling is performed are:

- the last reset was a system reset requested by CPU
- the two half words of SSW0 register are inverse to each other

If all the above conditions are true, the SSW evaluates BMI.PINDIS to determine if boot via pins is the chosen boot option. STSTAT.HWCON determines the actual boot mode via pins. For non pin-booting, SSW considers SSW0[15:0] content as new BMI value to be installed and executes the following:

- check either the current BMI (in CS0) is User_Productive AND the new value is NOT User_Productive:
  - if yes - erase the complete user Flash and install ASC_BSL (or SBSL if supported) mode as new BMI value
  - if not - install the new BMI value from SSW0[15:0]
- instal all zero in SSW0 to indicate no BMI-programming upon the next reset
- request master reset to be triggered

Upon the last action, a master reset is triggered and a next SSW execution will start with the new BMI value installed in CS0.

27.2.3.2 Debug system handling

If debug system must be enabled - start-up mode with debug support is selected in Boot Mode Index (refer to ***Chapter 27.2.2***) - SSW performs the following:

- configure the debug interface from BMI value

75 If available in device and selected in BMI.

- enable the debug interface
- if start-up mode with Halt After Reset request (UMHAR) is selected in BMI upon master reset - enter an endless NOP (no operation) loop. From this point on, an external tool (debugger) can take over the control of the device, in particular:
  - if/when a debugger connects to device, it can halt the CPU and check BMI and/or the core program counter (PC) register
  - if HAR is selected, this can be identified by BMI value (refer to ***Chapter 27.2.2***) and the PC value will point inside the ROM. The debugger can then manipulate PC and start the user code as desired - the default start address (taken without HAR) is according to the content at location $1000'1004_H$ in user Flash (refer to ***Table 305***)

27.3 Data in Flash for SSW and User SW

Table 305 shows the data in Flash which is relevant for SSW execution and can be used by user software in IMC300A.

Table 305 Flash data for SSW and user SW in IMC300A

Address	Length	Function	Target location
Start-up mode selection			
$1000'0E00_H$	2 B	Boot Mode Index (BMI)	---
$1000'0E10_H$	2 B	Inverse BMI	---
Chip Identification			
$1000'0F00_H$	4 B	Chip ID	SCU_IDCHIP
$1000'0F04_H$	28 B	Chip Variant Identification Number	---
$1000'0FF0_H$	16 B	Unique Chip ID	---
Temperature-sensor and DCO related data			
$1000'0F20_H$	16 B	Temperature-sensor constant data 1	---
$1000'0F30_H$	1 B	ANA_TSE_T1	---
$1000'0F31_H$	1 B	ANA_TSE_T2	---
$1000'0F32_H$	1 B	DCO_ADJLO_T1	---
$1000'0F33_H$	1 B	DCO_ADJLO_T2	---
$1000'0F34_H$	161 B	Temperature-sensor constant data 2	---
Application software related data			
$1000'1000_H$	4 B	Initial Stack Pointer value after SSW	SP_main
$1000'1004_H$	4 B	Start address after SSW in User modes	PC
Clock system related data			
$1000'1010_H$	4 B	Clock configuration value CLK_VAL1	If bit[31]=0: Installation of • bits[21:10] into SCU_CLKCR[19:8] • bits[9:8] into SCU_CLKCR1[1:0] • bits[7:0] into SCU_CLKCR[7:0]

Table 305 Flash data for SSW and user SW in IMC300A (continued)

Address	Length	Function	Target location
$1000'1014_H$	4 B	Clock gating configuration value CLK_VAL2	If bit[31]=0: Installation of • bits[21:16] into SCU_CGATCLR0[21:16] • bits[10:0] into SCU_CGATCLR0[10:0]
$1000'1018_H$	4 B	Wait time before ASC BSL channel selection configuration value WAIT_ASCBSL_ENTRY	If bit[31]=0: Installation of • bits[30:0] for wait time before ASC BSL channel selection

28 Bootstrap Loaders (BSL) and User Routines

This chapter describes the Bootstrap Loaders (BSL) and the user-accessible routines in the ROM memory.

The ASC (UART) BSL (***Chapter 28.1***) and the SSC BSL (***Chapter 28.2***) is entered with the BMI settings as described in the Boot and Startup Chapter. The main purpose of BSL Mode is to allow easy and quick programming/erasing of the Flash.

Chapter 28.4 describes user-accessible routines that can be called by application software. These routines are located in the ROM memory.

28.1 ASC (UART) Bootstrap Loader

ASC (UART) Standard Bootstrap Loader (ASC BSL) in IMC300A uses USIC0 module to download code/data into SRAM starting at address 2000 0200_H.

After the last code/data Byte is received and stored, the Startup Software starts user code from address 2000 0200_H.

28.1.1 Pin usage

ASC BSL in IMC300A is selected by a single BMI value but it allows to download user code/data via several variants of pins, modes and USIC0 channels:

- Channel 0
  - full duplex mode with RxD at P0.14 and TxD at P0.15
  - half duplex mode with RxD/TxD at P0.14
- Channel 1
  - full duplex mode with RxD at P1.3 and TxD at P1.2
  - half duplex mode with RxD/TxD at P1.3

Note: The above set of pins also accommodate all the assignments for SWD/SPD (debug) interfaces.

28.1.2 ASC BSL execution flow

The complete ASC Bootstrap Loader procedure consists of two parts as described below.

28.1.2.1 ASC BSL entry check sequence

IMC300A SSW is able to provide wait time before ASC BSL channel selection. The wait time handling is user-configurable by installing the value in a one word location in Flash (refer to ***Table 305***).

- if WAIT_ASCBSL_ENTRY[31]=0 - SSW executes wait loops before ASC BSL channel selection

Downloading is only initiated after a Start (zero) and a Header (described below) Bytes are received through one of the channels whereas both the channels are active (“listening”) until the selection is done by the routine itself as follows:

- Channel selection - based on the fact at which RxD pin (see the above assignments) first Start+Header Bytes are received
- Full/half duplex selection - based on the Header Byte received

*Note: For definitions of header/acknowledge byte values exchanged with the host - refer to **Chapter 28.1.3**.*

The ASC bootloader functionality includes:

1. enable and configure the both USIC0 communication channels 0 and 1 as follows:
   a. ASC mode, 8 data bits, 1 stop bit, no parity
2. configure ASC clock-generation circuitry for measurement
3. perform continuously the following sequence for both USIC0 channels one after another
   a. check either Start zero Byte has been received

      if yes - then:
   b. reconfigure ASC clock-generating circuitry for normal operation according to the baudrate measured from the Start Byte, then:
   c. check either Header Byte has been received

      if yes - then:
   d. check the Header Byte received
      - if equal to BSL_ASC_F or BSL_ENC_F - full duplex mode is selected - continue with step 4.
      - if equal to BSL_ASC_H or BSL_ENC_H - half duplex mode is selected - continue with step 4.
      - otherwise - go to sequence for the other channel
4. select the current (Cy) channel for further handling; restore default configuration for the channel C(y-1) which is not selected
5. for the selected channel and mode (full/half duplex) :
   a. configure TxD pin and ASC transmitter
   b. adapt (in case) RxD pin settings
   c. enable transmission, single shot mode
6. check which Header byte was received:
   a. BSL_ASC_F or BSL_ASC_H - standard BSL entry sequence was executed, the communication will use further the baudrate detected - continue with ***ASC BSL download sequence*** (see ***Chapter 28.1.2.2***)
   b. BSL_ENC_F or BSL_ENC_H - the communication during ***ASC BSL download sequence*** will potentially use different (e.g. higher) baudrate than the initially detected - continue with the ***Enhanced ASC BSL entry sequence*** (see below))

The above check sequence is executed

- in ASC BSL mode without time-out - until valid Start+Header Bytes are received
- otherwise - only for some time according to BMI.BSLTO

Note: If mode with time-out is selected but BMI.BSLTO=0 - User mode with start from Flash is directly taken.

28.1.2.1.1 Enhanced ASC BSL entry sequence

This is an extension of the standard ***ASC BSL entry check sequence*** and will be used when higher baudrates are required for the communication channel.

It includes the following steps:

1. Send BSL_ENC_ID to acknowledge the establishment of the initial baud rate and entry into enhanced ASC BSL
2. Send current PDIV divider from USIC0_CHy_BRG register - the 10-bit value is sent in 2 bytes (most significant byte first)
3. Receive from host the 10-bit value to be written into the STEP bit field in USIC0_CHy_FDR register
4. Send BSL_BR_OK to acknowledge the establishment of the new baud rate

5. Configure USIC baud rate generator accordingly
6. Receive from host BSL_BR_OK to indicate that the communication channel has been successfully established
   - If no or wrong acknowledge value is received, a device software reset will be triggered

Figure 286 shows the outline of the sequence to configure the baud rate.

Requirements for Host

For the host to support enhanced ASC BSL, the host additionally has to:

- Receive from IMC300A device, the current 10-bit PDIV value in USIC0_CHy_BRG register
- Calculate the MCLK that the device is running on based on the received PDIV through the formula:

$$\text{MCLK} = \text{Initial Baud Rate} \times (\text{PDIV} + 1) \times 8$$

Equation 53

- Select a new baud rate that is supported by the enhanced ASC BSL given the MCLK (see ***Table 306***)
- Calculate the scaling factor, i.e. ratio of the new baud rate to the initial baud rate. Some examples are given in ***Table 307***. The scaling factor is rounded to the nearest integer in order to meet a frequency deviation of +/- 3%.

Table 306 Supported Baud Rates

MCLK (MHz)	Standard baud rates supported with ASC BSL (kHz)		Max. baud rate supported with Enhanced ASC BSL (MHz)
	Min.	Max.	
8	1.2	28.8	0.999
16	2.4	57.6	1.998
32	4.8	115.2	3.996
48	9.6	153.6	5.994

Table 307 Scaling Factor Examples

Initial standard baud rates (kHz) A	Targeted higher baud rates (kHz) B	Scaling factor rounded to the nearest integer (B/A)
9.6	1500	156
19.2	1500	78
57.6	1500	26
115.2	1500	13

- Calculate the 10-bit value to be written into the STEP bit field of USIC0_CHy_FDR register through the formula:

$$\text{STEP (in fractional divider mode)} = \frac{1024 \times \text{Scaling Factor}}{\text{PDIV} + 1}$$

Equation 54

- Send the 10-bit STEP value to the device
- Wait until the BSL_BR_OK is received from the device
- Echo the BSL_BR_OK back to the device

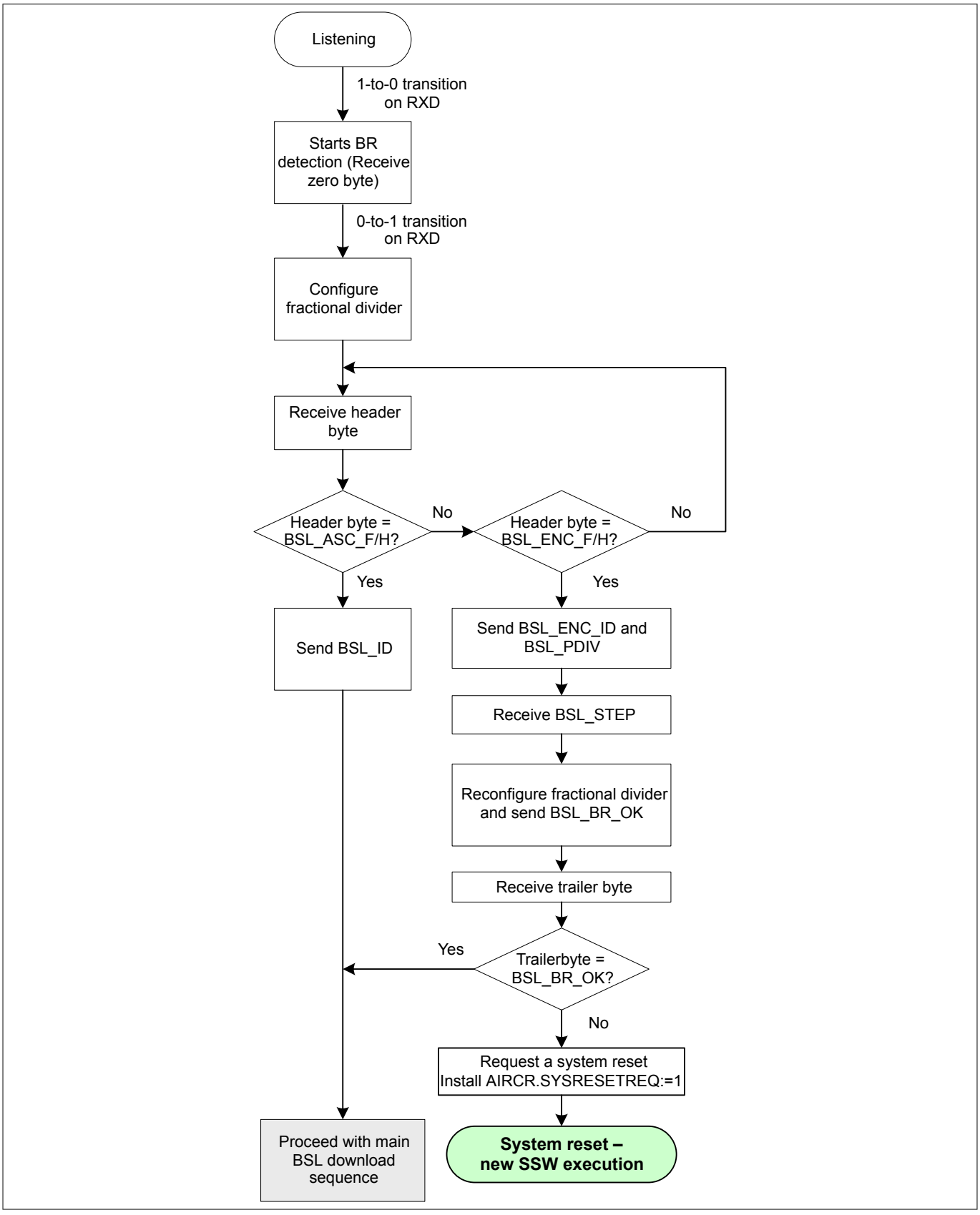


Figure 286 Baud Rate configuration sequence during IMC300A ASC BSL entry

28.1.2.2 ASC BSL download sequence

After the baud rate has been detected/configured and channel/mode (full/half duplex) selected, ASC BSL awaits 4 bytes describing the length of the application from the host (refer to ***Figure 287***). The least significant byte is received first.

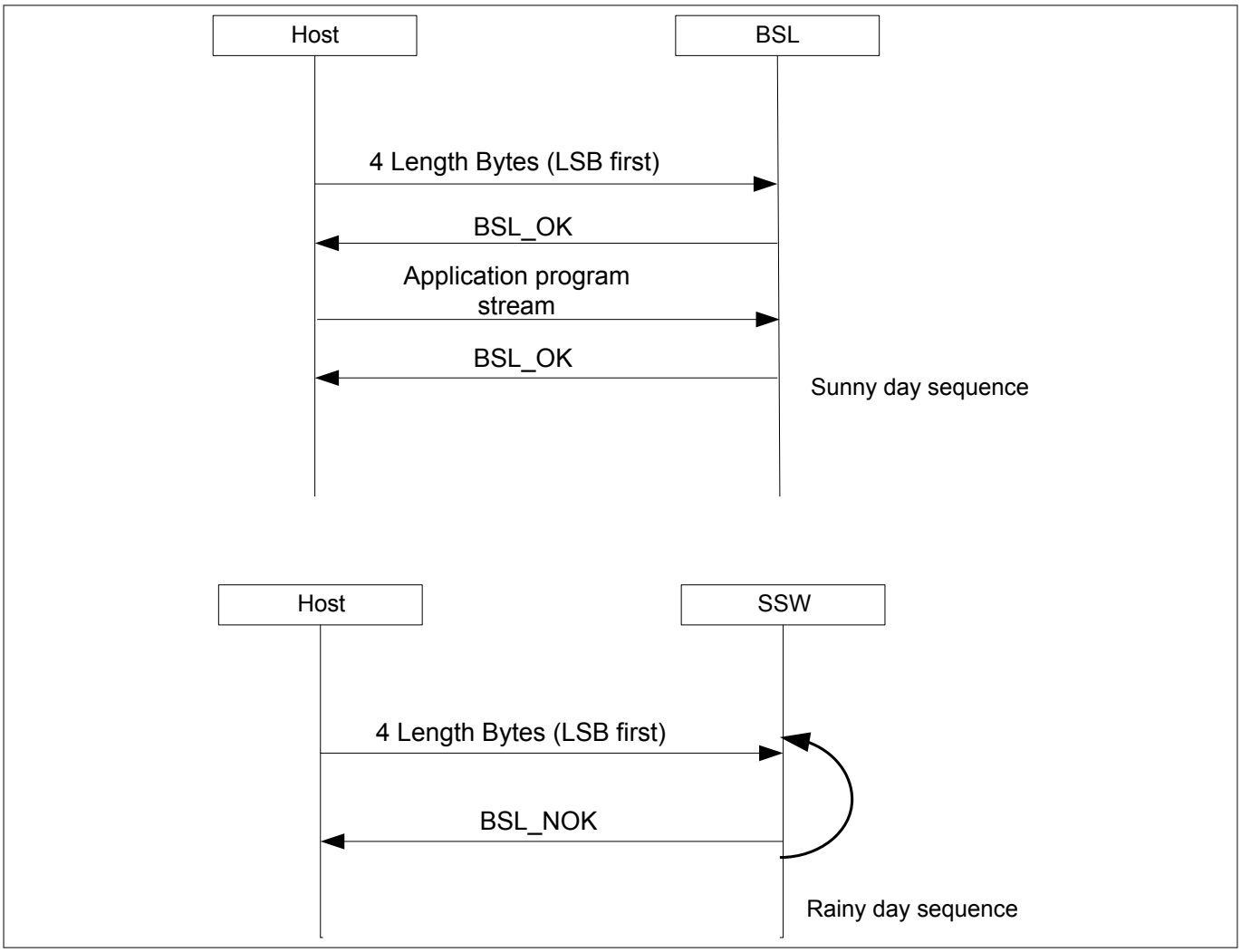


Figure 287 IMC300A Standard ASC BSL: Application download protocol

If application length is found alright by SSW, a BSL_OK byte is sent to the host following which the latter sends the byte stream belonging to the application. After the byte stream has been received, SSW terminates the protocol by sending a final OK byte and then cedes control to the downloaded application.

If application length is found to be in error (application length greater than device SRAM size), a BSL_NOK byte is transmitted back to the host and the SSW resumes awaiting the length bytes.

28.1.3 ASC BSL protocol data definitions

The interaction between IMC300A ASC Bootstrap Loader routine and the host implements handshake protocol based on ***Figure 288*** and request/acknowledge/data Bytes defined in ***Table 308***.

Table 308 Handshake protocol data definitions in IMC300A ASC BSL

Name	Length, Byte	Value	Description
Requests/data/acknowledge sent by the Host			
BSL_ASC_F	1	$6C_H$	Header requesting full duplex ASC mode with the current baud rate
BSL_ASC_H	1	12_H	Header requesting half duplex ASC mode with the current baud rate
BSL_ENC_F	1	93_H	Header requesting full duplex ASC mode with a request to switch the baud rate
BSL_ENC_H	1	ED_H	Header requesting half duplex ASC mode with a request to switch the baud rate
BSL_STEP	2	$0XXX_H$	10-bit value (LSB aligned) to be programmed into selected USIC channel's FDR.STEP bit field. Most significant 6 bits should contain all 0.
BSL_BR_OK	1	$F0_H$	Final baud rate is established in enhanced ASC BSL
Acknowledges sent by IMC300A firmware			
BSL_ID	1	$5D_H$	Start and header bytes are received, baud rate is established
BSL_ENC_ID	1	$A2_H$	Start and header byte(s) are received in enhanced ASC BSL, initial baud rate is established
BSL_PDIV	2	$0XXX_H$	10-bit value (LSB aligned) containing the selected USIC channel's BRG.PDIV bit field value. Most significant 6 bits should contain all 0.
BSL_BR_OK	1	$F0_H$	Final baud rate is established in enhanced ASC BSL.
BSL_OK	1	01_H	Data received is OK
BSL_NOK	1	02_H	Failure encountered during data reception

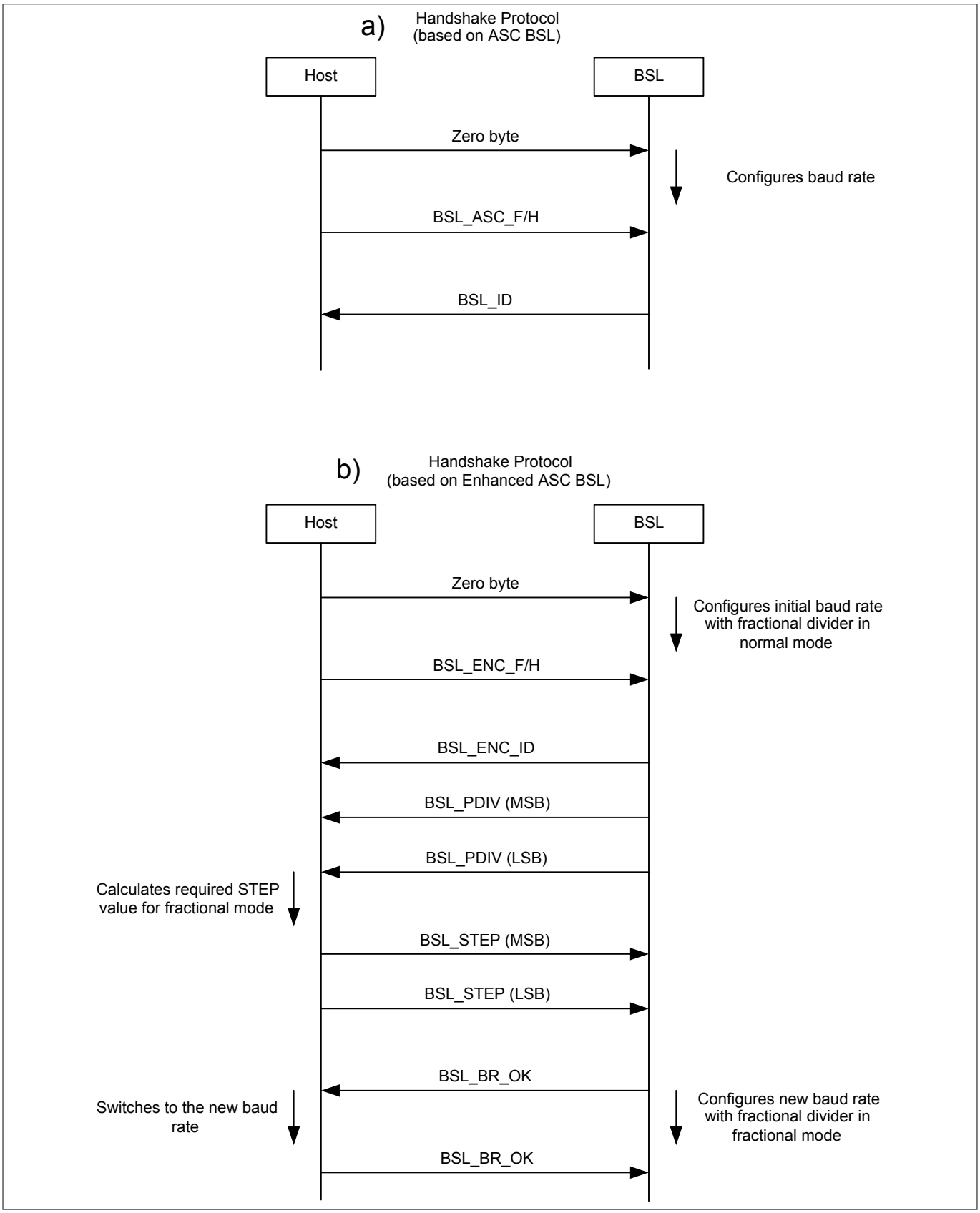


Figure 288 Handshake protocol for IMC300A ASC BSL entry

28.2 SSC Bootstrap loader

This procedure downloads code from a SPI-compatible serial EEPROM into SRAM starting at address 2000 0200$_H$ up to the user-available SRAM size, using Channel 0 of USIC0 Module.

IMC300A is the master SPI-device, following pins are used by the bootloader:

- MRST (master data input) and MTSR (master data output) - on the same P0.15, half-duplex mode used, open drain
- SCLK (clock signal) - P0.14, open drain
- SLS (chip-select $\overline{CS}$ to the EEPROM) - P0.13, open drain

Note: Due to IMC300A pin configured as open drain, external pull-up resistors are required to be added on to the bus for each of the above pins.

Note: The EEPROM pins SI (Serial Data Input) and SO (Serial Data Output) have to be connected to each other before connecting to the target device.

Note: The EEPROM pins $\overline{WP}$ and $\overline{HOLD}$ are not used by the SSC bootloader. An external circuitry is required. (e.g. pull-up from V_{DD})

A SPI-compatible serial EEPROM of type 25xxx must be connected to the pins as above defined. The clock signal is configured at MCLK/10 frequency upon device startup.

The SSC bootloader in IMC300A is able to communicate with a very broad range on serial-EEPROM types: from such using 8-bit addressing (size up to 2K bit, quite outdated already) up to devices using 24-bit addressing (1M bit and above). The connected EEPROM type is determined by examining the received header bytes, as indicated in ***Table 309***.

Note: Besides the bootloader supports all the device-types, the code/data length which can be downloaded is limited by the size of available SRAM.

Table 309 SSC BL: Determining the EEPROM Type and data-flow

SSC Frame		EEPROM with 8-bit addressing connected		EEPROM with 16-bit addressing connected		EEPROM with 24-bit addressing connected	
N	**data**	**IMC300A-send**	**IMC300A-receive**	**IMC300A-send**	**IMC300A-receive**	**IMC300A-send**	**IMC300A-receive**
1	03_H	Read command	XX_H default level	Read command	XX_H default level	Read command	XX_H default level
2	00_H	Address	XX_H	Address_H	XX_H	Address_H	XX_H
3	00_H/ FF_H[7] [6]	dummy	Identification	Address_L	XX_H	Address_M	XX_H
4	00_H/ FF_H[7] [6]	dummy	Size	dummy	Identification	Address_L	XX_H
5	FF_H	dummy	Data Byte 1	dummy	Size, High B	dummy	Identification

[76] Depending on which EEPROM type is checked.

Table 309 SSC BL: Determining the EEPROM Type and data-flow (continued)

SSC Frame		EEPROM with 8-bit addressing connected		EEPROM with 16-bit addressing connected		EEPROM with 24-bit addressing connected	
N	**data**	**IMC300A-send**	**IMC300A-receive**	**IMC300A-send**	**IMC300A-receive**	**IMC300A-send**	**IMC300A-receive**
6	FF_H	dummy	Data Byte 2	dummy	Size, Low B	dummy	Size, High B
7	FF_H	dummy	Data Byte 3	dummy	Data Byte 1	dummy	Size, Mid B
8	FF_H	dummy	Data Byte 4	dummy	Data Byte 2	dummy	Size, Low B
9 ...	FF_H	dummy	Data Byte 5 ...n	dummy	Data Byte 3 ...n	dummy	Data Byte 1 ...n

The EEPROM connected for downloading must contain:

- Identification Byte $5D_H$ at the first address (0000_H)
- The length of the code (Code_Length) in Bytes as follows:
  - in case of an EEPROM with 8-bit addressing - in one Byte at address 0001_H
  - in case of an EEPROM with 16-bit addressing - in two Bytes at addresses 0001_H / 0002_H ordered high/low
  - in case of an EEPROM with 24-bit addressing - in three Bytes at addresses 0001_H / 0002_H / 0003_H ordered high/middle/low
- The code of defined length follows sequentially

The SSC bootloader functionality includes:

1. Enable the communication channel by setting USIC0_C0_KSCFG.MODEN:=1
2. Assure clock gating for USIC0 module is de-asserted
3. Configure the USIC0_C0 channel as follows:
   - **a.** SSC mode, 8 data bits, MSB first
   - **b.** SCLK frequency = MCLK/10
   - **c.** no SLS activated (only one serial EEPROM is supported)
   - **d.** pin-configuration as defined above
   - **e.** enable transmission
4. Deselect EEPROM by setting $\overline{CS}$=1
5. Receive data from 8-bit EEPROM
   - **a.** enable EEPROM ($\overline{CS}$=0)
   - **b.** send Read command (03_H)
   - **c.** send address byte (00_H) for data to be received
   - **d.** send read response byte (FF_H)
6. Check the response based on the last received byte:
   - **a.** if equal to the Identification Byte ($5D_H$) - the EEPROM uses 8-bit addressing:
     - SSW reads one more byte and saves it as Code_Length - 1B only effective
     - continue with p.11
   - **b.** if not equal to the Identification Byte ($5D_H$) - the EEPROM does not use 8-bit addressing:
     - deselect EEPROM by setting $\overline{CS}$=1
7. Receive data from 16-bit EEPROM
   - **a.** enable EEPROM ($\overline{CS}$=0)
   - **b.** send Read command (03_H)

c. send 2 address bytes (00_H, 00_H) for data to be received
d. send read response byte (FF_H)

8. Check the response based on the last received byte:
a. if equal to the Identification Byte ($5D_H$) - the EEPROM uses 16-bit addressing:
- SSW reads two Bytes in order High/Low to determine Code_length (2 Bytes)
- continue with p.11

b. if not equal to the Identification Byte ($5D_H$) - the EEPROM does not use 16-bit addressing:
- deselect EEPROM by setting $\overline{CS}$ =1

9. Receive data from 24-bit EEPROM
a. enable EEPROM ($\overline{CS}$=0)
b. send Read command (03_H)
c. send 3 address bytes (00_H, 00_H, 00_H) for data to be received
d. send read response byte (FF_H)

10. Check the response based on the last received byte:
a. if equal to the Identification Byte ($5D_H$) - the EEPROM uses 24-bit addressing:
- SSW reads three more Bytes in order High/Middle/Low to determine Code_length (3 Bytes)
- continue with p.11

b. if not - exit the sequence

11. Check the value of Code_length:
a. if greater than allowed available SRAM in IMC300A, exit the sequence
b. otherwise, continue with p.12

12. Send one FF_H byte for each byte of user code. Read user code bytes [Code_Length] and store them sequentially from the beginning of SRAM (address 2000 0200_H) onwards, disable EEPROM ($\overline{CS}$=1).

13. Disable the communication channel by resetting USIC0_C0_KSCFG.MODEN:=0

14. Set SSW flag BSL_act=1 and exit the sequence

The Startup Software starts the downloaded code from address 2000 0200_H.

28.3 CAN BSL mode

The CAN bootstrap loader mode transfers user application via Node-0 or Node-1 of the CAN module into SRAM.

Users need to adhere to the three phases of the protocol for user application to be downloaded. The size of the user-available SRAM determines the maximum size of the downloadable application code.

Figure 289 shows the CAN BSL mode procedures.

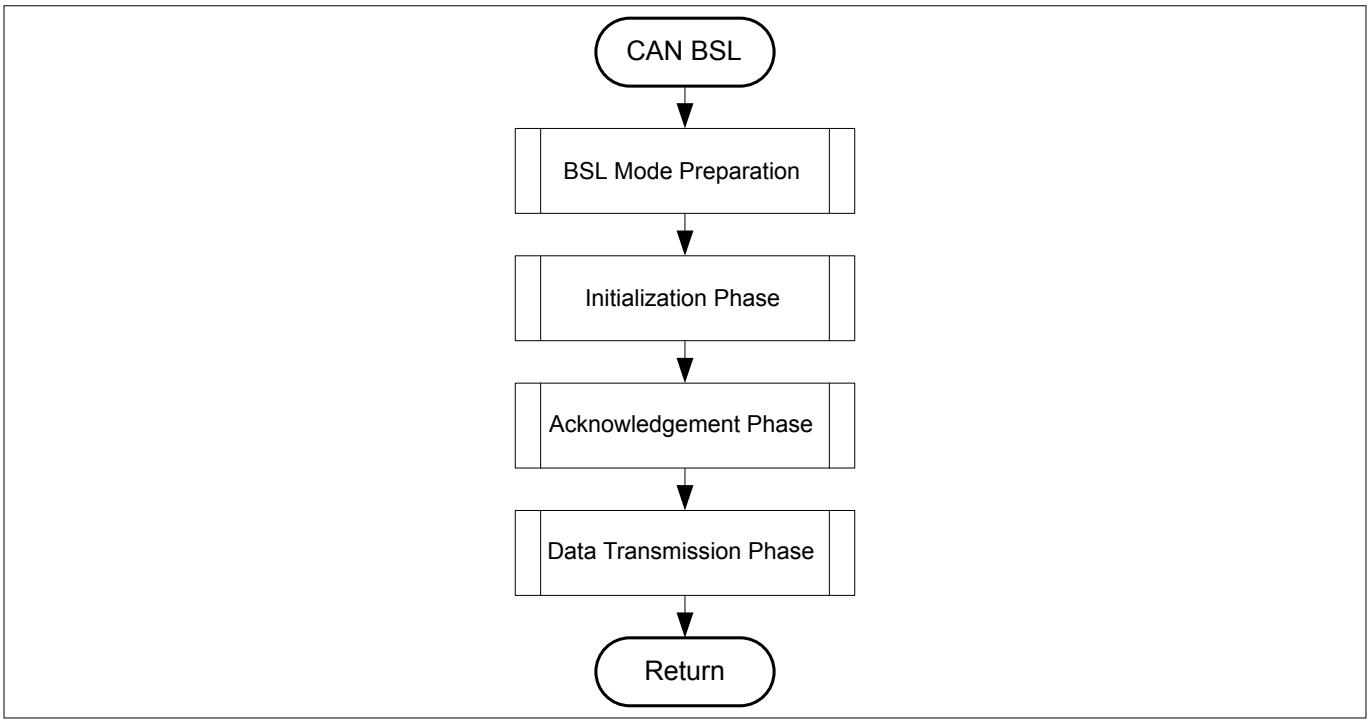


Figure 289 CAN BSL Sequence

28.3.1 Initialization Phase

SSW switches to the synchronous CAN clock source via internal oscillator or external oscillator, selected by BMI.CANCLK. If the internal oscillator is selected, f_{MCLK} is configured for 24MHz. For external oscillator selection, a stable external clock (OSC_HP) is mandatory. For transfer rates of 1 Mbps, the user has to ensure that the external clock is at least 10 MHz. The SSW determines the external clock frequency and configures f_{MCLK} to have the same frequency as f_{OSC_HP}. Independent of the CAN clock source selection, the CAN baud logic clock is configured as f_{MCLK} in MCR.CLKSEL.

In this phase, the CAN baud rate of the host is determined. A standard CAN initialization frame comprising eight data bytes is transmitted continuously by the external host. The LSB-aligned 11 bits message ID (0x555) of the frame is used for baud rate detection. Data bytes 2 and 3 contain the acknowledge identifier (ACKID). The SSW will send the ACKID back to the host in the acknowledge frame to indicate the completion of the initialization phase. The next 2 bytes (byte 4 and 5) contains the message count value, DMSGC. DMSGC indicates the number of eight byte data frames of user application which must be received by SSW and placed into the SRAM. The total size of the data frames should be selected to be smaller or equal than the available SRAM size. The last 2 bytes (byte 6 and 7) is the DMSGID identifier that is to be used in the Data frame to transmit the user application.

Simplified representation of initialization frame with 11 bit ID of 0x555

0	1	2	3	4	5	6	7
0x555	BTR-L	BTR-H	ACK IDL	ACK IDH	DMSGC-L	DMSGC-H	DMSGID-L	DMSGID-H

Figure 290 Data field of the Initialization Frame

Port pins used are P0.14 / P0.15 or P1.2 / P1.3. If SSW detects initialization frame on P0.14, it would configure P0.15 for TX functionality on Node 0. In contrary, if SSW detects initialization frame on P1.3, SSW configures P1.2 for TX functionality instead for Node 1.

28.3.2 Acknowledgement Phase

An acknowledgement frame is sent to the host indicating completion of initialization phase.

After SSW computes the baud rate of the host and reconfigures the NBTR register of node-0, it waits until the initialization frame is correctly and fully received. SSW signals its intent to use the bus by transmitting a dominant (0) bit in its ACK slot.

After the dominant bit has been transmitted, an acknowledgement frame using the ACK-ID extracted from the initialization frame is sent to the host. This ACK-ID is used as the LSB-aligned 11-bit message ID and for data bytes 2 and 3. The configured NBTR register value is captured through data bytes 0 and 1. If the size of application intended to be downloaded is greater than the size of SRAM on the device, a negative acknowledgement as depicted below is sent, where data bytes 4-7 contains the error code of 0xDEADBEEF. SSW enters acknowledgement phase again. If the size of the application is smaller or equal to the PSRAM size, then data byte 4 to 7 of the frame is a direct copy of the equivalent data bytes of the initialization frame. ***Figure 291*** depicts data part of acknowledgement frame.

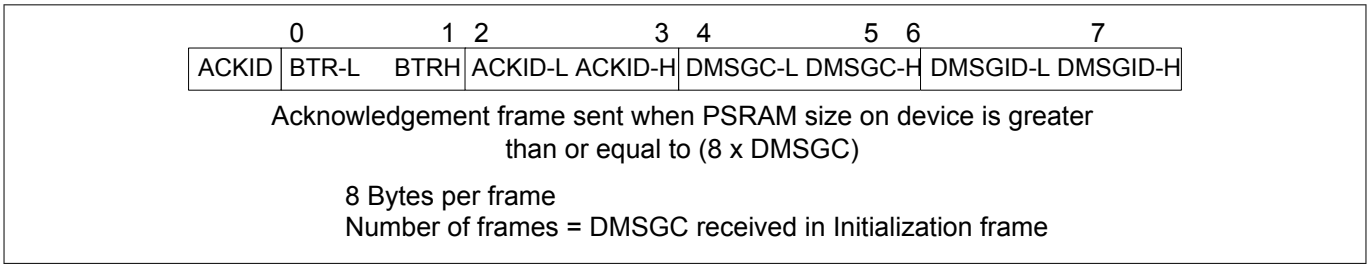


Figure 291 CAN Acknowledgement frame

28.3.3 Data Transmission Phase

Host transmits user application in several CAN frames to the device.

After the SSW transmits the acknowledgement frame, it prepares to receive user application. Each CAN frame carries eight data bytes and the number of CAN frames is limited to the value retrieved from the DMSGC (Data Message Count) field of the initialization frame. Message identifier is essentially the DMSGID extracted from the initialization frame.

The first data byte received is stored in the SRAM address 2000 0200_H. Subsequent data bytes are stored at incrementing address. After all the frames has been received, SSW continues its startup activities.

28.4 Firmware routines available for the user

Several user routines (refer to ***Table 310***) are available inside ROM so they can be called by application software.

Table 310 User routines' in IMC300A ROM

IMC300A ROM		Description
Address	**Content**	
$0000\ 0100_H$	_NvmErase	Pointer to ***Erase Flash Page*** routine
$0000\ 0104_H$	_NvmProgVerify	Pointer to ***Erase, Program & Verify Flash Page*** routine
$0000\ 0108_H$	_BmiInstallationReq	Pointer to ***Request BMI installation*** routine
$0000\ 0110_H$	_NvmEraseSector	Pointer to ***Erase Flash Sector*** routine
$0000\ 0114_H$	_NvmProgVerifyBlock	Pointer to ***Program & Verify Flash Block*** routine
$0000\ 0124_H$	_DCOCalc	Pointer to ***DCO Calibration*** routine

NVM-related functions (see ***Chapter 28.4.1*** and ***Chapter 28.4.2***) return status indication as shown in ***Table 311***.

Table 311 Status indicators returned by NVM routines in IMC300A ROM

Status Indicator		Description
Symbolic name	**Value**	
NVM_PASS	$0001\ 0000_H$	Function succeeded
NVM_E_FAIL	$8001\ 0001_H$	Generic error
NVM_E_SRC_AREA_EXCEEDED	$8001\ 0003_H$	Source data is not in RAM
NVM_E_SRC_ALIGNMENT	$8001\ 0004_H$	Source data is not 4 Byte aligned
NVM_E_NVM_FAIL	$8001\ 0005_H$	NVM module can not be physically accessed
NVM_E_VERIFY	$8001\ 0006_H$	Verification of the written page not successful
NVM_E_DST_AREA_EXCEEDED	$8001\ 0009_H$	Destination data is not (completely) located in NVM
NVM_E_DST_ALIGNMENT	$8001\ 0010_H$	Destination data is not properly aligned

The description below provides an overview of the features.

28.4.1 Erase Flash Page

IMC300A Flash can be erased with granularity of one page = 16 blocks of 16 Bytes = 256 Bytes using this routine.

- Input parameter
  - logical address of the Flash Page to be erased, must be page aligned and in NVM address range (pageAddr)
- Return status (refer to ***Table 311***)
  - OK (NVM_PASS)
  - invalid address (NVM_E_DST_AREA_EXCEEDED, NVM_E_DST_ALIGNMENT)
  - operation failed (NVM_E_FAIL, NVM_E_NVM_FAIL, NVM_E_VERIFY)
- Prototype

  NVM_STATUS NvmErasePage (unsigned long pageAddr)

28.4.2 Erase, Program & Verify Flash Page

This function performs erase (skipped if not necessary), program and verify of selected Flash page.

- Input parameters
  - logical address of the target Flash Page (dstAddr)
  - address in SRAM where the data starts (srcAddr)
- Return status (refer to ***Table 311***)
  - OK (NVM_PASS)
  - invalid addresses (NVM_E_SRC_AREA_EXCEEDED, NVM_E_SRC_ ALIGNMENT, NVM_E_DST_AREA_EXCEEDED, NVM_E_DST_ALIGNMENT)
  - operation failed (NVM_E_FAIL, NVM_E_NVM_FAIL, NVM_E_VERIFY)
- Prototype

  NVM_STATUS NvmProgVerify (unsigned long srcAddr, unsigned long dstAddr)

28.4.3 Request BMI installation

This procedure initiates installation of a new BMI value. In particular, it can be used as well as to restore the state upon delivery for a device already in User Productive mode.

- Input parameter
  - BMI value to be installed (requestedBmiValue)
- Return status - only upon error, if OK the procedure triggers a reset respectively does not return to calling routine
  - wrong input BMI value (0001_H)
- Prototype

  unsigned long BmiInstallationReq (unsigned short requestedBmiValue)

28.4.4 DCO Calibration

This procedure calibrates the DCO, based on the measured chip temperature using the IMC300A built-in sensor and data from Flash (refer to ***Table 312***). An offset value is calculated and used to start the DCO calibration.

- Input parameter
  - none
- Return status
  - OK
  - operation failed
- Prototype

  unsigned long CalibrateDCO (void)

28.4.5 Erase Flash Sector

IMC300A Flash can be erased with granularity of one sector = 16 pages of (16 blocks of 16 Bytes) = 4K Bytes using this routine.

- Input parameter
  - logical address of the Flash Sector to be erased, must be in NVM address range (sectorAddr)
- Return status (refer to ***Table 311***)
  - OK (NVM_PASS)
  - invalid address (NVM_E_DST_AREA_EXCEEDED, NVM_E_DST_ALIGNMENT)
  - operation failed (NVM_E_FAIL, NVM_E_NVM_FAIL, NVM_E_VERIFY)
- Prototype

  NVM_STATUS NvmEraseSector (unsigned long sectorAddr)

28.4.6 Program & Verify Flash Block

IMC300A Flash can be programmed and verified with granularity of one block (4 words of 4 Bytes) = 16 Bytes using this routine.

- Input parameter
  - logical address of the target Flash Block (dstAddr)
  - address in SRAM where the data starts (srcAddr)
- Return status (refer to ***Table 311***)
  - OK (NVM_PASS)

  - invalid addresses (NVM_E_SRC_AREA_EXCEEDED, NVM_E_SRC_ ALIGNMENT, NVM_E_DST_AREA_EXCEEDED, NVM_E_DST_ALIGNMENT)
  - operation failed (NVM_E_FAIL, NVM_E_NVM_FAIL, NVM_E_VERIFY)
- Prototype

  NVM_STATUS NvmProgVerifyBlock (unsigned long srcAddr, unsigned long dstAddr)

28.5 Data in Flash used by the User Routines

Table 312 shows the data in Flash which is used by the user routines in IMC300A.

Table 312 Basic Flash data for SSW and user SW in IMC300A

Address	Length	Function	Target location
Start-up mode selection			
$1000'0E00_H$	2 B	Boot Mode Index (BMI)	---
$1000'0E10_H$	2 B	Inverse BMI	---
Temperature-sensor related data			
$1000'0F20_H$	16 B	Temperature-sensor constant data 1	---
$1000'0F30_H$	1 B	ANA_TSE_T1	---
$1000'0F31_H$	1 B	ANA_TSE_T2	---
$1000'0F34_H$	161 B	Temperature-sensor constant data 2	---

29 Debug System (DBG)

The debug system is an extension to the regular processor architecture. The IMC300A Series Microcontrollers provide a complete hardware debug solution, with hardware breakpoint and watchpoint options. This allows high system visibility of the processor, memory and available peripherals. The debug functions are implemented with a standard ARM Cortex M0 configuration. Debug functions are integrated into the ARM Cortex-M0 processor architecture. The debug system supports serial wire debug and single pin debug interfacing.

29.1 Overview

The basic debug functionality of the Cortex-M0 debug system is limited to invasive debug and includes processor halt, single step, processor core register access, Reset and HardFault Vector Catch. Besides the hardware debug components unlimited software breakpoints are available. The Debugger can connect to the debug system via the Serial Wire Debug (SWD) or Single Pin Debug (SPD) interface port and uses CoreSight infrastructure and the regular access flow. This permits debugger to identify the processor and its debug capabilities. The debug system allows a full system memory access and access to zero-wait state system slaves via the internal debug access port (DAP) connected to the system bus matrix. This access is non-intrusive and a debugger can access the devices, including memory when the processor is halted or running. Core register full access is available, if the processor is halted. The System Control Space (SCS) provides debug through registers available. The Data Watchpoint Unit (DWT) provides two watchpoint register sets, each implement data address and PC based watchpoint functionality including comparator address masking. The processor BreakPoint Unit (BPU) provides four PC based breakpoint register. The system is accessible by the tool through DAP. DAP permits access to debug resources when the processor is running, halted, or held in reset. A processor enters Debug state if it is configured to halt on a debug event, and a debug event occurs. The supported debug infrastructure can be identified by checking the ROM table.

29.1.1 Features

The accurate Debug and Trace System provides the following functionality:

- Serial Wire Debug Port (SWD) provides Serial Wire Debug, which allows to debug via 2 pins.
- Single Pin Debug (SPD) provides a debug capability via 1 pin.
- Processor halt, single-step, processor core register access
- Reset and HardFault Vector Catch.
- Software breakpoints
- Full system memory access
- 4 Hardware breakpoints supported
- 2 watchpoints supported

*Note: Please refer to **[2]** for more detailed informations on the debug functionality.*

29.1.2 Block Diagram

The Debug system block diagram is shown in ***Figure 292***.

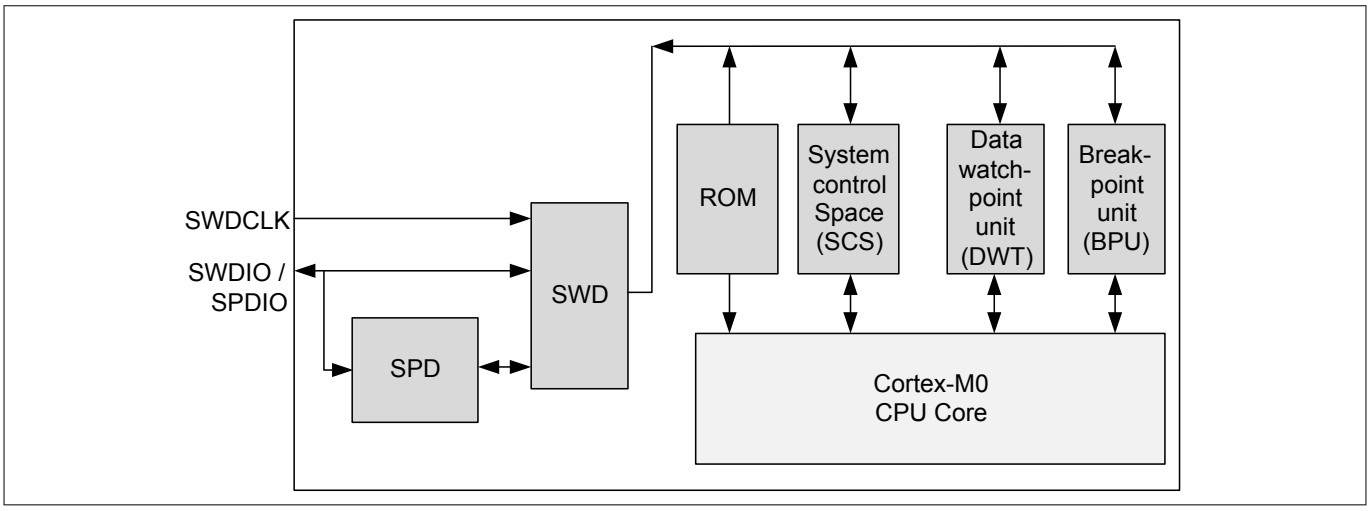


Figure 292 Debug and Trace System block diagram

29.2 Debug System Operation

The Debug System provides general debug options. Debug options are based on break points and CPU halt. Debug resources available are Data Watchpoint and Trace, Breakpoint unit, ROM table and the SCS system control block and debug control block. Debug capabilities can be accessed by a debug tool via Serial Wire Debug interface (SWD) or Single Pin Debug (SPD). The selection of the access protocol (SWD or SPD) is done by BMI mode setting.

29.2.1 System Control Space (SCS)

The SCS is the area where the debugger can have direct access to the memory mapped register debug register. The debug resources together with the debug register in the SCS are accessible through the DAP interface. Accessible resources are for example system control and ID registers including system control block. Additionally the system timer and the interrupt controller (NVIC) can be accessed via the SCS.

29.2.2 Data Watchpoint and Trace (DWT)

The DWT unit provides an external Program Counter (PC) sampling capability based on PC sample register and comparators, that support watchpoints for address matching and PC watchpoints for instruction address matching. The PC sampling feature and watchpoint support operate independently of each other and a watchpoint event is asynchronous to the instruction that caused it. The IMC300A supports two watchpoints, each supporting compare, mask and function registers. Watchpoint events result in a processor halt and enters the processor system into debug state. Data address matching results in a creation of a watchpoint event. Instruction address matching in a creation of a PC watchpoint event. The DWT register are accessible through the DAP interface.

A DWT program counter sample register permits a debugger to periodically sample the PC without halting the processor and allows coarse grained profiling. The PC sampling feature and the watchpoint support operate independently of each other. The register is defined so that a debugger can access it without changing the behavior of any code currently executing on the device.

The recommended mechanism for generating a breakpoint on a single instruction address is to use the BPU. The DWT based mechanism must be used to generate a PC matching event on a range of addresses. The debug return address value for a watchpoint event must be that of an instruction to be executed after the instruction responsible for generating the watchpoint.

29.2.3 Break Point Unit (BPU)

The Breakpoint (BKPT) instruction provides software breakpoints. It can cause a running system to halt depending on the debug configuration. A BKPT is a synchronous debug event, caused by execution of a BKPT instruction or by a match in the BPU. A BKPT causes the processor to enter debug state. The Debug tool can use this situation to investigate the system state when the instruction at a particular address is reached. The BPU provides support for breakpoint functionality on instruction fetches, based on instruction address comparator. The M0 provides four breakpoint comparator registers. Each breakpoint comparator register includes its own enable bit. The comparators match instruction fetches from the Code memory region and operate only on instruction read accesses. The comparators do not match data read or data write access. Address matching is available on the upper half word, lower half word or both half words. Potential reasons for a debug event are a debug halt, a BKPT, a DWT trap and Vector CATCH.

29.2.4 ROM Table

To identify the Cortex-M0 processor with the respective Debug System components the debugger locates and identifies the ROM table. ROM table Identification values are predefined and contain pointers to the SCS, BPU and DWT. Each of the debug modules requires it's own ROM table and indicate whether the block is present. The ROM table can be accessed through the DAP interface.

29.2.5 Debug tool interface access - SWD

The tool access based on SWD must use a connection sequence, to ensure that hot-plugging the serial connection does not result in unintentional transfer. The connection sequence ensures that the SWD is synchronized correctly to the header. The sequence consists of a sequence of 50 clock cycles data = 1s. This connection sequences is also used as a line reset sequence. The protocol requires that any run of 50 consecutive 1s on the data input is detected as line reset, regardless of the state of the protocol. After the line reset the debugger reads IDCODE register, which gives confirmation that correct packet frame alignment is has been achieved.

29.2.5.1 SWD based transfers

The SWD interface requires to continue the clock for a number of cycles after the data phase of any data transfer. This ensures the transfer is completely clocked through the SWD. The transfer completion can be achieved by a immediate start of a new SWD operation, continuos clocking of SWD interface until the host starts a new SWD operation or after the data parity bit the clock is continued for at least 8 more clock rising edges, before stopping the clock.

Each sequence of operation on the serial wire consists of two or three phases and is defined from debugger point of view. The package request and acknowledge response phases are always there. The data transfer phase is only present when either data read or data write request is followed by a valid acknowledge response or the Overrun Detect flag is set.

The SWD protocol applies a simple parity check to all packet request and data transfer phases. On a packet request the parity check is made over the four bit header. On a data transfer the parity check is made over the complete 32 data bits. The parity is added directly after the packet request and after the data transfers. The parity bits are not included in the parity calculation.

Serial Wire Debug protocol operation

The SWD protocol supports the following operations:

- **Write operation** including OK response (3-Phases: 8-bit write packet request, 3-bit OK ACK, 33-bit data write including1-bit parity at the end)
- **Read operation** including OK response (3-Phases: 8-bit read packet request, 3-bit OK ACK, 33-bit data read including a 1-bit parity at the end).

- **WAIT response** to read or write operation request (2 Phases: 8-bit read or write packet request, 3-bit WAIT ACK response)
- **FAULT response** Read or Write operation (2-Phases: 8-bit read or write packet request, 3bit FAULT ACK response)
- **Protocol error** sequence occurs when target failed to return a ACK response (1 Phase: 8-bit Packet request - line not driven by target for 32 bit cycles)

Note: A single-cycle turnaround period between the operation phases is required, for the transfer direction change only. If there is no transfer direction change, no turnaround period is introduced. If the protocol ends with a data transfer towards the debugger a turnaround period is introduced. After the single-cycle turnaround time the protocol must be proceeded.

29.2.5.2 SWD based errors

On the SWD interface protocol errors can occur. These errors might be detected by the parity checks on the data. A message header error can be detected by a parity error. A debugger not receiving a response or a port does not respond to the message, the debugger must back off. During the back off mechanism the debugger does read the IDCODE register and ensures the Debug Port is responsive and then retries the original access.

Errors can be returned by the DAP itself or might come from a debug resource. When an error occurs the error bit remains sticky until cleared. A debugger must check the error status after performing a series of transaction to be aware of an error.

Error conditions within the SWD interface are recorded using sticky flags. Potential errors are read and write errors, overrun detection, protocol errors. When the sticky bit is set to 1 it remains set until it is explicitly cleared to 0. When an error is flagged the current transaction is completed and any additional access port access transaction is discarded until the sticky flag is cleared to 0. A debugger must check periodically the Control/Status register after performing a series of transactions to detect the error.

A read and write error might occur within the DAP or come from the resource being accessed. Additionally a read or write error might be generated if the debugger makes an access port transaction request while the debugger power domain is powered down.

An overrun error might be detected on a sequence of transactions. Therefore the debugger must check after each sequence. The Overrun detection mode can be left by clearing the STICKYORUN and ORUNDETECT.

On the Serial Wire Interface protocol errors can occur, for example because of wire-level errors. These errors might be detected by the parity checks of data. If the SWD interface detects a parity error in a message header of the debug message the error is reflected. If the interface does not receive a response to a message, the debugger must back off. It must then requires a read of the IDCODE register, to ensure the debug port is responsive, before retrying the original access, again. If the SWD detects a parity error in the data phase of a write transaction, it sets the sticky write data error flag (WDATAERR) in the control and status register. Subsequent accesses from the debugger, other than IDCODE, CTRL/STAT or ABORT, result in a FAULT response.

29.2.6 Debug tool interface access - Single Pin Debug (SPD)

The SPD protocol based tool interface access allows to debug the system using a single pin only. The bit frequency is 2 MHz and allows an effective SWD telegram of 1.4 Mbits/s. The protocol is very robust against clock deviations between tool and device.

The SPD protocol encodes the SWD protocol bits with the distance between the SPD signal edges. A SWD value of ‘0’ is encoded with a short distance of 0.5 µs, a value of ‘1’ with a distance of 1 µs. This encoding is used in both transfer directions. Initially the SPD signal level always start with a positive SPD signal pulse with 1 µs width, encoded SPD start bit, which is not part of the SWD protocol. The transmission of the rest of the telegram will be independent of the edge direction. As the protocol starts with a logic one start bit detection it is recommended to finish the protocol with a logic 0 signaling level. If the SPD signal level is high after the last bit

of the telegram, that tool to add at '0' bit with a negative edge after 0.5 µs. This can be achieved by the tool transferring an odd number of bits.

SWD has a clean request response protocol, where the tool is always the requestor and the device executes and sends a response. So the SWD module will change the direction as defined by the SWD protocol operations (***Chapter 29.2.5.1***).

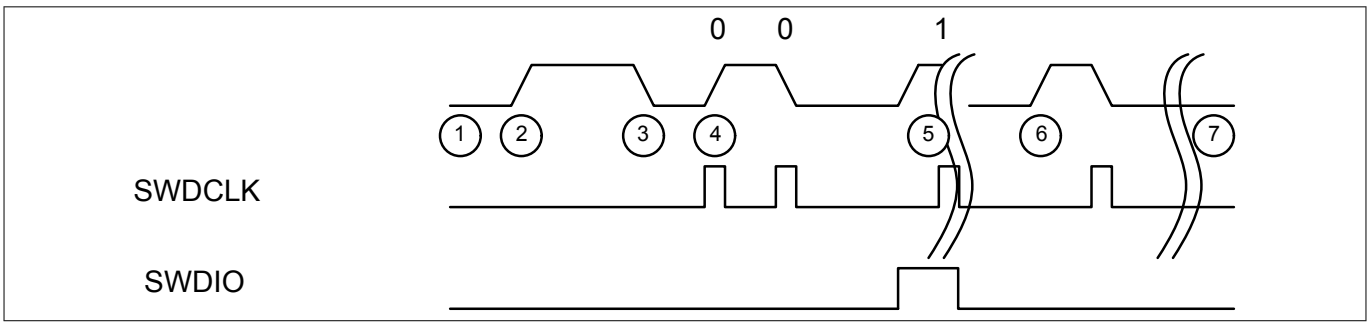


Figure 293 SPD Encoding Example

As a basic example a simple transfer is described in Figure before. Initially (1) the SPD module is in IDLE state. During IDLE state the SPD module does not generate a clock to the SWD module. At point (2) the SPD detects a rising edge and moves to a receive state. The first rising edge of the protocol is a start bit for the SPD module only and is not transferred to the SWD module. The following bits are the SWD header information and transferred to the SWD module. At point (5) a logic 1 shown and at (6) a logic zero. At the time the protocol direction is changed (which means for the implementation to go through IDLE state) the clock to SWD is switched off as shown in state (7). The SPD module requires to end on a Low signal value therefore it is required to have an odd number of bits moved into the interface.

Protocol transfer requirements between SWD and SPD module

The data transfer to and from SWD protocol is single bit based on the SWD clock. The SWD clock is generated by the SPD module and directly derived from the transferred bit. In RECEIVE direction the SPD module transfers the data to the SWD module bit wise, with one clock cycle per bit received.

The SPD module switches off SWD clock when going through module IDLE.

The Debugger adds a SPD start bit in front of the SWD telegram when it writes data to the device (form SPD point of view, RECEIVE). The SPD RECEIVE start bit is not transferred to the SWD module. The RECEIVE start bit is in front of the original SWD protocol on every new RECEIVE start, which is in front of the SWD header and again in front of debugger write data. Additionally the SPD module requires in RECEIVE direction a protocol to end with a logic zero signal level, which is achieved by an odd number of bits transferred by the tool. Based on the SWD protocol this is already achieved in the header phase by adding the described SPD start bit. During acknowledge phase as this phase does have 3 bits only. During the protocol data phase the Debugger has to add one more zero bit. (SPD Start bit, 32-bit data, parity bit, SPD odd bit as logic Zero).

As the SWD protocol requires in RECEIVE direction at least 8 clocks at the end of the data transferred to finish the protocol operation the Debugger has to add 9 logic zeros to the protocol (8 for this requirement and 1 to have an odd number).

SPD protocol based tool Interaction

All SPD communication is initiated by the tool. The tool will send a SWD header encoded to a SPD telegram (header) and then switches the SPD signal direction to input and wait for the acknowledge from the device.

SPD RECEIVE

Based on a low level the tool starts the protocol with SPD start bit. The start bit is indicated with a rising edge and a signal duration of 1µs. The following bits are based on the SWD protocol sequence.

The start sequence: SPD start bit + SWD HEADER + 0 Bit + 0 Bit (The two additional 0 bits at the end are required to achieve a low level at the signaling line.)

After receiving the header, the SWD will output his acknowledge response. Thus, SPD will change from RECEIVE to IDLE to SEND and ACK to IDLE again.

Leaving IDLE to RECEIVE state to transfer write data the start bit from tool is also required.

The SPD start bit must be a logic one with the defined time duration of a logic one. Is the signal duration longer it turns into a timeout situation. Is the signal duration shorter the start bit is not recognized.

The debug tool not sending data continuously in SPD RECEIVE direction, generates a Timeout in SPD module, which brings it to IDLE mode again. Starting from IDLE state the tool is required to provide SPD start bit for a new communication. A timeout is recognized after 1.4 µs.

A permanent write (SPD RECEIVE) allows to proceed the protocol without SPD start bit. In this case the SPD interface remains in RECEIVE state and only the SWD receive protocol has to be performed. In this case the SWD header has to start with a logic 1 as defined by the SWD protocol.

SPD SEND

The tool is required to end a RECEIVE at low level. Based on the low level the SEND start is indicated by a rising edge. SEND has to end with a signal low level, too.

IDLE

From RECEIVE to IDLE - driven by SPD or by timeout.

From SEND to IDLE - driven by SWD module caused by direction change.

Time to switch from RECEIVE to SEND is between 375 and 500 ns and always goes through IDLE phase. The tool must change from write (SPD RECEIVE) to read (SPD SEND) direction within 375 ns. SEND always starts with a rising edge.

29.2.7 Debug accesses and Flash protection

The IMC300A Flash implements read protection for sector 0 only. All other sectors can be read. Additionally a user configuration erase and write protection is available, which allows to protect Flash content from unintended writes or erase. Special care is taken, that the debugger can’t bypass this protection.

Because of this, per default and after a system reset the debug interface is disabled. The Boot Mode Index (BMI) determines if the debug mode can be entered and the debug interface enabled at the end of the SSW.

Before the BMI is configured to user productive mode a change of BMI to arbitrary value is supported, afterwards BMI can only be restored to its default value, which does not enable debug access.

Besides the BMI configuration the Debug system supports a protection mechanism which prevents a debug access to the system address area during the time startup software (SSW) is running. Fimware controls the debug access, based on register setting.

Software based Breakpoints are supported, but prevented during SSW.

29.2.8 Halt after reset

There are two possibilities to perform a halt after reset. The first possibility is Infineon specific an allows to perform a CPU halt after “power on”/”master” reset (HAR) at the very first instruction of the Application code. The HAR activation is based on BMI settings and SSW executing endless loop, allowing a debugger to take control over the device. A defined configuration sequence driven by the connected debug tool is required in this case. The second possibility is the regular ARM flow halt after reset, which is based on breakpoints and a system reset. This halt after reset is also named “Warm Reset”. In both cases the ARM system can not be accessed for security reasons from the debug port during the time SSW is running, as the physical pins are not available during that time. Based on the BMI setting the debug capability can be enabled at the end of the SSW by firmware. The default BMI configuration does not enable debug access.

29.2.8.1 HAR

The BMI can be configured to allow a HAR (UMHAR) at the end of the SSW, which always requires a power on reset to be executed. A new BMI configuration to BMI.UMHAR (User Mode with debug enabled and HAR) requires to perform a master reset to boot in UMHAR mode.

At a HAR (Cold Reset situation), the system comes from a PORST (or Master Reset). To achieve a HAR, the tool has to register (CDBGPWRUPREQ) and enable (DHSCR.C_DEBUGEN) the debug system. Additionally it has to halt (DHCSR.C_HALT) the CPU and manipulate the PC (Program Counter) to point to the start address of the user code. The debugger registration and debug system enable is possible at the end of the firmware, where firmware is waiting for a tool registration. During SSW execution the debugger as no access capability and cannot set the enabling bits CDBGPWRUPREQ, C_DEBUGEN or halt the CPU. The address of the user code start address can be read from address 0x10001004 in user Flash. It is recommended to check the Boot Mode Index BMI.HWCFG bit for UMHAR before manipulating the PC.

The following Figure (***Figure 294***) shows the software flow based on the modules participating to the HAR.

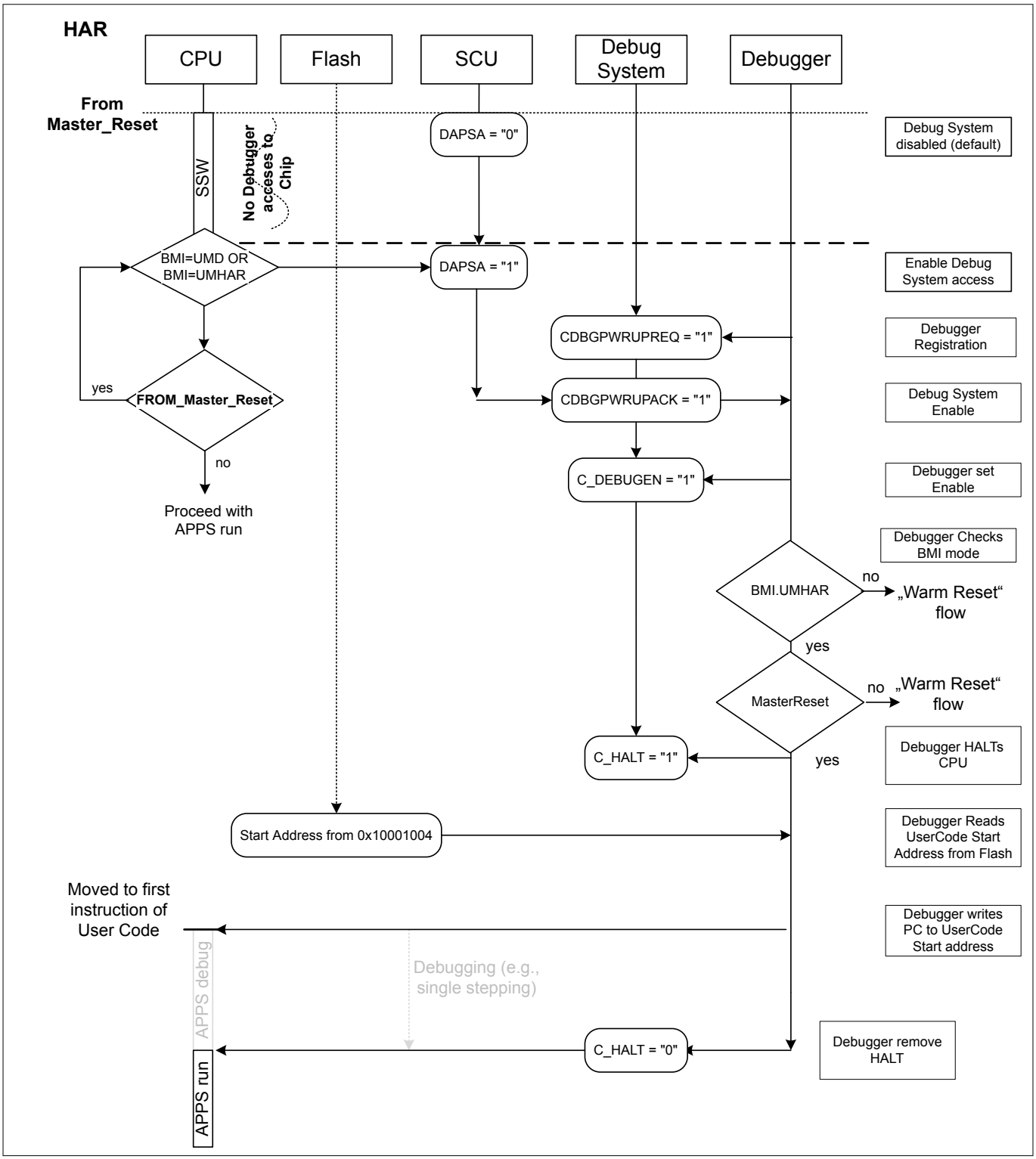


Figure 294 HAR - Halt After Reset Flow

29.2.8.2 Warm Reset

A halt after system reset (Warm Reset) can be achieved by programming a break point at the first instruction of the application code. Additionally the CDBGPWRUPREQ (tool registration) and the C_DEBUGEN has to be set by the debugger. After a system reset, the HAR situation is not considered, as the reset is not coming from PORST (Master_Reset).

Note: The CDBGPWRUPREQ and C_DEBUGEN does not have to be set after a system reset, if they have already been set before and the debugger remains registered. The bits are not affected by the system reset.

A tool hot plug situation allows to debug the system by enabling the CDBGPWRUPREQ and the C_DEBUGEN register. It is recommended to check the Boot Mode Index BMI.HWCFG. The Warm Reset flow can be done in both BMI modes, UMD (User mode with debug enabled) and UMHAR. In both cases the “Warm Reset” flow is based on breakpoint setting and system reset afterwards.

In general after a tool hot plug break points can be set or the CPU can directly be HALTED and stops at the actual program stage. To stop at the very first instruction of the user code the tool has to fire a system reset after setting the breakpoint there.

The following Figure (***Figure 295***) illustrates the debug tool HOT PLUG situation or the Halt after Warm Reset (system reset) and how to proceed to come to a Halt situation.

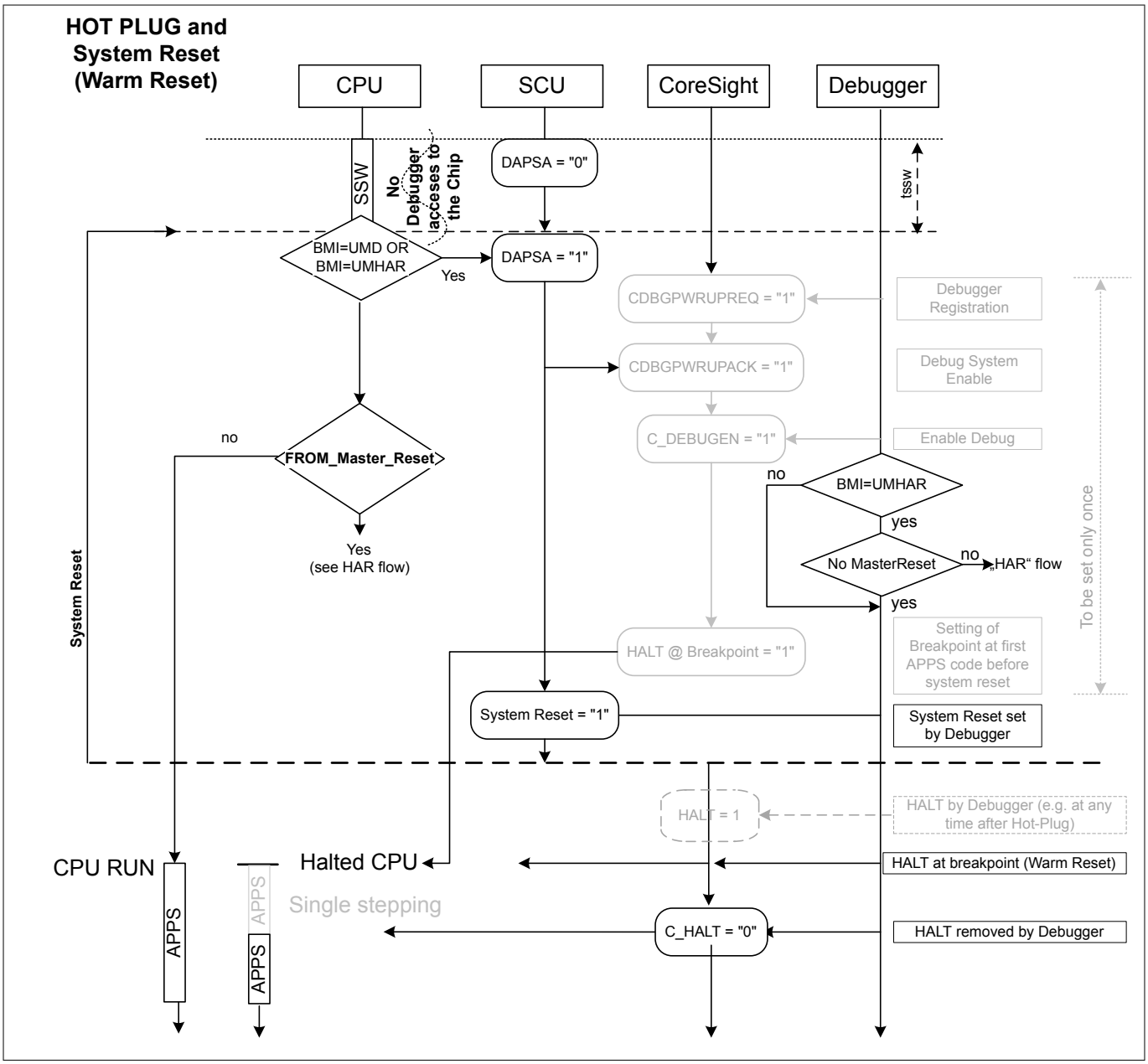


Figure 295 HOT PLUG or Warm Reset Flow

29.2.9 Halting Debug and Peripheral Suspend

The IMC300A device supports a suspend capability for peripherals, if the program execution of the CPU is stopped by the debugger, e.g. with a breakpoint, or with the C_HALT. This allows to debug critical states of the whole microcontroller. Whether the suspend function is supported or not has to be configured locally at the peripheral.

In some cases it is important to keep certain peripherals running, e.g. a PWM or a CAN node, to avoid system errors or even critical damage to the application. Because of this, the peripheral allows to configure how it behaves, when the CPU enters halt debug mode. Per default a peripheral is not sensitive on a suspend request. Sensitivity can be configured based on the system use case.

It can be decided at the peripheral to support a Hard Suspend or a Soft Suspend. At a Hard Suspend situation the clock at the peripheral is switched off immediately, without waiting on acknowledge from the module. At a soft suspend the peripheral can decide when to suspend. Usually at the end of the actual active transfer.

A Watchdog timer is only running when the suspend bus is not active. This is particularly useful as it can't be serviced by a halted CPU. A configuration option is available, which allows to enable the Watchdog timer also during suspend. This allows to debug Watchdog behavior, if a debugger is connected.

The user has to ensure, that always only those peripherals are sensitive to suspend, which are intended to be. To address this, each peripheral supporting suspend does have an enable register which allows to enable the suspend feature. The following table (***Table 313***) shows the peripherals, supporting or not supporting peripheral suspend or detailed information on the peripheral suspend behavior during soft suspend can be found at the respective peripheral chapter.

Table 313 Peripheral Suspend support

Peripheral	supported	default mode	Hard Suspend	Soft Suspend
RTC	yes	not active	yes	no
USIC	yes	not active	no	yes
CCU4	yes	not active	yes	yes
CCU8	yes	not active	yes	yes
POSIF	yes	not active	yes	yes
DAC	yes	not active	yes	no
WDT	yes	active	yes	no
ADC	yes	not active	yes	yes
VADC	yes	not active	yes	yes
MATH	yes	not active	yes	yes
PRNG	no	- - -	- - -	- - -
MultiCAN+	no	- - -	- - -	- - -

Note: Enable debug suspend function in the user initialization code after every reset. In addition the user has to consider debug suspend register at peripherals can only be configured after the clock of the module is enabled via CGATCLR0 register.

Important tool provider note:

The peripheral suspend logic is connected to the system reset. A system reset activation results in a peripheral suspend configuration loss. Therefore the suspend configuration at the peripherals "outlasting" a system reset, requires the tool to reconfigure the suspend configuration after system reset. This is achieved by shadowing the

user peripheral suspend configuration in the tool and set a HW breakpoint at the first instruction of use code, if the suspend function is activated. After the CPU halts at that breakpoint the tool has to reconfigure the suspend configuration at the peripheral, as it has been configured before the system reset.

Note: Suspend activation results in loosing one HW breakpoint, as it is used by the tool to handle the suspend reconfiguration after system reset.

A debug tool should offer the peripheral suspend reconfiguration after system reset with an option to proceed Usercode without an user interaction requirement after tool reconfiguration or remain stopped at first line of user code and wait for user action.

(The user configures the desired suspend behavior only once and the tool stores the configuration to have it present for a automatic reconfiguration after a system reset.)

29.2.10 Debug System based processor wake-up

The debugger can wake-up a processor in sleep mode (sleep and deep sleep mode). The wake-up is based on a new pending interrupt event from the debug system, which is a HALT. The interrupt event does also wake-up the processor, if the interrupt is disabled or has insufficient priority to cause exception entry. The interrupt wake-up mode is derived by the NVIC (Programmable Multiple Priority Interrupt System) available in the processor system. The debugger is able to register, enable the Debug System and HALT the CPU also in sleep and deep sleep mode.

Note: The wake-up from deep-sleep mode via debugger halt is only supported using SWD interface. A wake-up from deep-sleep based on SPD interface is not supported.

29.2.11 Debug Signals

IMC300A MC product family provides debug capability using ARM M0 Debug port SWD or the Infineon proprietary SPD. The SWD Port has 2 interface signals (Clock + Bidirectional data). The SPD port has one interface signal (SPDIO - bidirectional data) with an overlay of SWD interface SWDIO pin.

Table 314 SWD toplevel IO signal

Signal	Direction	Function
SWDCLK	I	Serial Wire Clock. This pin is the clock for debug module when running in Serial Wire debug mode.
SWDIO	I / O	Serial Wire debug data IO. Used by an external debug tool to communicate with and control the Cortex-M0 debug system.

The HALTED and EDBGRQ signals can be used to halt the CPU based on an external event. This allows to halt an external hardware synchronously with the CPU. The halt can be recognized by the external hardware based on the HALTED output. This can be used for example to synchronize with an logic analyzer and request a breakpoint or in a multi CPU scenario.

29.2.11.1 Internal pull-up and pull-down on SWD/SPD pins

It is a requirement to ensure none floating SWD/SPD input pins, as they are directly connected to flip-flops controlling the debug function. To avoid any uncontrolled I/O voltage levels internal pull-up and pull-downs on SWD/SPD input pins are provided.

- SWDIO/SPD: Internal pull-up
- SWCLK: Internal pull-down

29.2.12 Reset

The debug system register bits are reset by Power-on reset. Other reset in the system do not have an effect on the debug register, if the tool is registered.

29.3 Debug System Power Save Operation

The Debug System is in the “always-on” power domain, which allows to connect the debugger to the device. The Debug System does not support any special power mode or power save operation. The power supply of the Debug System is directly connected to the main chip part including the system components.

29.4 Service Request Generation

The debugger can set DHCSR.C_MASKINTS to 1 to prevent PendSV, SysTick and external configured interrupts from occurring.

29.5 Debug behavior

The Debug System is based on events. Whereas events are an entry to debug state, if halting debug is enabled. Debug events available are:

- Internal halt request
- Breakpoint
- Watchpoint
- Vector catch
- External debug request based on

The following events are synchronous debug events:

- Breakpoint debug events, caused by execution of a BKPT instruction
- Breakpoint debug events, caused by execution of a match in the BPU
- Vector catch debug events
- Step debug events (DHCSR.C_STEP)

The following events are asynchronous debug events:

- Watchpoint debug events, including PC match watchpoints
- Halt request debug event (DHCSR.C_HALT)
- External signal based debug request event (EDBGRQ signal)

Asynchronous debug events do have a lower prioritization then synchronous generated events. An instruction can generate a number of synchronous debug events. It also can generate a number of asynchronous exceptions.

The Debug Fault Status register (DFSR) contains a status bit for each debug event. The bits are write-one-to-clear. These bits are set to 1 when a debug event causes the processor to halt or generate an exception. The bits are also updated if the event is ignored.

Software must write 0xA05F to the DHCSR.DBGKEQ register in order to be able to have debug support available form CPU side.

29.6 Power, Reset and Clock

The requirements for power, reset and clock are derived from ARM.

29.6.1 Power management

There is no power management implemented for the debug system. Nevertheless the tool does has to follow the regular tool flow by setting the CDBGPWRUPREQ in order to register the tool.

29.6.2 Debug System reset

The SWD register are in the power on reset (PORST) domain.

The Debug logic is reset by system reset, if no tool is connected to chip and therefore not registered, which is indicated by CDBGPWRUPREQ not set.

Processor reset

A processor or warm reset (SYSRESETn) initializes the majority of the processor, excluding debug logic, BKPT unit, DWT unit and SCS.

PowerOn reset

PORESETn reset initializes the SWD access port, the AHB-AP logic and all other debug system related functions.

Normal operation

During normal operation the resets PORESETn and SYSRESETn are deasserted.

Processor reset affects Debug System

A System reset also affects the Debug System, if a tool is not registered. The tool registration is reflected by an activation of the register bit CDBGPWRUPACK, which activates by a debugger enabling the CDBGPWRUPREQ.

29.6.3 Debug System Clocks

The Debug system clock is called DCLK and is derived directly from SCLK (free running clock). DCLK must always be driven while a debugger is connected.

29.7 Initialization and System Dependencies

29.7.1 ID Code

Available ID Code is used by a debug tool to identify the available debug components during tool setup.

Table 315 ARM CoreSight™ Component ID code

ID	Value	Description
SW_DP	0BB1 1477$_H$	The ARM SW-DP ID

29.7.2 ROM Table

To identify Infineon as manufacturer and IMC300A as device, the ROM table has to be read out. The format of the ROM table is illustrated in ***Table 316***.

Table 316 Peripheral ID Values of IMC300A ROM Table

Name	Offset	Value[77]	Bits	Reference	Infineon JTAG ID Code
PID0	$FE0_H$	XXXXXXXX_B	[7:0]	Part Number [7:0]	DBGROMID [19:12]
PID1	$FE4_H$	$0001XXXX_B$	[7:4] [3:0]	JEP106 ID code [3:0] Part Number [11:8]	DBGROMID [4:1] DBGROMID [23:20]
PID2	$FE8_H$	$XXXX1100_B$	[7:4] [3] [2:0]	Revision JEDEC assigned ID fields JEP106 ID code [6:4]	DBGROMID [31:28] '1' DBGROMID [7:5]
PID3	FEC_H	00000000_B	[7:4] [3:0]	RevAnd, minor revision field Customer-modified block (if non-zero)	
PID4	$FD0_H$	00000000_B	[7:4] [3:0]	4KB count JEP106 continuation code	4KB count DBGROMID [11:8]

The ROM table values representing Infineon Part Number, JEP106 and Revision number can be checked in the SCU chapter.

29.8 Debug System Registers

Registers Overview

The absolute register address is calculated by adding:

The DWT, BPU, ROM table, DCB and debug register in the SCS are accessible memory mapped by the debugger and also from the CPU.

Table 317 Registers Address Space

Module	Base Address	End Address	Note
DWT	$E000\ 1000_H$	$E000\ 1FFF_H$	Data Watchpoint
BP	$E000\ 2000_H$	$E000\ 2FFF_H$	Breakpoint Unit
SCS	$E000\ E000_H$	$E000\ EEFF_H$	SCS (here DBG CTRL)
ROM	$E00F\ F000_H$	$E00F\ FFFF_H$	ROM table area

Table 318 Register Overview

Short Name	Description	Offset Addr.	Access Mode		Description See
			Read	Write	
SCS_DFSR	Debug Fault Status Register	$D30_H$			Page 937
SCS_DHCSR	Debug Halting Control and Status Register	$DF0_H$			Page 938
SCS_DCRSR	Debug Core Register Selector Register	$DF4_H$			Page 943
SCS_DCRDR	Debug Core Register Data Register	$DF8_H$			Page 944

77 For "X" values please refer to DBGROMID in the SCU chapter.

Table 318 Register Overview (continued)

Short Name	Description	Offset Addr.	Access Mode		Description See
			Read	Write	
SCS_DEMCR	Debug Exception and Monitor Control Register	DFC_H			Page 945
DWT_CTRL	DWT Control Register	000_H			Page 946
DWT_PCSR	DWT program Counter Sample Register	$01C_H$			Page 946
DWT_COMP0	DWT Comparator register	020_H			Page 947
DWT_COMP1	DWT Comparator register	030_H			Page 947
DWT_MASK0	DWT MASK register	024_H			Page 948
DWT_MASK1	DWT MASK register	034_H			Page 948
DWT_FUNCTION0	DWT Comparator Function register	028_H			Page 948
DWT_FUNCTION1	DWT Comparator Function register	038_H			Page 948
BP_CTRL	Breakpoint Control register	000_H			Page 949
BP_COMP0	Breakpoint Comparator register	008_H			Page 950
BP_COMP1	Breakpoint Comparator register	$00C_H$			Page 950
BP_COMP2	Breakpoint Comparator register	010_H			Page 950
BP_COMP3	Breakpoint Comparator register	014_H			Page 950

29.8.1 Register SCS_DFSR

The DFSR registers provides the top level reason why a debug event has occurred. Writing 1 to a register bit clears the bit to 0. A read of the HALTED bit by an instruction executed by stepping returns an UNKNOWN value.

SCS_DFSR Address: $D30_H$

Debug Fault Status Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0											EXTERNAL	VCATCH	DWTTRAP	BKPT	HALTED
r											rw	rw	rw	rw	rw

Field	Bits	Type	Description
HALTED	0	rw	**HALTED** Indicates a debug event generated by a C_HALT or C_STEP request, triggered by a write to the DHCSR. 0_B no active halt request debug event. 1_B halt request debug event active.
BKPT	1	rw	**BKPT** Indicates a debug event generated by BKPT instruction execution or a breakpoint match in the BPU. 0_B no breakpoint debug event. 1_B at least one breakpoint debug event.
DWTTRAP	2	rw	**DWTTRAP** Indicates a debug event generated by the DWT. 0_B no debug events generated by the DWT. 1_B at least one debug event generated by the DWT.
VCATCH	3	rw	**VCATCH** Indicates whether a vector catch debug event was generated. 0_B no vector catch debug event generated. 1_B vector catch debug event generated. *Note: The corresponding FSR shows the primary cause of the exception.*
EXTERNAL	4	rw	**EXTERNAL** Indicates an asynchronous debug event generated because of EDBGRQ being asserted. 0_B no EDBGRQ debug event. 1_B EDBGRQ debug event.
0	31:5	r	**Reserved**

29.8.2 Register SCS_DHCSR

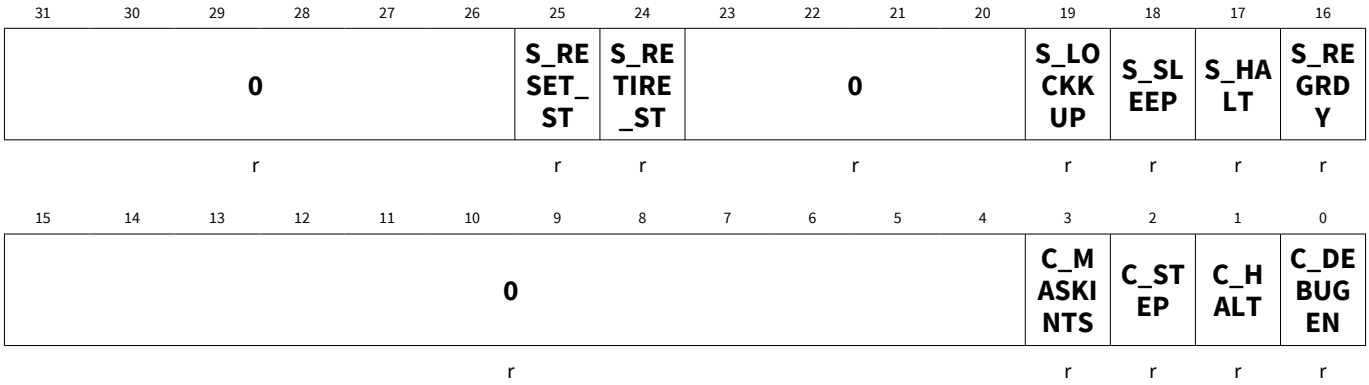
Controls halting debug. When C_DEBUGEN is set to 1, C_STEP and C_MASKINTS must not be modified when the processor is running (S_HALT is 0 when the processor is running). When C_DEBUGEN is set to 0, the processor ignores the values of all other bits in this register.

A separate register is represented below for read and write as the function changes at some bits access based.

29.8.2.1 Register SCS_DHCSR [Read Mode]

SCS_DHCSR Address: $DF0_H$

Debug Halting Control and Status Register [Read Mode] Reset Value: $0000\ 0000_H$



Field	Bits	Type	Description
C_DEBUGEN	0	r	**Halting debug enable bit** 0_B Halting debug disabled. 1_B Halting debug enabled. *Note: If a debugger writes to DHCSR to change the value of this bit from 0 to 1, it must also write 0 to the C_MASKINTS bit, otherwise behavior is UNPREDICTABLE. This bit can only be written from the DAP Access to the DHCSR from Software running on the processor it cannot be set. This bit is 0 after Power-on reset.*
C_HALT	1	r	**Processor halt bit.** The effects of writes to this bit are: 0_B Request a halted processor to run. 1_B Request a running processor to halt. *Note: This bit is unknown after power-on reset*
C_STEP	2	r	**Processor step bit.** The effects of writes to this bit are: 0_B Single-stepping disabled. 1_B Single-stepping enabled. *Note: This bit is unknown after power-on reset*

(continued)

Field	Bits	Type	Description
C_MASKINTS	3	r	**Mask PEDSV, SysTick and external configurable interrupts.** The effects of writes to this bit are: 0_B Do not mask 1_B Mask PendSV, SysTick and external configurable interrupts. The effect of any attempt to change the value of this bit is UNPREDICTABLE unless both: • before the write to DHCSR, the value of the C_HALT bit is 1 • the write to the DHCSR that changes the C_MASKINTS bit also writes 1 to the C_HALT bit. This means that a single write to DHCSR cannot set the C_HALT to 0 and change the value of the C_MASKINTS bit. When DHCSR.C_DEBUGEN is set to 0, the value of this bit is UNKNOWN. This bit is UNKNOWN after Power-on reset.
S_REGRDY	16	r	**S_REGRDY status - a handshake flag for transfers through DCRDR** How to work with: • Writing to DCRSR clears the bit to 0. • Completion of the DCRDR transfer then sets the bit to 1 Check DCRDR for more information. 0_B There has been a wrote to the DCRDR, but the transfer is not complete. 1_B The transfer to or from the DCRDR is complete. *Note: This bit is only valid when the processor is in Debug State, otherwise the bit is UNKONWN.*
S_HALT	17	r	**S_HALT indicates whether the processor is in Debug state.** 0_B Not in Debug State. 1_B In Debug State.
S_SLEEP	18	r	**S_SLEEP indicates whether the processor is sleeping.** 0_B Not sleeping. 1_B Sleeping. *Note: The debugger must set the DHCSR.C_HALT bit to 1 to gain control, or wait for an interrupt or other wake-up event to wake-up the system.*

(continued)

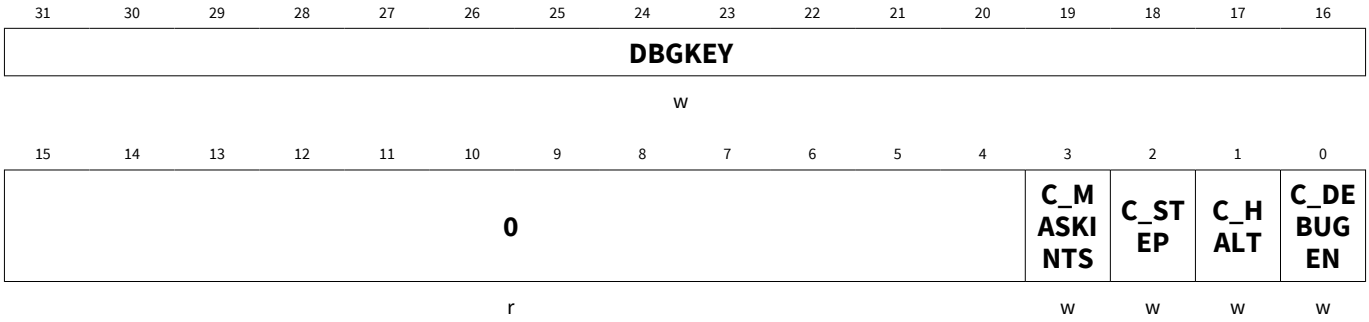
Field	Bits	Type	Description
S_LOCKKUP	19	r	**S_LOCKUP indicates whether the processor is locked up because of an unrecoverable exception.** 0_B Not locked up. 1_B Locked up. *Note: This bit is only read as 1 when accessed by a remote debugger using the DAP. The value of 1 indicates that the processor is running, but locked up due to an unrecoverable exception case.*
S_RETIRE_ST	24	r	**S_RETIRE_ST - When not in Debug state, indicates whether the processor has completed the execution of an instruction since the last read of DHCSR:** 0_B No instruction has completed since the last DHCSR read. 1_B At least one instructions has completed since last DHCSR read. This is a sticky bit, that clears to 0 on a read of DHCSR. This bit is UNKNOWN: • after a Local reset, but is set to 1 as soon as the processor completes execution of an instruction • when S_LOCKUP is set to 1 • when S_HALT is set to 1 *Note: When the processor is not in Debug state, a debugger can check this bit to determine if the processor is stalled on a load store or fetch access.*
S_RESET_ST	25	r	**S_RESET_ST indicates whether the processor has been reset since the last read of DHCSR.** 0_B No reset since last DHCSR read. 1_B At least one rest since last DHCSR read. *Note: This is a sticky bit, that clears to 0 on a read of DHCSR.*
0	15:4, 23:20, 31:26	r	**Reserved**

29.8.2.2 Register SCS_DHCSR [Write Mode]

SCS_DHCSR Address: $DF0_H$

Debug Halting Control and Status Register [Write Mode] Reset Value: $0000\ 0000_H$

29 Debug System (DBG)



Field	Bits	Type	Description
C_DEBUGEN	0	w	**Halting debug enable bit** 0_B Halting debug disabled. 1_B Halting debug enabled. *Note: If a debugger writes to DHCSR to change the value of this bit from 0 to 1, it must also write 0 to the C_MASKINTS bit, otherwise behavior is UNPREDICTABLE. This bit can only be written from the DAP Access to the DHCSR from Software running on the processor it cannot be set. This bit is 0 after Power-on reset.*
C_HALT	1	w	**Processor halt bit.** The effects of writes to this bit are: 0_B Request a halted processor to run. 1_B Request a running processor to halt. *Note: This bit is unknown after power-on reset*
C_STEP	2	w	**Processor step bit.** The effects of writes to this bit are: 0_B Single-stepping disabled. 1_B Single-stepping enabled. *Note: This bit is unknown after power-on reset*

(continued)

Field	Bits	Type	Description
C_MASKINTS	3	w	**Mask PEDSV, SysTick and external configurable interrupts.** The effects of writes to this bit are: 0_B Do not mask 1_B Mask PendSV, SysTick and external configurable interrupts. The effect of any attempt to change the value of this bit is UNPREDICTABLE unless both: • before the write to DHCSR, the value of the C_HALT bit is 1 • the write to the DHCSR that changes the C_MASKINTS bit also writes 1 to the C_HALT bit. This means that a single write to DHCSR cannot set the C_HALT to 0 and change the value of the C_MASKINTS bit. When DHCSR.C_DEBUGEN is set to 0, the value of this bit is UNKNOWN. This bit is UNKNOWN after Power-on reset.
DBGKEY	31:16	w	**DEBUG Key Bits [31:16]!!!** Software must write **0xA05F** to this field to enable write access to bits [15:0], otherwise the processor ignores the write access
0	15:4	r	**Reserved**

29.8.3 Register SCS_DCRSR

The DCRSR together with DCRDR (Debug Core Register Data Register) provides debug access to the ARM core register and special-purpose registers. A write to DCRSR specifies the register to transfer, whether the transfer is a read or a write, and starts the transfer. This register is only accessible in Debug state.

SCS_DCRSR Address: $DF4_H$

Debug Core Register Selector Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															REGWnR
r															rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0											REGSEL				
r											rw				

Field	Bits	Type	Description
REGSEL	4:0	rw	**REGSEL - Specifies the ARM core register or special-purpose register to transfer** 00000_B-01100_B ARM core register R0-R12. For example, 0b00000 specifies R0 and 0b00101 specifies R5 01101_B The current SP. See also values 0b10001 and 0b10010. 01110_B LR. 01111_B Debug Return Address. 10000_B xPSR. 10001_B Main stack pointer, MSP. 10010_B Process stack pointer, PSP. 10100_B Bits[31:24] Control; Bits[23:8] Reserved; Bits[7:0] PRIMASK. In each field, the valid bits are packed with leading zeros. For example DCRDR [31L26] is 0b00000.
REGWnR	16	rw	**REGWnR specifies the type of access for the transfer** 0_B read. 1_B write.
0	31:17, 15:5	r	**Reserved**

29.8.4 Register SCS_DCRDR

The DCRDR works with the DCRSR (Debug Core Register Selector Register). The DCRDR provides debug access to the ARM core registers and special-purpose registers. The DCRDR is the data register for these accesses.

SCS_DCRDR Address: $DF8_H$

Debug Core Register Data Register Reset Value: $xxxx\ xxxx_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DBGTMP															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DBGTMP															
rw															

Field	Bits	Type	Description
DBGTMP	31:0	rw	**DBGTMP - Data temporary cache, for reading and writing register.** This register is UNKONWN: • on reset • when DHCSR.S_HALT = 0 • when DHCSR.S_REGRDY = 0 during execution of a DCRSR based transaction that updates the register.

29.8.5 Register SCS_DEMCR

The DEMCR purpose is to manage vector catch behavior and enable the DWT.

A Power-on reset sets all register bits to 0. A local reset sets DWTENA to 0 but does not affect VC-HARDERR or VC_CORERESET.

SCS_DEMCR Address: DFC_H

Debug Exception and Monitor Control Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0							DWTENA	0							
r							rw	r							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0					VC_HARDERR	0									VC_CORERESET
r					rw	r									rw

Field	Bits	Type	Description
VC_CORERESET	0	rw	**VC_CORERESET - Enable Reset Vector Catch. This causes a Local reset to handle a running system** 0_B Reset Vector Catch disabled. 1_B Reset Vector Catch enabled. *Note: If DHCSR.C_DEBUGEN is set to 0, the processor ignores the value of this bit.*
VC_HARDERR	10	rw	**VC_CORERESET - Enable Reset Vector Catch. This causes a Local reset to halt a running system.** 0_B halting debug trap disabled. 1_B hating debug trap enabled. *Note: If DHCSR.C_DEBUGEN is set to 0, the processor ignores the value of this bit.*

(continued)

Field	Bits	Type	Description
DWTENA	24	rw	**DWTENA - Global enable for all features configured by the DWT unit.** 0_B DWT disabled. 1_B DWT enabled. *Note: When DWTENA is set to 0 DWT registers return UNKNOWN values on reads. In addition the processor ignores writes to the DWT while DWTENA is 0.*
0	31:25, 23:16, 15:11, 9:1	r	**Reserved**

29.8.6 Register DWT_CTRL

The DWT_CTRL register defines the number of comparators implemented.

DWT_CTRL Address: 000_H

Debug Halting Control and Status Register Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NUMCOMP				**0**											
rw				r											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0															
r															

Field	Bits	Type	Description
NUMCOMP	31:28	rw	**Number of comparators available**
0	27:0	r	**Reserved**

29.8.7 Register DWT_PCSR

The DWT_PCSR register samples the current value of the program counter. The register is UNKNOW on reset.

DWT_PCSR Address: $01C_H$

Program Counter Sample Register Reset Value: $xxxx\ xxxx_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EIASAMPLE															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EIASAMPLE															
rw															

Field	Bits	Type	Description
EIASAMPLE	31:0	rw	**EIASAMPLE** Executed instruction address sample register

29.8.8 Register DWT_COMPx

The DWT_COMPx register provides a reference value for use by comparator x. The value is UNKNOW on reset. DWT_CTRL.NUMCOMP defines the number of implemented DWT_COMPx register, from 0 to (NUMCOMP-1).

The DWT_COMP [1 .. 0] register are implemented.

DWT_COMP0 Address: 020_H

DWT Comparator register 0 Reset Value: $xxxx\ xxxx_H$

DWT_COMP1 Address: 030_H

DWT Comparator register 1 Reset Value: $xxxx\ xxxx_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COMP															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP															
rw															

Field	Bits	Type	Description
COMP	31:0	rw	**COMP** Reference value for comparison

29.8.9 Register DWT_MASKx

The DWT_MASKx register provides the size of the ignore mask applied to the access address range matching by comparator x. The value is UNKONWN on reset. DWT_CTRL.NUMCOMP defines the number of implemented DWT_COMPx register, from 0 to (NUMCOMP-1).

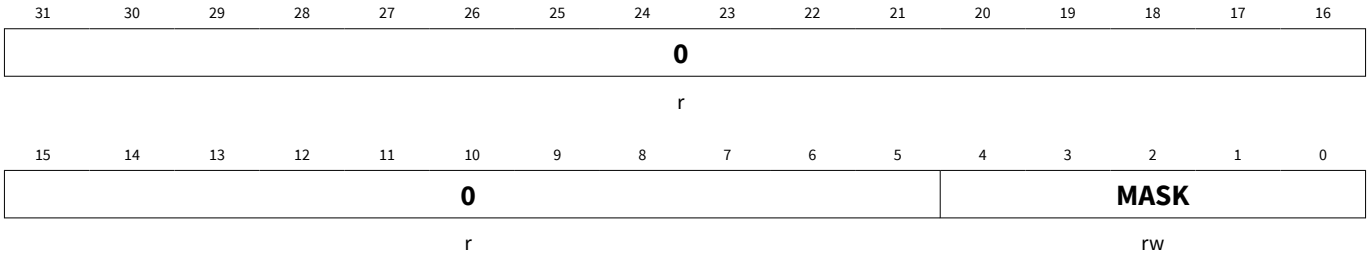
The DWT_MASK [1 .. 0] register are implemented.

DWT_MASK0 Address: 24_H

Debug Halting Control and Status Register Reset Value: $0000\ 0000_H$

DWT_MASK1 Address: 34_H

Debug Halting Control and Status Register Reset Value: $0000\ 0000_H$



Field	Bits	Type	Description
MASK	4:0	rw	**MASK** The size of the ignore mask applied to address range matching. Writing all ones to this field and reading it back can be used to determine the maximum mask size supported (not all mask bit must be implemented).
0	31:5	r	**Reserved**

29.8.10 Register DWT_FUNCTIONx

The DWT_FUNCTIONx register controls the operation of the comparator DWT_COMPx register. DWT_CTRL.NUMCOMP defines the number of implemented DWT_FUNCTIONx registers, from 0 to (NUMCOMP-1).

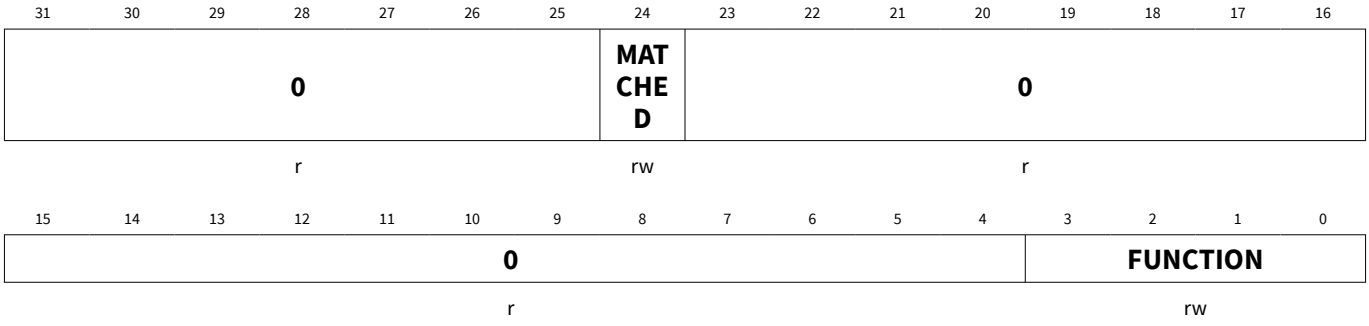
The DWT_FUNCTION [1 .. 0] register are implemented.

DWT_FUNCTION0 Address: 28_H

Comparator Function Register Reset Value: $0000\ 0000_H$

DWT_FUNCTION1 Address: 38_H

Comparator Function Register Reset Value: $0000\ 0000_H$



Field	Bits	Type	Description
FUNCTION	3:0	rw	**FUNCTION** Select action on comparator match- 0000_B Disabled. 0001_B Reserved. 0010_B Reserved. 0011_B Reserved. 0100_B PC watchpoint event - input Iaddr. 0101_B Watchpoint event - input Daddr (read only) 0110_B Watchpoint event - input Daddr (write only) 0111_B Watchpoint event - input Daddr (read/write) $1xxx_B$ reserved *Note: This field is set to 0 on a Power-on reset.*
MATCHED	24	rw	**MATCHED** Comparator match. It indicates that the operation defined by FUNCTION has occurred since the bit was last read. 0_B the associated comparator has matched. 1_B the associated comparator has not matched. *Note: Reading the register clears this bit to 0.*
0	31:25, 23:16, 15:4	r	**Reserved**

29.8.11 Register BP_CTRL

The Breakpoint Control Register provides BPU implementation information and the global enable for the BPU.

BP_CTRL Address: 000_H

Breakpoint Control Register Reset Value: $0000\ 0040_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								NUM_CODE				0		KEY	ENABLE
r								r				r		rw	rw

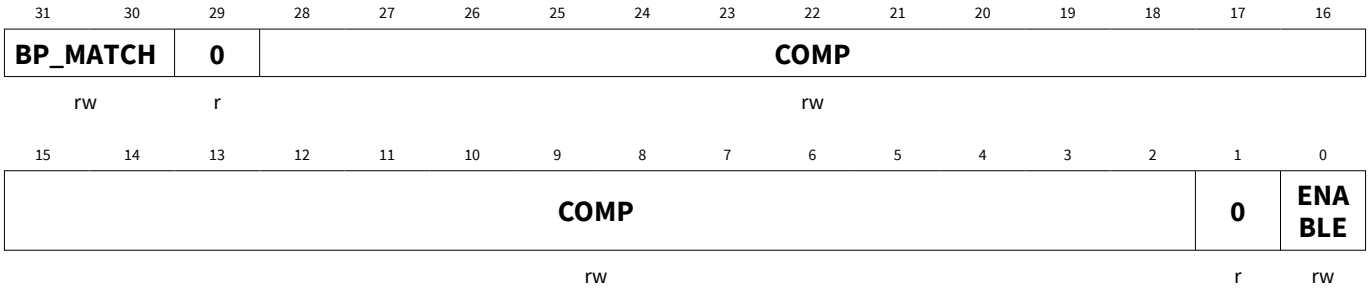
Field	Bits	Type	Description
ENABLE	0	rw	**ENABLE the BPU** 0_B BPU is disabled. 1_B BPU is enabled. *Note: This bit is set to 0 on Power-on reset.*
KEY	1	rw	**KEY reads as 0 on reads, should be 1 for writes.** If written as zero, the write to the register is ignored.
NUM_CODE	7:4	r	**NUM_CODE, the number of breakpoint comparators.**
0	31:8, 3:2	r	**Reserved**

29.8.12 Register BP_COMPx

The BP_COMPx register holds a breakpoint address for comparison with instruction addresses in the Code memory region. A comparator can only be enabled when BP_CTRL.ENABLE is set to 1. BP_CTRL.NUM_CODE defines the number of implemented BP_COMPx registers, from 0 to (NUM_CODE-1).

The BP_COMP [3 .. 0] register are implemented.

BP_COMP0	Address:	008_H
Breakpoint Comparator X Register	Reset Value:	$0000\ 0000_H$
BP_COMP1	Address:	$00C_H$
Breakpoint Comparator X Register	Reset Value:	$0000\ 0000_H$
BP_COMP2	Address:	010_H
Breakpoint Comparator X Register	Reset Value:	$0000\ 0000_H$
BP_COMP3	Address:	014_H
Breakpoint Comparator X Register	Reset Value:	$0000\ 0000_H$



Field	Bits	Type	Description
ENABLE	0	rw	**ENABLE the comparator** 0_B Comparator is disabled. 1_B Comparator is enabled. *Note: This bit is set to 0 on a Power-on reset. BP_CTRL:ENABLE must also be set to 1 to enable a comparator.*
COMP	28:2	rw	**Stores bits [28:0] of the comparison address.** The comparison address is compared with the address from the Code memory region. Bits [31:29] and [1:0] of the comparison address are zero. *Note: The field is UNKNOWN on Power-on reset.*
BP_MATCH	31:30	rw	**BP_MATCH defines the behavior when the COMP address is matched.** 00_B no breakpoint matching. 01_B breakpoint on lower halfword, upper is unaffected. 10_B breakpoint on upper halfword, lower is unaffected. 11_B breakpoint on both lower and upper halfwords. *Note: The field is UNKNOWN on reset.*
0	29, 1	r	**Reserved**

30 References

[1] Cortex™-M0 Generic User Guide, ARM DUI 0497A (ID112109) [78]
[2] ARMv6-M Architecture Reference Manual (ARM DDI 0419) [78]
[3] Cortex-M0 Technical Reference Manual (ARM DDI0432) [78]
[4] CoreSight Components Technical Reference Manual (ARM DDI0314) [78]
[5] CoreSight DAP-Lite Technical Reference Manual (ARM DDI0316) [78]
[6] ARM Debug Interface Architecture Specification V5 [78]
[7] Cortex Microcontroller Software Interface Standard (CMSIS) [78]
[8] References to ARM figures: ***http://www.arm.com***
[9] I2C Bus Specification (Philips Semiconductors v2.1)
[10] Infineon iMOTION™ MCE Software Reference Manual ***http://www.infineon.com/imotion***

78 The document can be accessed through ***http://infocenter.arm.com***

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Document version	Date of release	Description of changes
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