Hardware design guidelines and design calculator for EVAL_PMG1-B1_DRP_KIT

USB PD MCU and charging solution for two-five-cell battery pack

About this document

Scope and purpose

This document provides an overview of hardware design guidelines for EVAL_PMG1-B1_DRP_KIT in cordless power tool chargers, wireless speakers, and portable electronics charging applications (sink/DRP application).

This document also provides comprehensive and easy-to-follow guidelines for the power stage design calculator for the peak current mode controlled (PCMC) and continuous conduction mode (CCM) power tool sink battery charger for 2-5 cell batteries based on the PMG1-B1 USB-PD MCU.

Intended audience

This document is intended for power electronics hardware designers using the EZ-PD™ PMG1-B1 USB PD MCU and USB PD Type-C as the input to the cordless power tool charger, wireless speakers, and portable electronics charging applications (sink/DRP applications).

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1 Introduction

EZ-PD™ PMG1-B1 is a highly integrated single-port USB Type-C Power Delivery (PD) solution with integrated buck-boost controllers and a solution design for cordless power tool charger applications. This solution is based on a peak-current-controlled four-switch buck-boost mode converter (FSBBC) for USB Type-C Power Delivery and is used in cordless power tool chargers, wireless speakers, and portable electronics charging applications (sink applications). The integration offered by EZ-PD™ PMG1-B1 reduces the bill of materials (BOM) and provides a footprint-optimized solution.

EZ-PD™ PMG1-B1 has integrated gate drivers for the V_{BUS} NFET on the consumer path, and GPIO controls the V_{BAT} PFET in the provider path. It includes hardware-controlled protection features on V_{BUS}. EZ-PD™ PMG1-B1 supports a wide input voltage range (4 V to 24 V with 40-V tolerance) and programmable switching frequency (150 kHz to 600 kHz) in an integrated PD solution. The EZ-PD™ PMG1-B1 integration features, such as monitoring, protection, and communication help to build robust cordless power tool chargers, wireless speakers, and portable electronics charging applications (sink applications).

EVAL_PMG1-B1_DRP_KIT has a KITPROG section attached to it which can be used to program the EZ-PD™ PMG1-B1. Pin 1(VDDD),3(GND),5(RESET),7(SWDCLK) and 9(SWDIO) of KITPROG are used to flash the EZ-PD™ PMG1-B1.

EZ-PD™ PMG1-B1 is a programmable USB PD solution with an on-chip 32-bit Arm® Cortex®-M0 processor, 128 KB flash, 16 KB RAM, and 32 KB ROM that leaves most flash available for user application use. It also includes various analog and digital peripherals such as 12-bit analog-digital-converters (ADCs), PWMs, I2C/SPI/UART interfaces, and timers. The inclusion of a fully programmable MCU with analog and digital peripherals allows for the implementation of custom system management functions such as battery pack charging current control, temperature monitoring, and fault protection.

The EZ-PD™ PMG1-B1 USB PD MCU-based charging solution EVAL_PMG1-B1_DRP_KIT for 2-5-cell battery pack needs to deliver a wide range of positive output voltage (varying from 6 V for 2-cell battery to 21 V for 5-cell battery) and power from a Type-C power adapter. The input voltage can be varied from 5 V to 20 V. A four-switch buck-boost converter is the suitable topology, which can support variable input and variable output voltage applications such as a cordless power tool chargers, wireless speakers, and portable electronics charging applications (sink applications).

The four-switch buck-boost converter (FSBBC) configuration can act as a buck, boost, or buck-boost converter to provide an output voltage with the same polarity as the input voltage. Improved efficiency of the FSBBC is observed due to synchronous rectification. In similar lines, buck-only and boost-only operations can be achieved. Constant-frequency peak current mode control (PCMC) is a popular control technique for switched-mode power converters. The PCMC offers built-in overcurrent protection, robust dynamic responses, simplified voltage-loop compensator design, and rejection of input voltage disturbances.

To support DRP applications, external supply is used. When EZ-PD™ PMG1-B1 is detected as a source, it will advertise only 5 V and 9 V power data objects (PDOs) and provide a maximum power of 27 W. Programmable power supply (PPS) mode is not supported in source mode. Along with the buck converter operation, there is a load switch to connect and disconnect the buck converter to the USB Type-C connector.

2 EZ-PD™ PMG1-B1 applications and features

2.1 Applications

- Cordless power tool chargers
- Wireless speakers
- Portable electronics

2.2 Features

2.2.1 USB PD

- Supports a single USB PD port
- Supports the latest USB PD 3.1 specification

2.2.2 Type-C

- Configurable Type-C pull-up termination resistors (RP) and pull-down termination resistors (RD)
- Dead battery support (RD-DB)
- VBUS NFET gate driver
- Integrated 100 mW VCONN power supply, control, and protection

2.2.3 1x buck-boost controller

- 150 kHz to 600 kHz switching frequency
- 5.5 V to 24 V input, 40 V tolerant
- 3.3 V to 21.5 V output
- Supports forced continuous current/conduction mode (FCCM) for minimum ripple
- Soft start to reduce the inrush current
- Programmable spread spectrum frequency modulation for low electromagnetic interference (EMI)
- Supports current sensing for constant current control

2.2.4 1x legacy/proprietary charging blocks

- Supports Apple Charging 2.4 A and USB BC 1.2

2.2.5 System-level fault protection

- On-chip VBUS, overvoltage protection (OVP), undervoltage protection (UVP)
- VBUS to CC short protection
- VOUT undervoltage protection (UVP), overvoltage protection (OVP), and overcurrent protection (OCP)
- VCONN overcurrent protection
- Supports overtemperature protection through the integrated ADC circuit and internal temperature sensor
- Supports connector and board temperature measurement using external thermistors

2.2.6 32-bit MCU subsystem

- 48-MHz Arm® Cortex®-M0 CPU
- 128-KB flash
- 16-KB SRAM
- 32-KB ROM

2.2.7 Peripherals and GPIOs

- Up to 21 GPIOs including 2 overvoltage GPIOs
- 2x 8-bit ADC
- 8x 16-bit Timer/Counter/PWMs (TCPWM)
- 1x 12-bit ADC

2.2.8 Communication interfaces

- 3x SCBs (I2C/SPI/UART/LIN)

2.2.9 Clocks and oscillators

- Integrated oscillator eliminating the need for an external clock

2.2.10 Power supply

- 4 V to 24 V input (40-V tolerant)
- 3.3 V to 21.5 V output
- Integrated LDO capable of 5.0 V at 75 mA
- Integrated standby regulator 3.0 V at 10 mA

2.2.11 Packages

- 48-pin 6 mm × 6 mm QFN
- Supports ambient temperature range (–40°C to +105°C) with 125°C operating junction temperature

2.3 PMG1-B1 functional block diagram

Figure 1 shows a functional block diagram and Figure 2 shows a logical block diagram of the EZ-PD™ PMG1-B1 architecture. For more details, see the EZ-PD™ PMG1-B1 datasheet [8].

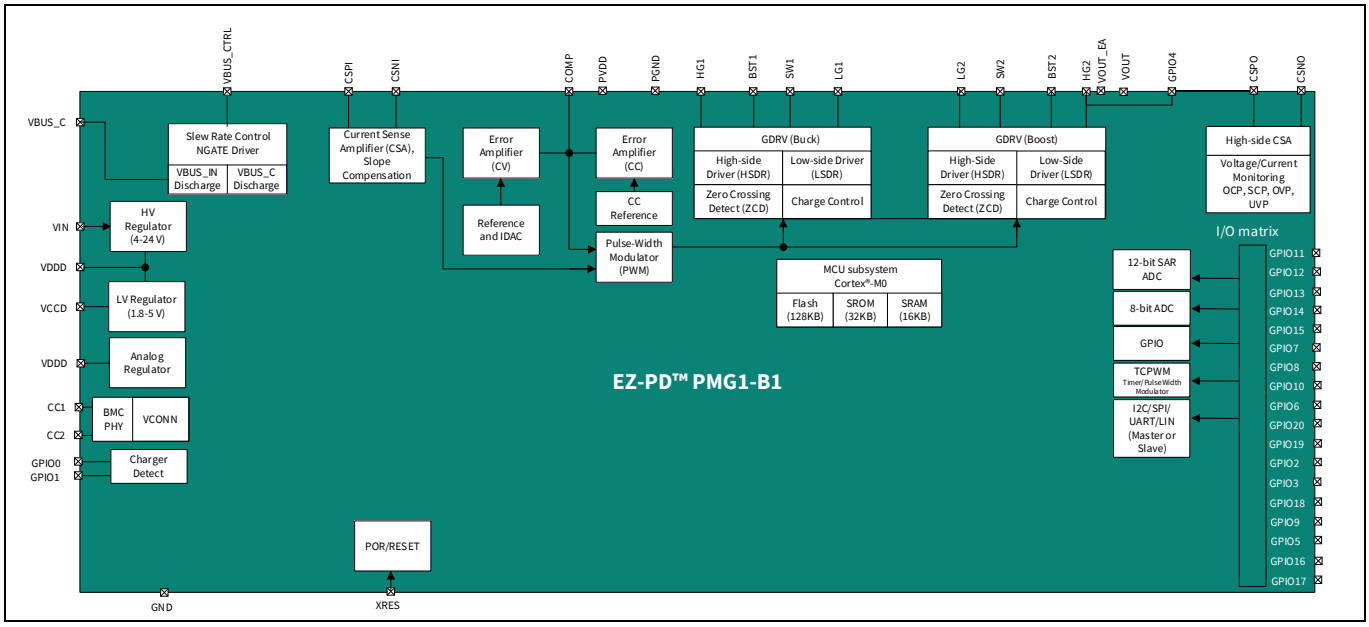

Figure 1 Functional block diagram

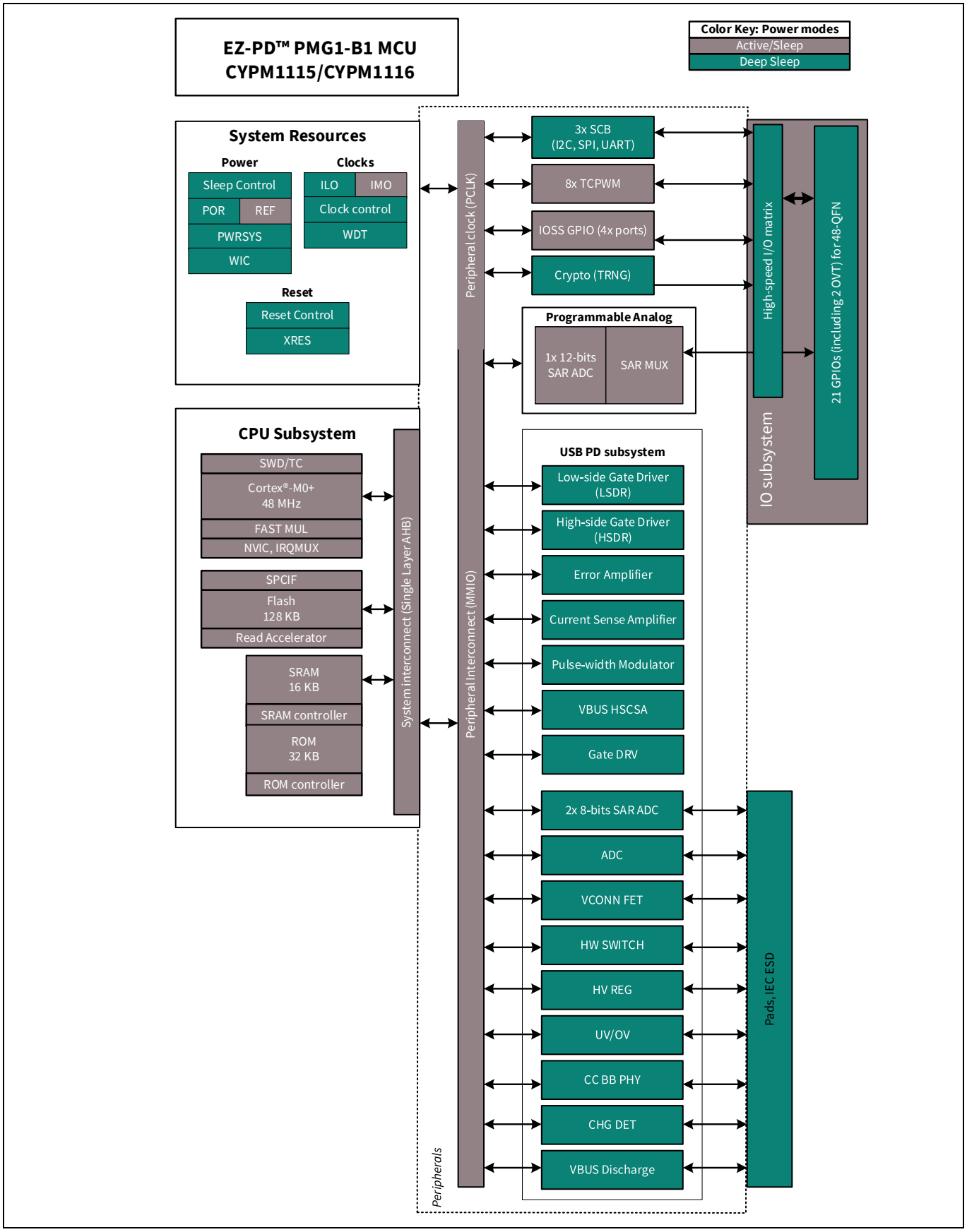

Figure 2 Logic block diagram

2.4 EZ-PD™ PMG1-B1 in cordless power tool charger applications

Figure 3 shows EZ-PD™ PMG1-B1 in cordless power tool charger applications.

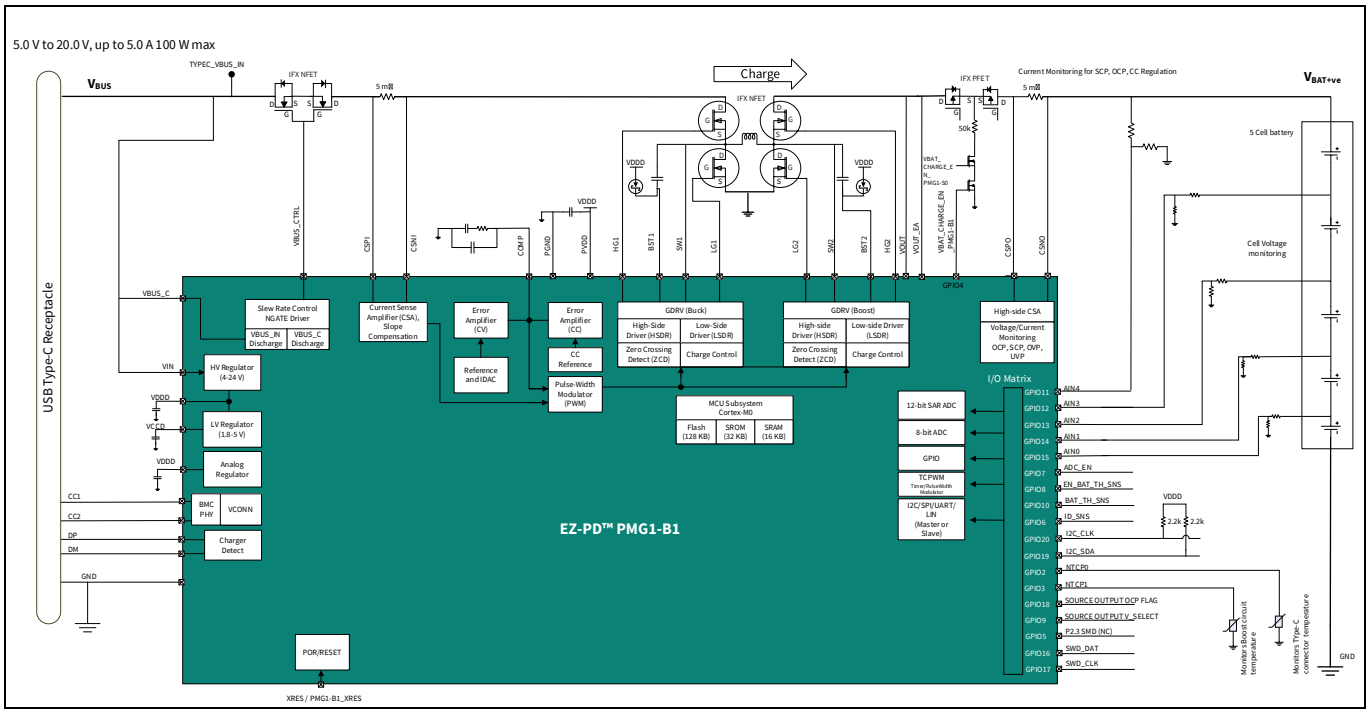

Figure 3 EZ-PD™ PMG1-B1 cordless power tool charger application diagram

3 USB Power Delivery specification

This section provides the basics of USB Power Delivery. The USB PD specification defines a PD-enabled USB port can get the required power from V_{BUS} by negotiating with external power sources (such as wall adapters).

A USB port providing power is known as a 'source', and a USB port consuming power is known as a 'sink'. There is one source port and one sink port in each PD connection. In the legacy USB specification, the USB port on the host computer (such as a notebook or a PC) is always a source and the USB peripheral device is always a sink. The USB PD specification allows the source and sink to interchange their roles so that a USB peripheral device (such as an external self-powered hard disk or monitor) can supply power to a USB host. These new power roles are independent of the USB data transfer roles between the USB host and the USB device. An example is a self-powered USB peripheral, such as a monitor that can charge the battery pack of a Notebook or PC, which is a USB host.

Figure 4 shows a logical block diagram of the Type-C and PD architecture.

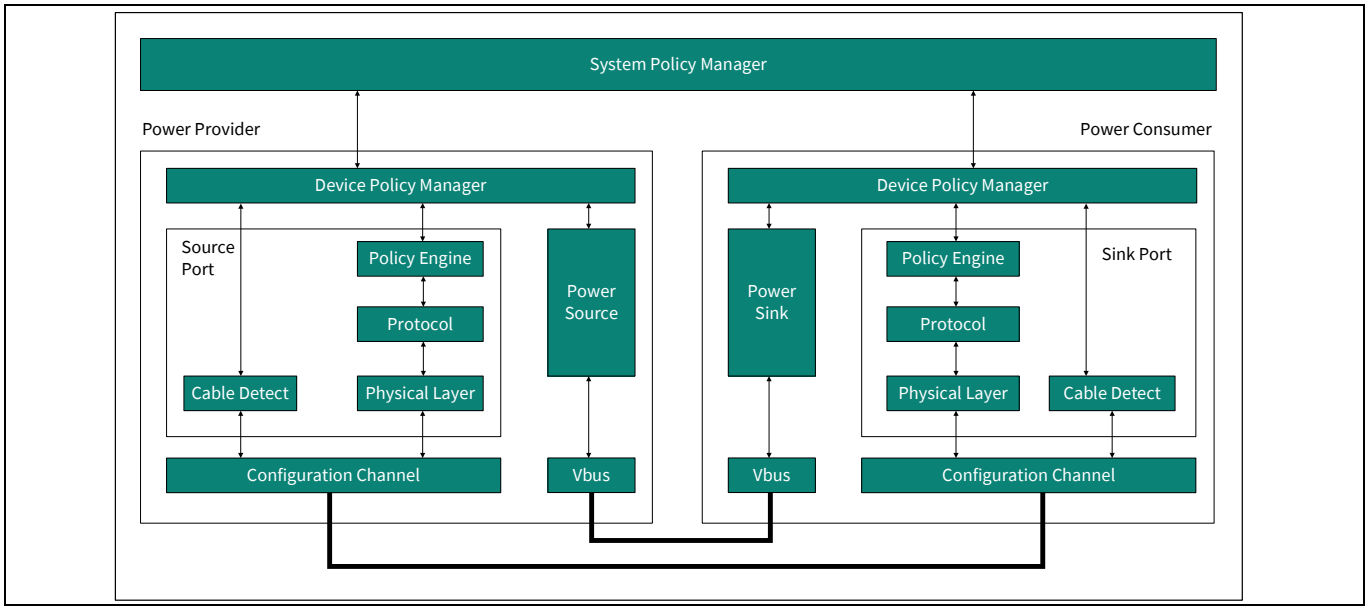

Figure 4 Type-C and PD architecture for dual-role power applications

- **System policy manager:** The PD specification defines a system policy manager that is implemented on the USB host running as an operating system stack. For more details on system policy, see the PD specification.
- **Device policy manager:** The device policy manager is the module running in the power provider or power consumer, which applies a local policy to each port in the device via the policy engine.
- **Source port:** The source port is the power provider port, which supplies power over V_{BUS}. It is, by default, a USB port on the host or hub.
- **Sink port:** The sink port is the USB power consumer port, which consumes power over V_{BUS}. It is, by default, a USB port on a device.
- **Policy engine:** The policy engine interprets the device policy manager's input to implement the policy for the port. It also directs the protocol layer to send messages.
- **Protocol:** The protocol layer creates the messages for communication between port partners.
- **Physical layer:** The physical layer sends and receives messages over either V_{BUS} or the configuration channel (CC) between port pairs.

- **Power source:** The ability of a PD port to source power over V_{BUS}. This refers to a Type-C port with R_P asserted on CC.
- **Power sink:** The ability of a PD port to sink power from V_{BUS}. This refers to a Type-C port with R_d asserted on CC.
- **Cable detection module:** The cable detection module detects the presence of an electronically marked cable assembly (EMCA) cable attached to a Type-C port.

The dual-role devices can be developed by combining both the provider and the consumer elements in a single device.

When a USB host and USB device are interconnected, they form a USB link pair, and each link partner has a configuration channel (CC) controller. The messages are then logically exchanged among device policy managers within each PD controller. These messages are physically transferred over the CC, a PD contract is setup between the link pair, and then power is delivered over V_{BUS}.

3.1 Type-C signal definition

Figure 5 shows the USB Type-C receptacle, plug, and flipped-plug signals. Table 1, Figure 6, and Table 2 show the signals used on the USB Type-C receptacle and plug.

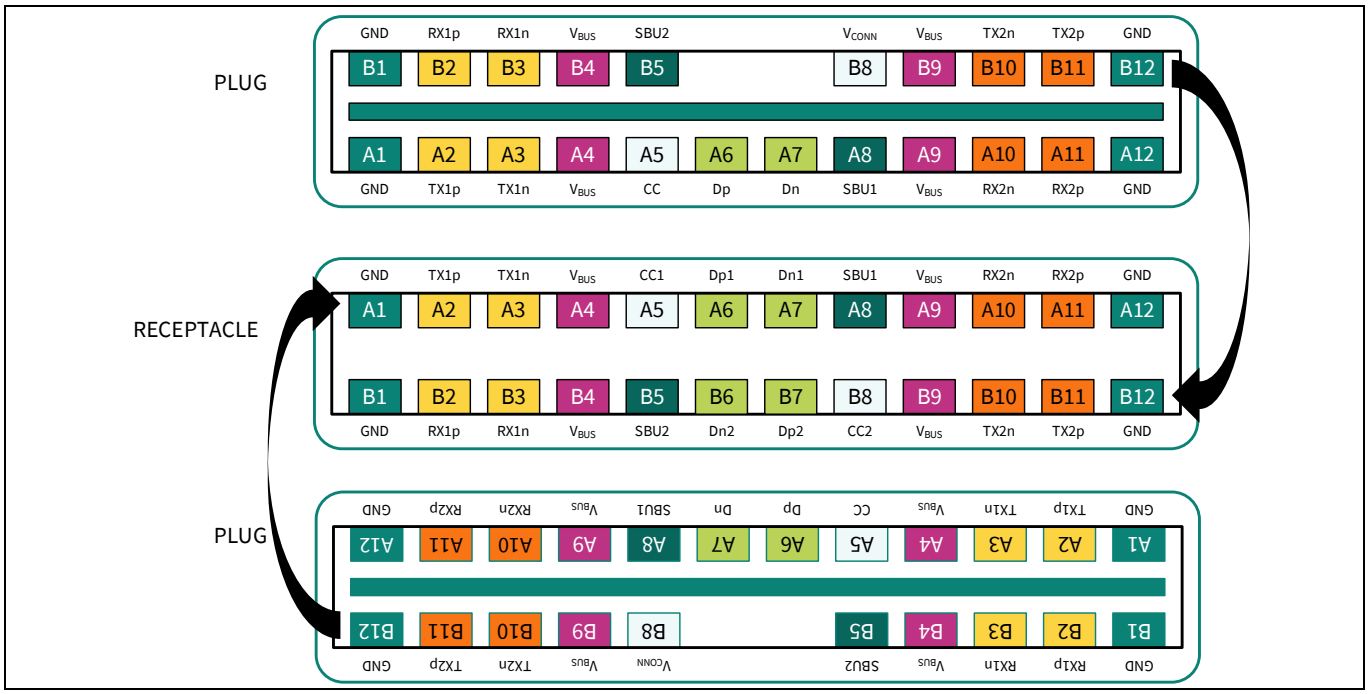

Figure 5 USB Type-C plug, receptacle, and flipped-plug signals (source: USB PD Specification 3.1)

Table 1 USB Type-C receptacle signals

Signal group	Signal	Description
USB 3.1	TX1p, TX1n, RX1p, RX1n, TX2p, TX2n, RX2p, RX2n	The USB 5 Gbps serial data interface defines differential transmit and receive pairs. Two pairs of USB 5 Gbps signal pins are defined to enable the plug-flipping feature on a USB Type-C receptacle.
USB 2.0	Dp1, Dn1 Dp2, Dn2	The USB 2.0 serial data interface defines a differential pair. Two sets of USB 2.0 signal pins are defined to enable plug-flipping on a USB Type-C receptacle.
Configuration channel	CC1, CC2	The CC in the receptacle detects the signal orientation and channel configuration.
Auxiliary signals	SBU1, SBU2	Sideband use. See the USB Type-C Cable and Connector Specification Revision 1.3 for more details.
Power	V_{BUS}	USB cable bus power
	GND	USB cable return current path

Table 2 USB Type-C plug signals

Signal group	Signal	Description
USB 3.1	TX1p, TX1n RX1p, RX1n TX2p, TX2n RX2p, RX2n	The USB 5 Gbps serial data interface defines differential transmit and receive pairs. Two pairs of USB 5 Gbps signal pins are defined to enable the plug-flipping feature on a USB Type-C plug
USB 2.0	D_P, D_N	The USB 2.0 serial data interface defines differential pair on a USB Type-C plug
Configuration channel	CC	The CC in the plug is used for connection detection and interface configuration
Auxiliary signals	SBU1, SBU2	Sideband use. See the USB Type-C Cable and Connector Specification Revision 1.3 for more details
Power	V_{BUS}	USB cable bus power
	V_{CONN}	Type-C cable plug power
	GND	USB cable return current path

As shown in Figure 5, the USB Type-C receptacle has USB 3.1 (Tx and Rx pairs) and USB 2.0 (Dp and Dn) data buses, USB power (V_{BUS}), ground (GND), CC signals (CC1 and CC2), and two sideband use (SBU) signal pins. As listed in Table 1 and Table 2, the descriptions of the USB Type-C plug and receptacle signals are the same, except for the CC and V_{CONN} signals. The two sets of USB 2.0 and USB 3.1 signal locations in this layout facilitate the mapping of the USB signals independent of the plug orientation in the receptacle.

When a cable with the Type-C plug is inserted into the receptacle, one CC pin is used to establish signal orientation, and the other CC pin is repurposed as V_{CONN} for powering the electronics in the USB Type-C cable (plug).

3.2 Type-C ports

3.2.1 Downstream facing port and upstream facing port

A Type-C downstream facing port (DFP) is a USB host and a power source by default, whereas a Type-C upstream facing port (UFP) is a USB device and a power sink by default. A DFP exposes R_P terminations on its CC pins (CC1 and CC2), while a UFP exposes Rd terminations on its CC pin, as shown in Figure 6.

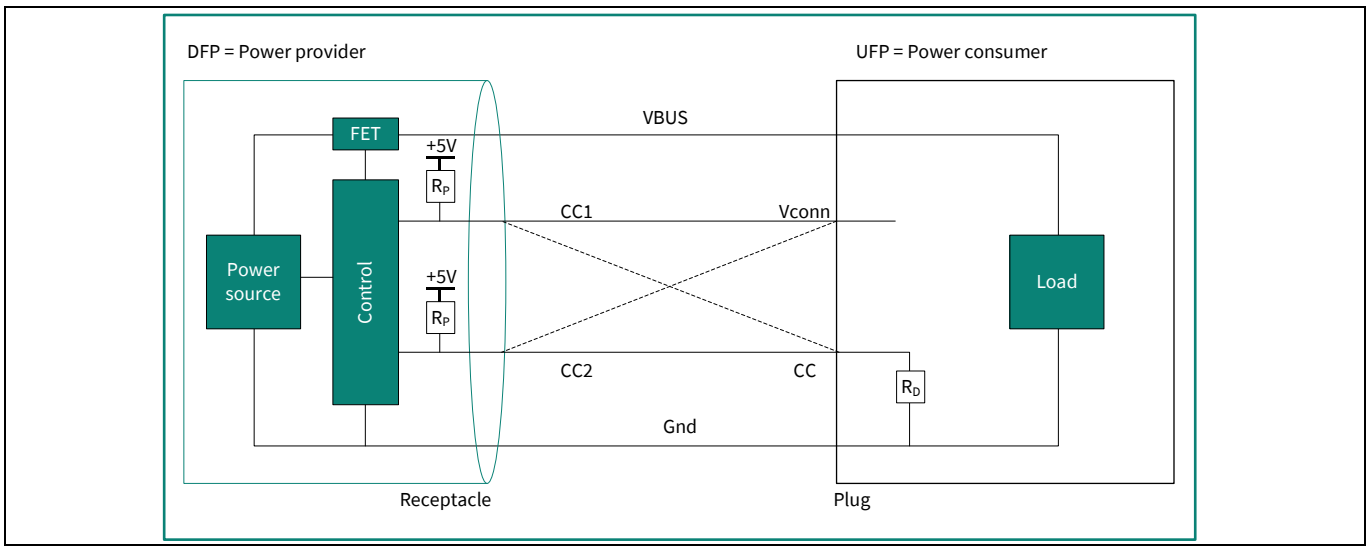

Figure 6 Direct connection of a downstream facing port and upstream facing port

DFPs, specifically those associated with the flow of data in a USB connection are typically the USB ports on a host such as a PC or a HUB. In its default state, the DFP sources V_{BUS} and V_{CONN}. On the other hand, UFP sinks V_{BUS}.

3.2.2 USB PD dual-role power

PD-enabled USB products (such as a notebook with a Type-C port) operate as power providers and consumers. The USB PD specification refers to such a USB Type-C port as dual-role power (DRP).

The DRP devices detect the presence of the R_P and R_D resistors on the CC lines. A typical DRP device can perform the roles listed in Table 3.

Table 3 Roles of a DRP device

No.	Data port role (USB host or device)	Power port role (Power provider or power consumer)
1	DFP	Source (power provider; connect R_P and disconnect R_D)
2	DFP	Sink (power consumer; disconnect R_P and connect R_D)
3	UFP	Source (power provider; connect R_P and disconnect R_D)
4	UFP	Sink (power consumer; disconnect R_P and connect R_D)

4 EVAL_PMG1_B1_DRP kit requirements and features

In this hardware design user guide, EVAL_PMG1-B1 _ DRP kit is taken as a use case to elaborate the design guidelines for EZ-PD™ PMG1-B1 in cordless power tool chargers, wireless speakers, and portable electronics charging applications (sink applications).

4.1 System description

This EVAL_PMG1_B1_DRP kit board provides a USB PD charger solution for cordless power tool battery packs and cordless power tool charger features of the EZ-PD™ PMG1-B1 USB Type-C controller with PD and buck-boost controller. It is designed to operate from a 5-V to 20-V USB PD Type-C as the input and supports charging a 2-5-cell lithium-ion battery pack. The solution board can work in source mode to support the USB PD Type-C source application, where the connector J11(to which power supply is connected) will act as input and provides PDOs of 5.0 V/3.0 A and 9.0 V/3.0 A.

4.2 Detailed feature list – sink application

- Highly integrated single-port USB Type-C PD controller-based solution
- Supports DRP applications
- Charging operation for 2-5-cell lithium-ion battery pack
- Supports the latest USB Type-C and PD specifications, and is targeted for applications such as cordless power tools, wireless speakers, and portable electronics as applications
- Programmable constant voltage (CV) and constant current (CC) settings for charger
- Configurable inductor current limit protection
- Nominal switching frequency of 400 kHz
- Supports dead battery mode
- Comprehensive power path management and protection
- 12-bit ADC for battery pack parameters measurement
- USB PD
  - Supports one USB PD port
  - Supports the latest USB PD 3.1 specification
- Type-C
  - Configurable resistors R_P and R_D
  - V_{BUS} NFET gate driver
  - Integrated 100-mW V_{CONN} power supply and control
- Power output protections
  - Battery pack overvoltage protection (OVP)
  - Battery pack undervoltage protection (UVP)
  - Battery pack overcurrent protection (OCP)
  - Battery pack over-temperature protection (OTP)
  - Board over-temperature protection (NTC0, NTC1)

- Other power protections
  - VBUS to CC short-circuit protection
  - VBUS overvoltage protection (OVP)
  - VBUS undervoltage protection (UVP)
  - Inductor current limit protection (ILIM)
  - Reverse current protection (RCP)
- Legacy charging support
  - USB BC 1.2
  - 2.4 A Apple Charging

4.3 Enable/disable the buck converter

4.4 Detailed feature list – source application

- 27-W buck converter (source application)
  - Provides controlled fixed PDO's 5.0 V/3.0 A and 9.0 V/3.0 A
  - Supports the latest USB PD 3.1
  - Built-in overcurrent protection (OCP)
  - VBAT overvoltage protection (OVP)

4.5 Operating conditions and characteristics

Table 4 Operating conditions and characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input voltage	V_{BUS}	Full performance – meets all PDO specifications	5.0	-	20	V
Output voltage range	V_{BAT}	Rated load I_{BAT}	6.0	-	21.0	V
Output current range	I_{BAT}	Based on the input and output voltages	0	-	6.0	A
Switching frequency	F_{SW}	Full load (with 5% spread spectrum)	380	400	420	kHz
Battery power	P_{BAT}	–	-	-	95	W

4.5.1 Power throttling based on temperature

In temperature-based power throttling, the power budget that is available to charge the battery pack depends on the measured temperature values. There are two NTC thermistors on the board; NTC0 is mounted close to the USB Type-C connector and NTC1 is mounted close to the boost converter MOSFET or inductor. Lithium-ion battery packs have an option to measure the internal battery pack temperature and must react to the conditions described in Table 7.

Use the configuration table to set the sensor's temperature settings for power throttling. The sensor can be enabled or disabled by setting the value of the sensor control parameter. Once the sensor is enabled, the required temperature thresholds can be set by changing the value against the operating condition threshold parameters in the configuration table.

PMG1-B1 keeps monitoring the thermistor temperature ranges and the operating conditions are shown in Table 5 for NTC 0. Note that for the different ranges when the temperature is rising and falling, a 10°C hysteresis must be implemented.

Table 5 Operating conditions for NTC 0 mounted close to the USB Type-C connector

Temperature set point thermistor	Operating condition	Power	Temperature set point translation
T < 70°C (rising) T < 60°C (falling)	T < T1	I1 – Battery pack max. charger current or max. current based on the PD contract (whichever is lower)	The battery pack will charge at I1 for a temperature range of 70°C or below
70°C ≤ T < 85°C (rising) 60°C ≤ T < 75°C (falling)	T1 ≤ T < T2	I2 – 2 A, if the above condition results in a current greater than 2 A; else the current would be I1/2.	The battery pack will charge at I2 for a temperature range of 70°C to 85°C
T ≥ 85°C (rising) T ≥ 75°C (falling)	T ≥ T2	Disable charging	Disable the battery pack charging at a temperature greater than or equal to 85°C

The thermistor temperature ranges, and operating conditions being monitored by PMG1-B1 are shown in Table 6 for NTC 1. Note that for the different ranges when the temperature is rising and falling, a 10°C hysteresis must be implemented.

Table 6 Operating conditions for NTC 1 mounted close to the boost FETs and inductor

Temperature set point thermistor	Operating condition	Power	Temperature set point translation
T < 85°C (rising) T < 75°C (falling)	T < T1	I1 - Battery pack max. charger current or max. current based on the PD contract (whichever is lower)	The battery pack will charge at I1 for a temperature range of 85°C or below
85°C ≤ T < 100°C (rising) 75°C ≤ T < 90°C (falling)	T1 ≤ T < T2	I2 - 2 A, if the above condition results in a current greater than 2 A; else the current would be I1/2.	The battery pack will charge at I2 for a temperature range of 85°C to 100°C
T ≥ 100°C (rising) T ≥ 90°C (falling)	T ≥ T2	Disable charging	Disable the battery pack charging at a temperature greater than or equal to 100°C

The battery built-in thermistor temperature ranges and operating conditions being monitored by EZ-PD™ PMG1-B1 are shown in Table 7. Note that for the different ranges when the temperature is rising and falling, a 5°C hysteresis must be implemented.

Table 7 Operating conditions for built-in battery pack temperature sensor

Thermistor reading	Operating condition	Charging	Temperature set point translation
T < 10°C (rising) T < 5°C (falling)	T < T1	Disable charging	The battery pack charging shall be disabled at a temperature less than or equal to 5°C
10°C ≤ T < 20°C (rising) 5°C ≤ T < 15°C (falling)	T1 ≤ T < T2	1 A fixed current	The battery pack will charge at 1 A for a temperature range higher than 10°C and below 20°C
20°C ≤ T < 50°C (rising) 15°C ≤ T < 45°C (falling)	T2 ≤ T < T3	I1 - Battery max. charger current or max. current based on PD contract (whichever is lower)	The battery pack will charge at I1 for a temperature range of 50°C or lower
T ≥ 50°C (rising) T ≥ 45°C (falling)	T ≥ T3	Disable charging	Disable the battery pack charging at a temperature greater than or equal to 50°C

5 Hardware design for the buck-boost converter

In the given range of the input voltage, the choice of converter topology needs to provide a stable output voltage. From the application specifications, the input voltage can be either higher or lower than the required output voltage. The four-switch buck-boost converter topology provides step-up and step-down voltages seamlessly without inverting the polarity of the output voltage with respect to the input voltage. The solution board hardware components were chosen to meet the Type-C USB PD standards.

5.1 Key specifications

- Input voltage range (V_{BUS}): +5.0 V to +20 V
- Output voltage range: +6 V to +21 V
- Topology: Four-switch buck-boost converter (FSBBC)
- Control method: Peak current mode controlled (PCMC)
- Compensator: Type 2 compensator
- Programmable constant current mode

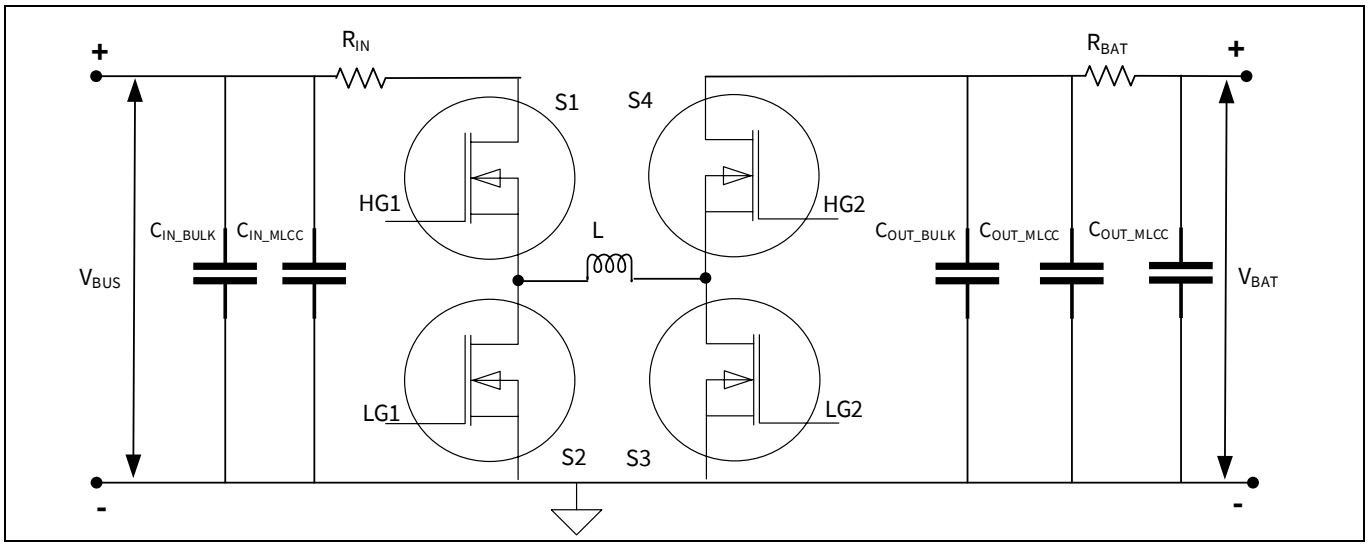

Figure 7 Simplified topology of four-switch buck-boost converter

5.2 Input capacitor selection

The function of the input multilayer ceramic capacitors (MLCC) is to reduce the ripple voltage amplitude on the input line; this in turn reduces the RMS ripple current handled by input bulk capacitors. Additionally, these reduce the switching noise on the input lines, thereby reducing the conducted electromagnetic interference (EMI). The input capacitor bank comprises a combination of ceramic and electrolytic capacitors. The ceramic capacitors are used to bring down the effective series resistance (ESR) of the capacitor bank, because ceramics offer extremely LOW ESR and limit the input voltage switching ripple. The bulk electrolytic capacitors supports the change in the line current during load transients.

When the converter operates in Buck mode, the series switch (S1) as shown in Figure 7 causes a pulsating ripple current with high di/dt at the input. In the absence of input filter capacitors, DC resistance of printed circuit boards and the parasitic inductance generates a large voltage ripple at the input. Input filter capacitors provide a short and low-impedance path for the ripple current, which reduces the conducted and radiated EMI, and provides stability to the line voltage during input voltage fluctuations. Note that pulsating input current waves have high RMS values, which cause significant heating and high harmonic content, resulting in EMI.

In an application, a good practice is maintain the input voltage ripple lower than ±5 percent to ±10 percent of the input voltage. The input voltage peak-to-peak ripple produced by the input capacitor is equal to the input capacitor ESR multiplied by the capacitor's RMS current.

The chosen input capacitor's current ratings should be equal to or greater than the RMS capacitor current I_{Cin_rms} ; its voltage rating is 40 to 50 percent higher than the maximum applied input voltage.

5.2.1 Input capacitor RMS current – buck mode

The RMS current of the input capacitor in buck mode is as follows:

$$I_{C_{IN\_RMS}} = \sqrt{\frac{1}{T}\int_0^T I_{C_{IN}}^2 \, dt}$$

The input capacitor current, when switch S1 ON is ($I_{BUS} - I_L$) and when switch S1 OFF is I_{BUS}, then $I_{C_{IN\_RMS}}$ can be written as follows:

$$I_{C_{IN\_RMS}} = \sqrt{\frac{1}{T}\left(\int_0^{DT} (I_{BUS} - I_L)^2 \, dt + \right) + \int_{DT}^{T} (I_{BUS})^2 \, dt}$$

By neglecting the inductor ripple current (ΔI_L) in a buck converter ($I_L = I_{BAT}$) and using the relation ($I_{BUS} = D*I_{BAT}$)x, the RMS current of the input capacitor in buck mode is:

$$I_{C_{IN\_RMS}} = I_{BAT}\sqrt{D(1-D)}$$

where,

I_L = Inductor current

I_{BAT} = Charging current

Duty cycle of a buck converter

$$D = \frac{V_{BAT}}{V_{BUS} * \zeta}$$

ζ = Efficiency of the power converter

5.2.2 Input ceramic capacitor selection – buck mode

The current flowing through the input capacitor ($I_{C_{IN\_RMS}}$) is the difference between input current (I_{BUS}), inductor current (I_L) during the switch S1 ON-state, and only the input current (I_{BUS}) during the switch S1 OFF-state. From this operation, during the switch S1 OFF-state, the input capacitors (C_{IN}) get charged with input current (I_{BUS}); during the switch S1 ON-state, the input capacitor (C_{IN}) gets discharged. In steady-state, the input capacitors' added and removed charge are equal (i.e., capacitor amp-second balance). The input voltage ripple ΔV_{BUS_PK-PK} goes from its minimum to maximum value during the S1 OFF-state (the charging period).

It is known that,

$$I_{BUS} = C\frac{dV_{BUS}}{dt} = \frac{C\Delta V_{BUS}}{T_{OFF}}; \qquad \text{in buck converter } I_{BUS} = D\ I_{BAT} \text{ and } T_{OFF} = (1-D)\ T_{sw}$$

The input MLCC value to meet the input voltage ripple requirement in buck mode is

$$C_{IN\_MLCC} \gg = \frac{D\ (1-D)\ I_{BAT\_MAX}}{\Delta V_{BUS_{PK-PK}} * F_{SW}}$$

where,

$\Delta V_{BUS\_PK\_PK}$ = Allowed maximum peak-to-peak input voltage ripple

T_{SW} = Operating switching period of the converter

I_{BAT_MAX} = Rated maximum output current

The loss due to the input capacitors ESR is

$$P_{C_{IN}} = I^2_{C_{IN\_RMS}} * R_{C_{IN\_MLCC}}$$

where,

'$R_{C_{IN\_MLCC}}$' = The input MLCC network's total equivalent series resistance

5.2.3 Input bulk capacitor selection – buck mode

The input supply lines are typically incapable of providing the required input current quickly enough for the converter to respond to a fast-transient load current. The input bulk capacitor provides the energy necessary to source current to the buck supply until the host supply can fill the demand. The choice of the input bulk capacitor should meet the allowable ripple current requirement and overshoot and undershoot specifications due to load transients.

The ESR of the input bulk capacitor ($R_{C_{IN\_BULK}}$) and the capacitance (C_{IN_BULK}) must meet the transient response requirement.

ESR of the input bulk capacitor is

$$R_{C_{IN\_BULK}} \ll 0.5\left(\frac{V_{BUS\_TRANSIENT}}{I_{BAT\_STEP} * D_{BUCK\_MAX}}\right)$$

where,

$V_{BUS\_TRANSIENT}$ = Allowed input voltage transient undershoot or overshoot due to output load current transients

I_{BAT_STEP} = Allowed change in output load/charge current

D_{BUCK_MAX} = Maximum duty cycle in buck mode

The capacitance of the input bulk capacitor to meet the output load transients is

$$C_{IN\_BULK} \gg \frac{D_{BUCK} * I_{BAT\_STEP}}{2 * \pi * F_{BW} * V_{BUS\_TRANSIENT}}$$

where,

F_{BW} = Bandwidth of the connected source

D_{BUCK} = Duty cycle in buck mode

Input voltage transient undershoot/overshoot due to load step is

$$V_{BUS\_TRANSIENT} = \frac{I_{BAT\_STEP} * D_{BUCK}}{2 * \pi * F_{BW} * (C_{IN\_BULK} + C_{IN\_MLCC})} + I_{BAT\_STEP} * D_{BUCK} * (R_{C_{IN\_BULK}})$$

Input voltage ripple is

$$V_{IN\_RIPPLE} = \frac{I_{BAT} * D_{BUCK} * (1 - D_{BUCK})}{F_{SW} * (C_{IN\_BULK} + C_{IN\_MLCC})} + I_{BAT\_MAX} * D_{BUCK} * (R_{C_{IN\_MLCC}})$$

5.2.4 Input capacitor RMS current – boost mode

When the converter operates in boost mode, connect the boost inductor (L) to the input to reduce the capacitance and to reduce the RMS currents in the input capacitors.

The RMS current ($I_{C_{IN\_RMS}}$) of the input capacitor in boost mode is

$$I_{C_{IN\_RMS}} = \frac{\Delta I_L}{\sqrt{12}} \cong 0.3\ \Delta I_L$$

where ΔI_L = Power inductor peak-to-peak ripple current (continuous conduction mode)

5.2.5 Input bulk capacitor selection – boost mode

The capacitance of the input bulk capacitor to meet the output load transients is

$$C_{IN\_BULK} \gg \frac{D_{BOOST} * I_{BAT\_STEP}}{2 * \pi * F_{BW} * V_{BUS\_TRANSIENT}}$$

5.3 Power inductor selection

The chosen power inductor value must satisfy both buck and boost mode conditions. The lower the inductor value, the smaller the size. However, it results in a higher peak current.

5.3.1 Power inductor value – buck mode

The basic inductor current and voltage relation can be written as $V_L = L\frac{dI_L}{dt}$. In a buck converter, the change in the inductor current during the switch S1 ON-time is equal to the change in current during the switch S1 OFF-time. The change in the inductor current (I_L) during the switch S1 ON-time can be written as $\frac{\Delta I_L}{DT_{sw}}$.

$$L_{BUCK} = \frac{(V_{BUS\_MAX} - V_{BAT}) * D_{BUCK}}{\Delta I_L * F_{SW}}$$

ΔI_L can be fraction (0.2 to 0.4) of the I_{BAT_MAX}

where,

V_{BUS_MAX} = Maximum input voltage

5.3.2 Inductor peak current – buck mode

The maximum current passing through the power inductor in buck mode is

$$I_{L\_MAX\_BUCK} = \frac{\Delta I_L}{2} + I_{BAT\_MAX}$$

Switches S1 and S2 must withstand this peak current.

5.3.3 Inductor RMS current – buck mode

The RMS current passing through the power inductor in buck mode is

$$I_{L\_RMS\_BUCK} = \sqrt{(I_{BAT\_MAX})^2 + \frac{(\Delta I_L)^2}{12}}$$

5.3.4 Power inductor value – boost mode

$$L_{BOOST} = \frac{V_{BUS\_MAX} * D_{BOOST}}{\Delta I_L * F_{SW}}$$

ΔI_L can be fraction (0.2 to 0.4) of the I_{BAT_MAX} multiplied by $\frac{V_{BAT}}{V_{BUSMIN}}$

Note: In a boost converter $I_{BUS} \approx I_L$

$$\Delta I_L = (0.2 \text{ to } 0.4) * I_{BAT\_MAX} * \frac{V_{BAT}}{V_{BUS\_MIN}}$$

where,

boost converter duty cycle $D_{BOOST} = 1 - \frac{(V_{BUS\_MAX} * \zeta)}{V_{BAT}}$

V_{BUS_MAX} = Maximum input voltage

I_{BUS} = Average input current

I_L = Average inductor current

ζ = The efficiency of the converter

5.3.5 Inductor peak current – boost mode

In the boost converter, the average input current I_{BUS} and average inductor current I_L are equal. The peak-to-peak inductor ripple current is $\Delta I_L = D_{BOOST} * \frac{V_{BUS}}{L*F_{SW}}$

The peak inductor current $I_{L\_PK\_BOOST}$ is the sum of the average value of input current + one half of the peak-to-peak inductor ripple current.

The peak current passing through the inductor is

$$I_{L\_PK\_BOOST} = I_{BUS\_AVG} + \frac{\Delta I_L}{2} = \frac{I_{BAT\_MAX}}{(1-D)} + \frac{\Delta I_L}{2}$$

The chosen switches S3 and S4 should withstand this peak current.

Where,

I_{BUS_AVG} = Average input current

5.3.6 Inductor RMS current – boost mode

The RMS current passing through the inductor is

$$I_{L\_RMS\_BOOST} = \sqrt{(I_{BUS\_MAX})^2 + \frac{(\Delta I_L)^2}{12}}$$

5.4 Power switches selection

The voltage rating of the selected power switches should be 1.5 to 2 times the maximum applied input voltage to the converter. The continuous drain current rating should be greater than the computed switch peak current in a converter. The power losses of a converter depend on the chosen MOSFET characteristics like drain-source on-state resistance (R_{ds_ON}), rise time (T_R), fall time (T_F), total gate charge (Q_g), MOSFET diode reverse recovery charge (Q_{rr}), and switching frequency (F_{sw}) of the converter. The efficiency of the converter depends heavily on the chosen power MOSFETs. Therefore, a few basic empirical formulas are provided in the following sections.

5.4.1 Power MOSFET selection – buck mode

When the switch (S1) is turned ON, the current passed through the switch I_{S1} is the current drawn from the input line. The switch RMS current $I_{S1\_RMS\_ON}$ is

$$I_{S1\_RMS\_ON} = \sqrt{\left(I_{BAT}^2 + \frac{\Delta I_L^2}{12}\right)(D_{BUCK})}$$

When the switch (S2) is turned ON, the current passed through the switch RMS current $I_{S2\_RMS\_ON}$ is

$$I_{S2\_RMS\_ON} = \sqrt{\left(I_{BAT}^2 + \frac{\Delta I_L^2}{12}\right)(1 - D_{BUCK})}$$

5.4.2 Power MOSFET selection – boost mode

When the switch (S3) is turned ON, the current passed through the switch I_{S3} is the current drawn from the input line.

The switch RMS current $I_{S3\_rms\_ON}$ is

$$I_{S3_{rms_{ON}}} = \sqrt{\frac{1}{T_{sw}}\int_0^{DT_{sw}} I_s^2\, dt} = \sqrt{\frac{1}{T_{sw}}\int_0^{DT_{sw}} \left(\frac{I_{BAT}}{1 - D_{BOOST}}\right)^2 dt} = \frac{I_{BAT}}{1 - D_{BOOST}}\sqrt{\frac{1}{T_{sw}}\int_0^{DT_{sw}} dt}$$

$$= \frac{I_{BAT}}{1 - D_{BOOST}}\sqrt{\frac{1}{T_{sw}} D_{BOOST} T_{sw}}$$

$$= \sqrt{\left(\left(\frac{I_{BAT}}{1 - D_{BOOST}}\right)^2 + \frac{\Delta I_L^2}{12}\right)(D_{BOOST})}$$

When the switch (S4) is turned ON, the current passed through the switch RMS current $I_{S4\_rms\_ON}$ is:

$$I_{S4\_RMS\_ON} = \sqrt{\left(\left(\frac{I_{BAT}}{1 - D_{BOOST}}\right)^2 + \frac{\Delta I_L^2}{12}\right)(1 - D_{BOOST})}$$

5.4.3 Power MOSFET losses – buck mode

In a synchronous buck converter, power MOSFET losses can be conduction losses, switching losses, body diode reverse recovery losses, dead time losses, and gate charge losses. The empirical formulas for each of the losses are given for S1 and S2 separately.

Conduction losses in switch (S1): $\left(I_{S1\_RMS\_ON}\right)^2 * R_{ds\_ON}$

Switching losses in switch (S1):

$$V_{BUS} * \left(I_{BAT} - \frac{\Delta I_L}{2}\right) * 0.5 * \left(T_{R\_S1}\right) * F_{SW} + V_{BUS} * \left(I_{BAT} + \frac{\Delta I_L}{2}\right) * 0.5 * \left(T_{F\_S1}\right) * F_{SW}$$

Diode reverse recovery losses $(T_{F\_S1}) = V_{BUS} * Q_{rr} * F_{SW}$

Conduction losses in switch (S2): $\left(I_{S2\_RMS\_ON}\right)^2 * R_{ds\_ON}$

Switching losses in switch (S2):

$$V_{S2DIODE} * \left(I_{BAT} + \frac{\Delta I_L}{2}\right) * 0.5 * \left(T_{R\_S2}\right) * F_{SW} + V_{S2DIODE} * \left(I_{BAT} - \frac{\Delta I_L}{2}\right) * 0.5 * \left(T_{F\_S2}\right) * F_{SW}$$

Dead time and gate charge losses are for both the S1 and S2.

Dead time losses = $2 * V_{S2DIODE} * (I_{BAT}) * (T_{DEADTIME}) * F_{SW}$

MOSFET gate charge losses = $2 * Q_g * F_{SW} * V_{GD}$

where,

$T_{DEADTIME}$ = Dead time between S1 and S2

T_{R_S1} = Rise time of the S1

T_{F_S1} = Fall time of the S1

T_{R_S2} = Rise time of the S2

T_{F_S2} = Fall time of the S2

Q_{rr} = Reverse recovery charge of the switch

R_{ds_ON} = MOSFET drain-source on-state resistance – datasheet parameter

V_{GD} = Gate driving voltage

Q_G = Gate charge

5.4.4 Power MOSFET losses – boost mode

In a synchronous boost converter, power MOSFET losses can be conduction losses, switching losses, body diode reverse recovery losses, dead time losses, and gate chare losses. The empirical formulas for each of the losses are given for S3 and S4 separately.

Conduction losses in switch (S3): $(I_{S3\_RMS\_ON})^2 * R_{ds\_ON}(T)$

Switching losses in switch (S3):

$$V_{BAT} * \left(\frac{I_{BAT}}{(1 - D_{BOOST})} - \frac{\Delta I_L}{2}\right) * 0.5 * (T_{R\_S3}) * F_{SW} + V_{BAT} * \left(\frac{I_{BAT}}{(1 - D_{BOOST})} + \frac{\Delta I_L}{2}\right) * 0.5 * (T_{F\_S3}) * F_{SW}$$

Conduction losses in switch (S4): $(I_{S4\_RMS\_ON})^2 * R_{ds\_ON}$

Switching losses in switch (S4):

$$V_{S4DIODE} * \left(\frac{I_{BAT}}{(1-D_{BOOST})} + \frac{\Delta I_L}{2}\right) * 0.5 * (T_{R\_S4}) * F_{SW} + V_{S4DIDOE} * \left(\frac{I_{BAT}}{(1-D_{BOOST})} - \frac{\Delta I_L}{2}\right) * 0.5 * (T_{F\_S4}) * F_{SW}$$

Diode reverse recovery losses (S4) = $V_{BAT} * F_{SW} * Q_{rr\_S4}$

Dead time and gate charge losses are for both the S3 and S4.

Dead time losses = $2 * V_{S4DIODE} * I_{BAT} * T_{DEADTIME} * F_{SW}$

MOSFET gate charge losses = $2 * Q_g * F_{SW} * V_{gd}$

where,

T_{R_S3} = S3 MOSFET rise time – datasheet parameter

T_{F_S3} = S3 MOSFET fall time – datasheet parameter

T_{R_S4} = S4 MOSFET rise time – datasheet parameter

T_{F_S4} = S4 MOSFET fall time – datasheet parameter

Q_{rr_s4} = MOSFET diode reverse recovery charge – datasheet parameter

Q_g = MOSFET gate charge total – datasheet parameter

V_{GD} = MOSFET gate drive voltage – specified in the controller datasheet

R_{ds_ON} = Drain-source ON-state resistance – datasheet parameter

$T_{DEADTIME}$ = Dead time between S3 and S4

$V_{S4DIODE}$ = High-side switch inverse diode forward voltage

5.5 Output capacitors selection

When there is a change in the load current (load transient), the converter's output feedback control loop senses the change and adjusts the duty cycle of the converter. Typically, in an application, the rate of change in load current is faster than the loop response. Therefore, to support the load transients, add bulk capacitors at the output. To ensure that the output ripple is in the specified limits, add high-frequency bypass capacitors (MLCC) in parallel to the output bulk capacitors.

5.5.1 Output capacitor selection – buck mode

An output capacitor is required to maintain a regulated output voltage while the switch (S1) is OFF and must be able to respond to changes in the load current. It is necessary to minimize the amount of ripple on the output voltage. The output capacitors' maximum ESR can be computed using the specified maximum output voltage ripple (ΔV_{BAT_PK-PK}) and the maximum load current (I_{OUT_MAX}). The maximum ESR of the output capacitors must be lower than the computed $R_{C_{OUT\_MAX}}$ to have an output voltage ripple below the specification value.

$$R_{C_{OUT\_MAX}} = 0.5 * \left(\frac{\Delta V_{BAT\_PK-PK}}{I_{BAT\_MAX}}\right)$$

where,

ΔV_{BAT_PK-PK} = Allowed output voltage ripple. Typically, it is 3 to 5 percent of V_{BAT}.

The output capacitor value in a buck converter to meet the specified ripple requirement is

$$C_{OUT\_MLCC} \gg \frac{\Delta I_L}{8 * F_{SW} * \Delta V_{BAT\_PK-PK}}$$

The output capacitor must be able to handle output current transient requirements.

$$C_{OUT} = \frac{I_{BAT\_STEP}}{\Delta V_{BAT\_TRANSIENT}} * \frac{1}{2 * \pi * F_{BW\_BUCK}}$$

The output voltage ripple equation can be written as

$$\Delta V_{BAT\_PK-PK} = \frac{\Delta I_L}{8 * F_{SW} * C_{OUT\_MLCC}} + \Delta I_L R_{C_{OUT\_MAX}}$$

5.5.2 Output capacitor RMS current – buck mode

The ripple current flowing through the output capacitor in buck mode is

$$I_{C_{OUT\_RMS}} = \sqrt{I^2_{L\_MAX\_BULK} - I^2_{BAT\_MAX}}$$

or

The RMS current in the output capacitor in buck mode is

$$I_{C_{OUT\_RMS}} = \frac{\Delta I_L}{\sqrt{12}} \cong 0.3\Delta I_L$$

Where,

ΔI_L = Power Inductor peak-to-peak ripple current (continuous conduction mode)

5.5.3 Output capacitor selection – boost mode

Output voltage ripple is contributed by the capacitor ESR and charging/discharging of the output capacitor. When the power switch S3 is ON, the output capacitor supports the required load demand; when the power switch (S3) turns OFF, $I_{L_{MAX\_BOOST}}$ flows into the output capacitor causing the change in output voltage $\Delta V_{BAT} = I_{L_{MAX\_BOOST}} \times R_{C_{OUT\_MAX}}$

The output capacitor in a boost converter can be computed by using:

$$C_{OUT\_MLCC} = \frac{I_{BAT\_MAX} * D_{MAX\_BOOST}}{F_{SW} * \Delta V_{BAT}}$$

The maximum ESR of the output capacitor must be lower than the computed $R_{C_{OUT\_MAX}}$ to have an output voltage ripple below the specification value.

$$R_{C_{OUT\_MAX}} \ll \frac{\Delta V_{BAT}}{\frac{I_{BAT\_MAX}}{1 - D_{MAX\_BOOST}} + \frac{\Delta I_L}{2}}$$

Boost converters will have a right half plane (RHP) zero in the control to the output transfer function. Therefore, the total loop bandwidth is limited to one fifth of the RHP zero frequency (F_{RHP_ZERO}).

$$F_{RHP\_ZERO} = \frac{R_{OUT}}{2\pi L_{BOOST}} * (\frac{V_{BUS}}{V_{BAT}})^2 = \frac{V_{BUS}}{I_{BAT} * 2\pi L} * (\frac{V_{BUS}}{V_{BAT}})^2$$

Now, the choice of an output bulk capacitor to meet the load transient requirement is

$$C_{OUT\_BULK} = \frac{I_{BAT\_STEP}}{\Delta V_{BAT\_TRANSIENT}} * \frac{1}{2 * \pi * F_{BW\_BOOST}}$$

where,

I_{BAT_STEP} = Step change of output load

$\Delta V_{BAT\_TRANSIENT}$ = Output voltage variation due to the step change of the output load

Output voltage ripple ΔV_{BAT_RIPPLE} is

$$\Delta V_{BAT\_RIPPLE} = \frac{I_{BAT\_MAX} * D_{MAX\_BOOST}}{F_{SW} * C_{OUT\_BULK}} + (I_{BAT\_MAX} * R_{C_{OUT\_MAX}})$$

5.5.4 Output capacitor RMS current – boost mode

The output capacitor ripple current in boost mode is:

$$I_{C_{OUT\_RMS}} = \sqrt{(I_{BUS} - I_{BAT})^2 * (1 - D_{BOOST}) + I_{BAT}^2 * D_{BOOST}}$$

$$I_{C_{OUT\_RMS}} = I_{BAT} \sqrt{\frac{D_{BOOST}}{(1 - D_{BOOST})}}$$

5.6 Current sense resistor (R_{IN}) selection

The internal high-side current sense amplifiers (CSA) in EZ-PD™ PMG1-B1 measure the peak current (I_{IN}) sensing through an external current sense resistor (R_{IN}) placed in the V_{BUS} path. The drop across R_{IN} applies between the CSPI and CSNI terminals. The choice of an external current sense resistor (R_{IN}) is critical to the control of FSBBC; a small value of R_{IN} provides low power loss and supports the dynamic range required for the measurement.

A minimum of 5 mΩ current sense resistor is required to have a good signal-to-noise ratio (SNR) in the feedback path to measure the input current accurately. EZ-PD™ PMG1-B1 has the programmable CSA gain to amplify the feedback signal. Ensure that the product of CSA gain and (I_{IN}*R_{IN}) is not greater than 1.60 V. A CSA gain setting of 9 is recommended for better signal fidelity.

5.7 Bootstrap circuit design

A bootstrap circuit is used in half-bridge configuration to supply the bias to the high-side MOSFET (S1) because it requires a voltage supply referenced at the source of the high-side MOSFET. The basic circuit elements are C_{BOOT} and D_{BOOT} designed to reliably drive the high-side MOSFET.

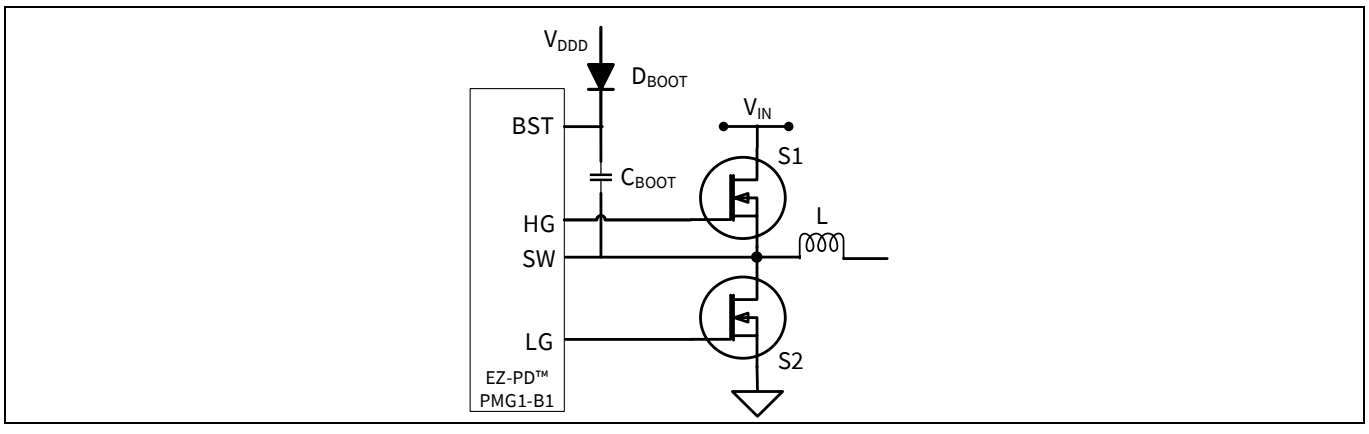

Figure 8 Bootstrap circuit

5.7.1 Bootstrap capacitor (C_{BOOT}) selection

The minimum charge needs to be supplied by the bootstrap capacitor $Q_{BS} = 2 * Q_g$

The bootstrap capacitor must be able to supply this charge and retain its full voltage. If that does not happen, there will be a significant amount of ripple on the V_{BS} voltage (voltage across C_{BOOT}).

$$C_g = \frac{Q_g}{(V_{DDD} - V_{F\_BOOTDIODE})}$$

$$C_{BOOT} \gg 20 * C_g$$

where,

V_{DDD} = Supply voltage

$V_{F\_BOOTDIODE}$ = Forward voltage drop across the bootstrap diode

Q_g = Gate charge of the high-side FET

The chosen bootstrap capacitor (C_{BOOT}) should be able to withstand a minimum of switch node voltage (SW) + V_{DDD} .

5.7.2 Bootstrap diode (D_{Boot}) selection

The bootstrap diode (D_{BOOT}) is required to block the full power rail voltage, which is seen when the high-side MOSFET (S1) is switched ON. It must be a fast recovery diode to minimize the amount of charge fed back from the bootstrap capacitor (C_{BOOT}) into the V_{DDD} supply. Similarly, the high-temperature reverse leakage current is important if the capacitor must store charge for long periods of time. The current rating of the bootstrap diode is the product of the gate charge of the MOSFET and the switching frequency (F_{SW}).

$$I_{DBoot} = Q_g * F_{SW}$$

5.8 Bypass capacitor selection

The choice of bypass capacitors at V_{DDD}, V_{CCD}, and PVDD should meet the values recommended in the EZ-PD™ PMG1-B1 datasheet and the typical values shown in Figure 9. The chosen capacitors should have low ESR to bypass the AC signal present in the DC voltage; typically, it is a combination of high- and low-value capacitors. The high-value capacitors in the range of 4.7 µF to 10 µF suppress the low-frequency noise, while the low-value capacitors in the range of 0.01 µF to 0.1 µF suppress the high-frequency noise.

To absorb the dynamic change of voltages at VBUS_IN_EA, VBUS_C, and VIN, it is recommended to place the capacitor value in the order of 0.1 µF.

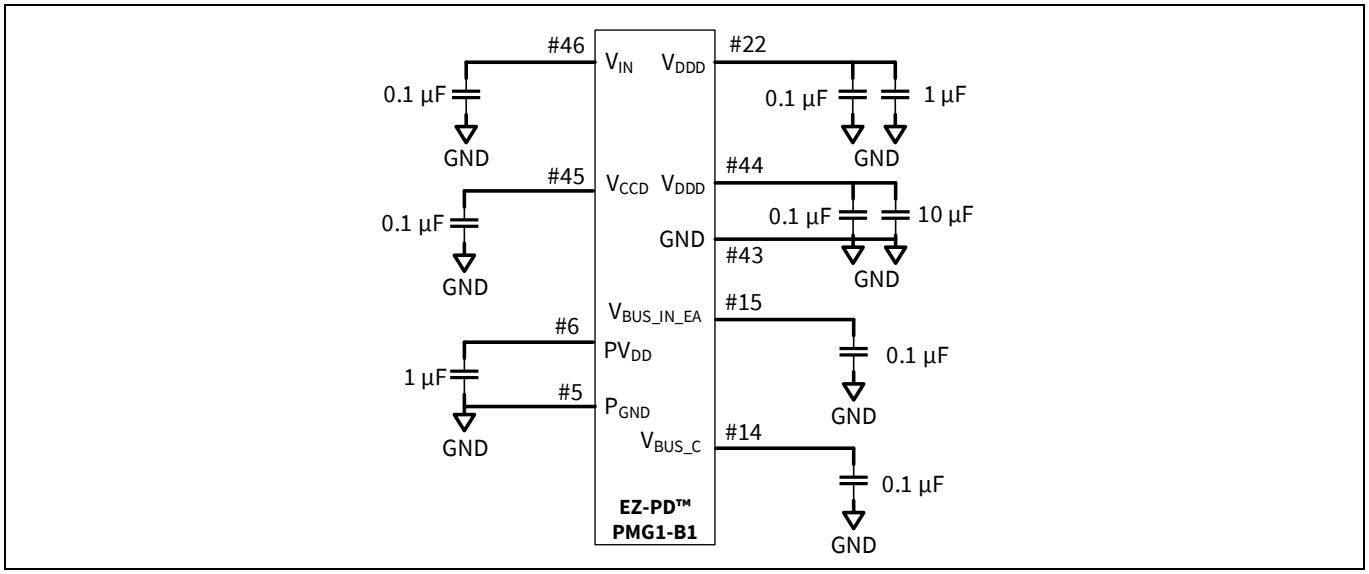

Figure 9 Bypass capacitors

5.9 V_{BUS} discharge

EZ-PD™ PMG1-B1 supports voltage discharge capability on both V_{OUT} and V_{BUS_C} ends. V_{BUS_C} discharge is via #14, and V_{OUT} discharge is via #08 of EZ-PD™ PMG1-B1. The discharge FET and resistors are internal to EZ-PD™ PMG1-B1 and no external components are needed for either of the discharge paths.

Re-attaching the USB Type-C cable enables the V_{BUS_C} and V_{OUT} discharge. The default discharge resistor values are set to 500 Ω on V_{BUS_IN} and 2 kΩ on V_{BUS_C}. Maximum and minimum discharge strength values are software-configurable pre-processor switches.

5.10 CC terminations

PMG1-B1 supports the termination required on the configuration channel line for Type-C PD from the connected source. A 390 pF external capacitor is required on each CC line (CC1 and CC2).

PMG1-B1 also has the required termination on the D+/D- lines to support legacy charging protocols such as BC1.2, Samsung AFC, Apple charging, and Qualcomm charging.

5.11 Dead battery charging

If the battery pack of a power tool application is completely dead, it can be charged by connecting a DFP (such as a power adapter) or DRP devices (such as a monitor or self-powered external hard disk) to its Type-C port.

By default, a DFP or DRP presents an R_P resistor. Upon connection, the CC line on the EZ-PD™ PMG1-B1 device in a power tool charger with a dead battery is pulled HIGH. This turns FET Q2 ON through resistor R1, and the EZ-PD™ PMG1-B1 device (in the power tool charger with the dead battery) presents a dead battery R_D resistor on the CC line (CC1 and CC2), as shown in Figure 10.

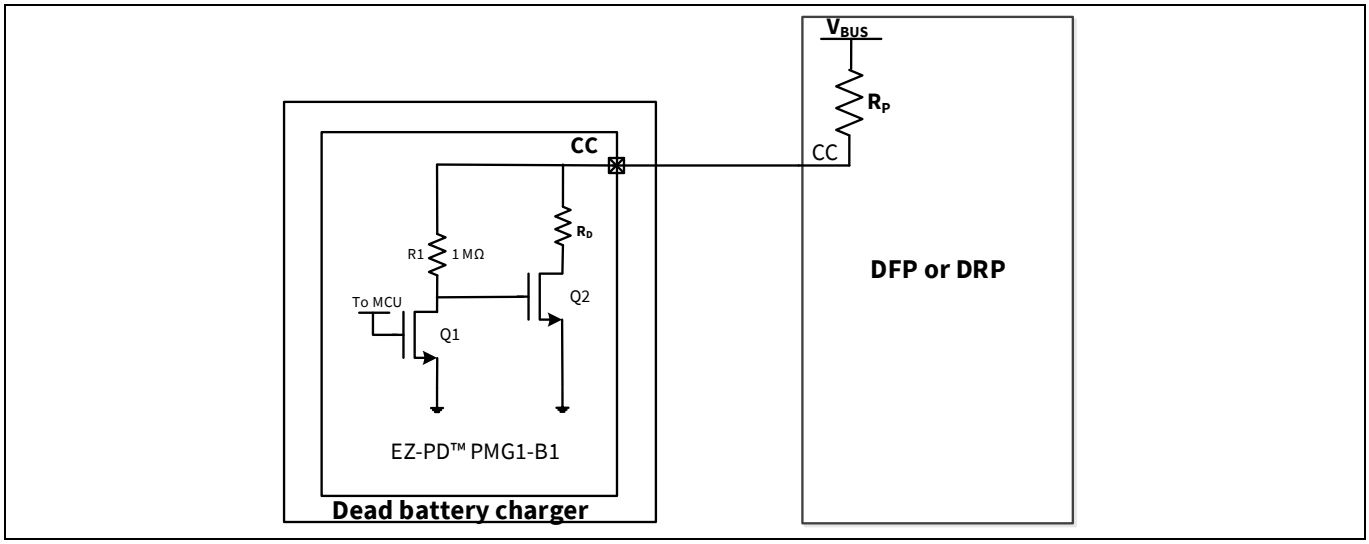

Figure 10 Power tools dead battery charging from a Type-C adapter

By presenting the R_D resistor, a Type-C connection is established between the EZ-PD™ PMG1-B1 (in the power tool charger with the dead battery) and the DFP or DRP. Now, the power tool charger with the dead battery is a power consumer and receives a default 5 V on V_{BUS}, which charges the dead battery. In Figure 10, FET Q1 is turned OFF after the EZ-PD™ PMG1-B1 device is powered. After 5 V is available on V_{BUS}, the EZ-PD™ PMG1-B1 in the power tool charger is powered and starts negotiating with the connected DFP or starts charging the UFP for a higher V_{BUS}, depending on the application configuration.

PMG1-B1 has integrated dead battery termination resistors (R_D) on both CC1 and CC2 lines. CC has an integrated termination resistor (R_D) on the CC2 line and a dedicated RD1 resistor pin that must be shorted with the CC1 line of CC. The dead battery R_D resistors are disabled by the application firmware once the device is powered up. EZ-PD™ PMG1-B1 devices have internal active R_D terminations that are used after the dead battery R_D resistors are disabled.

5.12 Power provider/consumer role

This section explains the recommended external hardware circuits for V_{BUS} control and overvoltage and overcurrent protection in a power tool charger design. A power tool charger design using an EZ-PD™ PMG1-B1 device can act as the following:

- Power provider when running from its internal battery pack
- Power consumer when being charged from a DFP (such as a power adapter) or a DRP (such as a monitor or external, self-powered hard drive).

5.12.1 Consumer and provider path control

The consumer FETs (Q12 and Q13) are connected between the USB Type-C connector and the input to the buck-boost converter. The supported USB Type-C source maximum voltage and currents are seen by the consumer FET (in this application, it is nominal 20 V and 5 A). The chosen back-to-back N-MOSFET common-source configuration should have a low RDSON because this switch is used only to connect or disconnect USB Type-C with the charger. The high-side MOSFET gate drive is provided by the EZ-PD™ PMG1-B1 VBUS_CTRL pin; the chosen FET Gate threshold voltage should be lower than the V_{DDD} of the silicon (5 V). Figure 11 shows the recommended implementation to control the consumer FETs (Q12 and Q13).

The provider FETs (Q5 and Q9) are connected between the output of the buck-boost converter and the battery pack positive terminal. The supported buck-boost converter's maximum output voltage and currents are seen by the provider FETs (in this application, it is nominal 20 V and 6.5 A when a five-cell battery pack is connected). The chosen back-to-back P-MOSFET common-source configuration should have a low $R_{DS(on)}$ because this switch is used only to connect or disconnect the battery pack with the charger. The high-side MOSFET gate drive is controlled with an additional low-side N-MOSFET; the N_MOSFET gate is turned ON/OFF with an PMG1-B1 GPIO. Figure 11 shows the recommended implementation to control the provider FETs (Q5, Q9).

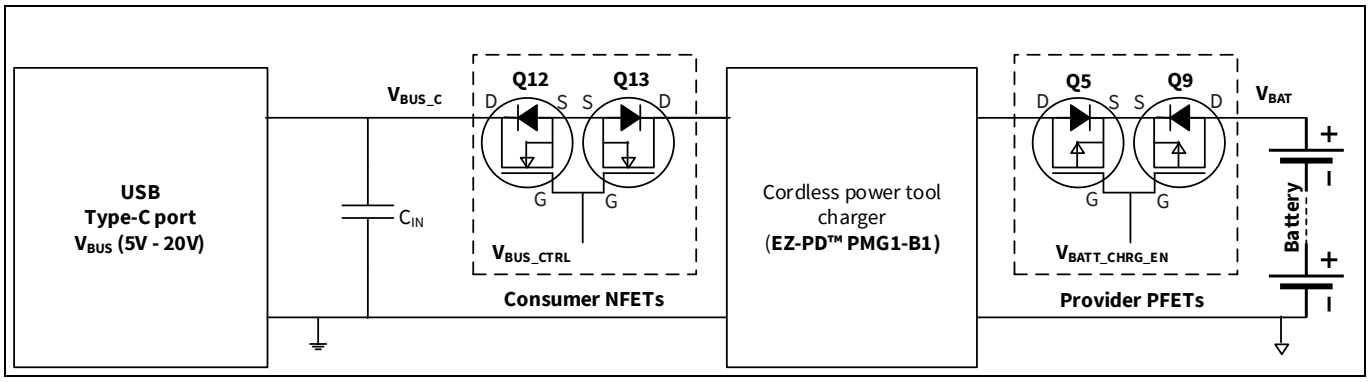

Figure 11 Consumer and provider path control

5.12.2 Selection of consumer MOSFETs

The voltage and current rating of the consumer N-channel MOSFETs (Q12, Q13 can be up to the expected USB Type-C port V_{BUS} voltage and supported current with the required margin.

EZ-PD™ PMG1-B1 devices have an integrated high-voltage gate driver to drive the gate of an external high-side NFET on the V_{BUS} consumer path. The gate driver signal V_{BUS_CTRL} drives the consumer MOSFETs Q12 and Q13 in Figure 11, which control the connection between V_{BUS} and V_{IN}. To turn OFF the external high-side NFET, the gate driver drives the V_{BUS_CTRL} LOW to 0 V. To turn ON the external NFET, the gate driver drives the gate to V_{BUS_C} + 8 V. There is an optional high-side NFET slow turn-ON feature that reduces the high inrush current/spikes at V_{IN} that is the output of the high-side NFET. For a typical gate capacitance of 3 nF, a slow turn-on time of 2 ms to 10 ms can be configured using firmware.

5.12.3 Selection of provider path MOSFETs

The voltage and current rating of the provider path P-channel MOSFETs (Q5, Q9) can be up to the expected battery pack voltage (V_{BAT}) and supported battery pack charging current (I_{BAT}) with the required margin.

The P-channel MOSFETs are driven with external N-channel MOSFET circuit (Q4), which is driven from EZ-PD™ PMG1-B1 as shown in Figure 12. These MOSFETs control the connection between V_{OUT} and V_{BAT}.

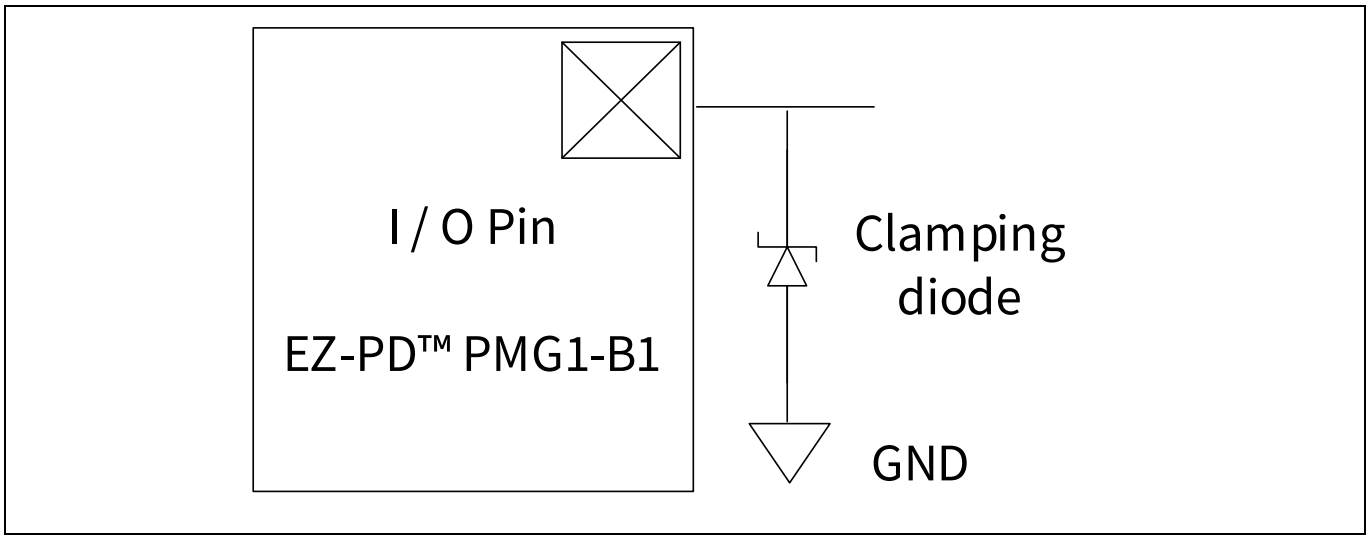

Figure 12 Provider path MOSFETs gate drive control

5.13 Protection diodes

In a highly noisy environment, you need to ensure that signals are clamped to within the power rails specified in the EZ-PD™ PMG1-B1 datasheet table, “pin-based absolute maximum ratings” (see the device datasheet [8]). Adding an external clamp diode prevents the device from exceeding the operating conditions, which enhances the life span and ensures the correct functionality. Choose the clamping diode in such a way that its diode drop falls within the absolute maximum ratings. The diode connectivity is shown in Figure 13.

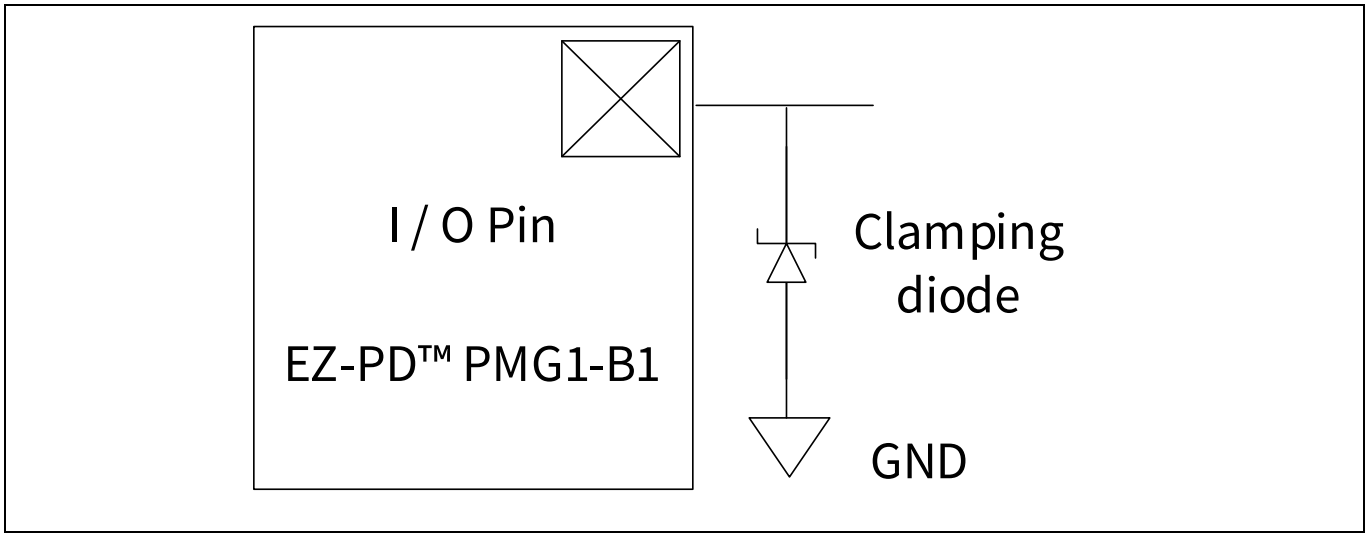

Figure 13 External clamping diodes

5.14 TVS diode selection

The transient voltage suppression (TVS) diode at the input of a system protects the downstream electronic circuits and equipment during a transient overvoltage to immediately conduct and shunt current to the ground, keeping the system voltage exposure to a safe, low-level. However, during normal operation, the TVS diode has no impact. Choose a diode that has a breakdown voltage (VBR) higher than the normal operating voltage. Ensure that the nominal voltage (V_{BUS}) stays below the reverse standoff/reverse working maximum voltage (VRWM), rather than the breakdown voltage (VBR), to ensure very low system leakage.

6 ADC measurements

The PMG1-B1 controller has a built-in 12-bit SAR ADC module used to measure critical parameters such as battery pack voltage, cell voltage, and other battery pack parameters.

The 12-bit 1-Msps SAR ADC operates at a maximum clock rate of 18 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion.

The internal references (1.2 V) from bandgap or VDDA/2 are buffered with the reference buffer. This reference is routed to the Ext V_{REF} / SAR bypass pin (pin #38 in PMG1-B1 controller; see device datasheet [8]), where an external capacitor is used to filter internal noise that may exist on the reference signal (see Reference manual [9]).

Note: The SAR ADC sample rate is limited to 100 ksps (at 12-bit) without an external reference bypass capacitor at pin #38 in the PMG1-B1 controller; see the device datasheet [8]. For example, without a bypass capacitor and with (2 x 1.2) 2.4-V internal VREF, the maximum SAR ADC clock frequency is 1.6 MHz.

The ADC measurement resistive divider network is designed in such a way that the maximum sensed signal voltage (V_{SIGNAL}) with margins should not exceed 2.4 V at V_{AINX}. The combination of C_L and R_L low-pass filter time constant must be defined based on the chosen sampling time of the ADC. It is a recommended practice to keep the filtering capacitors close to the PMG1-B1 controller pins.

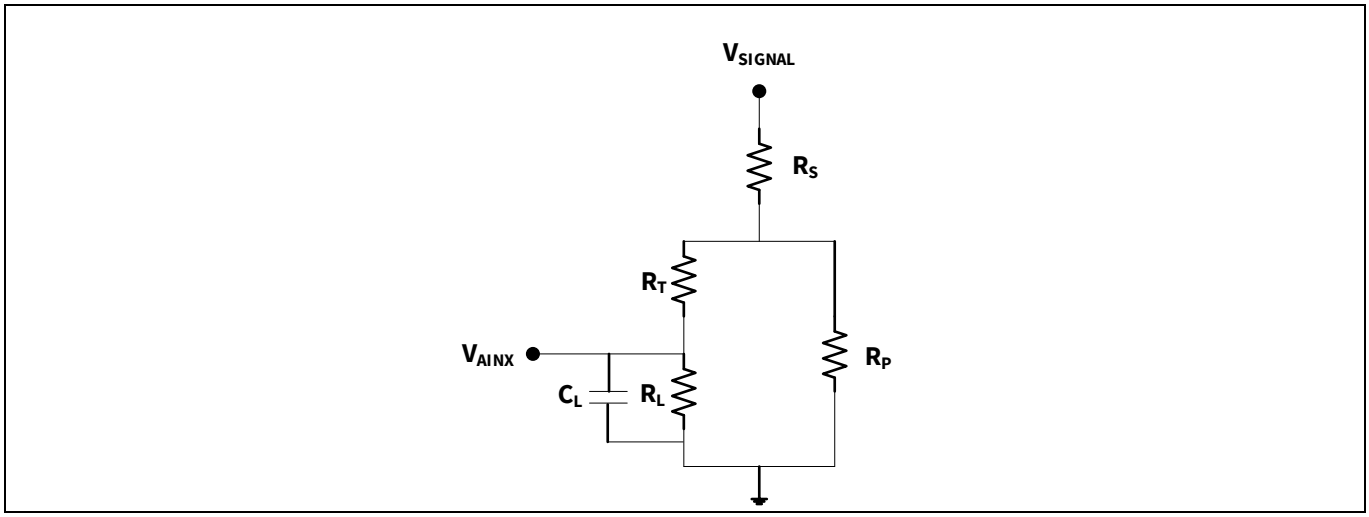

Figure 14 ADC measurement network

$$R_{EQU} = R_S * \left\{\left[1 + \frac{R_T}{R_L}\right] * \left[\frac{1}{R_P} + \frac{1}{R_S} + \frac{1}{R_T}\right] - \left[\frac{1}{R_T}\right]\right\}$$

$$V_{AINX} = \frac{V_{SIGNAL}}{R_{EQU}}$$

The 12-bit PMG1-B1 ADC controllers continuously measure the battery parameters such as battery pack/cell voltages, battery pack temperature, and battery pack ID (battery ID is represented as a voltage value, depending on the battery type). The 8-bit PMG1-B1ADC controllers continuously measure the board temperature with a fixed interval such as 500 ms when the USB PD Type-C source is not connected. However, to

save the battery pack energy, an external N-MOSFET is connected between the signal measurement network and the PMG1-B1 controller ADC measurement pin.

7 Fault protections

EZ-PD™ PMG1-B1 offers integrated fault protection features such as the following:

- Input undervoltage and overvoltage protection
- Output undervoltage and overvoltage protection
- Overcurrent protection (OCP)
- Short-circuit protection (SCP)
- VBUS-to-CC short protection
- Internal temperature protection

This document discusses a few external system-level fault protections also.

7.1 Provides battery pack charger reverse current protection

To prevent the current flow from the battery to the kit board, reverse current protection is provided. Once the reverse current is detected then the controller turns off the HG2 MOSFET which prevents the flow of current from battery to the kit board.

7.2 Input undervoltage and overvoltage (V_{BUS}) protection

PMG1-B1 supports input undervoltage and overvoltage protection when the input voltage is below or above the reliable threshold levels from the connected USB PD Type-C source. It guarantees predictable behavior when PMG1-B1 is up and running.

7.3 Battery pack and individual cells undervoltage and overvoltage protection

PMG1-B1 supports monitoring of battery pack and individual cells undervoltage and overvoltage faults using a 12-bit ADC. After fault detection, the P-channel MOSFETs Q5 and Q9 will be open along with turning off the buck-boost converter. When the converter is operating in charging mode and the battery pack and individual cell levels are falling into the operating range, the converter starts charging the battery pack automatically. When the battery pack is discharging to support the source application, after the undervoltage fault detection of the battery pack, the converter will enter latch mode and recover when the USB PD Type-C cable is detached and attached again. See the ADC measurements section for more recommendations.

7.4 Battery overcurrent protection (OCP)

PMG1-B1 supports monitoring output or battery pack overcurrent and short-circuit faults using the internal comparators. A short-circuit is at a higher threshold as compared to an overcurrent threshold. Response times for short-circuit protection are much faster when compared to overcurrent condition (OC). The external filters on the current-sensing path increase the response time to overcurrent and short-circuit current protections.

7.5 Battery temperature protection

PMG1-B1 supports the measurement of battery pack temperature signals (these signals will be specific to the chosen battery pack) and detection of overtemperature condition to turn off the P-channel MOSFETs Q5, Q9 and the buck-boost converter. Once the measured battery pack temperature signal falls within the configured safe operating limit, the converter starts charging the battery pack automatically in charging mode and starts discharging the battery pack in source application.

Based on the measurement of the battery pack temperature, the charging and discharging current levels are controlled to safeguard the battery pack. The temperature limits can be adjusted based on the battery pack characteristics and default values that are tabulated in Table 7.

7.6 External thermistor overtemperature protection

The temperature of power circuit components in the vicinity of the USB PD Type-C connector and boost converter circuit is measured with a negative temperature coefficient (NTC) thermistor. Being an NTC thermistor, the resistance falls as the temperature increases; the voltage drop across the thermistor is measured to protect the circuit by turning OFF the PWM to the power switching MOSFETs. The temperature thresholds can be adjusted based on a series resistor connected to the NTC thermistor. These characteristics can be obtained from the NTC thermistor datasheets. Select an NTC thermistor and resistor (R) value such that the voltage is linear in the desired temperature region.

NTC 0 is terminated at PMG1-B1 pin #23 and senses the temperature close to the USB Type-C connector. NTC 1 is terminated at EZ-PD™ PMG1-B1 pin #24 and senses the temperature close to the boost MOSFET. If the measured temperature exceeds the operating conditions, the DUT enters overtemperature protection mode.

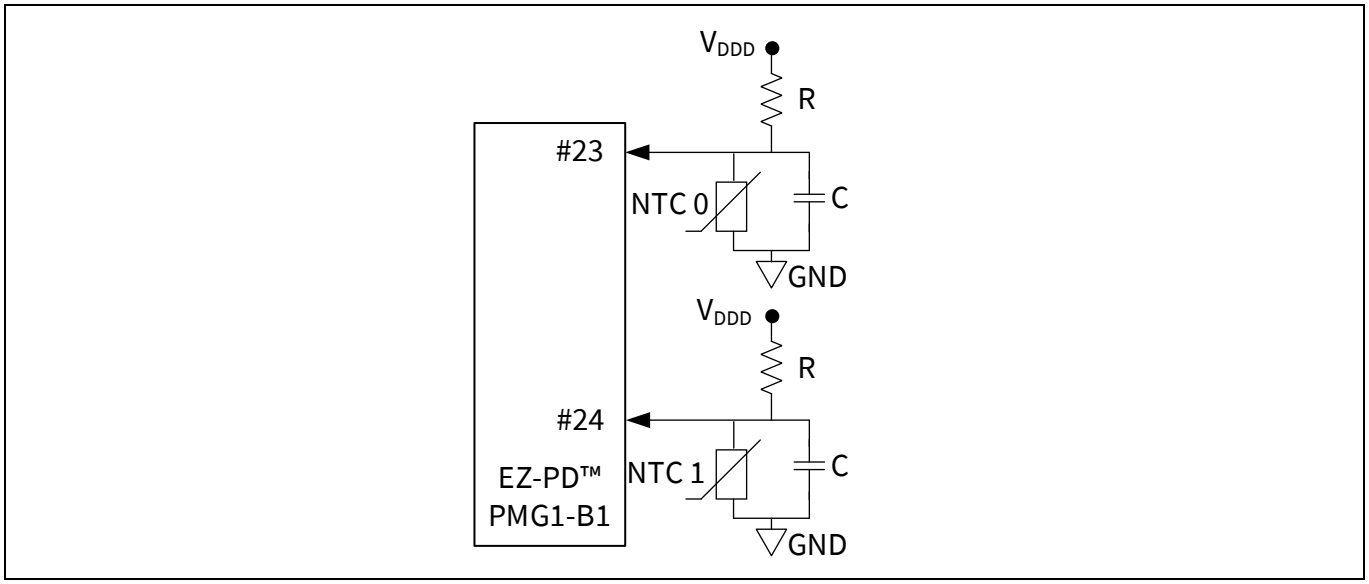

Figure 15 NTC thermistors

7.7 V_{BUS} to CC short protection

EZ-PD™ PMG1-B1 CC pins have integrated protection from accidental shorts to high-voltage V_{BUS} and CC lines. PMG1-B1 silicon handles up to 24.0 V external voltage on its CC pins without damage.

8 Constant current and constant voltage regulation

The EZ-PD™ PMG1-B1 is targeted at charging cordless power tool batteries. The PMG1-B1 has a built-in constant current loop (CC) and a constant voltage loop (CV), which transition automatically from CC to CV mode and vice-versa based on the connected battery pack status. In CC mode, the PMG1-B1 modulates the feedback to keep the charging current constant; in CV mode, the battery pack voltage is constant.

The CC/CV feedback loops are implemented using two transconductance amplifiers and an external compensator network, which sets the frequency response of the CC and CV feedback loops. In Figure 16, the control loop architecture of the PMG1-B1 pinout is shown for reference.

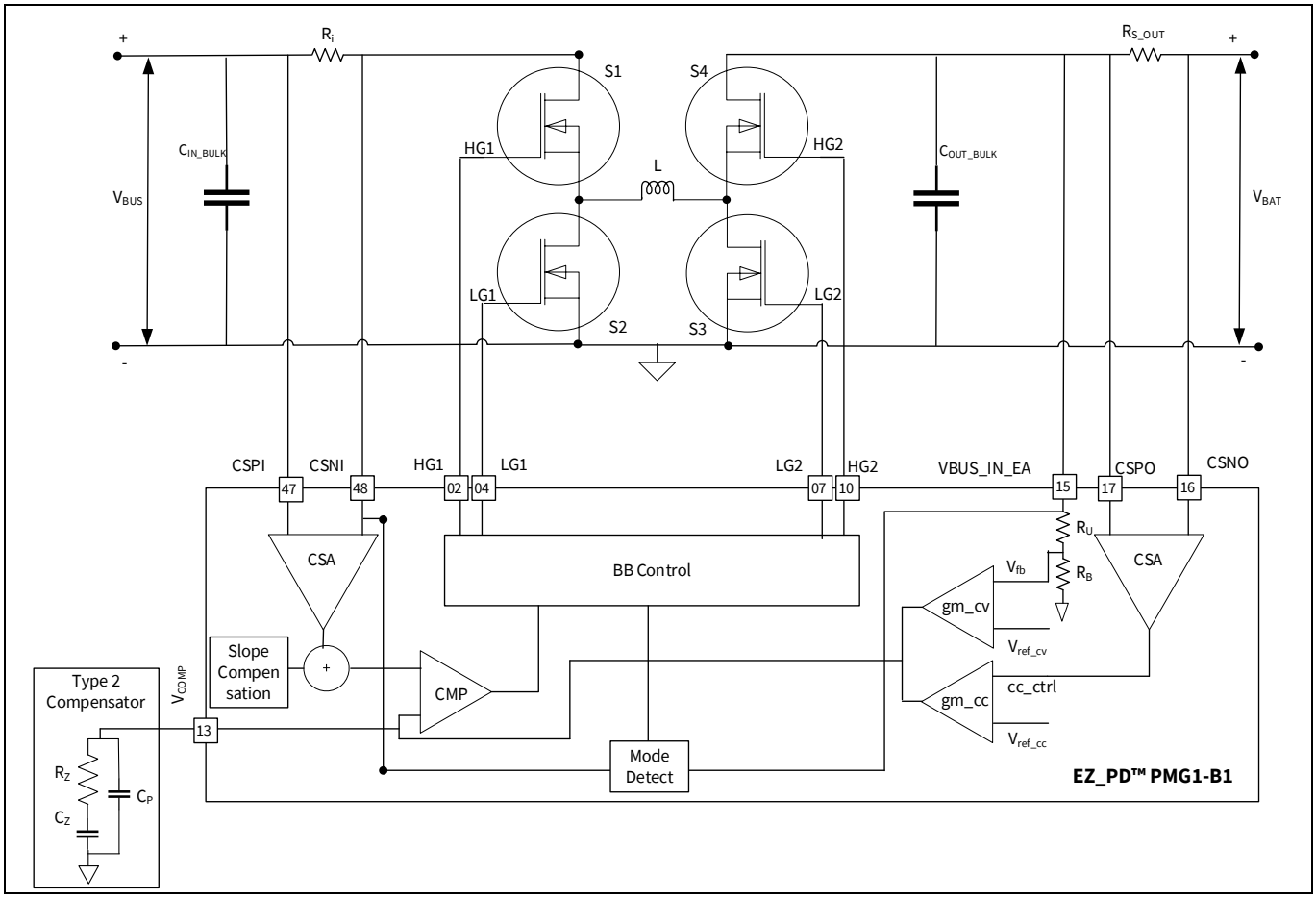

Figure 16 Control loop architecture of EZ-PD™ PMG1-B1

The error amplifier block regulates the output voltage (V_{BAT}) or output current (I_{BAT}) during CV or CC mode respectively.

EVAL_PMG1-B1_DRP_KIT is designed to regulate the constant output voltage (V_{BAT}) based on the control algorithm implemented. The battery pack voltage (V_{BAT}) is dictated by the reference voltage V_{REF_CV} and the internal resistor divider of R_U (200 kΩ) and R_B (34.5 kΩ).

Constant current and constant voltage regulation

The PMG1-B1 silicon family supports battery pack charging current (I_{BAT}) measurement and control using an external sense resistor RS_OUT (5 mΩ) in series with the V_{BAT} path. The voltage drop across the external sense resistor, RS_OUT, measures the average battery pack charging current (I_{BAT}). Constant current (CC) operation can be achieved based on the VREF_CC setting and gain of the amplifier (CSAOUTPUT).

The CV and CC loops are independent of each other but share the same external compensation network. The compensation network must be designed based on the choice of the power converter operating mode and chosen power stage component values.

9 Control system design

The choice of Type 2 external compensator component (R_Z, C_Z, and C_P) values are based on the desired loop crossover frequency (fc), chosen power component values, and transconductance amplifier gain (gm cv).

9.1 Type 2 compensator component selection

Choose the required crossover frequency to compute the compensator resistor R_Z. As a rule of thumb, in a buck converter, the crossover frequency can be about one-tenth of the switching frequency.

In a boost converter, the crossover frequency can be about one-tenth of the switching frequency and about one fifth of the right half plane (RHP) zero frequency, whichever is lower.

$$R_Z = \frac{2\pi*(R_U+R_B)*R_i*C_{OUT}*F_c}{R_B*g_{m\_cv}}$$ – for buck converter

$$R_Z = \frac{\pi*(R_U+R_B)*R_i*C_{OUT}*F_c}{R_B*g_{m\_cv}*(1-D)}$$ – for boost converter

EZ-PD™ PMG1-B1 has an internal resistive divider from the output to the error amplifier.

R_B = 34.5 kΩ and R_U = 200 kΩ.

R_i = Input current sense resistor multiplied by the input current sense amplifier (CSA) gain (G_{CSA})

The compensator zero (f_{Zcomp}) is placed at the dominant pole (f_{pplant}) of the power converter and simplifying the equation to get C_Z

$$C_Z = \frac{R_{OUT}*C_{OUT}}{R_Z}$$ – for buck converter

$$C_Z = \frac{R_{OUT}*C_{OUT}}{2*R_Z}$$ – for boost converter

The compensator pole (f_{Pcomp}) is placed at ESR zero (f_{zplant}) of the power converter and simplifies the equation to get C_P

$$C_P = \frac{R_{C_{OUT}}*C_{OUT}}{R_Z}$$

10 Application example – four-switch buck-boost converter

10.1 Key specifications

- Input voltage range: +5.0 V to +20 V
- Input current range: 0.0 A to 5.0 A
- Output voltage range: +5 V to +20 V

Note: Design calculations are shown separately for the buck converter and boost converter. If the power converter is a non-inverting output four-switch buck-boost converter, choose the best components from the buck and boost converter calculations. In these calculations, a Lithium-ion five-cell battery pack is considered. See the excel based design calculator to select power components, compensator, efficiency graphs, and Bode plots.

10.2 Power components selection – buck converter

Buck converter design example calculations are made considering the following inputs:

- V_{BUS}: 20.0 V, I_{BUS}: 5.0 A, V_{BAT}: 15.0 V, I_{BAT}: 6.0 A, F_{SW}: 400 kHz; Loop BW (F_{C_BUCK}): 10 kHz

Table 8 Buck converter power components calculation

Parameter	Formula	Calculated value	Remarks
Input bulk capacitor	$\frac{D_{BUCK} * I_{TRAN\_MAX}}{2 * \pi * F_{BW} * V_{BUS\_TRANSIENT}}$	11.93 µF	Considered load transient (I_{TRAN_MAX}) 1 A Bandwidth of the connected source (F_{BW}) 10 kHz Allowed input voltage transient ($V_{BUS\_TRANSIENT}$) 5% of V_{BUS}
Input MLCC capacitor	$\frac{D_{BUCK}\,(1 - D_{BUCK})\,I_{OUT\_MAX}}{\Delta V_{IN\_PK-PK} * F_{SW}}$	4.68 µF	Considered 3% of V_{BUS} as (ΔV_{IN_PK-PK}) peak-to-peak ripple
Power inductor	$\frac{(V_{BUS\_MAX} - V_{BAT}) * D_{BUCK}}{\Delta I_L * F_{SW}}$	5.21 µH	Considered 30% of I_{BAT} as inductor ripple (ΔI_L) - I_{TRAN_MAX} considered as 1.0 A
Output bulk capacitor (C_{OUT})	$\frac{I_{TRAN\_MAX}}{2 * \pi * F_{C\_BUCK} * V_{BAT\_TRANSIENT}}$	35.37 µF	Considered 3% transient on output voltage ($V_{BAT\_TRANSIENT}$)
Output MLCC capacitor (C_{OUT_MLCC})	$\frac{\Delta I_L}{8 * F_{SW} * \Delta V_{BAT\_PK-PK}}$	3.75 nF	Considered 1% of output voltage as output voltage ripple (ΔV_{BAT_PK-PK}) $\Delta I_L = \frac{(V_{BUS} - V_{BAT}) * D_{BUCK}}{L * F_{sw}}$

10.3 Plant transfer function – buck converter

The plant transfer function for the buck converter is

$$G_{vc}(s) = \frac{kR_{OUT}(1 + sR_{C_{OUT}}C_{OUT})F_n(s)}{R_i(1 + kR_{OUT}C_{OUT}\,s)}$$

The above component values are considered for the following frequency analysis.

Table 9 Buck converter plant calculations

Parameter	Formula	Calculated value	Remarks
Plant pole - 1 $f_{Pplant1}$	$\frac{1}{2\pi R_{OUT}C_{OUT}}$	1.62 kHz	C_{OUT} is the sum of output bulk and MLCC capacitors $R_{OUT} = V_{BAT}/I_{BAT}$
Plant zero f_{zplant}	$\frac{1}{2\pi R_{C_{OUT}}C_{OUT}}$	203.42 kHz	Considered ESR as 20 mΩ. The actual ESR value should be noted from the selected output capacitor.
Plant pole - 2 $f_{Pplant2}$	$\frac{F_{SW}}{2}$	200 kHz	aproximately $F_{SW}/2$
Plant DC gain	$k = \frac{\frac{k * R_{OUT}}{R_i}}{\left(1 + \frac{T_s R_{OUT}}{L}(m_c D' - 0.5)\right)}$	42 dB	$m_C = 1 + \frac{S_e}{S_n}$, where Se is the external slope added (50% to 100% of (V_{BAT}/L)) Sn is the input slope of inductor current (V_{BUS}/L) D` = (1-D) Ts = 1/F_{SW}
Feedback network gain $G_{div}(s)$	$\frac{R_B}{R_U + R_B}$	0.147 p.u	R_B = 34.5 kΩ R_U = 200 kΩ

10.4 Compensator transfer function – buck converter

The compensator transfer function is

$$G_{cv}(s) = \frac{(1 + sR_ZC_Z)}{sC_Z\,(1 + sR_ZC_P)}$$

Table 10 Buck converter type -2 compensator calculations

Parameter	Formula	Calculated value	Remarks
R_Z	$\frac{2\pi * (R_U + R_B) * R_i * C_{OUT} * F_{C\_Buck}}{R_B * g_{m\_cv}}$	626.52 Ω	Ri= R_{IN} x CSAin gm_cv = 1.20 mS CSA_{IN}= 9 Rs = 5 mΩ F_{C_Buck} = 10 kHz
C_Z	$\frac{R_{OUT} * C_{OUT}}{R_Z}$	56 nF	
C_P	$\frac{R_{C_{OUT}} * C_{OUT}}{R_Z}$	1.23 nF	Considered ESR as 20 mΩ
Compensator pole f_{PComp}	$\frac{1}{2\pi R_Z C_P}$	206.528 kHz	Locate the pole to cancel the plant zero
Compensator zero f_{ZComp}	$\frac{1}{2\pi R_Z C_Z}$	1.628 kHz	Locate the zero to cancel the plant pole
Compensator DC gain	$20 \log (\frac{g_{m\_cv}}{C_Z})$	77.72 dB	–

10.5 Loop transfer functions – buck converter

Table 11 Buck converter loop transfer function calculations

Parameter	Formula	Calculated value	Remarks
Loop gain $G_{LTF}(s)$	$20\log [\frac{R_B}{R_U+R_B} * \frac{gm\_cv}{2\pi F_x} * \frac{1}{R_i * C_{OUT}} * R_Z]$	0.183 dB	$F_X = F_{C\_BUCK}$; Loop gain will be '1'
Crossover frequency F_{C_BUCK}	$[\frac{R_B}{R_U+R_B} * \frac{gm\_cv}{2\pi} * \frac{1}{R_i * C_{OUT}} * R_Z]$	10.21 kHz	Calculated crossover frequency is close to designed crossover frequency
Loop phase	$90 + \mathrm{Tan}^{-1}\left(\frac{F_{C\_BUCK}}{F_{ZCOMP}}\right) - \mathrm{Tan}^{-1}\left(\frac{F_{C\_BUCK}}{F_{PPLANT1}}\right) + \mathrm{Tan}^{-1}\left(\frac{F_{C\_BUCK}}{F_{ZPLANT}}\right) - \mathrm{Tan}^{-1}\left(\frac{F_{C\_BUCK}}{F_{PCOMP}}\right)$	89.99°	–

10.6 Power components selection – boost converter

Boost converter design example calculations are made considering the following inputs.

- V_{BUS}: 12 V, V_{BAT}: 20 V, I_{BAT}: 2.72 A, F_{SW}: 400 kHz; F_{C_BOOST}: 4 kHz

Table 12 Boost converter power components calculation

Parameter	Formula	Calculated value	Remarks
Input bulk capacitor	$\frac{I_{TRAN\_MAX}/(1-D_{BOOST})}{2*\pi*F_{BW}*V_{BUS\_TRANSIENT}}$	44.21 µF	Considered load transient (I_{TRAN_MAX}) 1 A Bandwidth of the connected source (F_{BW}) 10 kHz. Allowed input voltage transient ($V_{BUS\_TRANSIENT}$) 5% of V_{BUS}
Input MLCC capacitor	$\frac{\Delta I_L}{8*F_{SW}*\Delta V_{BUS\_PK-PK}}$	4.72 µF	Considered 1% of V_{BUS} as (ΔV_{BUS_pk-pk}) peak-to-peak ripple $\Delta I_L = (0.2 \text{ to } 0.4) * I_{BAT\_MAX} * \frac{V_{BAT}}{V_{BUS\_MIN}}$
Power inductor	$\frac{V_{BUS\_MAX}*D_{BOOST}}{\Delta I_L * F_{SW}}$	6.61 µH	–
Output bulk capacitor	$\frac{I_{TRAN\_MAX}}{2*\pi*F_{C\_BOOST}*V_{BUS\_TRANSIENT}}$	66.3 µF	Considered 3% transient on output voltage. F_{RHP} zero = 62 kHz. Make sure F_{C_BOOST} << (F_{RHP} zero/5)
Output MLCC capacitor	$\frac{I_{BAT}*D_{BOOST}}{F_{SW}*\Delta V_{BAT\_PK-PK}}$	22.67 µF	Considered 1% output voltage ripple

10.7 Plant transfer function – boost converter

Plant transfer function $G_{vc}(s) = \frac{\hat{V}_{OUT}(s)}{\hat{V}_C(s)} = \frac{kR_{OUT}D'\left(1-\frac{s}{\left(R_{OUT}D'^2/L\right)}\right)\left(1+\frac{s}{\left(1/R_{COUT}C_{OUT}\right)}\right)F_n(s)}{R_i\left(1+\frac{s}{\left(2/R_{OUT}C_{OUT}\right)}\right)}$

Table 13 Boost converter plant calculations

Parameter	Formula	Calculated value	Remarks
Plant pole - 1 F_{Pplant}	$2/(2\pi R_{OUT}C_{OUT})$	486.76 Hz	Considered total C_{OUT}
Plant zero F_{zplant}	$1/(2\pi R_{C_{OUT}}C_{OUT})$	89.44 kHz	Considered ESR as 20 mΩ. The actual ESR value should be noted from the selected output capacitor.
RHP zero (F_{RHP} zero)	$R_{OUT}(1-D_{BOOST})^2/(2\pi L_{BOOST})$	63.71 kHz	–
Plant DC gain	$20\log(\frac{R_{OUT}}{R_i} * (1-D_{BOOST}))$	39.82 dB	$R_i = R_{IN} \times$ CSA gain R_i = 5 mΩ * 9 = 45 mΩ
Plant phase	$\mathrm{Tan}^{-1}\left(\frac{F_{CP}}{F_{zplant}}\right) - \mathrm{Tan}^{-1}\left(\frac{F_{CP}}{F_{Pplant}}\right)$	61°	Plant crossover frequency (F_{CP}) is $F_{Pplant} * 10^{DCgain/20}$
Feedback network gain $G_{div}(s)$	$\frac{R_B}{R_U + R_B}$	0.147 p.u	R_B = 34.5 kΩ R_U = 200 kΩ

10.8 Compensator transfer function – boost converter

Type 2 compensator transfer function $G_{ea}(s) = \frac{(1+sR_ZC_Z)}{sC_Z(1+sR_ZC_P)}$

Table 14 Boost converter type 2 compensator calculations

Parameter	Formula	Calculated value	Remarks
R_Z	$\frac{\pi * (R_U + R_B) * R_i * C_{OUT} * F_{C\_BOOST}}{R_B * g_{m\_cv} * (1-D_{BOOST})}$	474.96 Ω	g_{m_cv} = 1.20 mS
C_Z	$\frac{R_{OUT} * C_{OUT}}{2 * R_Z}$	688.4 nF	–
C_P	$\frac{R_{C_{OUT}} * C_{OUT}}{R_Z}$	3.74 nF	Considered ESR as 20 mΩ. The actual ESR value should be noted from the selected output capacitor.
Compensator pole f_{PComp}	$\frac{1}{2\pi R_Z C_P}$	89.596 kHz	–
Compensator zero f_{ZComp}	$\frac{1}{2\pi R_Z C_Z}$	486.77 Hz	–
Compensator DC gain	$20\log(\frac{g_{m\_cv}}{C_Z})$	65 dB	–

10.9 Loop transfer functions – boost converter

Table 15 Boost converter loop transfer function calculations

Parameter	Formula	Calculated value	Remarks
Loop gain $G_{LTF}(s)$	$20\log\left[\frac{(1-D_{BOOST})}{R_i} * \frac{R_B}{R_U+R_B} * g_{m\_cv} * \frac{1}{\pi F_{C\_BOOST}} * \frac{R_Z}{C_{OUT}}\right]$	-0.005 dB	$F_X = F_{C\_BOOST}$; Loop gain will be '1'
Crossover frequency F_{C_BOOST}	$\left[\frac{(1-D_{BOOST})}{R_i} * \frac{R_B}{R_U+R_B} * g_{m\_cv} * \frac{1}{\pi} * \frac{R_Z}{C_{OUT}}\right]$	4 kHz	–
Loop phase	$\left[90 + \left(\mathrm{Tan}^{-1}\left(2\pi F_{C\_BOOST} R_Z C_Z\right) * \frac{180}{\pi}\right) - \left(\mathrm{Tan}^{-1}\left(\pi F_{C\_BOOST} R_{OUT} C_{OUT}\right) * \frac{180}{\pi}\right)\right]$	89.99°	–

11 Design calculator

11.1 Introduction

The PMG1-B1 USB-PD MCU based EVAL_PMG1_B1_DRP kit power stage design calculator is a Microsoft Excel file that calculates the power stage components for a PCMC CCM non-inverting 4-switch buck-boost converter. Based on user inputs, the design calculator suggests components for the power stage and Type 2 compensator values.

Figure 17 shows the high-level block diagram of the power stage of the EVAL_PMG1_B1_DRP kit based on the PMG1-B1 USB-PD MCU. The same component designators are referenced in the document titled *"PMG1-B1 USB-PD MCU based Battery Charger Power Stage Design Calculator"* (see *002-38895 .xlsx*) available with this document.

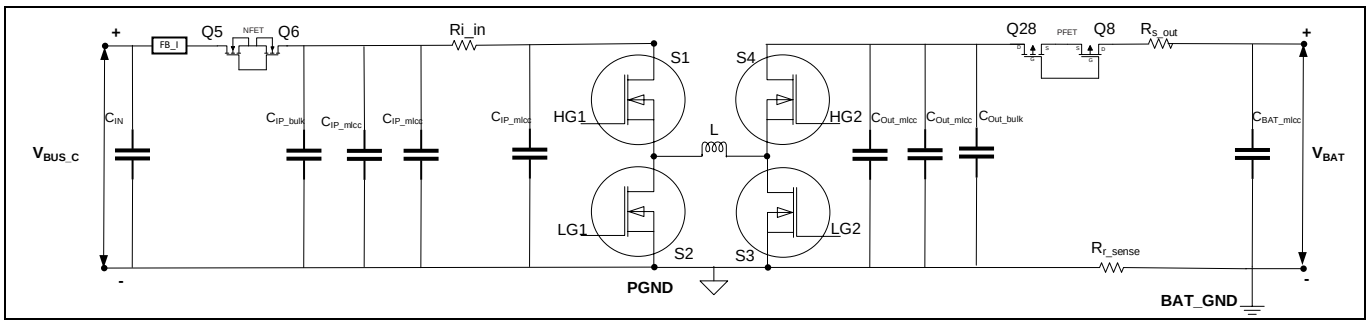

Figure 17 High-level block diagram

Figure 18 shows the Type 2 compensator used in this EVAL_PMG1_B1_DRP kit. The same component designators are referenced in the document titled "*PMG1-B1 USB-PD MCU based Battery Charger Power Stage Design Calculator*" (see *002-35689.xlsx*) available with this document.

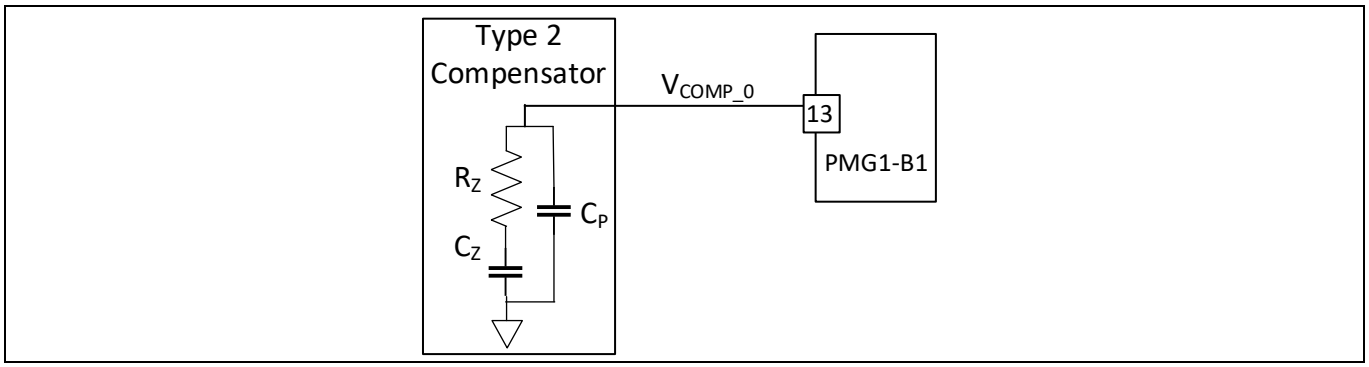

Figure 18 Type 2 compensator

11.2 General description

EZ-PD™ PMG1-B1 is a highly integrated single-port USB Type-C Power Delivery (PD) solution with integrated buck-boost controllers. It complies with the latest USB Type-C and USB-PD specifications and is targeted at battery charging application for power and garden tools. Integration offered by PMG1-B1 not only reduces the BOM but also provides a footprint-optimized solution.

For more, see Introduction section.

11.3 Features

The EVAL_PMG1_B1_DRP kit power stage design calculator allows you to choose the power stage and Type 2 compensator components for a PCMC CCM non-inverting FSBBC and buck converters.

The power stage design calculator is based on the CCM power stage of the PCMC non-inverting FSBBC topology. The inputs to the calculator include the following:

- Design inputs:
  - Operating input voltage range (V_{BUS})
  - Operating output voltages / battery voltage (V_{BAT})
  - Output battery charging current (I_{BAT})
  - Nominal switching frequency of the power converter (F_{SW})
- Converter performance parameters:
  - Input voltage transients due to change in load conditions ($V_{BUS\_TRANSIENT}$)
  - Input voltage ripple (V_{BUS_RIPPLE})
  - Output voltage transients due to change in load conditions ($V_{BAT\_TRANSIENT}$)
  - Output voltage ripple (V_{BAT_RIPPLE})
  - Load step ($I_{BAT\_TRANSIENT}$)
- Control loop and EMI filter parameters:
  - Buck converter control loop crossover frequency (F_{C_BUCK})
  - Boost converter control loop crossover frequency (F_{C_BOOST})

Note: The crossover frequency in a buck converter can be one-tenth of the chosen switching frequency. In a boost converter, the crossover frequency can be less than one-tenth of the switching frequency and less than one-fifth of the right half plane (RHP) zero frequency, whichever is lower.

This design calculator provides design guidance for the following:

- Power stage components:
  - Power inductor (L)
  - Input bulk capacitor (C_{IP_BULK})
  - Output bulk capacitor (C_{OUT_BULK})
  - Power MOSFETs (S1-S4)
  - Input MLCC (C_{IP_MLCC})
  - Output MLCC (C_{OUT_MLCC})
  - Type-C Side back-to-back NFET (Q5, Q6)
  - Battery Side back-to-back PFET (Q8, Q28)
- Type 2 compensator components:
  - Compensator resistor (Rz)
  - Compensator capacitor (Cz)
  - Compensator capacitor (C_P)

Note: *The calculated Type 2 compensator (Rz, Cz, and Cp) values are based on the selected buck converter crossover frequency referenced in the design calculator - Cross over frequency-buck (F_{C_Buck}).*

The design calculator provides the following converter performance parameters for the provided inputs:

- Input voltage transients due to change in load conditions ($V_{BUS\_TRANSIENT\_Calc}$)
- Input voltage ripple ($V_{BUS\_RIPPLE\_Calc}$)
- Output voltage transients due to change in load conditions ($V_{BAT\_TRANSIENT\_Calc}$)
- Output voltage ripple ($V_{BAT\_RIPPLE\_Calc}$)

This design calculator provides the following plots and graphs for the entered values:

- Efficiency graphs of the converter in buck mode operation (CCM)
- Efficiency graphs of the converter in boost mode operation (CCM)
- Bode plots of the buck converter
- Bode plots of the boost converter

11.4 Usage model

The EVAL_PMG1_B1_DRP kit design calculator is a Microsoft Excel file with the following worksheets:

- **About the calculator:** Includes basic information about the design calculator.
- **HomePage:** Allows you to provide design inputs for the power stage and compensator values for the chosen topology.
- **Designers recipe:** Lists the PMG1-B1 silicon parameters that must be validated. Note that only Infineon representatives can modify the parameters.
- **Buck mode - CV_Bode Plot:** Displays the peak buck converter plant, compensator, and loop gain plots.
- **Boost mode - CV_Bode Plot:** Displays the peak boost converter plant, compensator, and loop gain plots.

- **Efficiency buck mode:** Displays the efficiency graphs of the buck converter for the chosen inputs.
- **Efficiency boost mode:** Displays the efficiency graphs of the boost converter for the chosen inputs.

The HomePage of the design calculator has the following sections:

Note: *In the HomePage, you can provide the design inputs in the fields marked blue ( ) and observe the design outputs in the fields marked ( ).*

- **Section 1 - Design inputs:** Allows you to provide the design inputs. By default, PCMCC CCM non-inverting buck–boost converter power stage components are displayed. An option is given to choose to select the number of battery cells in the “No of Cells” drop-down menu. Number of cells of battery can be selected from a drop down of 2, 3, 4, or 5. Maximum output voltage depends on number of cells. As this kit supports fixed output voltage operation, minimum output voltage is 5 V.
- **Section 2 - Power components - Computed values:** Displays the calculated values for the selected topology and design inputs. Based on the values, you can choose either the off-the-shelf or custom parts.
- **Section 3 - Type 2 compensator computed values and Type 2 compensator - User chosen values:** Provides guidance on Type 2 compensator RC values; this also has the option to plug in components available off-the-shelf. The Bode plots in the ‘Buck mode - CV_Bode Plot’ and ‘Boost Mode - CV_Bode Plot’ worksheets are based on the plugged-in values.
- **Section 4 - Power components:** From the guidance values computed in Section 2, choose the off-the-shelf components and enter their characteristics. The efficiency graphs and Bode plots are derived based on the selected components and their characteristics. The component part numbers are slectedselected- based on the 5- cell design calculations, for the 2-4 battery cells power circuit design the component part numbers must be selected and entered in the section 4.
- **Section 5 - Design output for the user-chosen components:** Provides the performance of the power stage for the components selected in Section 4.
- **Section 6 - Plots/graphs for the user-chosen values:** Displays efficiency graphs and Bode plots for the components selected in Section 4.

Note: *For practical purposes, the maximum allowed duty cycle in the buck topology is 90%. Keep this in mind while choosing the required V_{OUT} voltage for a given input voltage.*

12 Printed circuit board (PCB) layout guidelines – best practices

The printed circuit board (PCB) layout plays an important role in achieving the system's functional, EMC, and thermal goals. The following guidelines help to reduce the design cycle time and cost to achieve electrical performance and to meet respective regulatory standards. Acceptable performance can be obtained with alternate layout schemes as well.

The following best practices are intended as guidelines.

Note: The silicon pin numbers referenced in this document are with respect to the EZ-PD™ PMG1-B1 48-pin QFN package.

- **PCB layers stack – multilayer board:** A multilayer PCB helps to achieve the highest level of signal integrity. Here is one of the examples to choose the layer stacking for a single-sided component placement PCB design.
  - Top layer: Switching power components and power traces
  - Second layer: Ground (GND) plane; it is a common practice to almost fill with the ground. This is the layer immediately below the power components/traces layer.
  - Third layer: Switching signals and GND plane. Ensure that signals in the third layer do not overlap with signals or power traces in the bottom layer.
  - Bottom layer: DC and low-frequency signals, GND plane, and DC power traces
  - All layer's copper thickness is 2 oz. (70 µm)

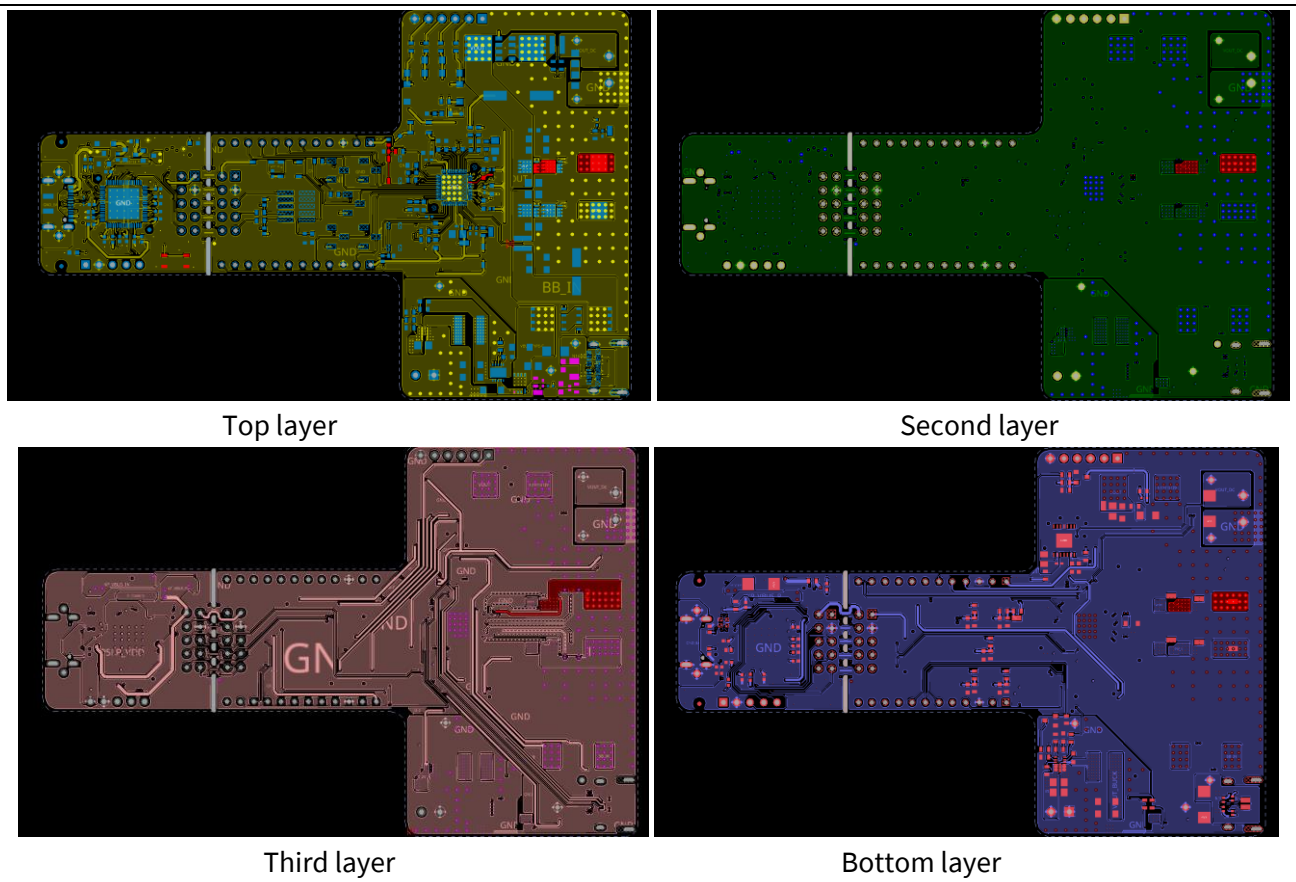

Figure 19 PCB layers – top, second, third, and bottom layers

- **EZ-PD™ PMG1-B1 mounting:** Connect the silicon exposed pad (EPAD) to the GND plane and connect this to the battery pack/board input (V_{BUS}) negative terminal via a low-impedance path. The exposed EPAD helps to dissipate the heat into the PCB; for better transfer of heat, through-hole vias can be made over the silicon exposed pad (EPAD) area.

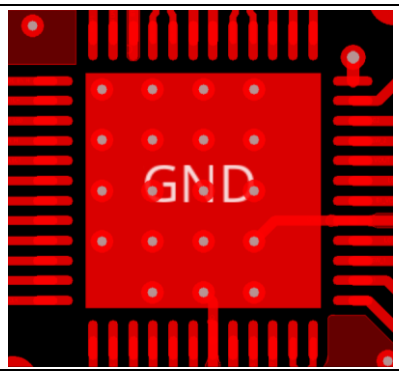

Figure 20 EZ-PD™ PMG1-B1 EPAD through-hole vias

- **SW1 and PGND traces:** Connect the PMG1-B1 SW1 and PGND pins to the drain and source of the power MOSFET (controlled by PMG1-B1 LG1 pin #4 is LG1_0) using dedicated low-impedance traces. Route the SW1 and PGND differentially with no other switching or noise supply traces next to them. A good option is to provide ground guarding traces on either side; pin #3 is SW1, and pin #5 is PGND.

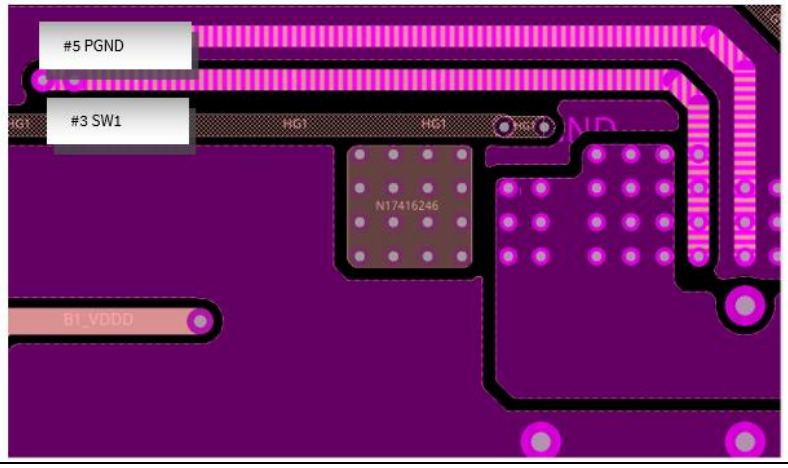

Figure 21 SW1 and PGND traces

- **SW2 and V_{OUT} traces:** Connect the PMG1-B1 SW2 and V_{OUT} pins to the source and drain of the power MOSFET (controlled by the PMG1-B1 pin #10 is HG2) using dedicated low-impedance traces. Route the SW2 and V_{OUT} differentially with no other switching or noise supply traces next to them. A good option is to provide ground guarding traces on either side; pin #9 is SW2, and pin #8 is V_{out}.

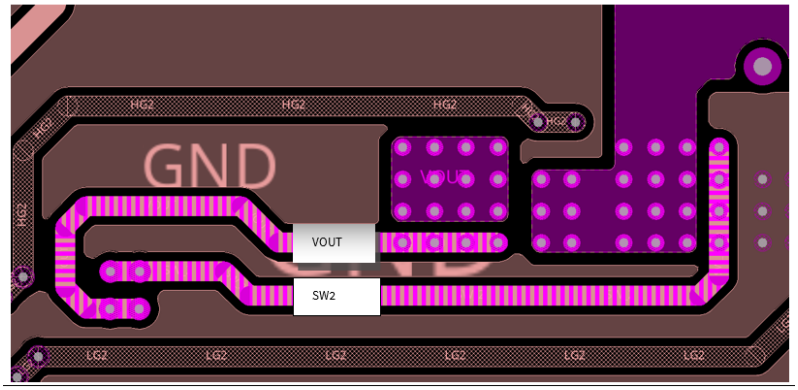

Figure 22 SW2 and V_{OUT} traces of port #0 and port #1

- **CSPI and CSNI pin traces:** Connect the peak input current sense resistor (R45) positive terminal to the EZ-PD™ PMG1-B1 pin #47 CSPI and the negative terminal to pin #48 CSNI using a dedicated Kelvin connection. Route the CSPI and CSNI differentially with no other switching or noise supply traces next to them; a good option is to provide ground guarding traces on either side.

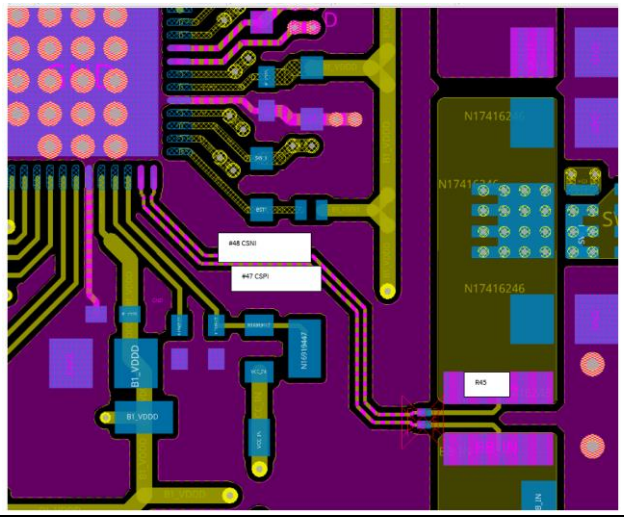

Figure 23 Peak input current sense resistor traces connection to EZ-PD™ PMG1-B1

- **CSPO and CSNO pin traces:** Connect the output current sense resistor (R48) positive terminal to the PMG1-B1 pin #17 CSPO and the negative terminal to pin #16 CSNO using a dedicated Kelvin connection. Route the CSPO and CSNO differentially with no other switching or noise supply traces next to them. A good option is to provide ground guarding traces on either side. Provide an option to place a decoupling capacitor between CSPO and CSNO to suppress noise, if any.

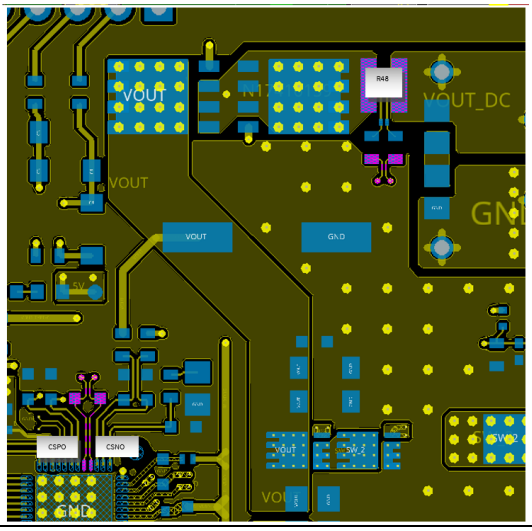

Figure 24 Output current sense resistor traces connection to EZ-PD™ PMG1-B1

- **Bootstrap capacitor placement:** Keep the buck and boost converter as close as possible to EZ-PD™ PMG1-B1 pins. Place the buck converter circuit bootstrap capacitor C_{BOOT} close to pin #1 (SW1) and pin #3 (BST1), and boost converter circuit bootstrap capacitor C_{BOOT} close to pin #9 (SW2), and pin #11 (BST2).

  Similarly, place the buck converter bootstrap diode D_{BOOT} close to pin #3 (BST1), and boost converter bootstrap diode D_{BOOT} close to pin #11 (BST2).

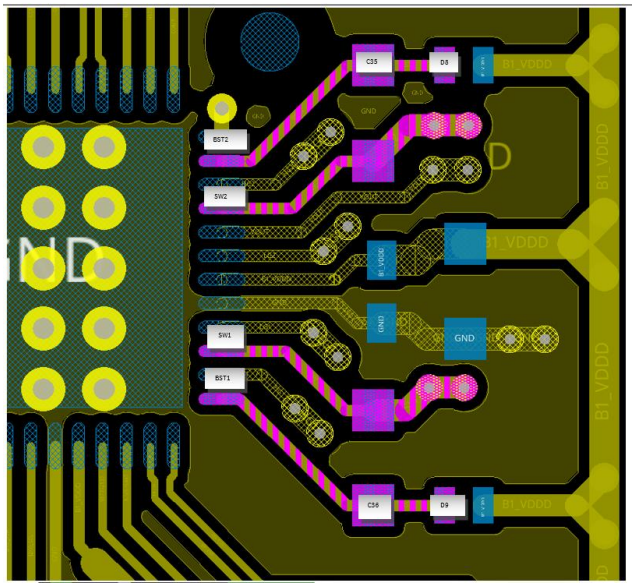

Figure 25 Buck and boost converter bootstrap capacitor and diode placement of port #0

- **Error amplifier traces (COMP):** Place the Type 2 compensator network components (Rz, Cz, C_P) near the EZ-PD™ PMG1-B1 COMP pin and the silicon ground. Ensure that traces do not pass through noisy areas, such as switch nodes. Error amplifier output pin #13 is connected to the Type 2 compensator network R42, C38, and C39.

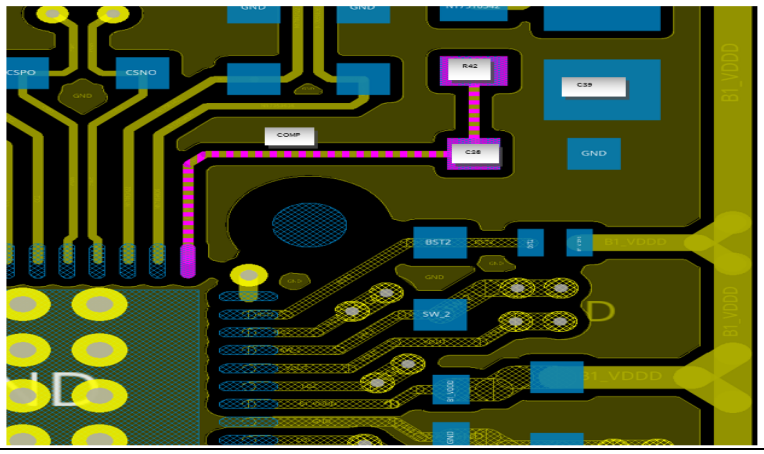

Figure 26 Error amplifier traces (COMP)

- **Bypass or decoupling capacitors to ground plane:** Bypass or decoupling capacitors to the ground plane can reduce the return current path, which reduces the size of the loop and hence radiation. Ensure that no bypass capacitor is connected between a power plane and an unrelated ground plane, which can cause capacitive coupling. The capacitor value is selected based on the Impedance vs. Frequency graph. The bypass capacitor should be placed as close as possible to the silicon pins and silicon ground via the low-impedance path.

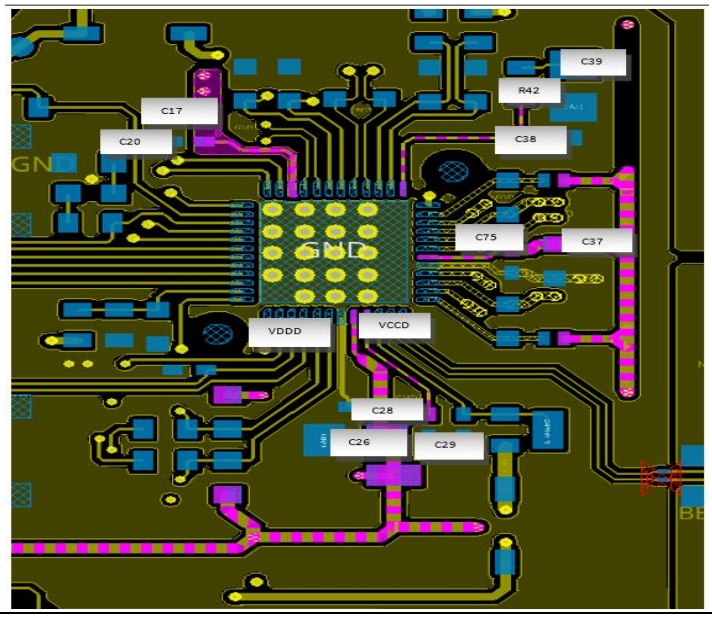

Figure 27 MLCC capacitors placement

- **MOSFET gate drive traces:** The four-switch buck-boost converter gate drive loops must be as small as possible to improve the switch turn ON/OFF performance and to reduce electromagnetic interference. The gate drive trace length should be short with a wide trace to minimize the gate path impedance. Ensure that there is a solid ground plane in the layer adjacent to any layer with the gate drive signals.

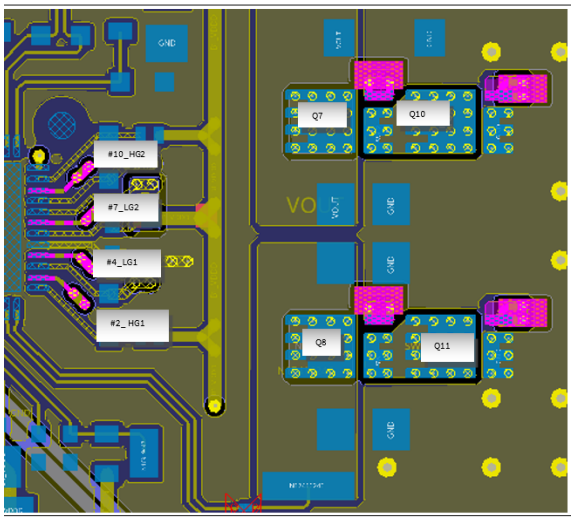

Figure 28 Gate drive traces

- **Shorten return paths:** Keep return current paths as short as possible and route them along paths of least resistance. Return paths should be about the same length as transmit traces or shorter.

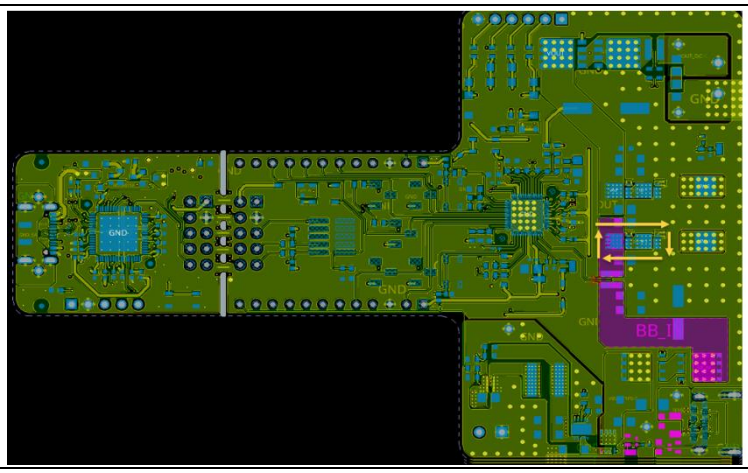

Figure 29 Shorter return paths

- **High-frequency capacitors:** The high (di/dt) pulsating currents radiate magnetic fields and generate high-voltage ringing and spikes across MOSFETs and PCB traces. The high-frequency decoupling capacitors (C_{HF}) should be placed as close as possible to the half-bridge MOSFETs to mitigate artifacts of high di/dt.

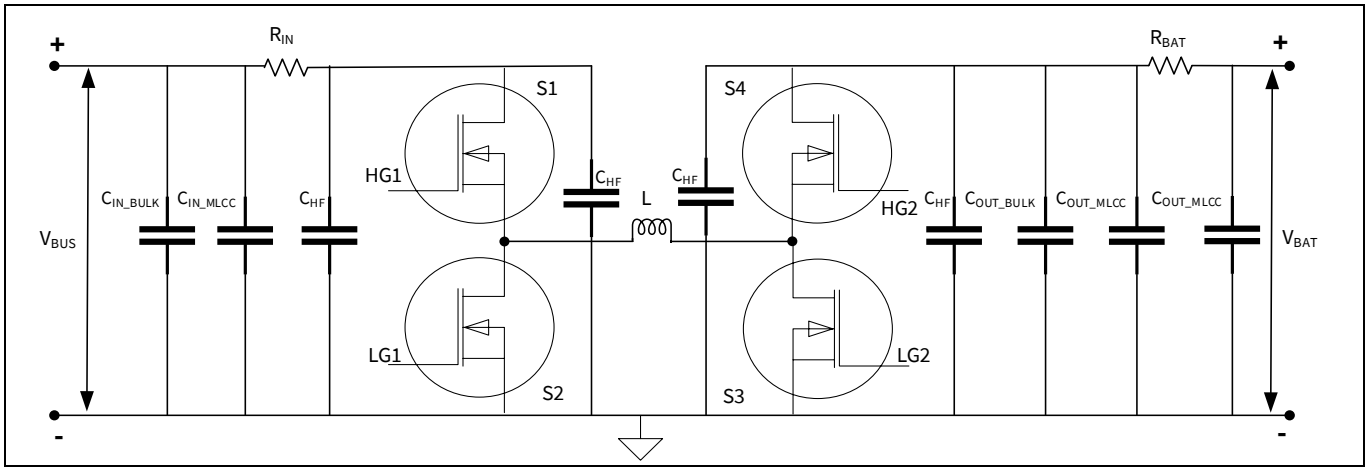

Figure 30 High-frequency capacitors (C_{HF}) in the circuit schematics

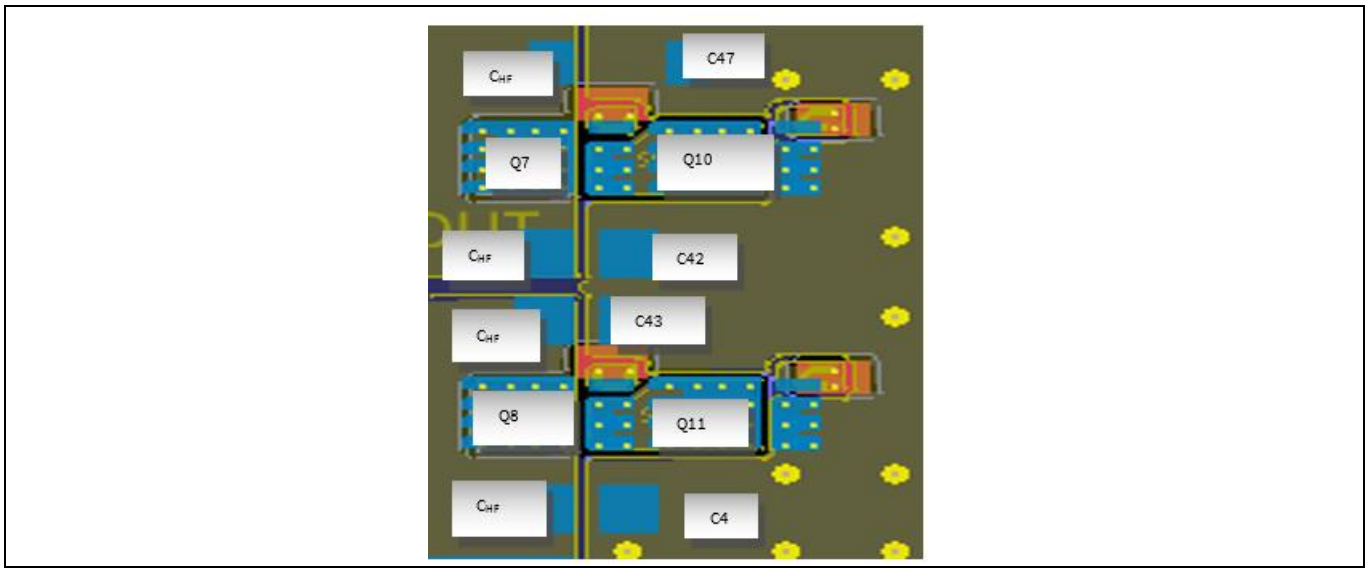

Figure 31 High-frequency capacitors (C_{HF}) placement on the PCB layout

- **Minimize switch node area:** In Buck mode, the high dV/dt switch node voltage SW1 swings between V_{IN} and GND, and in boost mode, the high dV/dt switch node voltage SW2 swings between V_{OUT} and GND, this causes high frequency switching noise which is a strong source of EMI noise. The switch node copper area should be minimal to have the least coupling capacitance between the switch node and other noise-sensitive traces. However, to have an allowable temperature rise of power MOSFETs, provide a solid copper area in the immediate PCB layer.

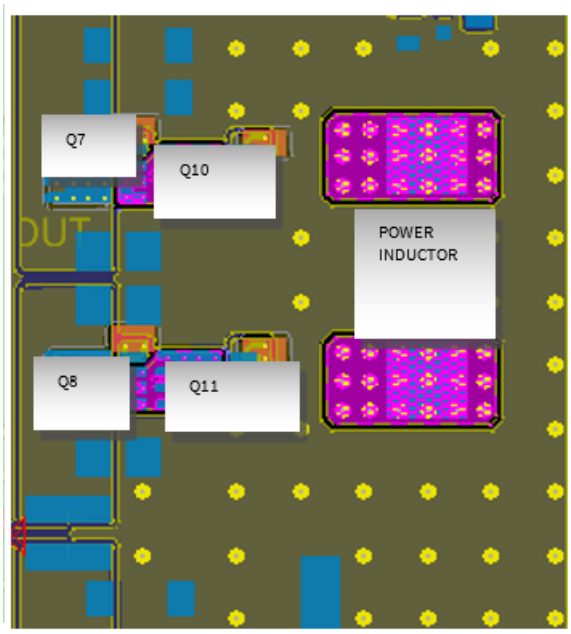

Figure 32 Switch node traces

- **Unused area:** In all layers, fill unused areas with copper to reduce the temperature of power components. Connect the copper areas to either V_{BUS}, $V_{BUS,}$ or GND (preferably to GND).
- **Ground connection:** When routing the circuitry around the IC, the analog small signal ground and the power ground (used for the compensation networks) for switching currents must be kept separate. They should be connected together at a point where switching activity is at a minimum. This helps keep the analog ground quiet.
- **Ground plane:** Larger solid ground planes provide lower impedance; signals can disperse more easily with more area, reducing emissions, cross-talk, and noise. Ensure there is a good reason to use a split ground plane and ensure that they are only connected at a single point (a few of the applications may demand separate analog and digital grounds to avoid noise coupling). Multiple ground connections in a split-ground PCB can create loops, resulting in an antenna that radiates EMI. The ground plane layer should be as close as possible to the layer with power MOSFETs.

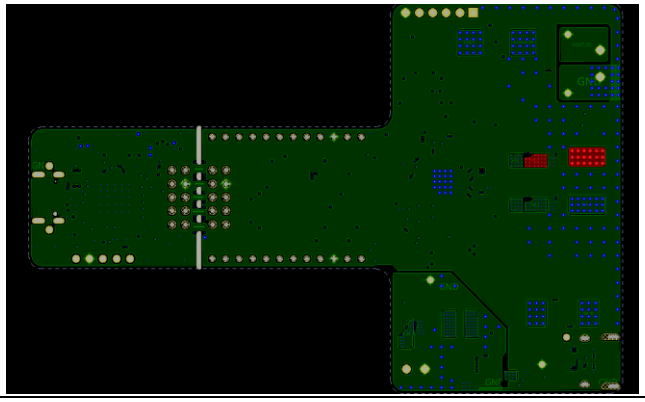

Figure 33 PCB layer 2

- **Ground vias:** Place a few ground-connecting vias close to the component grounds directly to the dedicated ground plane. Do not keep the ground plane isolated. Stitch it to internal layers with vias for better EMI/EMC. A few are marked in Figure 34.

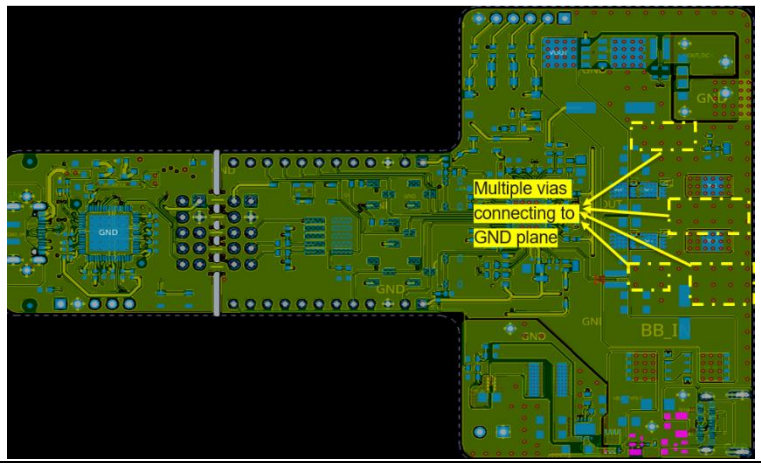

Figure 34 Multiple vias connecting to the GND plane

- **Avoid sharp right-angle bends:** Sharp right-angle bends cause changes in the characteristic impedance and reflections. This can be mitigated by rounding the right-angle bend to help reduce the radiated EMI.
- **High dV/dt signals:** Keep the high dV/dt nodes such as SW1, SW2, BST1, BST2, HG1, and HG2 nodes away from sensitive small signal nodes.
- **Separate high-speed and low-speed signals:** Keep high-speed signals such as PWM signals separate from low-speed signals such as compensation networks and analog signals separate from digital signals.
- **Control signals trace width:** To minimize the trace impedance, control signals traces should be at least 10 to 20-mil wide.
- **High-current-carrying power path traces:** High-current-carrying power path traces should be as short as possible and should be sized to carry twice the rated current.
- **ESD immunity:** To improve ESD immunity, connect MLCCs close to the USB Type-C connector GND and V_{BUS} terminals through the low-impedance paths.
- **CC lines:** Keep the trace length to a minimum from the Type-C receptacle to the configurable channels (CC) lines and to the external ESD diodes.

13 Thermal considerations

In cordless power tool charging applications, the solution boards are concealed into an enclosure without air cooling, and without an external heat sink. Typically, the components such as power MOSFETs and inductors are surface mounted; therefore, the placement of power components, trace width, and the size of the copper area are critical to limit thermal stress.

Place the power components in such a way that they minimize the length of high-current-flow paths through power MOSFETs, inductors, current sense resistors, and input and output capacitors that results in lower conduction losses. Low-impedance traces and solid low-impedance power component land patterns minimize the thermal stress.

See Design calculator section for more details on best practices.

14 Application example: buck converter with load switch

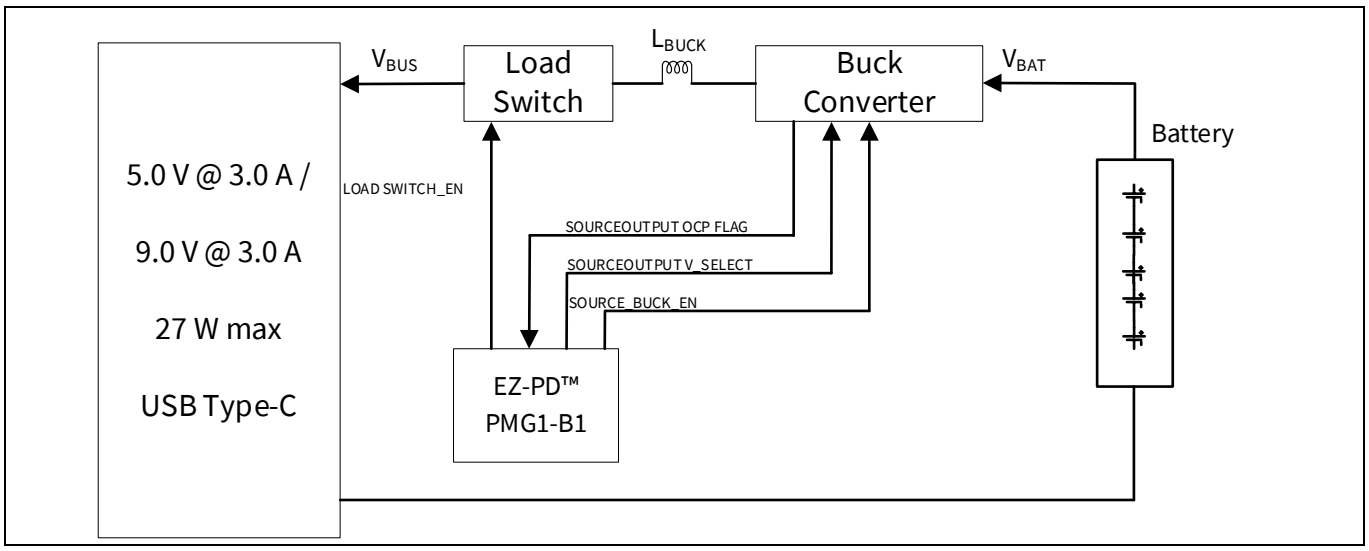

Figure 35 Buck converter with load switch

To support the DRP applications, external power supply or battery is connected. When EZ-PD™ PMG1-B1 is detected as a source, it will advertise only 5 V and 9 V power data objects (PDOs) and provide a maximum power of 27 W. programmable power supply (PPS) mode is not supported in Source mode. Along with the buck converter operation there is a load switch to connect and disconnect the buck converter to the USB Type-C connector.

15 Circuit schematic and PCB layout review checklist

Table 16 is a checklist for the key circuit schematic component choices; Table 17 is a checklist for the PCB layout guidelines. Please provide an answer to each checklist item to find out the extent to which your hardware design meets these guidelines.

Note: The silicon pinout details are based on the EZ-PD™ PMG1-B1 controller.

Table 16 Circuit schematic checklist

Sl. No	Schematic checklist	Answer (Yes/no/NA)
1	Are the current measurement resistors chosen with a minimum of 5 mΩ resistance value and its tolerance is better than 1%?	–
2	Is the bypass capacitor connected between V_{BUS_IN} and GND 0.1-µF at maximum operating output voltage?	–
3	Is the bypass capacitor connected between PVDD and PGND 1.0-µF at an operating voltage of 5.0 V?	–
4	Is the capacitor connected at V_{CCD} 0.1-µF at an operating voltage of 1.8 V?	–
5	Is the bootstrap capacitor connected at the buck-side SW node and BST 0.1 µF at the maximum input voltage?	–
6	Is the bootstrap capacitor connected at the boost-side SW node and BST 0.1 µF at the maximum output voltage?	–
7	Is the chosen bootstrap diode forward voltage small enough to ensure lower conduction losses?	–
8	Is the chosen bootstrap diode reverse recovery time small enough to achieve a reduction in reverse recovery losses?	–
9	Is a 1.0-µF capacitor connected in parallel with the 0.1-µF capacitor connected at V_{DDD} pin #6? Does this capacitor offer the specified capacitance at the operating voltage of 5.0 V?	–
10	Is a 10-µF capacitor connected in parallel with the 0.1-µF capacitor connected at V_{DDD} pin #44? Does this capacitor offer the specified capacitance at the operating voltage of 5.0 V?	–
11	Is a 0.1-µF ceramic bypass capacitor connected at V_{IN} pin #46? Does this capacitor offer the specified capacitance at the maximum operating input voltage?	–
12	Is a 0.1-µF ceramic bypass capacitor connected at V_{BUS} pin #14 to ground? Does this capacitor offer the specified capacitance at the maximum operating output voltage?	–
13	Is a 0.1-µF ceramic bypass capacitor connected at V_{OUT} pin #15 to ground? Does this capacitor offer the specified capacitance at the maximum operating output voltage?	–
14	Is a provision given for a ceramic capacitor between the silicon pins CSPO and CSNO?	–
15	Is the 390 pF capacitor terminated between CC1, CC2, and ground respectively?	–
16	Can the chosen bulk capacitors carry the computed ripple current?	–

Sl. No	Schematic checklist	Answer (Yes/no/NA)
17	Is the calculated maximum temperature of the bulk capacitors within the temperature range offered by the chosen capacitor?	–
18	Can the chosen bulk capacitor's ESR result in lower than the specification ripple limits?	–
19	Do the chosen type 2 compensator resistor and capacitors have lower tolerance across the operating conditions?	–
20	Are the chosen buck-boost switches N-channel logic level MOSFETs?	–
21	Is the gate threshold voltage of the chosen N-channel buck-boost MOSFET much lower than 5.0 V?	–
22	Is the chosen provider MOSFET an N-channel?	–
23	Is the maximum gate-source voltage of the chosen N-channel provider MOSFET more than DUT rated output voltage?	–
24	Is the selected input TVS diode's reverse working maximum voltage (V_{RWM}) higher than the maximum operating voltage?	–
25	Is the TVS diode breakdown voltage (V_{BR}) significantly lower than the maximum allowable voltage rating of the silicon, specified in the silicon datasheet table "Electrical Specifications: Absolute Maximum Ratings and pin Based Absolute Maximum Ratings" at V_{IN}, V_{BUS}, DP, DM, CC1, CC2?	–
26	Is the reverse current of the TVS diode (I_R) low in nominal operating voltage?	–
27	Are the chosen inductors magnetically shielded to minimize EMI?	–
28	Does the chosen inductor have a lower DCR value to ensure better efficiency?	–
29	Is the inductance variation of the chosen inductors less than 20%?	–
30	Is the saturation current of the chosen inductor much higher than the inductor peak operating current (minimum two times)?	–
31	Is the selected power inductor SRF much higher (at least ten times) than the operating switching frequency?	–
32	Is the selected NTC thermistor's operating range between -40°C to 125°C and or lower than the maximum operating conditions of the DUT?	–
33	Is the resistor connected in series with the NTC chip thermistor, and the nominal resistance value meeting the maximum operating temperature specifications?	–
34	Is a capacitor connected across (~1000 pF) the NTC thermistor to roll off high-frequency noises?	–
35	Is there a provision to assemble 10-µF to 20-µF capacitors across V_{BAT} to GND protection MOSFET and its sense resistor? *Note: This provision is not required where V_{BAT} to GND protection circuit is not used.*	–
36	Can the male receptacle and housing be locked to have a secure connection and orientation?	–

Table 17 PCB layout guidelines checklist

Sl. No	Layout checklist	Answer (Yes/no/NA)
1	Is EZ-PD™ PMG1-B1 exposed pad (EPAD) connected to the ground using vias?	–
2	Are the EZ-PD™ PMG1-B1 'SW1' and 'PGND' pins routed differentially to the respective silicon pins with dedicated low-impedance trace?	–
3	Are the EVAL_PMG1-B1_DRP_KIT 'SW1' and 'PGND' traces provided ground guarding on either side?	–
4	Are the EZ-PD™ PMG1-B1 'SW2' and 'V_{OUT}' pins routed differentially to the respective silicon pins with dedicated low impedance trace?	–
5	Are the EVAL_PMG1-B1_DRP_KIT 'SW2' and 'V_{OUT}' traces provided ground guarding on either side?	–
6	Are the EZ-PD™ PMG1-B1'CSPI' and 'CSNI' pins connected to the input current sense resistor using dedicated Kelvin connections and have the shortest trace length?	–
7	Are the EZ-PD™ PMG1-B1 'CSPI' and 'CSNI' pins routed differentially with no other switching or noisy trace next to them?	–
8	Are the EVAL_PMG1-B1_DRP_KIT 'CSPI' and 'CSNI' traces provided ground guarding on either side?	–
9	Are the EZ-PD™ PMG1-B1 'CSPO' and 'CSNO' pins connected to the output current sense resistor using dedicated Kelvin connections and have the shortest trace length?	–
10	Are the EZ-PD™ PMG1-B1 'CSPO' and 'CSNO' pins routed differentially with no other switching or noisy trace next to them?	–
11	Are the EVAL_PMG1-B1_DRP_KIT 'CSPO' and 'CSNO' traces provided ground guarding on either side?	–
12	Are bootstrap capacitors and diodes placed close to EZ-PD™ PMG1-B1 pins?	–
13	Are compensator network elements (R_Z, C_Z, C_P) placed near the EZ-PD™ PMG1-B1 'COMP' pin and the silicon ground? Is it ensured that corresponding traces avoid noisy nodes and traces?	–
14	Are the decoupling capacitors placed close to the silicon pin and silicon ground with minimum trace length?	–
15	Is it ensured that the MOSFET gate driver traces are short and wide?	–
16	Is it ensured that a solid ground plane is placed in layers adjacent to MOSFET gate driver signal traces?	–
17	Is it ensured that the return current path is as short as possible?	–
18	Are the high-frequency capacitors placed as close as possible to the half-bridges to ensure that the high di/dt current loop area is reduced significantly?	–
19	Is it ensured that the SW node area is optimized?	–
20	Is it ensured that the unused area is filled with copper and connected to GND?	–
21	Are analog small signal ground and power ground kept separated and connected at a point with minimal switching activities?	–

Circuit schematic and PCB layout review checklist

Sl. No	Layout checklist	Answer (Yes/no/NA)
22	Is it ensured that a large solid ground plane is provided without any unnecessary split?	–
23	Is it ensured that sufficient ground vias are placed near the component ground to the dedicated ground layer?	–
24	Is it ensured that sharp right-angle bends are avoided?	–
25	Is it ensured that high dV/dt nodes are kept away from sensitive small signal nodes?	–
26	Is it ensured that high-frequency and low-frequency signal traces are kept separate?	–
27	Is it ensured that the ADC measurement signal low pass filter capacitor is close to the controller pins?	–

References

[1] USB specifications library

[2] USB Type-C cable and connector specification revision 2.1

[3] AN210403 – Hardware design guidelines for DRP applications using EZ-PD™ USB Type-C controllers

[4] AN218254 – Design considerations for EMI reduction in automotive power management systems

[5] AN210403 – Hardware design guidelines for DRP applications using EZ-PD™ USB Type-C controllers

[6] AN91378 – EZ-USB™ hardware design guidelines and schematic checklist

[7] AN-CoolMOS™-03: How to select the right CoolMOS™ and its power handling capability

[8] 002-35400 (datasheet): EZ-PD™ PMG1-B1 USB Type-C buck-boost controller

[9] 002-35275: EZ-PD™ PMG1-B1 MCU architecture technical reference manual

[10] AP63357 – 3.8 V to 32 V input, 3.5 A low IQ synchronous buck with enhanced EMI reduction from Diodes Incorporated

[11] STELPD01: Electronic load switch for power line from STMicroelectronics

[12] 002-35689: Power design calculator for EZ-PD™ PMG1-B1 USB PD MCU-based charging solution demo for 3-5 cell batteries

[13] 002-34168: EZ-PD™ CCG7X RSC POWER STAGE DESIGN CALCULATOR

[14] 002-34222: HARDWARE DESIGN GUIDELINES FOR EZ-PD™ CCG7X IN AUTOMOTIVE APPLICATIONS

[15] 002-28172 - CYPD7291, EZ-PD™ CCG7D Automotive USB Type-C and Buck-boost Controller Dual-port

[16] 002-33534 - CYPD7191-40LDXS EZ-PD™ CCG7S Automotive single-port USB Type-C with PD and buck-boost controller

[17] 002-35400: CYPM1115, CYPM1116, EZ-PD™ PMG1-B1 USB Type-C Buck-boost controller single-port (Preliminary)

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**	2023-11-27	Initial release.

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