Half-bridge buck converter evaluation board using the EiceDRIVER™ 2EDL803x gate driver user manual

EVAL_HB_2EDL803x-G3C/G4B/G4C/F5B

About this document

Scope and purpose

The EiceDRIVER™ 2EDL803x family is designed to drive both high-side and low-side MOSFETs in a half-bridge configuration. The floating high-side driver is capable of driving a high-side MOSFET operating at up to 120 V bootstrap voltage. Version 4 provides full 4 A current capability, while version 3 provides 3 A capability. The high-side bias voltage is generated using a bootstrap technique with an integrated bootstrap diode. The inputs of the driver are TTL logic compatible and can withstand input common mode swing from -10 V up to 20 V. Independent inputs allow controlling high- and low-side domains independently. Undervoltage lockout (UVLO) on both high- and low-side supplies forces the corresponding outputs low in the case of insufficient supply. The 2EDL803x is available in SON-8 pins 4 mm x 4 mm, SON-10 pins 4 mm x 4 mm, SON-10 pins 3 mm x 3 mm, and SOIC-8 packages.

The half-bridge buck converter evaluation board (EVAL_HB_2EDL803x) described in this document is designed as a test platform for evaluating the performance of 2EDL8034_G3C. For evaluation of different packages, evaluation boards are available as shown in Table 1.

Table 1 Board specifications

Part number	Package	Body size	Evaluation Board
2EDL803x-G3C	PG-VDSON-10-4	3 mm x 3 mm	EVAL_HB_2EDL803x-G3C
2EDL803x-G4B	PG-VSON-8-5	4 mm x 4 mm	EVAL_HB_2EDL803x-G4B
2EDL803x-G4C	PG-VDSON-10-2	4 mm x 4 mm	EVAL_HB_2EDL803x-G4C
2EDL803x-F5B	PG-DSO-8	5 mm x 6 mm	EVAL_HB_2EDL803x-F5B

Intended audience

The intended audience for this user manual is power supply designers, component engineers, hardware engineers, etc.

Evaluation Board

This board is to be used during the design-in process for evaluating and measuring characteristic curves, and for checking datasheet specifications.

Note: PCB and auxiliary circuits are NOT optimized for final customer design.

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Safety precautions

Note: Please note the following warnings regarding the hazards associated with development systems.

Table 2 Safety precautions

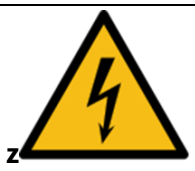	**Warning:** *The DC link potential of this board is up to 1000 VDC. When measuring voltage waveforms by oscilloscope, high-voltage differential probes must be used. Failure to do so may result in personal injury or death.*
	**Warning**: *The evaluation or reference board contains DC bus capacitors, which take time to discharge after removal of the main supply. Before working on the drive system, wait 5 minutes for capacitors to discharge to safe voltage levels. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Warning:** *The evaluation or reference board is connected to the grid input during testing. Hence, high-voltage differential probes must be used when measuring voltage waveforms by an oscilloscope. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Warning:** *Remove or disconnect power from the drive before you disconnect or reconnect wires, or perform maintenance work. Wait five minutes after removing power to discharge the bus capacitors. Do not attempt to service the drive until the bus capacitors have discharged to zero. Failure to do so may result in personal injury or death.*
	**Caution:** *The heat sink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.*
	**Caution:** *Only personnel familiar with the drive, power electronics and associated machinery should plan, install, commission and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.*
	**Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	**Caution:** *A drive that is incorrectly applied or installed can lead to component damage or reduction in product lifetime. Wiring or application errors such as undersizing the motor, supplying an incorrect or inadequate AC supply, or excessive ambient temperatures may result in system malfunction.*
	**Caution:** *The evaluation or reference board is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials that are unnecessary for system installation may result in overheating or abnormal operating conditions.*

Table of contents

1 Introduction

The evaluation board provides the design engineer with a test platform for evaluating the performance of the 2EDL8034 gate driver – such as, but not limited to, its propagation delay, delay matching, and rise/fall time characteristics. The influence of the surrounding gate drive circuitry such as the external gate resistors on the MOSFET's switching behavior can also be evaluated. The board is configured as a half-bridge buck converter in an open-loop configuration and tested with 48 V typical input voltage and 12 V typical output voltage. The Infineon components used in this evaluation board are:

- EiceDRIVER™ 2EDL8034 as half-bridge driver for the low-side and high-side MOSFET
- OptiMOS™ 5 100 V 4 mΩ (BSC040N10NS5) in a SuperSO8 package as the power MOSFET

Table 3 shows the typical board electrical specifications, but the user can vary the input voltage (60 V maximum), output voltage, output current, switching frequency, and dead-time, because the board is configured in an open-loop configuration. Care must be taken not to exceed the components' maximum voltage ratings and current ratings (for example, the inductor's saturation current rating), as well as the devices' temperature ratings. Provide adequate airflow or forced air if necessary.

Table 3 Board specifications

Parameter	Symbol	Value	Unit
Input voltage	Vin	48	V
Output voltage	Vout	12	V
Output current	Iout	0 to 8	A
Switching frequency	Fsw	200	kHz
Dead-time	DTon, DToff	100	ns
Board dimensions	88.0 mm (L) x 60.5 mm (W)		

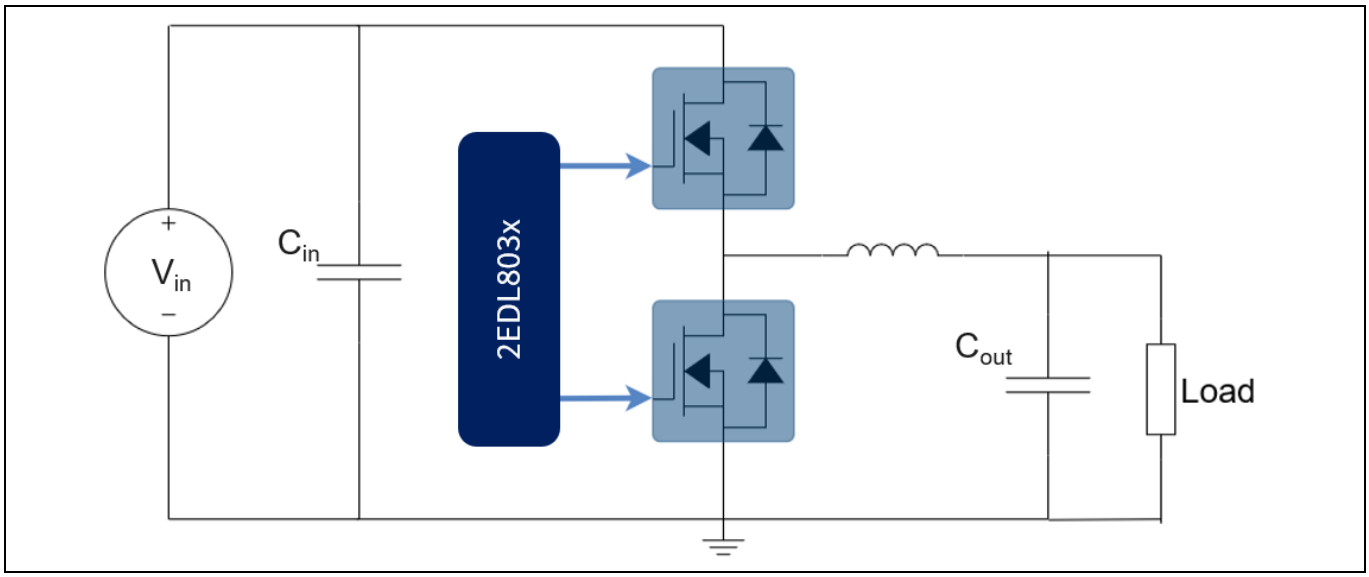

Figure 1 Block diagram of EVAL_HB_2EDL803x

2 Hardware setup

2.1 Evaluation board

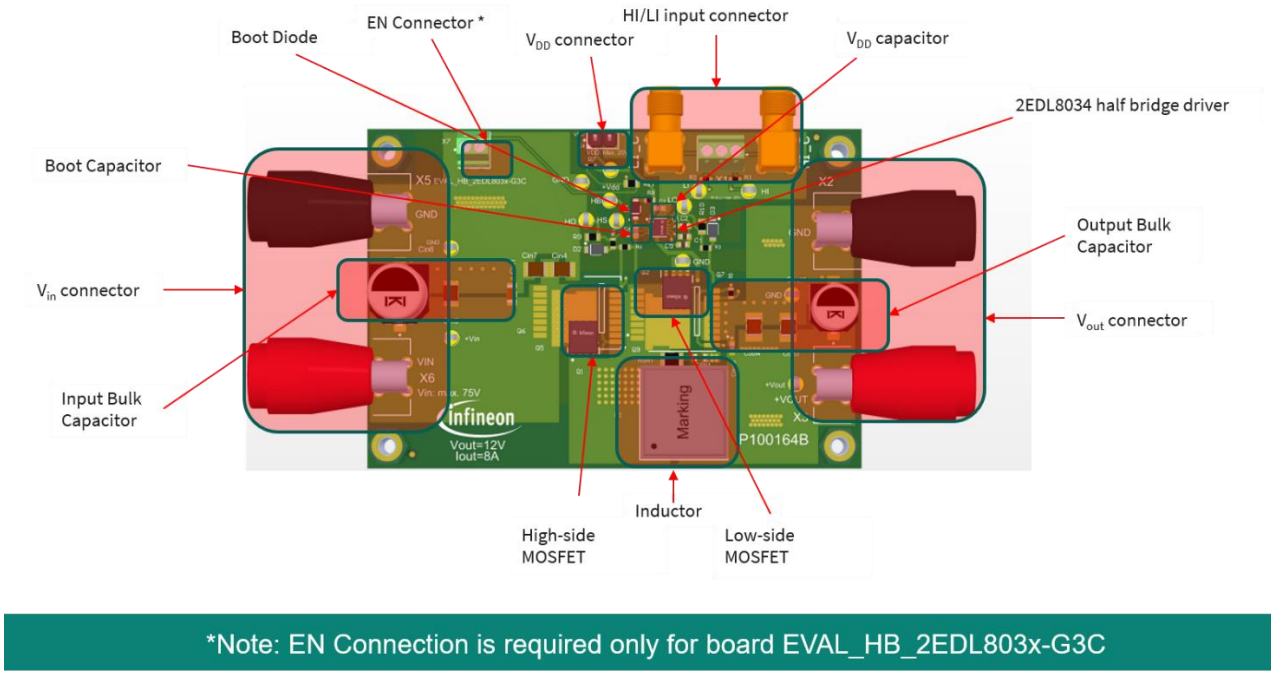

Figure 2 EVAL_HB_2EDL803x – top side

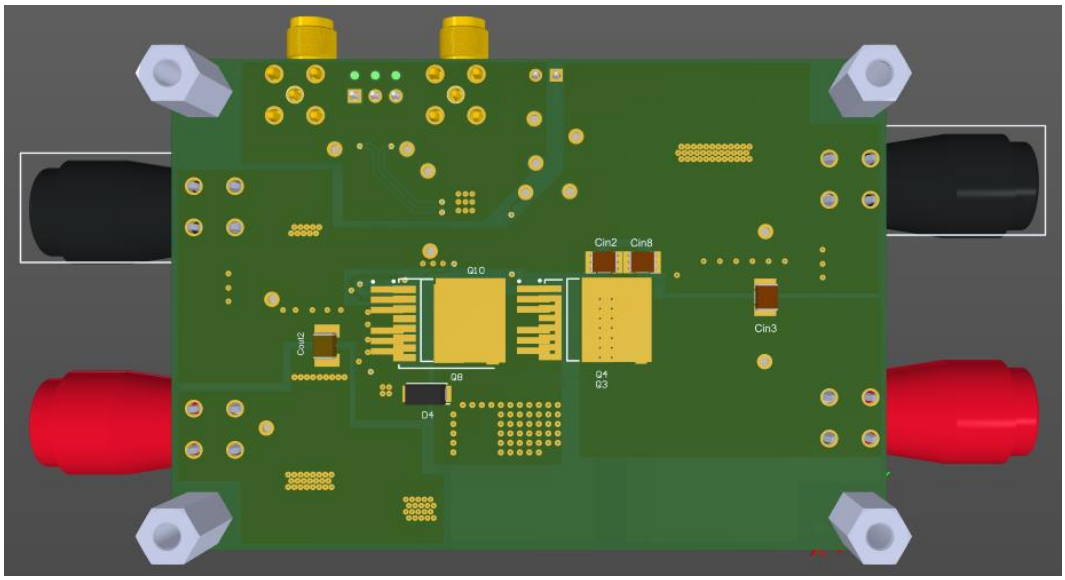

Figure 3 EVAL_HB_2EDL803x – bottom side

2.2 List of connection and test points

Table 4 Connection and test points – functional descriptions

Connection/test point	Description
X1	HI and LI PWM input
X2	Input GND
X3	Vout connector
X4	VDD connector
X5	Output GND
X6	Vin connector
X7*	EN connector
+Vin	Vin sense point
+Vout	Vout sense point

Note: EN connector (X7) is only available on the EVAL_2EDL803x-G3C board.

2.3 Quick start guide

1. Input the PWM signals (LI and HI) using a function generator with the desired pulse width, dead-time, and frequency through connector X1.
   Ensure that there is sufficient dead-time to avoid cross-conduction of the two MOSFETs.
2. Supply V_{DD} voltage using an external auxiliary power supply between 8 V and 17 V through connector X4.
3. For 2EDL803x-G3C, the enable signal should be supplied between 3 V and V_{DD} + 0.3 V through connector X7. Other drivers do not require an enable signal.
4. Supply the V_{in} voltage using an external power supply with 48 V (60 V maximum) through connector X6 (V_{in}) and X2 (GND).
   If verifying the gate driver IC characteristics only, such as propagation delay, there is no need to supply the V_{in} voltage. In this case, the HS pin must be shorted to GND to have a charging path for the bootstrap capacitor.
5. Connect the V_{out} to the electronic load through connector X3 (V_{out}) and X5 (GND) and increase the output current up to 8 A maximum.
   Care must be taken not to exceed the inductor's saturation limit.
6. The V_{DD}, LI, HI, LO, and HS pins of the gate driver can be measured by a low-voltage single-ended probe, while the HO-HS and HB-HS should be measured using low-voltage differential probes.
   Probing loops should be as short as possible to avoid any induced ringing, and probes should be placed near the driver pins to ensure accurate measurement of the driver's performance.
7. To power down the board, turn off the load first and then turn off the input voltage supply. Then turn off the enable signal in the case of 2EDL80x-G3C. Finally, turn off the driver bias supply.

3 Test results

Figure 4 and Figure 5 show the falling and rising propagation delay of the low-side and high-side drives with the V_{DD} bias supplied and V_{in} = 48 V with no load on output.

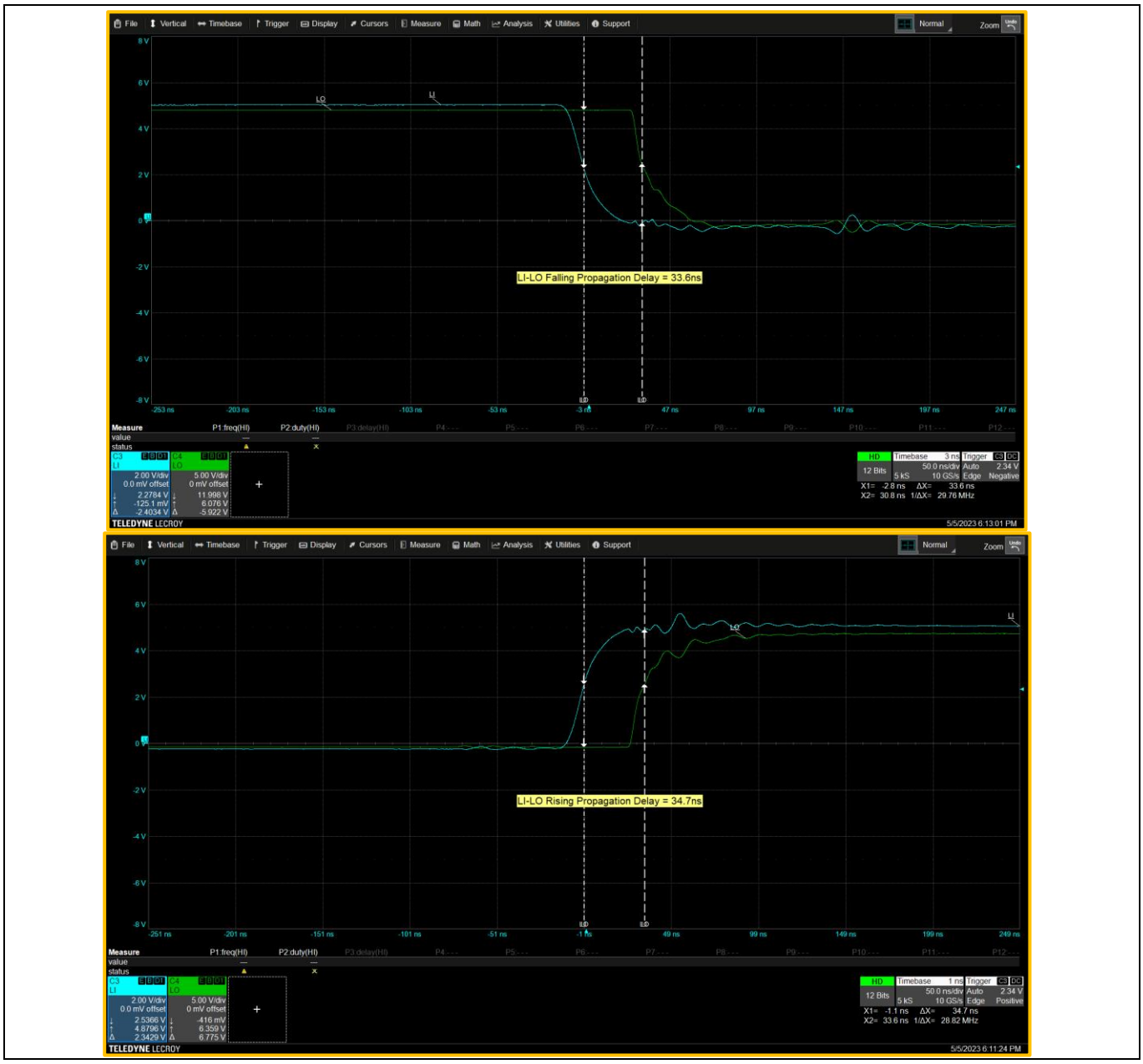

Figure 4 LI-LO falling (33.6 ns) and rising (34.7 ns) propagation delay (V_{DD} = 12 V, V_{in} = 48 V, C_{load} = 4.1 nF)

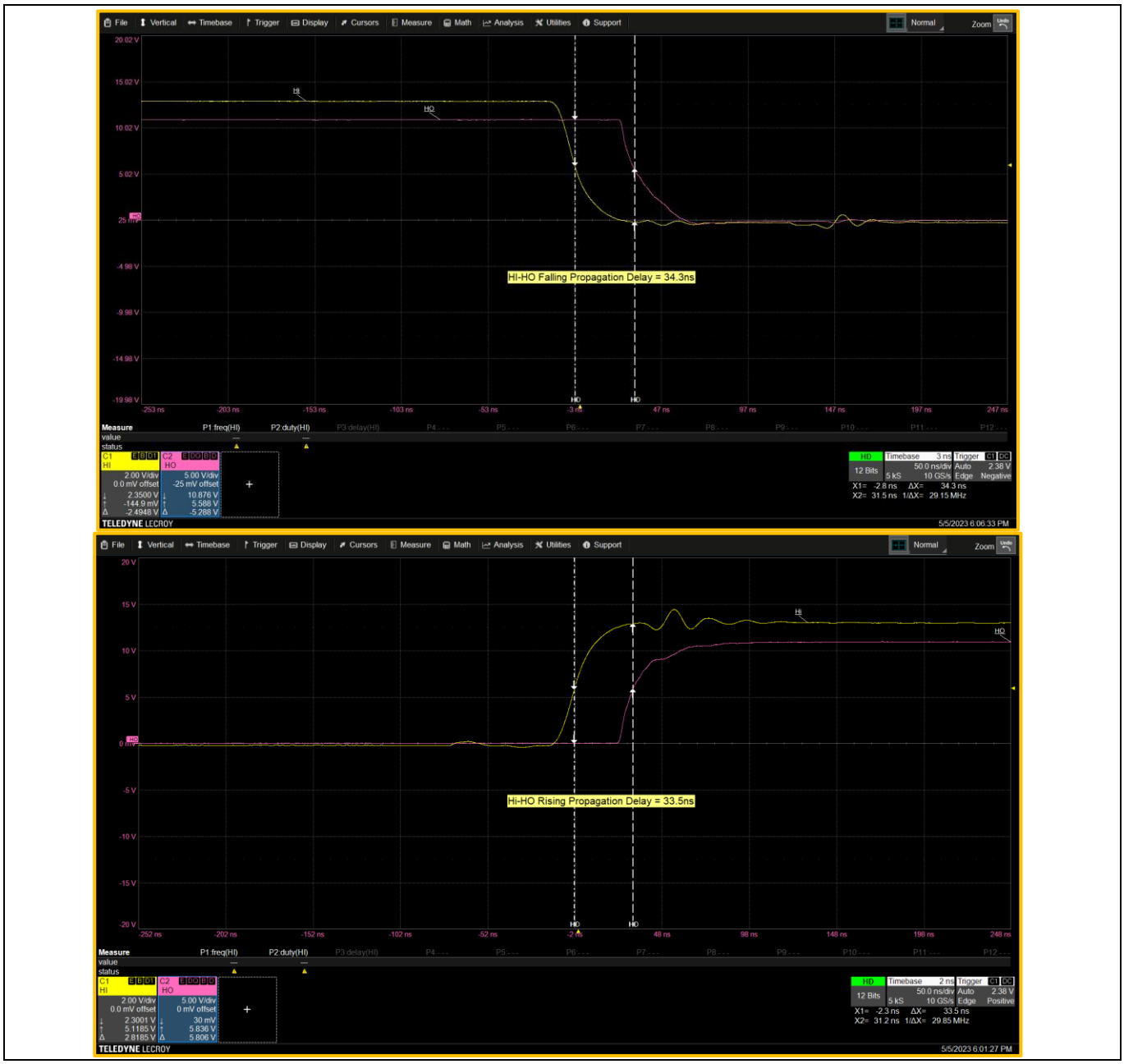

Figure 5 HI-HO falling (34.3 ns) and rising (33.5 ns) propagation delay (V_{DD} = 12 V, V_{in} = 48 V, C_{load} = 4.1 nF)

Figure 6 shows the high-side and low-side output waveforms together with the switch node waveforms at V_{in} = 48 V, V_{DD} = 12 V, duty = 23 percent, F_{sw} = 200 kHz, load = 8 A, and T_A = 25°C.

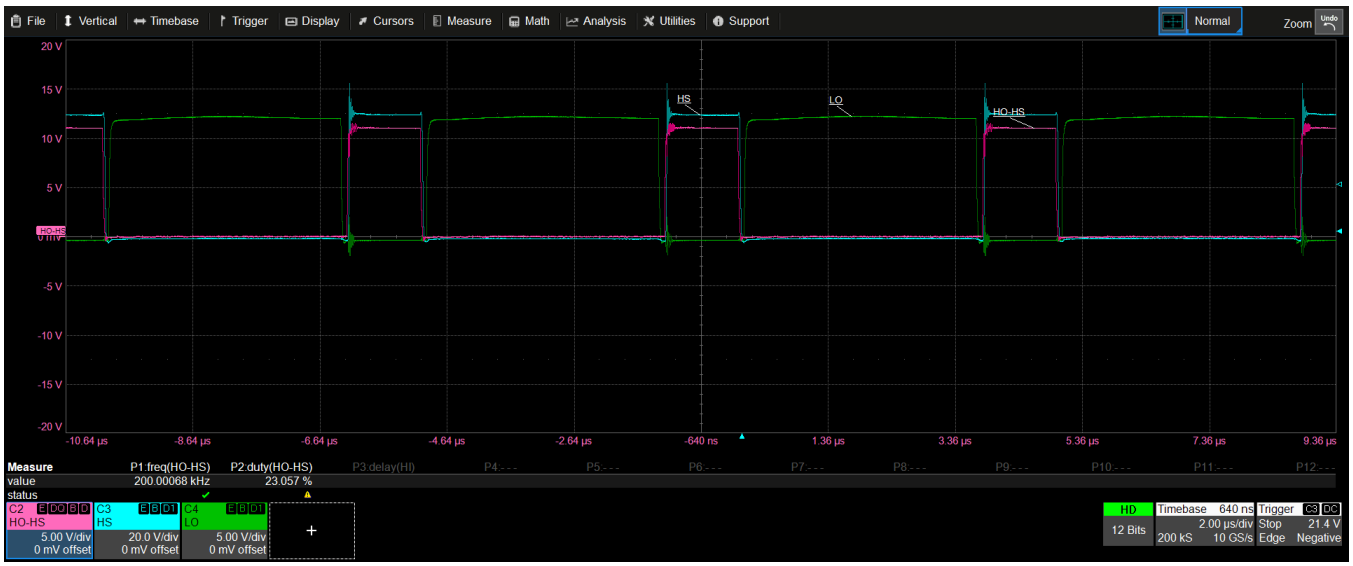

Figure 6 LO (green), HO (pink), HS (yellow) waveforms

4 Footprint selection for different FETs

The evaluation board allows the user to test the performance of the driver IC with different FETs available in various footprints. Table 5 lists all the footprints supported on this board.

Table 5 FET footprints supported on the evaluation board

Package	Ref. designator	Preferred FET	Figure
PG-TDSON-8-1 (SuperSO8)	Q1 and Q2	BSC040N10NS5	Figure 7
TO263-7-3	Q3 and Q10	IPB032N10N5	Figure 8
PG-HSOF-8-1	Q4 and Q9	IPT020N10N3	Figure 9
PG-HSOG-8-1	Q5 and Q8	IAUS300N10S5N014	Figure 10
PG-HDSOP-16-2	Q6 and Q7	IAUS260N10S5N019T	Figure 11

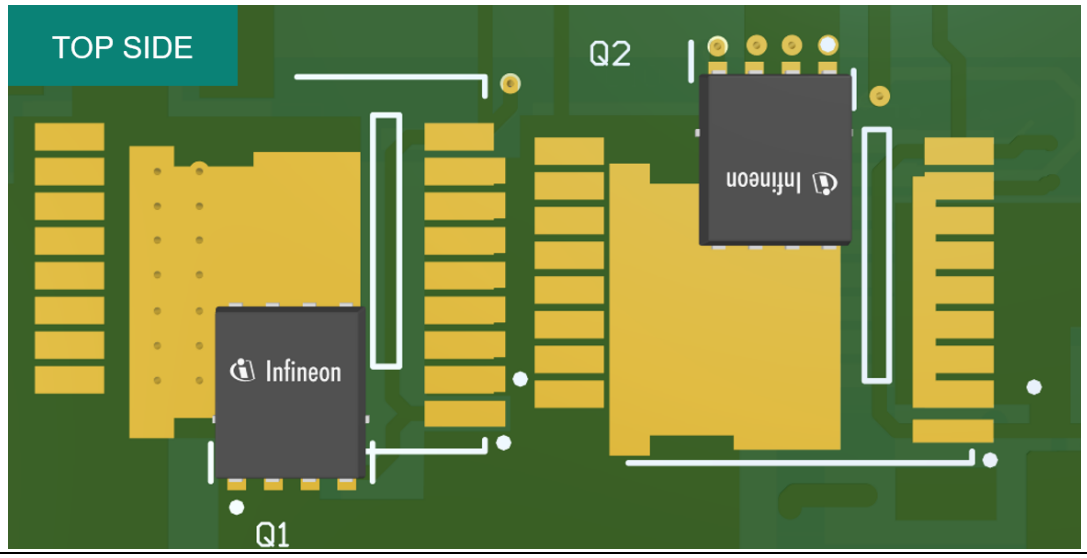

Figure 7 PG-TDSON-8-1 (SuperSO8) package

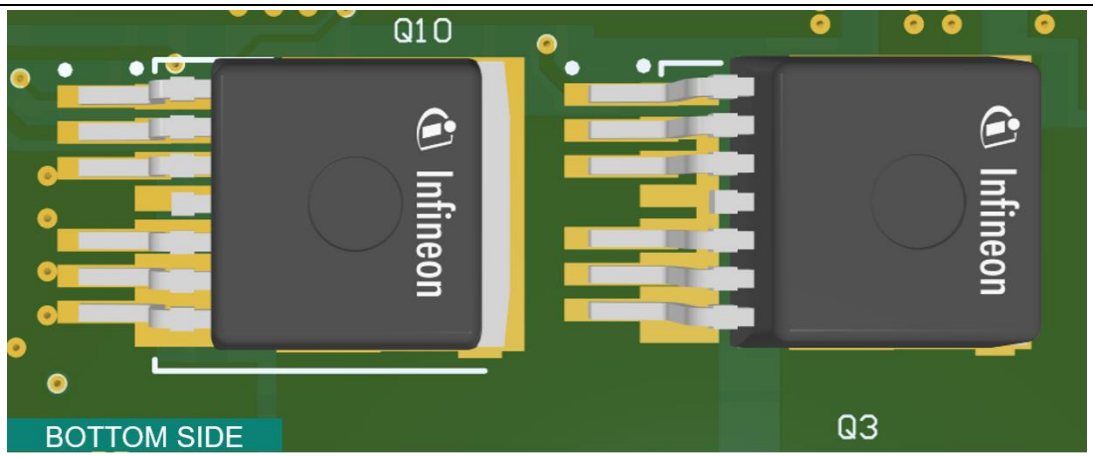

Figure 8 TO263-7-3 package

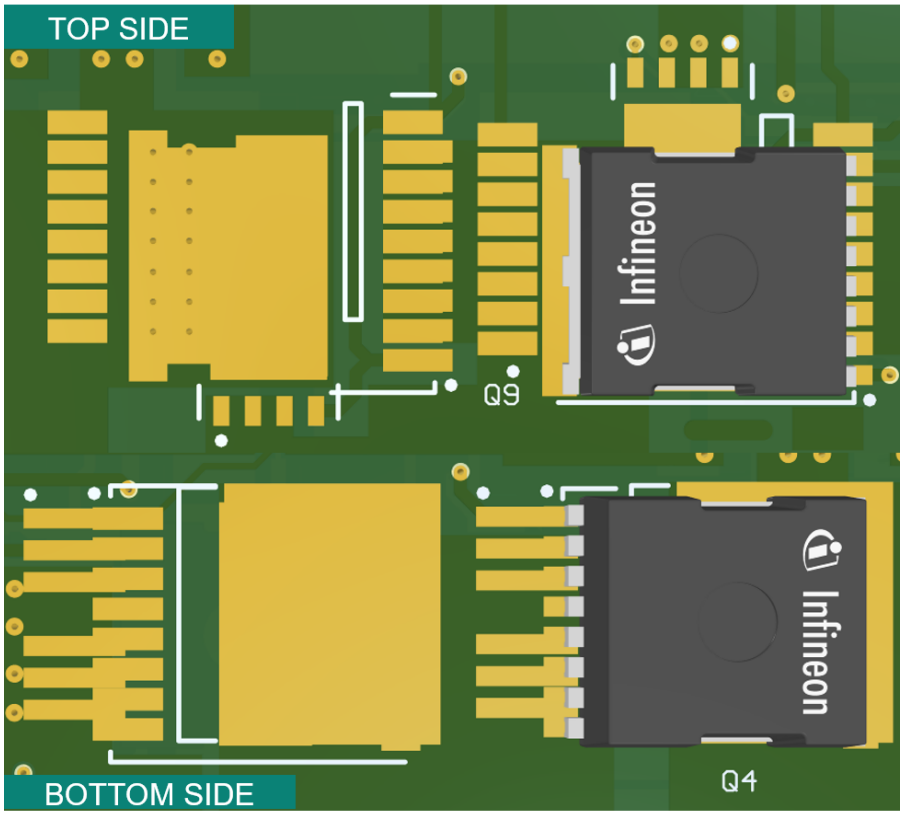

Figure 9 PG-HSOF-8-1 package

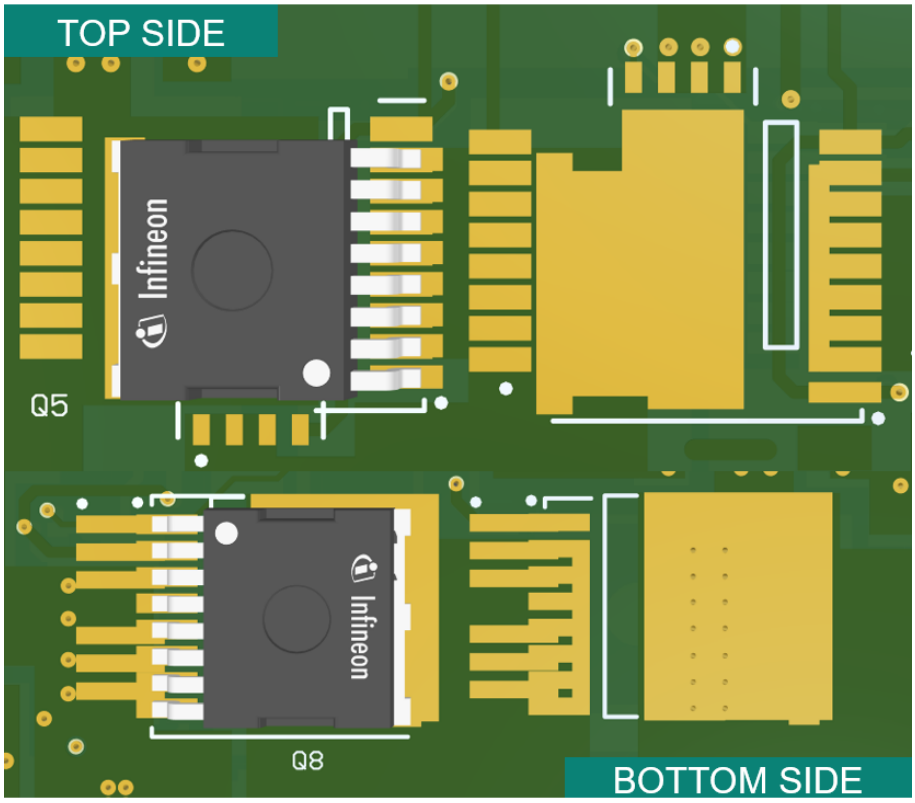

Figure 10 PG-HSOG-8-1 package

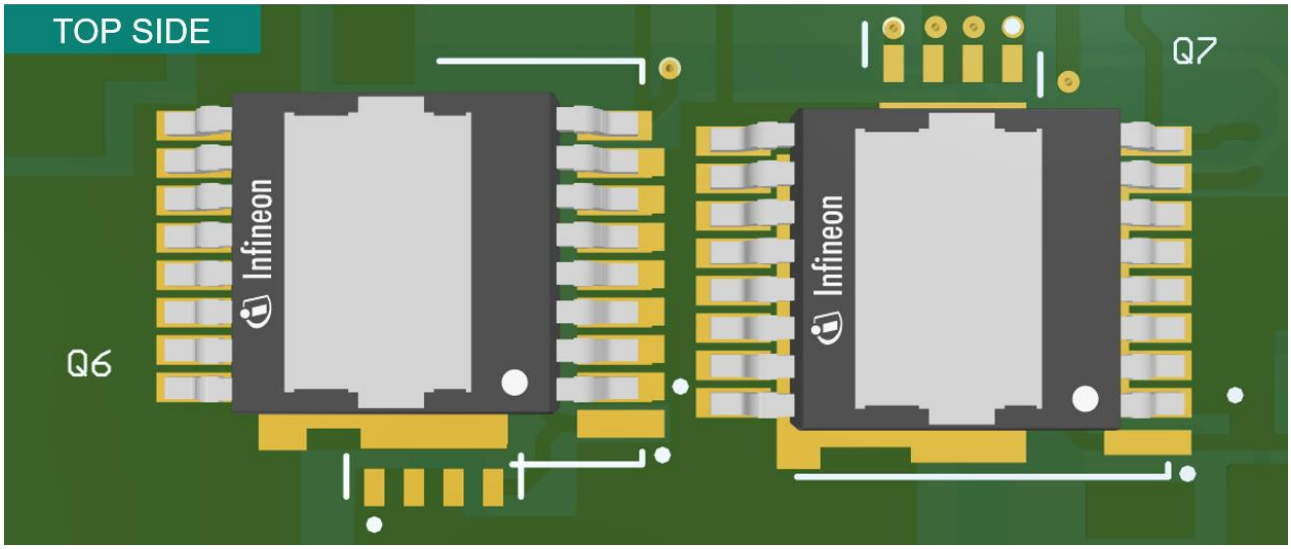

Figure 11 PG-HDSOP-16-2 package

5 System design

5.1 Schematics

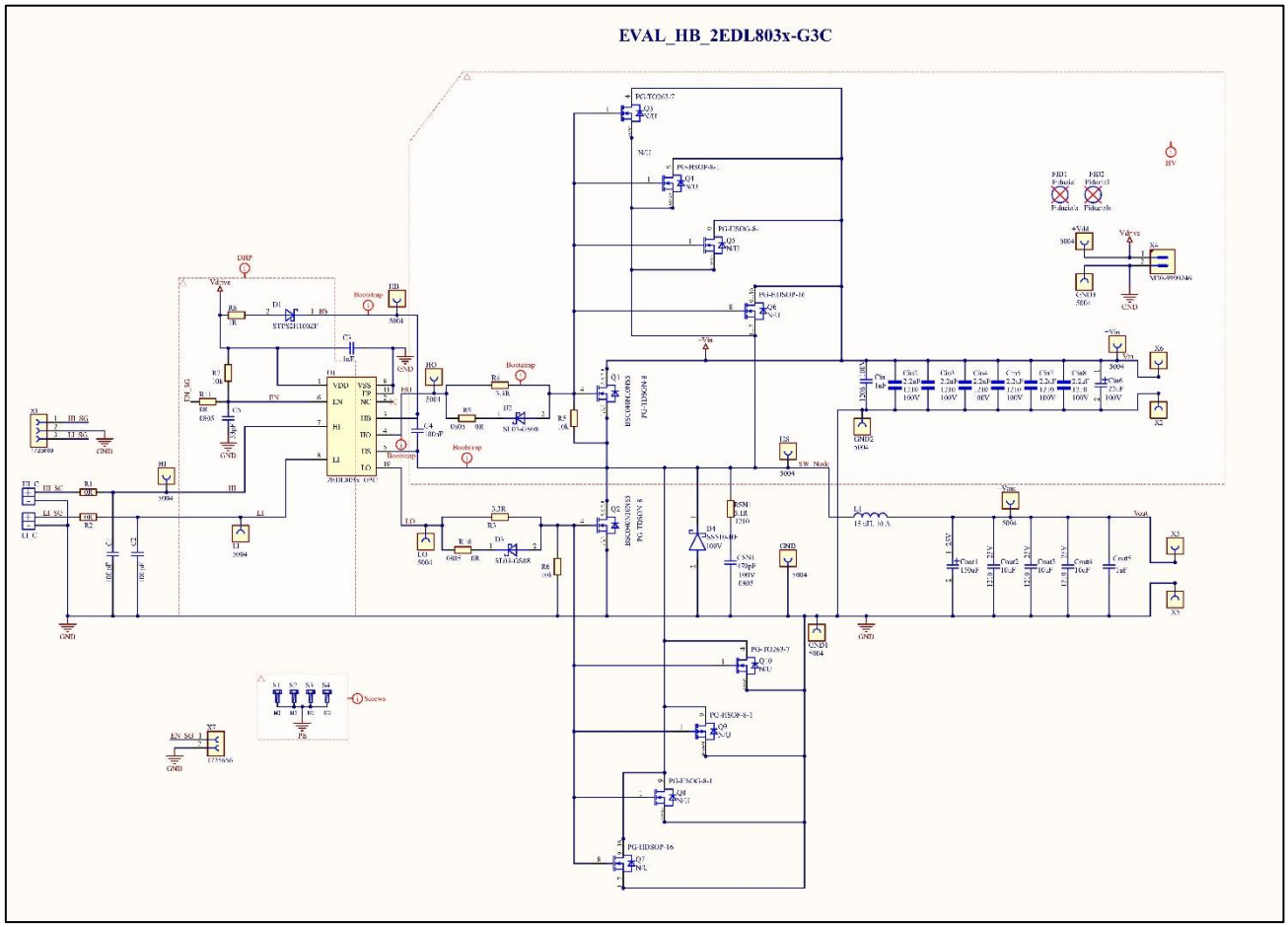

Figure 12 EVAL_HB_2EDL803x-G3C board schematic

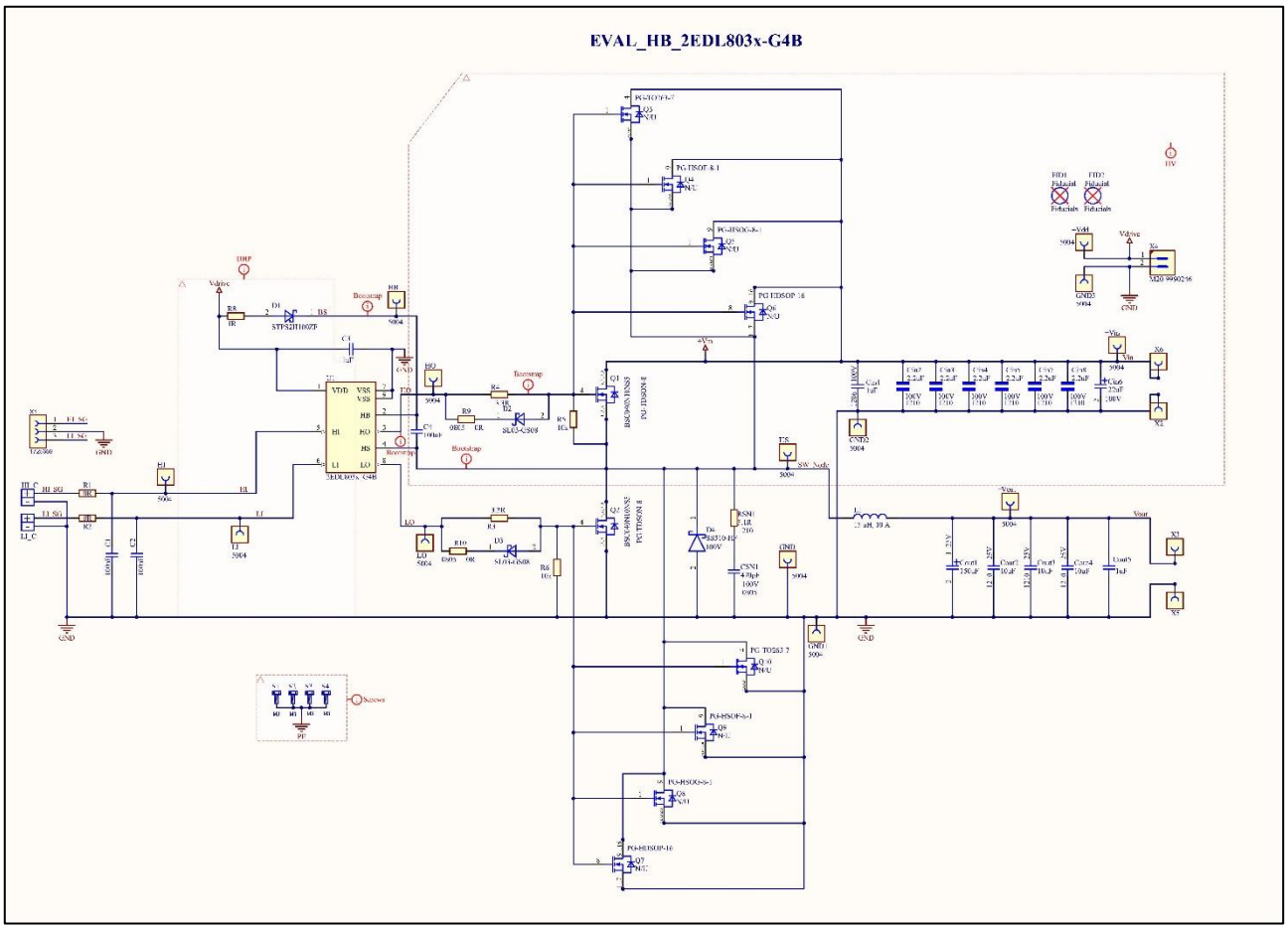

Figure 13 EVAL_HB_2EDL803x-G4B board schematic

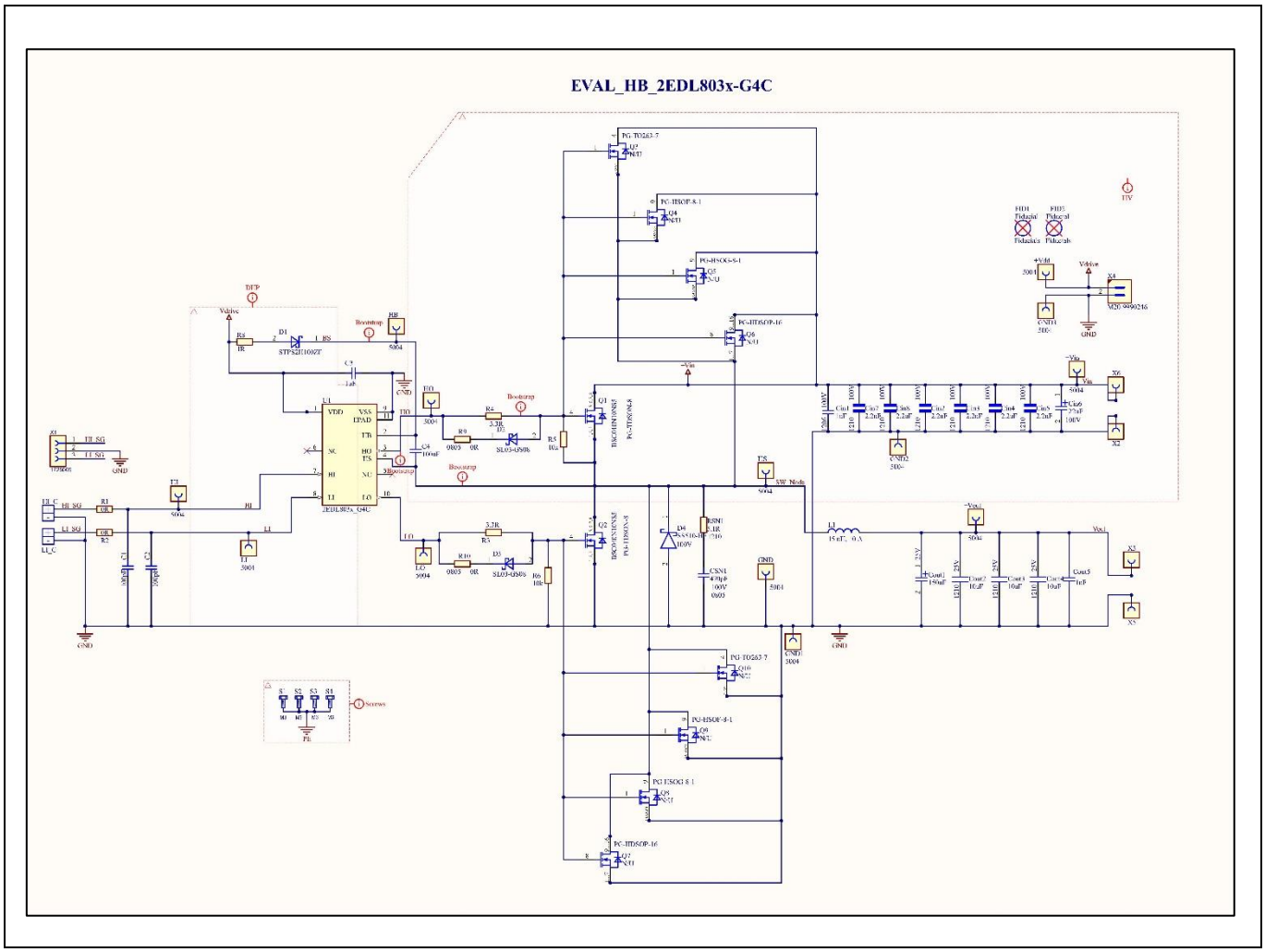

Figure 14 EVAL_HB_2EDL803x-G4C board schematic

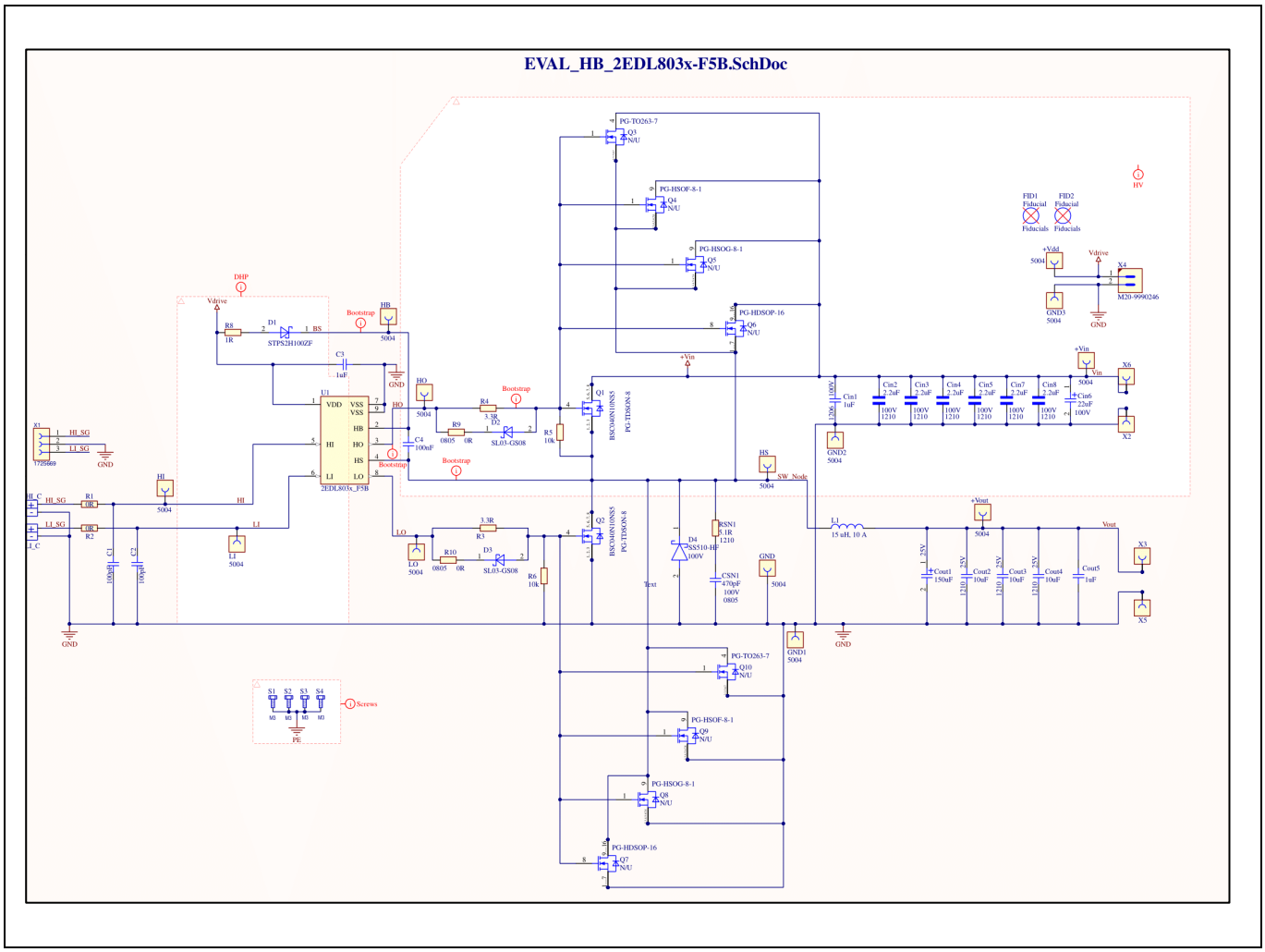

Figure 15 EVAL_HB_2EDL803x-F5B board schematic

5.2 Layout

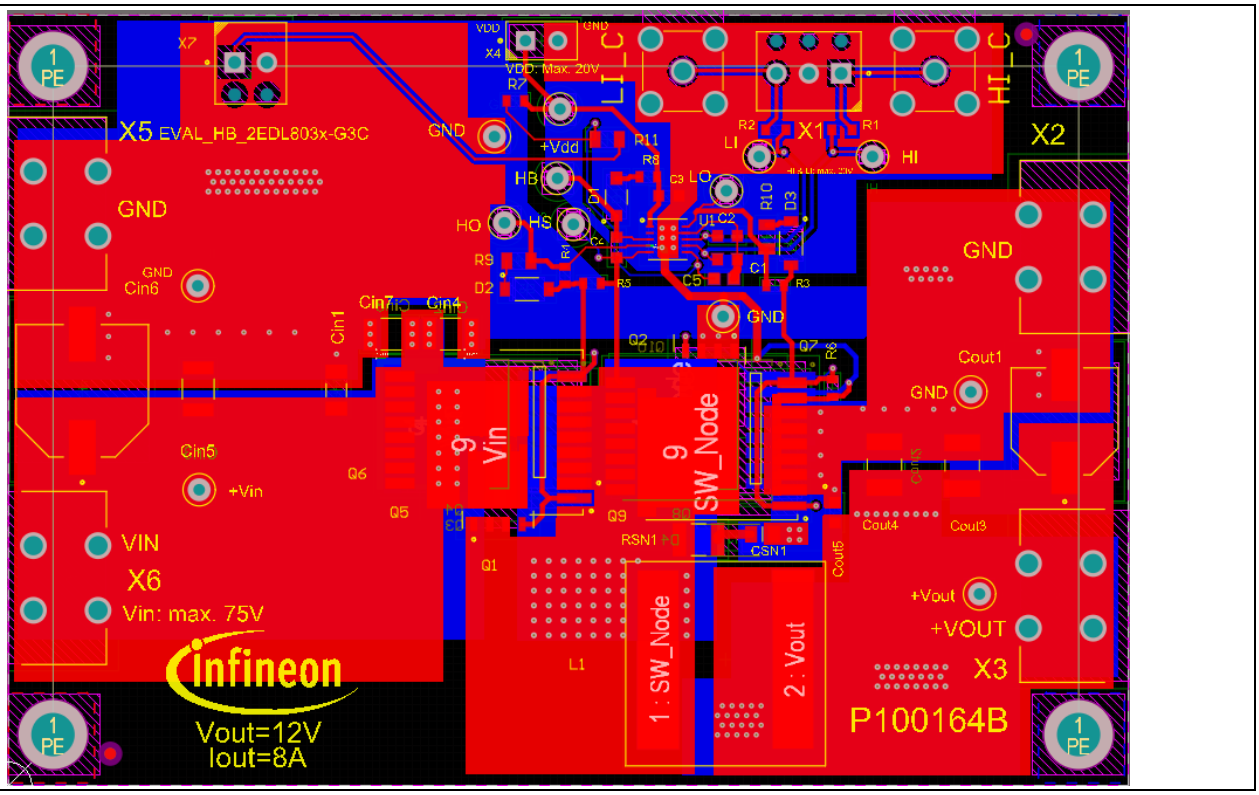

Figure 16 EVAL_HB_2EDL803x-G3C board layout

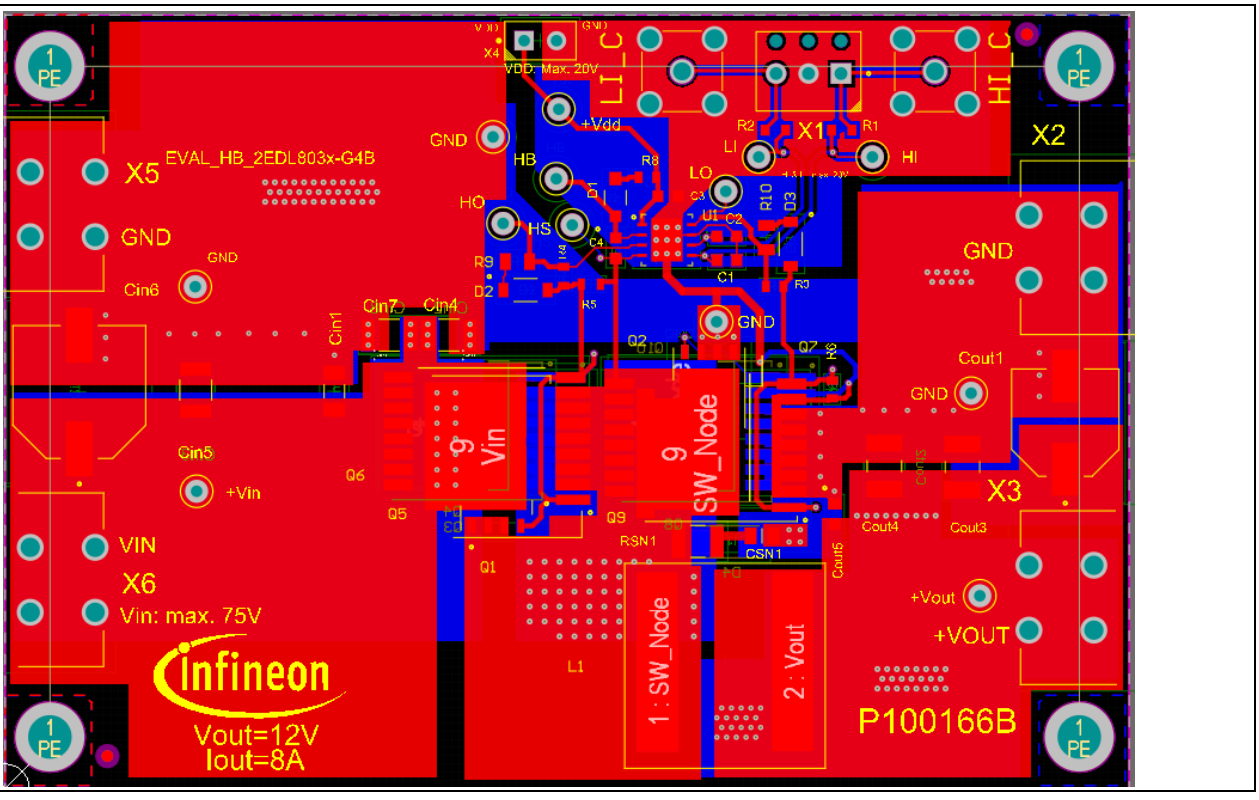

Figure 17 EVAL_HB_2EDL803x-G4B board layout

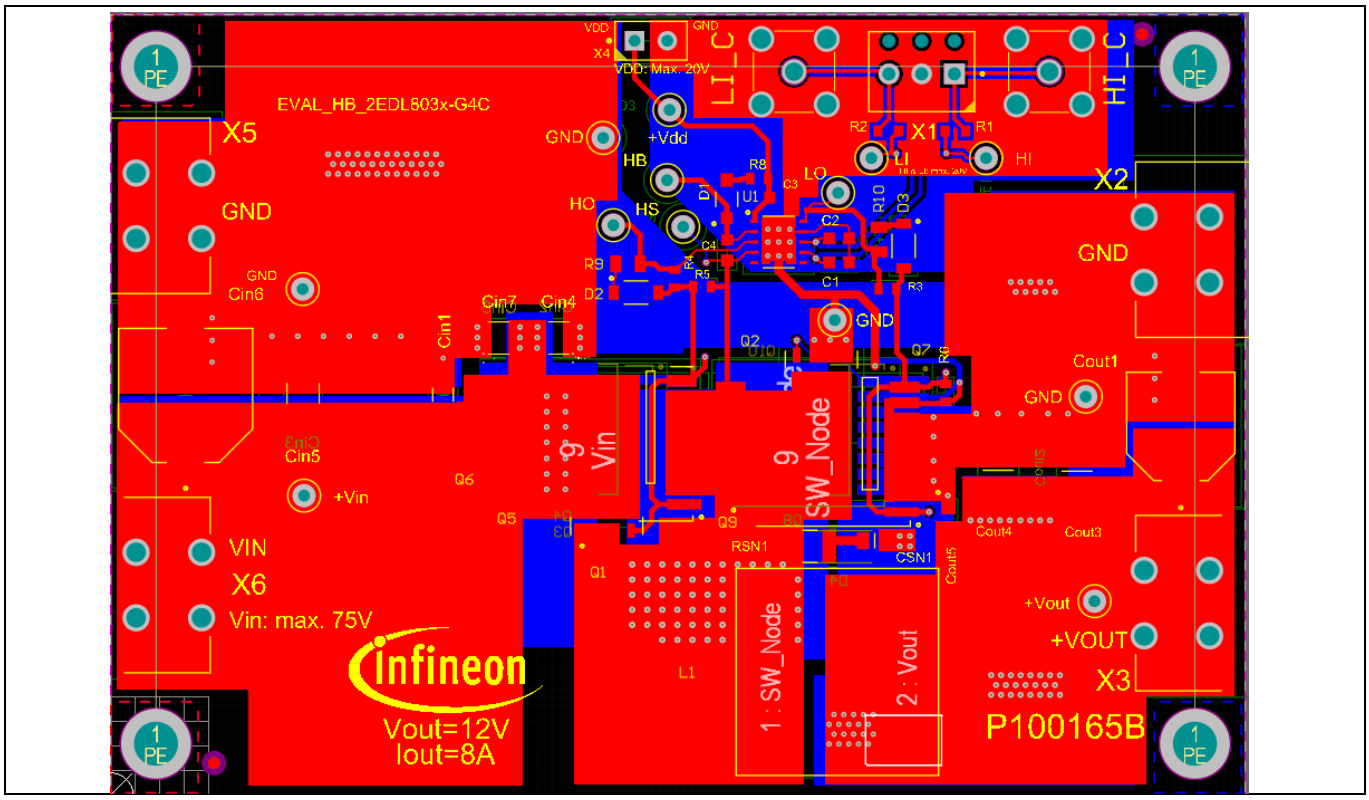

Figure 18 EVAL_HB_2EDL803x-G4C board layout

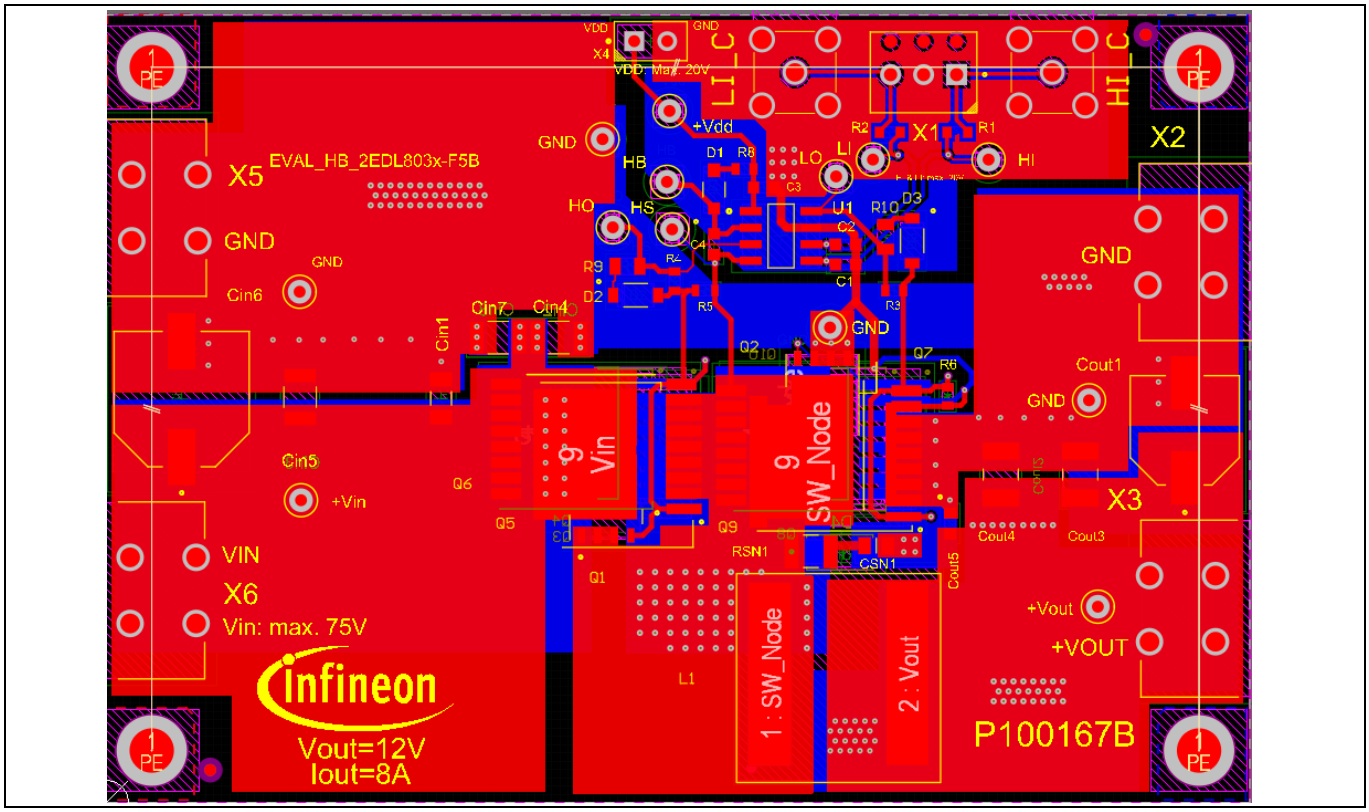

Figure 19 EVAL_HB_2EDL803x-F5B board layout

5.3 Bill of materials (BOM)

Table 6 EVAL_HB_2EDL803x board BOM

Designator	Value	Part Description	Package	Manufacturer	Manufacturer Order Number
+Vdd, +Vin, +Vout, GND, HB, HI, HO, HS, LI, LO, GND1, GND2, GND3	5004	Circuit Board Hardware - PCB TEST POINT YELLOW		Keystone	5004
C1, C2	100 pF	MLCC - X7R - 25V	0603	MuRata	C0603C101J3GACAUTO
C5*	33 pF	MLCC - X7R - 25V	0603	Kemet	C0603C330K3RACTU
C3, Cout5	1 µF	MLCC - X7R - 25V	0603	Samsung	CL10B105KA8VPNC
C4	100 nF	MLCC - X5R - 25V	CAPC1608X90N	Kemet	C0603C104K3PAC7867
Cin1	1 µF	MLCC - X7R - 100V	1206	MuRata	GRM31CR72A105KA01
Cin2, Cin3, Cin4, Cin5, Cin7, Cin8	2.2 uF	MLCC - X7R - 100V	1210	TDK Corporation	C3225X7R2A225K230AB
Cin6	22 µF	Al Polymer Cap	Radial: 10x12.6mm	Panasonic	100SXV22M
Cout1	150 µF	Al Polymer Cap	SMD	Kemet	A768KE157M1ELAE029
Cout2, Cout3, Cout4	10 µF	MLCC - X7R - 25V	1210	MuRata	GRM32DR71E106KA12K
CSN1	470 pF	MLCC - C0G - 100V	0805	MuRata	GRM219R72A471KA01
D1	STPS2H100ZF	Schottky Barrier Diode 100 V - 2 A	SOD123 Flat	STMicroelectronics	STPS2H100ZF
D2, D3	SL03-GS08	Schottky Diodes & Rectifiers 1.1A .395V	DO-219AB (SMF)	Vishay	SL03-GS08
D4	SS510-HF	Schottky Barrier Diode 100 V - 5 A	DO-214AC (SMA)	Comchip Technology	SS510-HF
HI_C, LI_C		RF Connectors / Coaxial Connectors SMA R/A JACK PCB DIECAST		Amphenol RF	132225
L1	15 µH	15 µH Shielded Drum Core, Wirewound Inductor 10 A 11.3 mΩ Nonstandard		Wuerth Elektronik	74439370150
Q1, Q2	BSC040N10NS5	OptiMOS5 Power-MOSFET 100V 4mΩ	PG-TDSON-8-1	Infineon Technologies	BSC040N10NS5
R1, R2	0R	Standard Thick Film Chip Resistor	0603	Yageo	AC0603FR-070RL
R3, R4	3.3R	General Purpose Chip Resistor	0603	Yageo	RT0603FRD073R3L
R5, R6, R7*	10K	Standard Thick Film Chip Resistor	0603	Yageo	RC0603FR-0710KL
R8	1R	Standard Thick Film Chip Resistor	0603	Vishay	CRCW06031R00FK
R9, R10, R11*	0R	Standard Thick Film Chip Resistor	0805	Yageo	RC0805FR-070RL, RC0805JR-070RL
RSN1	5.1R	Standard Thick Film Chip Resistor	1210	Panasonic	ERJ-14YJ5R1U
U1*	2EDL8034_G3C	EiceDRIVER™ 2EDL803x, Junction-Isolated High-Side and Low-Side gate driver IC	PG-VSON-10-4	Infineon Technologies	2EDL8034_G3C
X1	1725669	Fixed Terminal Blocks 3P 2.54mm 90DEG		Phoenix Contact	1725669
X5, X2	CT3151SP-0	Test Plugs & Test Jacks SafetyJack,Horz PCB, Black		Cal Test Electronics	CT3151SP-0
X3, X6	CT3151SP-2	Test Plugs & Test Jacks SafetyJack,Horz PCB, Red		Cal Test Electronics	CT3151SP-2
X4	M20-9990246	Headers & Wire Housings 02 SIL VERTICAL PIN HEADER TIN		Harwin	M20-9990246
X7*	1725656	Fixed Terminal Blocks 2P 2.54mm 90DEG		Phoenix Contact	1725656

*Note: For other eval boards, U1 used is the corresponding gate driver IC Package and C5, R7, R11 and X7 are not available

References

[1] Infineon Technologies AG: EiceDRIVER™ 2EDL803X datasheet; Available online

[2] Infineon Technologies AG: OptiMOS™ 5 100 V 4 mΩ BSC040N10NS5 product page; Available online

Revision history

Document revision	Date	Description of changes
V 1.0	2023-06-07	Initial release
V 1.1	2024-07-09	Added 2EDL803x-F5B

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