

About this document

Scope and purpose

This user guide explains how to set up the hardware and serves as a user manual for the EVAL_XDPP1140_1148_DB daughterboard. XDP™ XDPP1140-100B and XDP™ XDPP1148-100B belong to Infineon's XDP™ digital power controller family, optimized to provide a high level of performance and design flexibility for DC-DC converters. This controller is designed to achieve high efficiency, system control, and cost savings for applications such as telecom, server, data centers, and computing DC-DC solutions. The daughter board is designed to be used as a test and firmware development tool for XDPP1140 and XDPP1148. This document describes the configuration of various jumper pins based on the device, features, and applications.

Intended audience

This document is intended for power supply design engineers, system engineers, and embedded power designers.

Evaluation Board

This board is to be used during the design-in process for evaluating and measuring characteristic curves, and for checking datasheet specifications.

Note: PCB and auxiliary circuits are NOT optimized for final customer design.



Important notice

Important notice

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Safety precautions

Safety precautions

Note: Please note the following warnings regarding the hazards associated with development systems

Table 1	Safety precautions
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Warning: The DC link potential of this board is up to 1000 VDC. When measuring voltage waveforms by oscilloscope, high voltage differential probes must be used. Failure to do so may result in personal injury or death.



Warning: The evaluation or reference board contains DC bus capacitors which take time to discharge after removal of the main supply. Before working on the drive system, wait five minutes for capacitors to discharge to safe voltage levels. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.



Warning: The evaluation or reference board is connected to the grid input during testing. Hence, high-voltage differential probes must be used when measuring voltage waveforms by oscilloscope. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.



Warning: Remove or disconnect power from the drive before you disconnect or reconnect wires, or perform maintenance work. Wait five minutes after removing power to discharge the bus capacitors. Do not attempt to service the drive until the bus capacitors have discharged to zero. Failure to do so may result in personal injury or death.



Caution: The heat sink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.



Caution: Only personnel familiar with the drive, power electronics and associated machinery should plan, install, commission and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.



Caution: The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.



Caution: A drive that is incorrectly applied or installed can lead to component damage or reduction in product lifetime. Wiring or application errors such as undersizing the motor, supplying an incorrect or inadequate AC supply, or excessive ambient temperatures may result in system malfunction.



Caution: The evaluation or reference board is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials that are unnecessary for system installation may result in overheating or abnormal operating conditions.



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Introduction

1 Introduction

The EVAL_XDPP1140_1148_DB is a daughter board used for testing and programming the XDPP1140 and XDPP1148 VQFN 4 mm × 4 mm 24-pin version controller. This evaluation board allows you to configure hardware and software of the controller to evaluate its performance in DC-DC converter applications. You can also debug the controller, simulate various power stage conditions, and communicate through different communication protocols such as I2C, SPI, UART, and SWD.

EVAL_XDPP1140_1148_daughter board is developed to make XDPP1140 and XDPP1148 evaluation convenient, quick, and compatible with DC-DC power modules and other evaluation powerboard. It also offers the flexibility to develop and debug custom firmware patch. All the special purpose analog, digital, and general-purpose pins of XDPP1140 and XDPP1148 are easily accessible and configurable using this board. This includes communication and debug pins.

1.1 Features and applications

- Supports both XDPP1140 and XDPP1148 controllers for evaluation
- Configuration jumpers to put device in different modes and applications
- Dedicated I2C communication port for PMBus communication
- 10-pin JTAG SWD connector port for firmware debug
- LED indicators
- Loop connector test point to probe oscilloscope and clipper cable easily to the device
- Male header test points for all the pins of the microcontroller
- Additional auxiliary 1.8 V and 3.3 V supply on board
- DIP switch for creating I2C and PMBus address offset
- High speed mezzanine connectors to communicate with the powerboards



Hardware requirements

2 Hardware requirements

2.1 Board overview

A visual representation of an EVAL_XDPP1140_1148_DB is shown in Figure 1. As shown in the figure, the board is packed with various jumpers, test points, debugger port, and the IC. This board is powered with 3.3 V input. The board is designed for ease-of-IC evaluation with pins and test points spread based on the sides. Top and bottom sides of the board consist of various test points for all high speed analog and digital pins such voltage, current sense, and GPIOs. Left side consists of communication ports such as I2C, SPI, and JTAG. The connection for board's bias and address offset configuration are on the right side of the board. The central area of the board contains the device/microcontroller. Bottom side of the board consists high speed mezzanine connectors for connecting it to evaluation powerboards such as EVAL_1kW_LLC_XDPP1148.

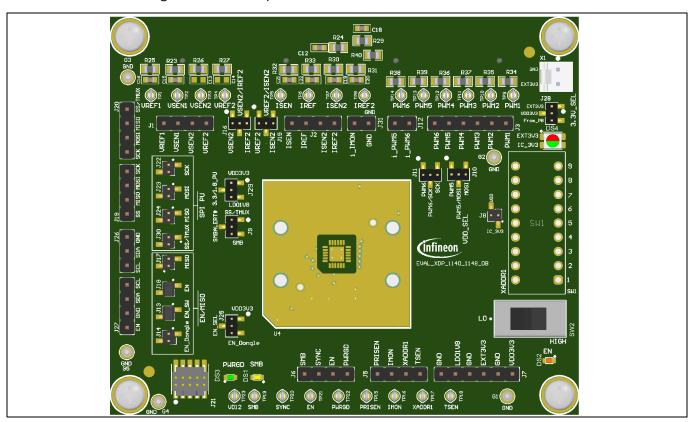


Figure 1 EVAL_XDPP1140_1148_DB Evaluation Board

There are two types of test points on the top and the bottom side.

- Regular male connector
- Hook-type probe connection, which makes connecting oscilloscope probes easy. See Section 2.2 for more information.

There are multiple small jumper connectors between the IC and test point. Their role is to change the device configuration for various applications. This board can be used for two different products, XDPP1140 and XDPP1148. It is also backward-compatible for the older generation XDPP1100-Q24.

XDPP1140 has two voltage sense and one current sense, whereas XDPP1148 has two current sense and one voltage sense. To accommodate both the ICs, jumpers are used. Another example is configuring analog and



Hardware requirements

digital GPIOs or multi-purpose pins on microcontroller for one specific application such as using PWM as a high-speed digital PWM or as a fast fault input pin or SPI communication pin. See the Section 2.3 for more details.

2.2 Pinout

As this board is designed to operate with two types of XDPP11XX controllers and provide backward compatibility with the older generation devices, it offers all the pins available on each microcontroller to sense and send signals.

Figure 2 shows a simplified version of the board, where only the main pins are shown. See for a detailed description of each pin.

Note:

Table 2 provides information about the default configuration of each pin. Many pins in the list are general purpose analog or digital pins and can be used for different purposes. See Table 2 for detailed information about the pins.

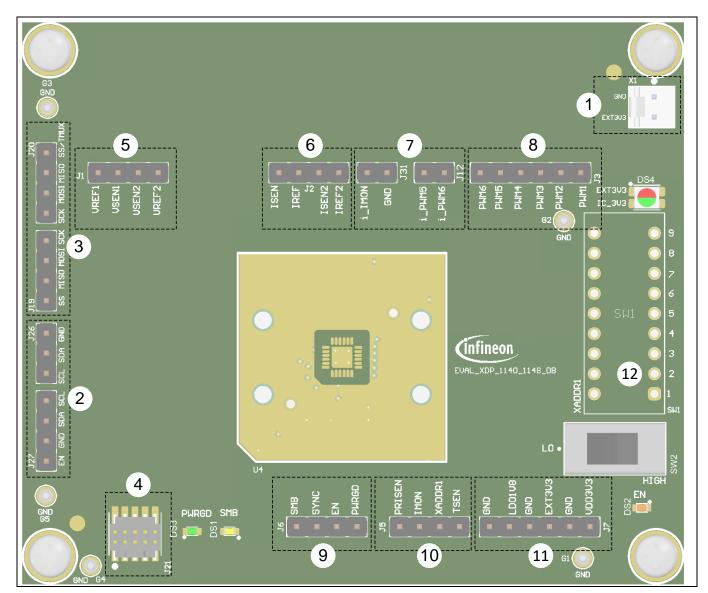


Figure 2 Board diagram with pin layout



Hardware requirements

Table 2 Primary pinout table for EVAL_XDPP1140_1148_DB

Number	Socket	Pins	Purpose/description
1	X1	EXT3v3	External DC power positive
	Power connector	GND	External DC power ground
2	J26-J27	SCL	Serial clock for I2C/PMBus
	I2C/PMBus connector	SDA	Serial data for I2C/PMBus
		GND	Ground connector for USB007 dongle
		EN	EN pin for USB007 dongle / 3.3V output pin for isolated USB007 dongle
3	J19-J20	SCK	Serial clock for SPI
	Connector for SPI communication	MOSI	Master out/Data out, Slave in pin for SPI
		MISO	Master in/ Data In, Slave out pin for SPI
		SS/TMUX	Slave select pin for SPI
4	J21 Debugger port	10-pin JTAG header	Port to connect JTAG or Lauterbach debugger
5	J1 Voltage sensing port	VREF1	Analog voltage sense reference voltage pin for VSEN_1 on XDPP1140 & XDPP1148
		VSEN1	Analog voltage sense voltage pin for voltage VSEN_1 on XDPP1140 & XDPP1148
		VREF2	Analog voltage sense reference voltage pin for VSEN_2 on XDPP1140 only
		VSEN2	Analog voltage sense voltage pin for VSEN_2 on XDPP1140 only
6	J2 Current sensing port	ISEN	Analog current sense voltage pin for ISEN on XDPP1140 and XDPP1148
		IREF	Analog current sense reference voltage pin for ISEN on XDPP1140 and XDPP1148
		ISEN2	Analog current sense voltage pin for ISEN on XDPP1148 only
		IREF2	Analog current sense voltage pin for ISEN on XDPP1148 only
7	J12	i_PWM5	To use PWM5 as an IMON disconnect pin for current sharing
		i_PWM6	To use PWM6 as an IMON disconnect pin for current sharing
	J31	i_IMON- GND	Short this 2 pin to connect 2.2K Ohm resistor to IMON pin for RC filter
8	J3	PWM1	Digital PWM1 output pin
	Digital PWM output port	PWM2	Digital PWM2 output pin
		PWM3	Digital PWM3 output pin
		PWM4	Digital PWM4 output pin
		PWM5	Digital PWM5 output pin



Hardware requirements

Number	Socket	Pins	Purpose/description
		PWM6	Digital PWM6 output pin
9	J6	SMB	SMB Alert pin
	General purpose Digital port	SYNC	Sync input/output pin
		EN	Enable pin
		PWRGD	PowerGood# pin
10	J5	PRISEN	Primary voltage sensing input
	General purpose Analog port	IMON	Output current monitor pin
		XADDR1	Address offset pin
		TSEN	External temperature sensing pin
11	J7	LDO1V8	1.8 V output from onboard LDO
	Power output port	VDD3V3	3.3 V bias voltage supply, it could be from X1 or from powerboard connected via high-speed mezzanine connectors
		EXT3V3	External 3.3 V from X1
		GND	Ground pin (All the ground pins are connected)
12	SW1 (DNP)	DIP Switch	DIP switch to create resistance for I2C and PMBus address offset

The XDPP11XX series devices are compact and feature-loaded devices. The PCB footprint makes it unique and most of the pins on the die can be used for multiple applications. See the datasheet [1] for more details.

2.3 Jumper configuration

EVAL_XDPP1140_1148_DB serves multiple purposes for evaluating XDPP1140 and XDPP1148 MCUs. To accommodate all the features of both IC and various important functionalities on a limited number of pins, function jumpers/application jumpers are used on the board. See Figure 3 for more information.

All the major function jumpers are placed inside the perimeter of main testing points and to distinguish visually, a small jumpers of pitch mating of 1.27 mm are used.

This section focuses on jumper configuration that helps to achieve certain configuration. Table 2 explains role of each jumper and its result on the application/ defining the purpose.

V 1.0



Hardware requirements

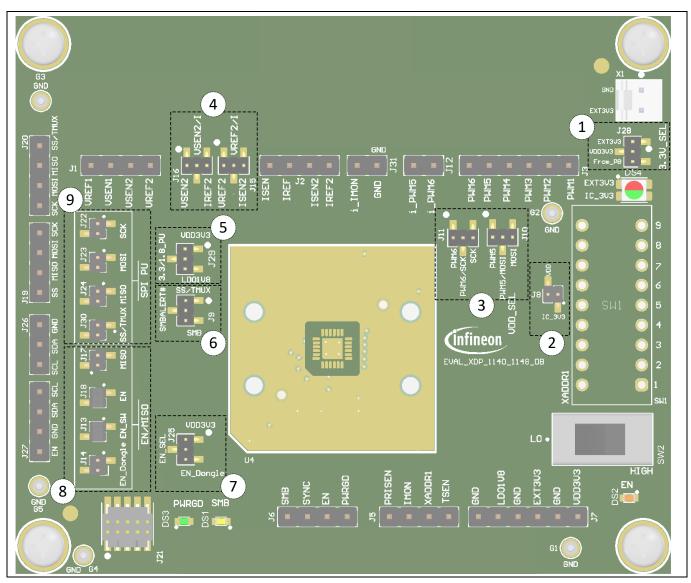


Figure 3 **Board diagram with function jumpers**

To understand role of each jumper configuration, see Table 3. Here, silk screen name is used for reference along with pin number. For more information on the pin numbers, see Section 4.1 for pin number.

Table 3 Jumper configuration table

No.	Jumper	Connection		Application/result
1	J28	VDD3V3	EXT3V3 (1)	To power IC externally
	3.3V_SEL	(2)	From_PB (3)	To power IC using powerboard
2	J8 VDD_SEL	VDD (2)	VDD3V3 (1)	Connector to measure current consumption of a microcontroller
3	J11	PWM6/SCK (2)	PWM6 (1)	To use pin as PWM6 output
	P6_SEL		SCK (3)	To use SCK pin for SPI
	J10	PWM5/MOSI (2)	PWM5 (1)	To use pin as PWM5 output
	P5_SEL		MOSI (3)	To use MOSI pin for SPI



Hardware requirements

No.	Jumper	Connection		Application/result
4	J16 VSEN2/IREF2	VSEN2/IREF2 (2)	VSEN2 (1)	To use pin as a voltage pin for VSEN_2 in XDPP1140
			IREF2 (3)	To use pin as a current reference voltage pin for ISEN_2 in XDPP1148
	J15 VREF2/ISEN2	VREF2/ISEN2 (2)	VREF2 (1)	To use pin as a reference voltage pin for VSEN_2 in XDPP1140
			ISEN2 (3)	To use pin as a current voltage pin for ISEN_2 in XDPP1148
5	J29	3.3/1.8_PU (2)	VDD3V3 (1)	To pullup SPI pin to 3.3V level
	3.3/1.8_PU		LDO1V8 (3)	To pullup SPI pin to 1.8V level
6	J9 SMB_SEL	SMBALERT#	SS/TMUX (1)	To use SMBALERT# as a Slave select OR TMUX*
			SMB (3)	To use SMBALERT# as regular SMBALERT# pin
7	J25	EN_SEL	VDD3V3(1)	To make 3.3V available for USB007B (isolated dongle)
	EN_SEL	(2)	EN_Dongle (3)	To control EN pin on the controller using XDPGUI + USB007 dongle
8	J13	EN_MISO (2)	EN_SW (1)	To control EN pin via switch on board
	J14		EN_DONGLE (1)	To control EN pin via dongle (need option7 to be connected)
	J17		MISO (1)	To use EN pin as a Master_In Slave_Out pin for SPI
	J18		EN (1)	To see value of EN pin on LED_2
9	J22	SPI_PU (2)	SCK	Pull up connector for SPI clock
	J23		MOSI_PU	Pull up connector for Master_Out Slave_in (Data out)
	J24		MISO_PU	Pull up connector for Master_In Slave_Out (Data in)
	J30		SS	Pull up connector for SPI Slave Select

2.4 Test points

Test points are convenient points to probe any of the signal on oscilloscope or logic analyzer or any other testing measurement machine (such as a digital multi-meter, voltage or current meter, or waveform generator).

EVAL_XDPP1140_1148_DB offers two types of test points, male header sockets and loop test points. Section 2.2 describes the first type of test points. This section describes the loop test points. Board offers five ground pins on each side of the board for easy ground pin connection.



Hardware requirements

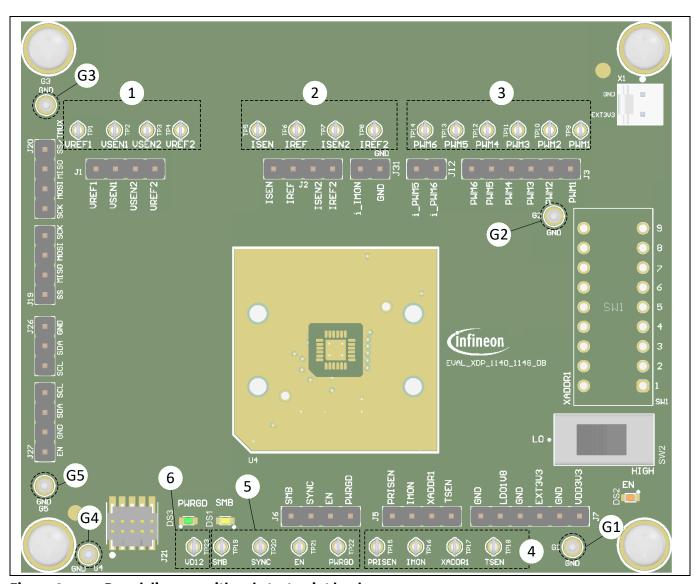


Figure 4 Board diagram with only test point hook

See Table 4 for detailed descriptions of the loop test points.

Table 4 Test point connection

No.	Test point group	TP number	Pin on microcontroller	Male header connectors
1	Analog voltage sensing	TP1	VREF1	J1 – VREF1
		TP2	VSEN1	J1 – VSEN1
		TP3	VSEN2 (only for XDPP1140)	J1 – VSEN2
		TP4	VREF2 (only for XDPP1140)	J1 – VREF2
2	Analog current sensing	TP5	ISEN	J2 – ISEN
		TP6	IREF	J2 – IREF
		TP7	ISEN2 (only for XDPP1148)	J2 – ISEN2
		TP8	IREF2 (only for XDPP1148)	J2 – ISEN2
3	Digital PWM output	TP9	PMW1	J3 – PWM1



Hardware requirements

No.	Test point group	TP number	Pin on microcontroller	Male header connectors
		TP10	PWM2	J3 – PWM2
		TP11	PWM3	J3 – PWM3
		TP12	PWM4	J3 – PWM4
		TP13	PWM5	J3 – PWM5
		TP14	PWM6	J3 – PWM6
4	General purpose analog pin	TP15	PRISEN	J5 – PRISEN
		TP16	IMON	J5 – IMON
		TP17	XADDR1	J5 – XADDR1
		TP18	TSEN	J5 – TSEN
5	General purpose digital pin	TP19	SMB	J6 – SMB
		TP20	SYNC	J6 – SYNC
		TP21	EN	J6 – EN
		TP22	PWRGD	J6 – PWRGD
6	Microcontroller bias test pin	TP23	VD12	N/A
7	Ground pins	G1	Ground	N/A
		G2	Ground	N/A
		G3	Ground	N/A
		G4	Ground	N/A
		G5	Ground	N/A

2.5 LED indicators

LEDs provide visual cues and are easy way to communicate with the system. EVAL_XDPP1140_1148_DB offers five LEDs as shown in Figure 5. It uses four LEDs for power and regulation status indication. See Table 5 for more details.



Hardware requirements

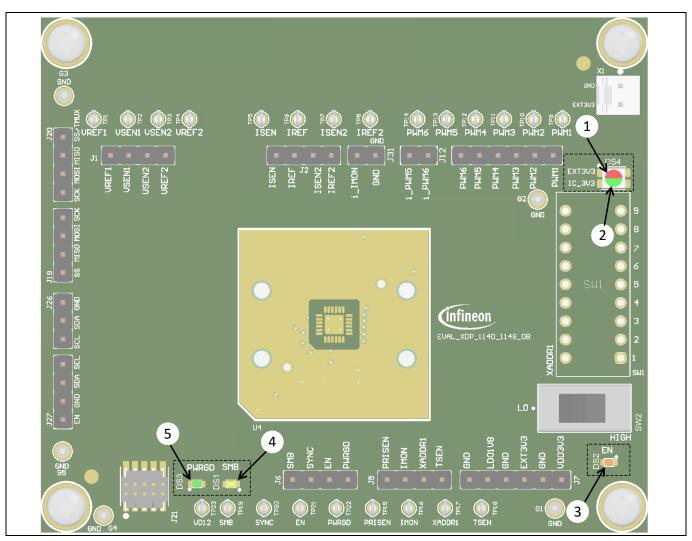


Figure 5 LED indicators

Table 5LED configuration table

No.	LED	Color	Signals	Light	Description
1-2	DS4	Dual	External power	Red ON	External voltage supply is present
		color	and	Red OFF	External voltage is not present
	IC bias	IC bias	Green ON	IC is biased	
				Green OFF	IC is not biased
3	DS2	Orange	EN	ON	EN is high
				OFF	EN is low
4	DS1	Yellow	SMBALERT#	ON	SMBALERT signal is LOW
				OFF	SMBALERT signal is High
5	DS3	Green	PWRGD	ON	Power Good is achieved
				OFF	Power Good is not achieved



Getting started

3 Getting started

3.1 Equipment requirements

To use any board, an interactive portal that allows changing the parameters for the device is necessary. Similarly, for EVAL_XDPP1140_1148_DB board, you need the XDP™ Designer GUI to interact with the board. Along with this, a medium that can communicate with the I2C/PMBus or SPI that the device on the board can understand is required.

Therefore, XDP™ Designer GUI and Infineon's USB006 or USB007 USB to I2C translator dongle are needed to communicate with XDPP1140 or XDPP1148.

3.2 Hardware setup

Connect the USB007 and EVAL_XDPP1140_1148_DB as shown in the Figure 6.

USB007 dongle has a standard USB-A port on one end and four cables for I2C/PMBus output on the other. As shown in the figure, it includes **SCL**, **SDA**, **GND**, and **EN** pin.

SCL and SDA are standard clock and data pin for I2C/PMBus protocol. GND is a ground pin for the EN pin reference. EN pin can be used as a control pin. You can set its value to either of the following:

- 0 V representing logic 0 to the device
- 3.3 V representing logic level 1 on the line

Note:

- 1. The dongle has one switch inside the plastic housing, which controls the voltage logic level for I2C/PMBus. By default, it is set to 3.3 V. It can be used to change pull up to either 1.8 V or 3.3 V.
- 2. In this Figure 6, USB007A is a non-isolated version of a dongle. With the isolated version (USB007B), there is no output voltage on the EN pin. You need to supply 3.3 V on the EN pin for the isolated side pull up.

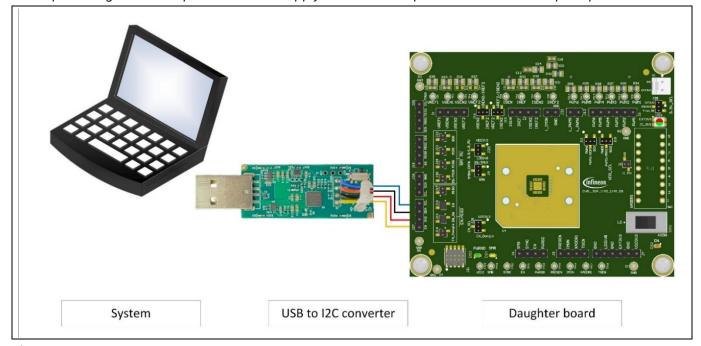


Figure 6 Hardware setup



Getting started

3.3 Software setup

As described in Section 3.1, you can download and install the software XDP™ Designer GUI and the drivers for the UBS007X dongle from the Infineon Development Center. To install the XDP™ Designer GUI and install the drivers from the Infineon development center, perform the following steps.

- 1. Search for **XDP Designer** in the search bar or use alphabet shortcut to jump to letter "X".
- Select the latest version from the **Version** dropdown and click **Install**.
 This downloads the GUI and installs it. It will automatically select the path for installation. Keep the default recommended path.

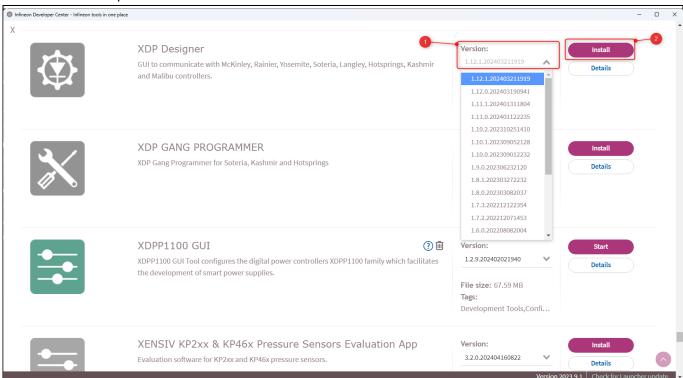


Figure 7 Download XDP™ Designer GUI

Once the installation is complete, the installation of the drivers for USB007/USB006 begins and you will see installation wizard shown in Figure 8.

3. Click **Next** to download the required files and drivers for the dongle.



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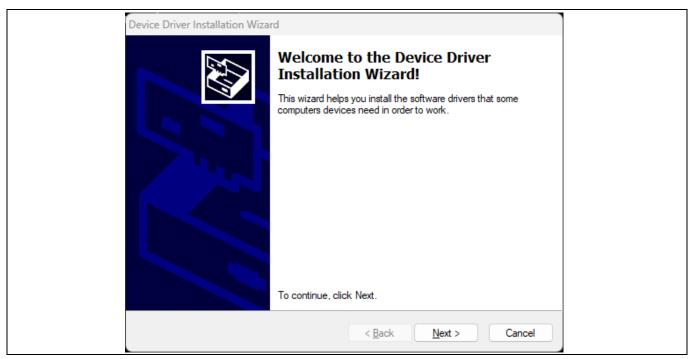


Figure 8 Driver installation

Once installation is complete for both the GUI and driver, a pop up a message confirms the completion. Now, you can go to **My Tools** and it will show **XDP Designer GUI** and any other GUI that is installed.

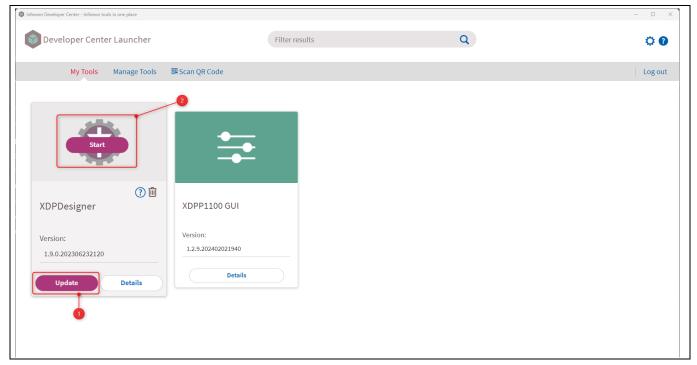


Figure 9 Update and open XDPDesigner

As shown in Figure 9, when a new **update(1)** for the GUI is available, it shows an option to update it. Updating the version will not uninstall the older version and you will have access to both new and older version.

Once the latest version is installed, hover your mouse on the GUI and click **Start(2)**.



Getting started

Once GUI is open, it will detect the dongle first and then scan for the connected device. See the XDP Designer GUI download guide for information.

Note: You will need the license file to access the GUI, get it from MyICP or contact Infineon support.

3.4 Testing

You can perform tests with or without the powerboard. The following sections describes the tests that can be performed.

3.4.1 Testing with the powerboard

This board is designed to test powerboards such as LLC powerboard. The hardware connections are described below.

- High-speed mezzanine connectors are used to provide strong, reliable, and high speed connection with MCU.
- Power up the MCU from the board power by changing J28 connector to *From_PB* pin.

See Section 4.1 for more information about these connections. Jumper configurations for this test are available in Table 6.

Table 6 Pin configuration for testing with powerboard

Jumper	Connection	Purpose
J28	VDD - EXT3V3	Powerup the board with external voltage
J8	VDD - IC_3V3	Power up the IC with 3.3 V
J16	VSEN2/IREF2 – IREF2	Configuration for XDPP1148 with second current sense in use
J15	VREF2/ISEN2 – ISEN2	Configuration for XDPP1148 with second current sense in use
J11	PWM6/SCK – PWM6	To use PWM6 as a PWM6
J10	PWM5/MOSI – PWM5	To use PWM5 as a PWM5
J9	SMBALERT# - SMB	To use SMBALERT pin as a SMBALERT#
J25	EN_SEL - EN_Dongle	To use EN pin from dongle to control my operation ON/OFF
J14	EN_Dongle	Activate connection of EN_Dongle to EN pin from J27
J18	EN	Connect EN_Dongle to EN LED

After these connections, you can power up the board. For this demonstration, a EVAL_LLC_XDPP1148 powerboard is used.

The hardware connections are shown in Figure 13.



Getting started

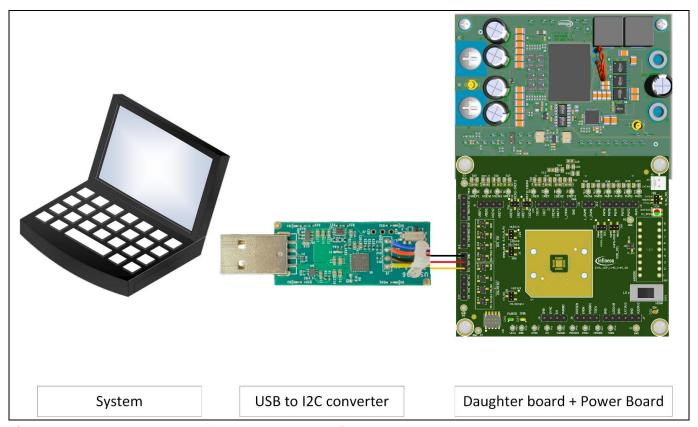


Figure 10 Hardware setup for powerboard testing

Once the hardware is setup, you can load the configuration and patch file to the device and turn on the operation. For more details on loading configuration and patch, see the XDPGUI help file or user guide for EVAL_LLC_XDPP1148.

3.4.2 Testing without the powerboard

Another important application of this evaluation board is to test the device without the powerboard so that you can develop configuration files or firmware patch without damaging the actual powerboard.

For testing the device without the powerboard, use the following connection of jumper to make device online with external power. This includes various tests like open-loop testing, close-loop testing, PWM observation, deadtime setting, multi-device sync test, current sharing test, and many more.

The setup for the two main applications are explained below.

3.4.2.1 Emulating the close loop operation

One important feature of this board is that it can replicate certain conditions such as emulating output and input voltage and current. You can also create various fault conditions (such as undervoltage, short circuit, etc.,) and see how the device and firmware behave in these conditions.

Use the jumper configuration given in Table 7 for this test.



Getting started

 Table 7
 Pin configuration for emulating the close loop operation

Jumper	Connection	Purpose	
J28	VDD-EXT3V3	Powerup the board with external voltage	
J8	VDD-IC_3V3	Powerup the IC with 3.3 V	
J16	VSEN2/IREF2-VSEN2	Configuration for XDPP1140 with 2 nd voltage sense in use	
J15	VREF2/ISEN2-VREF2	Configuration for XDPP1140 with 2 nd voltage sense in use	
J11	PMW6/SCK-PWM6	To use PWM6 as a PWM6	
J10	PWM5/MOSI-PWM5	To use PWM5 as a PWM5	
J9	SMALERT#-SMB	To use SMALERT pin as a SMBALERT#	
J25	EN_SEL-EN_Dongle	To use EN pin from dongle to control operation ON/OFF	
J14	EN_Dongle	Activate connection of EN_Dongle to EN pin from J27	
J18	EN	Connect EN_Dongle to EN_LED	

After configuring the jumpers on the board, connect the external power supply for emulating input and output voltage and current as shown in the following figure.



Getting started

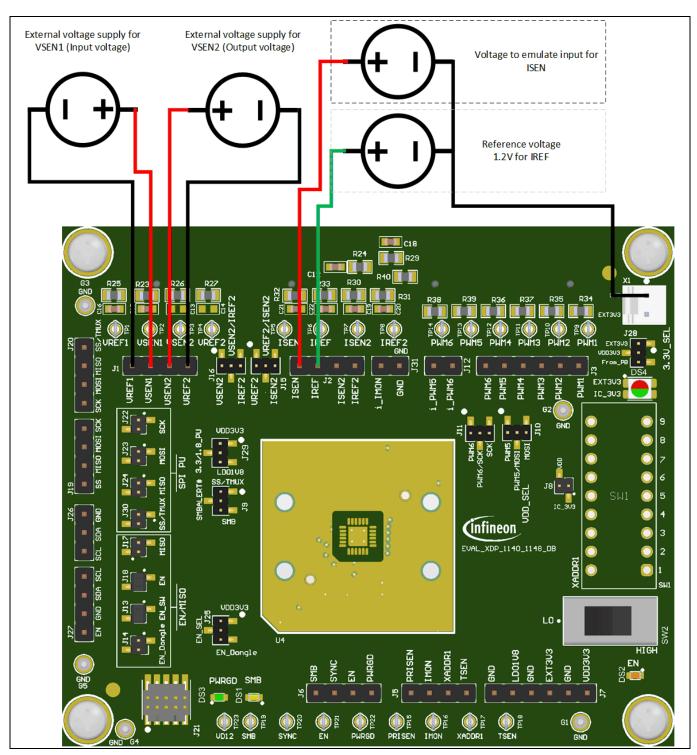


Figure 11 Hardware setup for emulating input, output voltage, and current

As shown in the figure, connect the different voltage supplies to VSEN1-VREF1 and VSEN2-VREF2 pin.

Based on the scale loop value, you can set its value anywhere between 0-2.1 differential voltage. For current sense, XDPP1140 and XDPP1148 have a differential current sense module. Hence, you must provide a separate 1.2 V reference voltage for IREF.

Note: Ensure that the ground for all the external power supply is connected together with device's ground.



Getting started

Once the hardware setup is ready, use the standard configuration files provided with XDPGUI (such as FBFB config file) to load to the device. Once the configuration is ready, proceed to turn on the application.

You can slowly increase the input and output voltage to see the device trying to control/balance the loop in case it is set for close-loop operation.

3.4.3 Multiple boards in Sync

Another application is to use the Sync feature available in XDPP1140 and XDPP1148. When two or more devices are used for any application you may need to sync both the devices switching frequency, then this application is useful. For this, hardware setup is the simple, just connect SYNC pin from the two daughter boards together.

For this application, you can again use example configuration such as FBFB configuration file. One device will work as a master, sending the SYNC signal out and another device will work as a slave device getting SYNC signal in from the master.

Use the Sync Configuration design tool from **Advanced** design tool to configure for both master and slave. See the XDPGUI user guide for more information.

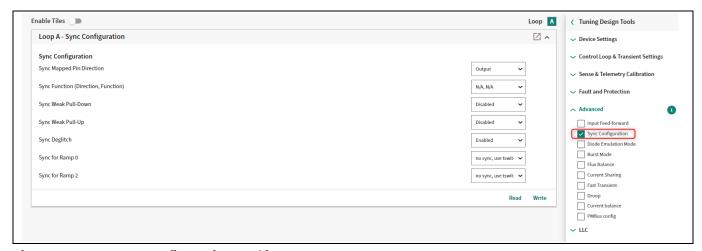


Figure 12 SYNC configuration tool in XDP GUI



System design details

4 System design details

4.1 Schematics

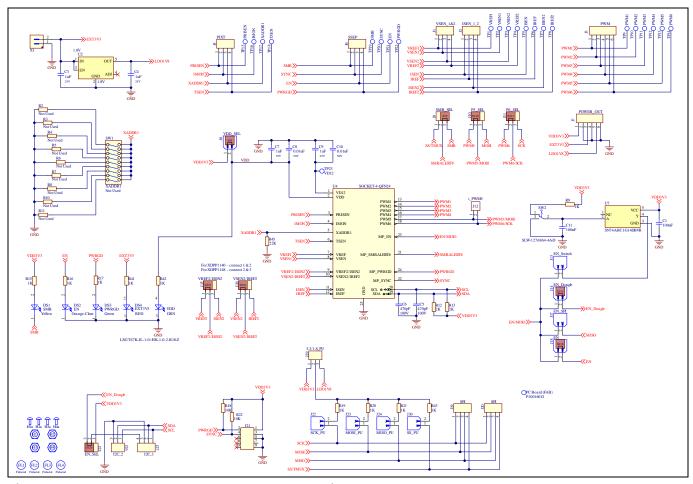


Figure 13 EVAL_XDPP1140_1148_DB schematic

V 1.0



System design details

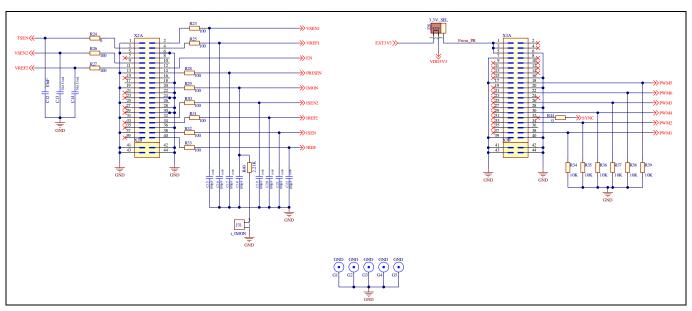


Figure 14 EVAL_XDPP1140_1148_DB schematic

4.2 Bill of materials

Table 8 BOM of the most important/critical parts of the evaluation or reference board

Designator	Quantity	Value	Manufacturer	Part number
C1	1	100 nF	Kyocera	KAE15AR71H104KT24
C3, C4, C7,C9	4	1 μF	TDK	C1608X7R1E105K080AB
C5, C6	2	470 pF	TDK	C1608C0G2A471K080AA
C8, C10	2	0.01 μF	TDK	C1608X7R1H103K080AA
C11, C12	2	100 nF, 10 nF	TDK	C1608C0G2A103J080AC
C13, C14	2	Not used	AVX	Not used
C15, C16,C17,C18,C19,C20,C21, C22	8	100 pF	TDK	C1608C0G2A101K080AA
DS1	1	Yellow	Wurth	150060YS75000
DS2	1	Orange-Clear	Rohm Semiconductor	SML-311DTT86
DS3	1	Green	Wurth	150060GS75000
DS4	1	GREEN/RED CLEAR	ams-OSRAM USA	LSG T67K-JL-1-0+HK-1-0- 2-R18-Z
G1, G2, G3, G4, G5	5	PIN42	Vector	K31C/M
H1, H2, H3, H4	4	Standoff	Keystone	2203
H1a,H2a,H3a,H4a	4	Screw 4-40 x 1/4	Keystone	9900
J1,J2,J5,J6,J19,J20,J27	7	CON4	Wurth	61300411121
J3,J7	2	PWM, POWER_OUT	Wurth	61300611121
J8,J13,J14,J17,J18,J22,J2 3,J24,J30	9	CONN SMD 2POS	Sullins	GRPB021VWTC-RC



System design details

Designator	Quantity	Value	Manufacturer	Part number
J9,J10,J11,J15,J16,J25,J2 8,J29	8	CON3	Sullins	GRPB031VWTC-RC
J12,J31	2	CON2	Wurth	61300211121
J21	1	SMD_CON10	Samtec	FTSH-105-01-L-DV-007-K
J26	1	CONN3	Wurth	61300411121
R2	1	Not used	Panasonic	Not used
R3	1	Not used	Panasonic	Not used
R4	1	Not used	Panasonic	Not used
R5	1	Not used	Panasonic	Not used
R6	1	Not used	Panasonic	Not used
R7	1	Not used	Panasonic	Not used
R8	1	Not used	Panasonic	Not used
R9,R15,R16,R19,R20,R21,R 41,R42,R43	9	1K	Panasonic	ERJ-6ENF1001V
R10	1	Not used	Panasonic	Not used
R11	1	Not used	Panasonic	Not used
R12,R13	2	2K	Panasonic	ERJ-6ENF2001V
R17	1	1K	Panasonic	ERJ-6ENF1002V
R18,R22,R34,R35,R36,R37, R38,R39	8	10K	Panasonic	ERJ-6ENF1002V
R23,R25,R26,R27,R28,R29, R30,R31,R32,R33	10	100,	Panasonic	ERJ-6ENF1000V
R24	1	0	Panasonic	ERJ-6ENF1000V
R40	1	2.21K	Panasonic	ERJ-6ENF2211V
R44	1	0	Panasonic	ERJ-3GEY0R00V
R45	1	22K	Panasonic	ERJ-6ENF2202V
SW1	1	Not used	CTS	Not used
SW2	1	SLW-1276864-4A-D	CUI Devices	SLW-1276864-4A-D
TP1,TP2,TP3,TP4,TP5,TP6 ,TP7,TP8,TP9,TP10, TP11,TP12,TP13,TP14,TP 15,TP16,TP17,TP18, TP19,TP20,TP21,TP22,TP 23	23	loop	Keystone	5020
U2	1	1.8 V	TI	TLV70018DDCR
U7	1	1 bit Inverter	TI	SN74AHC1G14DBVR
X1	1	640456-2	TE Connectivity	640456-2
X2,X3	2	QTE-020-01-L-D-A	Samtec	QTE-020-01-L-D-A
XJ8,XJ9,XJ10,XJ11,XJ14,X J15,XJ16,XJ18,XJ25,XJ28	10	Con Jumper	Sullins	NPB02SVFN-RC



References

References

Contact Infineon support for the documents

[1] Infineon technologies: XDPP11XX series datasheet



Glossary

Glossary

DB

Daughter Board (DB)

GUI

Graphical User Interface (AAUI)

PCB

Printed Circuit Board (PCB)

PMRIIS

Power Management Bus protocol (PMBus)

I2C

Inter-Integrated Circuit (I2C)

SWD

Serial Wire Debug (SWD)

JTAG

Joint Test Action Group protocol (JTAG)



Revision history

Revision history

Document revision	Date	Description of changes
V 1.0	2024-10-10	Initial release

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Edition 2024-10-10 Published by

Infineon Technologies AG 81726 Munich, Germany

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Document reference UG211531

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