XDP™ XDP711-001 evaluation PCBA user guide

About this document

Scope and purpose

This document describes how to set up the XDP™ XDP711-001 Evaluation Board and configure the internal registers to evaluate the performance of the XDP711-001 hot-swap controller for positive rail.

Intended audience

This document is intended for test engineers who want to evaluate the performance of the XDP711-001 hot-swap controller.

Important notice

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Safety precautions

Note: Please note the following warnings regarding the hazards associated with development systems

Table 1 Safety precautions

	**Warning**: *The evaluation or reference board contains DC bus capacitors which take time to discharge after removal of the main supply. Before working on the drive system, wait five minutes for capacitors to discharge to safe voltage levels. Failure to do so may result in personal injury.*
	**Caution:** *The heat sink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.*
	**Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	**Caution:** *The evaluation or reference board is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials that are unnecessary for system installation may result in overheating or abnormal operating conditions.*

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1 Introduction

The XDP™ XDP711-001 power controller is the latest addition to the XDP™ digital hot-swap family with several other new features and improvements compared to XDP™ XDP710-002. Infineon digital hot-swap power controllers are highly integrated wide-input-voltage system monitoring and protection devices, which are digitally configurable and use a power management bus (PMBus®) communication interface to access their register map to configure the features.

The USB010 series dongle is a PC-USB COM port to PMBus® bridge dongle that allows access to the XDP711-001 (compatible with other XDP7xx devices) registers from the PC software configurator.

This document describes how to set up the evaluation board and configure the internal registers to evaluate the performance of XDP711-001 to limit inrush current (regulation on programmed FET safe operating area (SOA)) during startup and highlights the fault detection and control.

2 Hardware and software requirements

The following hardware and software are required for the setup:

- XDP711-001 Evaluation Board (Order code: EVAL_XDP711)
- XDP™ Designer USB dongle USB007 or higher (**Order code**: USB0010)
- XDP™ Designer graphical user interface (GUI)

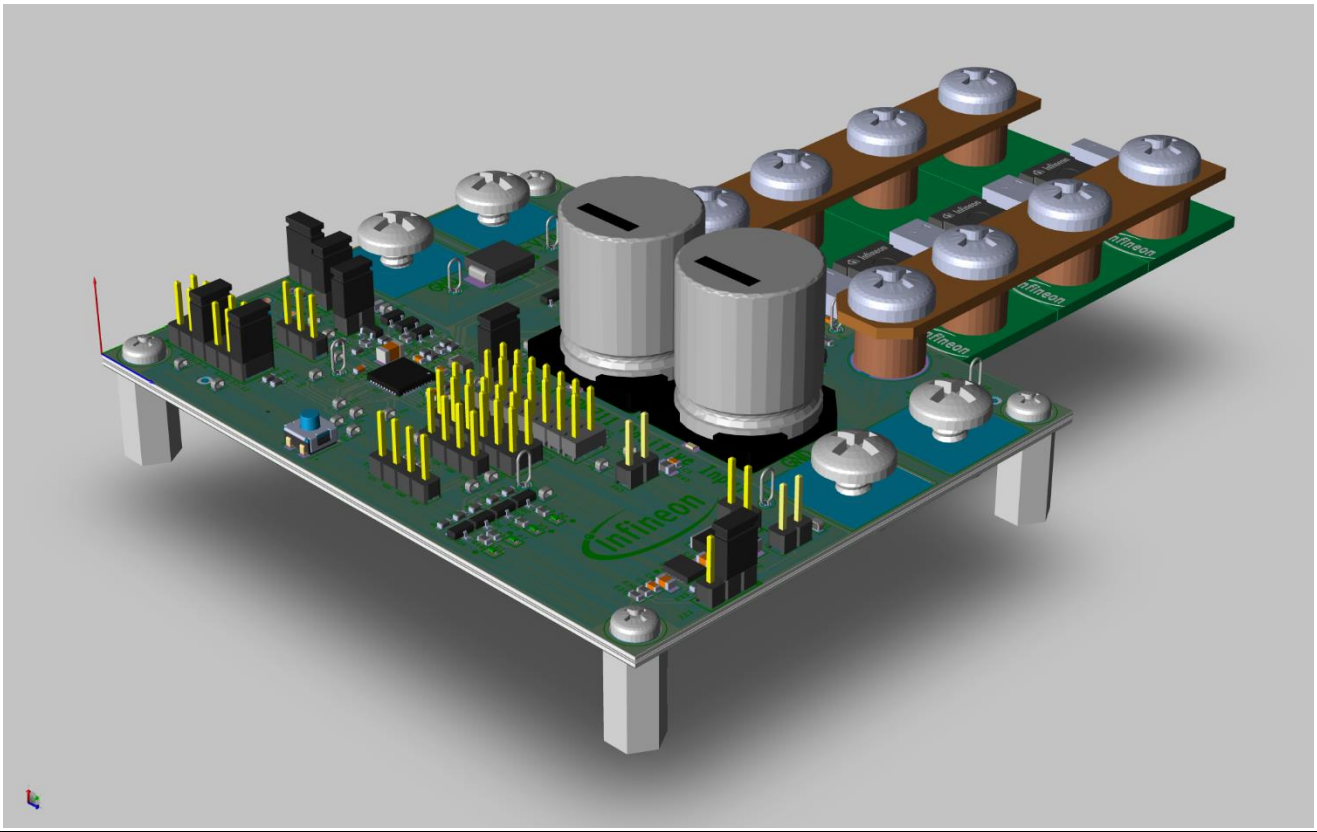


Figure 1 XDP711-001 Evaluation Board



Figure 2 USB0010 dongle

Hardware and software requirements

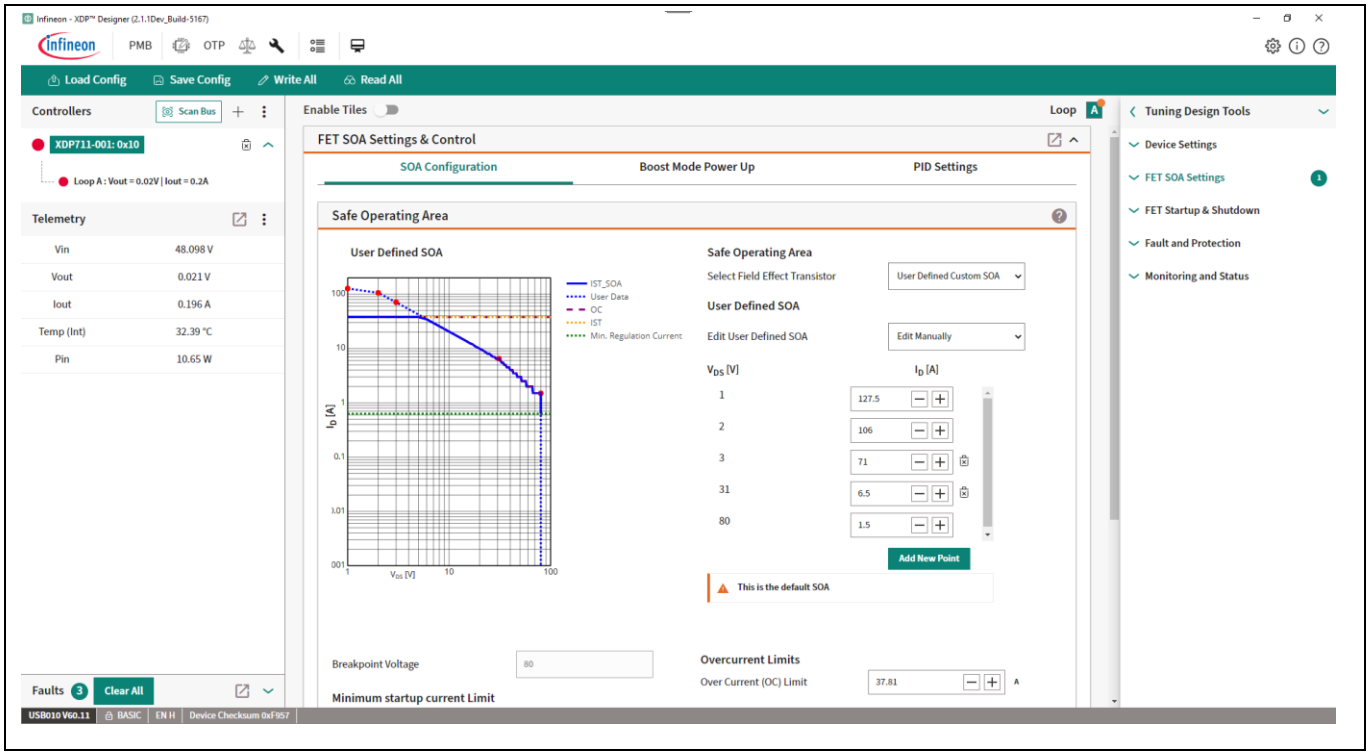


Figure 3 XDP™ Designer GUI

3 XDP711-001 evaluation platform

The following sections describe the XDP711-001 Evaluation Board highlighting the electrical specifications, block diagram, schematics, layout, bill of materials (BOM), and different configuration settings that could be used on this evaluation board.

3.1 Electrical specifications

- Input and output voltage range: 12 V DC to 80 V DC
- Verified current: 75 A

Note: For more current, increase the number of FETs. The MOSFET adapter boards can be removed and added to the evaluation board based on the required current level.

3.2 Block diagram

The XDP711-001 evaluation platform consists of:

- **XDP711-001 Evaluation Board**: Positive input hot-swap controller and its circuitry designed to run a single-channel controller including its corresponding FET. Additionally, communication, control, and protection circuitry are included
- **USB010 dongle**: The interface between the PC and XDP711-001 that communicates via the USB dongle. The commands are sent by the XDP™ Designer GUI to the XDP711-001 device, which are received via the PMBus® communication. The USB0010 dongle translates from USB to PMBus®
- **XDP™ Designer GUI**: Software GUI tool for XDP711-001 PMBus® communication that provides commands for configuration and general control

XDP711-001 evaluation platform

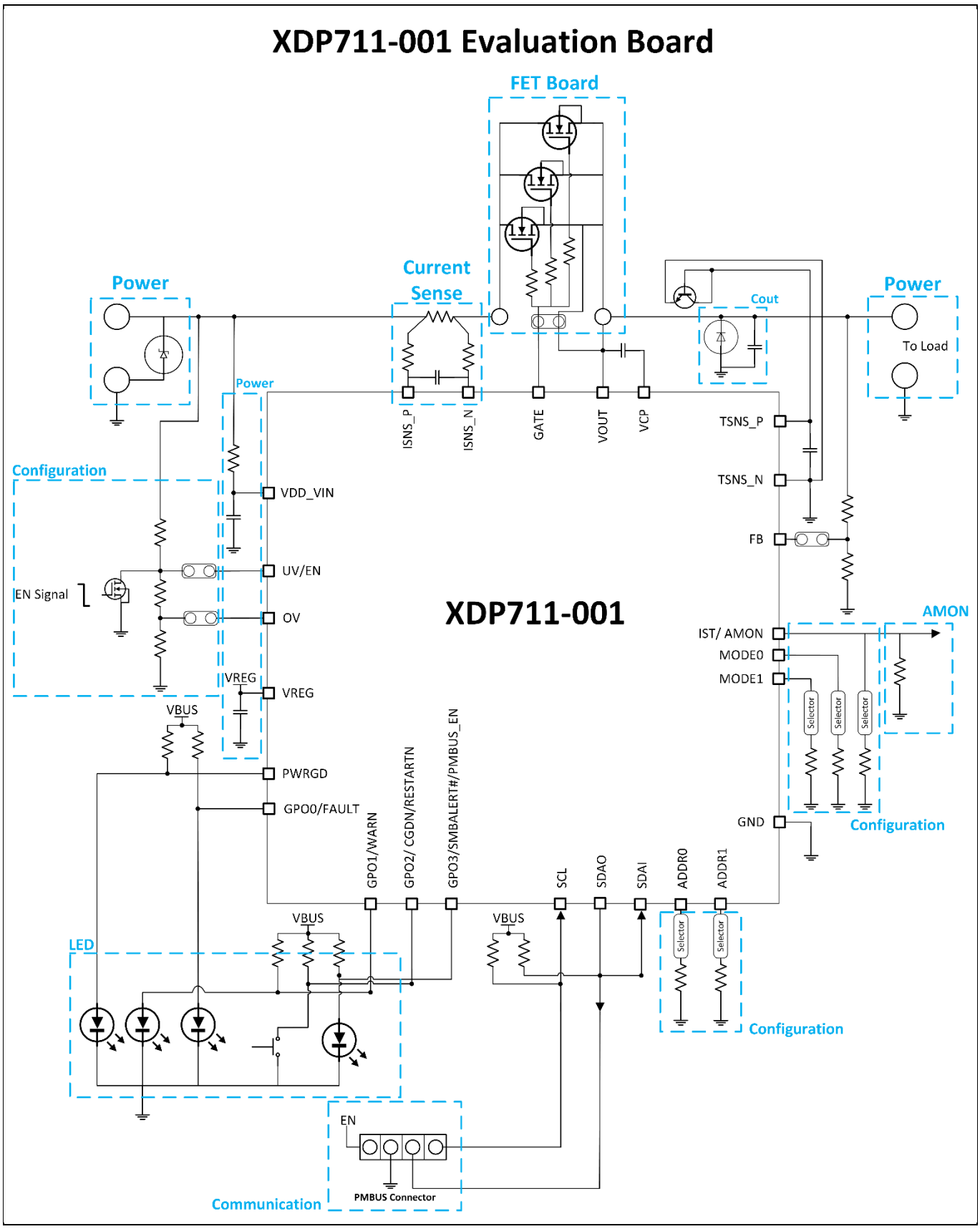


Figure 4 XDP711-001 evaluation platform

3.3 XDP711-001 Evaluation Board schematics

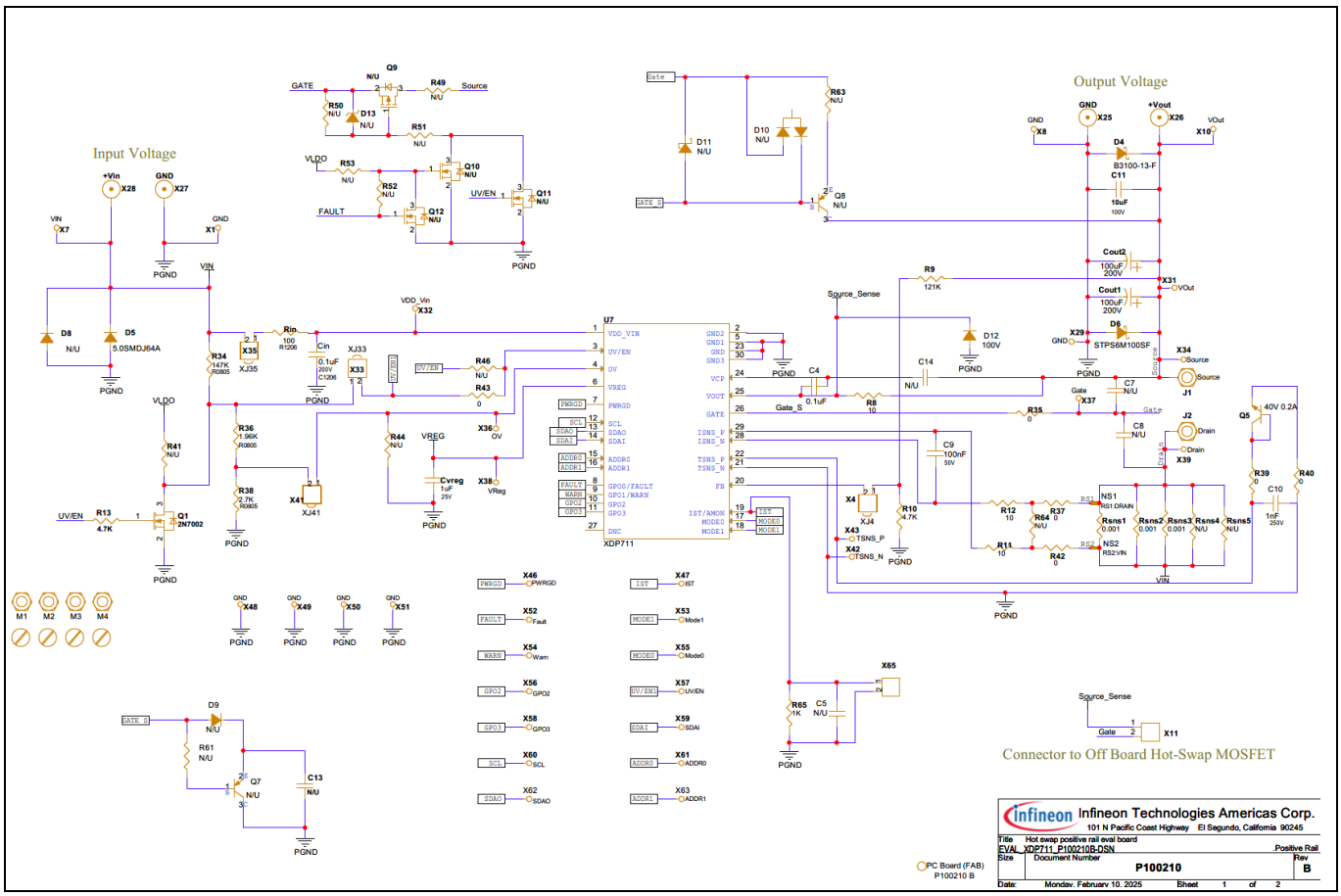


Figure 5 Main IC

XDP711-001 evaluation platform

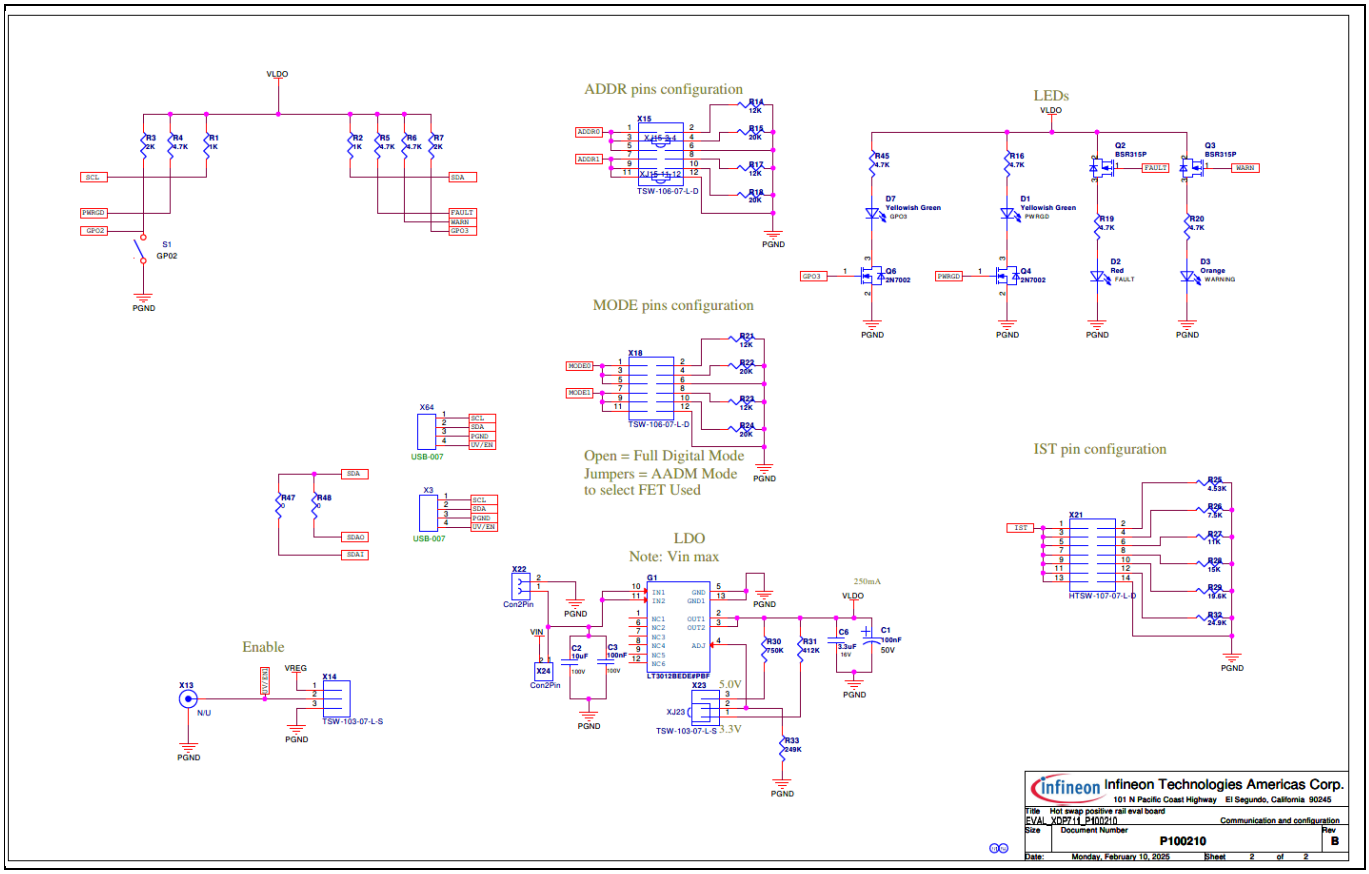


Figure 6 Main PCBA ports

XDP711-001 evaluation platform

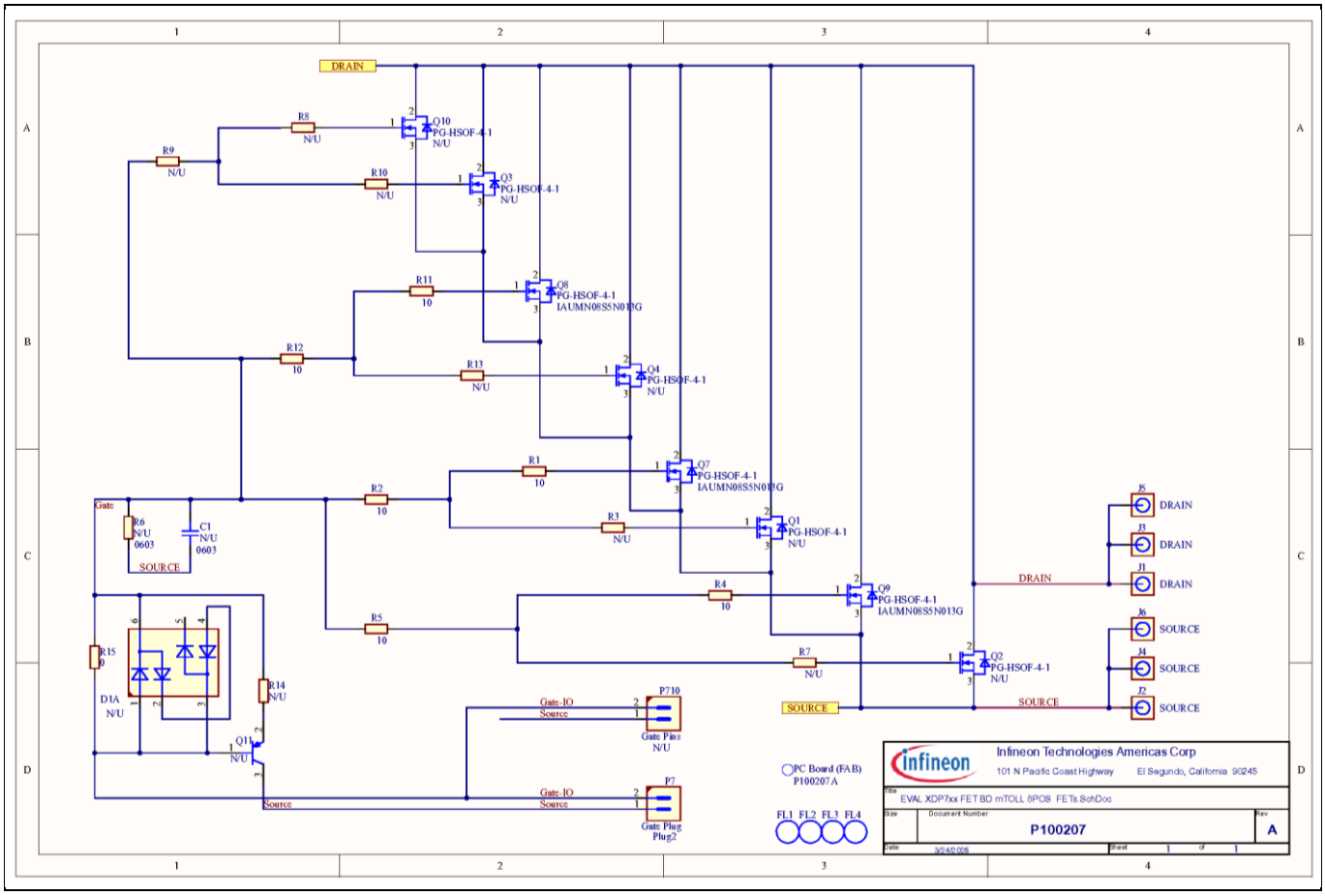


Figure 7 MOSFET PCBA

3.4 XDP711-001 Evaluation Board layout

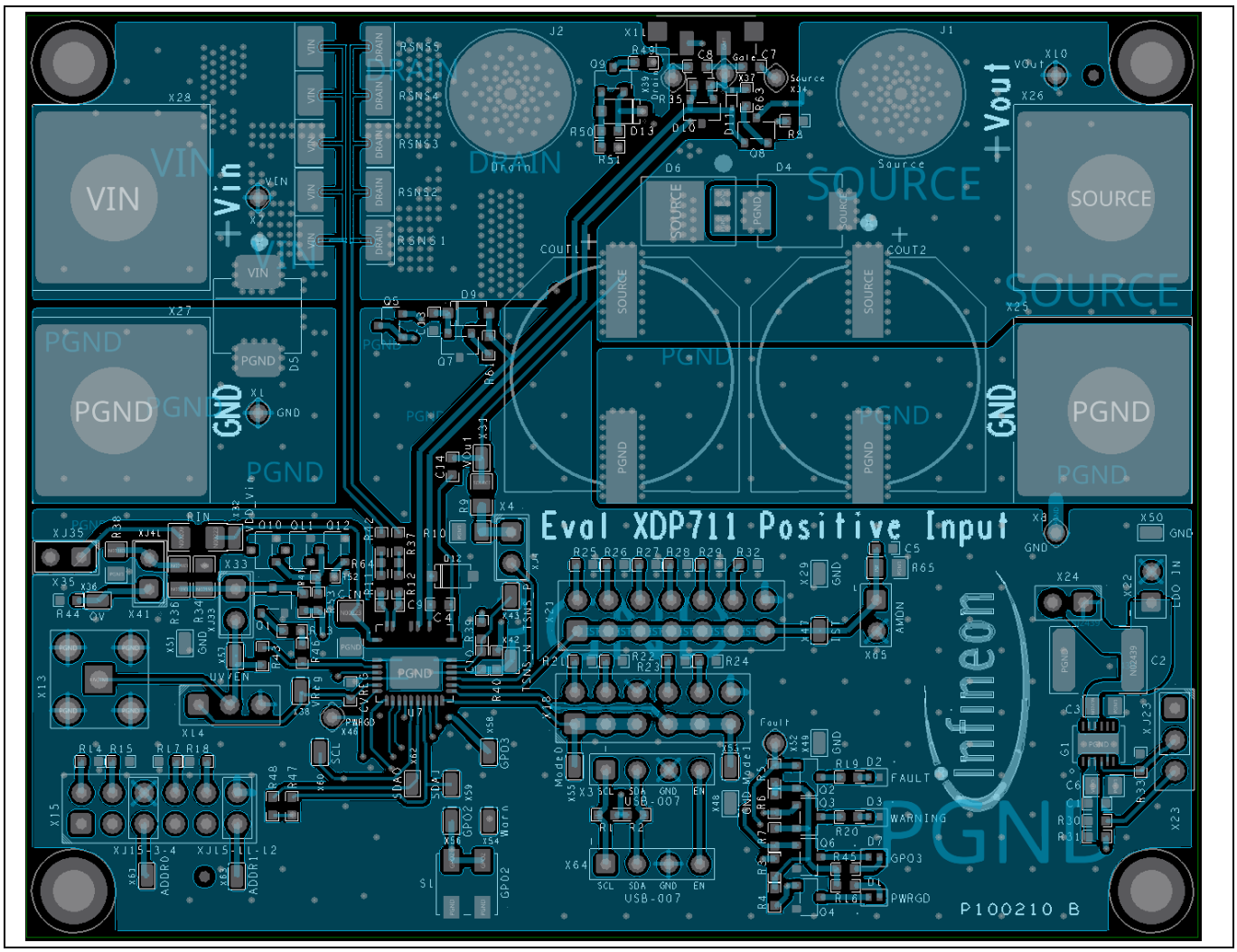


Figure 8 Top layer layout of main PCB

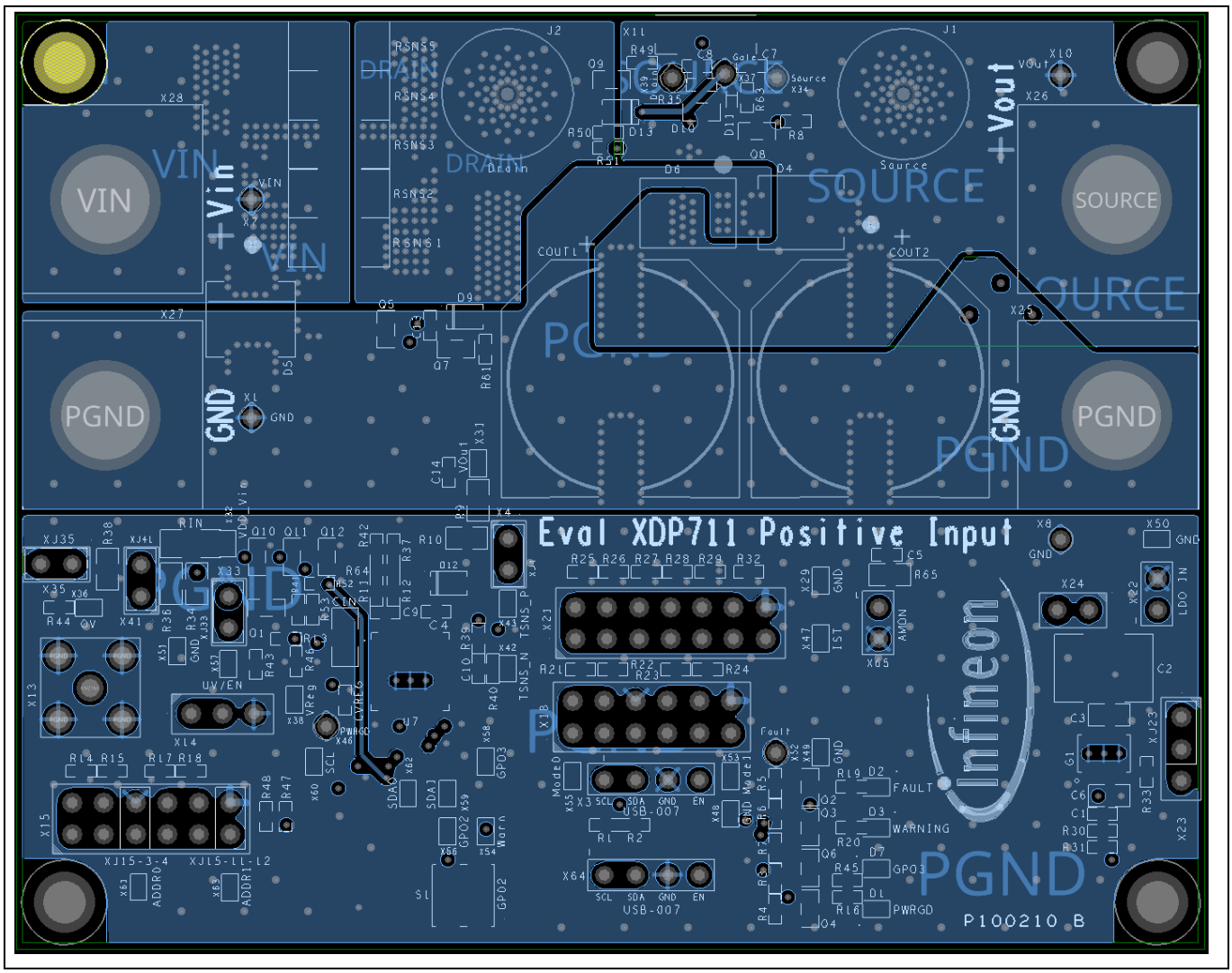


Figure 9 Mid 1 layer layout of main PCB

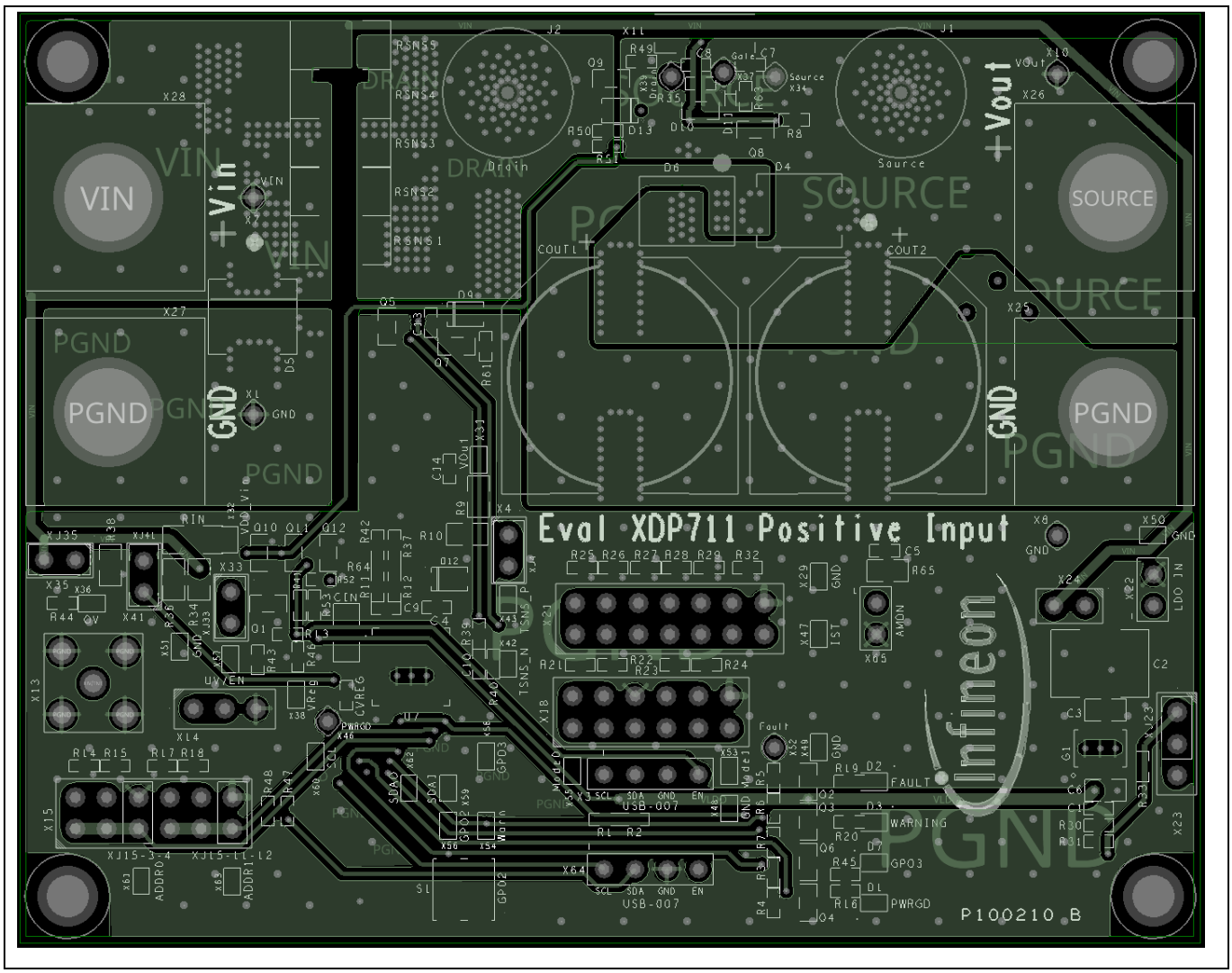


Figure 10 Mid 2-layer layout of main PCB

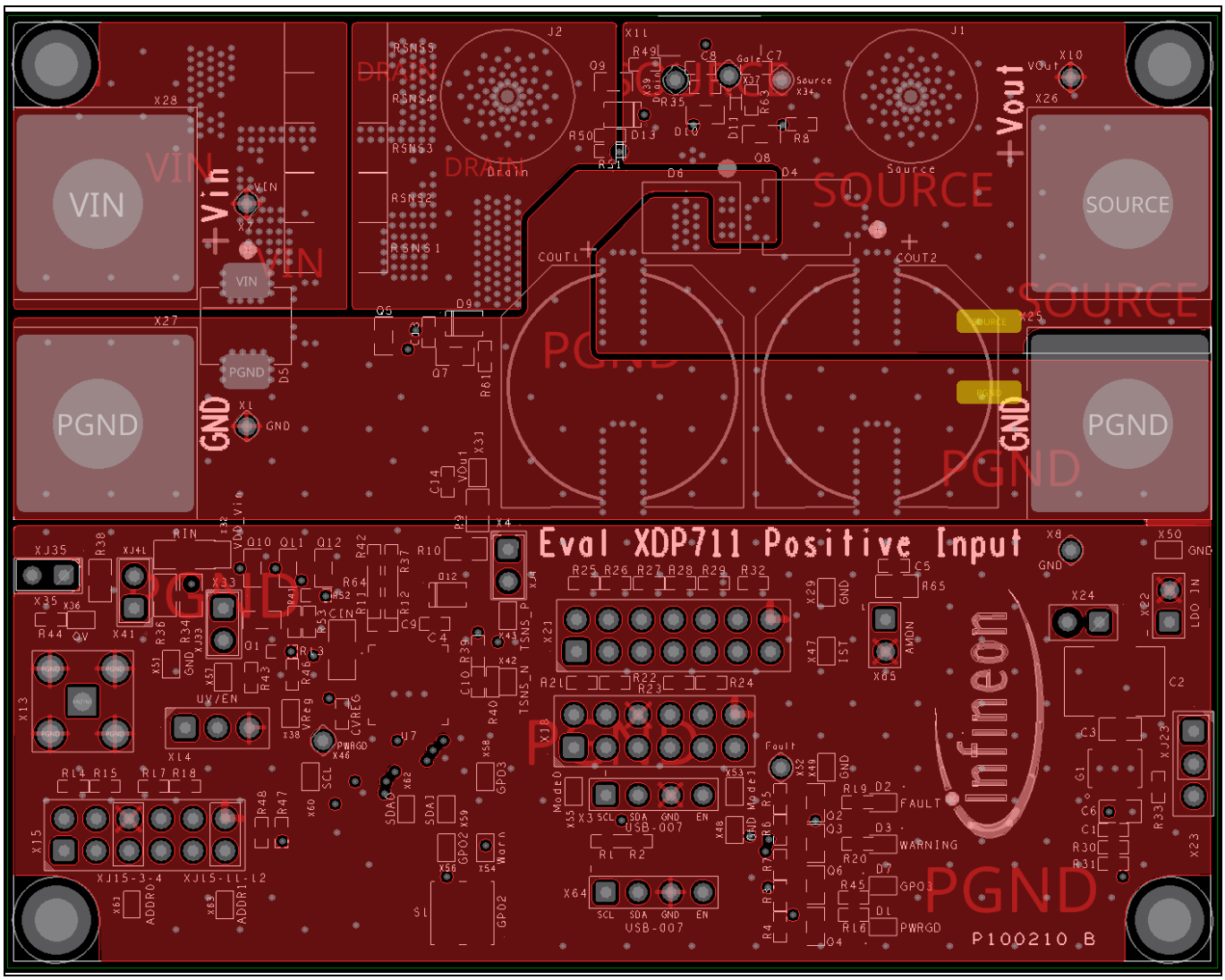


Figure 11 Bottom layer layout of main PCB

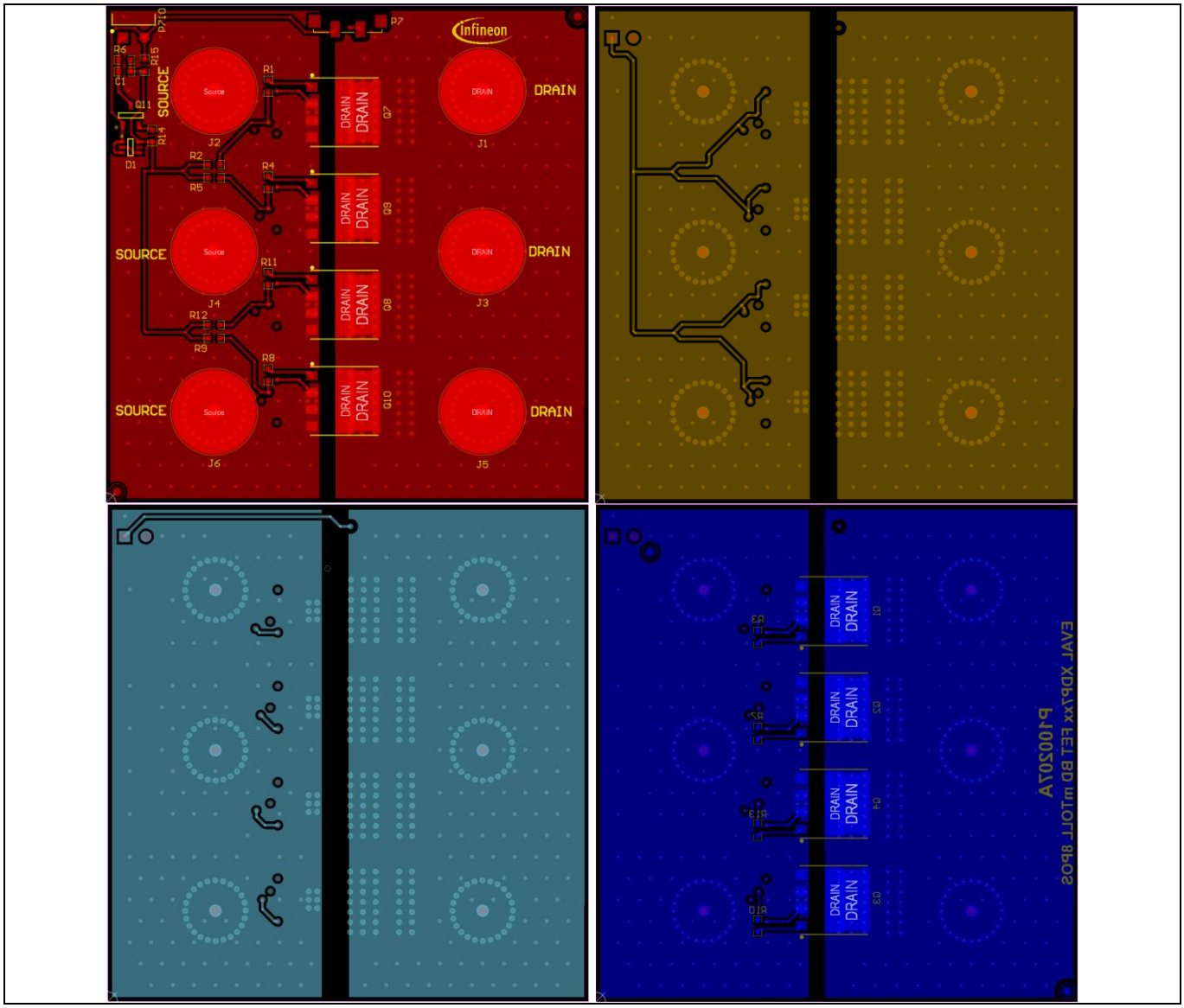


Figure 12 Top, Mid 1, Mid 2, and bottom layer layouts of MOSFET PCB

3.5 XDP711-001 Evaluation Board bill of materials

Table 2 BOM for the main PCBA

Item	Qty	Reference designator	Value	Characteristic	Manufacturer	Part number
1	1	Cin	100nF	200V X7R	Murata	GRM31CR72D104KW03L
2	2	Cout1, Cout2	100uF	160V Elect	Rubycon	160SGV100M18X16.5
3	1	Cvreg	1uF	25V X7R	Murata	GCJ188R71E105KA01D
4	2	C1, C9	100nF	50V X7R	Murata	GCM188R71H104JA57D
5	2	C2, C11	10uF	100V X7S	TDK	C5750X7S2A106K230KB
6	1	C3	100nF	100V X7R	Kemet	C0805X104K1RACTU
7	1	C6	3.3uF	16V X7R	Murata	GCM21BR71C335KA73L
8	1	C10	1nF	250V X7R	Murata	GRM188R72E102KW07
9	2	D1, D7	Yellowish Green		ROHM	SML-P11MTT86R
10	1	D2	Red		ROHM	SML-P11UTT86R
11	1	D3	Orange		ROHM	SML-P11DTT86R
12	1	D4	B3100-13-F		Diodes Inc	B3100-13-F
13	1	D5	5.0SMDJ64A		LittlefFuse	5.0SMDJ64A
14	1	D6	STPS6M100SF		STMicro	STPS6M100SF
15	1	D12	100V	300mA	Diodes Inc	BAV16W-7-F
16	1	G1	LT3012BEDE#PBF		Analog Devices	LT3012BEDE#PBF
17	2	J1, J2	SO-M5		Würth Elektronik	7466105R
18	4	M1, M2, M3, M4	MTG_Standoff		Keystone	2203
19	4	M5, M6, M7, M8	Screw PHMS 4-40 x 1/4		Keystone	9900
20	3	Q1, Q4, Q6	2N7002		Infineon	2N7002H6327XTSA2
21	2	Q2, Q3	BSR315P		Infineon	BSR315PH6327XTSA1
22	1	Q5	40V 0.2A		Nexperia	MMBT3904,215
23	1	Rin	100	1%	Panasonic	ERJ-8ENF1000V
24	3	Rsns1, Rsns2, Rsns3	0.001	5W 1%	Bourns	CSS2H-2512R-1L00F
25	2	R1, R2	1K	1%	Panasonic	ERJ-3EKF1001V
26	2	R3, R7	2K	1%	Panasonic	ERJ-3EKF2001V
27	8	R4, R5, R6, R13, R16, R19, R20, R45	4.7K	1%	Panasonic	ERJ-3EKF4701V
28	3	R8, R11, R12	10	1%	Panasonic	ERJ-3EKF10R0V
29	1	R9	121K	1%	Vishay	CRCW0805121KFK
30	1	R10	4.7K	1%	Panasonic	ERJ-6ENF4701V

XDP711-001 evaluation platform

Item	Qty	Reference designator	Value	Characteristic	Manufacturer	Part number
31	4	R14, R17, R21, R23	12K	1%	Panasonic	ERJ-3EKF1202V
32	4	R15, R18, R22, R24	20K	1%	Panasonic	ERJ-3EKF2002V
33	1	R25	4.53K	1%	Panasonic	ERJ-3EKF4531V
34	1	R26	7.5K	1%	Panasonic	ERJ-3EKF7501V
35	1	R27	11K	1%	Panasonic	ERJ-3EKF1102V
36	1	R28	15K	1%	Panasonic	ERJ-3EKF1502V
37	1	R29	19.6K	1%	Panasonic	ERJ-3EKF1962V
38	1	R30	750K	1%	Panasonic	ERJ-3EKF7503V
39	1	R31	412K	1%	Panasonic	ERJ-3EKF4123V
40	1	R32	24.9K	1%	Panasonic	ERJ-3EKF2492V
41	1	R33	249K	1%	Panasonic	ERJ-3EKF2493V
42	1	R34	147K	1%	Vishay	CRCW0805147KFK
43	8	R35, R37, R39, R40, R42, R43, R47, R48	0	1%	Panasonic	ERJ-3GEY0R00V
44	1	R36	1.96K	1%	Vishay	CRCW08051K96FK
45	1	R38	2.7K	1%	Vishay	CRCW08052K70FK
46	1	R65	1K	0.1%	Panasonic	ERA-6AEB102V
47	1	S1	SW SPST			7914J-1-000E
48	1	U7	XDP711-001		Infineon	XDP711-001
49	8	XJ4, XJ23, XJ24, XJ33, XJ35, XJ41, XJ15-3-4, XJ15-11-12	CON2_Jumper		Sullins	SPC02SYAN
50	9	X1, X7, X8, X10, X34, X37, X39, X46, X52	Loop		Keystone	5020
51	2	X3, X64	CON4		Würth Elektronik	61300411121
52	7	X4, X22, X24, X33, X35, X41, X65	Con2Pin		Harwin	M20-9770246
53	1	X11	SOC2		AVX	2.09159E+14
54	2	X14, X23	TSW-103-07-L-S		Samtec	TSW-103-07-L-S
55	2	X15, X18	TSW-106-07-L-D		Samtec	TSW-106-07-L-D
56	1	X21	HTSW-107-07-L-D		Samtec	HTSW-107-07-L-D

XDP711-001 evaluation platform

Item	Qty	Reference designator	Value	Characteristic	Manufacturer	Part number
57	4	X25, X26, X27, X28	PEM NUT 8-32 + Screw		PEM + McMaster-Carr	KF2-832-ET + 91241A652
58	23	X29, X31, X32, X36, X38, X42, X43, X47, X48, X49, X50, X51, X53, X54, X55, X56, X57, X58, X59, X60 X61, X62, X63	Smd Loop		Harwin	S2761-46R
59		C4	0.47uF	50V X7R	TDK	C1608X7R1H474K080AC
60	5	C14, C5, C7, C8, C13	N/U			Not Used
61	1	D8	N/U			Not Used
62	1	D9	N/U			Not Used
63	7	Q7, Q8, Q9, Q10, D10, Q11, Q12	N/U			Not Used
64	1	D11	N/U			Not Used
65	1	D13	N/U			Not Used
66	2	Rsns4, Rsns5	N/U			Not Used
67	11	R41, R44, R46, R49, R50, R51, R52, R53, R61, R63, R64	N/U			Not Used
68	1	X13	N/U			Not Used

Table 3 BOM for MOSFET PCBA

Item	Qty	Reference designator	Value	Characteristic	Manufacturer	Part number
1	1	P7	Plug2		KYOCERA AVX	109159002101916
2	1	Q11	MMBT3906LT1G		ON Semiconductor	MMBT3906LT1G
3	12	R2, R5, R9, R12, R8, R10, R11,	10	1/10W	Panasonic	ERJ-3EKF10R0V

Item	Qty	Reference designator	Value	Characteristic	Manufacturer	Part number
		R13, R1, R3, R4, R7				
4	6	J1, J2, J3, J4, J5, J6	SO-SMD-M5-FEMALE		Würth Elektronik	7466105R
5	3	Q7, Q9, Q8	IPM018N10NM5LF2	100V	Infineon	IPM018N10NM5LF2
6	0	R15	0	1/10W	Panasonic	ERJ-3GEY0R00V
7		Q11	N/U		ON Semiconductor	MMBT3906LT1G
8	1	D1	100V		Nexperia	BAV99S,115
9	1	R14	N/U	1/10W	Panasonic	ERJ-3EKF1800V
10	1	C1	N/U	100V	TDK	Not Used
11	1	P710	N/U		Samtec	Not Used
12	5	Q10, Q3, Q4, Q1, Q2	N/U	100V	Infineon	IPM018N10NM5LF2
13	2	R6, R15	N/U	1/10W	Panasonic	Not Used

3.6 XDP711-001 Evaluation Board default settings

See the jumpers on the board as shown in Table 4.

Table 4 Jumper settings

Reference designator	Default configuration	Usage
X4	Open	• **Shorted**: Connects FB to the voltage divider for overvoltage/undervoltage sensing. To be used in AADM, ACM, and Hybrid modes • **Open**: This header can be left open for digital comparator mode (DCM)
X14	Open	• **Shorted 1 to 2**: Connects UV/EN to VREG (R46: 0 Ω, R13: DNI) • **Shorted 2 to 3**: Connects UV/EN to GND (R46: 0 Ω, R13: DNI) • **Open**: UV/EN can be driven by an SMA connector (R46: 0 Ω, R13: DNI)
X15	Between pins 5 and 6 and between pins 11 and 12	ADDRx pins configuration to 0x10. Move the jumpers to change the PMBus® address
X18	Open	MODEx pins configuration. Leave them open for fully digital mode (FDM)
X21	Open	IST pin configuration, to use IST pin ensure that R65 is DNI

Reference designator	Default configuration	Usage
X23	Shorted 1 to 2	• **Shorted 1 to 2**: VLDO = 3.3 V • **Shorted 2 to 3**: VLDO = 5 V This header must not be left open
X24	Shorted	• **Shorted**: LDO is supplied by VIN • **Open**: LDO is supplied by external source connected to X22 **Use an external 12 V source on X22 to avoid adding bias capacitance on the Vin**
X33	Shorted	• **Shorted**: Connects UV/EN to the voltage divider and by the signal on X64/ X3 Pin 4. • **Open**: UV/EN can be driven by X14 configuration
X35	Shorted 1 to 2	• **Shorted**: VDD_VIN is connected to the input voltage • **Open**: A current meter can be connected to this header to measure input current to the IC
X41	Open	• **Shorted**: Connects OV to the voltage divider • **Open**: This header can be left open for DCM
X65	Open	Use to measure the AMON (IMON or PMON) voltage

Table 5 Resistors and capacitors

Reference designator	Default configuration	Notes
R35	0 Ω	This value can be increased to reduce the slew rate of gate turn off during a short-circuit or on-chip overvoltage event
C7	Not installed	C_{gs} of FET can be modified to adjust the surge immunity recovery behavior
C8	Not installed	C_{gd} (if populated, unexpected behavior is observed)
R11, R12	10 Ω	For high dV/dt application to avoid damage to the SENSE pins
R37, R64	R37 = 0 Ω R64 = Not Installed	If the Rsns value needs to be modified apart from changing the Rsns resistors, the resistor divider can be added by placing R64 = 10 Ω and adjusting the divider ratio with R64. This also adds some offset into the current ADC
C9	100nF	R_{sns} filter; recommended to keep this capacitor as 100 nF
R39, R40	0 Ω	Recommended to keep it as 0 Ω
C10	1 nF	Temperature sensor filter
R46	Not installed	• **Populate 0 Ω**: If EN is driven directly by X64 (Pin 4) or X63 (Pin 4) and X41 is open • **Not populated**: If EN is driven by X33

Reference designator	Default configuration	Notes
R43	0 Ω	• **Populate 0 Ω**: If EN is driven by X33, if X33 jumper is not installed then drive by X14 • **Not populated**: If EN is driven by X64 (Pin 4) or X63 (Pin 4)
Rin	100 Ω	The resistor value can be scaled depending on the maximum current sourcing on VREG pin Recommended to keep it as >= 100 Ω for application with high short-circuit current to prevent the damage due to high dV/dt on the VDD_VIN pin
R30, R31, R33	750 kΩ, 412 kΩ, 249 k Ω respectively	LDO feedback voltage dividers; the current combination provides 5 V and 3.3 V on VLDO. Ensure that this value does not exceed 5.5 V or goes below 2.5 V
R41	Not installed	• **Populate 10 kΩ**: If EN is driven directly by X64 (Pin 4) or X63 (Pin 4), X41 and R43 populated but R36 is not installed • **Not populated**: If EN minimum voltage is controlled via Vin voltage and On/Off operation is controlled via X64 (Pin 4) or X63 (Pin 4)

Other components are populated as specified in the schematics.

3.7 R_{sns}

Five current sense resistors of size 2512 can be placed in parallel on Rsns1, Rsns2, Rsns3, Rsns4, and Rsns5. For the eval board to get 0.33 mΩ sense value, three 1 mΩ resistors are populated on Rsn1, Rsns2, and Rsns3.

3.8 FET board

The XDP711-001 Evaluation Board comes with an option to place different FET boards depending on the FET footprint required for the application. The eval board comes with the mTOLL FET footprint where eight FETs can be paralleled together. By default, the eval board comes with 3x IPM018N10NM5LF2 FETs populated on it as a 3 kW reference design.

3.9 Different FET footprint options on FET board

There are various FET boards available to support different designs. The P100147A FET board footprint supports PG-TO263-7 (D^2PAK-7), PG-HSOF-8 (TOLL), PG-HDSOP-16 (TOLT), and PG-TSON-8 (SSO8) packages in the following positions:

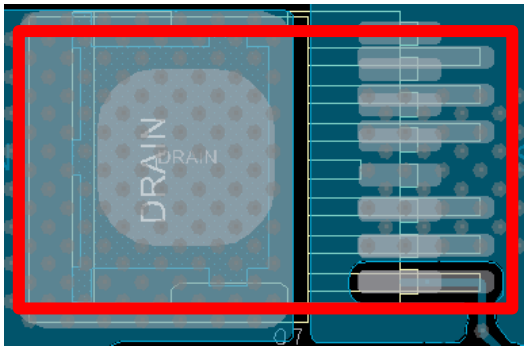


Figure 13 PG-TO263-7 (D²PAK7) position (top side)

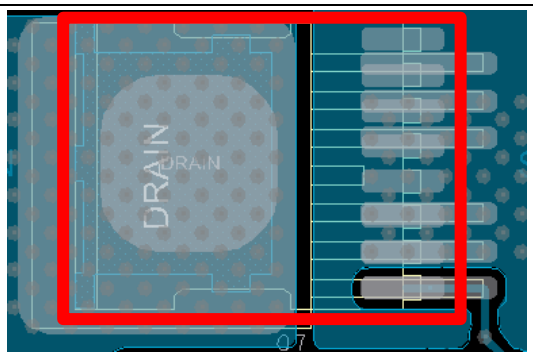


Figure 14 PG-HSOF-8 (TOLL) position (top side)

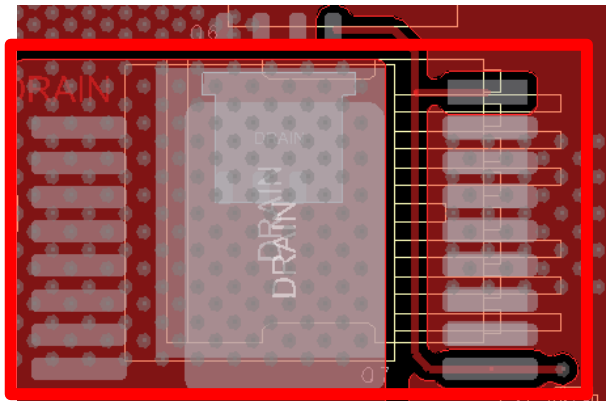


Figure 15 PG-HDSOP-16 (TOLT) position (bottom side)

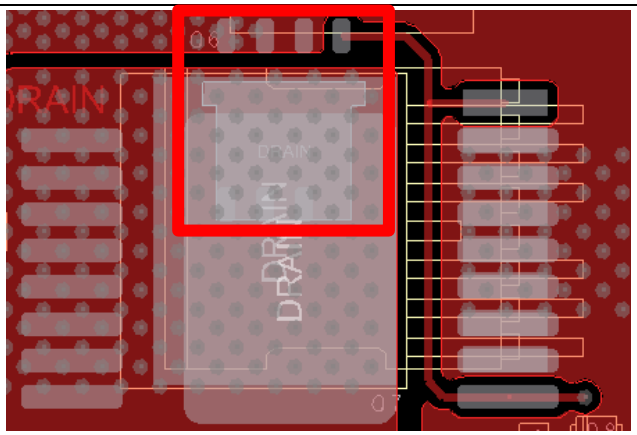


Figure 16 PG-TSON-8-3 (SSO8) position (bottom side)

To test multiple FETs in parallel, up to 3x of P100147A boards can be connected in parallel.

To have a simpler design, more FET board options are available as shown in Table 6.

Table 6 Various FET board options

FET Footprint	Order Code No.	Number of FET positions
PG-HSOF-8 (TOLL)	EVAL_XDP7xx_FET_BRD_TOLL	8
PG-TSON-8-3 (SSO8)	EVAL_XDP7xx_FET_BRD_SSO8	12
PG-TO263-3 (D^2PAK-3)	EVAL_XDP7xx_FET_BRD_D2PAK3	8
PG-TO263-7 (D^2PAK-7)	EVAL_XDP7xx_FET_BRD_D2PAK7	8
PG-HSOF-8 (mTOLL)	EVAL_XDP7xx_FET_BRD_mTOLL	8

3.10 Various ways to enhance the turn-off speed during regular faults

XDP711-001 offers the pull-down strength of 1.25 mA for regular fault conditions. This pull-down strength is sufficient for most of the applications, but some designs require it to be higher to have a fast turn-off. The eval board has two circuits to achieve this fast pull-down.

3.10.1 External fast turn-off circuit using GATE pin for activation

Circuit in Figure 17 shows the external fast turn-off circuit using the GATE pin for activation.

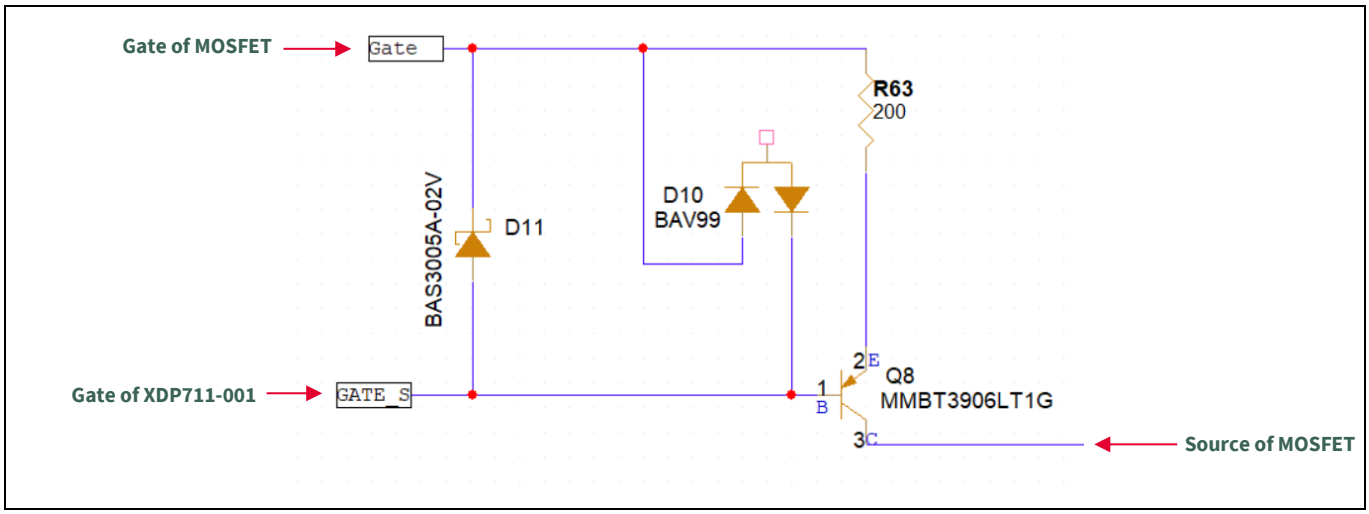


Figure 17 Fast turn-off external circuit using gate pin for activation

Figure 17 show the simplified schematics for the external circuit for fast turn-off circuit, (a) for gate turning on, and (b) for gate turning off.

During gate turn-on, as shown in Figure 18 (a), the gate charging current I_{DAC_FS} flows from the GATE pin of XDP711-001 to the gate of external power MOSFETs, through the Zener diode D11. A Schottky diode is used for D11 so that a maximum voltage drop of 0.3 V is observed for the gate-to-source voltage on the MOSFET side. Diode D10 and the BJT transistor Q8 are OFF.

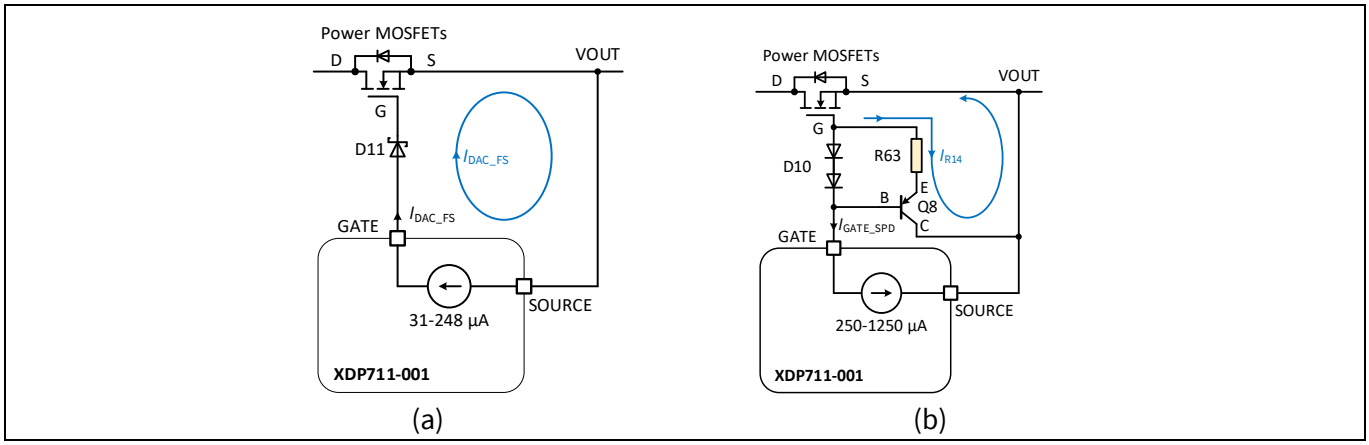


Figure 18 Simplified schematics of external circuit for fast turn-off in circuit #2, (a) gate turn-on, (b) gate turn-off

During gate turn-off, as shown in Figure 18 (b), the gate discharging current I_{GATE_SPD} flows from the MOSFET gate to the GATE pin of XDP711-001 goes through D10. The two diodes in series, and the BJT transistor Q8 turns ON. The voltage drop on the resistor R63 is almost constant (≈ 0.7 V), and the gate-to-source turn-off current of the MOSFETs has an extra path through R14 and the emitter terminal (E) of Q5 to the collector terminal (C), with the current value shown in Equation 1:

$$I_{R14} = \frac{V_{D10} - V_{EB_Q8}}{R63} \approx \frac{0.7\,V \times 2 - 0.7\,V}{R63} = \frac{0.7\,V}{R14}$$

Equation 1

From Equation 1, the extra gate switching-off current I_{R14} is a constant current source, depending only on the R63 resistor value. Therefore, you can adjust the R63 value to achieve the required switching-off time for different situations.

Note: R35 must be de-populated to use this circuitry.

The advantage of this circuit is that the control is fully dependent on the behavior of the gate pin. On the other hand, it has the drawback that there will always be a 0.3 V drop on the gate signal.

For more detailed explanation, refer [3].

3.10.2 External fast turn-off circuit using FAULT pin for activation

Circuit in Figure 19 shows the external fast turn-off circuit using the gate pin for activation.

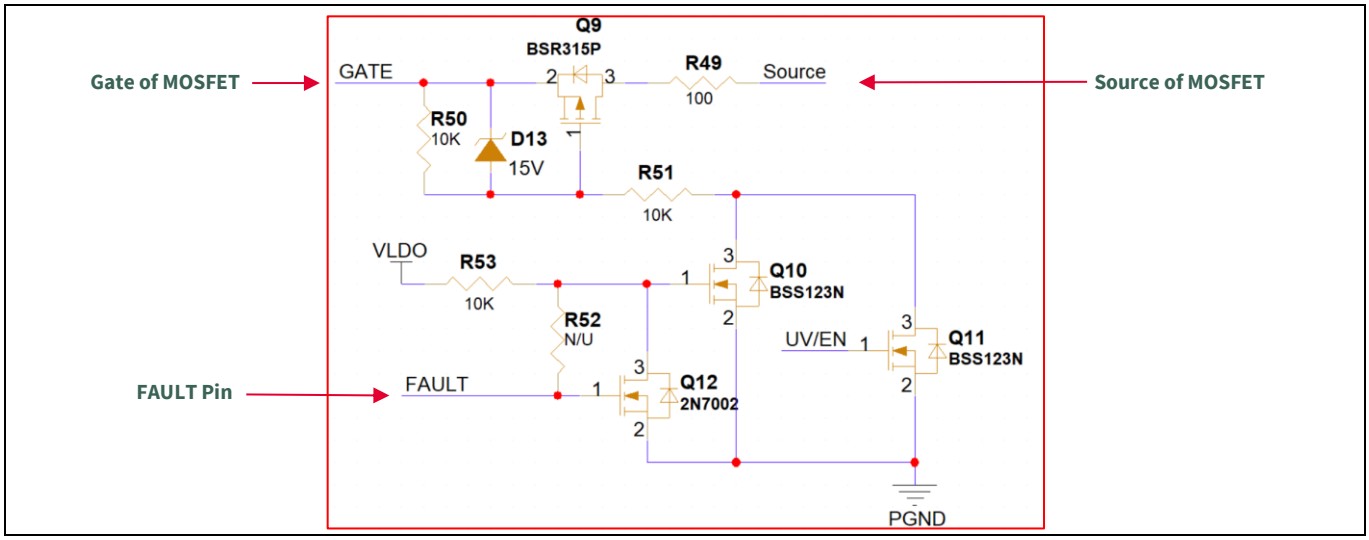


Figure 19 Fast turn-off external circuit using FAULT pin for activation

Figure 19 shows a closer view of the external circuit for fast switch-off #1. A P-channel small-signal MOSFET (Q9) is used to connect the gate to the source of the MOSFET through a resistor (R49) controlled by the digital signals FAULT_N (active LOW FAULT) or FAULT (active HIGH FAULT), or an external control signal EN_N (active LOW). If FAULT_N is connected to the fault pins of other devices, the alternative signal, GPO1/WARN/LED#, of XDP711-001 can be used as the control signal instead of FAULT_N. When Q9 turns on, its $R_{DS(on)}$ is negligible compared to R49. The Zener diode (D13) is used to clamp the gate-to-source voltage of Q9 to prevent damage when the N-channel small-signal MOSFET Q10 or Q11 is on.

When both Q10 and Q11 are off, Q9 is off; the external power MOSFETs can be controlled by XDP711-001 normally for startup with (or without) Boost Mode, and normal operations when the power MOSFETs' gates are fully on.

The N-channel small-signal MOSFET (Q12) inverts the signal FAULT_N if the controller's GPO0/FAULT is configured as active LOW. If GPO0/FAULT is configured active HIGH, R52 can be populated with 0 Ω, but Q12 and R53 must be depopulated.

Figure 20 shows the simplified schematics for the external circuit for fast switch-off #1. Figure 20 (a) shows the condition when no fault happens and it is in normal operation, so Q11 is OFF, and its body diode is not conducting unless gate source voltage is negative for the power MOSFET.

Figure 20 (b) shows a fault is occurring. Therefore, Q11 is on and the power MOSFETs switch off. When the power MOSFETs switch off at normal faults, the current through resistor R30 (I_{R30}) and slow pull-down current I_{GATE_SPD} discharge through the MOSFETs' gate. In this section, calculations are presented for the switch-off time at a normal fault.

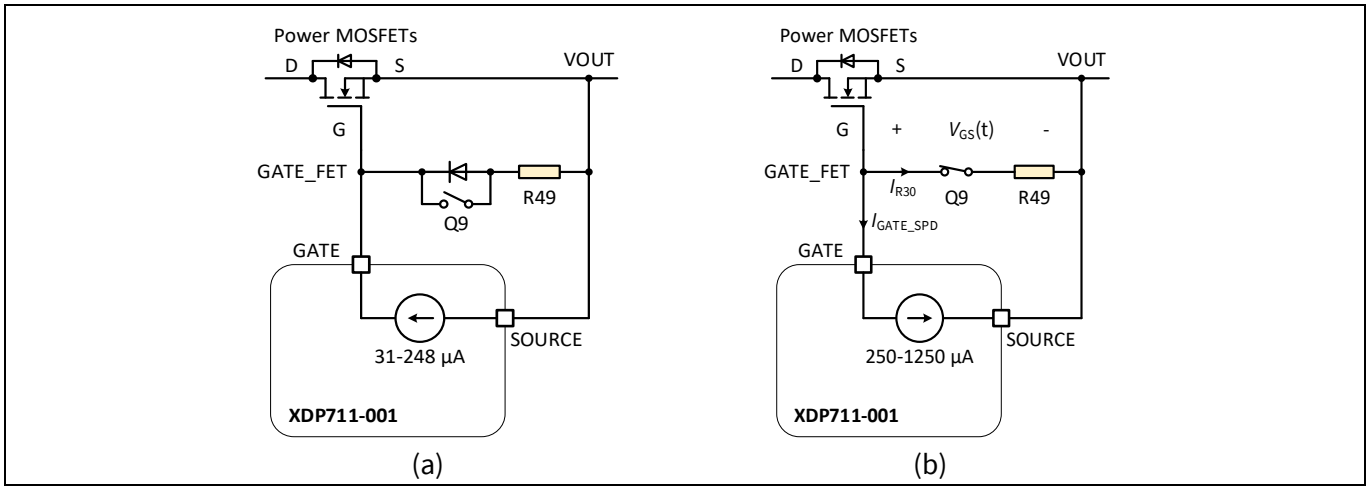


Figure 20 Simplified schematics of external circuit for fast switch-off #1, (a) no fault and normal operation, (b) at fault and power MOSFETs switch off

This circuit does not cause any interference with the normal FET operation. However, you should ensure the following:

- Faults that require fast turn-off are mapped onto the FAULT pin
- FAULT pin must not be tied to any other FAULT pin because this can cause an unexpected turn-off
- SMBALERT pin shall not be used for this application Only a pin that is configured as FAULT (GPO0) or LED (GPO1) can be used for this
- VLDO must be pulled up using VREG to ensure that supply is available before the hotswap operation can occur. If the VLDO is supplied with a supply available after the startup then startup will not occur

For more details, refer [3].

3.11 USB00010 dongle schematics

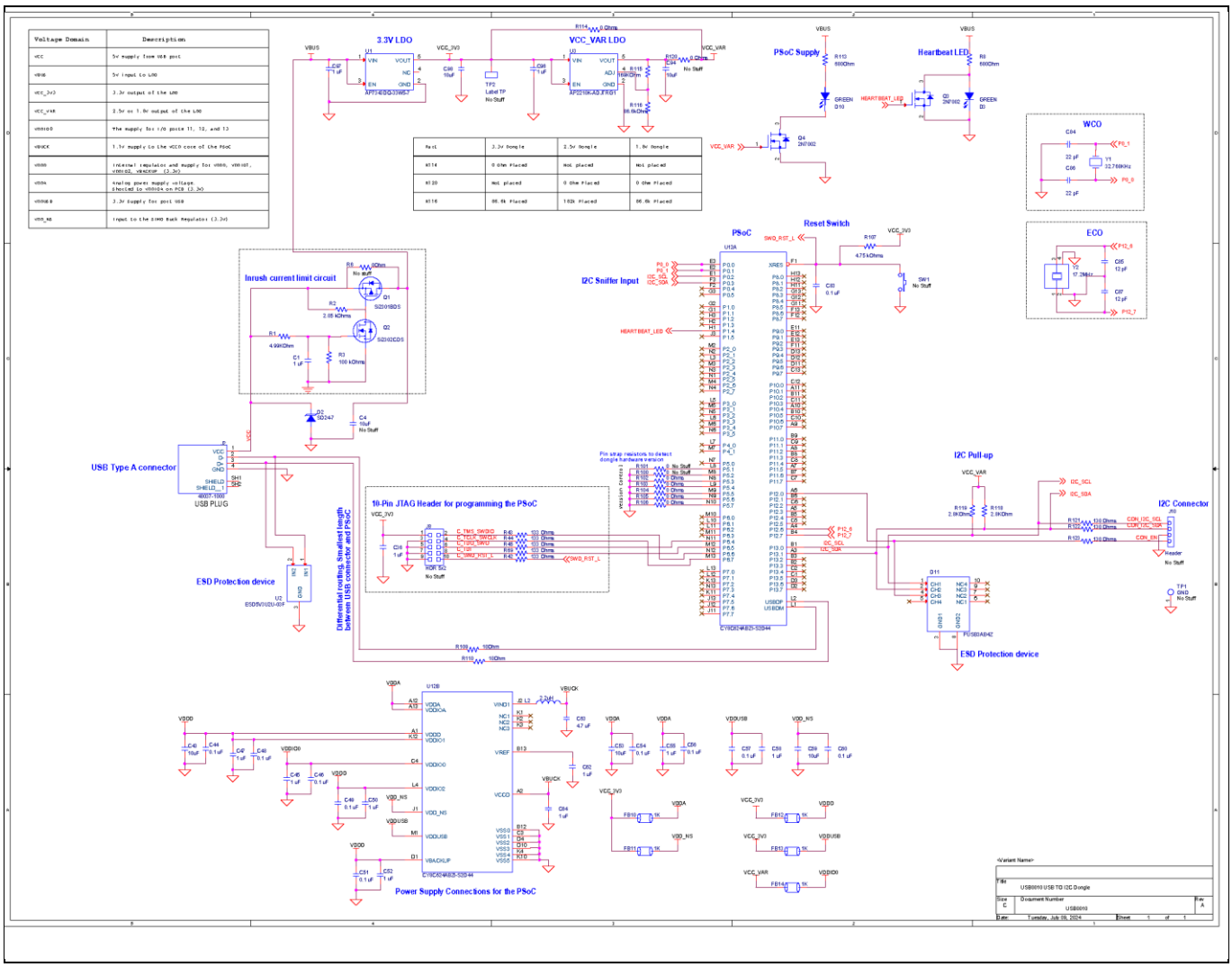


Figure 21 USB0010 dongle schematics

4 Programming, set up, and turn-on instructions

Set up the system as follows:

1. Connect the USB010 dongle to the XDP711-001 Evaluation Board X3 as shown in Figure 22
2. Connect the USB010 dongle to a PC USB port
3. Ensure that the jumpers are connected properly
4. Connect 48 V from VDD_VIN (X28 connector) to the GND (X27) on the left side of the board

XDP711-001 powers up as soon as VDD_VIN is equal to or greater than 5.5 V. At this point, communication and programming is possible, but the FET will be off. To turn on the FET, a minimum of 9 V is required, after which at least the following registers must be programmed to turn on the device.

- FET select
- R_{sns}

UV/EN is controlled by an external trigger; it will hold the signal HIGH depending on VIN voltage until it is toggled manually. Alternatively, it can be controlled by UV/EN1, which is controlled by the X14 header. It must be held LOW until the necessary registers are written. Use one signal at a time.

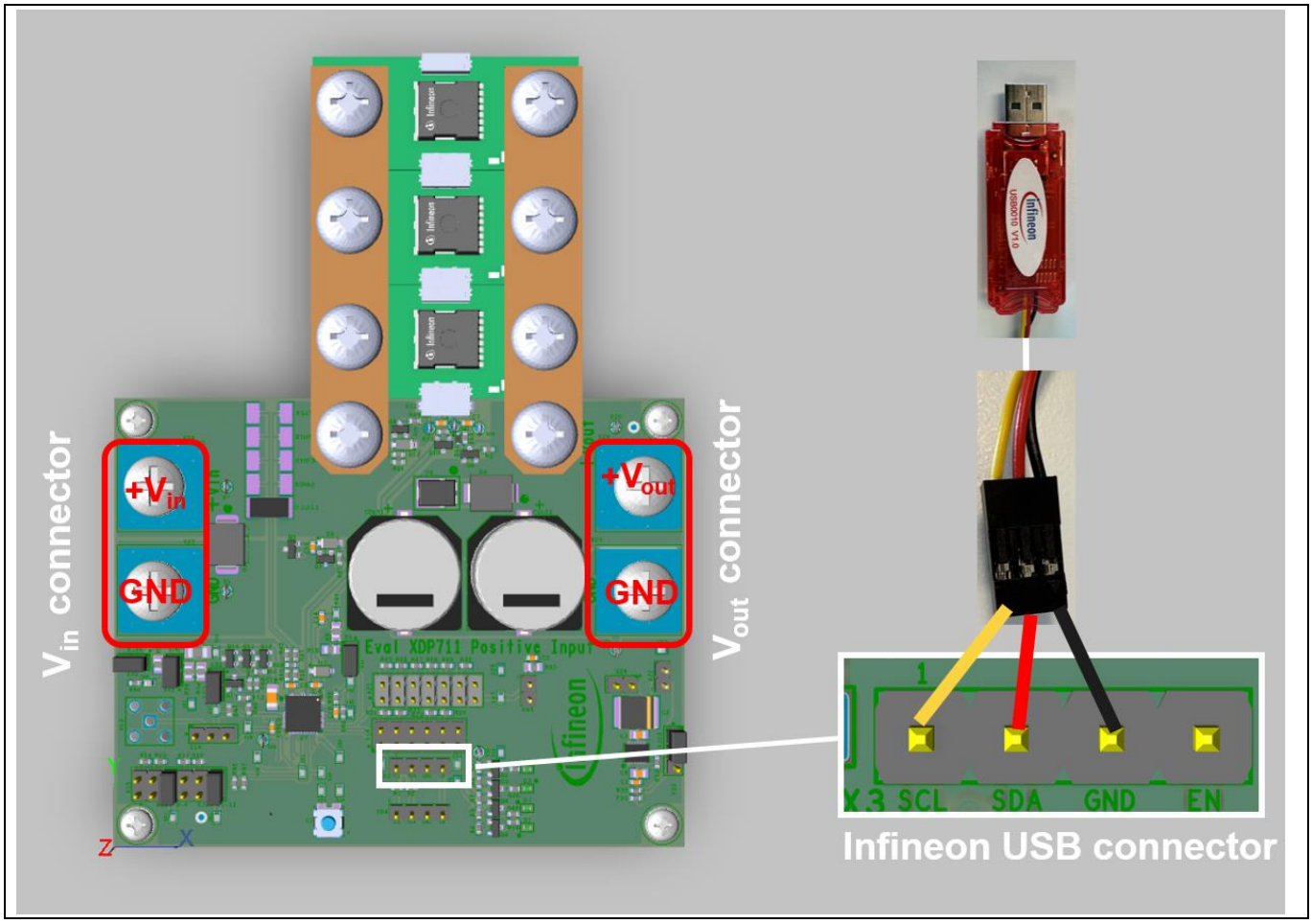


Figure 22 XDP711-001 Evaluation Board and dongle setup

4.1 XDP™ Designer communication setup

Install the XDP™ Designer software from the Infineon Development Center.

The following sections explain how to configure and test the evaluation board and dongle using the XDP™ Designer software.

4.1.1 Dongle connection in XDP™ Designer

1. Open the XDP™ Designer GUI
2. Wait for a few seconds and check the bottom status bar for the dongle connection.
   If the highlighted area, as shown in Figure 23, turns green and displays **USB0010**, the dongle has been successfully detected by the GUI
3. Ensure that the EN pin is pulled HIGH externally

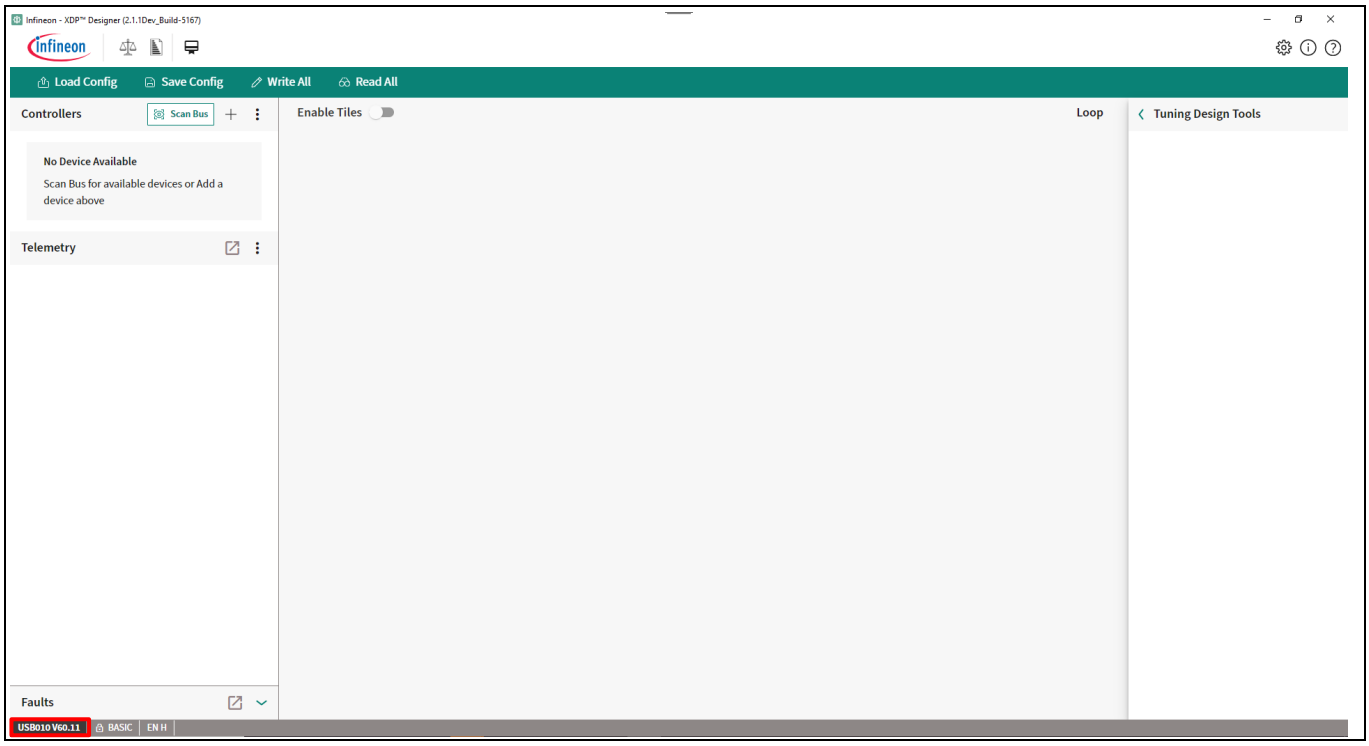


Figure 23 USB0010 detection on XDP™ Designer

4.1.2 Detecting XDP711-001

1. Click **Scan Bus**, as shown in Figure 24
2. Wait for a few seconds for the device to be detected by the GUI automatically. If the device is not detected automatically, click **Scan For Devices**

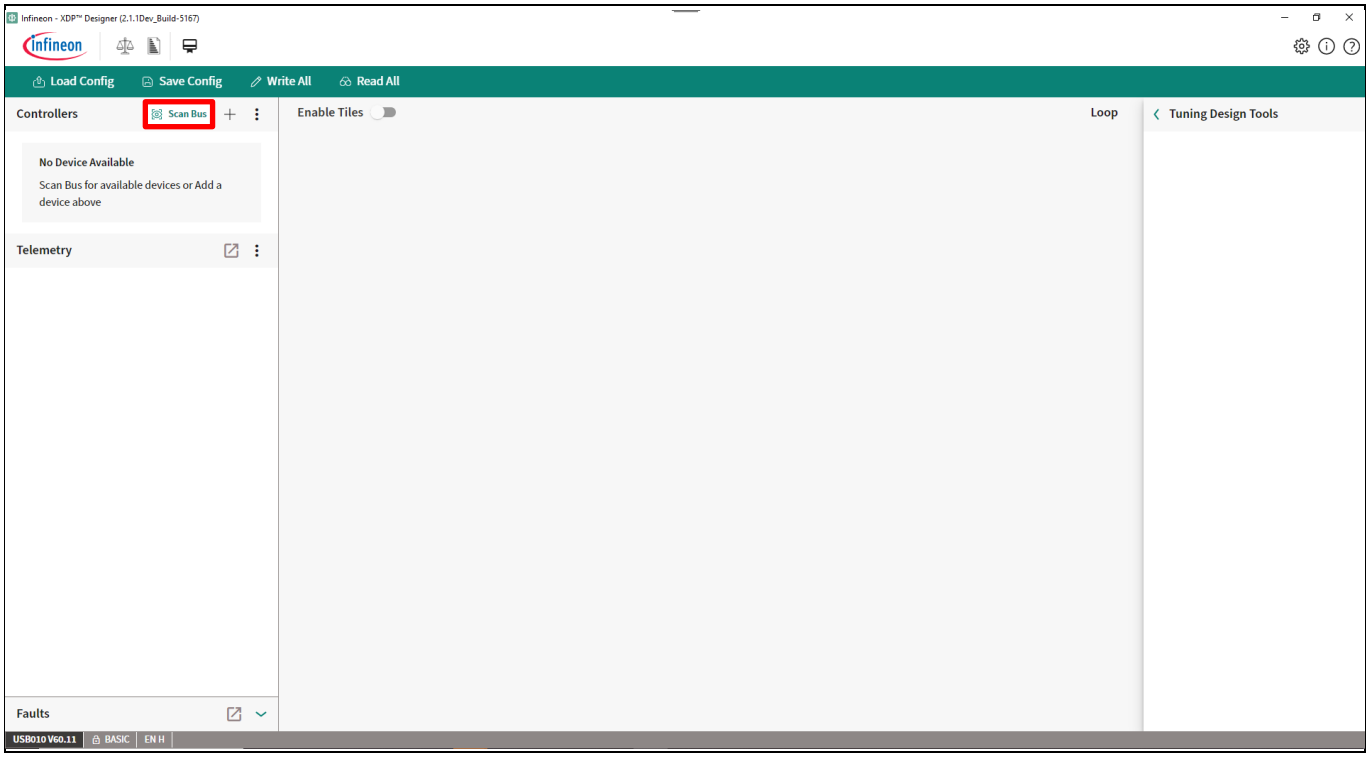


Figure 24 XDP711-001 detection

The detected device is XDP711-001, with the **Telemetry** displayed on the left as shown below:

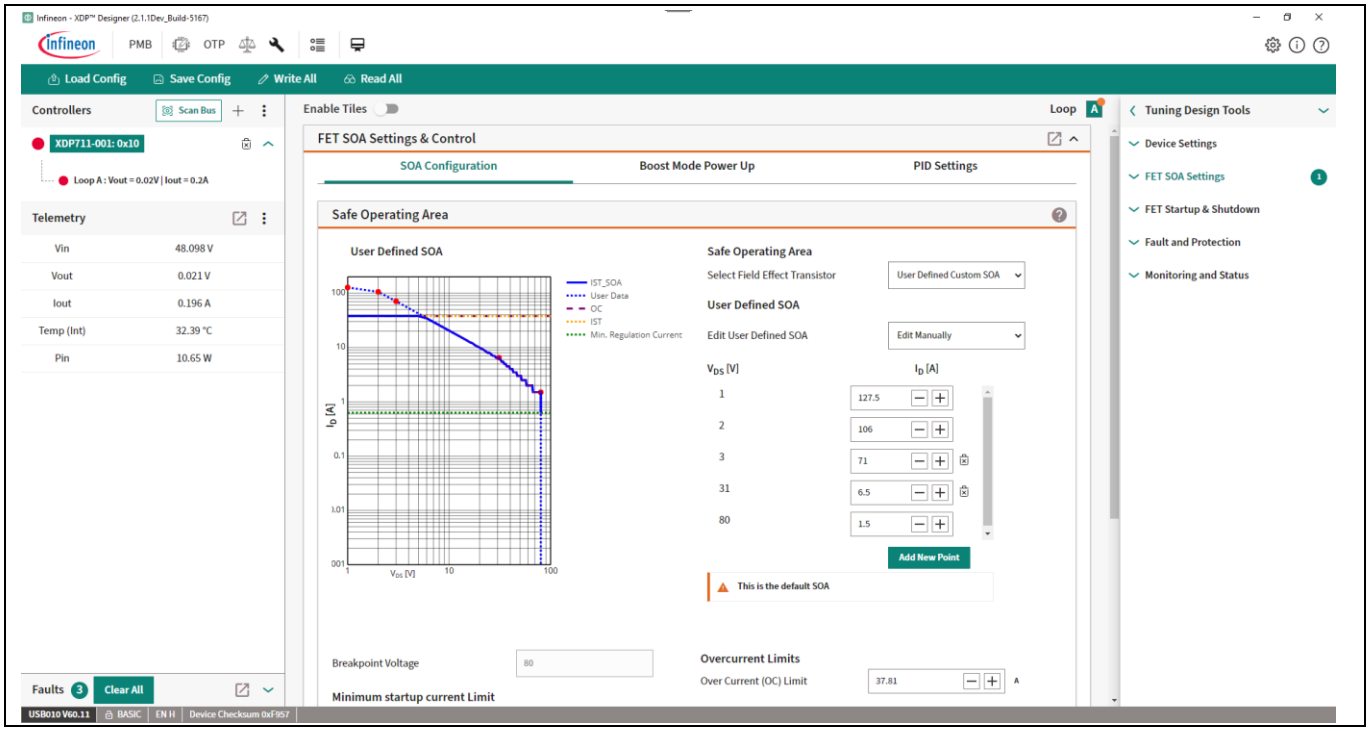


Figure 25 Live telemetry of the connected XDP711-001

Click **PMB** to view the PMBus® registers and the values stored in them

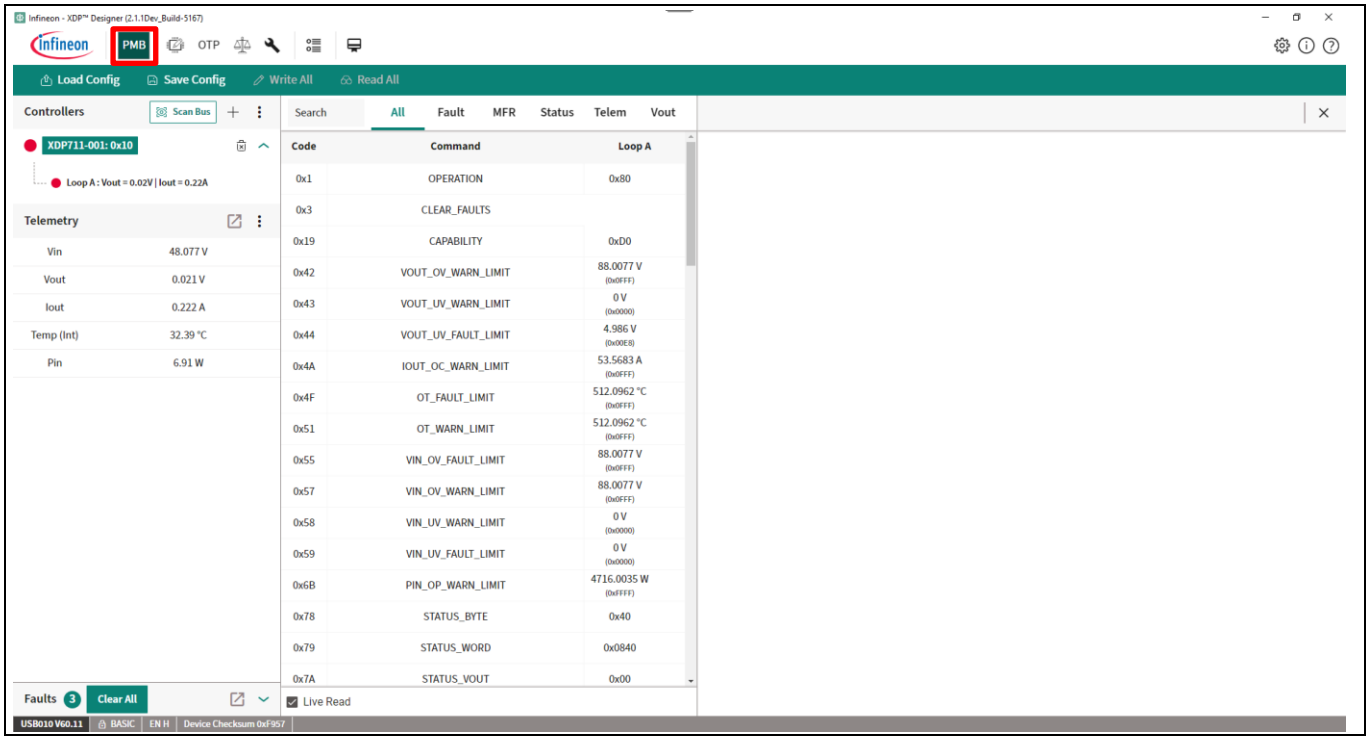


Figure 26 XDP™ Designer displaying all the PMBus® registers of the connected XDP710-002

4.1.3 Reading and writing registers

1. To edit a register individually, click on the corresponding PMBus® register, make the necessary changes, and then click **Write**

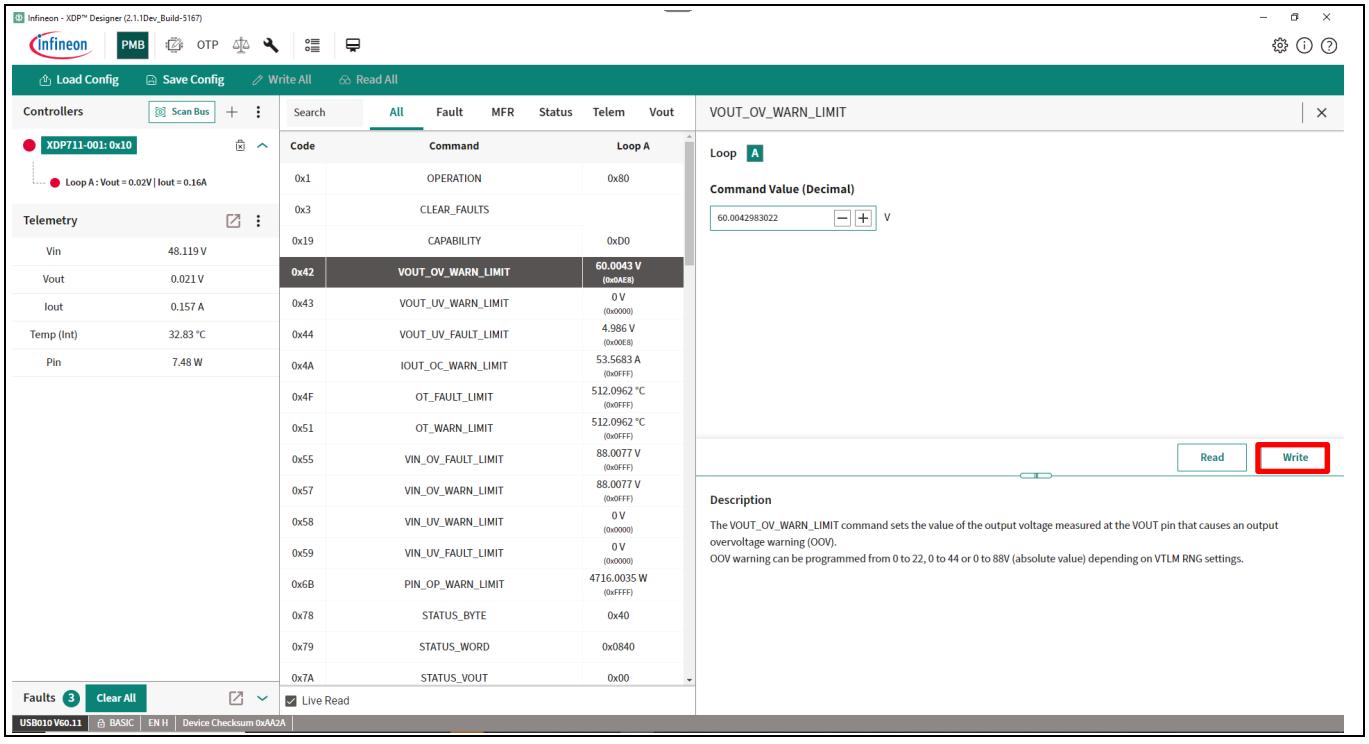


Figure 27 Editing VOUT_OV_WARN_LIMIT

- Most of the registers are updated automatically. Click **Read** to read the corresponding register values

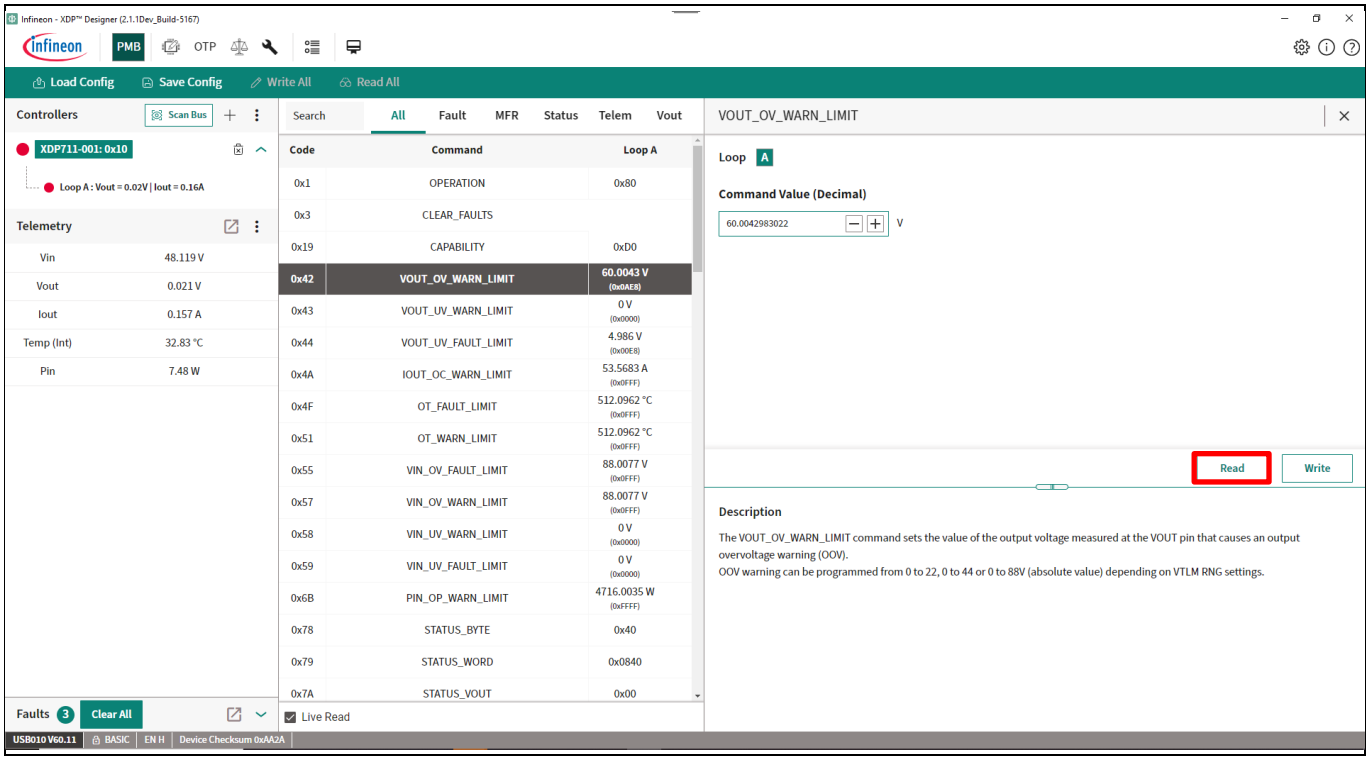


Figure 28 Reading VOUT_OV_WARN_LIMIT

4.1.4 Program FET

Note: If using analog-assisted digital mode (AADM), the FET is pre-programmed. You can skip this step.

Note: If using FDM, the FET must be programmed in the FET_SELECT bits of the MODE register (0xD1) according to the one populated on the board.

Note: The board has FET IPM018N10NM5LF2 populated. For this design, use the SOA profile of IPB017N10N5.

1. Select the IPB017N10N5 FET
2. Modify the FET_SELECT bit to 0xB and then click **Write**. See Figure 29

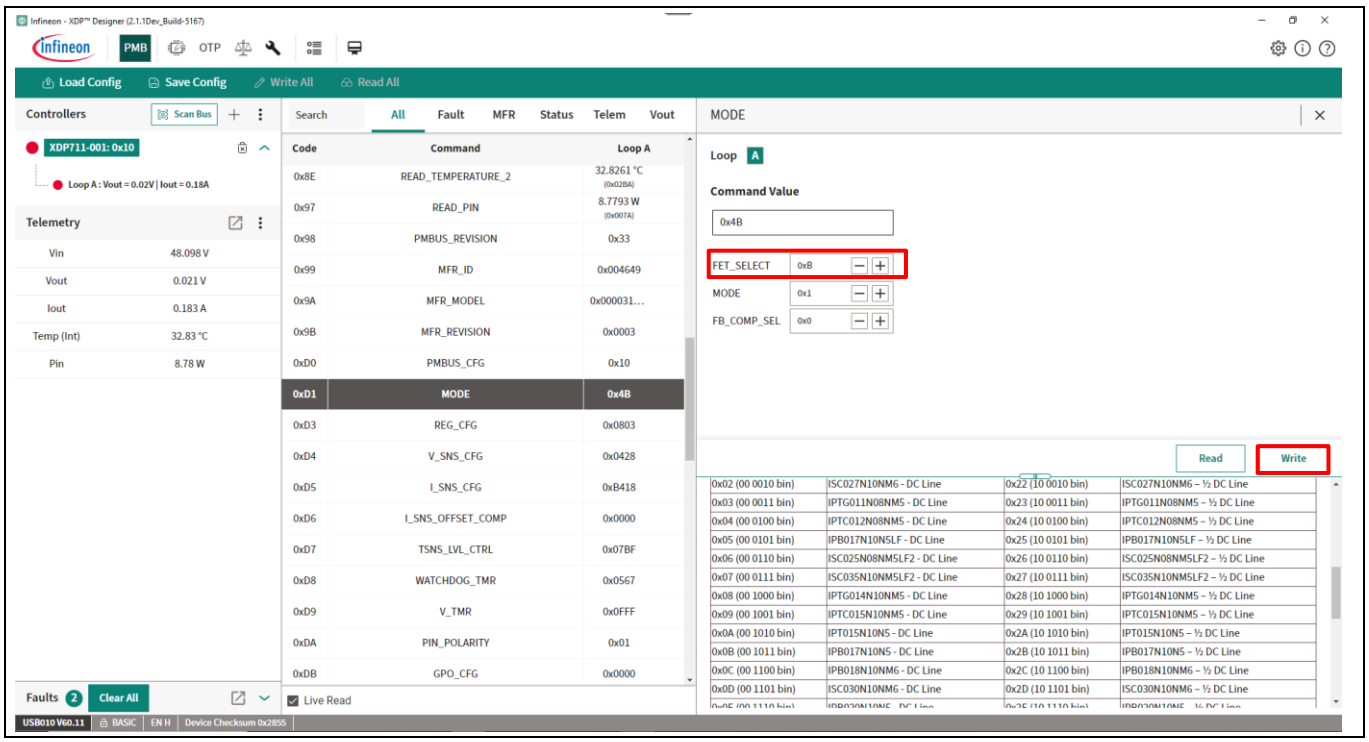


Figure 29 FET selection in FDM

4.1.5 Select the current sense range

Note: This design is intended for a 75 A overcurrent application. Therefore, the current sense range of CS_RNG of 25 mV is selected.

- Modify the register CS_RNG bit to 0x1, and then click **Write** as shown in Figure 30

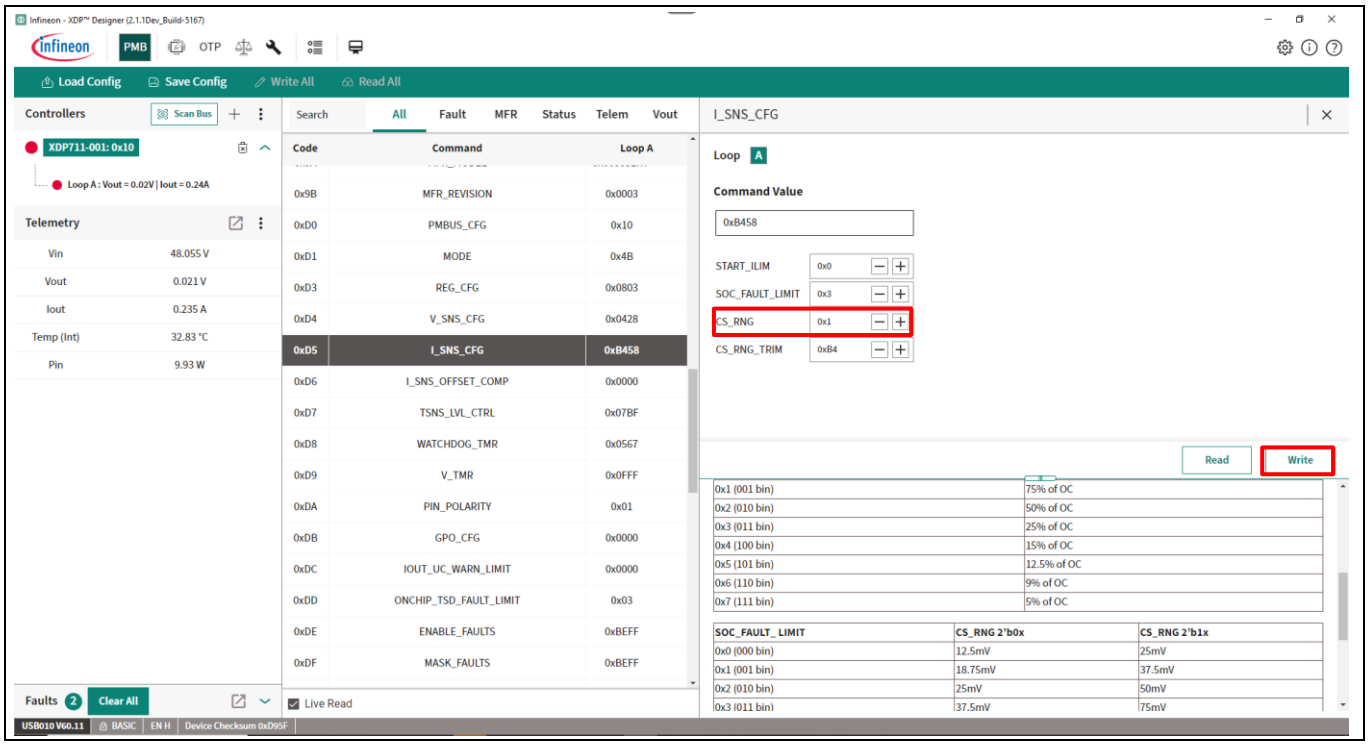


Figure 30 R_{sns} selection

4.1.6 Program Rsns

Note: The sense resistor value must be programmed in the R_{sns} bits of the REG_CFG register according to the one populated on the board.

- The board has R_{sns} **0.33 mΩ** populated. To select this resistor, modify the R_{sns} bit to 0x3, and then click **Write** as shown in Figure 31

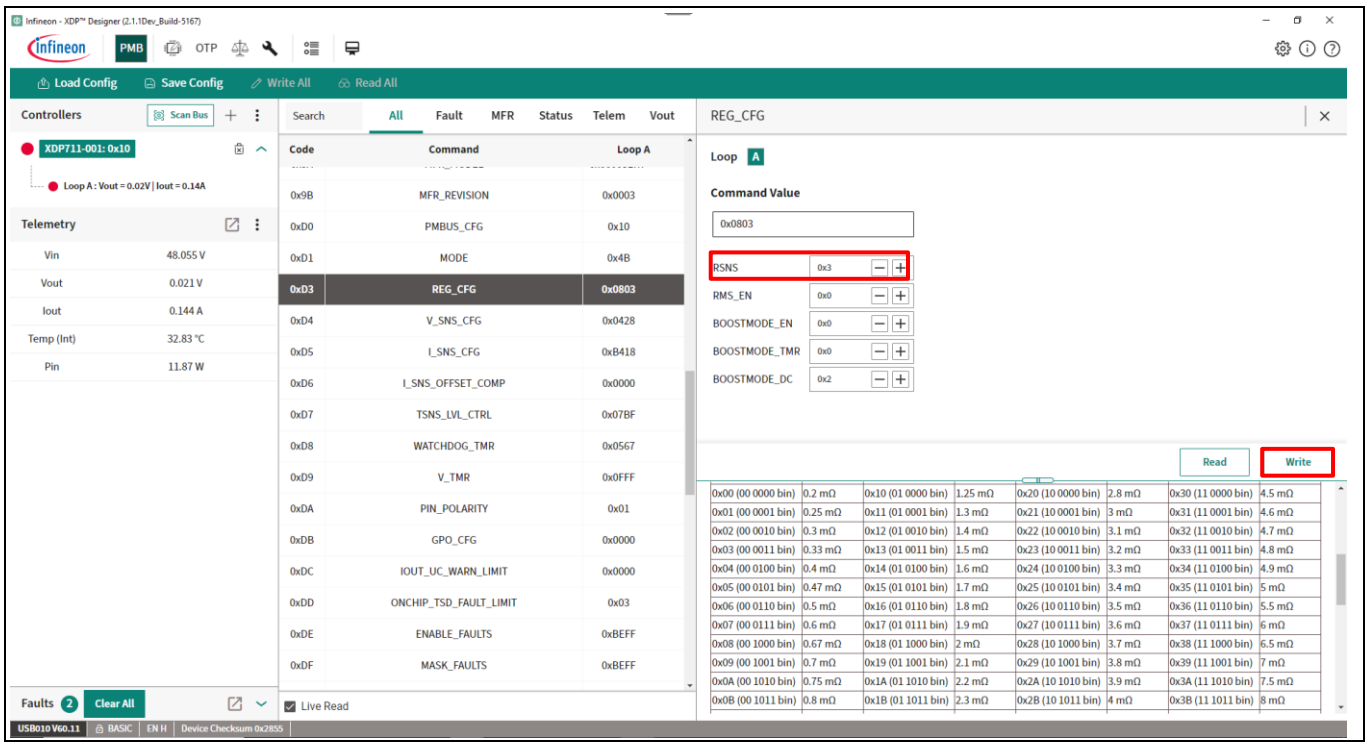


Figure 31 R_{sns} selection

4.1.7 Select the watchdog timer

Set the watchdog timer to be higher than the turn-on time to ensure that the watchdog timer does not expire before the turn-on. Keep in mind that the watchdog timer value must not be set much longer than the turn-on time to prevent damage to the FET in the event of a short-circuit during a turn-on. Select 100 ms for this design as shown in Figure 32.

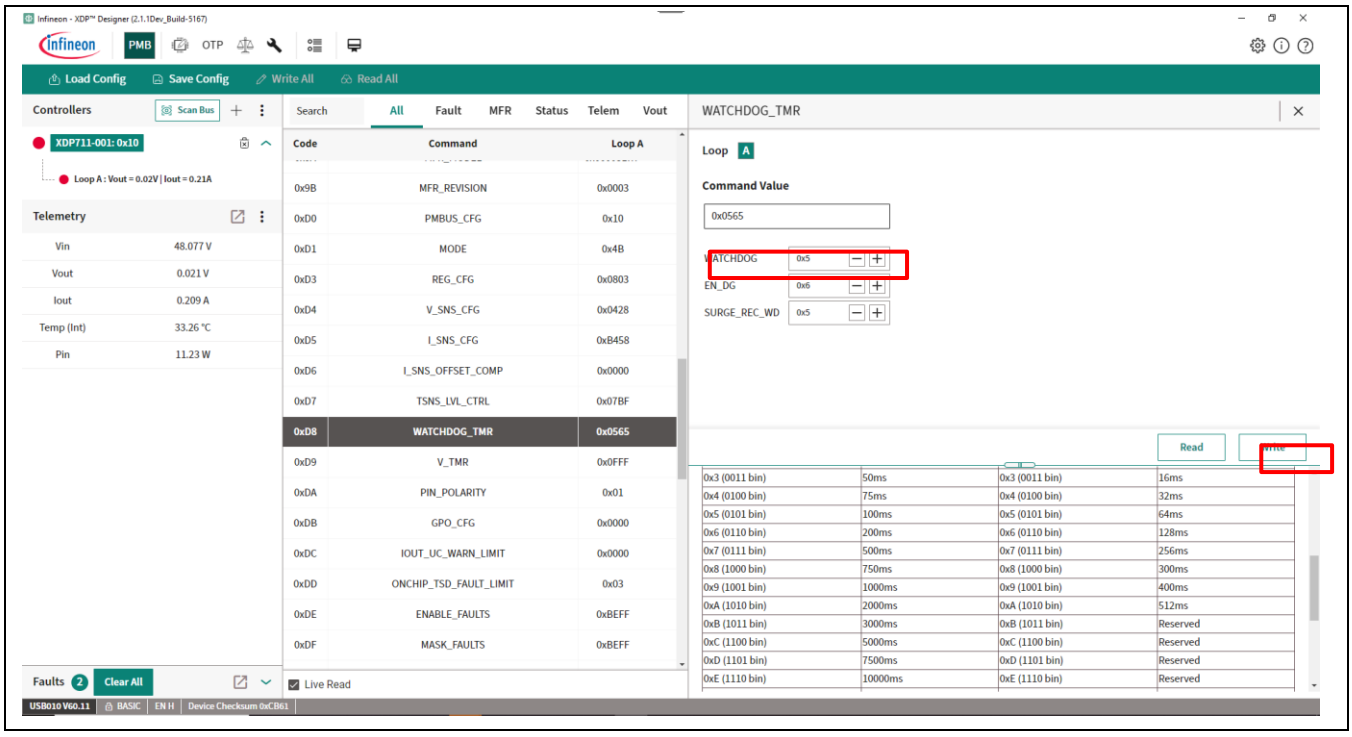


Figure 32 Watchdog timer selection

4.1.8 Program the current sense range (CS_RNG) and start-up current limit (IST)

Note: If using AADM, skip this step because the resistor on the IST pin selects the start-up current limit and current sense range.

In FDM, program the required current sense range and start-up current limit in the I_SNS_CFG register (0xD5), as shown in Figure 33.

1. This design is intended for a 75 A overcurrent application. Therefore, the current sense range (CS_RNG) of 25 mV is selected. Modify the register CS_RNG bit to 0x1, and then click **Write** as shown in Figure 33

- The maximum startup current is restricted to 5% of the (CS_RNG/Rsns). To select this startup current, modify the START_ILIM bit to 0x7, and then click **Write** as shown in Figure 33

Note: Do not set the current sense range as 50 mv with 0.33 mΩ sense resistor. The SOA regulation loop does not work when (Current Sense Range/ R(mΩ)) > 83.333 A.

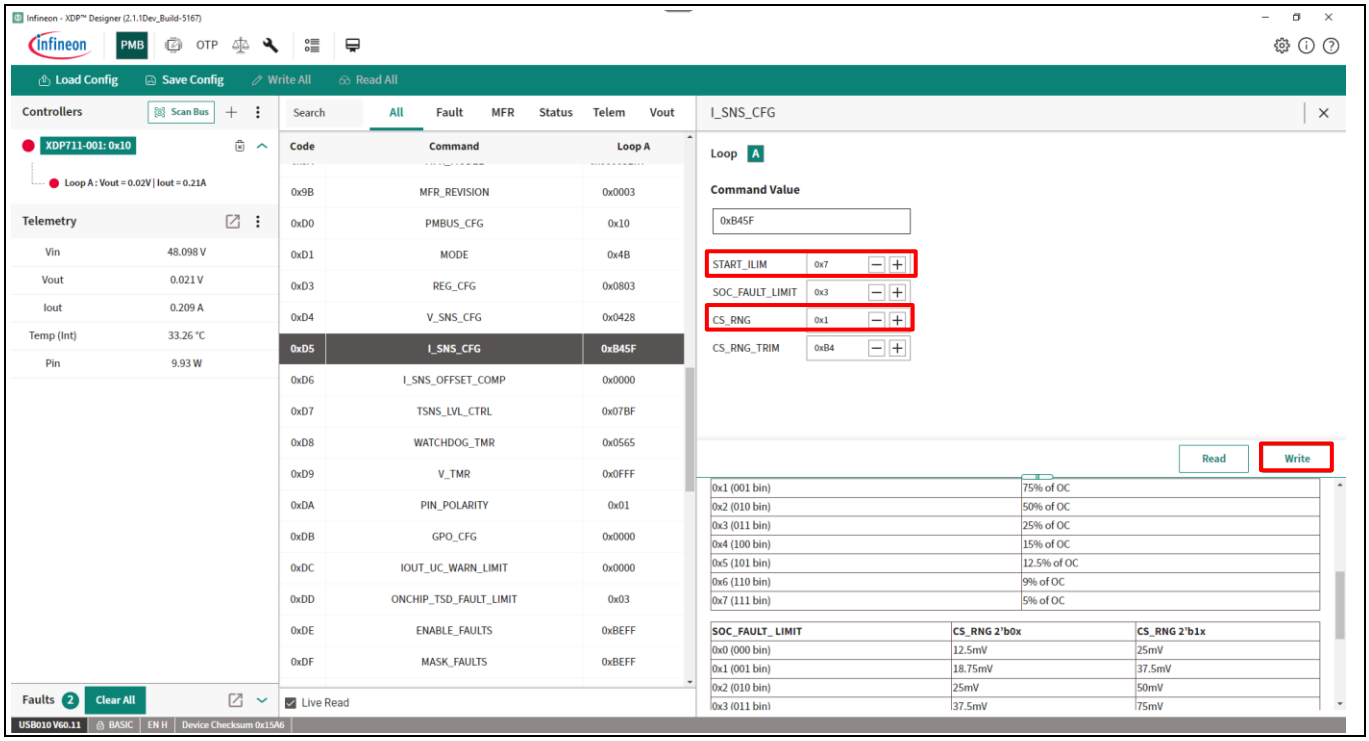


Figure 33 Current sense range and start-up current limit setting

4.1.9 Program VIN_UV_FAULT_LIMIT

Note: If using AADM or ACM, skip this step because the input undervoltage (UV) fault limit is set by external resistors on the UV pin.

In Digital Comparator Mode (DCM), program the desired undervoltage (UV) fault limit in the VIN_UV_FAULT_LIMIT register (0x59). If the UV fault is not used, the register can be programmed to 0 V, or the fault can be disabled. For this design, program VIN_UV_FAULT_LIMIT as **38 V**.

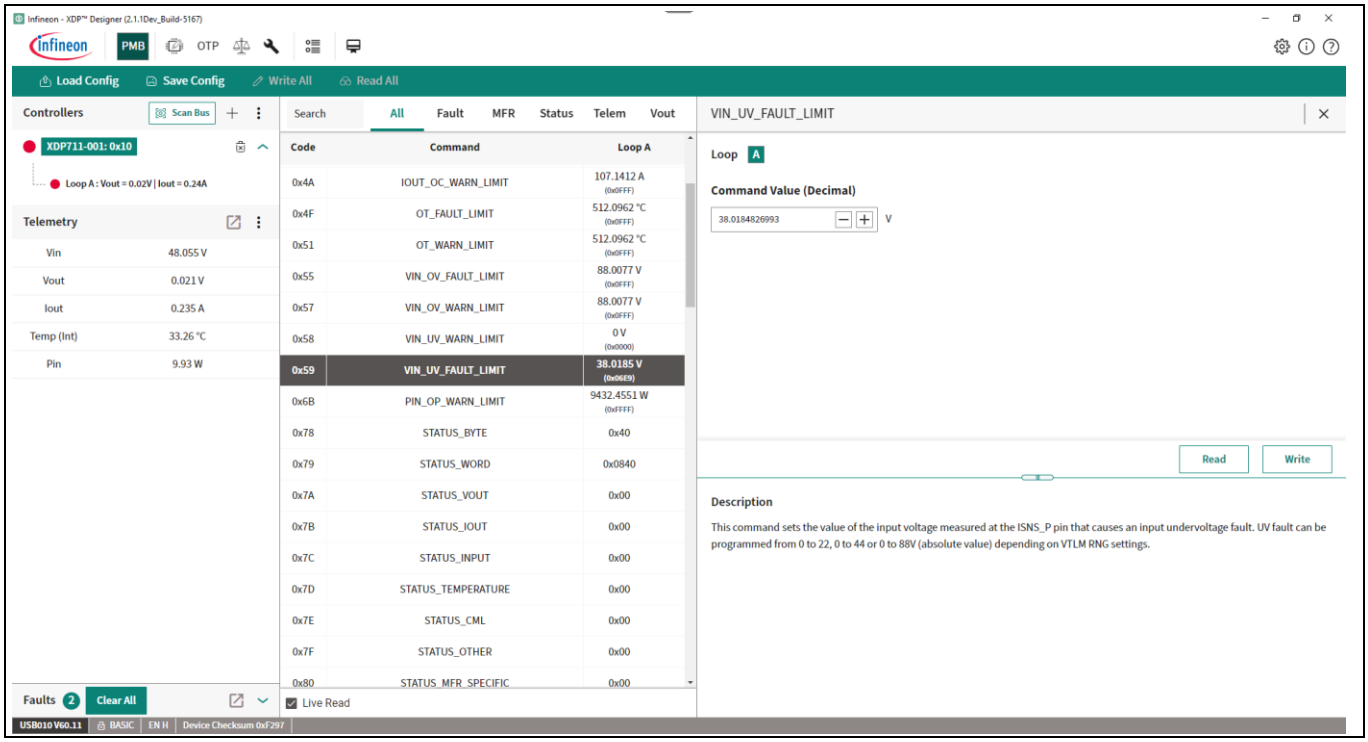


Figure 34 Program VIN_UV_FAULT_LIMIT

4.1.10 Program VIN_OV_FAULT_LIMIT

Note: If using AADM or ACM, skip this step because the input overvoltage (OV) fault limit is set by external resistors on the OV pin.

In DCM, program the required overvoltage (OV) fault limit in the VIN_OV_FAULT_LIMIT register (0x55). If the OV fault is not used, the register can be programmed to 88 V, or the fault can be disabled. For this design, program VIN_OV_FAULT_LIMIT as **62 V**.

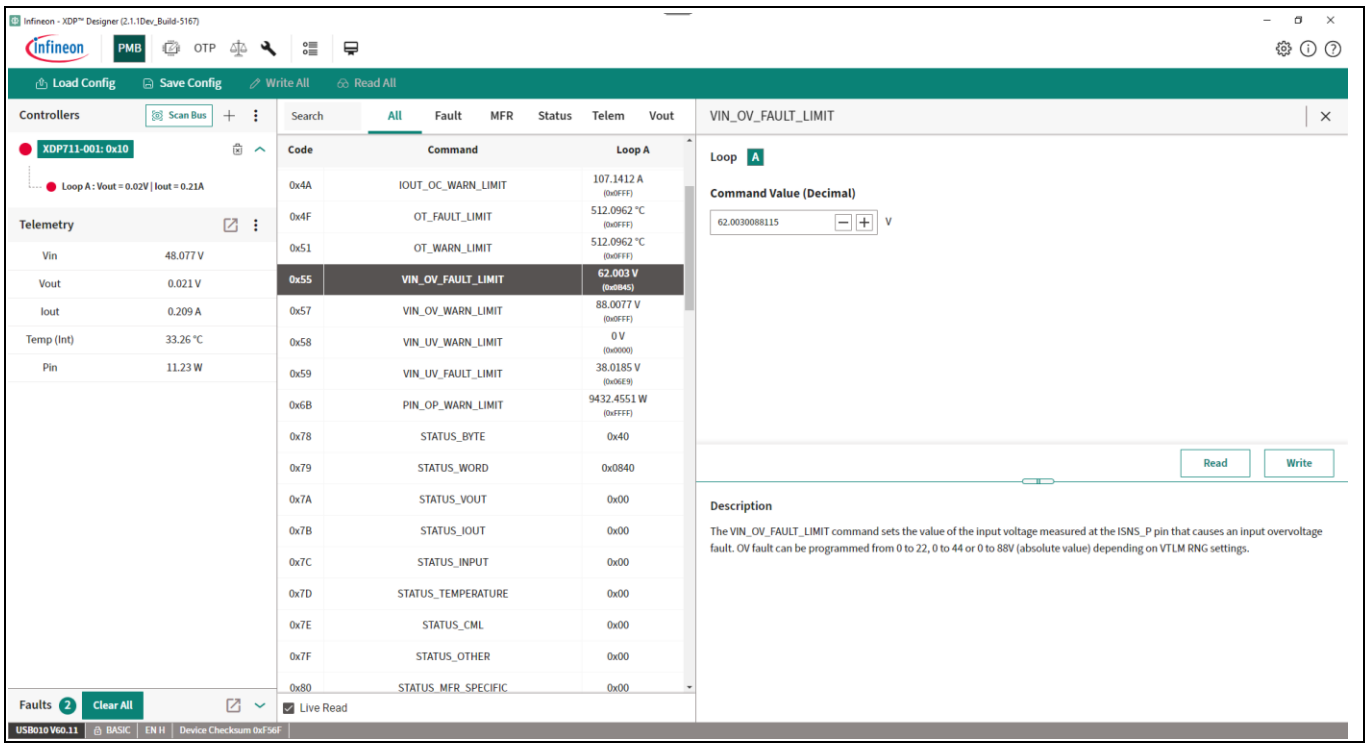


Figure 35 Program VIN_OV_FAULT_LIMIT

4.1.11 Program VOUT_UV_FAULT_LIMIT

Note: If using AADM or ACM, skip this step because the output UV fault limit is set by external resistors on the FB pin.

In DCM, program the required output undervoltage (UV) fault limit in the VOUT_UV_FAULT_LIMIT register (0x44). If the VOUT_UV fault is not used, the register can be programmed to 0 V, or the fault can be disabled. For this design, program VOUT_UV_FAULT_LIMIT as **34 V**.

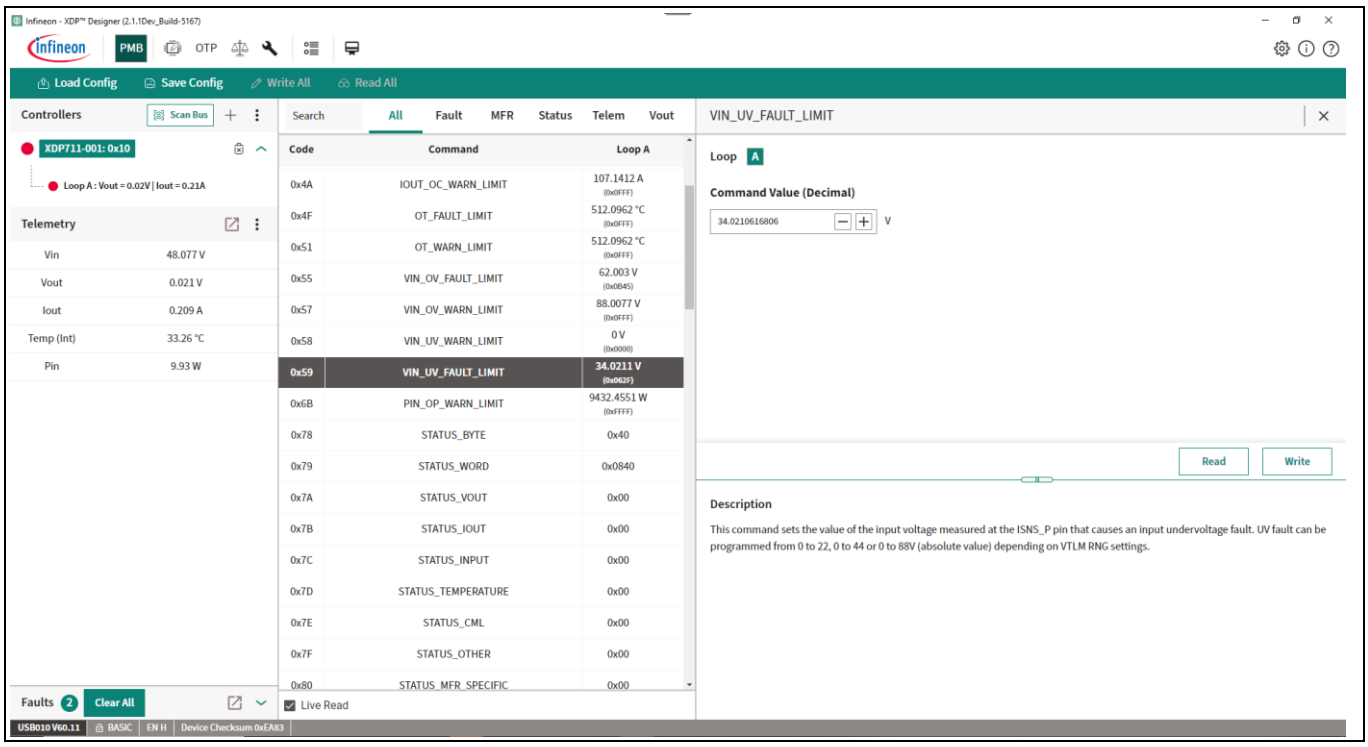


Figure 36 Program VOUT_UV_FAULT_LIMIT

4.2 XDP711-001 programming under different modes

There are two different modes in which the XDP711-001 can be operated: Fully-Digital Mode (FDM) and Analog Assisted Digital Mode (AADM). FDM has three selections: DCM, ACM, and Hybrid. AADM or FDM can be selected based on the resistor connected to the Mode 0 and Mode 1 pins on the evaluation board. Based on the mode selected, different PMBus® registers must be configured.

4.2.1 FDM

In FDM, you can select the FET, startup current limit, and current sense range via PMBus® registers. In DCM, the input and output voltage fault sensing are done via digital comparators and is based on the telemetry of the device, which reduces the amount of analog circuitry required while in ACM.

External voltage dividers are needed on the UV, OV, and FB pins, and the voltage on the divider is compared with the internal threshold to detect the faults. Voltage warnings are still set internally. The following PMBus® registers must be programmed in FDM for both DCM, ACM, and Hybrid:

- FET_SELECT: See Section 4.1.4
- R_{sns}: See Section 4.1.5
- Watchdog (optional): See Section 4.1.7
- Current sense range (CS_RNG) and startup current limit (IST): See Section 4.1.8
- Telemetry enable
- Enabling warnings (if needed)
- Setting warnings (if needed)

4.2.2 FDM (DCM)

If the device is programmed using DCM, select the DCM in register 0xD1 and modify bit '7' to '1'. Modify the following register to detect the necessary faults if the corresponding fault bits are enabled in PMBus® register (0xDE):

- VOUT_UV_FAULT_LIMIT (0x44): See Section 4.1.11
- VIN_OV_FAULT_LIMIT (0x55): See Section 4.1.10
- VIN_UV_FAULT_LIMIT (0x59): See Section 4.1.9

To turn on the FET, reduce the voltage on Pin 4 of X3 to 0 V.

4.2.3 FDM (ACM)

If the device is programmed using ACM, select ACM in register 0xD1 and modify bit 7 to '0'. In this mode, all the voltage faults are sensed using external resistors. Therefore, the following jumpers must be placed on the evaluation board to detect necessary faults if the corresponding fault bits are enabled in the PMBus® register (0xDE):

- **VOUT_UV_FAULT_LIMIT (FB pin)**: Jumper is required on connector X4; the output UV fault limit can be modified by modifying R9 and R10
- **VIN_OV_FAULT_LIMIT (OV pin)**: Jumper is required on connector X41; the input OV fault limit can be modified by modifying R34, R36, and R38
- **VIN_UV_FAULT_LIMIT (UV pin)**: Jumper is required on connector X33. If UV_FAULT is disabled, ensure that the UV pin gets the necessary enable signal voltage to turn on the FET

4.2.4 FDM (Hybrid)

If the device is programmed using Hybrid, select ACM in register 0xD1 and modify bit 7 to '0'. In this mode, the input voltage faults are sensed digitally while the output undervoltage fault is sensed using external resistors. Therefore, the following jumpers must be placed on the evaluation board to detect necessary faults if the corresponding fault bits are enabled in the PMBus® register (0xDE):

- **VOUT_UV_FAULT_LIMIT (FB pin)**: Jumper is required on connector X4; the output UV fault limit can be modified by modifying R9 and R10
- **VIN_OV_FAULT_LIMIT (0x55)**: See Section 4.1.10
- **VIN_UV_FAULT_LIMIT (0x59)**: See Section 4.1.9

4.2.5 AADM

In AADM, you can select the FET, startup current limit, and current sense range via external resistors connected on pins Mode 0, Mode 1, and IST. For the evaluation board, the settings are done as shown in Table 7.

Table 7 AADM selection resistors

Connector	Jumper position (resistor)	Function
X18 (mode pins)	No jumper (Mode 0: Open)	Selects the FET IPB017N10N5ATMA1
	Between 9 and 10 (Mode 1: 20 kΩ (2.0 V))	

Connector	Jumper position (resistor)	Function
X21 (IST pins)	Between 7 and 8 recommended (IST: 15 kΩ (1.5 V)) and depopulate R65.	25 mV current sense range is selected, and 12.5 percent of overcurrent (OC) level is selected.

The following jumpers must be placed on the evaluation board to detect the necessary faults if the corresponding fault bits are enabled in PMBus® register (0xDE):

- **VOUT_UV_FAULT_LIMIT (FB pin)**: Jumper is required on connector X4; the output UV fault limit can be modified by modifying R9 and R10
- **VIN_OV_FAULT_LIMIT (OV pin)**: Jumper is required on connector X41; the input OV fault limit can be modified by modifying R34, R36, and R38
- **VIN_UV_FAULT_LIMIT (UV pin)**: Jumper is required on connector X33. If UV_FAULT is disabled, ensure that the UV pin gets the necessary enable signal voltage to turn on the FET

Modify the necessary PMBus® registers for proper operation:

- R_{sns}: See Section 4.1.5
- Watchdog: See Section 4.1.7
- Telemetry enable
- Enabling warnings (if needed)
- Setting warnings (if needed)

5 Loading the configuration file

This section describes how to load the configuration file directly into the device, which eliminates the need to manually modify the required register. Do the following to load the configuration file into the device:

1. Click **Load Config**, as shown in Figure 37

- Click **Browse** and select the *.xdp* file that needs to be loaded onto the device, as shown in Figure 38
- Click **Load** to load the necessary configuration onto the device, as shown in Figure 39

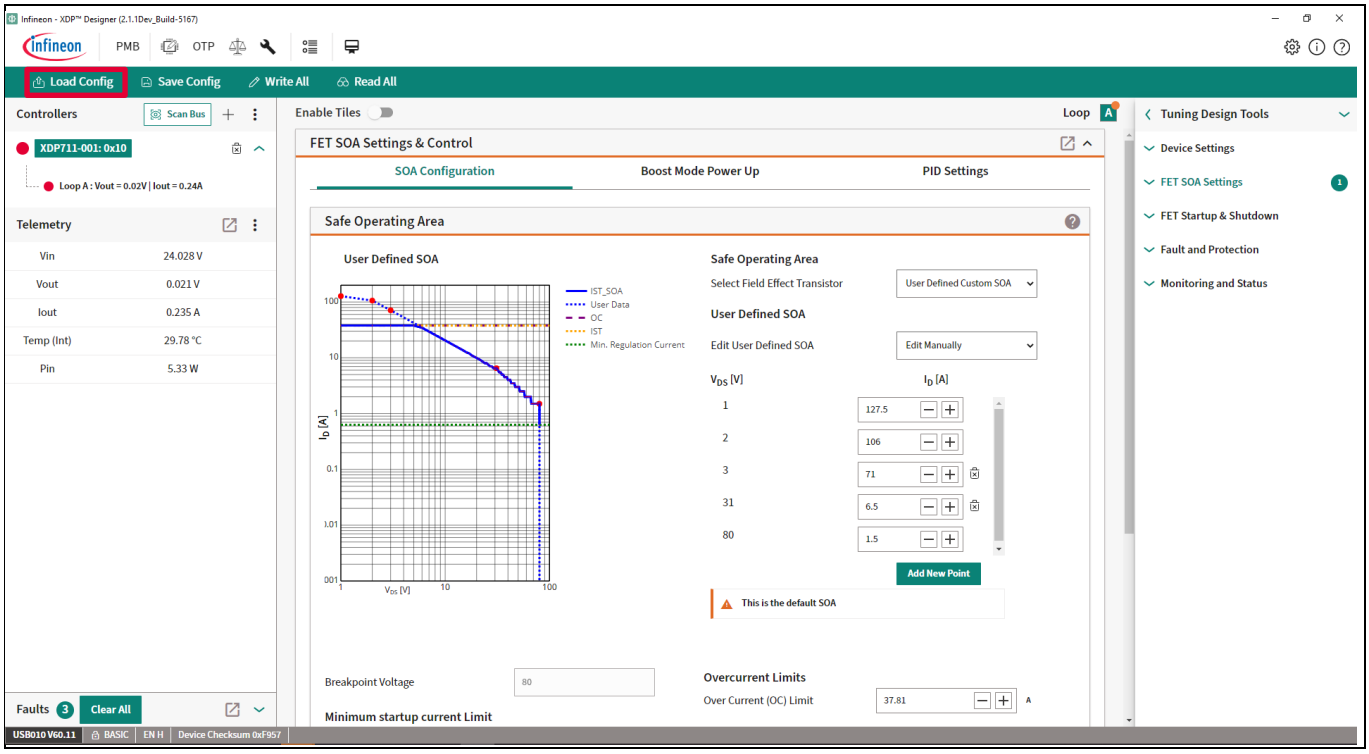


Figure 37 Select Load Config option



Figure 38 Browse to select the necessary configuration file

Loading the configuration file

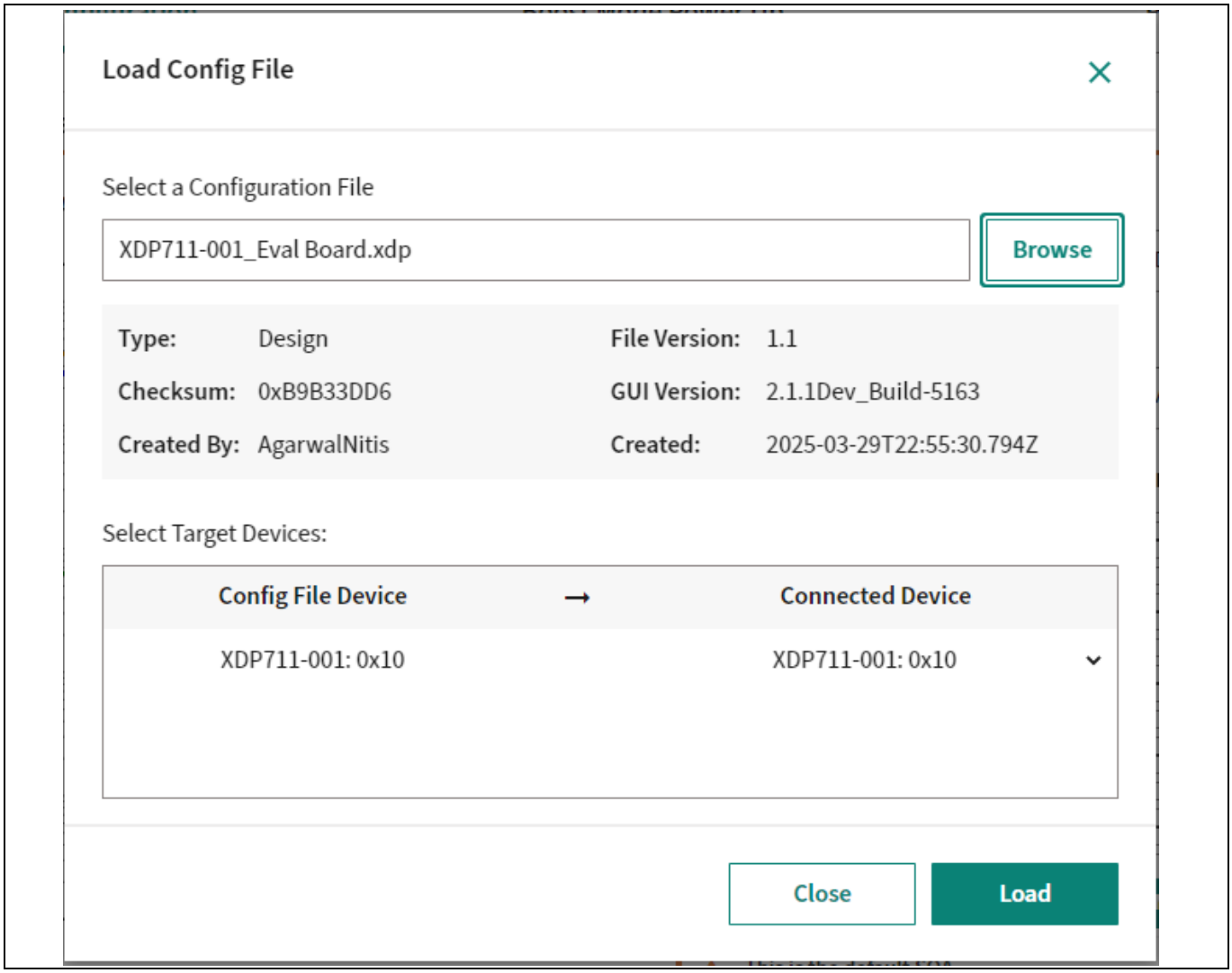


Figure 39 Load the selected configuration file

An example configuration file in .txt format is available on the XDP710-002 Evaluation Board page [2] as *XDP711-001_EvalBoard.xdp*. This configuration file is compatible with the evaluation board in the default configuration.

6 XDP711-001 evaluation

For this section, it is assumed that the proper input voltage (52 V) is available on the input of the evaluation board and the example config is loaded onto the device and the device is not yet enabled.

6.1 Turn-on FET test

To turn on the FET, reduce the voltage on pin 4 of X3 to 0 V.

Note: Ensure that the load is not on when enabling the FET because it could lead to a watchdog timer fault and the FET will not be able to turn on.

Turn-on waveforms are shown in Figure 40. This test was done with 1200 µF of added load capacitance. It is observed that the startup current closely follows the programmed SOA of the FET shown in Figure 40 and ensures that the FET SOA is not violated during turn-on operation, which provides a safe and fast turn-on. Additionally, the maximum startup current observed is 4 A at an IST setting of 5%.

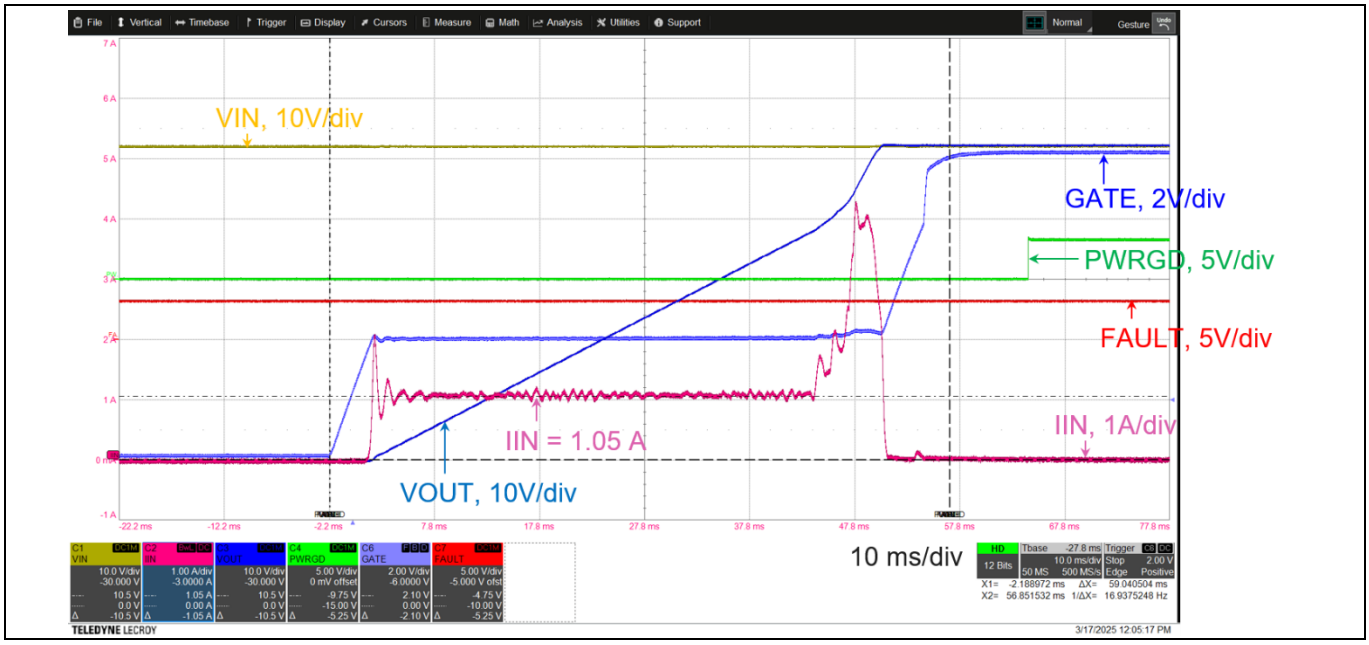


Figure 40 Startup current waveform at 52 V input

6.2 Boost mode test

For FETs with weaker SOA with current capability of less than 0.25 A at higher voltages, it is recommended to turn on the FET with boost mode. In the following example, boost mode is enabled and with the parameters set as follows:

- Type of boost mode: Automatic boost mode
- SOA line: 1 ms
- Duty cycle: 20%

If the SOA is below 0.5 A, boost mode is activated. The controller sends out gate pulses allowing the drain current for only 1 ms with its limit restricted to 8x the programmed SOA level. When the regulation current reaches 0.5 A, boost mode is turned off and the FET is regulated with regular SOA. Figure 41 shows the startup behavior with automatic boost mode and at V_{DS} = 28 V, where I_{SOA} = 0.5 A, and the controller resumes with regular current regulation.

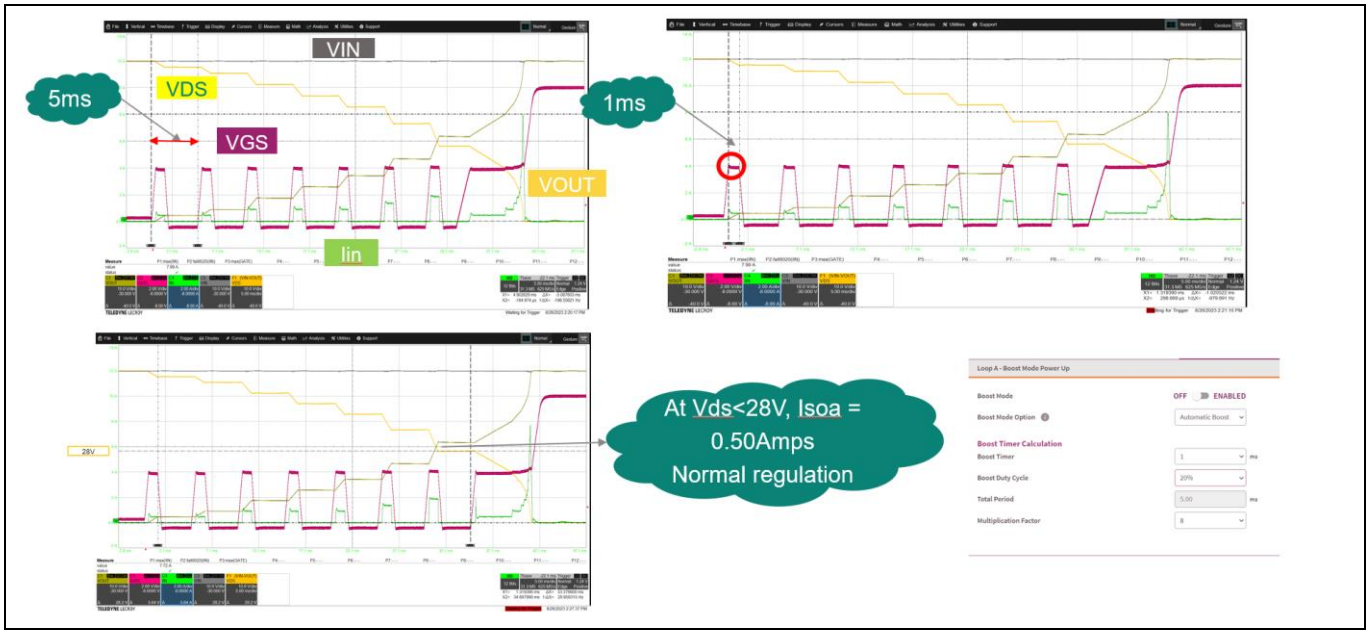


Figure 41 Automatic boost mode operation

Attention: ***Set the duty cycle according to C_{gs} to provide sufficient time for the gate to discharge to avoid double pulses and violation of SOA on 1 ms line.***

6.3 Overcurrent fault test

The overcurrent (OC) fault test is performed, and the overcurrent fault module is set to the following settings:

- Overcurrent level: 12 A
- SOA deglitch timer (SOAD_TMR): 1 ms
- SOA regulation timer (SOAR_TMR): 10 ms

From Figure 42, it can be observed that when the current reaches a level of 12 A, it is blanked for 1 ms as set by the SOAD_TMR. After SOAD_TMR expires, the gate voltage is reduced to regulate the current at 12 A for defined time of 10 ms set by the SOAR_TMR. During this time, if the current does not go below 12 A, the FET is turned off and an OC fault is declared.

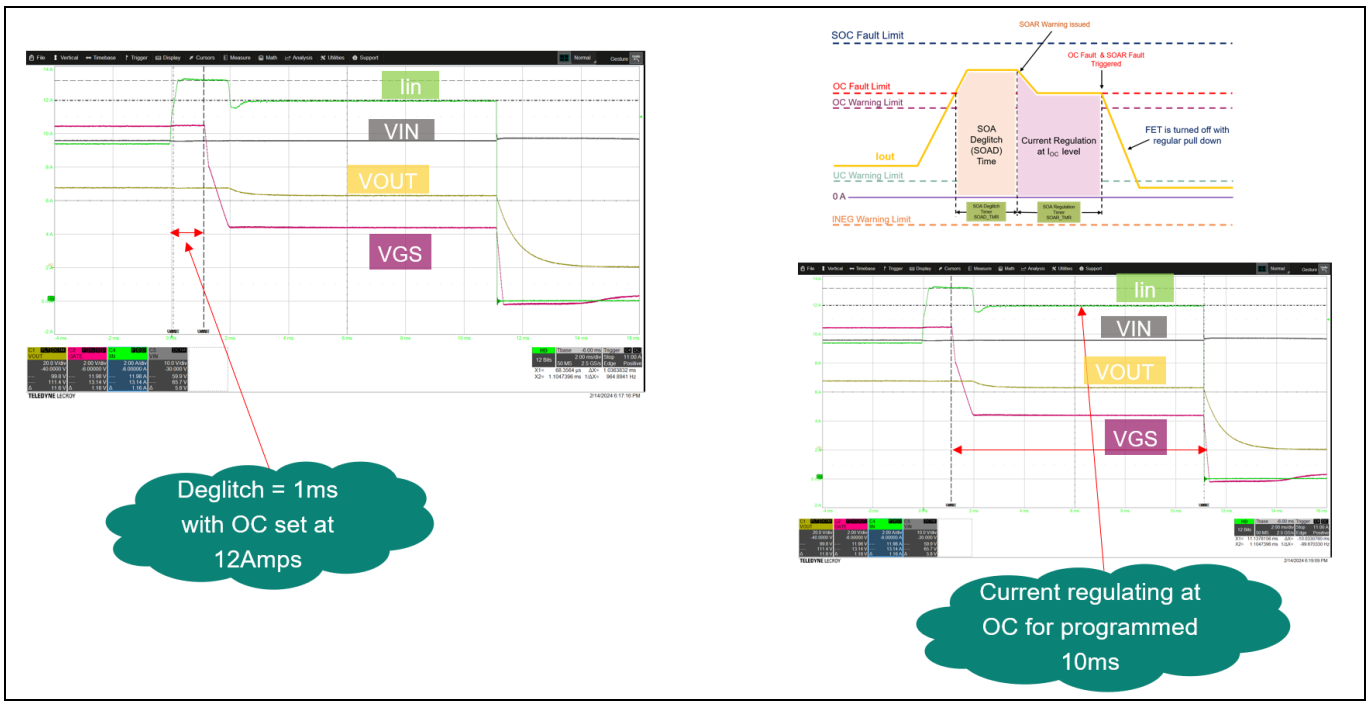


Figure 42 Overcurrent fault and regulation

6.4 Severe overcurrent fault test

XDP711-001 provides fast detection of severe overcurrent (SOC) faults by turning off the FET within 1 µs from detection to full turn-off by sinking 1.5 A of current out from the gate. The SOC fault module is set as follows in the following example:

- SOC fault limit: 18.75 A
- SOC_DG_TMR: 500 ns
- SOC_TMR: 0 µs
- One-step shutdown

Figure 43 shows the SOC fault detection and the fast turn-off feature of XDP711-001. Note that the deglitch is added to highlight the feature of XDP711-001 to ignore noise if expected. It is observed that after the deglitch time of 500 ns, the FET is turned off within 475 ns and SOC fault is declared.

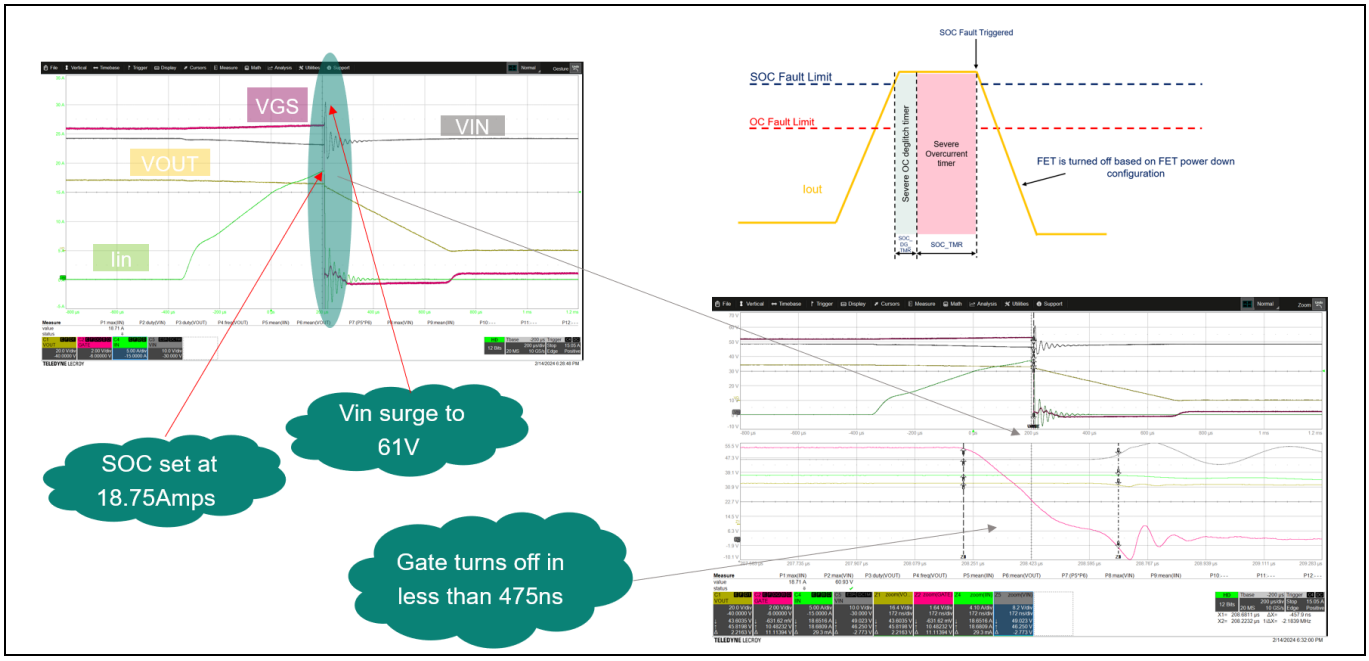


Figure 43 Severe overcurrent fault detection

6.5 Two-step turn-off test

It is observed from Figure 44 when the FET is turned off with a strong pull-down, due to inductance of input lines, the voltage spikes are induced on the input voltage (Vin). This adds stress on the FET and the system. In a two-step shutdown, the turn-off process is split into two sinks levels: the internal 200 Ω resistors is turned on for the time defined by the GATE_PD_TMR and after timer expires, the sink level is switched to current defined by the GATE_SLOW_PD (250 µA, 500 µA, 750 µA, or 1250 µA).

For testing, the two-step shutdown is set with GATE_PD_TMR = 4000 ns and GATE_SLOW_PD= 750 µA. Figure 44 shows the two-step gate turn off. Notice that the ringing on Vin has been significantly reduced at the expense of increasing the turn-off time.



Figure 44 Two-step shutdown to turn off MOSFET after SOC fault

7 Programming SOA, OTP, and MTP

As specified in the XDP711-001 datasheet [1], to program the desired settings in internal commands or OTP at power-up, follow these steps:

1. Apply a voltage at the VDD_VIN and ISNS_P pins:
   - At least 5.5 V to program commands into volatile memory
   - At least 20 V to program OTP or MTP
2. Keep the UV/EN pin at chip GND potential

   Communication via PMBus® is possible as soon as the STANDBY state is entered. At this point, commands, OTP, or MTP can be programmed.

3. To ensure successful programming, ensure that the internal temperature of the device stays below 125°C

To program OTP or MTP sections:

- Program the commands in volatile memory as required
- Click the button highlighted as shown in Figure 45

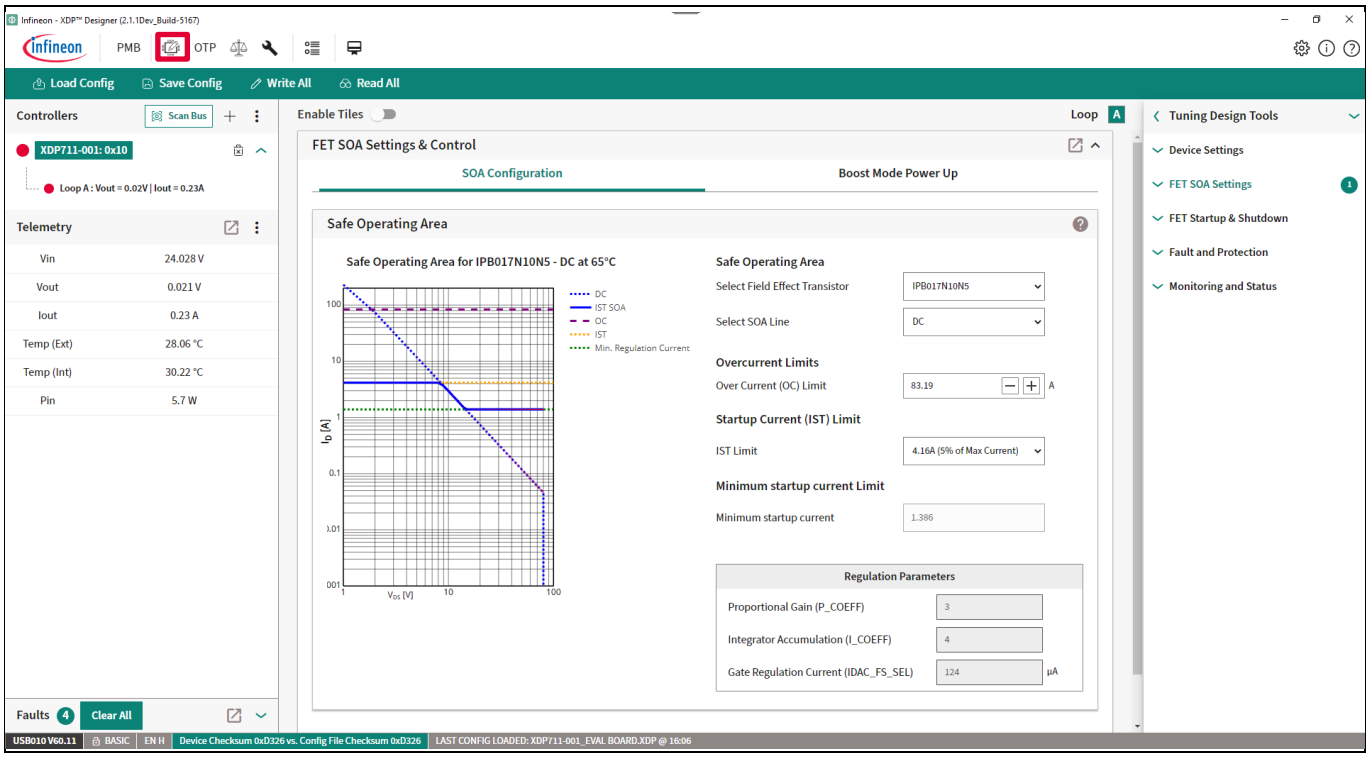


Figure 45 Programming tab

- Set the program from **Registers**, select the memory section that needs to be programmed and then click **Program to OTP**, as shown in Figure 46

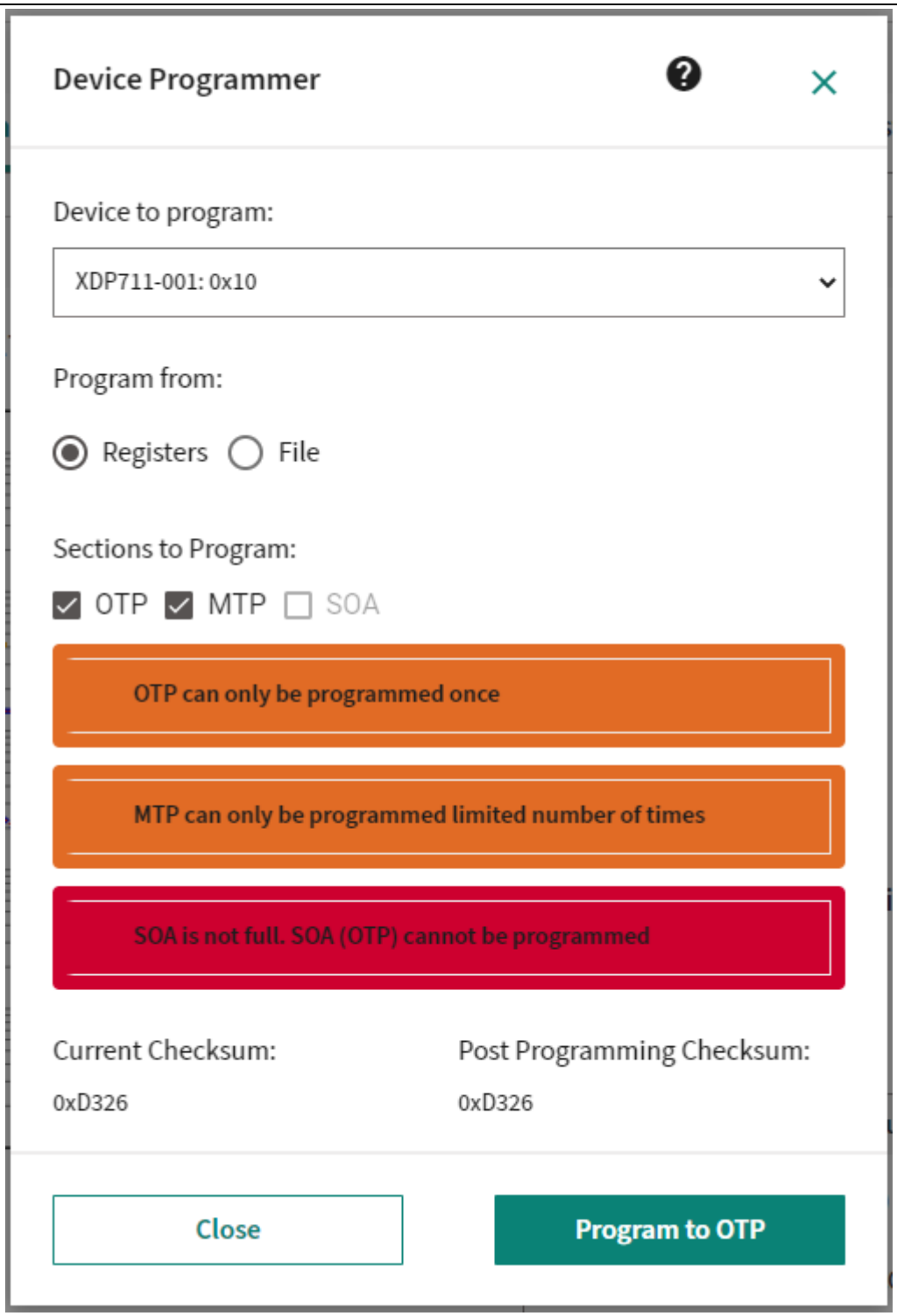


Figure 46 OTP and MTP programming

The command configuration will be automatically copied to the selected memory section.

References

Note: Contact Infineon Support to obtain these documents.

[1] Infineon Technologies AG: *XDP711-001 hot-swap controller datasheet;*

[2] Infineon Technologies AG: *XDP711-001 Evaluation Board webpage*;

[3] Infineon Technologies AG: *External fast switch-off circuit for XDP™ XDP7xx hot-swap controllers*; Available online

[4] Infineon Technologies AG: EVAL_XDP711-001 Evaluation board for XDP711-001; Available online

Revision history

Document revision	Date	Description of changes
V 1.0	2023-08-11	Initial release
V 1.1	2025-06-30	Added XDP710-002 evaluation Section Updated configuration file

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