TDA38540 dual-phase Evaluation Board user manual

80 A dual-phase Buck regulator with 1.0 V output

About this document

Scope and purpose

This user manual describes the operation, schematic, and bill of materials (BOM) for the EVAL_TDA38540_1Vout_2P Evaluation Board. The detailed application information for TDA38540 is available in the TDA38540 datasheet [1].

Intended audience

This document is intended as a guide for design engineers evaluating TDA38540 performance with the engineering EVAL_TDA38540_1Vout_2P Evaluation Board.

Important notice

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Safety precautions

Note: Please note the following warnings regarding the hazards associated with development systems.

Table 1 Safety precautions

	**Warning:** *The DC link potential of this board is up to 1000 VDC. When measuring voltage waveforms by oscilloscope, high-voltage differential probes must be used. Failure to do so may result in personal injury or death.*
	**Warning**: *The evaluation or reference board contains DC bus capacitors, which take time to discharge after removal of the main supply. Before working on the drive system, wait 5 minutes for capacitors to discharge to safe voltage levels. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Warning:** *The evaluation or reference board is connected to the grid input during testing. Hence, high-voltage differential probes must be used when measuring voltage waveforms by an oscilloscope. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Warning:** *Remove or disconnect power from the drive before you disconnect or reconnect wires, or perform maintenance work. Wait five minutes after removing power to discharge the bus capacitors. Do not attempt to service the drive until the bus capacitors have discharged to zero. Failure to do so may result in personal injury or death.*
	**Caution:** *The heat sink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.*
	**Caution:** *Only personnel familiar with the drive, power electronics and associated machinery should plan, install, commission and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.*
	**Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	**Caution:** *A drive that is incorrectly applied or installed can lead to component damage or reduction in product lifetime. Wiring or application errors such as undersizing the motor, supplying an incorrect or inadequate AC supply, or excessive ambient temperatures may result in system malfunction.*
	**Caution:** *The evaluation or reference board is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials that are unnecessary for system installation may result in overheating or abnormal operating conditions.*

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1 Introduction

The TDA38540 is a stackable synchronous buck converter, providing a compact, high-performance, and flexible solution in a small 6 mm x 5 mm power QFN package.

The key features offered by the TDA38540 are:

- Standalone or stackable 2-phase, 3-phase, or 4-phase operation with up to 40 A/phase
- Internal digital soft-start, precision 0.6 V reference voltage
- Power good (PGood) signal
- Thermal protection
- Programmable switching frequency in the range of 400 kHz to 2 MHz
- Optional synchronization to an external clock signal
- Enable input, output undervoltage protection (UVP), output overvoltage protection (OVP), and pre-bias startup
- Output overcurrent protection (OCP) function is implemented by sensing the voltage developed across the on-resistance of the synchronous MOSFET for optimum cost and performance, and the current limit is thermally compensated.

2 Dual-phase Evaluation Board

2.1 Board features

- Vin = +12 V, V_{out} = +1.0 V at 0-80 A
- Fsw = 600 kHz/800 kHz/1000 kHz
- L= 150 nH (12.4 mm x 8.3 mm x 8.0 mm, DCR = 0.15 mΩ)
- Cin = 20 x 22 µF (25 V, ceramic 0805) + 2 x 330 µF (25 V, electrolytic, optional)
- Cout = 12 x 47 µF (6.3 V, ceramic 0805) + 4 x 470 µF (2 V, 6 mΩ, SP-cap)

2.2 Connections and operating instructions

The TDA38540 dual–phase Evaluation Board requires a single +12 V for the input power and can deliver up to 80 A load current (TDC). The operation modes and OCP limits can be selected through jumpers.

Table 2 Connections

Label			Descriptions
Input	PVin	J1, J3	Connect input power (+12 V) to this pin
	GND	J2, J4	Return of input power
	PVin, GND	1P2 and 2P2	Sense pins for the input voltage
Output	Vout	1TB1, 2TB1	Connect a load (80 A max) to this pin
	GND	1TB2, 2TB2	Return of V_{out}
	Vout, GND	1P8, 2P8	Sense pins for the output voltage
Enable	EN, GND	1P1, 2P1	Connect a scope probe to this pin to monitor enable signal or an external enable signal can be applied to this pin to over-drive the onboard enable signal
Bode	BODE A, B	1P7	For bode plot measurement
Fsw	RT	1P27, 1P28, 1P29, 1P30, 1P35	Use a jumper to make one of the eight F_{sw} selections (1P27–1P30) for the primary phase. The board is designed for 600 kHz, 800 kHz and 1000 kHz. 1P35 is used to monitor RT signal for test purpose.
		2P27, 2P28, 2P29, 2P30, 2P35	Use a jumper to make one of the eight F_{sw} selections (2P27–2P30) for the secondary phase. Note that same Fsw must be selected for both the primary and the secondary phase.
ILIM/SS	ILIM/SS	1P22, 1P23, 1P24, 1P25, 1P6	Use a jumper to select one of the two soft-start time options and one of four OCP limits (1P22–1P25) for the primary phase. 1P6 is used to monitor ILIM/SS signal for test purpose.
		2P22, 2P23, 2P24, 2P25, 2P6	Use a jumper to select one of the two soft-start time options and one of four OCP limits (2P22–2P25) for the secondary phase. It is recommended to use the same setting on both the primary and the secondary phase.
Ext Sync Clock	EXT CLK	TP4	An external sync clock signal can be applied either through a SMD connector (TP4) or a two–pin header (1P4) for the primary and a two–pin (2P9) for the secondary.
	CLK_IN, GND	1P4, 2P9	

Label			Descriptions
Ext 3.3 V	Ext 3.3 V, GND	P4	An external 3.3 V PGOOD pull-up bias voltage can be applied through a two-pin header (P4). To use the external PGOOD pull-up bias voltage, remove 1R4 and populate 1R5 with a 10 kΩ resistor.
P_{GOOD}	PGOOD, GND	1P5, 2P5	Connect a scope probe to 1P5 to monitor power good signal of the primary phase, and 2P5 to monitor power good signal of the secondary phase.
VCC	PVIN, VIN, VCC	1P12, 2P12	The standard demo board is configured to use the internal LDO by connecting PVIN and VIN of 1P12 with a jumper the primary, PVIN and VIN of 2P12 for the secondary. To use the external VCC, connect VIN and VCC of 1P12, ExtVCC and VCC of 1P37 for the primary. VIN and VCC of 2P12, ExtVCC and VCC of 2P37 for the secondary. Apply the external VCC to Ext VCC header (P3).
	EXT VCC, VCC	1P37, 2P37	
	EXT VCC, GND	P3	
RAMP	RAMP	1P31, 1P32, 1P33, 1P34, 1P36	Use a jumper to make one of eight RAMP selections (1P31–1P36) for the primary. Ramp 5 is selected for the demo board configuration. 1P36 is used to monitor RAMP signal for test purpose.
		2P31, 2P32, 2P33, 2P34, 2P36	Use a jumper to make one of eight RAMP selections (2P31–2P36) for the secondary. Same ramp configuration should be used for both the primary and the secondary.
PHST	PHST	1P18, 1P19, 1P20, 1P21, 1P11	Use a jumper to set the phase shift for the primary. 1P11 is used to monitor RAMP signal for test purpose.
		2P18, 2P19, 2P20, 2P21, 2P11	Use a jumper to set the phase shift for the secondary. 1P11 is used to monitor RAMP signal for test purpose.
	VOUT, GND	1P26, 2P26	Mini-slammer sockets for transient load tests.
	SW	1TP1, 2TP1	SW node signal can be monitored by connecting the UMCC connector to an oscilloscope. 1TP1 is for the primary and 2TP1 is for the secondary.

2.3 Evaluation Board configuration

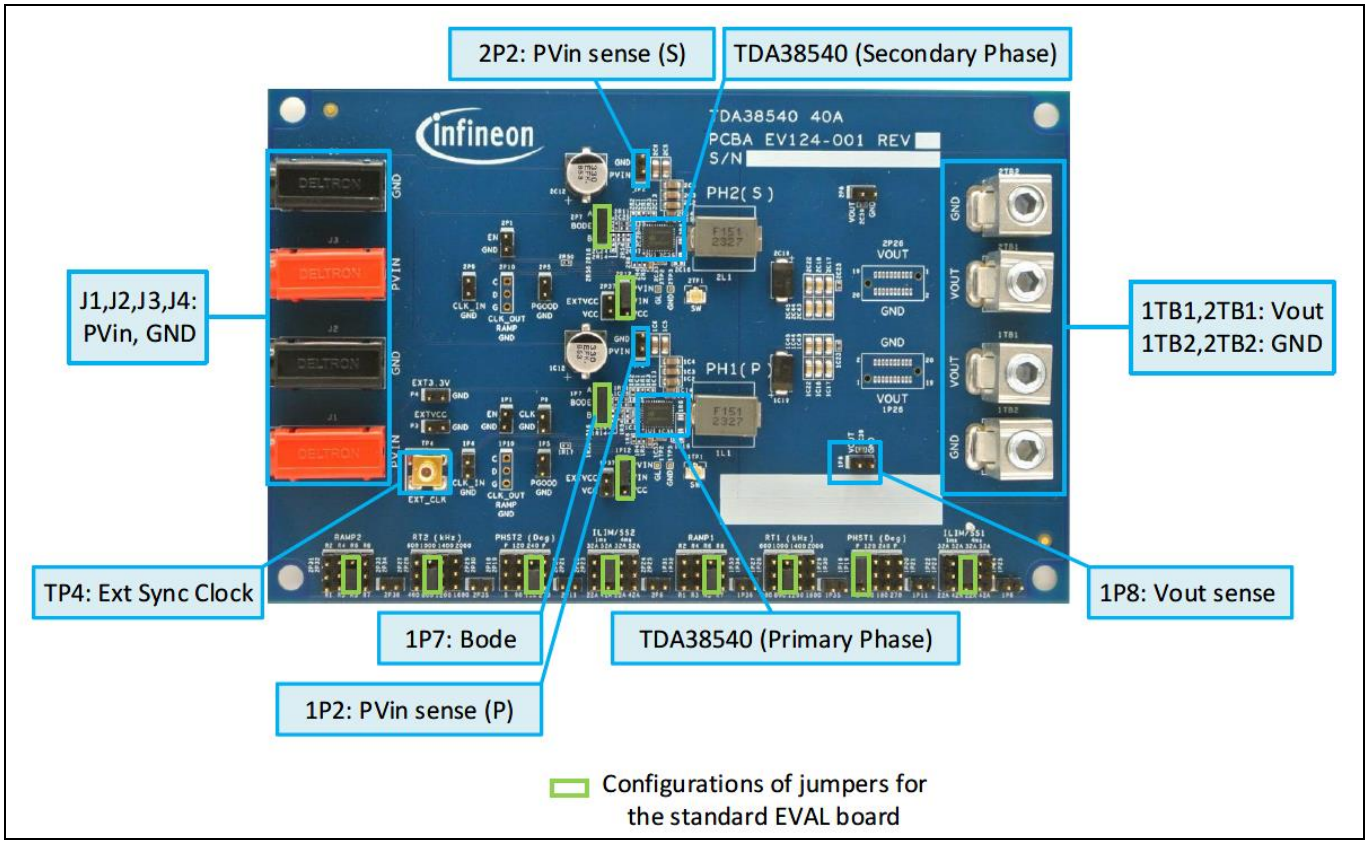


Figure 1 Illustration of dual–phase EVAL_TDA38540_1Vout_2P Evaluation Board.

2.4 Layout

The PCB is an eight-layer board (6.40-inch x 4.10 inch) using FR4 material. All layers use 2-ounce copper. The PCB thickness is 0.062 inch. The TDA38540 and other major power components are mounted on the topside of the board.

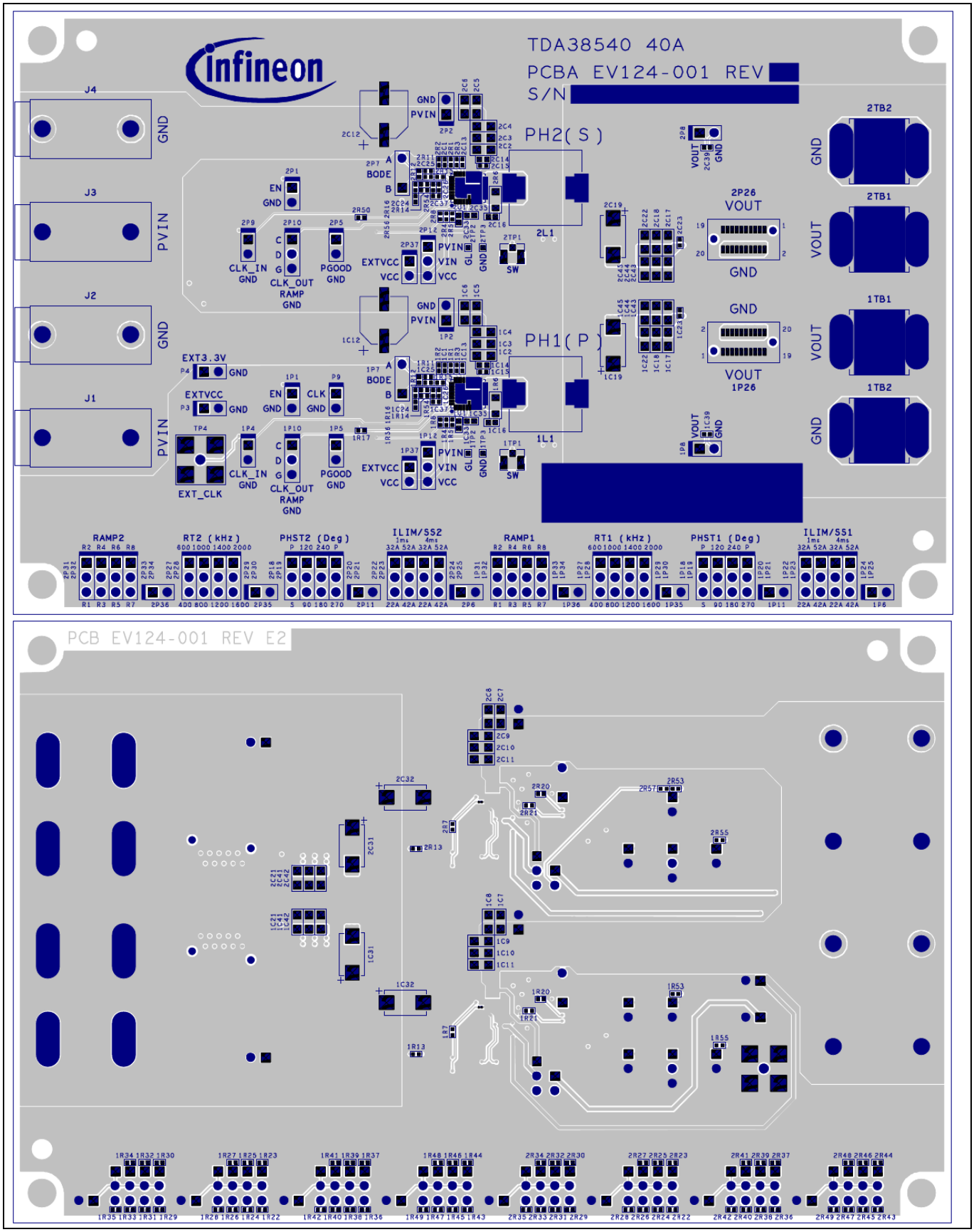


Figure 2 Top and bottom layer of TDA38540 Evaluation Board

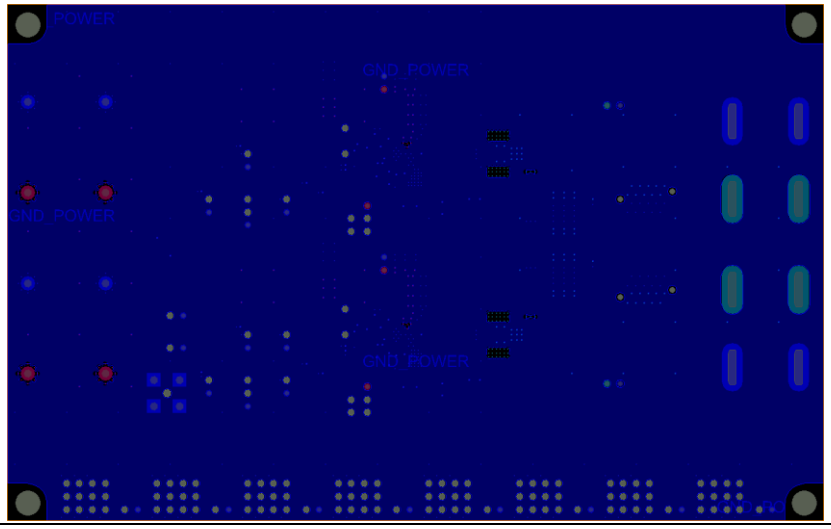


Figure 3 Mid layer 1

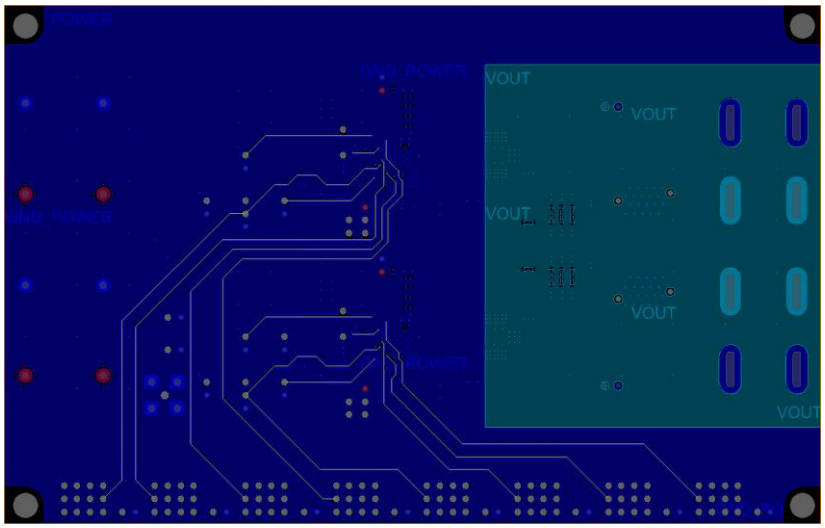


Figure 4 Mid layer 2

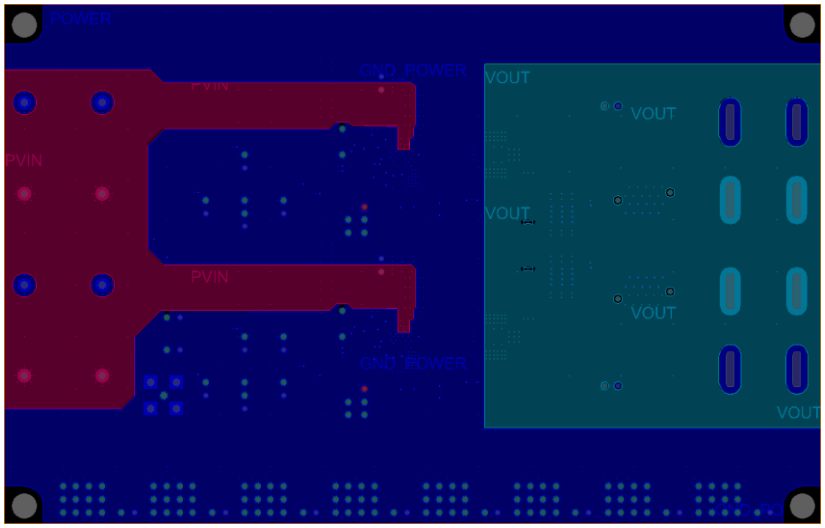


Figure 5 Mid layer 3

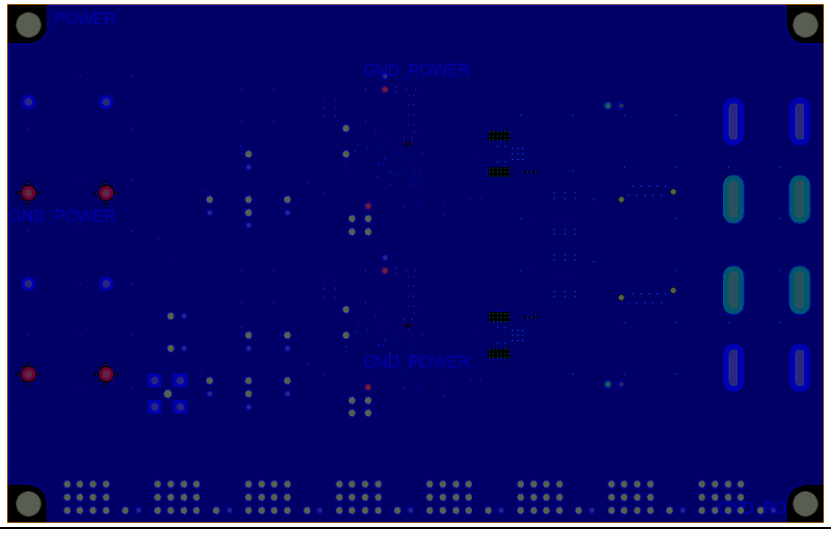


Figure 6 Mid layer 4

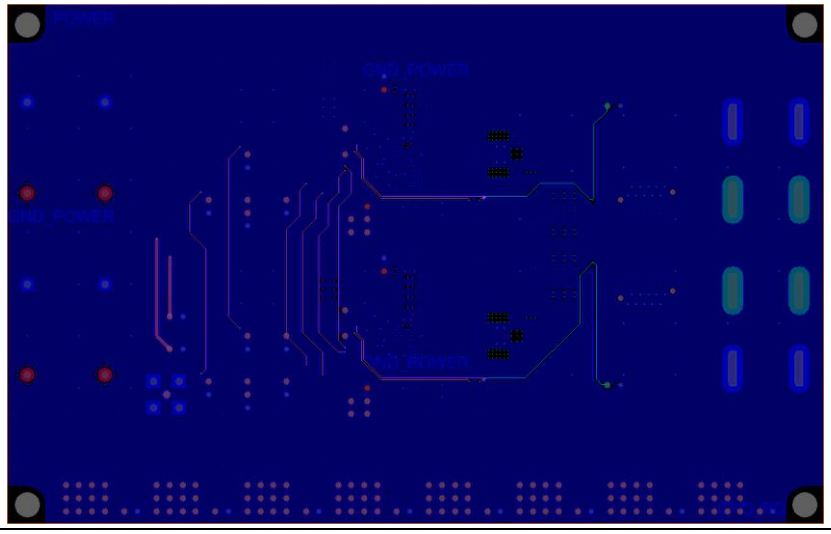


Figure 7 Mid layer 5

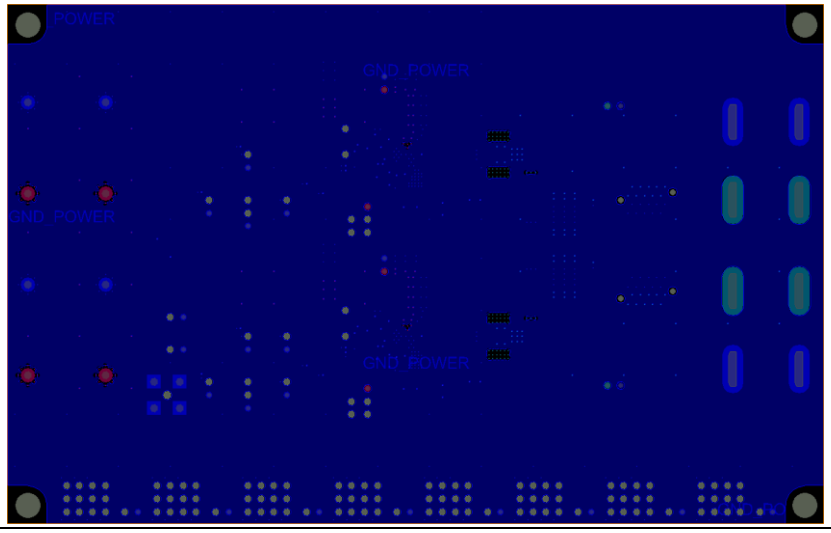
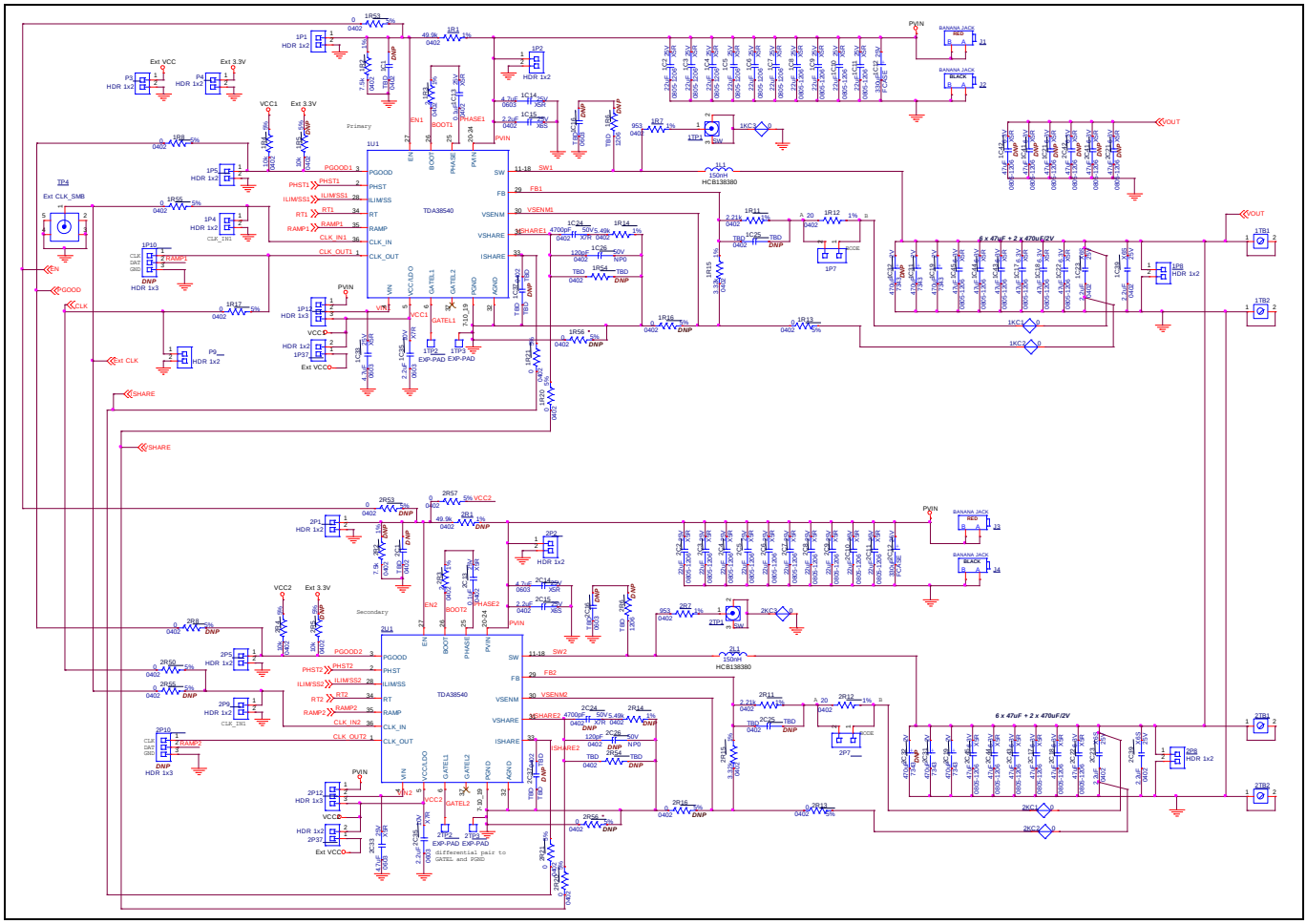


Figure 8 Mid layer 6

2.5 Schematics



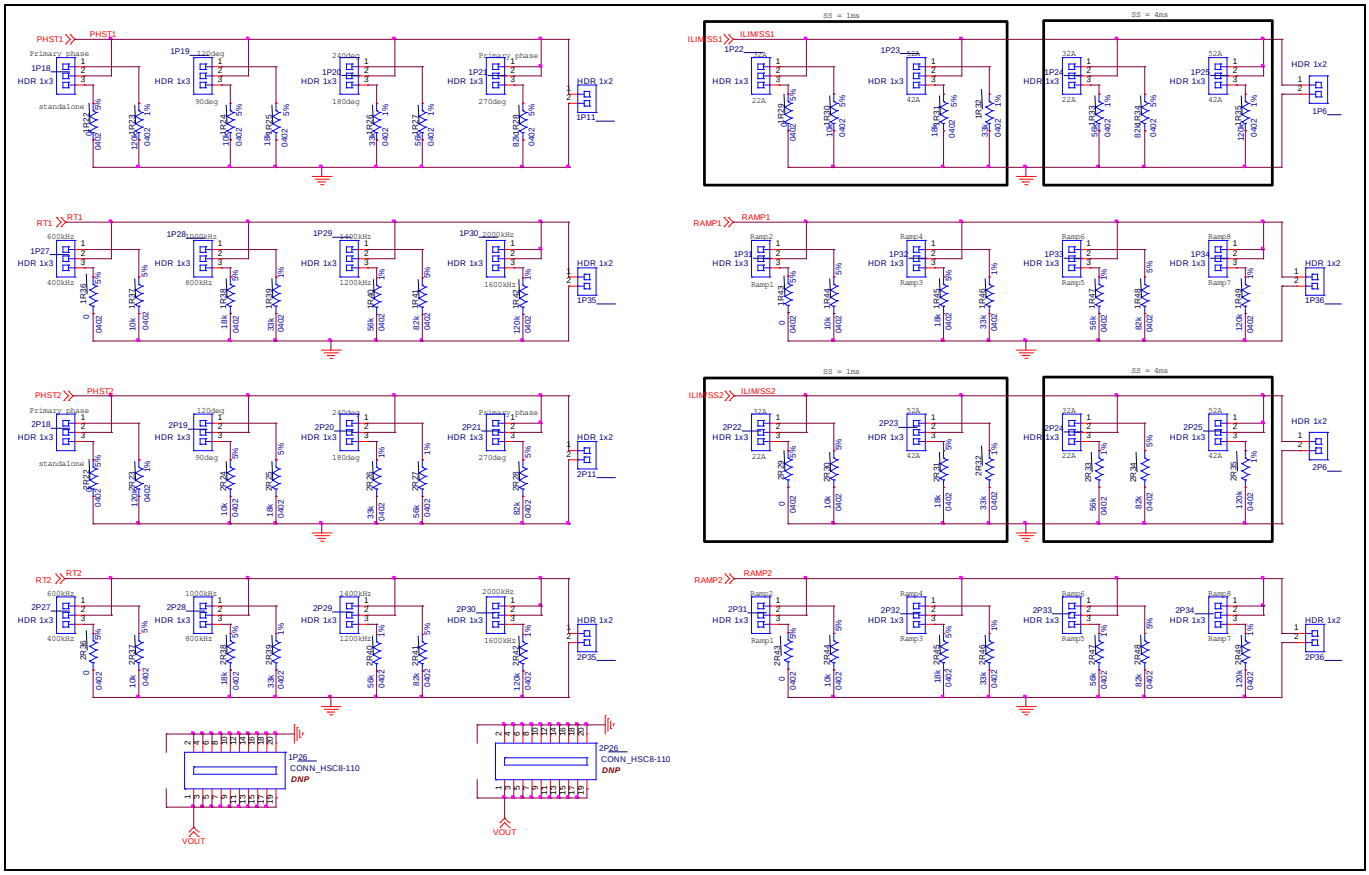


Figure 9 **Schematic of the EVAL_TDA38540_1Vout_2 phase board V_{in} = 12 V, V_{out} = 1.0 V, I_{outmax} = 80 A (TDC)**

2.6 Bill of materials

Table 3 Bill of materials

Qty	Reference	Value	Manufacturer	Part number	Description
2	1C12, 2C12	330 µF	Panasonic	PCE4439CT-ND	Aluminum capacitor, 330 µF, 20%, 25 V, SMD
2	1C13, 2C13	0.1 µF	Taiyo Yuden	TMK105BJ104KV-F	Ceramic capacitor, 0.1 µF, 25 V, 10%, X5R, 0402
4	1C14, 1C33, 2C14, 2C33	4.7 µF	Murata	GRM188R61E475KE11D	Ceramic capacitor, 4.7 µF, 25 V, 10%, X5R, 0603
6	1C15, 1C23, 1C39, 2C15, 2C23, 2C39	2.2 µF	Murata	GRM155C81E225KE11D	Ceramic capacitor, 2.2 µF 16 V 10% X6S 0402
12	1C17, 1C18, 1C22, 1C43, 1C44, 1C45, 2C17, 2C18, 2C22, 2C43, 2C44, 2C45	47 µF	Murata	GRM21BR60J476ME11#	Ceramic capacitor, 47 µF 6.3 V 20% X5R 0805
4	1C19, 1C31, 2C19, 2C31	470 µF	Panasonic	EEF-SX0D471XE	Aluminum capacitor, 470 µF, 20%, 2 V, 6 mΩ
20	1C2, 1C3, 1C4, 1C5, 1C6, 1C7, 1C8, 1C9, 2C2, 2C3, 2C4, 2C5, 2C6, 2C7, 2C8, 2C9, 1C10, 1C11, 2C10, 2C11	22 µF	Murata	GRM21BR61E226ME44L	Ceramic capacitor, 22 µF, 25 V, 20%, X5R, 0805
1	1C24	4700 pF	Murata	GRM155R71H472KA01J	Ceramic capacitor, 4700 pF 50 V 10% X7R 0402
1	1C26	120 pF	KEMET	C0402C121J5GAC7867	Ceramic capacitor, 120 pF 50 V 5% NP0 0402
2	1C35, 2C35	2.2 µF	Murata	GRM188R71A225KE15D	Ceramic capacitor, 2.2 µF 10 V 10% X7R 0603
2	1L1, 2L1	150 nH	Delta	HCB138380D-151	INDUCTOR 150 nH, Isat = 80 A DCR=0.15 mΩ, 12.4x8.3x8.0 mm, SMD
1	1R1	49.9 kΩ	Panasonic	ERJ-2RK4992X	Resistor, 49.9 kΩ, 1/10 W, 1% 0402, SMD
2	1R11, 2R11	2.21 kΩ	Panasonic	ERJ-2RKF2211X	Resistor, 2.21 kΩ, 1/10 W, 1% 0402, SMD

Qty	Reference	Value	Manufacturer	Part number	Description
2	1R12, 2R12	20 Ω	Vishay	CRCW040220R0FKED	Resistor, 20.0 Ω, 1/16 W 1%, 0402, SMD
1	1R14	5.49 kΩ	Panasonic	ERJ-2RKF5491X	Resistor, 5.49 kΩ, 1/10 W 1%, 0402, SMD
2	1R15, 2R15	3.32 kΩ	Panasonic	ERJ-2RK3321X	Resistor, 3.32 kΩ, 1/10 W 1%, 0402, SMD
1	1R2	7.5 kΩ	Panasonic	ERJ-2RKF7501X	Resistor, 7.50 kΩ, 1/10 W 1%, 0402, SMD
8	1R23, 1R35, 1R42, 1R49, 2R23, 2R35, 2R42, 2R49	120 kΩ	Panasonic	ERJ-U02F1203X	Resistor, 120 kΩ, 1/10 W 1% 0402 SMD
8	1R25, 1R31, 1R38, 1R45, 2R25, 2R31, 2R38, 2R45	18 kΩ	Panasonic	ERJ-U02J183X	Resistor, 18 kΩ, 1/10 W 5% 0402 SMD
8	1R26, 1R32, 1R39, 1R46, 2R26, 2R32, 2R39, 2R46	33 kΩ	Panasonic	ERJ-2RKF3302X	Resistor, 33 kΩ, 1/10 W 5% 0402 SMD
8	1R27, 1R33, 1R40, 1R47, 2R27, 2R33, 2R40, 2R47	56 kΩ	Panasonic	ERJ-2RKF5602X	Resistor, 56 kΩ, 1/10 W 1% 0402 SMD
8	1R28, 1R34, 1R41, 1R48, 2R28, 2R34, 2R41, 2R48	82 kΩ	Panasonic	ERJ-2GEJ823X	Resistor, 82 kΩ, 1/10 W 5% 0402 SMD
21	1R8, 2R8, 1R13, 1R17, 1R20, 1R21, 1R22, 1R29, 1R36, 1R43, 1R53, 1R55, 2R13, 2R20, 2R21, 2R22, 2R29, 2R36, 2R43, 2R50, 2R57	0 Ω	Panasonic	ERJ-2GE0R00X	Resistor, 0 Ω, 1/10 W 0402 SMD
2	1R3, 2R3	2 Ω	Panasonic	ERJ-U02F2R00X	Resistor, 2.0 Ω, 1/10W, 1%, 0402, SMD
10	1R4, 2R4, 1R24, 1R30, 1R37, 1R44, 2R24, 2R30, 2R37, 2R44	10 kΩ	Panasonic	ERJ-2GEJ103X	Resistor, 10 kΩ, 1/16 W, 5% 0402 SMD

Qty	Reference	Value	Manufacturer	Part number	Description
2	1R7, 2R7	953 Ω	Panasonic	ERJ-2RKF9530X	Resistor, 953 Ω, 1/10 W, 1% 0402 SMD
2	1U1, 2U1	TDA38540	Infineon	TDA38540AUMA1	IPOL 40 A single-voltage stackable synchronous Buck regulator

3 Typical operating waveforms

- V_{in} = 12.0 V
- V_{out} = 1.0 V
- I_{out} = 0-80 A

Operating conditions: room temperature with no airflow.

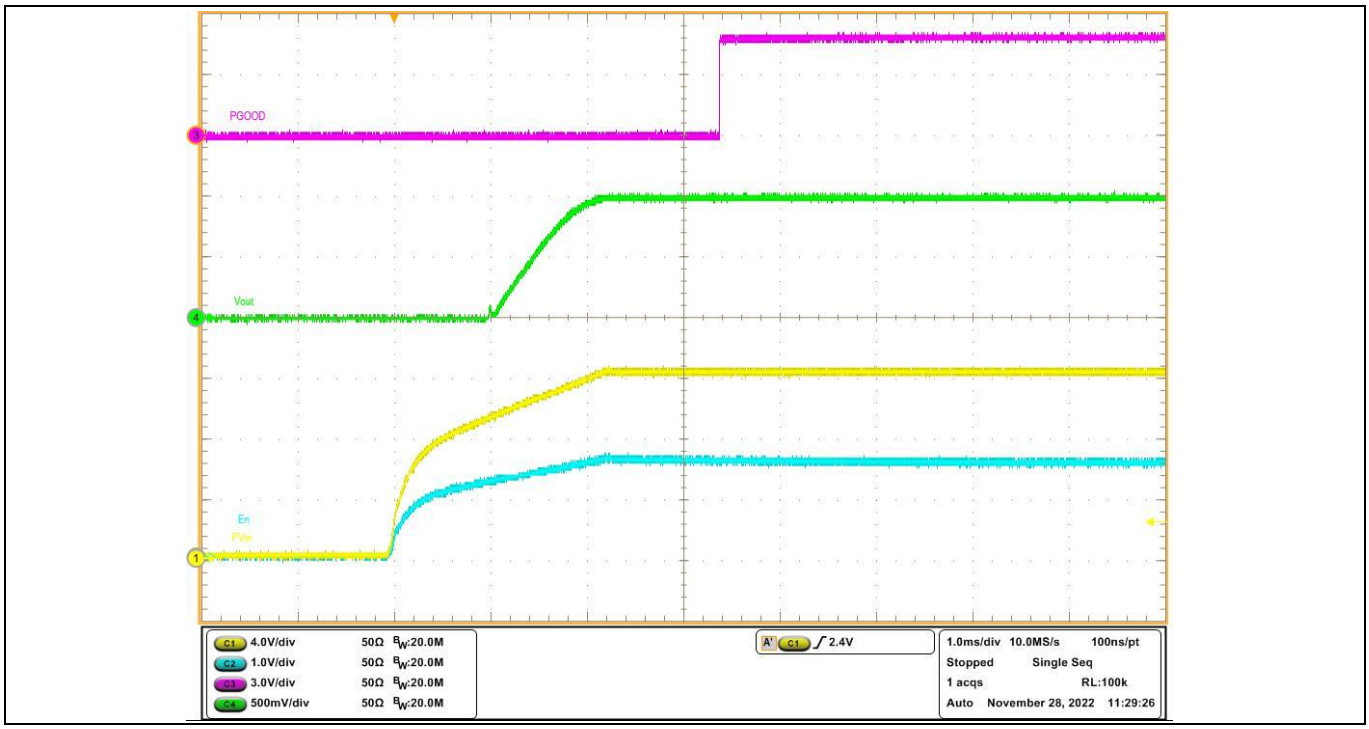


Figure 10 Startup at 0 A load (Ch_1: PV_{in}, Ch_2: Enable, Ch_3: PGOOD, Ch_4: V_{out})

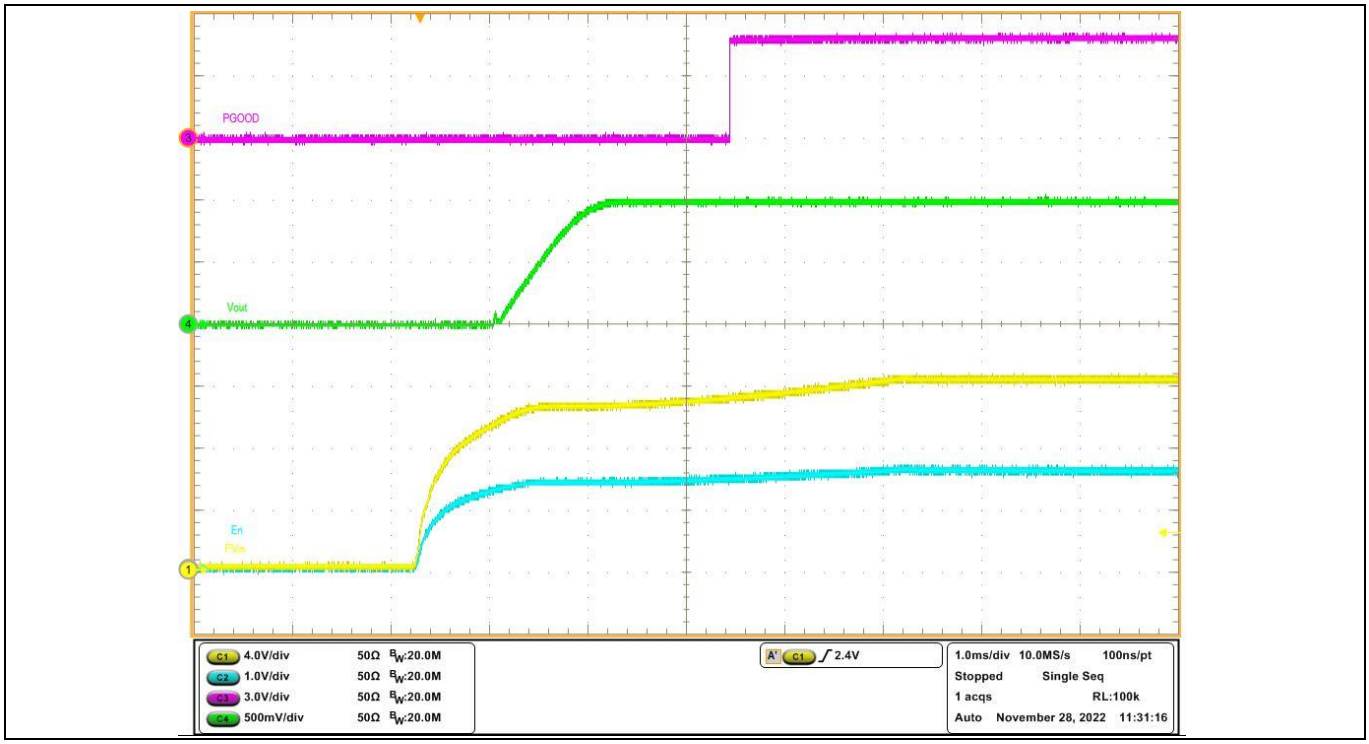


Figure 11 Startup at 80 A load (Ch_1: PV_{in}, Ch_2: Enable, Ch_3: PGOOD, Ch_4: V_{out})

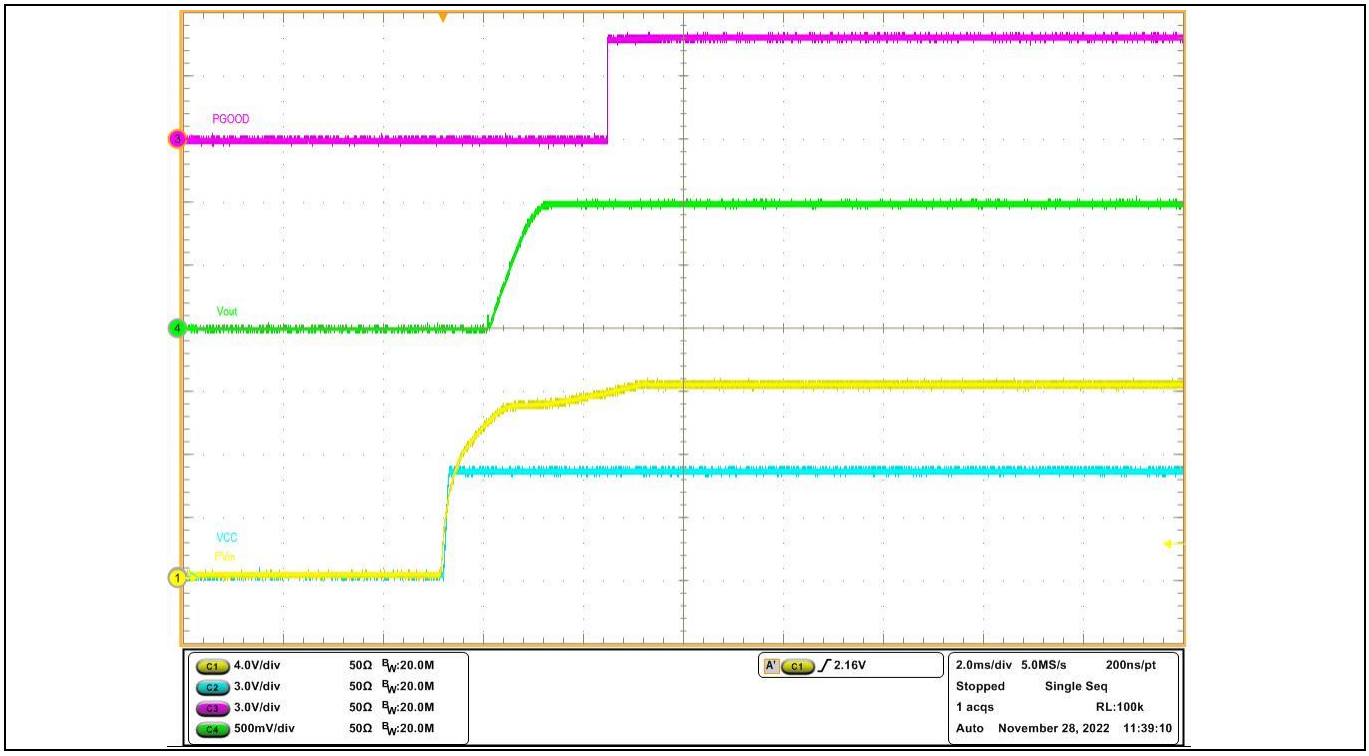


Figure 12 Startup at 80 A load (Ch_1: PV_{in}, Ch_2: VCC, Ch_3: PGOOD, Ch_4: V_{out})

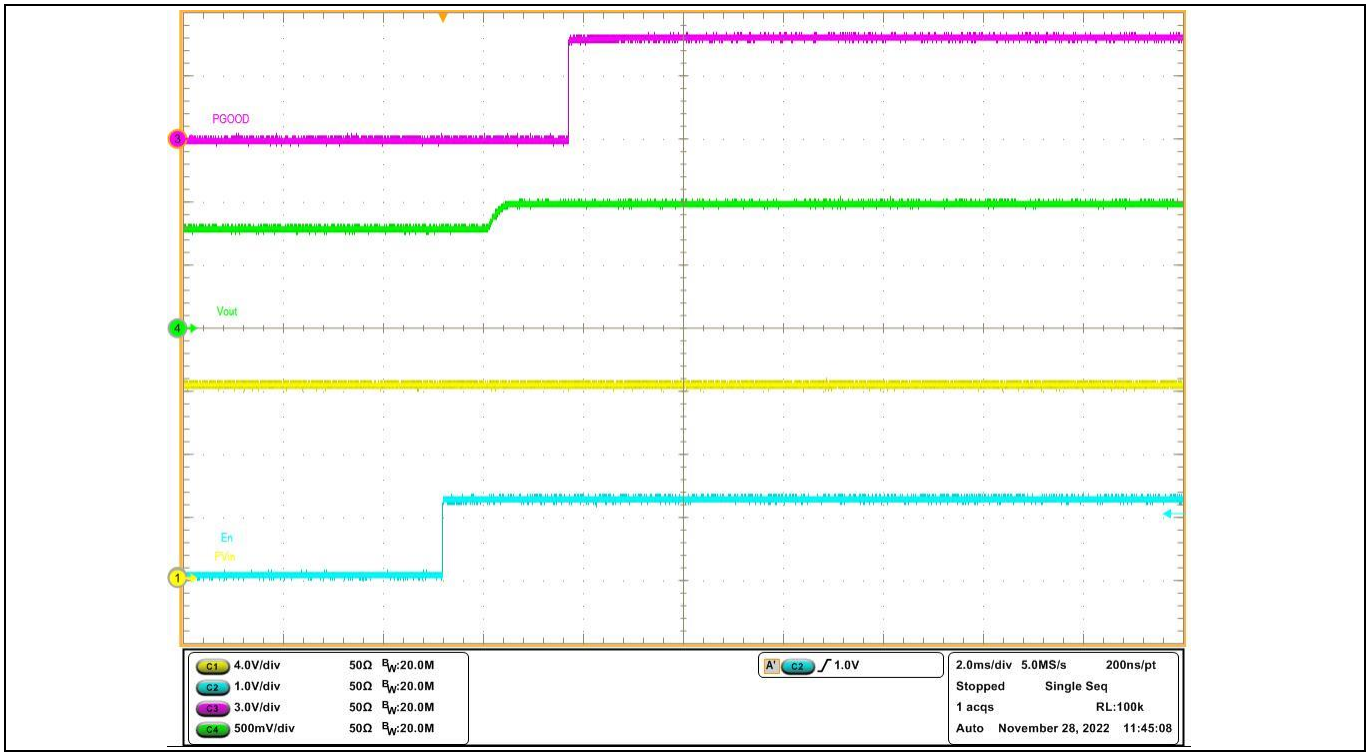


Figure 13 Pre-bias startup at 0 A load (Ch_1: PV_{in}, Ch_2: Enable, Ch_3: PGOOD, Ch_4: V_{out})

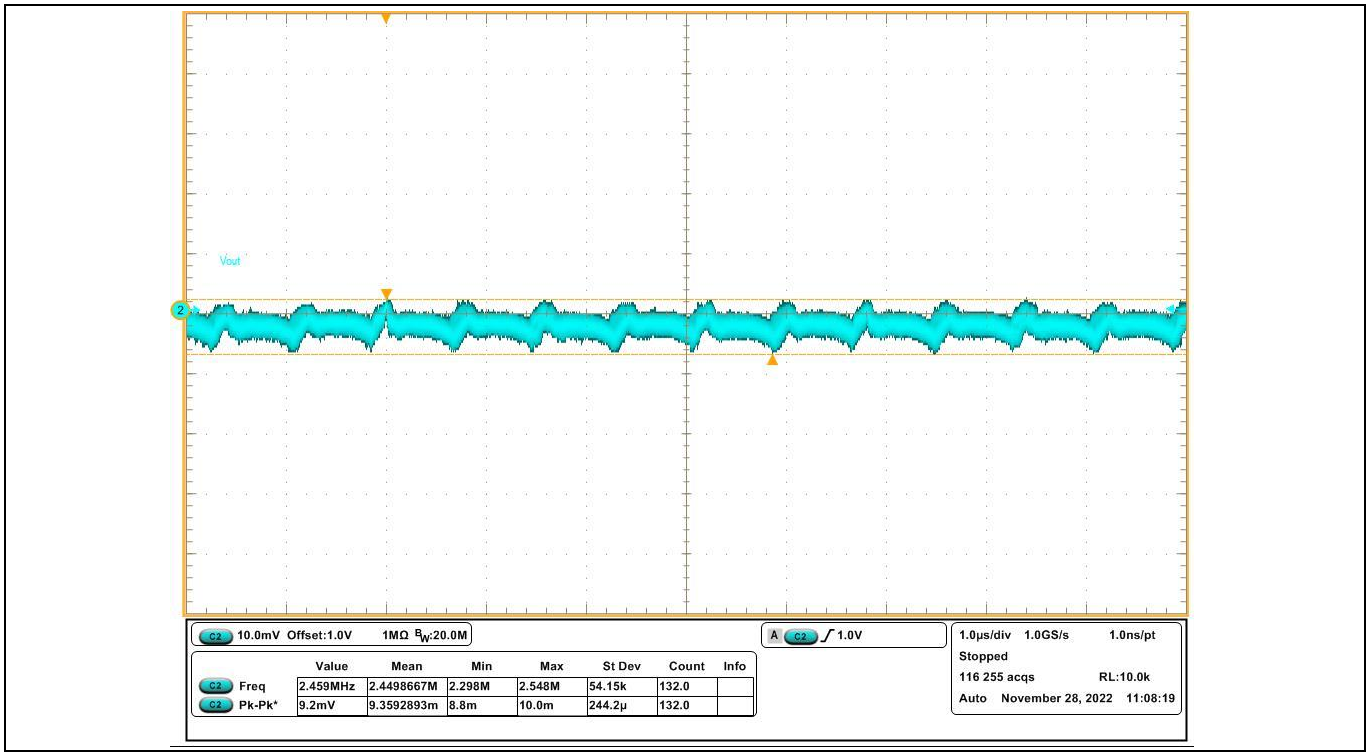


Figure 14 V_{out} ripple at 80 A load, F_{sw} = 600 kHz (Ch_2: V_{out}), peak to peak V_{out} ripple = 9.2 mV

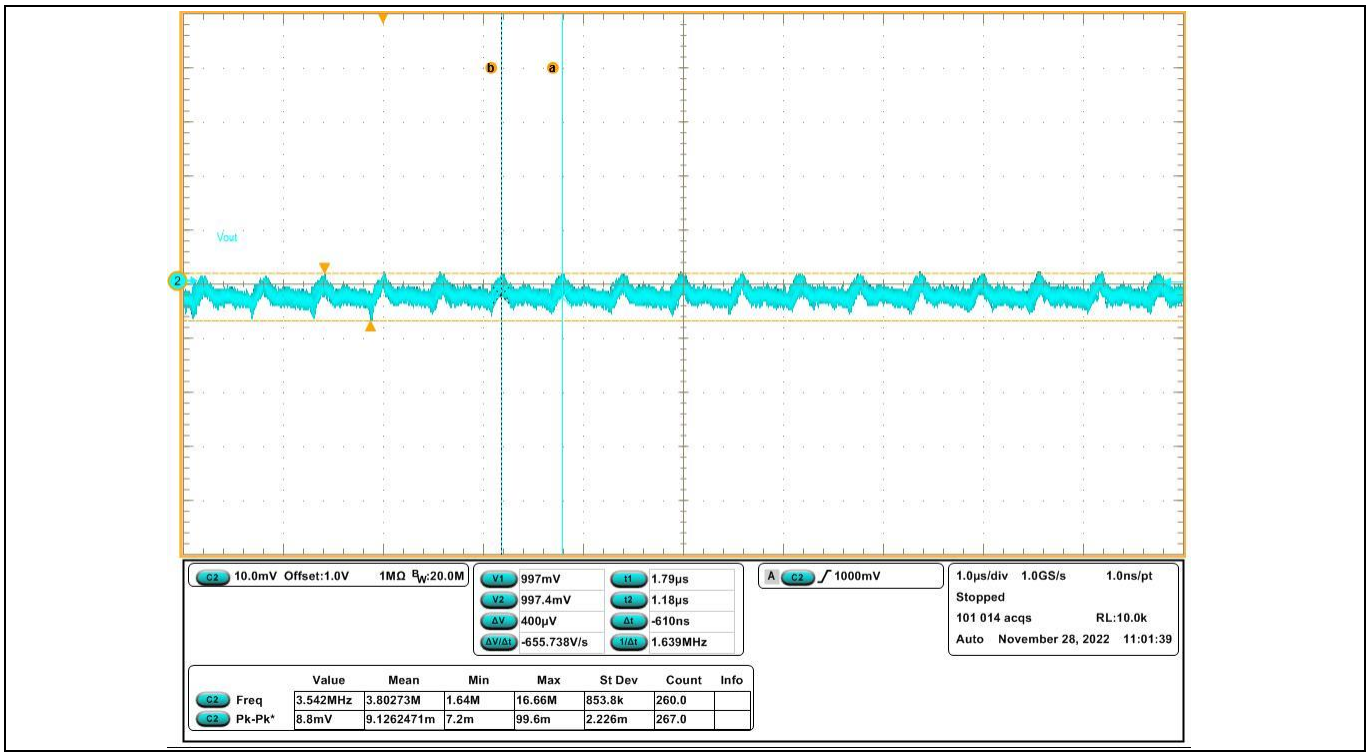


Figure 15 V_{out} ripple at 80 A load, f_{sw} = 800 kHz (Ch_2: V_{out}), peak to peak V_{out} ripple = 8.8 mV

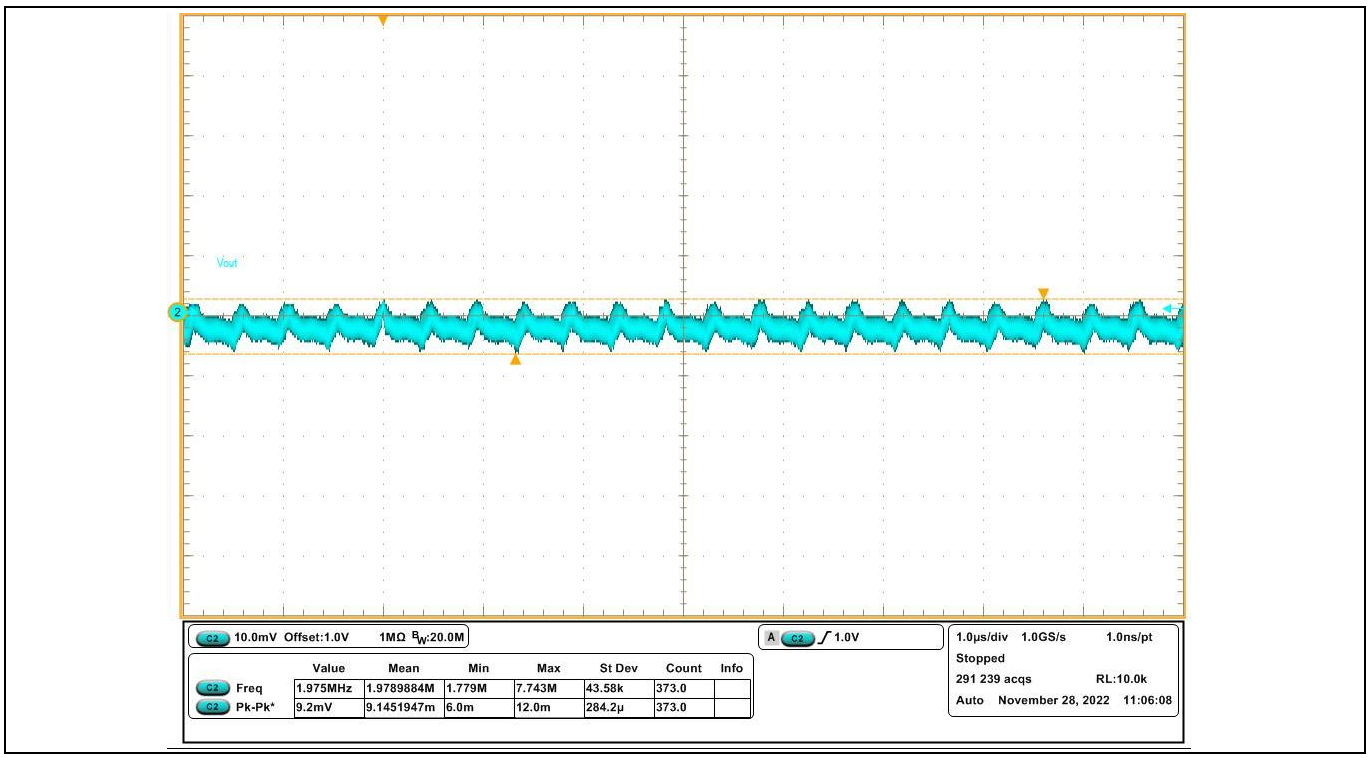


Figure 16 V_{out} ripple at 80 A load, f_{sw} = 1000 kHz (Ch_2: I_{out}, Ch_4: V_{out}), peak to peak V_{out} ripple = 9.2 mV

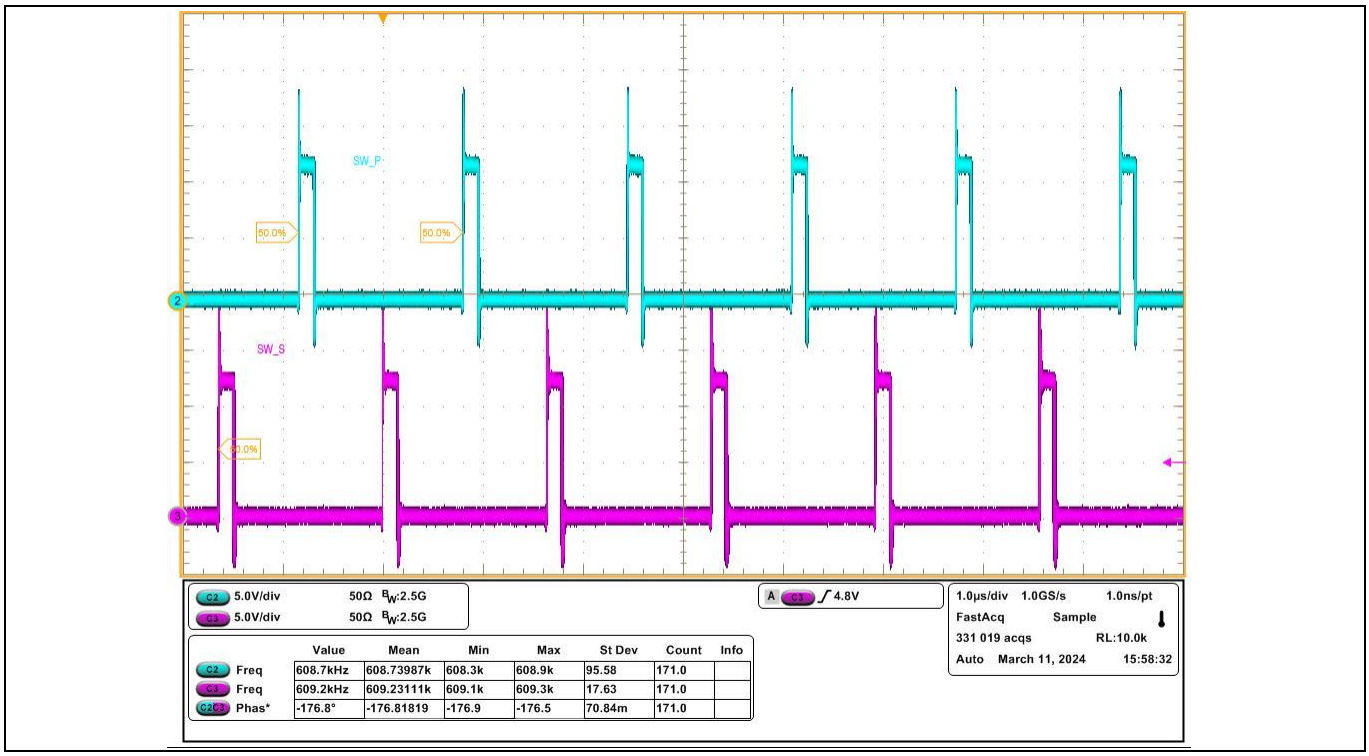


Figure 17 SW node, 80 A load, f_{sw} = 600 kHz

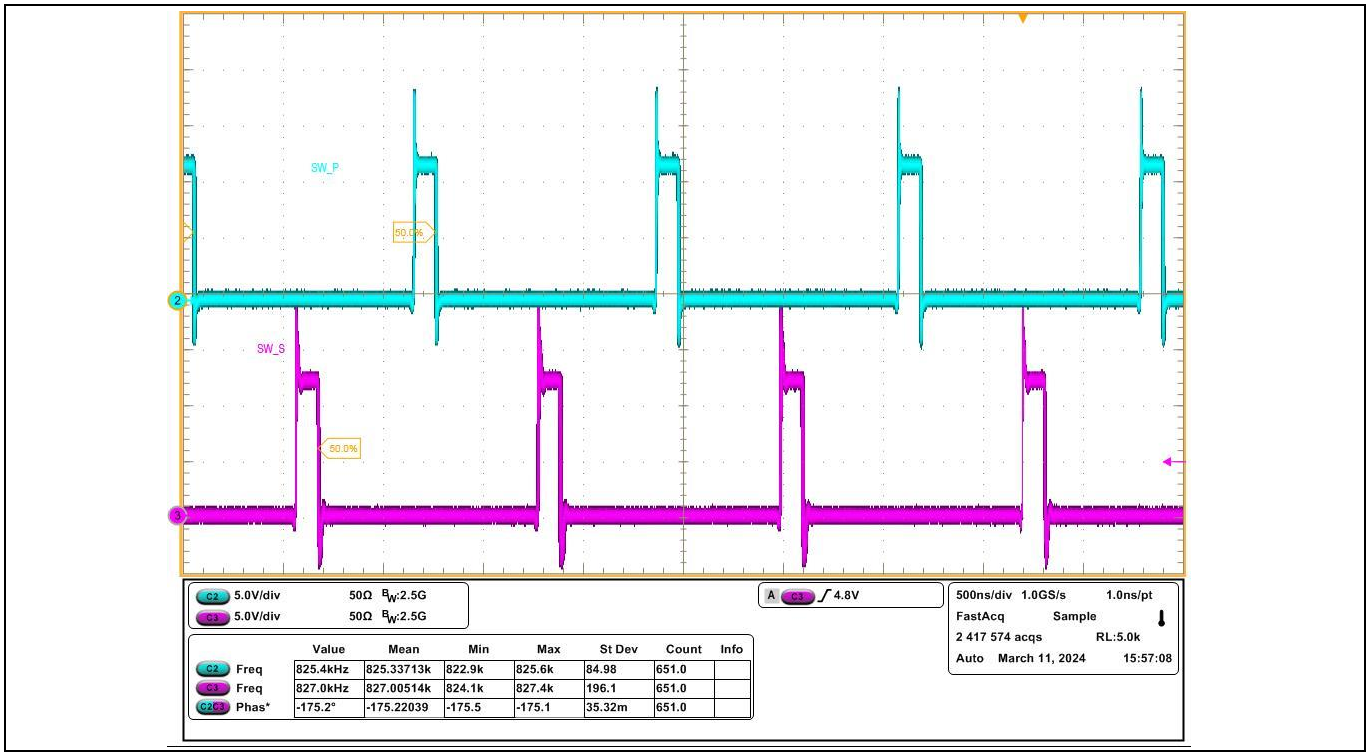


Figure 18 SW node, 80 A load, f_{sw} = 800 kHz

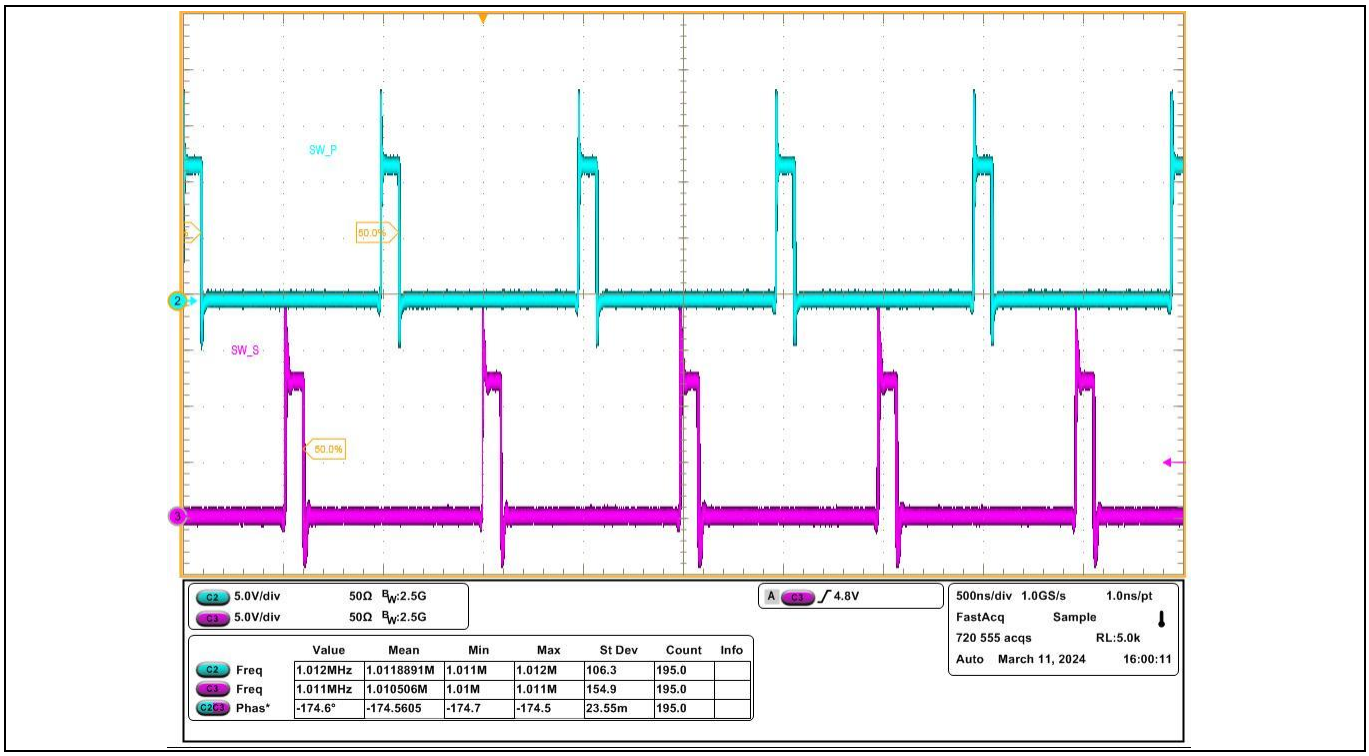


Figure 19 SW node, 80 A load, f_{sw} = 1000 kHz

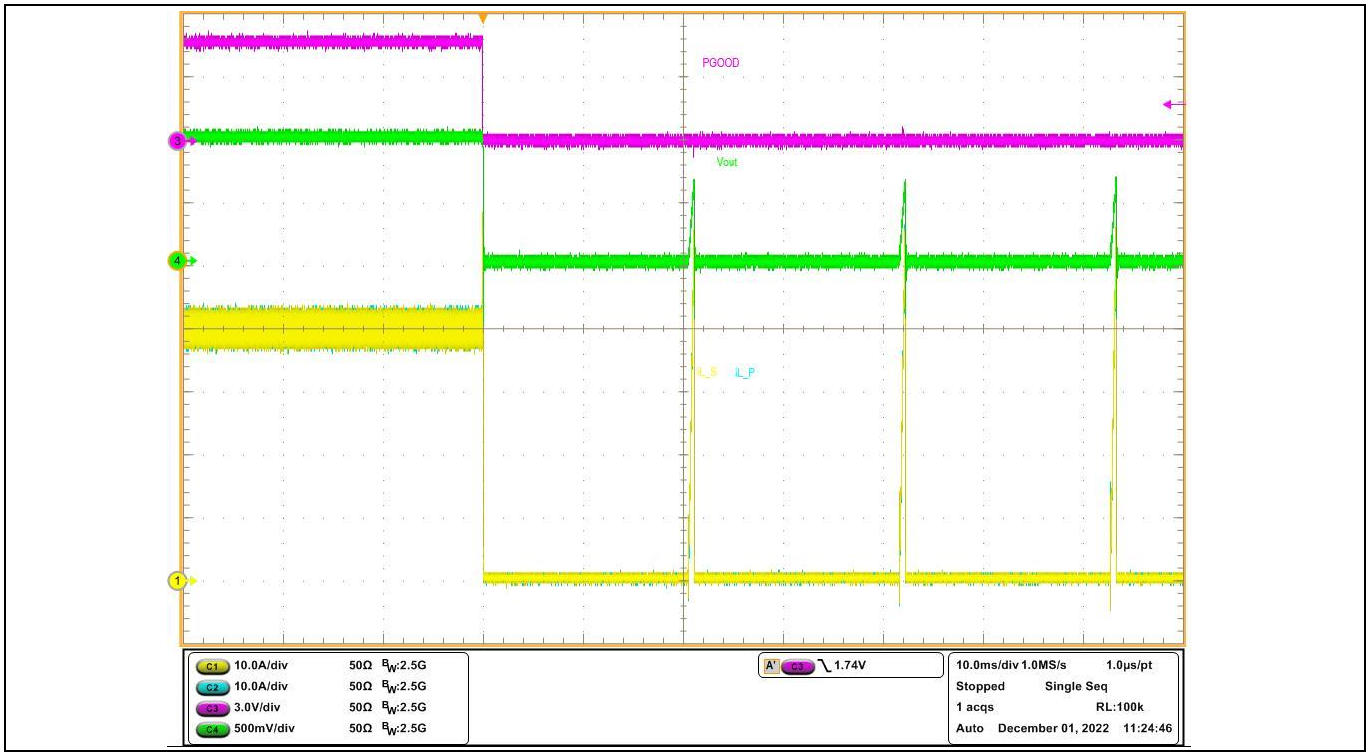


Figure 20 Short V_{out} when operating with 80 A load, (Ch_1: iL_s, Ch_2: iL_p, Ch_3: PGOOD, Ch_4: V_{out})

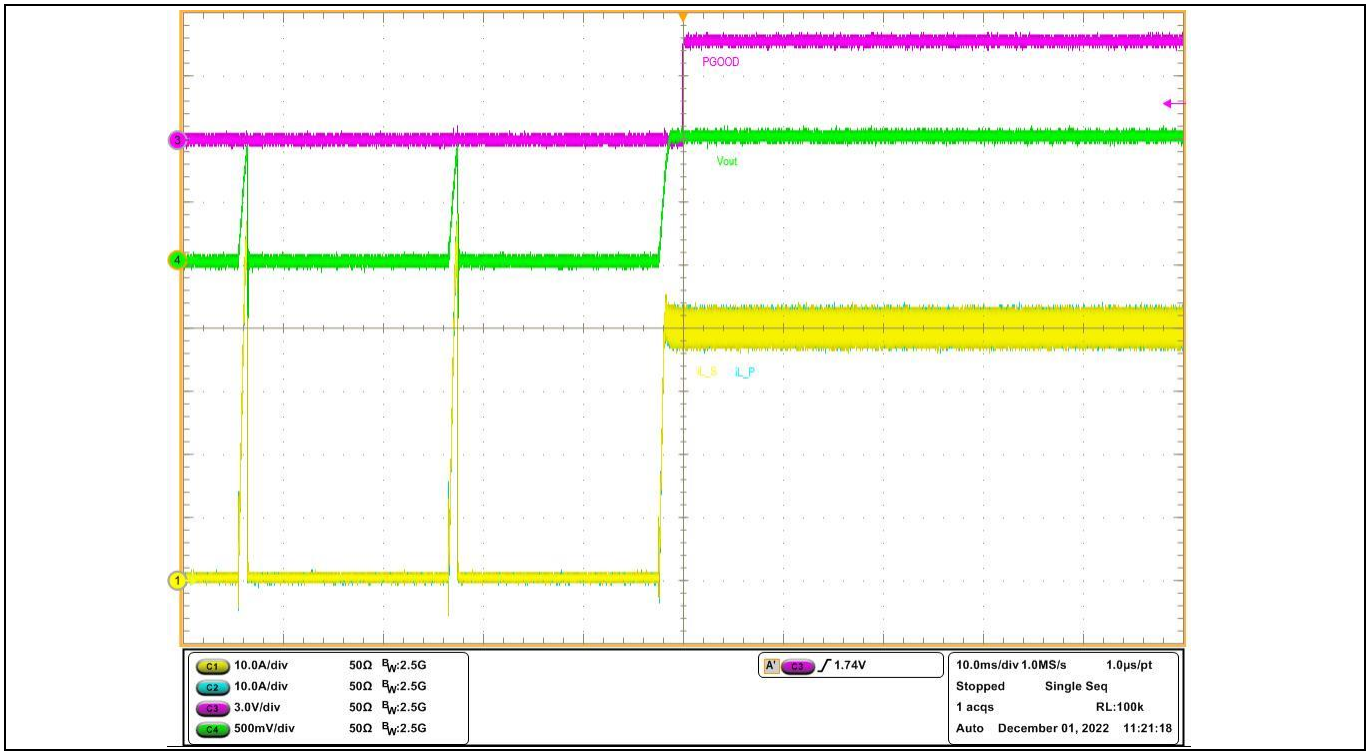


Figure 21 Recover from shorted V_{out} to 80 A load current (Ch_1: iL_s, Ch_2: iL_p, Ch_3: PGOOD, Ch_4: V_{out})

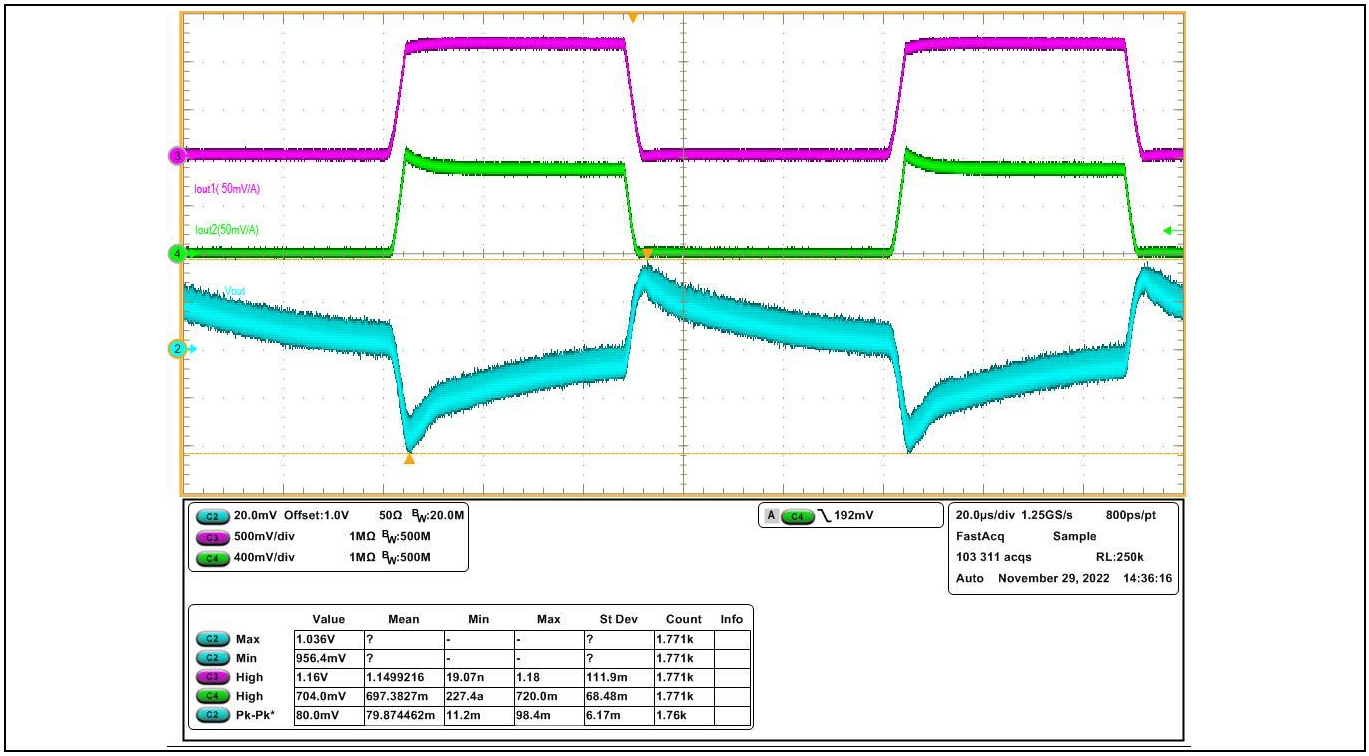


Figure 22 **Transient response at 40 A step-load current at 10 A/µs slew rate: I_{out} = 0 A to 40 A (Ch_2: V_{out}, Ch_3: I_{out1}, Ch_4: I_{out2}) pk-pk: 80 mV, f_{sw} = 600 kHz**

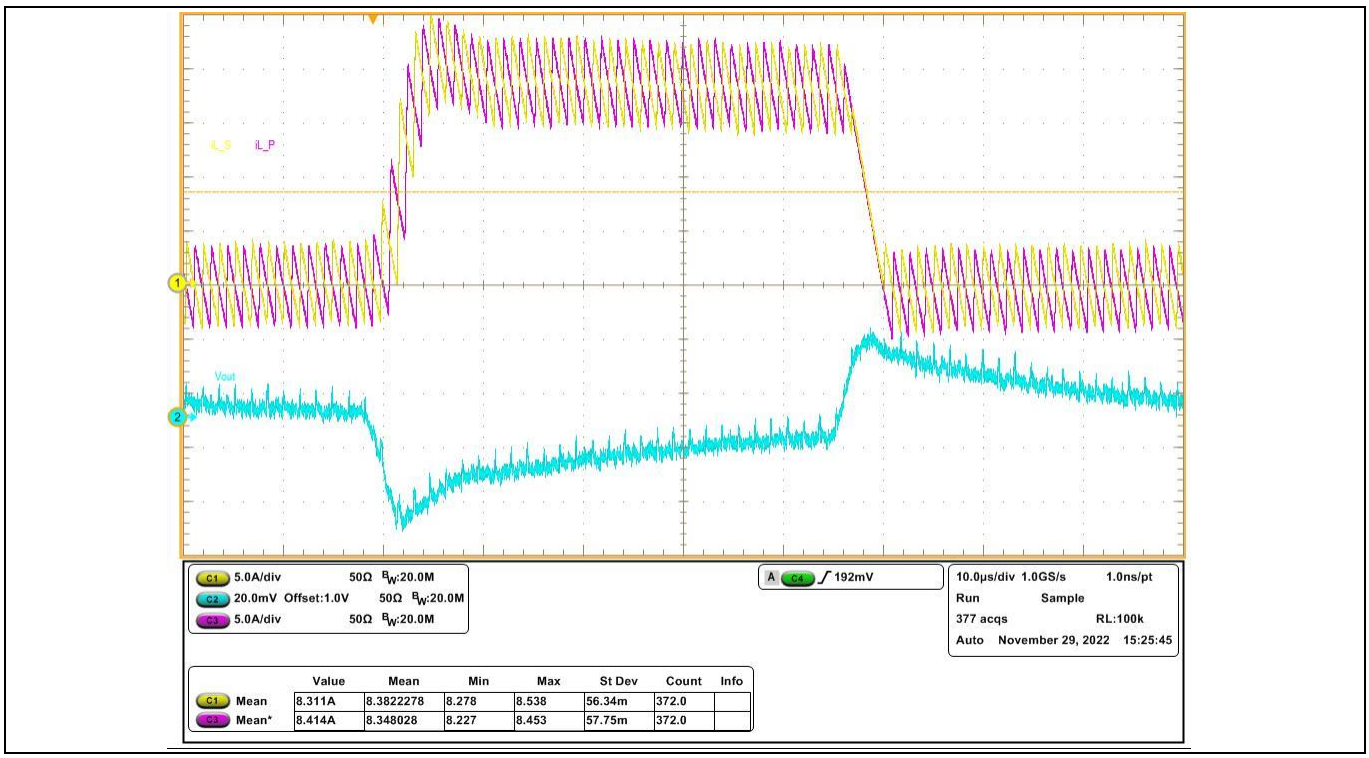


Figure 23 **Transient response at 40 A step-load current at 10 A/µs slew rate: I_{out} = 0 A to 40 A (Ch_1: iL_s, Ch_3: iL_p, Ch_2: V_{out}), f_{sw} = 600 kHz**

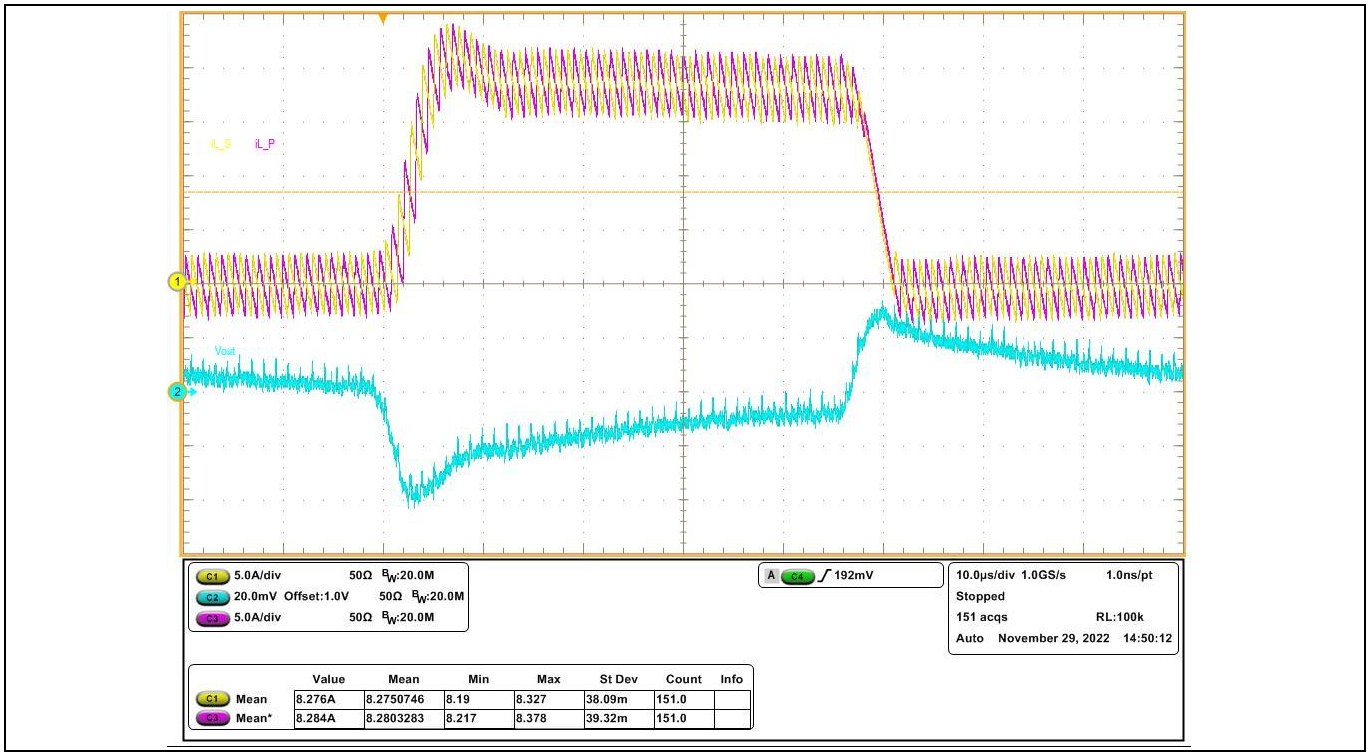


Figure 24 **Transient response at 40 A step-load current at 10 A/µs slew rate: I_{out} = 0 A to 40 A (Ch_1: iL_s, Ch_3: iL_p, Ch_2: V_{out}), f_{sw} = 800 kHz**

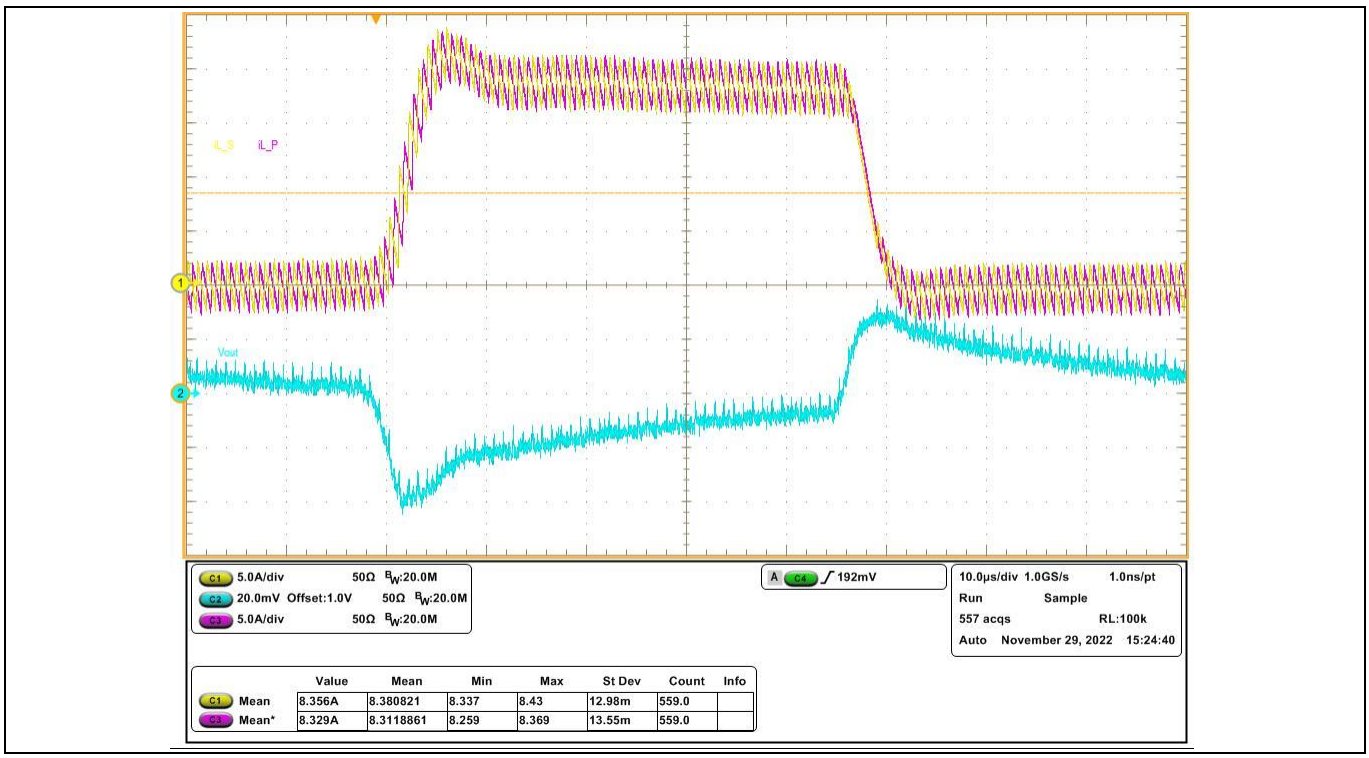


Figure 25 **Transient response at 40 A step-load current at 10 A/µs slew rate: I_{out} = 0 A to 40 A (Ch_1: iL_s, Ch_3: iL_p, Ch_2: V_{out}), f_{sw} = 1000 kHz**

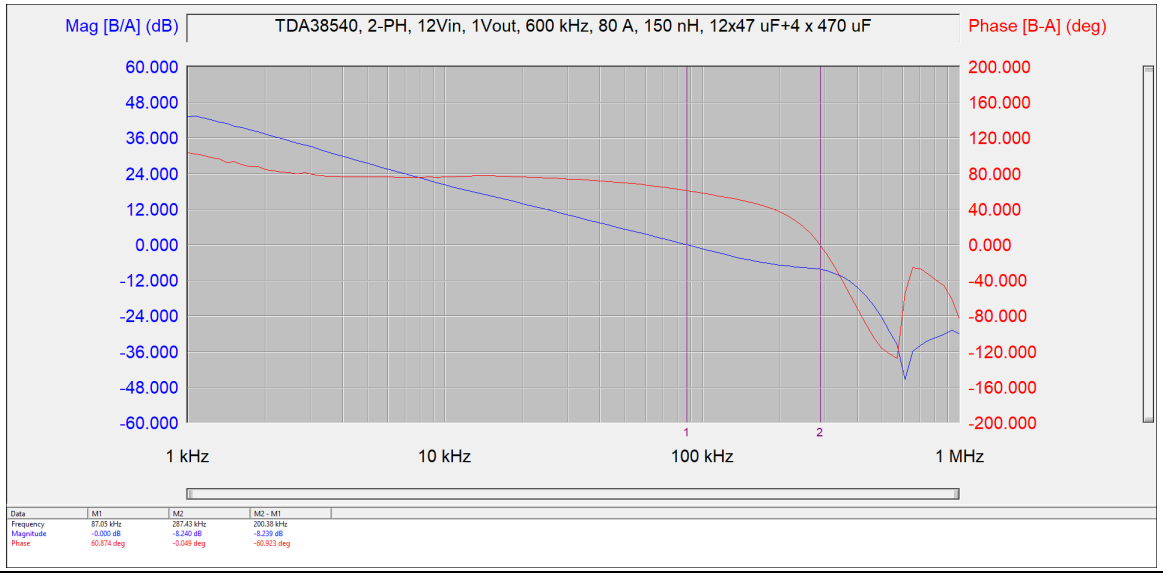


Figure 26 Bode plot at I_{out} = 80 A. BW = 87 kHz, PM = 61°C, GM = -8.2 dB, F_{sw} = 600 kHz, Ramp 5 = 100 m

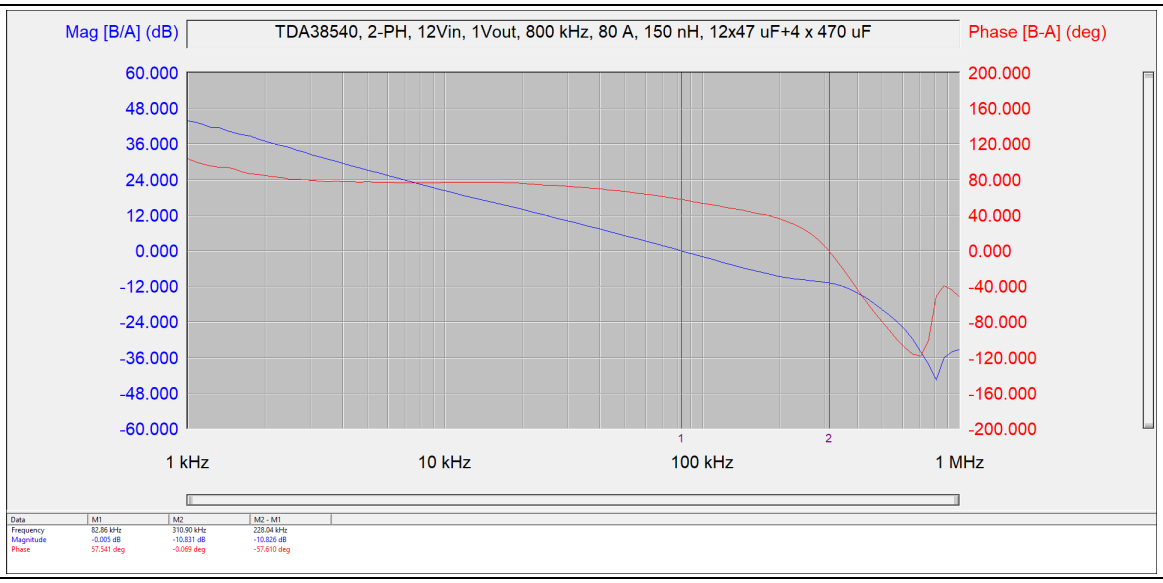


Figure 27 Bode plot at I_{out} = 80 A. BW = 83 kHz, PM = 57°C, GM = -10.8 dB, F_{sw} = 800 kHz, Ramp 5 = 100 m

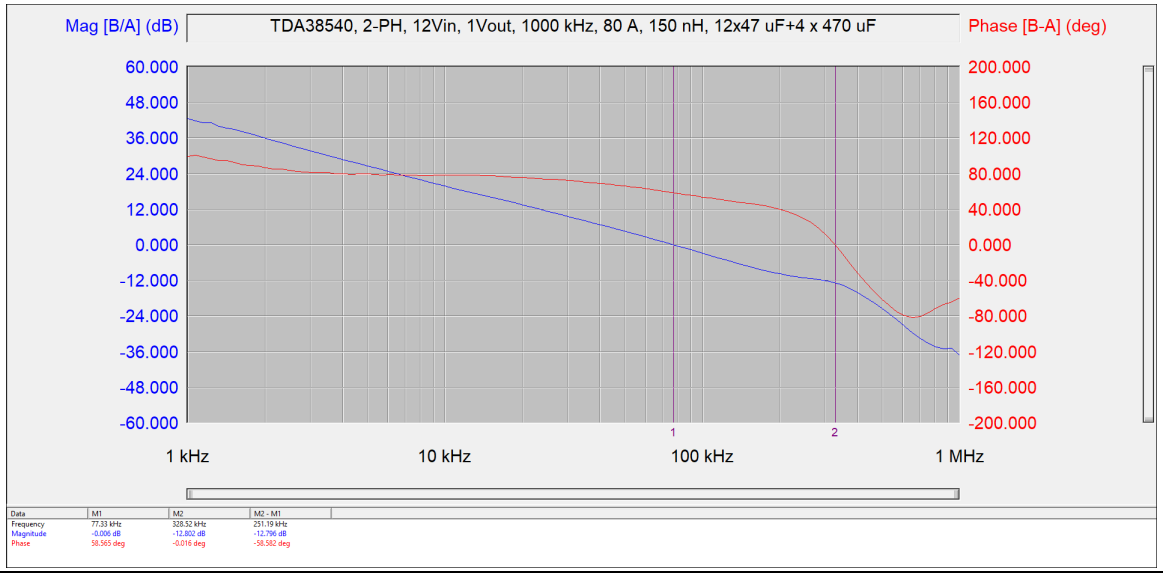


Figure 28 Bode plot at I_{out} = 80 A BW = 77 kHz, PM = 58°, GM = -12.8 dB, F_{sw} = 1000 kHz.

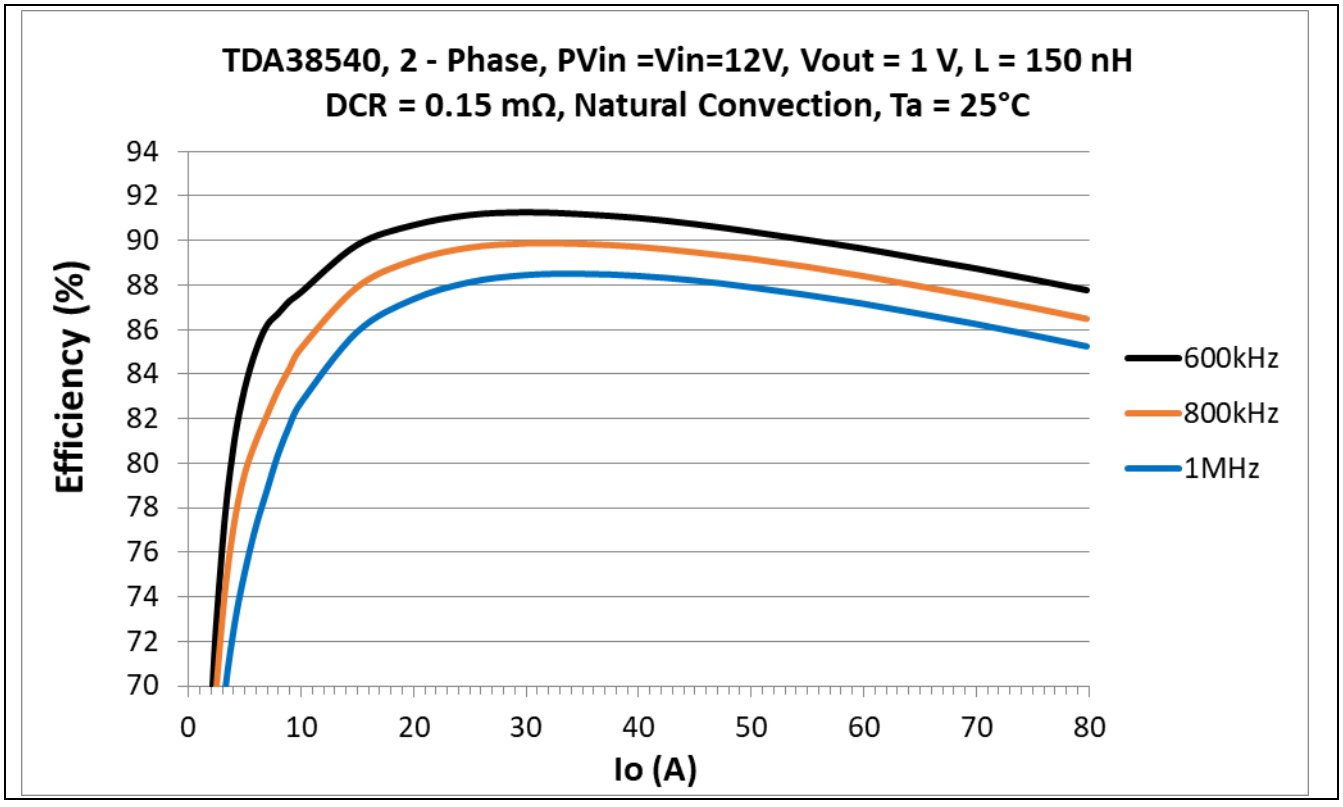


Figure 29 Efficiency vs. load current natural convection (12 V_{in}, 1 V_{out}, 150 nH, 600 kHz/800 kHz/1000 kHz, T_a = 25°C)

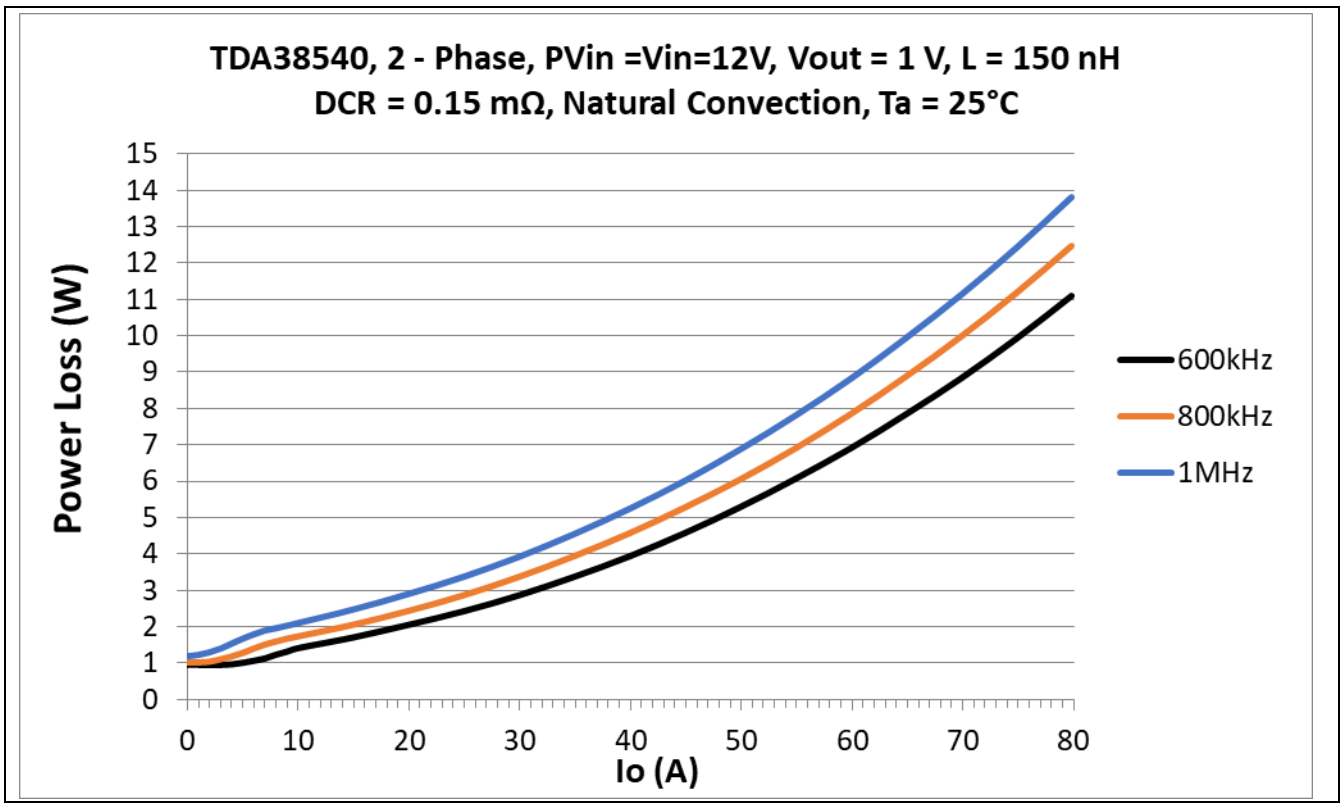


Figure 30 **Power loss vs. load current natural convection (12 V_{in}, 1.0 V_{out}, 150 nH, 600 kHz/800 kHz/1000 kHz, T_a = 25°C)**

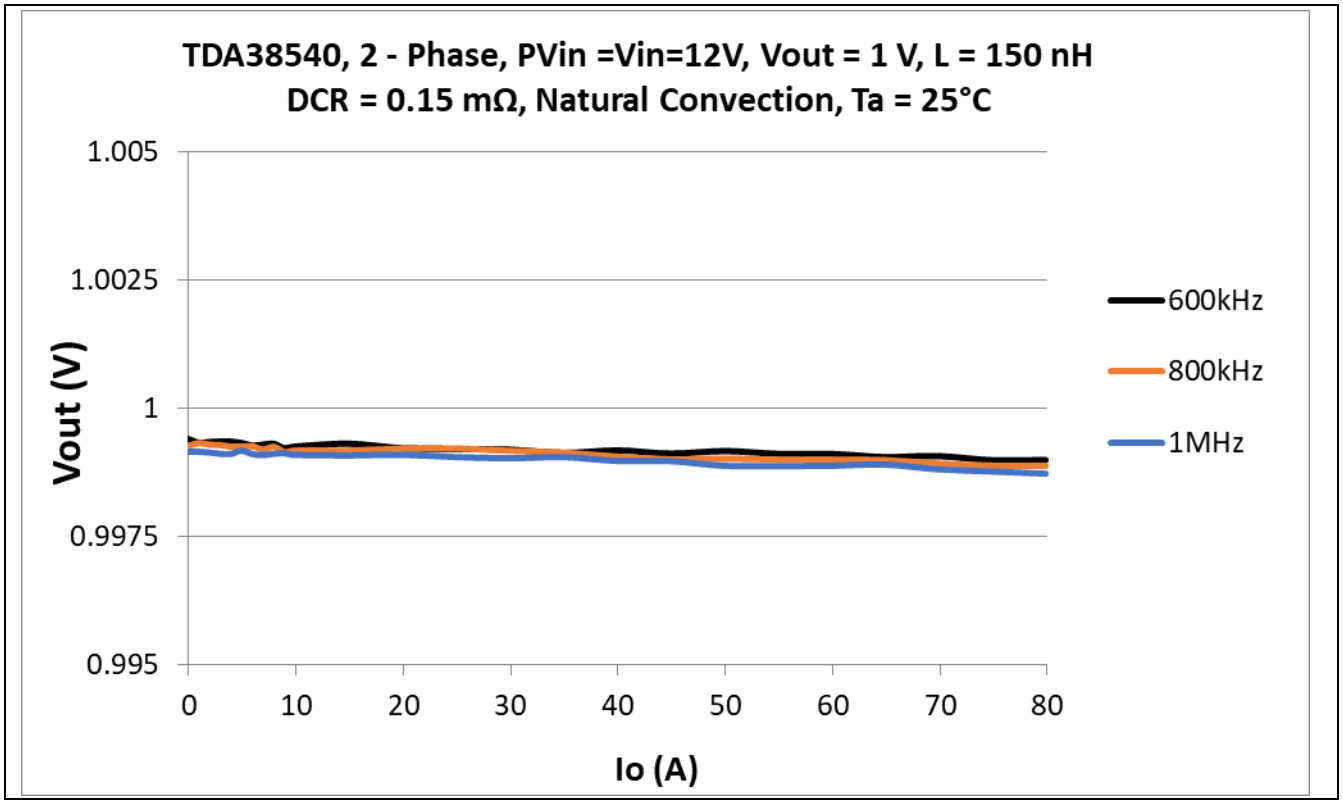


Figure 31 **TDA38540 V_{out} regulation (12 V_{in}, 1.0 V_{out}, 150 nH, 600 kHz/800 kHz/1 MHz, T_a = 25°C)**

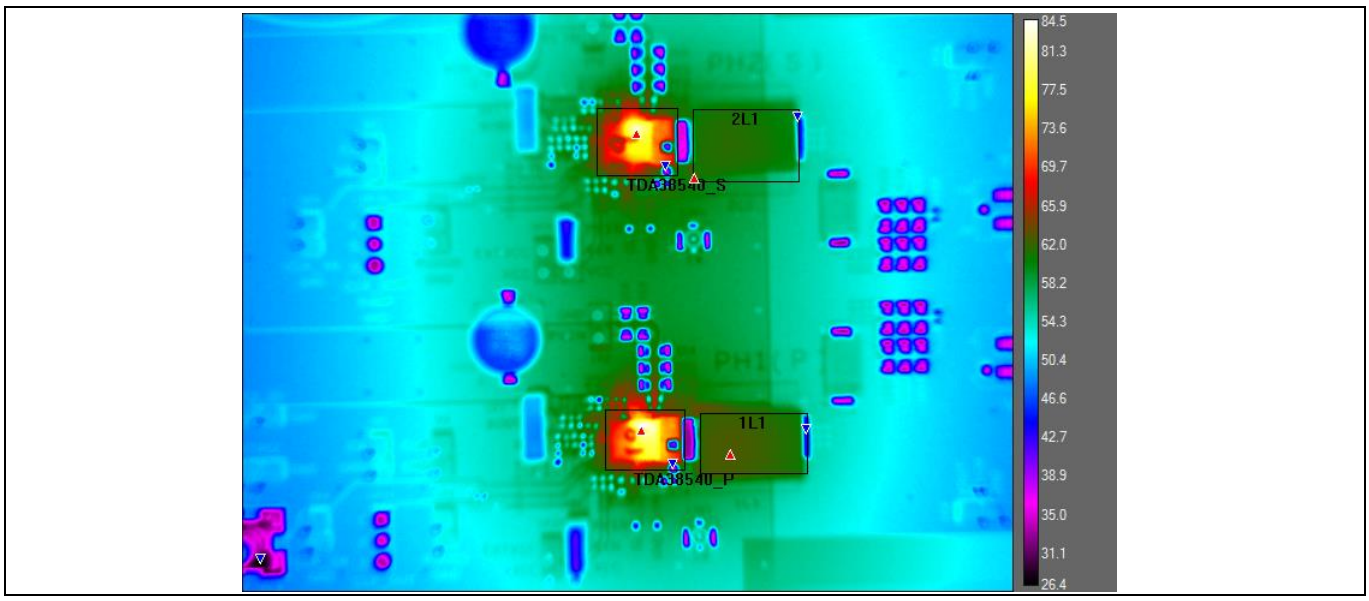


Figure 32 **Thermal image of the board at 80 A load TDA38540 (P) = 84.5 °C, L (P) = 62°C, TDA38540 (S) = 82°C, L (S) = 61°C, f_{sw} = 600 kHz, T_a = 26°C, natural convection**

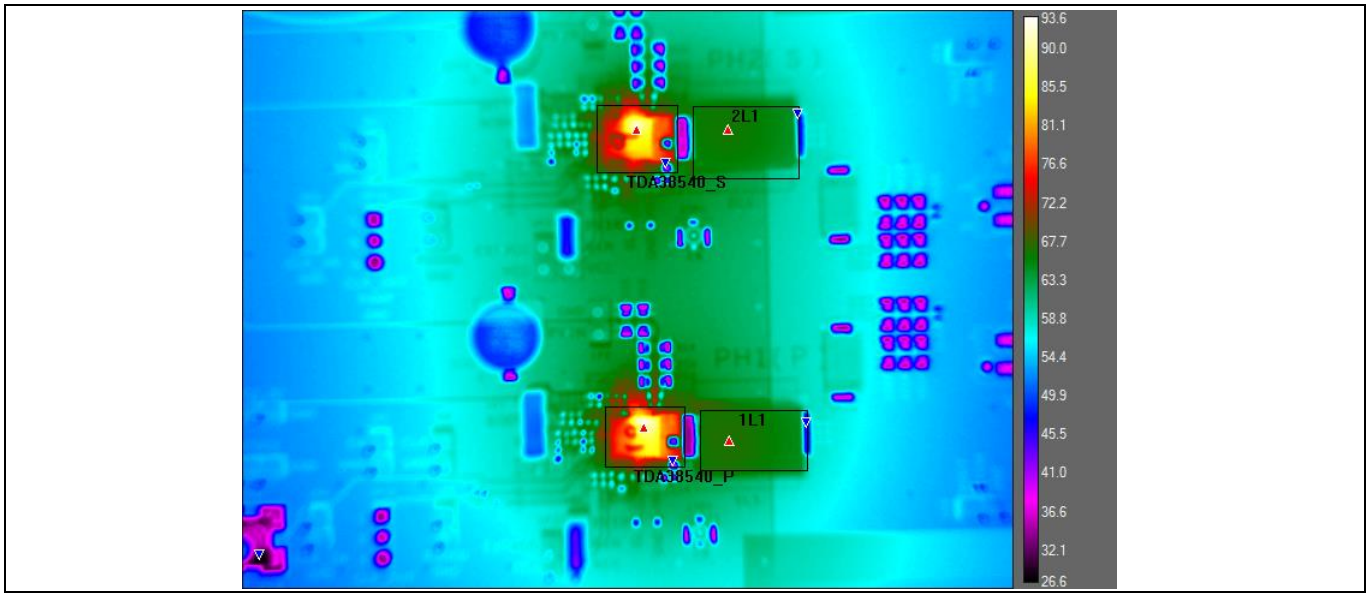


Figure 33 **Thermal image of the board at 80 A load TDA38540 (P)= 94°C, L (P) = 66°C, TDA38540 (S)= 91°C, L (S) = 66°C, F_{sw} = 800 kHz, T_a = 26°C , natural convection**

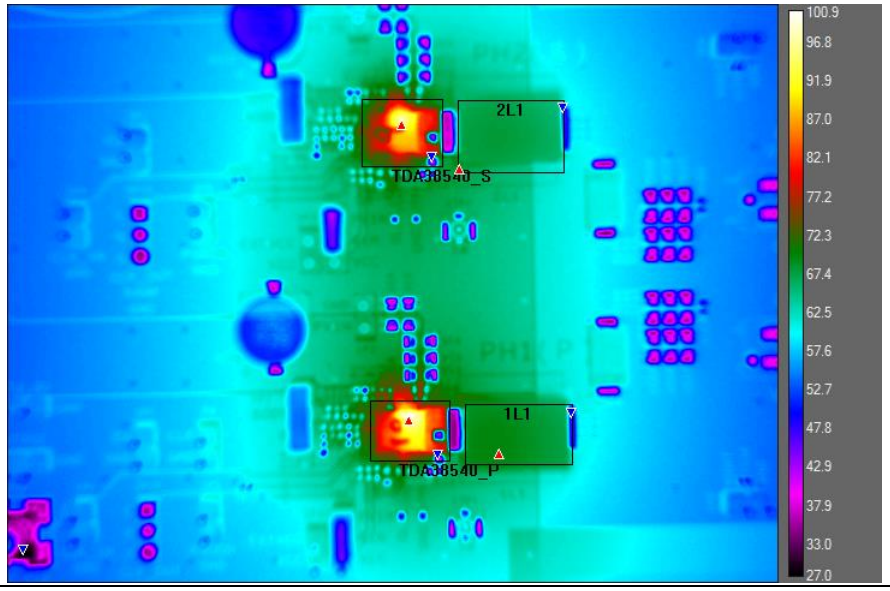


Figure 34 **Thermal image of the board at 80 A load TDA38540 (P)= 101°C, L (P) = 69°C, TDA38540 (S)= 97°C, L (S) = 68 °C, F_{sw} = 1000 kHz, T_a = 26°C, natural convection**

References

[1] Infineon Technologies AG: *TDA38540 OptiMOS™ IPOL 40 A single-voltage synchronous buck regulator datasheet*.

Revision history

Document revision	Date	Description of changes
V 1.0	2024-05-31	Initial release

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