EVAL_IGK120B041S_GaN user guide

CoolGaN™ BDS evaluation board

About this document

Scope and purpose

This user guide provides an overview of the EVAL_IGK120B041S_GaN Evaluation Board including its main features, key components, pin assignments, and mechanical dimensions.

EVAL_IGK120B041S_GaN is a small daughter board designed specifically to assemble and evaluate SG-UFWLB-12 pin BGA (WLCSP-1.2 x1.7 mm) package GaN bidirectional switch (BDS) [1]. The berg stick connector on this evaluation board is in line with the board-to-board connector on the EVAL_GD_BDS_GaN Evaluation Board, which eventually can be used a gate driver for this BDS board.

Note: This board is sensitive to ESD and must be used only under laboratory conditions.

Intended audience

This document is primarily intended to guide engineers evaluating bidirectional GaN switch performance.

About this product group

Target applications

- Consumer Electronics: USB-C chargers and load switches
- eFuses
- Battery management systems (BMS)

Product family

CoolGaN™ BDS are normally-off monolithic GaN bidirectional switches with dual-gate independent control, enabling a common-drain structure for blocking voltage and current in both directions. They replace multiple unidirectional switches, reducing component count while improving switching speed and overall performance. CoolGaN™ BDS switches enhance efficiency, power density, and reliability in applications.

Evaluation Board

This board can be used during design-in process for evaluation and measurement of characteristics, and proof of data sheet specifications of the said GaN BDS.

Note: PCB and auxiliary circuits are NOT optimized for final customer design.

Safety precautions

Note: *Please note the following warnings regarding the hazards associated with development systems.*

Table 1 Safety precautions

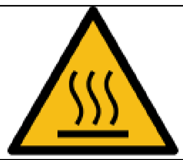
	**Warning**: *The evaluation or reference board contains DC bus capacitors, which take time to discharge after removal of the main supply. Before working on the drive system, wait 5 minutes for capacitors to discharge to safe voltage levels. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Warning:** *Remove or disconnect power from the drive before you disconnect or reconnect wires or perform maintenance work. Wait five minutes after removing power to discharge the bus capacitors. Do not attempt to service the drive until the bus capacitors have discharged to zero. Failure to do so may result in personal injury or death.*
	**Caution:** *The heat sink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.*
	**Caution:** *Only personnel familiar with the drive, power electronics and associated machinery should plan, install, commission and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.*
	**Caution:** *The evaluation or reference board contains parts and assembly's sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	**Caution:** *A drive that is incorrectly applied or installed can lead to component damage or reduction in product lifetime. Wiring or application errors such as under sizing the motor, supplying an incorrect or inadequate AC supply, or excessive ambient temperatures may result in system malfunction.*
	**Caution:** *The evaluation or reference board is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials that are unnecessary for system installation may result in overheating or abnormal operating conditions.*

Table of contents

1 The board at a glance

The EVAL_IGK120B041S_GaN Evaluation Board consists of a GaN bidirectional switch (BDS) in the SG-UFWLB-12 pin BGA (WLCSP-1.2 x 1.7 mm) package. The board has 3 Input terminals namely, D1 (Drain 1), D2 (Drain 2), and G (Gate).

The input terminals (berg stick) are in line with the board to board-to-board connector terminals on EVAL_GD_BDS_GaN Evaluation Board.

1.1 Scope

This evaluation board intended to evaluate bidirectional GaN switch performance.

1.2 Block diagram

Figure 1 shows a typical block diagram of the EVAL_IGK120B041S_GaN Board consisting of 3 terminals D1, D2, and G.

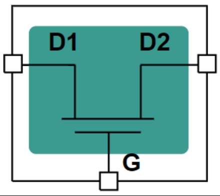


Figure 1 EVAL_IGK120B041S_GaN block diagram

1.3 Main features

- 40 V, 9 mΩ GaN BDS switch (IGK120B041S) [1], specifically designed for SG-UFWLB-12 pin BGA (WLCSP-1.2 x 1.7 mm) package
- Maximum current of 20 A

1.4 Board parameters and technical data

Table 2 EVAL board parameters

Parameter	Symbol	Conditions	Value			Unit
			Min	Nom.	Max.	
Drain-drain on state resistance	$R_{DD(on)}$	V_{GD} = 5V, I_D = 5A	–	9	12	mΩ
Continuous drain-drain voltage	V_{D1D2}	–	–	–	40	V
Gate-drain voltage	V_{GD1} or V_{GD2}	–	-40	–	6	V
Drain current	Idd	T_{amb} = 25°C	–	–	20	A
System environment						
Ambient temperature	$T_{amb.}$	–	–	25	–	°C
PCB characteristics						
Dimensions	L	Length	–	27.7	–	mm
	W	Width	–	12.5	–	mm
	H	Height	–	7.6	–	mm

Parameter	Symbol	Conditions	Value			Unit
			Min	Nom.	Max.	
No. of layers	–	–	–	4	–	–
PCB thickness	–	–	–	1.6	–	mm
Copper thickness	–	All layers	–	1	–	oz.
Weight	–	Weight of entire PCB assembly	–	–	–	g
Material	–	FR-4, RoHS-compliant				

2 System and functional description

This evaluation board is designed to evaluate a single GaN BDS in the SG-UFWLB-12 pin BGA (WLCSP-1.2 x 1.7 mm) package.

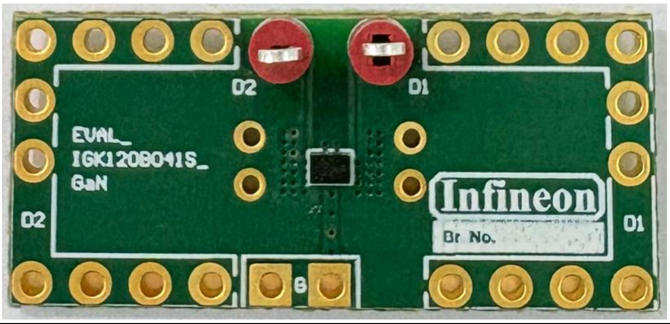


Figure 2 **EVAL_IGK120B041S_GaN Evaluation Board**

Figure 3 **EVAL_IGK120B041S_GaN as a daughter board for EVAL_GD_BDS_GaN gate driver evaluation board**

The GaN BDS switch in this evaluation board can be used along with the gate driver evaluation board (such as EVAL_GD_BDS_GaN) to drive this common-source configuration.

When the gate is referenced to D2 and V_{GD2} exceeds $V_{GD(th)}$ of the GaN BDS switch, bidirectional current flow is enabled. With V_{GD2} = 5 V, current can flow in both directions with minimal voltage drop ($R_{ON} \times I_{Load}$) and low power loss. If the gate signal is off with respect to D2 (i.e. V_{GD2} = 0 V), the channel acts like a diode, permitting conduction only from D2 to D1 with a higher voltage drop (2 to 2.5 V) [2].

Similarly, when the gate is referenced to D1 and V_{GD1} exceeds $V_{GD(th)}$, the bidirectional flow is again enabled. When the gate is turned off with respect to D1 (i.e., V_{GD1} = 0 V), the channel acts like a diode in other direction, allowing the conduction from D1 to D2 with a higher voltage drop [2].

Thus, when the current direction is fixed, then referencing to a particular ground reference helps to control the GaN BDS switch effectively [2].

3 System design

3.1 Schematics

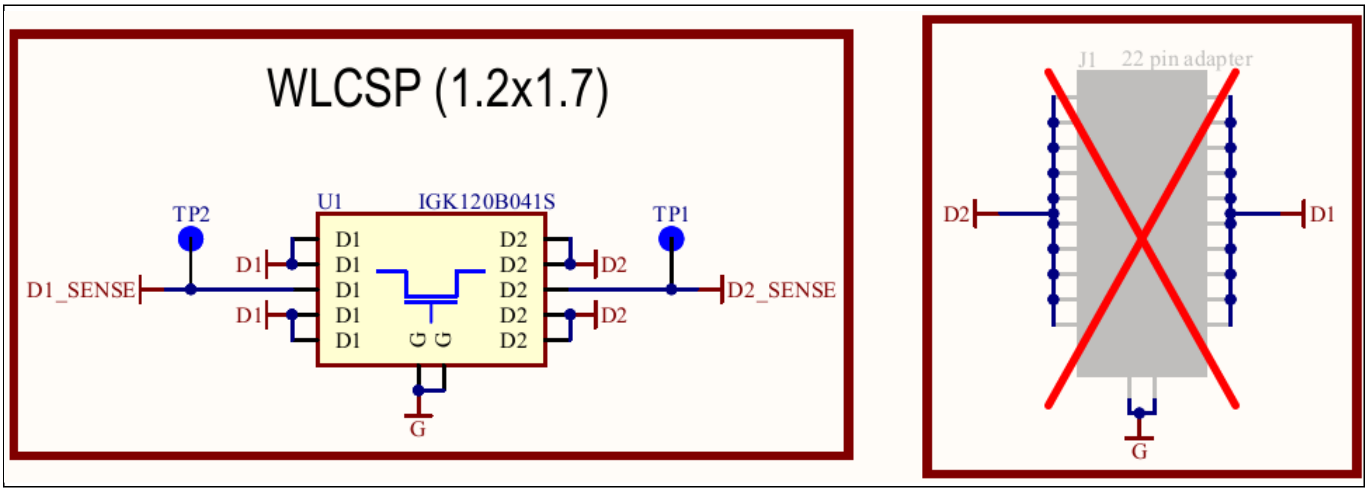


Figure 4 EVAL_IGK120B041S_GaN schematics

3.2 Layout

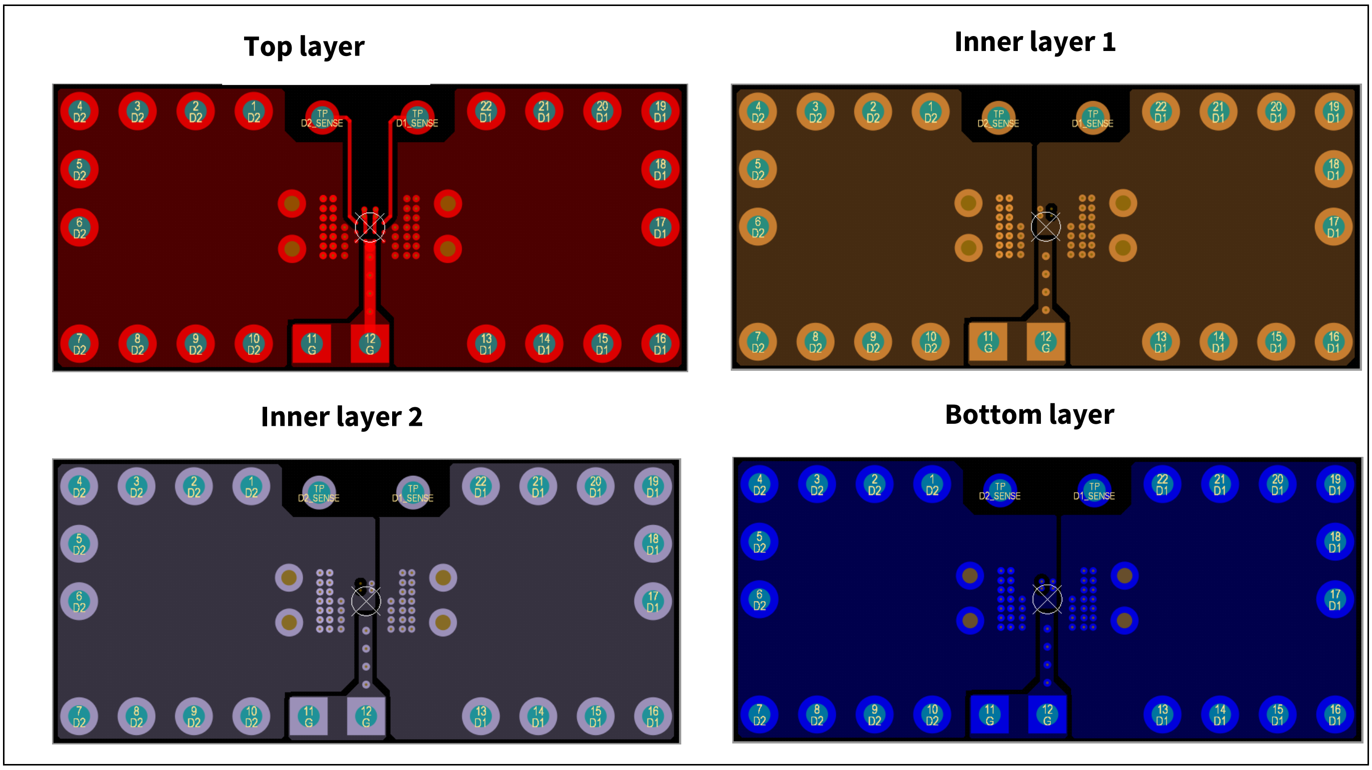


Figure 5 EVAL_IGK120B041S_GaN - layout (top view)

3.3 Bill of materials

The complete bill of materials is available on the download section of the board webpage. A log-in is required to download this material.

Table 3 BOM of the most important/critical parts of the evaluation or reference board (example)

S. No.	Ref designator	Description	Manufacturer	Manufacturer P/N	Populated
1	Q1	40 V 9 mΩ GaN BDS common source	Infineon Technologies	IGK120B041S	Yes

3.4 Connector details

Table 4 Connectors

Pin	Label	Function
D2	J1 – pins 1, 2, 9, 10	Drain-2 power input/output
D1	J1 – pins 13, 14, 21, 22	Drain-1 power input/output
G	J1 – pins 11, 12	Gate

4 System performance

4.1 Test points

Table 5 Test points

TP No.	Net	Description
TP1	D2 – Sense	Test point for Drain-2 Ron Sense
TP2	D1 – Sense	Test point for Drain-1 Ron Sense

4.2 BDS – Independent evaluation

4.2.1 Test setup

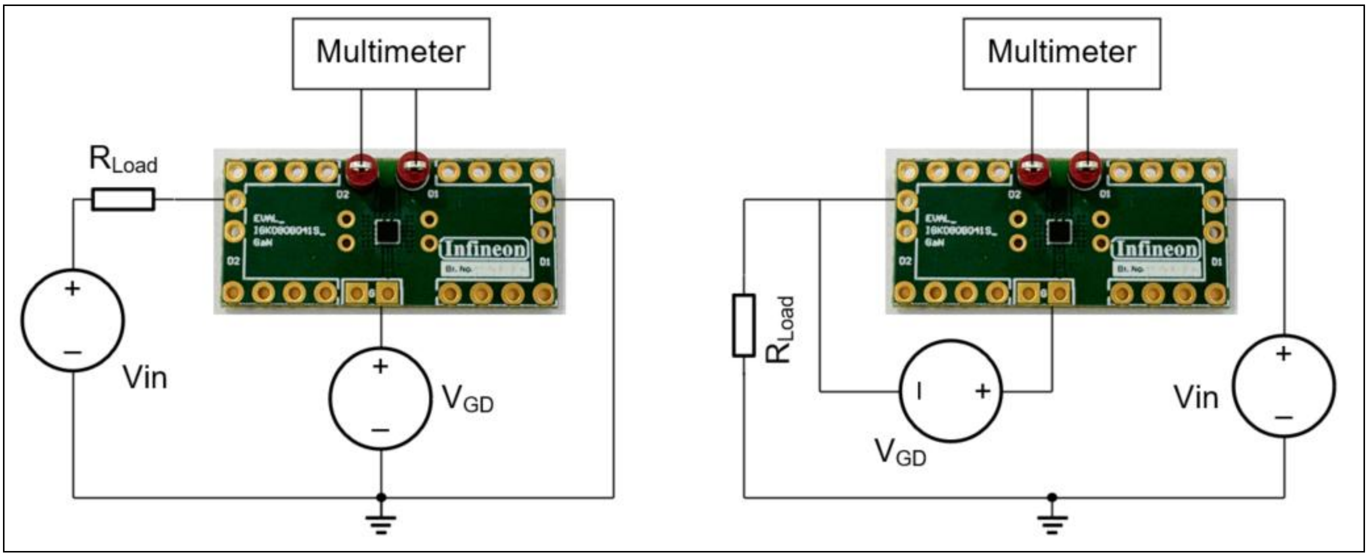


Figure 6 Test setup

Figure 6 represents the test setups to validate the GaN BDS in the EVAL_IGK120B041S_GaN Evaluation Board and test its operation at the required conditions. The input supply (Vin) can be given to either of the drain potentials (D1 or D2) and the gate voltage is given with respect to the other drain as shown in Figure 6. Also, BDS can be used in either the low or high side configuration, provided the gate voltage needs to be given with respect to the drain potential that is not connected to the input supply.

4.2.2 On-state resistance (R_{on}) vs. drain current (I_{Drain})

Table 6 Measurement results - R_{on}, Tc vs. Id at V_{D1} = 20 V and varying ambient temperature

V_{D1} = 20 V, V_{GD2} = 5 V	T_{amb}=25°C		T_{amb}=85°C	
I_{Drain}	R_{on}	Tc_{BDS}	R_{on}	Tc_{BDS}
0.1 A	10.0 mΩ	25.0°C	15.0 mΩ	85.0°C
1 A	9.8 mΩ	25.2°C	15.1 mΩ	85.3°C
2 A	9.9 mΩ	25.4°C	15.2 mΩ	85.8°C
3 A	10.1 mΩ	25.6°C	15.4 mΩ	86.0°C
4 A	10.3 mΩ	25.8°C	15.9 mΩ	86.9°C
5 A	10.7 mΩ	26.1°C	16.6 mΩ	87.3°C
6 A	11.2 mΩ	26.5°C	17.7 mΩ	87.9°C
7 A	11.9 mΩ	27.4°C	19.3 mΩ	89.1°C
8 A	12.6 mΩ	28.1°C	21.8 mΩ	90.2°C
9 A	13.5 mΩ	29.5°C	23.9 mΩ	91.5°C
10 A	14.4 mΩ	30.8°C	25.6 mΩ	92.8°C

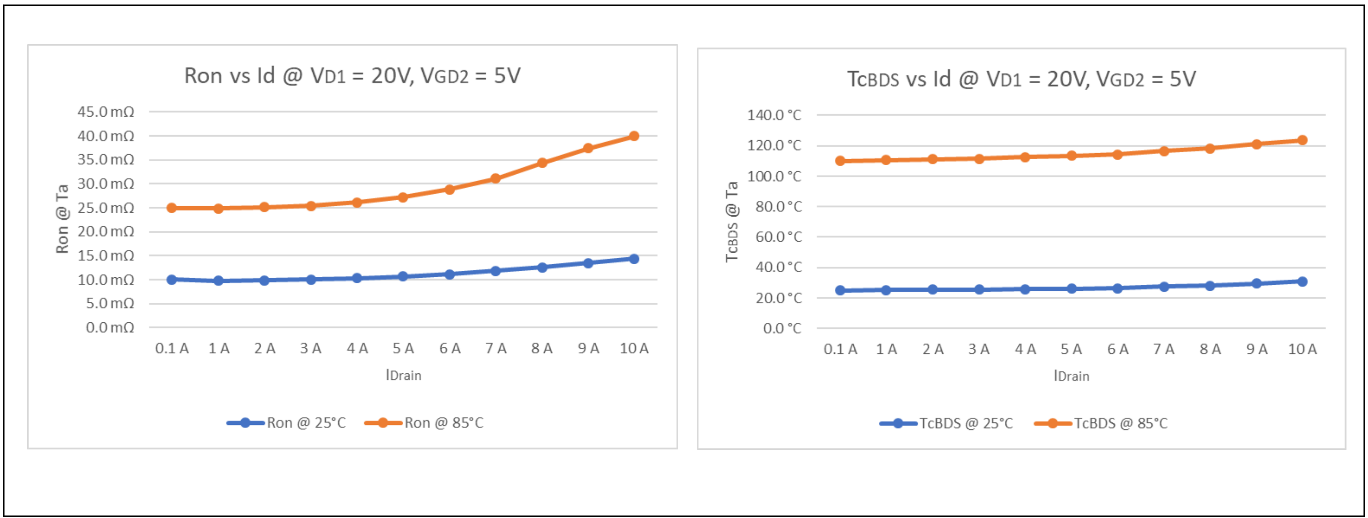


Figure 7 BDS R_{on} and case temperature (Tc) variation with respect to drain current (Id) at V_{D1} = 20 V

Key insights from the above measurements:

- **R_{on} is strongly temperature dependent**: at each current point, R_{on} at 85°C is ~1.5–1.8× higher than at 25°C
- **R_{on} increases with I_{Drain}** (load/self-heating effects):
  - **25°C:** R_{on} is fairly flat up to ~3–4A (≈9.8–10.3 mΩ), then rises to 14.4 mΩ at 10A (~+47% from 1 A)
  - **85°C:** R_{on} rises more steeply with current, 15.0 mΩ at 0.1 A to 25.6 mΩ at 10A (~+71%), indicating stronger thermal/operating-point sensitivity at high ambient
- **Tc_{BDS} tracks ambient with modest self-heating:**
  - At 25°C ambient, Tc_{BDS} increases 25.0 to 30.8°C from 0.1 to 10 A (≈5.8°C rise)

  - At 85°C ambient, Tc_{BDS} increases 85.0 to 92.8°C (≈7.8°C rise).
    This suggests the device is not undergoing extreme heating in this setup, but the extra junction/case rise at higher current correlates with the Ron increase.
- For higher-current operation, both ambient temperature and load current noticeably raise R_{on} (hence conduction loss). The "knee" where Ron starts rising faster is around 5–6 A, especially at 85°C

4.2.3 On-state resistance (R_{on}) and gate leakage current (I_{gss}) vs. gate-drain voltage (V_{GD2})

Table 7 Measurement results - R_{on} vs. V_{GD2} at V_{D1} =5 V and 28 V, Id = 1 A

	V_{D1} = 5 V, IDrain = 1 A			V_{D1} = 28 V, IDrain = 1 A		
V_{GD2}	R_{on} at 25°C	R_{on} at 85°C	R_{on} at -40°C	R_{on} at 25°C	R_{on} at 85°C	R_{on} at -40°C
3.5 V	12.8 mΩ	21.9 mΩ	8.0 mΩ	13.2 mΩ	22.6 mΩ	8.1 mΩ
4.0 V	11.2 mΩ	17.5 mΩ	7.2 mΩ	11.4 mΩ	17.9 mΩ	7.2 mΩ
4.5 V	10.3 mΩ	15.6 mΩ	6.8 mΩ	10.6 mΩ	16.0 mΩ	6.8 mΩ
5.0 V	10.0 mΩ	14.9 mΩ	6.6 mΩ	10.3 mΩ	15.7 mΩ	6.7 mΩ
5.5 V	9.6 mΩ	14.0 mΩ	6.4 mΩ	9.8 mΩ	14.4 mΩ	6.4 mΩ

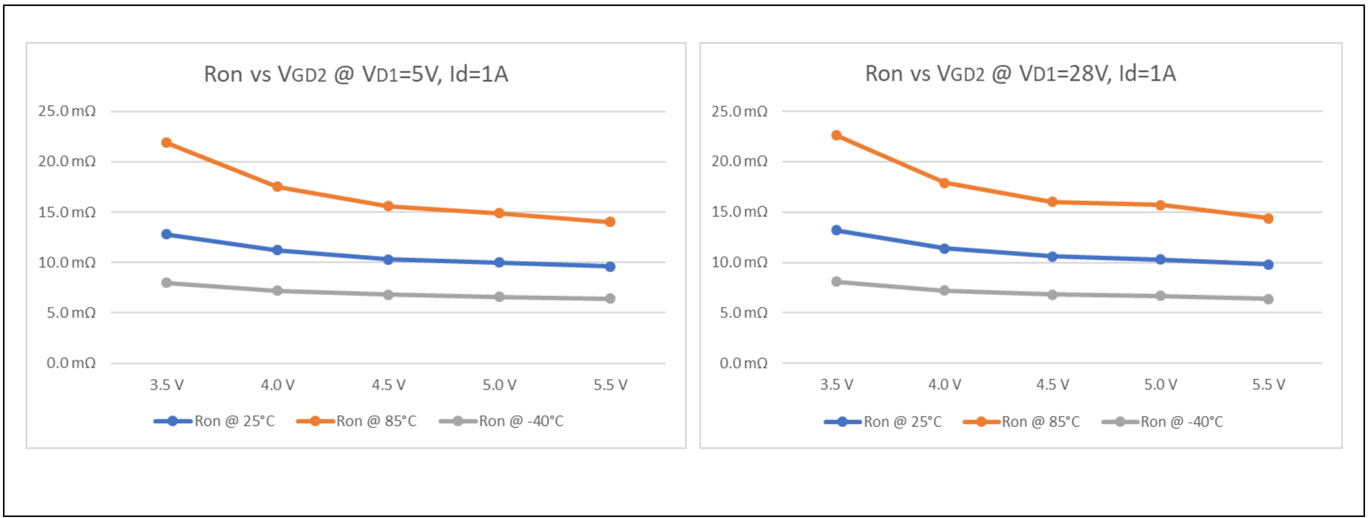


Figure 8 R_{on} variations with respect to gate-drain voltages (V_{GD2}) at V_{D1} = 5 V and 28 V

Key insights from the measurements:

- **R_{on} decreases with higher V_{GD2}** (stronger gate drive) at all temperatures, with the biggest improvement from 3.5 to 4.0 V, and **diminishing returns above ~5.0 V**
- **Temperature has a strong impact on R_{on}** (similar to MOSFET $R_{DS(on)}$):
  - At V_{GD2}=5.0 V, V_{D1}=5 V: 6.6 mΩ (at −40°C) to 10.0 mΩ (at 25°C) to 14.9 mΩ (@85°C).
    That's ~+50% from −40 to 25°C and ~+49% from 25 to 85°C (overall ~2.3× from −40 to 85°C).
  - The temperature penalty is worse at lower V_{GD2} (device is less strongly enhanced):
    at 3.5 V: 8.0 to 12.8 to 21.9 mΩ (~2.7× from −40 to 85°C), versus at 5.5 V: 6.4 to 9.6 to 14.0 mΩ (~2.2×)
- **V_{D1} (5 V vs. 28 V) barely affects R_{on}** at 1 A: values differ only slightly (typically ~0.1–0.7 mΩ, i.e., a few percent). This suggests R_{on} is dominated by **channel conduction set by V_{GD2} and temperature**, not by V_{D1} in this test range

- If you need stable/low R_{on} across temperature**, driving V_{GD2} to ~5.0–5.5 V** materially reduces R_{on} and also **reduces sensitivity to temperature**, while going from 5.0 to 5.5 V yields only a small additional R_{on} benefit

Table 8 Measurement results - I_{gss} vs. V_{GD2} at V_{D1} =5 V and 28 V, Id = 1 A

	V_{D1} = 5 V, IDrain = 1 A			V_{D1} = 28 V, IDrain = 1 A		
V_{GD2}	I_{gss} at 25°C	I_{gss} at 85°C	I_{gss} at -40°C	I_{gss} at 25°C	I_{gss} at 85°C	I_{gss} at -40°C
3.5 V	1.20 uA	1.30 uA	1.20 uA	1.20 uA	1.35 uA	1.21 uA
4.0 V	1.30 uA	1.76 uA	1.24 uA	1.32 uA	1.80 uA	1.25 uA
4.5 V	1.72 uA	3.01 uA	1.40 uA	1.72 uA	3.02 uA	1.41 uA
5.0 V	2.92 uA	6.28 uA	1.93 uA	2.90 uA	6.35 uA	1.95 uA
5.5 V	6.10 uA	15.03 uA	3.25 uA	6.10 uA	15.15 uA	3.25 uA

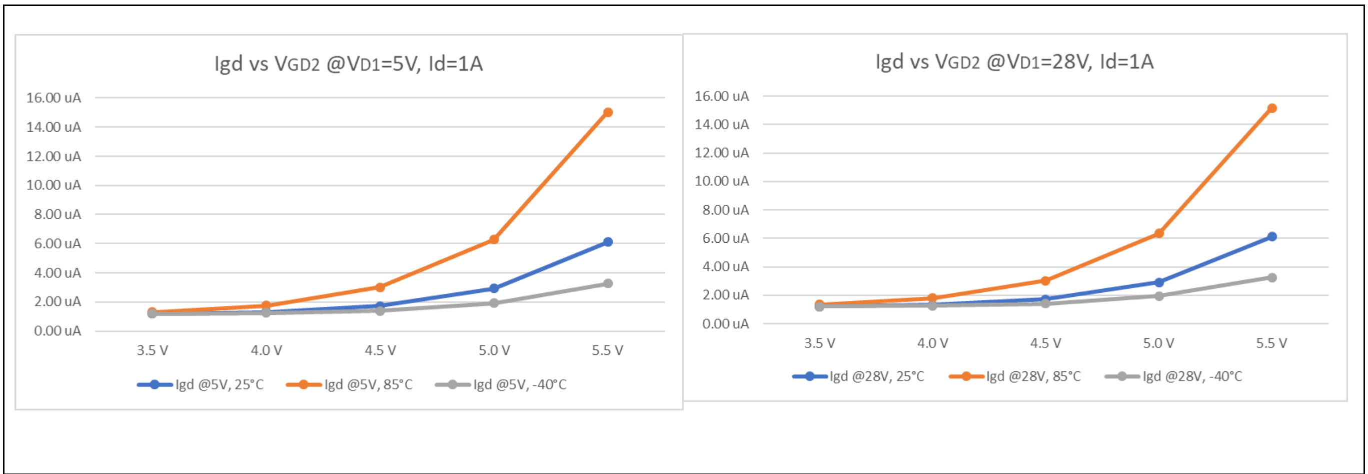


Figure 9 Gate leakage current (Igss) variations with respect to gate-drain voltages (V_{GD2}) at V_{D1} = 5 V and 28 V

Key insights from the measurements:

- **I_{gss} increases strongly with V_{GD2}** (gate bias dependence). This indicates leakage is much more sensitive to higher gate bias, especially at high temperature
- **I_{gss} increases with temperature at a fixed V_{GD2}**, and the temperature sensitivity grows at higher V_{GD2}
- **V_{D1} (5 V vs. 28 V) has essentially no impact on I_{gss}**: values are identical or differ by only ~0.01–0.12 µA (measurement noise level). This suggests I_{gss} is dominated by the gate structure/bias and temperature, not by V_{D1}
- Using higher V_{GD2} (≥5 V) will significantly increase gate leakage—particularly at 85°C—which can matter for standby current budgets or high-impedance gate-drive sources

4.3 Evaluation with gate driver board EVAL_GD_BDS_GaN

4.3.1 Test setup

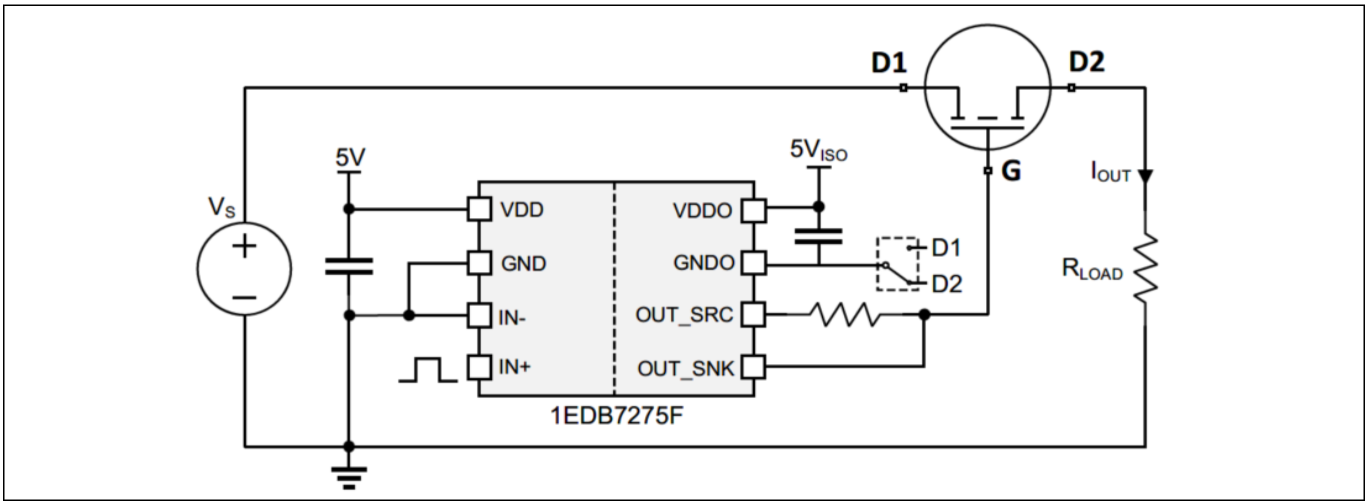


Figure 10 GaN BDS as a high-side switch using 1EDB7275F isolated gate driver

Figure 10 shows high-side operation of the GaN BDS using the isolated gate driver 1EDB7275F from Infineon for unidirectional current flow. The gate reference selector switch allows the gate return path to be connected to either D1 or D2, depending on the intended direction of current flow. The 1EDB7275F has a UVLO threshold of 4.2 V and thus can be powered directly from a 5 V supply.

4.3.2 Cyclic turn on/off waveform

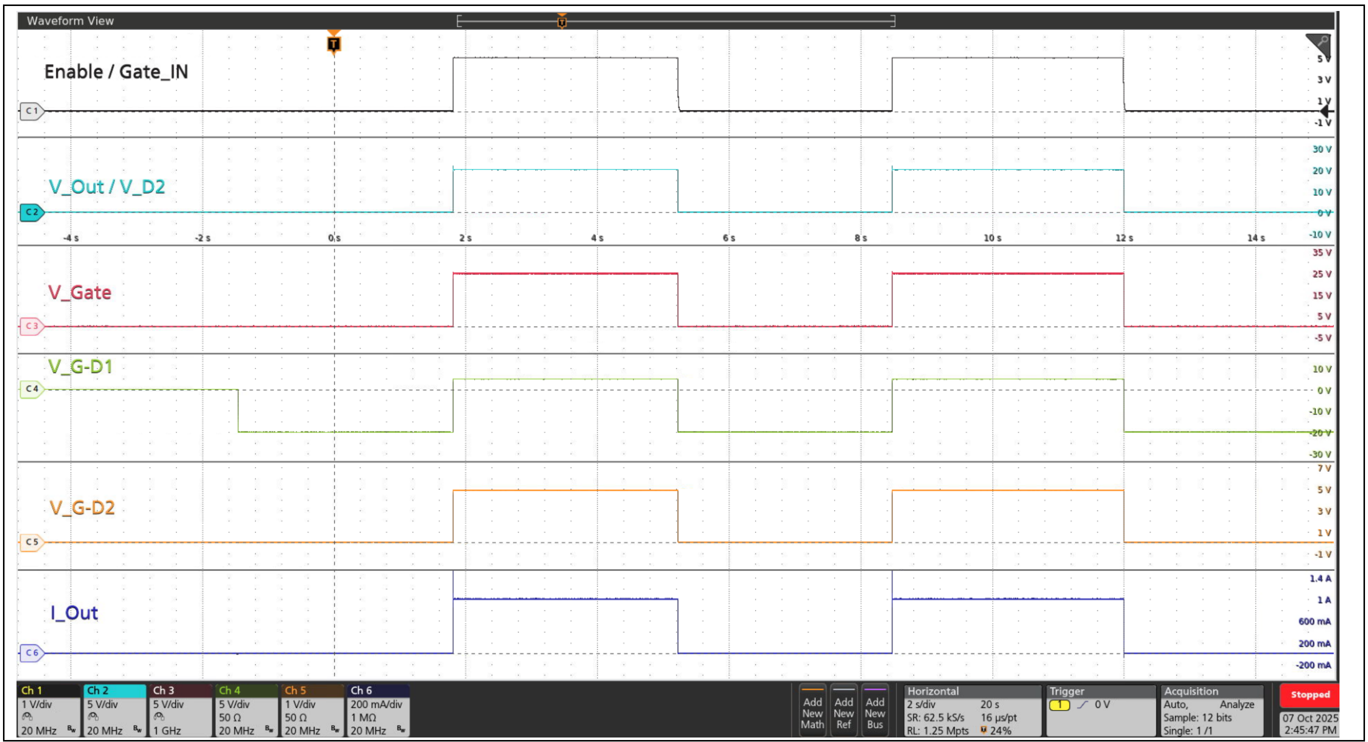


Figure 11 Unidirectional current flow and gate reference to D2

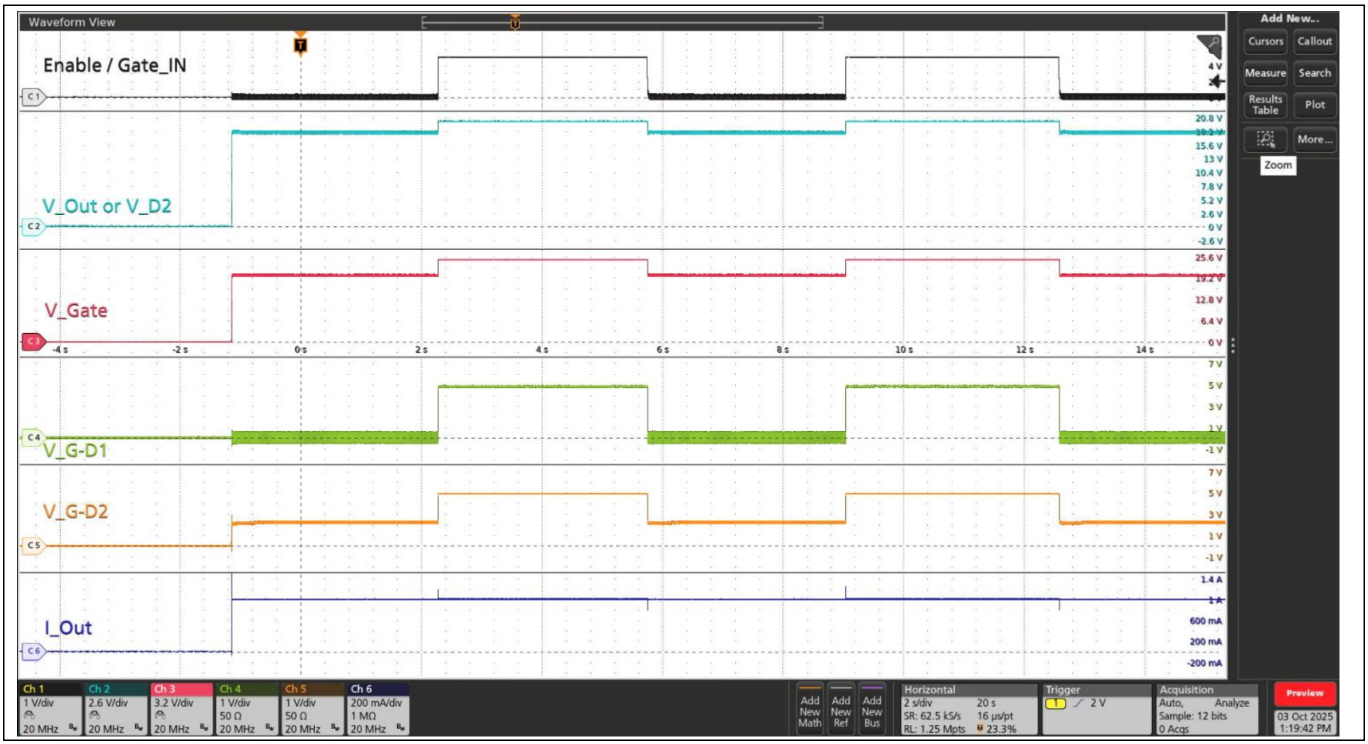


Figure 12 Unidirectional current flow and gate reference to D1

For the circuit in Figure 10 (with V_S = 20 V and R_{Load} = 20 Ω), Figure 11 shows the corresponding waveforms when the gate voltage is referenced to D2. When the power supplies (V_S and V_{DD}) are on and Enable/IN is inactive, gate voltage V_G = V_{GD2} = 0 V, and thus V_{GD1} = –20 V. Asserting Enable/IN causes V_{GD2} to increase to 5 V (V_G = 25 V), thereby turning on the GaN BDS.

For the same circuit, when the gate is referenced to D1, Figure 12 shows the corresponding waveforms. When the power supplies (V_S, V_{DD}, and V_{DDO}) are on and Enable/IN is inactive, gate voltage V_G = V_{GD1} = 20 V, turns on the GaN BDS and allows current flow from D1 to D2, with a significant voltage drop (V_{D1D2} ≈ 2 V), similar to diode mode. Asserting Enable/IN increases V_{GD1} to 5 V (V_G = 25 V), fully turning on the GaN BDS and decreasing the voltage drop to R_{ON} × I_{OUT}.

4.3.3 Startup Behavior

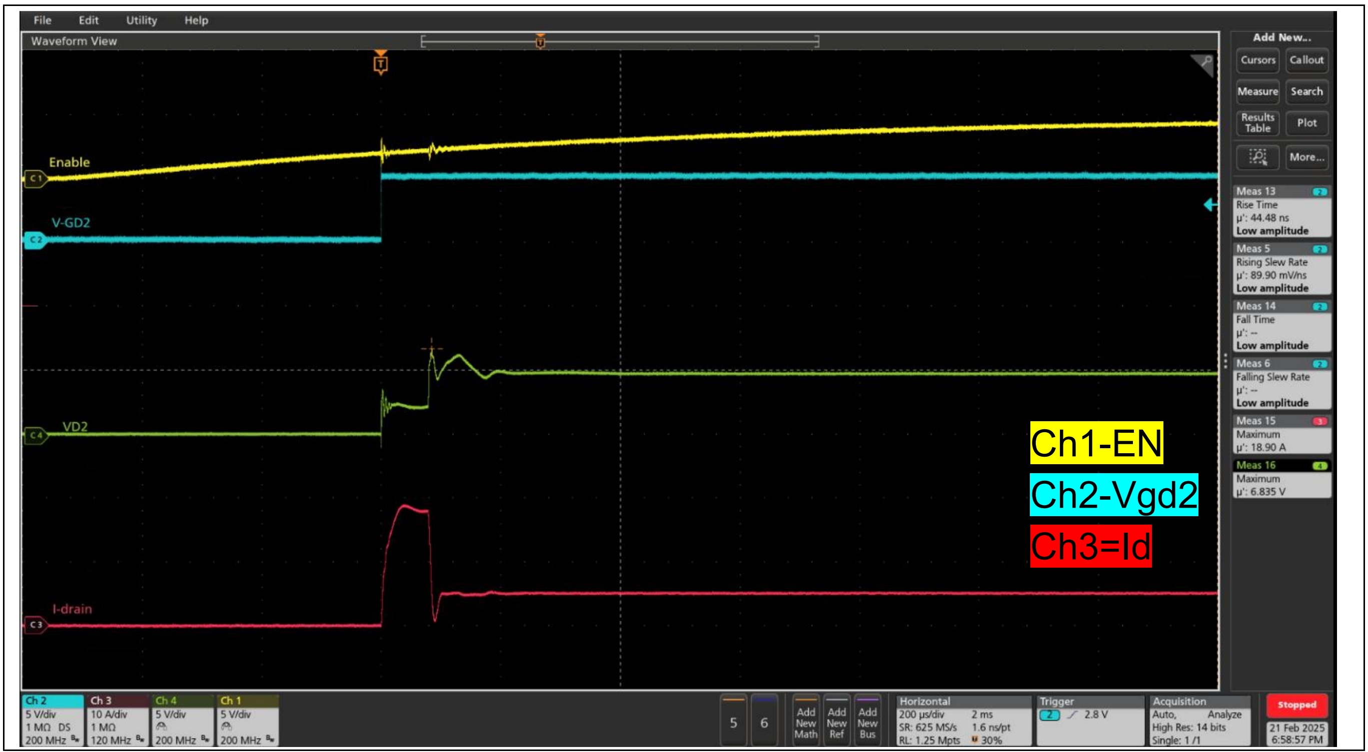


Figure 13 **Turn on without RC delay on gate drive path- V_{D1}=5 V, Id=10 A (load), V_{GD2} = 0 V to 5 V, Id_max = 18.9 A, t_Imax = 120 us**

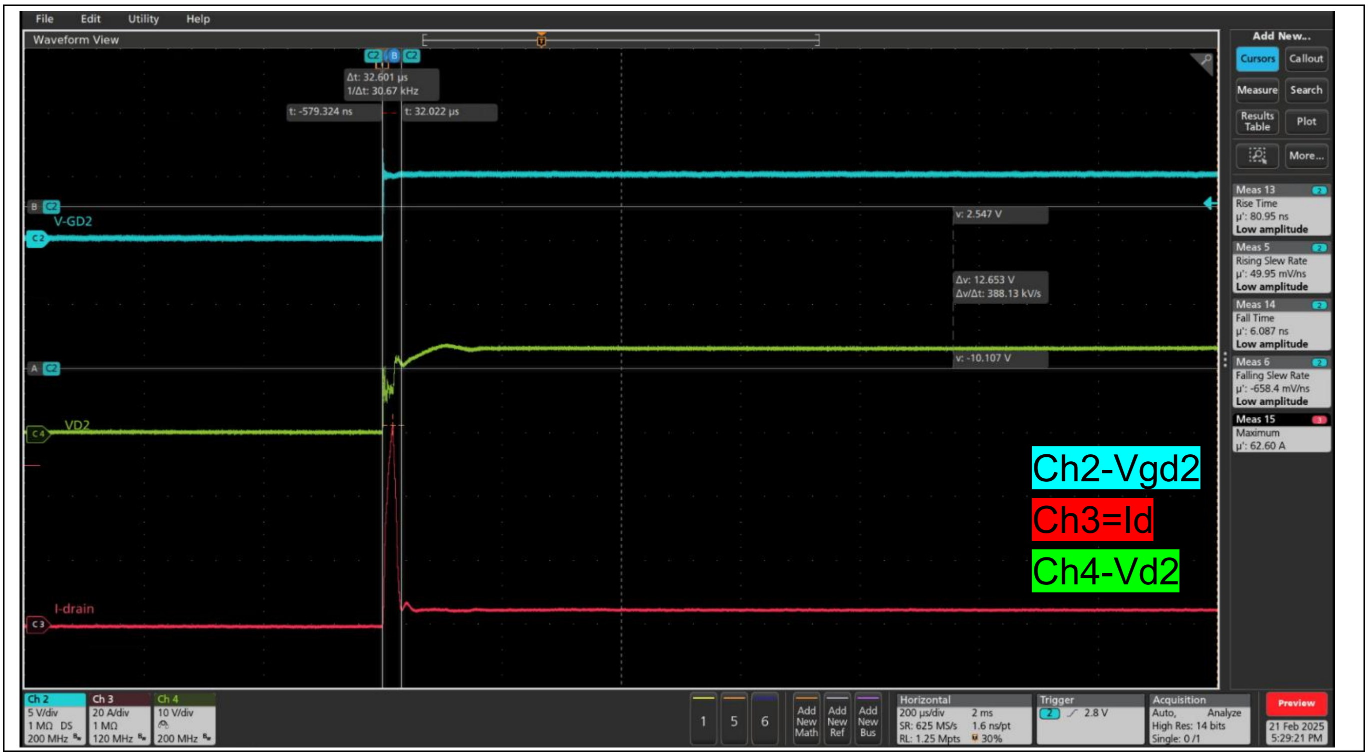


Figure 14 **Turn on without RC delay on gate drive path- V_{D1}=20 V, Id=5 A (load), V_{GD2} = 0 V to 5 V, Id_max = 62.6 A, t_Imax = 32.6 us**

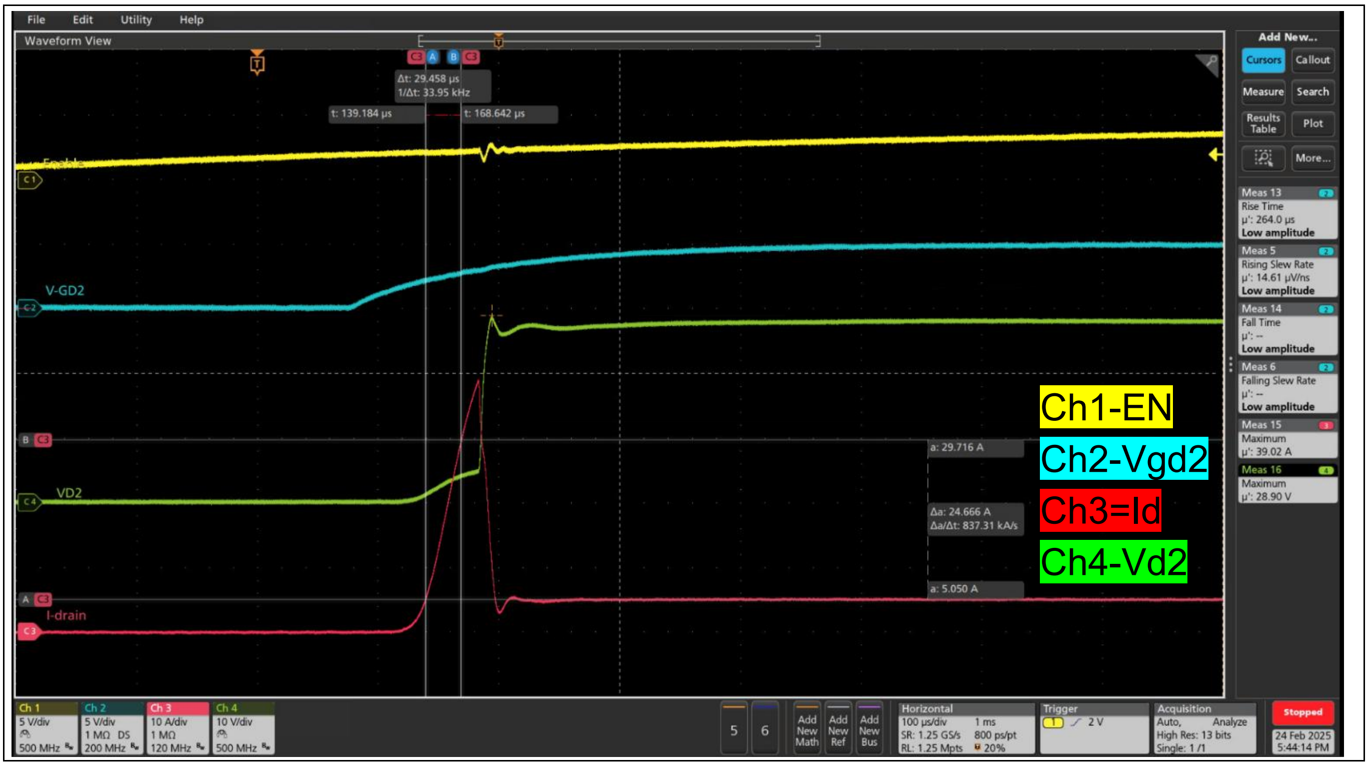


Figure 15 **Turn on with RC (1 kΩ, 100nF) delay on gate drive path- V_{D1}=28 V, Id=5 A (load), V_{GD2} = 0 V to 5 V, Id_max = 39.02 A, dI/dt = 0.837 A/us**

Since the isolated gate driver voltage is supplied externally, turn-on is fast with negligible delay. However, rapid turn-on can cause large inrush currents, which can damage the BDS if not controlled. Additionally, the inrush current increases with the increase in input voltage applied to the drain terminal.

By using an RC delay circuit on the gate terminal, the turn-on can be slowed, and inrush current can be limited.

5 Conclusion

This user guide provides a comprehensive overview of the working and results for the 40 V, 9 mΩ, GaN BDS evaluation board, enabling the user to start experimenting and working with the 1.2 x 1.7 mm WLCSP package BDS.

The board demonstrates the on-state resistance and device temperature variations with respect to the increasing drain current, as well as the variations in the on-state resistance with the changes in the gate drain voltage.

Note that these device parameter values measured are strictly for the particular device tested and may vary. However, these values will always be within the limits specified in BDS datasheet.

6 Related resources

- Gallium nitride (GaN) webpage
- EVAL_GD_BDS_GaN Evaluation Board
- Infineon Developer Community: GaN forum

References

[1] Infineon Technologies AG. Datasheet (2026): *IGK120B041S V 1.1*; Available online

[2] Infineon Technologies AG. Whitepaper (2026): *Gate driving techniques for medium voltage GaN bidirectional switches*; Available online

Glossary

Table 9 Abbreviations

Abbreviation	Expansion
BDS	Bidirectional switch
EN	Enable
EVAL	Evaluation
GaN	Gallium Nitride
GD	Gate driver
PCB	Printed circuit board

Revision history

Document revision	Date	Description of changes
V 1.0	2026-06-15	Initial release

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