Half-bridge evaluation board with 100 V CoolGaN™ power transistor and EiceDRIVER™ 1EDN7126G gate driver user guide

About this document

Scope and purpose

This user guide provides an overview and detailed feature description of the EVAL_7126G_100V_GaNc general purpose half-bridge evaluation board with the CoolGaN™ power transistor IGC033S10S1 and EiceDRIVER™ 1EDN7126G TDI gate driver. The board can be used for testing and assessing the performance of the products in half-bridge applications such as DC-DC conversion or motor drives. It provides a flexible platform for evaluating and optimizing the switching performance of these products under different operating conditions. Additionally, it gives a reference for the recommended PCB layout for a half-bridge and gate driving circuit with these products.

EVAL_7126G_100V_GaNc Evaluation Board is designed to showcase the performance of the IGC033S10S1 transistor when used with the 1EDN7126G gate driver in a half-bridge configuration. It provides optimized waveform measurement points as well as other features enabling easy lab bench usage.

A detailed description of the gate driver 1EDN7126G is available online [2] as well as the datasheet for the IGC033S10S1 [3].

Intended audience

This document is for power electronic engineers, technicians, and developers of power electronic systems who are interested in evaluating the performance of the 100 V CoolGaN™ power transistor IGC033S10S1 as well as the EiceDRIVER™ 1EDN7126G gate driver.

CoolGaN™

Infineon's CoolGaN™ solution offers unmatched quality that operate at higher switching speeds resulting in lower power losses, higher efficiency paving the way for smaller and lighter power supplies with the same power supplies with the same size but increased power capability.

CoolGaN™ target applications include:

- Consumer electronics
- Information and communication technologies
- Motor drives
- Robotics
- Energy Storage Systems
- Renewables

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1 Introduction

The EVAL_7126G_100V_GaNc Evaluation Board shown in Figure 1 is for general-purpose evaluation of the 100 V CoolGaN™ power transistor IGC033S10S1 in a PQFN package, along with the EiceDRIVER™ 1EDN7126G TDI gate driver. This board includes an optimized layout for a hard-switching half-bridge, as well as waveform measurement points and other useful features to enable easy lab bench characterization of these transistors and drivers. It is preconfigured as a buck or boost converter but can be easily reconfigured for a double-pulse test or any half-bridge topology with external connections.

Figure 1 EVAL_7126G_100V_GaNc Evaluation Board

1.1 EVAL_7126G_100V_GaNc Evaluation Board

The main parts of the EVAL_7126G_GaNc Evaluation Board are:

- CoolGaN™ power transistor IGC033S10S1 in a half-bridge configuration
- EiceDRIVER™ 1EDN7126G gate driver

It can be controlled by two PWM input signals directly. If only one PWM input signal is available, the second PWM signal can be generated using the on-board dead-time generation circuit. With the dead-time circuit, both dead-times can be set using on-board trimmers within a specified range.

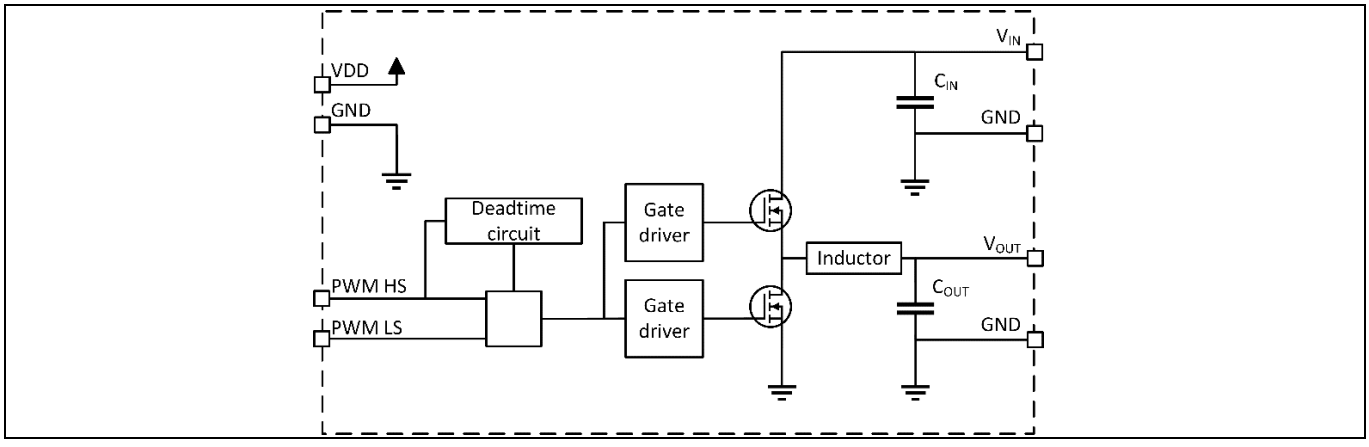


Figure 2 EVAL_7126G_100V_GaNc Evaluation Board

The board comes without a power inductor assembled but two large pads are available to solder any kind of power inductor. Input and output capacitors are assembled on-board providing enough capacitance for most of the operating conditions. A DC power supply and load can be connected to the four power connectors labeled as “V_{IN}”, “V_{OUT}”, and “GND”.

1.2 EVAL_7126G_100V_GaNc Evaluation Board specifications

Table 1 Recommended operating conditions

Parameter	Values			Unit	Note
	Min	Typ	Max		
V_{DD} supply voltage	4.5	5	5.5	V	–
V_{IN} to GND	–	–	80	V	–
V_{OUT} to GND	–	–	80	V	–
PWM voltage level	–	5	–	V	Rework needed for 3.3 V signals, see 4.1
DC input/output current	–	–	25	A	At 1 MHz and 48 V with bottom-side heatsink and 5 m/s airflow [1]

Table 2 Board characteristics

Parameter	Values			Unit	Note
	Min	Typ	Max		
V_{DD} supply current	–	20	–	mA	At 1 MHz switching frequency
V_{IN} to GND	–	–	100	V	Limited by capacitor ratings
V_{OUT} to GND	–	–	100	V	Limited by capacitor ratings
On-board deadtime adjustment range	7	–	100	ns	Limits depend on accuracy of trimmers
PWM pulse width	71	–	–	ns	Limited by gate driver

[1] The maximum DC current can be much higher at different switching frequencies and cooling conditions and is also limited by the saturation of the power inductor used.

1.3 Main board features

The EVAL_7126G_GaNc half-bridge evaluation board comes with additional features to support evaluation next to the half-bridge itself.

- The onboard deadtime generation circuit (mentioned in Section 1.1) can generate the second PWM control signal for the low-side gate driver when only one PWM signal is supplied to the board. Both dead-times between these two signals can be modified with the on-board trimmers. Rotating each trimmer clockwise will extend the respective deadtime within the specified range. The different options for PWM input can be selected with jumpers, as explained in Section 2.5
- A custom heatsink is provided for cooling the half-bridge. This can be mounted on either side of the board. Steps to assemble the heatsink are described in Section 2.6
- There are options to measure DC voltages V_{IN} and V_{OUT} directly or attenuated, as well as gate- and drain-to-source waveforms of both switches. For detailed descriptions for all voltage measurements, see Section 3
- An on-board temperature sensor, which is located close to the half-bridge. The sensor provides temperature information of the board, but not necessarily the device temperature. This can be used for a safety shutdown. If the specific component temperature is of interest, the use of a thermal infrared camera is recommended as explained in Section 3.3
- The main feature of the 1EDN7126G gate driver is that the high-side switch is supplied via the BST pin of the low-side driver. This prevents overcharging of the bootstrap capacitor and the resulting overvoltage on the high-side gate. This is important, because the maximum continuous gate voltage rating of the IGC033S10S1 is 5.5 V
- The board also offers the possibility to supply the bootstrap voltage directly from V_{DD}, by implementing the rework instructions in Section 4.3. For conventional bootstrapping from V_{DD}, a Zener diode is highly recommended to prevent the applied gate voltage from exceeding the maximum rating of the device

1.4 CoolGaN™ 100 V power transistor

The CoolGaN™ 100 V power transistor IGC033S10S1 comes in a PQFN package with very low inductance in the pH range, as well as dual-side cooling with an exposed thermal pad on the top-side of the transistor.

IGC033S10S1 can be operated at high switching frequencies and short deadtimes due to its fast switching transitions and low switching loss. This enables reducing the size of magnetics, capacitors, and heatsink in the application to improve power density and overall system efficiency.

Alternatively, IGB110S10S1 can also be assembled on the board as described in Section 4.5. IGB110S10S1 comes in a 3 mm x 3 mm PQFN package with exposed die for dual side cooling [4]. Both packages are shown in Figure 3.

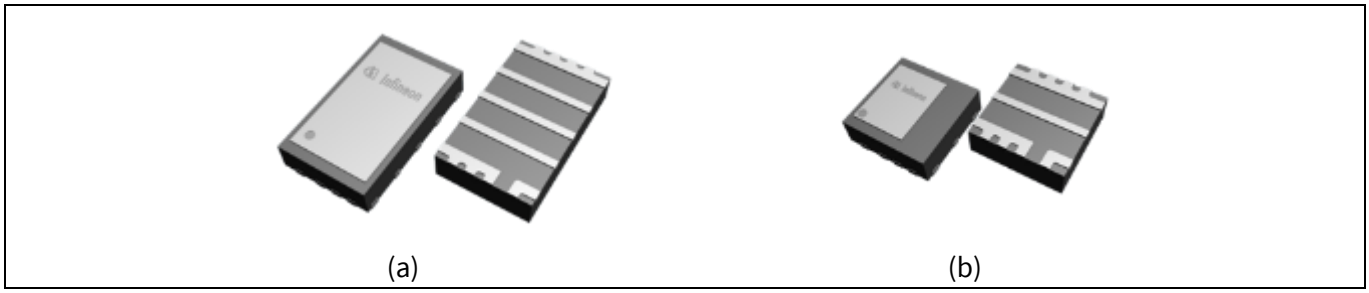


Figure 3 (a) CoolGaN™ 100 V power transistors IGC033S10S1; (b) GB110S10S1

1.5 EiceDRIVER™ 1EDN7126G gate driver

EiceDRIVER™ 1EDN7126G is an optimized gate-driver IC that is designed for driving CoolGaN™ power transistors. It features a truly differential input (TDI), active Miller clamp, bootstrap voltage clamp, and adjustable charge pump. TDI allows the gate driver output state to be controlled solely by the voltage difference between the two inputs. This is regardless of the driver's reference potential, as long as the common-mode voltage remains below 150 V (static) and 200 V (dynamic). This feature eliminates the risk of false triggering caused by ground bounce in low-side driving and enables 1EDN7126G to be used as a high-side driver.

The driver can be used with gate resistors (R_{GON} R_{GOFF})on the split source and sink outputs. However, on this board only a resistor in the output source path is used as a resistor in the output sink path is weakening the active Miller clamp feature of the driver. To change the driving strength and switching speed, the driver variant (R_{GON}) can be changed instead. In Section 5.3, example results are shown to demonstrate the influence of changing R_{GON} with the 1EDN7126G gate driver.

The board comes with two 1EDN7126G gate driver [1] assembled. These are a variant of the EiceDRIVER™ 1DEN71x6G family. It has four variants with different driving strengths available in the same package type and footprint. An overview of the important parameters for all variants is given in the following table.

Table 3 EiceDRIVER™ 1EDN71x6G family variants

Part number	Peak source/sink current	Input pulse blanking time	Typical propagation delay
1EDN7116G	2.0 A	20 ns	55 ns
1EDN7126G	1.5 A	40 ns	75 ns
1EDN7136G	1.0 A	60 ns	105 ns
1EDN7146G	0.5 A	80 ns	125 ns

EiceDRIVER™ 1EDN7126G gate driver has an integrated charge pump feature, which can optionally generate a negative off-state driving voltage. The negative voltage is adjustable to allow you to optimize the tradeoff between spurious turn-on risk and higher reverse conduction losses during dead-time.

The board’s default configuration has the charge pump disabled in each driver. To enable this feature, see Section 4.6. Example results for different gate off-state voltages are shown in Section 5.4.

2 Test setup description

The design and connections of the EVAL_7126G_100V_GaNc Evaluation Board can be used in different test setups. It can be operated in the following configurations:

- Buck converter test
- Boost converter test
- Buck-mode double pulse test
- Boost-mode double pulse test

Recommended test conditions:

- **Input and output voltage:** Maximum 60 V input and output voltage with the switching frequency in the range of 200 kHz to 1 MHz
- **Input/output current:** The maximum input/output currents are dependent on the thermal configuration and are in the range of 20 A to 30 A. However, as long as the voltage and temperature ratings of the board components are not violated, you can choose to exceed the voltage, frequency, and current at your own discretion

The following sections describe how to connect the board for each configuration.

2.1 Buck converter test setup

For performance characterization as well as waveform measurements.

Next to performance evaluation, this setup can be used to measure the gate and drain voltage waveforms of the low-side switch when soft-switching as a synchronous rectifier, as well as hard switching waveforms of the high-side switch. In this configuration, the board must be connected with one of the PWM input options as shown in Figure 4 and described in Section 2.5.

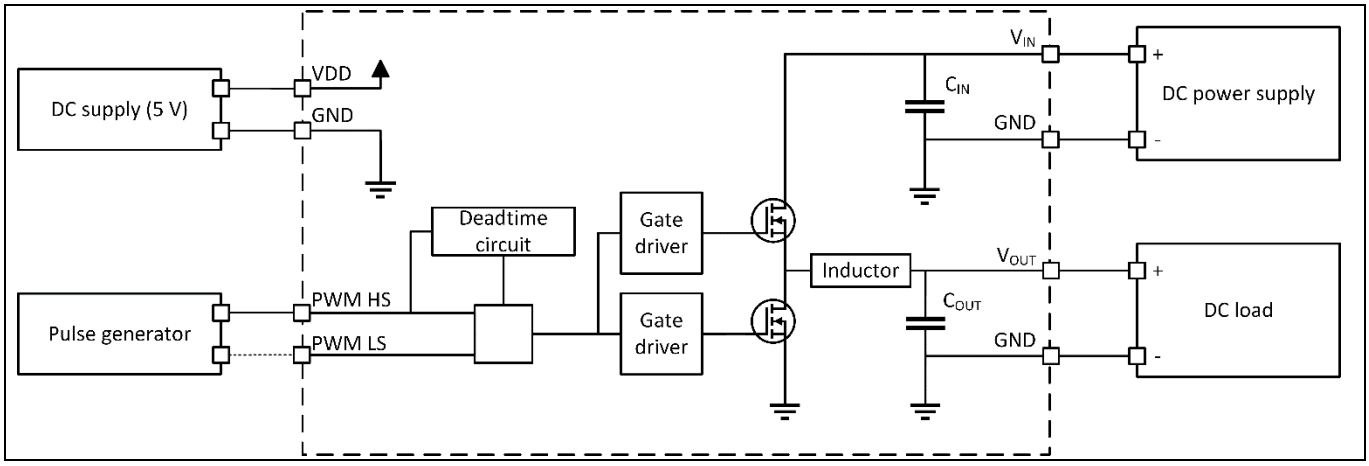


Figure 4 Block diagram of buck converter test setup

2.2 Boost converter test setup

For performance characterization as well as waveform measurements.

Next to performance evaluation, this setup can be used to measure the gate and drain voltage waveforms of the low-side switch when hard-switching, as well as the high-side waveforms when soft switching.

To set up the board as a boost converter, the connections for V_{IN} and V_{OUT} must be reversed with a voltage supply on V_{OUT} and a DC load on V_{IN} as shown in Figure 5.

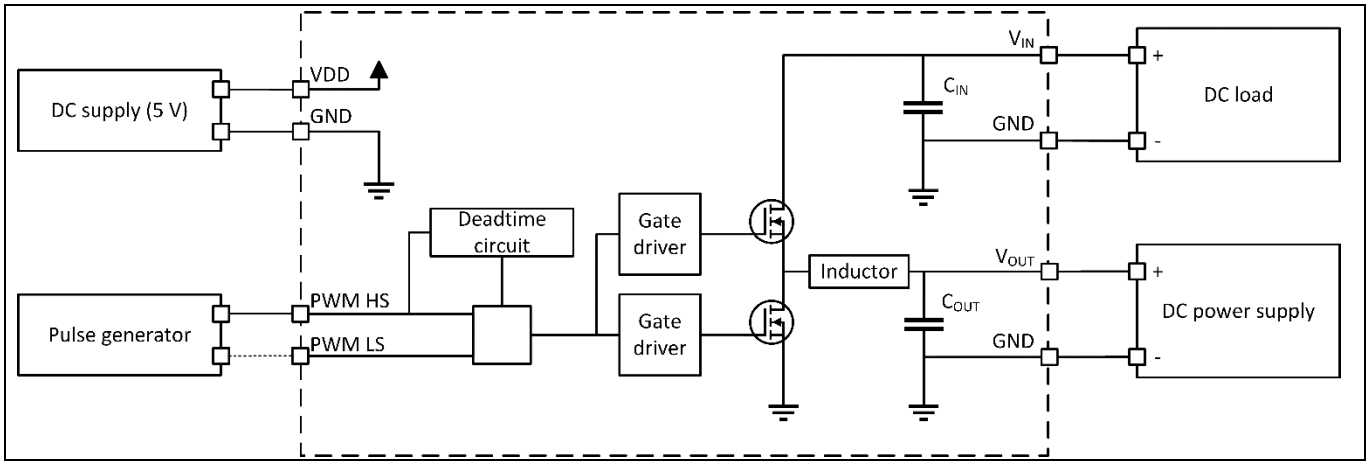


Figure 5 Block diagram of boost converter test setup

2.3 Buck-mode double pulse test setup

For capturing soft-switching voltage waveforms without self-heating effects.

Two different types of double pulse tests can be performed, buck-mode and boost-mode. For both modes the inductor should have a high inductance value, typically in the range of 10 µH to 100 µH, often routed off-board with cables to allow inductor current measurement using a split-core current probe.

V_{OUT} should be connected to GND and a DC power supply connected to V_{IN} as shown in Figure 6.

The high-side PWM is sent two pulses:

- One long pulse to raise the inductor current to the desired level
- One short pulse to view the turn-on and turn-off transitions, see [9] and [10]

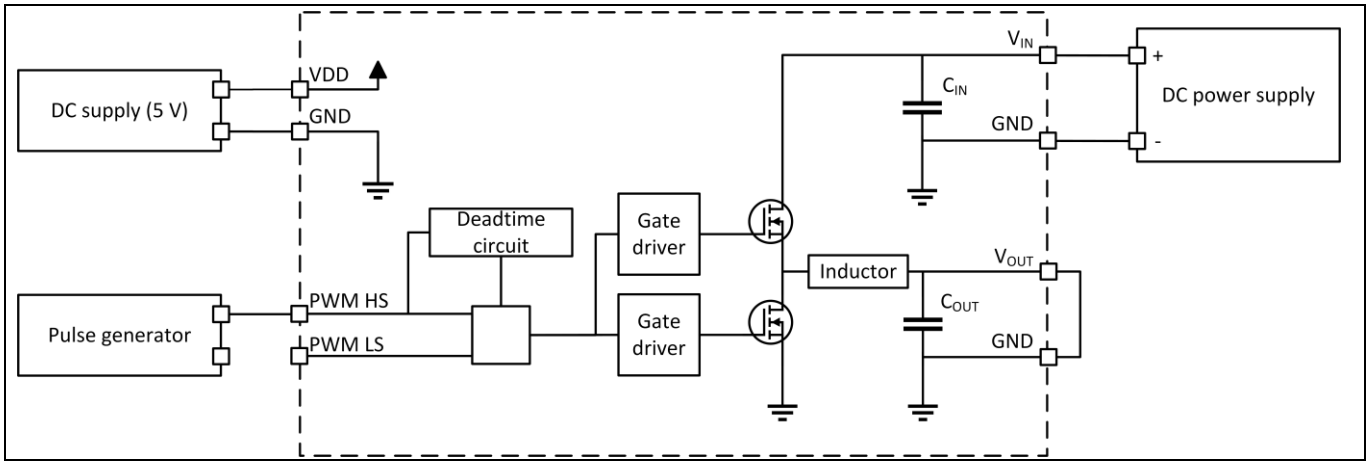


Figure 6 Block diagram buck-mode double pulse test setup

Typically, the low-side PWM input should be manually set to 0 V for safety during this test. This can be implemented on jumper J3 as shown in Figure 9. As the high-side gate driver is by default supplied via bootstrapping from the low-side driver, it is mandatory to change the bootstrapping for this setup to come from V_{DD} directly as explained in Section 4.3.

2.4 Boost-mode double pulse test setup

For capturing hard-switching voltage waveforms without self-heating effects.

The V_{IN} to V_{OUT} connectors should be shorted together, with one DC voltage supply controlling both voltage nodes as shown in Figure 7.

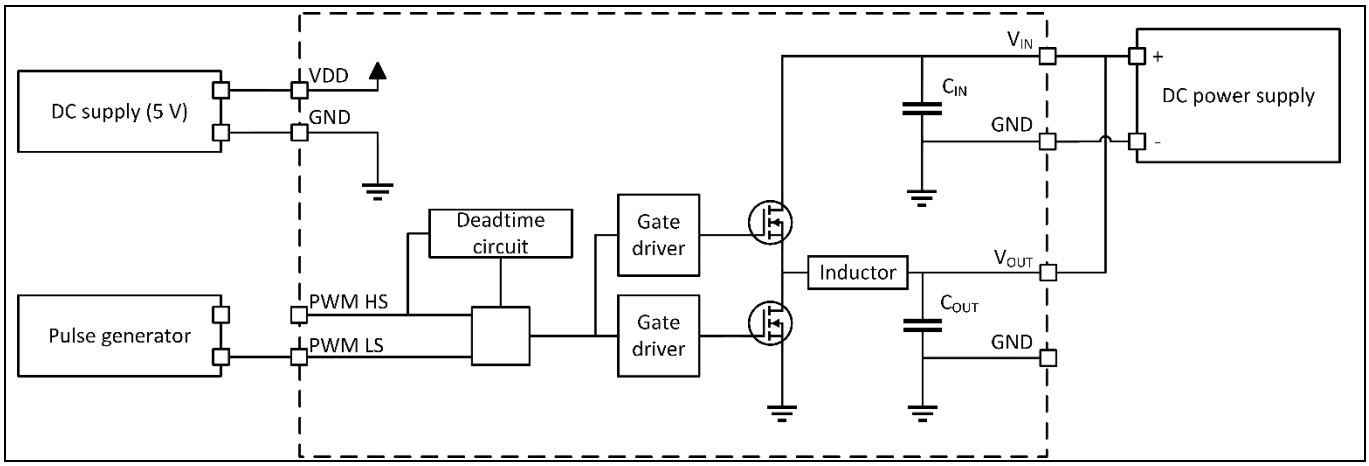


Figure 7 Block diagram boost converter double pulse test setup

For boost-mode double pulse testing, the low-side PWM is sent two pulses:

- One long pulse to raise the inductor current to the desired level
- One short pulse to view the turn-on and turn-off transitions

The high-side PWM can be switched complementary to the low-side but this is typically not necessary in a double pulse test. In this case, the high-side PWM input should be manually set to 0 V for safety during this test. This can also be done on jumper J3 as shown in Figure 9.

2.5 PWM input options

There are different options for the PWM signals to control the half-bridge:

- Dual 5 V logic inputs with 50 Ω terminated SMA
- Dual 3.3 V logic inputs with 50 Ω terminated SMA (rework needed per Section 4.1)
- Dual 5 V logic inputs with high-Z terminated 3-pin header
- Dual 3.3 V logic inputs with high-Z terminated 3-pin header (rework needed per Section 4.1)
- Single high-side 5 V logic input with 50 Ω terminated SMA, using on-board deadtime generator

When using a two-channel benchtop function/waveform generator to supply both high-side and low-side PWM signals, connect them via the two SMA connectors “PWM HS” and “PWM LS”. Each SMA input is terminated with 50 Ω and the function generator must be configured to drive a 50 Ω load. In the default configuration of the board, all logic signals must be based on 5 V, not 3.3 V. To configure the board for 3.3 V logic, the TDI resistors must be reworked as per the instructions in Section 4.1.

A single high-side PWM signal can be connected from a waveform generator, with 5 V logic and 50 Ω terminated SMA. In this configuration, both PWM signals are generated using the on-board dead-time generation circuit with dead-time determined by trimmer resistors (R5 and R6). The outputs of this dead-time generating circuit are complementary 5 V logic signals. The maximum dead-time achievable with this circuit is approximately 100 ns per edge, but it is recommended to start with a value close to 10 ns per edge.

The third option is to supply dual PWM signals directly to the header J1, but with a high-Z termination rather than 50 Ω. The function generator or other signal source must be configured to drive a high impedance load, rather than 50 Ω.

Figure 8 demonstrates how to set the jumpers or connect to a high-Z source on connector J1.

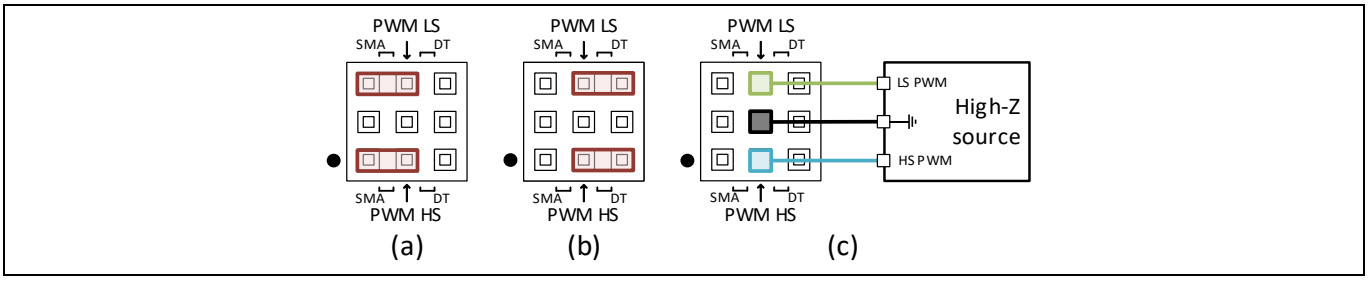


Figure 8 (a) Jumper J1 settings for dual 50 Ω logic inputs; (b) single high-side 5 V logic input; (c) dual 5 V high-Z terminated logic inputs

The dead-time can only be adjusted with the trimmers on-board if the jumpers are set according to Figure 8 (b). For the other options, the deadtime is defined by the dual PWM signals.

To perform double pulse tests, the jumper settings for buck-mode and boost-mode should be set as shown in Figure 9.

- For buck-mode, the low-side PWM channel is tied to GND, and pulses are sent only to the high-side PWM channel
- For boost-mode, the high-side PWM channel is tied to GND and the low-side PWM channel input is used to control the pulses

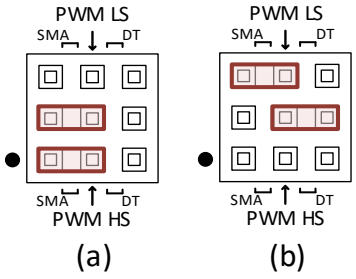


Figure 9 (a) Double pulse test jumper settings for buck-mode; (b) boost-mode

2.6 Heatsink attachment options

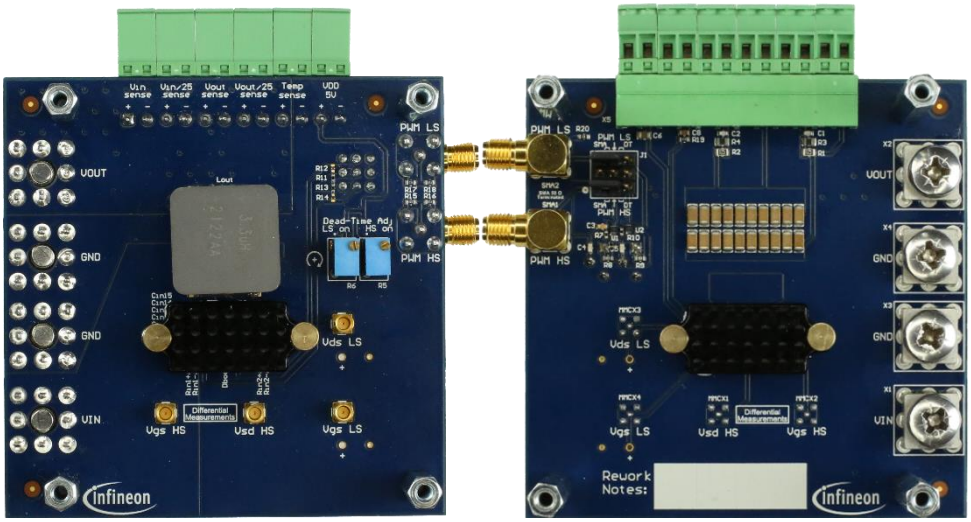
The provided heatsink comes with a preinstalled thermal interface material (TIM) pad of T-Global TG-A1780, which is an ultra-soft galvanically-isolated TIM pad with a thermal conductivity of 17.8 W/Mk and a thickness of 0.5 mm. Recommended TIM pads from T-Global include TG-A1780, TG-A1660, TG-A1450, TG-A1250, depending on the preference for cost vs. performance.

The heatsink can be installed on the bottom-side of the PCB for cooling or on top of the transistors for dual-sided cooling, as shown in Figure 10.

Install the heatsink

1. Remove the plastic protective tape from the TIM pad
2. Position the heatsink in the desired location
3. Press down on both the spring pins at the same time

Note: Use two flathead (slotted) screwdrivers or similar tools to avoid finger injuries on the pin fins as shown in Figure 11.



(a) (b)

Figure 10 (a) Heatsink attachment top-side; (b) bottom-side

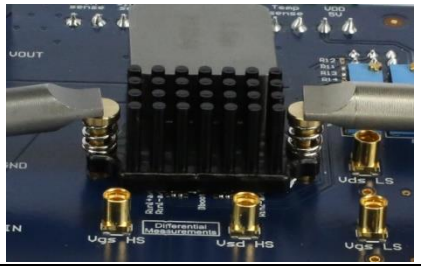
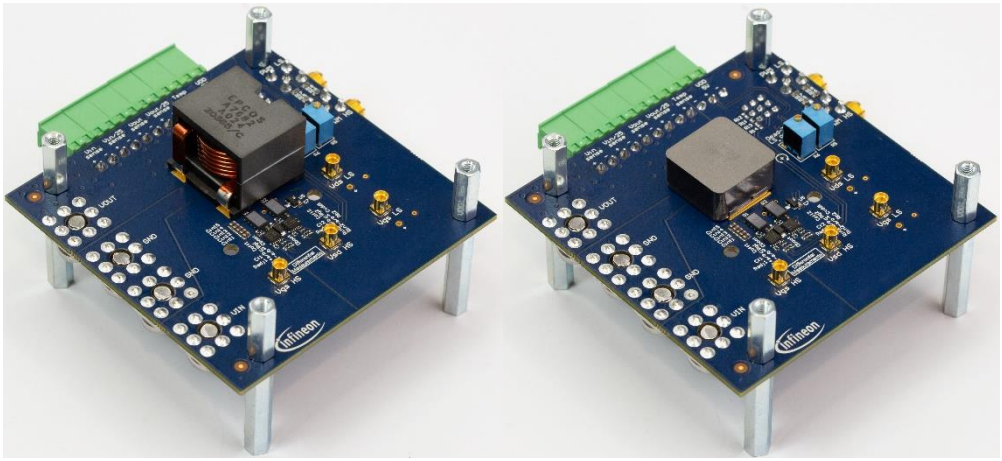


Figure 11 Heatsink attachment with two flathead screwdrivers to compress spring pins

2.7 Inductor mounting

Figure 12 shows two different inductors soldered to the board. A 10 µH inductor from TDK ERU series (a) and a 3.3 µH inductor from Vishay's IHLP7575-JZ series (b).



(a) (b)

Figure 12 (a) Mounted inductors – TDK ERU series; (b) Vishay IHLP7575-JZ series

3 Measurement options

3.1 DC voltage measurements

The board is equipped with screw terminal plugs for DC measurements. Input and output voltage can be measured with or without 25x attenuation, making it compatible with a digital multimeter or datalogger for efficiency measurements, or for inputs to an external controller.

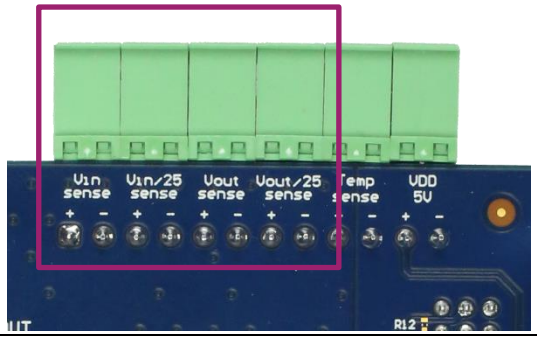


Figure 13 Screw terminal plugs for DC voltage measurement

3.2 Waveform measurements

The board offers multiple points to capture the device switching waveforms, as shown in Figure 14.

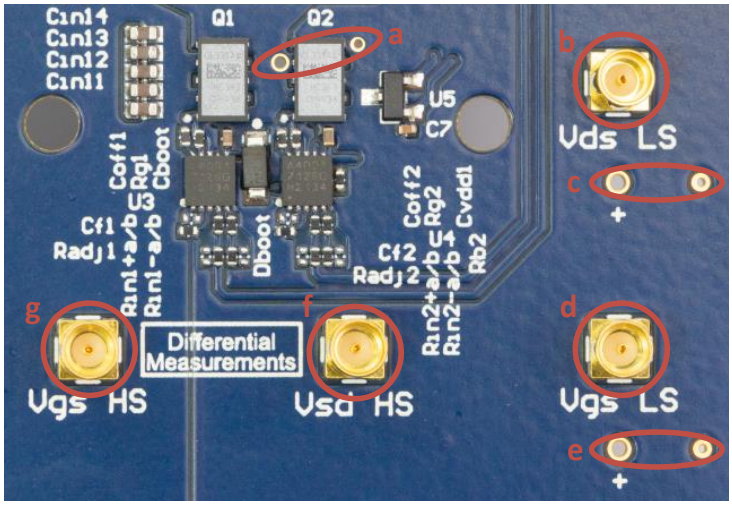


Figure 14 Device waveform measurements points

a) V_{DS} LS near device
b) V_{DS} LS MMCX
c) V_{DS} LS far
d) V_{GS} LS MMCX
e) V_{GS} LS far
f) V_{SD} HS MMCX
g) V_{GS} HS MMCX

The drain-to-source voltage of the low-side device (V_{DS} LS) can be measured at three different points, once with an MMCX tip and two times at vias with a spring clips probe vias. One spring clip via is near the device (a) and the other is further away (c), next to the MMCX connector (b).

The low-side gate-to-source voltage (V_{GS} LS) can be measured with an MMCX tip (d) and a spring clip probe at vias (e) next to the MMCX connector.

The high-side device source-to-drain voltage (V_{SD} HS) and gate-to-source voltage (V_{GS} HS) can be measured with a differential probe with MMCX tips, (f) and (g), respectively.

Low-side single-ended voltage measurements

Any passive probe can be used to measure low-side voltage waveforms for CoolGaN™ power transistors, but they should have suitable bandwidth and connectivity. The recommended bandwidth for all voltage probes and oscilloscopes is minimum 1 GHz. The loop between the probe tip and the measurement points (both + and – sides) should be within 10 mm, preferably shorter.

For example, the recommended probing solution is Tektronix TPP1000 [5] with an MMCX tip adaptor 206-0663-xx, which guarantees the tightest possible probing loop for this tip as shown in Figure 15. Alternatively, you can use the MMCX-A1025 probe from PMK [8] instead of the passive MMCX probe. Optionally, a spring clip probe tip solution can be employed at the provided vias, but this degrades the measurement fidelity to some degree.

The $V_{DS\,LS}$ waveform can be measured at three locations on the board: MMCX connector, two vias beside the MMCX connector (c), or two vias located close to the low-side switch (a). $V_{GS\,LS}$ can be measured at the MMCX connector or at the vias beside it.

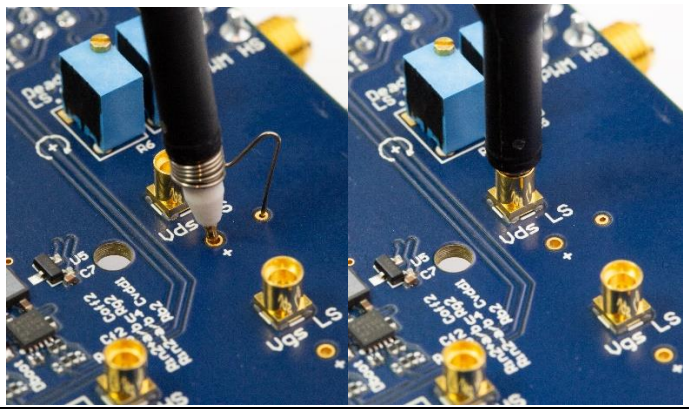


Figure 15 Low-side single ended voltage measurements options

High-side differential voltage measurements

In general, high-side voltage waveforms are challenging for a GaN-based half-bridge circuit, due to the extremely high dv/dt and di/dt involved. The most accurate measurement scheme comes from an extremely high-bandwidth optically isolated probing system, for example the IsoVu probe system from Tektronix [6] or the FireFly series from PMK [7].

Figure 16 High-side differential voltage measurements with high-bandwidth differential probes

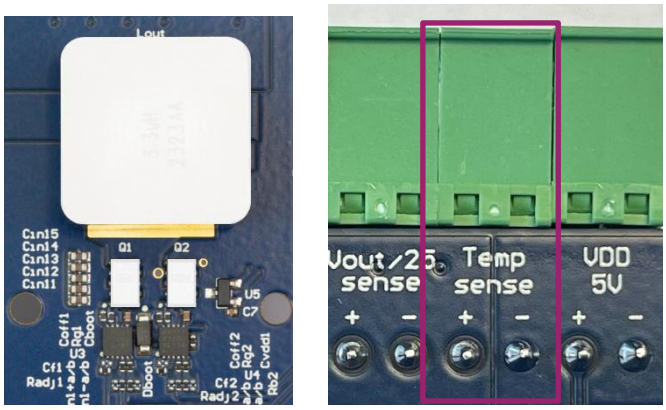
The high-side drain measurement connector is configured for V_{SD} rather than V_{DS} because a measurement with a stable DC reference point typically results in more accurate measurements. However, most oscilloscopes allow for convenient inverting of measurement channels to translate V_{SD} into V_{DS}.

In addition to the bandwidth of the probing system, the probing loop connectivity is critical. An MMCX tip adapter for high-side differential measurements is very important for an accurate measurement with the highest fidelity and the lowest signal degradation.

3.3 Temperature measurements

The board is equipped with an on-board PCB temperature sensor but it is recommended to use a contacting thermocouple solution or an infrared thermal camera to capture the temperature of the CoolGaN™ power transistor, as well as the power inductor.

When using a thermal camera, it is highly recommended to paint all target surfaces with a matte-finish paint (white or black is commonly used) to ensure the consistency of the emissivity for all temperature measurements. Reflections that can distort the temperature captured by a camera can also be avoided [1].



(a) (b)

Figure 17 (a) Exemplary painted surfaces for temperature measurement with a thermal infrared camera; (b) screw terminal plug connection to sense the output of the on-board temperature sensor

4 Rework options

4.1 TDI resistor adjustment for 3.3 V PWM input

The EiceDRIVER™ 1EDN7126G gate driver utilizes a TDI circuit for common-mode voltage rejection as an alternative to level-shifting or galvanic isolation. Input resistor values must be selected based on the logic voltage level of the PWM inputs, e.g., 5 V or 3.3 V. The default configuration of the board has a TDI resistance of 28 kΩ + 47 kΩ = 75 kΩ, which is required for a 5 V logic input.

To use the dual 3.3 V logic inputs, e.g., from an external control board, the input resistance must be reduced from 75 kΩ to 47 kΩ. To enable 3.3 V logic inputs, solder 0 Ω resistors or solder bridge the four empty 0402 footprints in parallel with the 28 kΩ resistors, leaving only the 47 kΩ un-bypassed, as shown in Figure 18.

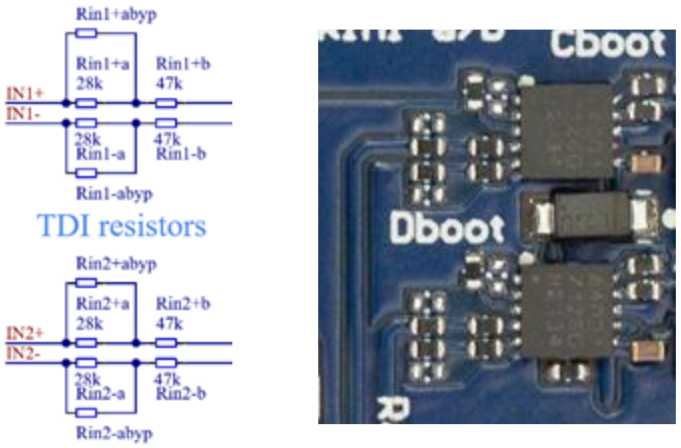


Figure 18 Rework option for 3.3 V input PWM signals

4.2 Cross-connected PWM inputs for overlap protection

By default, the input PWM signals can be overlapped to achieve very short dead-times. However, overlap protection can be enabled by cross-connecting the IN+ and IN- signals between the EiceDRIVER™ 1EDN7126G gate drivers. To implement this feature, the two 0 Ω resistors (R11 and R13) must be removed and instead soldered in positions R12 and R14, as shown in Figure 19. With this, the shortest achievable effective dead-time may be slightly higher.

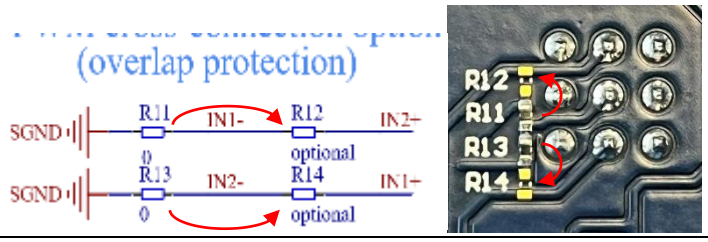


Figure 19 Rework option for overlap protection of the PWM input signals

4.3 Conventional bootstrapping direct from V_{DD} with Zener regulation

The EiceDRIVER™ 1EDN7126G gate driver provides a useful feature to avoid overcharging the bootstrap capacitor by connecting the bootstrap diode to the BST pin of the low-side gate driver instead of directly feeding it from V_{DD}.

However, you can also use conventional bootstrapping. To change bootstrapping schemes, remove resistor R_{b2} and populate R_{b1} with a value in the range of 1 Ω to 4.7 Ω.

In such a configuration, it is recommended to populate position Dz with a 5.1 V~5.6 V Zener diode in an SOD523 package, e.g., BZT585B5V6T-7. It may be more difficult to install a bottom-side heatsink with Rb2 and Dz installed.

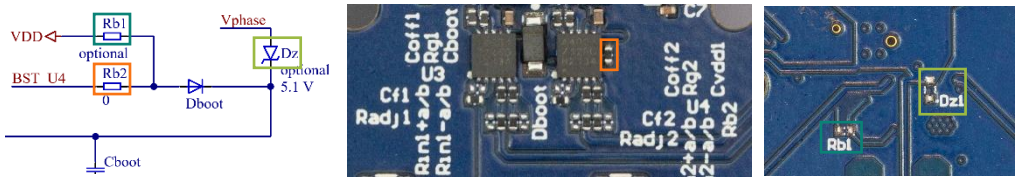


Figure 20 Rework instructions for conventional bootstrapping from V_{DD}

4.4 Split ground option

SGND and PGND are the two different grounds that exist on the board, as shown in the schematic in Figure 36. By default, both grounds are connected together with the resistor (R20). This is needed for the dead-time generation circuit to work properly. If the dead-time circuit is not used, R20 can be removed to isolate the external PWM generator's reference from PGND.

4.5 Changing the CoolGaN™ power transistor

The evaluation board comes with CoolGaN™ power transistor IGC033S10S1 in a 3 mm x 5 mm PQFN package assembled. Alternatively, the IGB110S10S1 transistor can also be assembled on the board. The transistor's 3x3 mm PQFN package can be soldered on the 3x5 mm PQFN footprint as shown in Figure 21.

Figure 21 Reworked board with IGB110S10S1 assembled instead of IGC033S10S1

4.6 Enable charge pump to generate negative V_{GS} for off-state driving

The EiceDRIVER™ 1EDN7126G has an integrated charge pump feature, which can optionally generate a negative off-state driving voltage. The negative voltage is adjustable to allow you to optimize the tradeoff between spurious turn-on risk and higher reverse conduction losses during dead-time. The board's default configuration has the charge pump disabled in each driver, which means the capacitor positions (Cf1 and Cf2) are empty, positions (Coff1 and Coff2) are populated with 0 Ω resistors and the resistors (Radj1 and Radj2) are shorting the driver pin to GND with 0 Ω resistors.

To enable the charge pump, it is recommended to populate Cf1 and/or Cf2 with a 100 nF capacitor. Likewise, Coff1 and/or Coff2 can be populated with a capacitor in the range of 0.47~1 µF.

The voltage V_{OFF} generated by the charge pump is configured at power-up of the board, based on the resistor value populated on Radj1 and/or Radj2 positions as shown in Table 4.

See the location of the components in the schematic and the board itself in Figure 22.

Table 4 EiceDRIVER™ 1DEN71x6G resistance values for negative off-state voltage

Radj1/Radj2	Unit	Negative voltage V_{OFF}	Unit
< 0.75	kΩ	Disabled	–
1.5	kΩ	-0.5	V
3.3	kΩ	-1	V
6.8	kΩ	-1.5	V
15	kΩ	-2	V
33	kΩ	-2.5	V
68	kΩ	-3	V

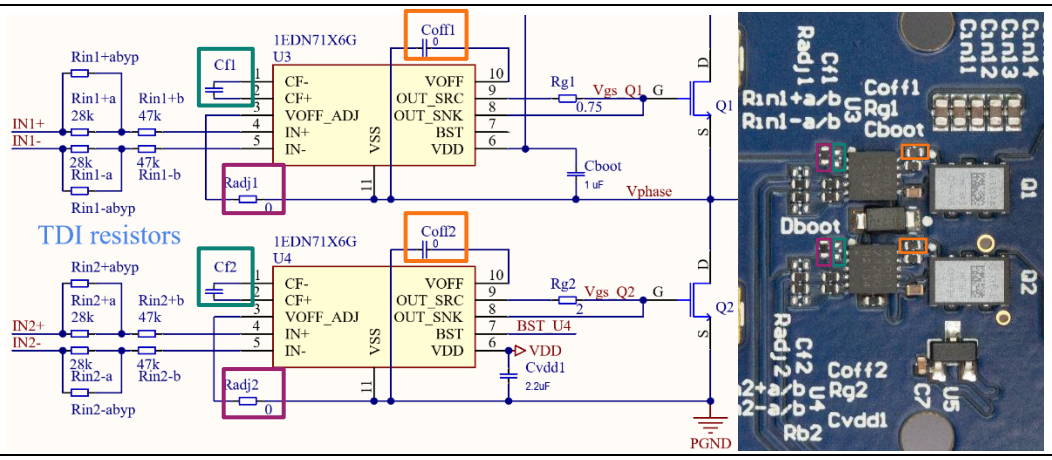


Figure 22 Rework instructions to enable charge pump feature in order to generate negative V_{GS} for off-state gate driving

5 Example experimental results

In this Section, the results shown have been measured with this board in different operating modes. Results are shown for buck-mode operation, including example waveforms. To show the influence of changing the gate resistance or gate off-state voltage, efficiency results, and waveforms are shown in Sections 5.3 and 5.4, respectively. Finally, example thermal images are shown in 5.5.

5.1 Example experimental efficiency and power loss

The efficiency and power loss are determined by measuring the input and output voltage at the measurement connector, the input and output current between the board and the source/load, and the supply voltage and current of the auxiliary VDD, then calculated as follows:

$$P_{LOSS} = V_{IN} \cdot I_{IN} - V_{OUT} \cdot I_{OUT} + V_{DD} \cdot I_{DD}$$

Equation 1

$$\eta = \frac{V_{OUT} \cdot I_{OUT}}{(V_{IN} \cdot I_{IN}) + (V_{DD} \cdot I_{DD})}$$

Equation 2

The efficiency and power loss results are shown for the board operating in buck-mode with an input voltage of 48 V, an output voltage of 12 V, at two different switching frequencies of 500 kHz and 1 MHz, and with three different cooling conditions.

First, the test was run without any heatsink attached or forced airflow, then with the heatsink attached to the bottom side of the board with an airflow of 5 m/s. Figure 23 and Figure 24 show the results for a 3.3 µH inductor mounted on the board.

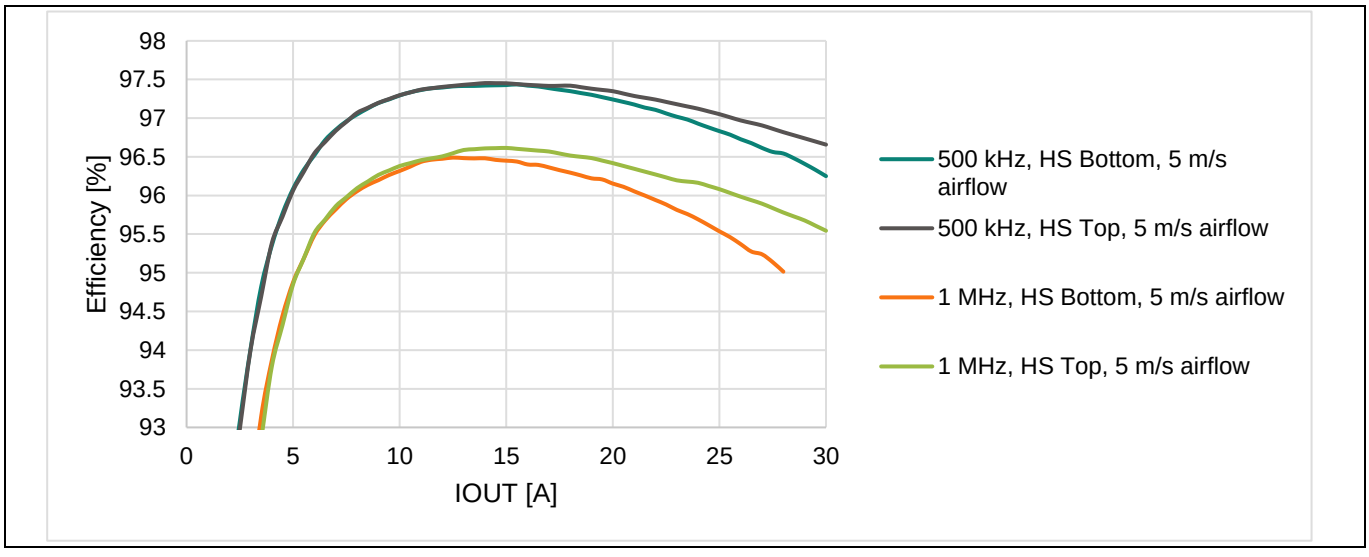


Figure 23 Example efficiency results, buck-mode 48 V to 12 V with 3.3 µH inductor, different cooling conditions and switching frequencies

Efficiency results are better for 500 kHz switching frequency because of the lower switching loss. However, the results at 1 MHz still show very good performance due to the very low Q_{OSS} of IGC033S10S1 compared to the conventional MOSFETs.

The influence of different cooling conditions is clearly visible. The best results can be achieved with the heatsink attached on top because the IGC033S10S1 is a dual-side cooling package and the heat flow is the best to the top-side of the package with its large, exposed die area.
With the heatsink attached on bottom, the losses increase at higher currents compared to the top-side heatsink results because of the superior thermal performance of dual-side cooling.

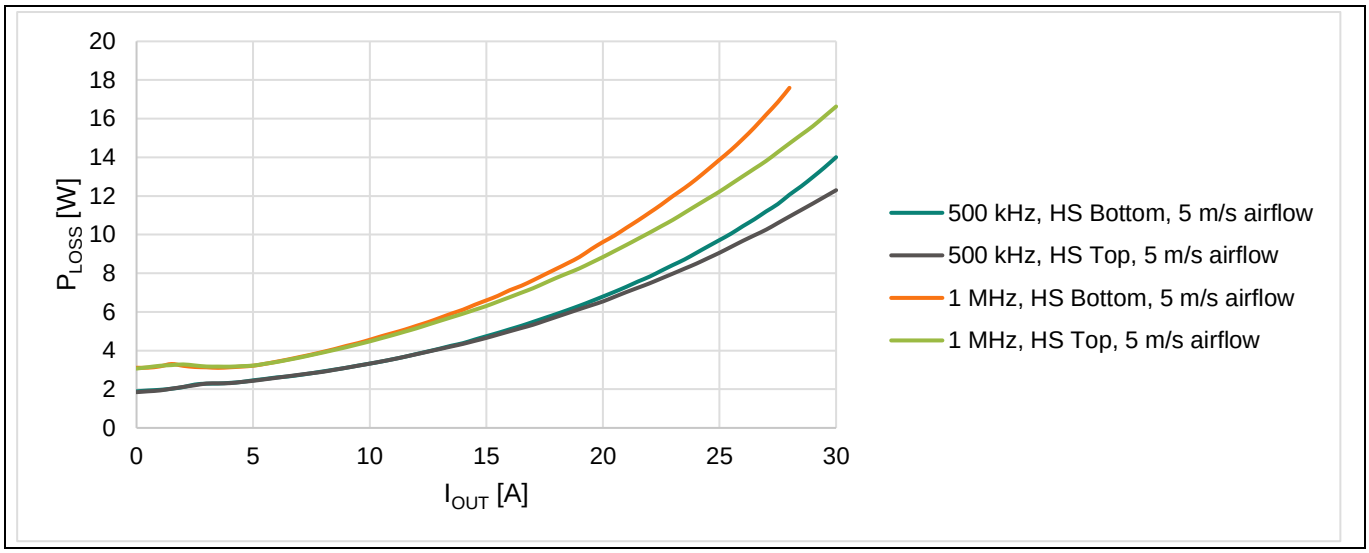


Figure 24 Example overall power loss, buck-mode 48 V to 12 V with 3.3 µH inductor, different cooling conditions and switching frequencies

There is no data for some conditions at higher currents because the devices have reached a temperature of 120°C. This is only due to the selected cooling condition, which does not represent any specific application and can always be improved with a different heatsink and/or airflow.

5.2 Example buck-mode waveforms

The board was set up to be used in buck-mode as described in Section 2.1. Waveforms at the mentioned points are shown in Figure 25 and Figure 26 for the turn-off of the high-side device. The results for the turn-on of the high-side device are shown in Figure 25. For the high-side device turn-off waveforms are shown in Figure 26. Operating conditions of the board in buck-mode are 48 V input voltage, 12 V output voltage, 20 A output current, a 3.3 µH power inductor, heatsink attached on bottom-side of the board, and an airflow of 5 m/s.

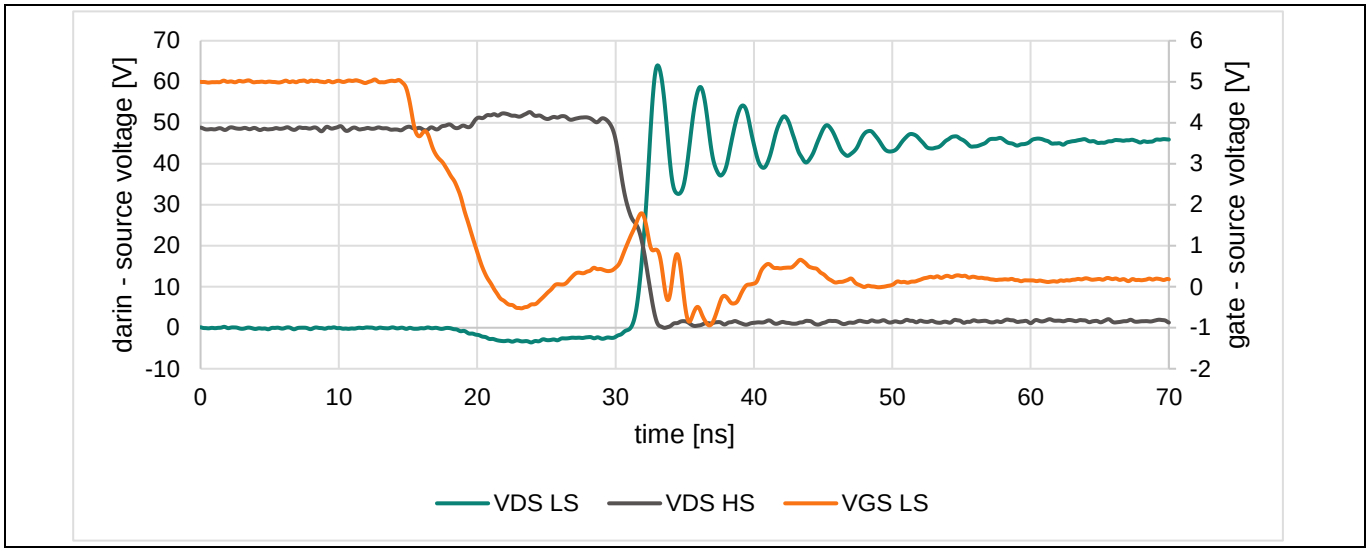


Figure 25 **Example waveforms during high-side turn-on transition in buck-mode 48 V to 12 V, 500 kHz at 20 A I_{OUT} with 3.3 µH inductor**

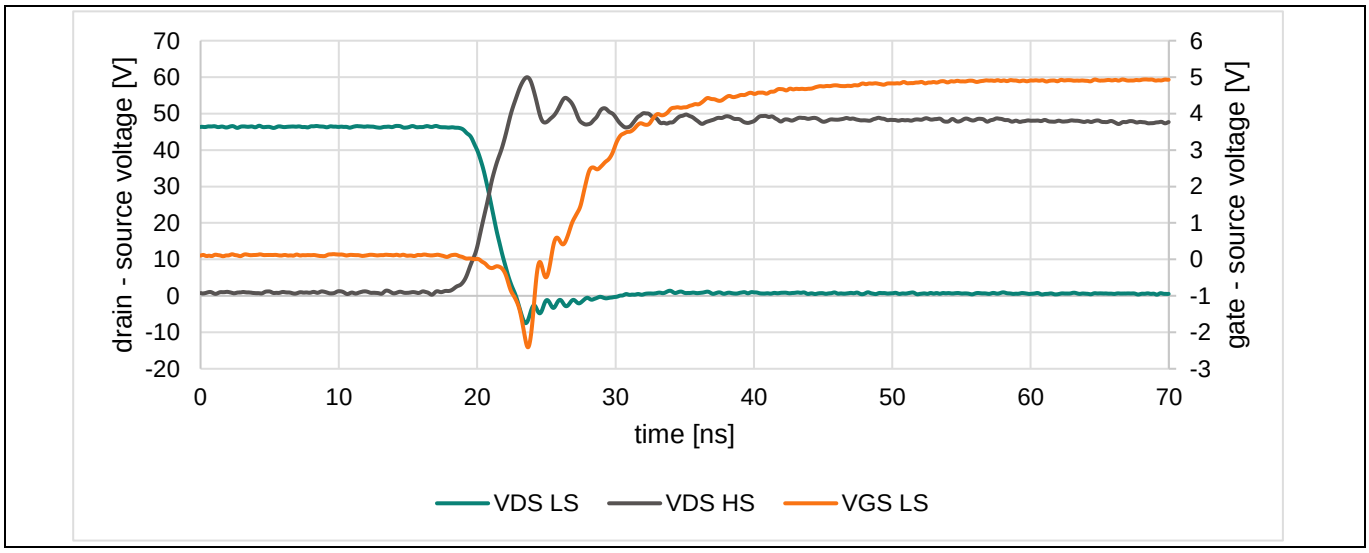


Figure 26 **Example waveforms during high-side turn-off transition in buck-mode 48 V to 12 V, 500 kHz at 20 A I_{OUT} with 3.3 µH inductor**

5.3 Example results for different high-side gate resistor values

As described in Section 1.5, the board includes gate resistors in the source gate path. To demonstrate the difference between various gate resistor values in combination with 1EDN7126G, the board was tested with different high-side gate resistor values at the same conditions for comparison: buck-mode with 48 V input voltage, 12 V output voltage, 500 kHz switching frequency, a 3.3 µH inductor, heatsink attached on the bottom side of the board, and an airflow of 5 m/s.

Since the low-side drain voltage overshoot is mostly affected by the different high-side gate resistor values, only these waveforms are shown in Figure 27. As expected, the lower the gate resistance, the higher the overshoot of the drain voltage. Comparing the highest and the lowest gate resistance chosen the difference of switching speed is significant.

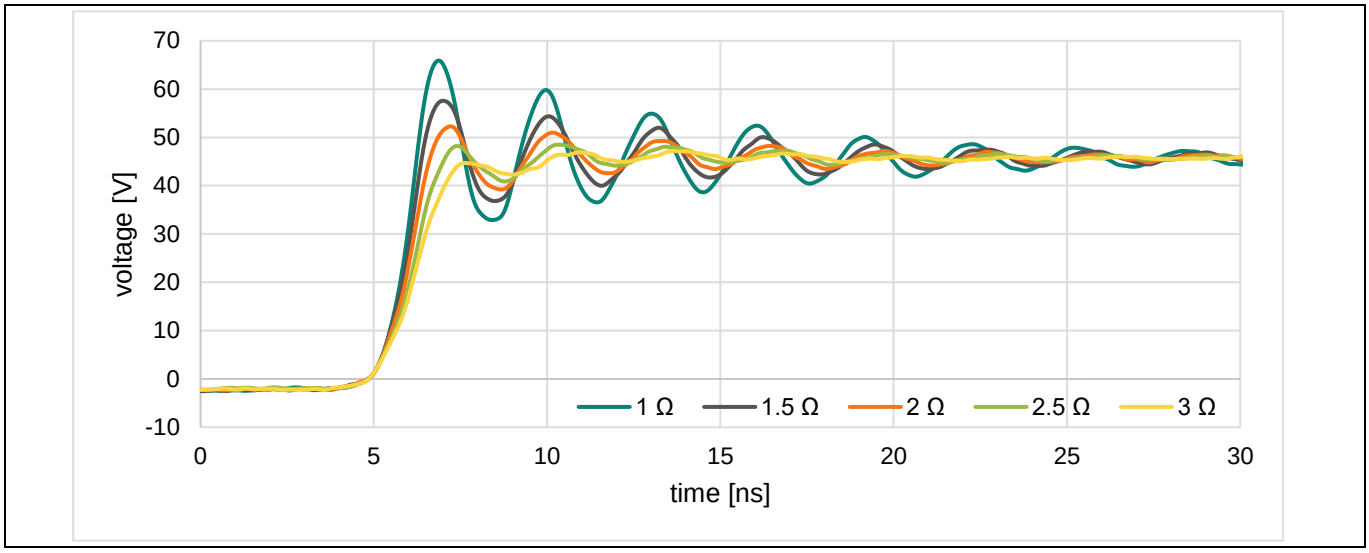


Figure 27 **Example V_{DS} LS waveform in buck-mode 48 V to 12 V, 500 kHz at 20 A I_{OUT} for different high-side gate resistor values with 1EDN7126G**

When looking at efficiency and power loss results in Figure 28 and Figure 29, the decrease of overall efficiency with a higher high-side gate resistance is seen. The results also show that there is no significant benefit in terms of losses and efficiency between 1 Ω and 1.5 Ω high-side gate resistance in this example. With the largest high-side gate resistor value, a much lower efficiency is achieved because of higher switching losses. However, there may be applications requiring this slower switching transition to reduce overshoots and meet EMI/EMC requirements.

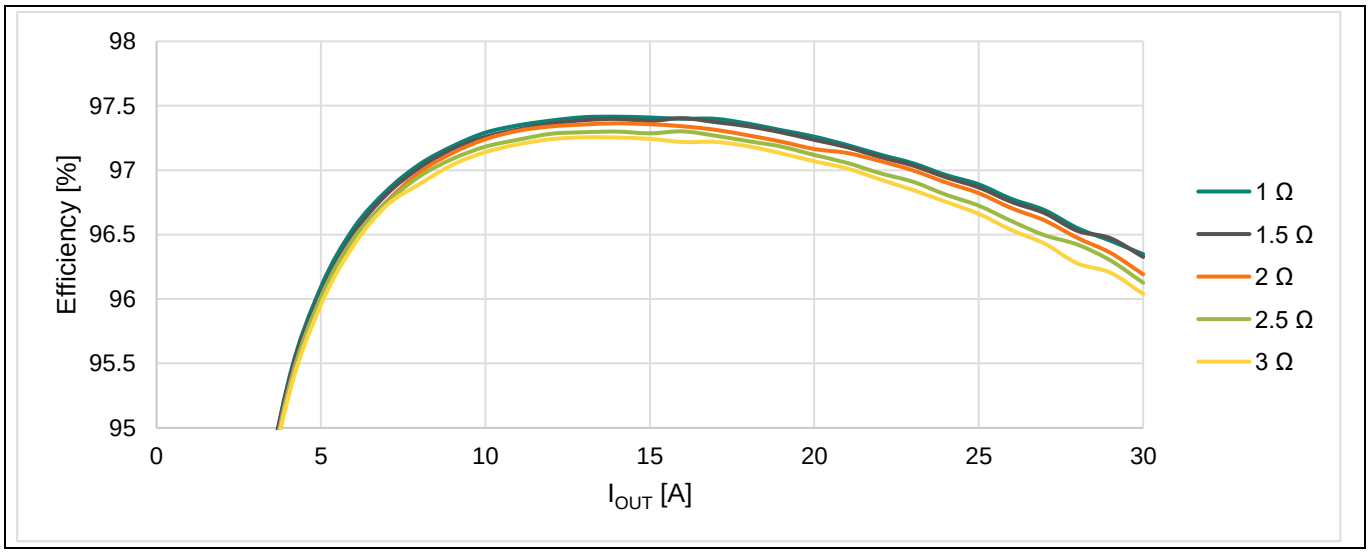


Figure 28 **Buck-mode 48 V to 12 V, 500 kHz example efficiency results for different high-side gate resistor values with 1EDN7126G**

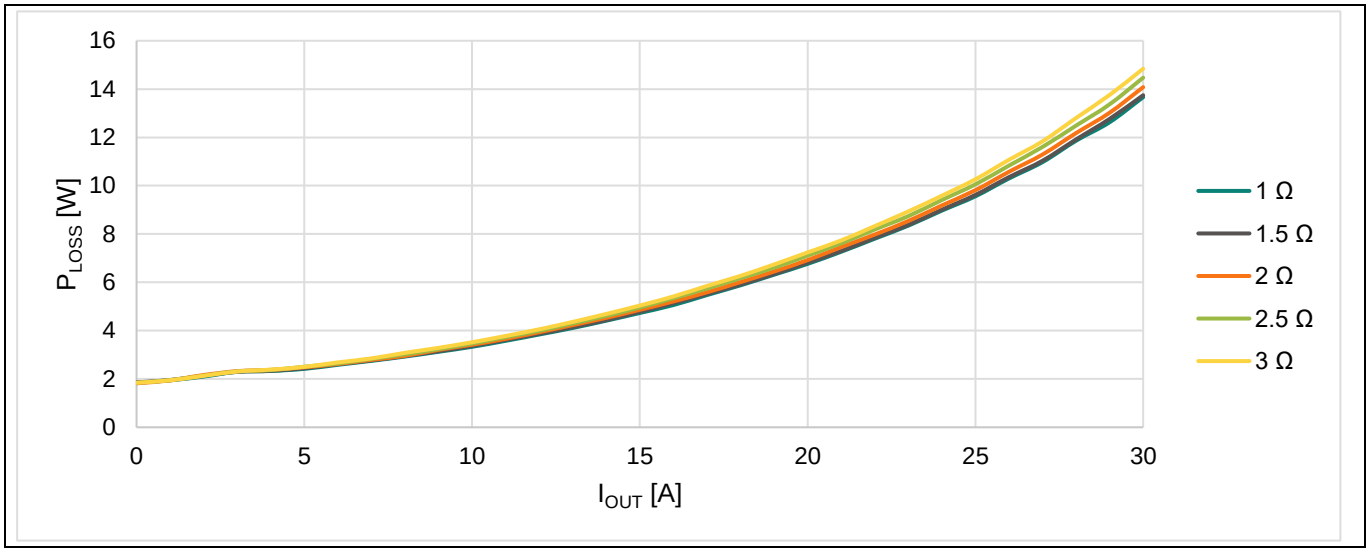


Figure 29 Buck-mode 48 V to 12 V, 500 kHz example overall power loss results for different high-side gate resistor values with 1EDN7126G

5.4 Example results for different gate drive off-state voltages

1EDN7126G comes with a charge pump feature as already described in Section 4.6. The negative voltage is adjustable to allow you to optimize the tradeoff between spurious turn-on risk and higher reverse conduction losses during dead-time. Therefore, the example results shown are for four off-state gate voltage conditions:

- Charge pump disabled – V_{OFF} = 0 V
- Charge pump enabled with:
  - R_{ADJ} = 1.5 kΩ resulting in V_{OFF} ≈ -0.5 V
  - R_{ADJ} = 3.3 kΩ resulting in V_{OFF} ≈ -1 V
  - R_{ADJ} = 6.8 kΩ resulting in V_{OFF} ≈ -1.5 V

As in Section 5.3, the board is operated with the same conditions for comparison: buck-mode with 48 V input voltage, 12 V output voltage, 500 kHz switching frequency, a 3.3 µH inductor, heatsink attached on the bottom side of the board, and an airflow of 5 m/s. The used gate resistor values are the default ones. The resulting example low-side voltage waveforms are shown in Figure 30.

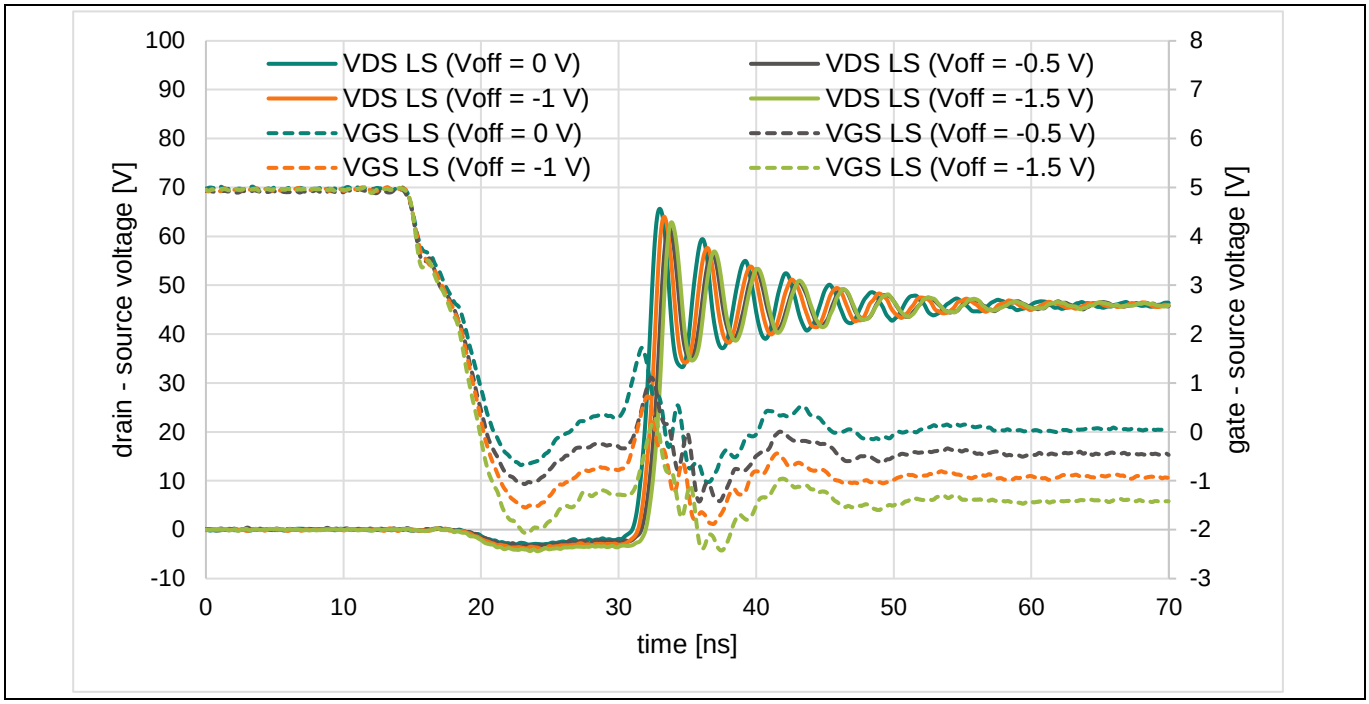


Figure 30 **Buck-mode 48 V to 12 V, 500 kHz example V_{DS} LS waveform at 20 A I_{OUT} for different off-state gate voltages with 1EDN7126G**

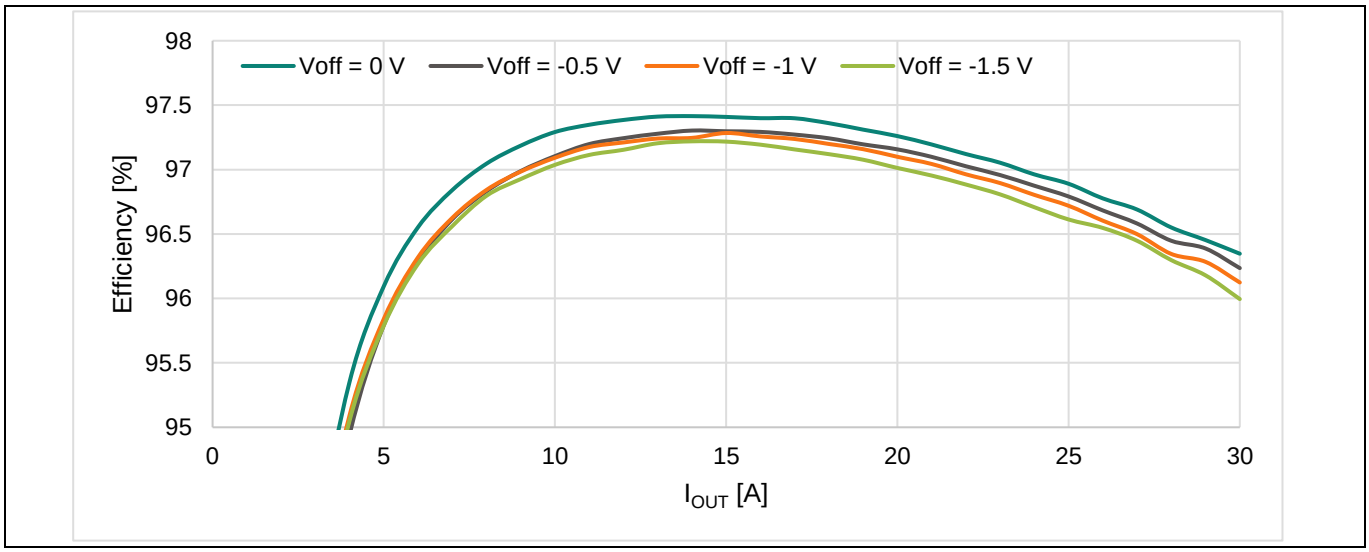


Figure 31 **Example efficiency results for different off-state gate voltages with 1EDN7126G, buck-mode 48 V to 12 V, 500 kHz, 3.3 µH inductor with heatsink attached on bottom and 5 m/s airflow**

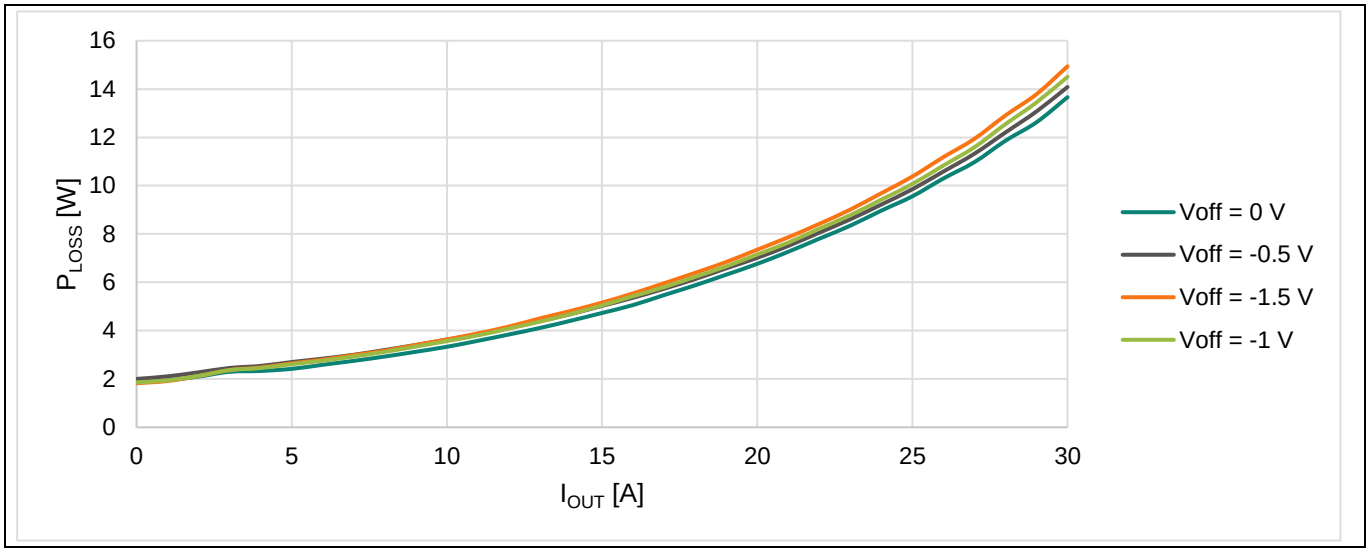


Figure 32 **Example overall power loss for different off-state gate voltages with 1EDN7126G, buck-mode 48 V to 12 V, 500 kHz, 3.3 µH inductor, heatsink attached on bottom and 5 m/s airflow**

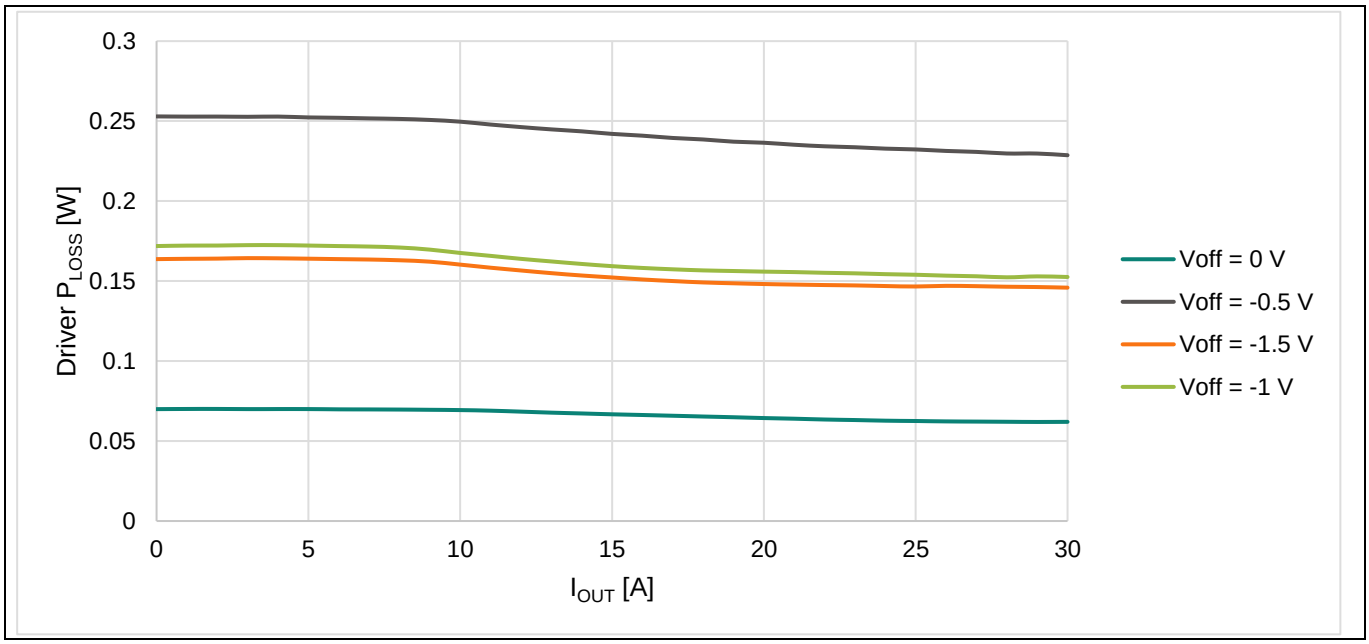


Figure 33 **Example driver power loss for different off-state gate voltages with 1EDN7126G, buck-mode 48 V to 12 V, 500 kHz, 3.3 µH inductor, heatsink attached on bottom and 5 m/s airflow**

GaN power transistors have a reverse conduction mechanism that mimics a MOSFET body diode, with the exception that the "body diode" voltage drop is directly proportional to the negative voltage applied. Therefore, applying a more negative off-state voltage than necessary produces higher losses during the dead-time.

5.5 Thermal images

To show the influence of different cooling and switching frequency to the temperature of the board, it is operated at 48 V input voltage, 12 V output voltage, 20 A output current, with a 3.3 µH inductor. The results for the heatsink attached on the bottom side of the PCB are shown in Figure 34. For the heatsink attached on the top side the results are shown in Figure 35.

At the given load condition of 20 A, the influence of different cooling is clearly visible. With the heatsink on the bottom-side of the board and an airflow of 5 m/s, the devices reach a maximum temperature of 57°C for the high-side switch and 52°C for the low-side switch at 500 kHz. Increasing the switching frequency to 1 MHz increases the temperature of the high-side device to 79°C and to 64°C for the low-side device in this example measurement.

The best results can be achieved when the heatsink is attached to the top-side of the switches because the IGC033S10S1 is a dual-side cooled package. It is not possible to capture the surface temperature for each device in a thermal image with the heatsink attached on top but the maximum temperature across the whole board is 38°C at 500 kHz and 45°C at 1 MHz switching frequency in this case.

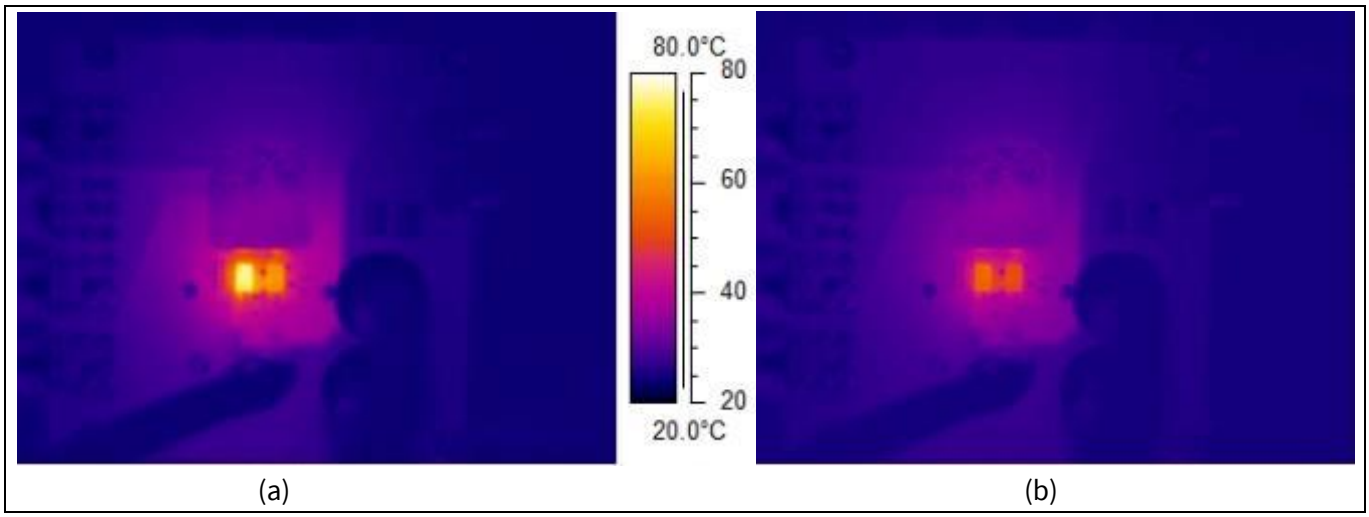


Figure 34 (a) Thermal imaging results for the board operated with heatsink on bottom and 5 m/s airflow, 48 V to 12 V buck-mode, 3.3 µH inductor, 20 A at 1 MHz; (b) 500 kHz

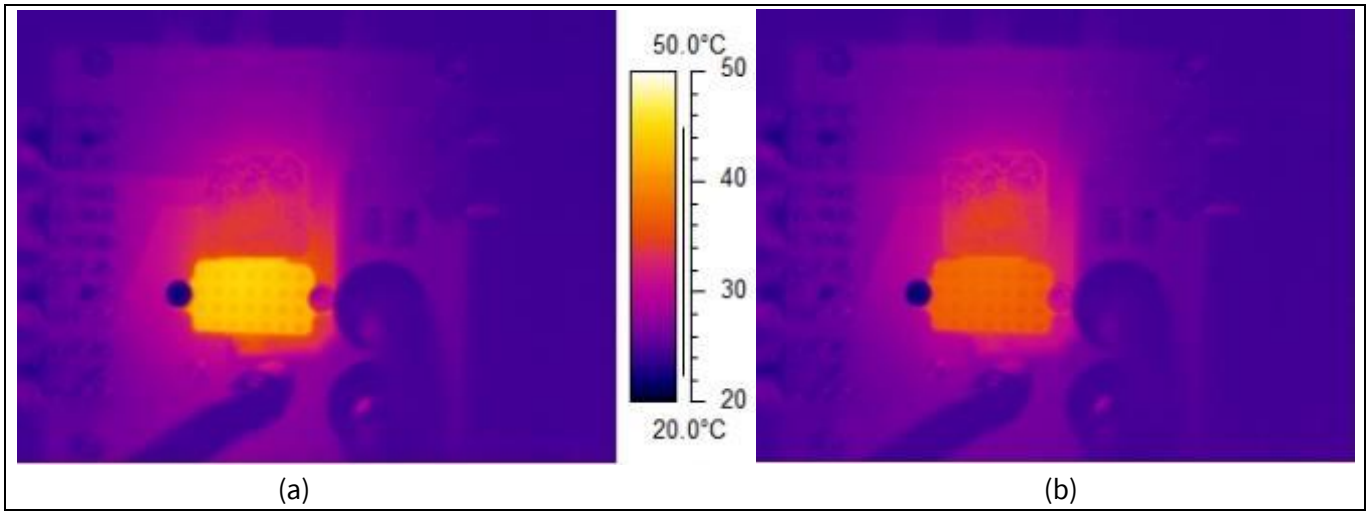


Figure 35 (a) Thermal imaging results for the board operated with heatsink on top and 5 m/s airflow, 48 V to 12 V buck-mode, 3.3 µH inductor, 20 A at 1 MHz; (b) 500 kHz

6 Board documentation

6.1 Schematic

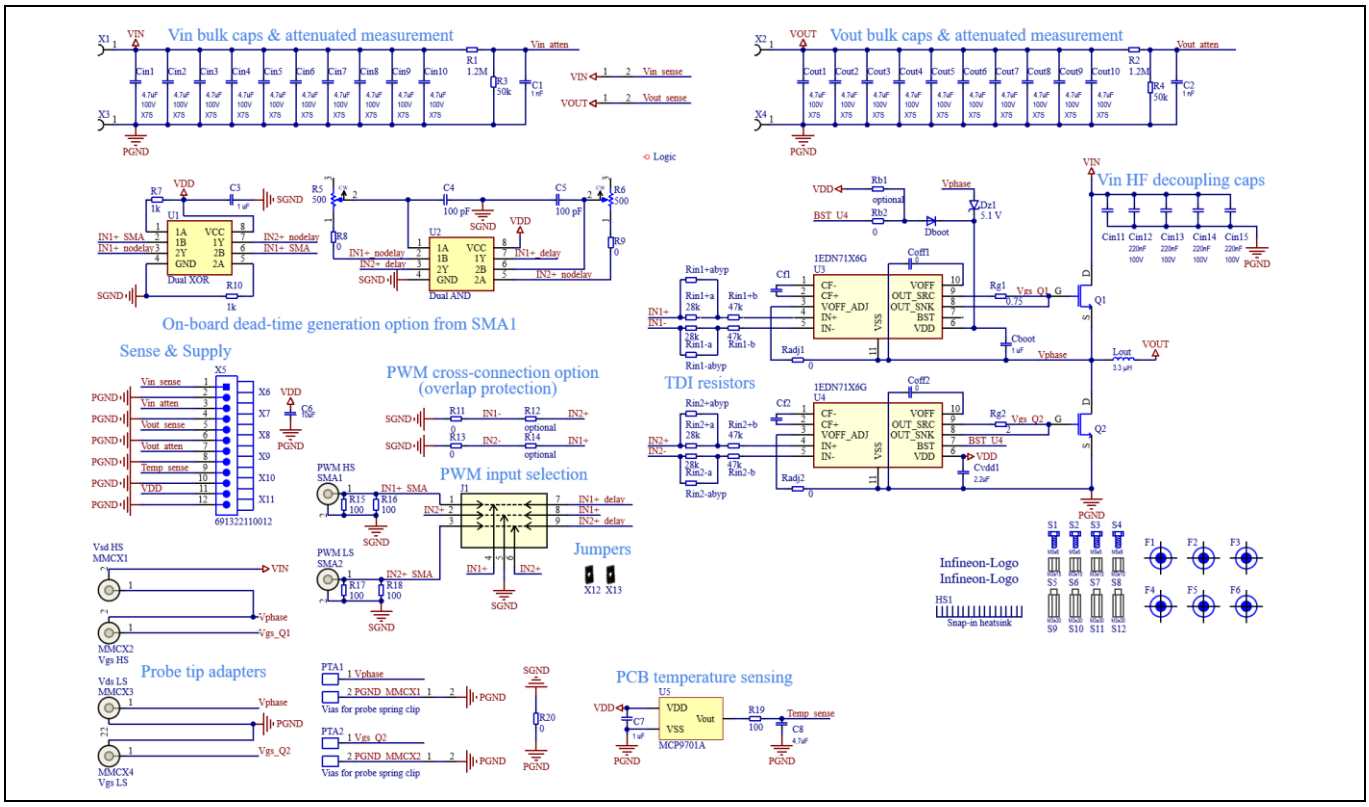


Figure 36 EVAL_7126G_100V_GaNc

6.2 Layout

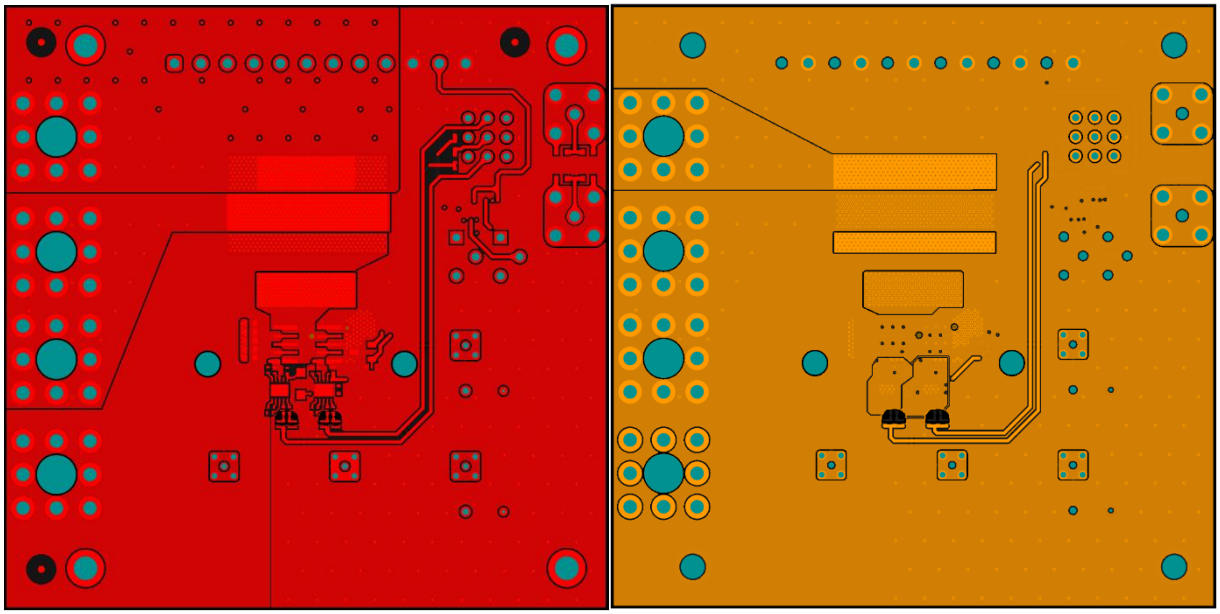


Figure 37 (a) PCB layout top-layer; (b) mid-layer 1

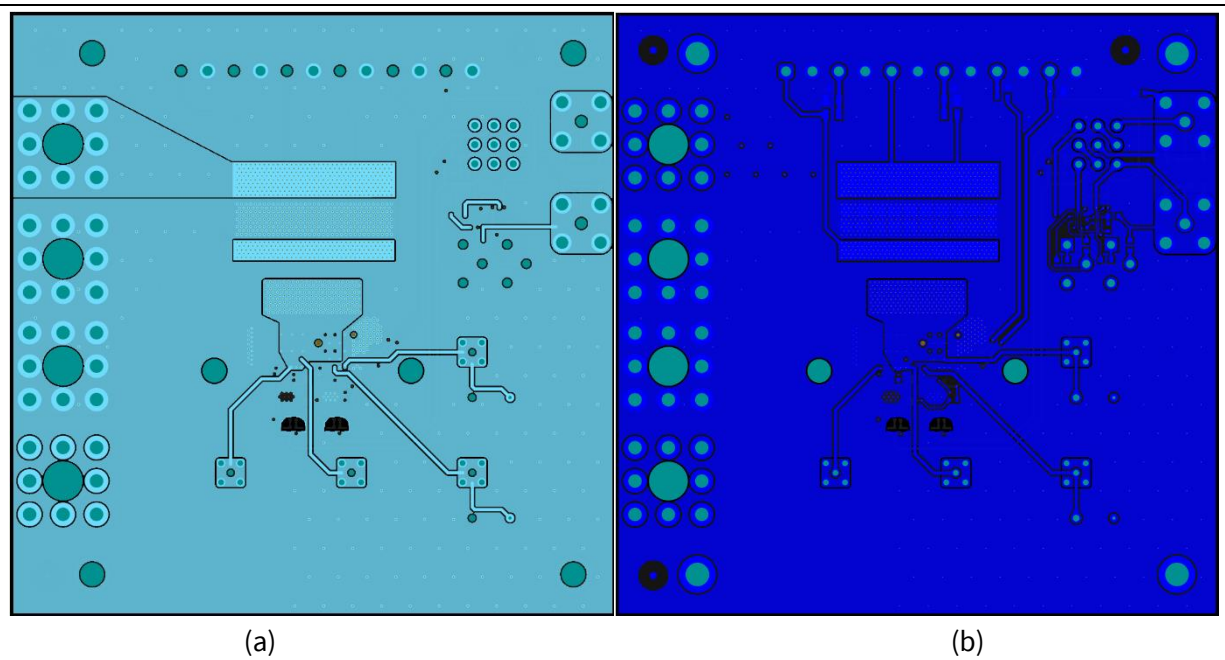


Figure 38 (a) PCB layout mid-layer 2; (b) bottom layer

6.3 Bill of materials

Table 5 Bill of materials

#	Designator	Value	Manufacturer	Manufacturer part number
1	C1, C2	1 nF	Kemet	C0603C102K3GACTU
2	C3	1 µF	Murata	GCM188R71E105KA64D
3	C4, C5	100 pF	Würth Elektronik	885012006023
4	C6	10 µF	Murata	GRM21BC71E106ME11L
5	C7, Cboot	1 µF	Murata	GRT155C81E105KE13D
6	C8	4.7 µF	Murata	GRM188C81E475KE11D
7	Cf1, Cf2	optional	–	–
8	Cin1 ~ Cin10, Cout1 ~ Cout10	4.7 µF	Murata	GRM31CC72A475ME11L
9	Cin11, Cin12, Cin13, Cin14, Cin15	220 nF	Taiyo Yuden	HMK107C7224KAHTE
10	Coff1, Coff2	0 Ω	Stackpole	RMCF0402ZT0R00
11	Cvdd1	2.2 µF	Murata	GRM155C81E225ME11D
12	Dboot	Schottky diode	ON semi	MBR2H200SFT1G
13	Dz1	optional	Diodes Inc	BZT585B5V6T-7
14	HS1	Heatsink	–	–
15	J1	Header	Samtec	TSW-103-07-G-T
16	Lout	3.3 µH	Vishay	IHLP7575JZERER3R3M5A
17	MMCX1 ~ MMCX4	MMCX vertical jack	Würth Elektronik	66012002111503
18	Q1, Q2	CoolGaN™ power transistor	Infineon	IGC033S10S1
19	R1, R2	1.2 MΩ	Susumu	RG2012P-125-B-T5
20	R3, R4	50 kΩ	Vishay	PTN0805E5002BST1
21	R5, R6	500 Ω	Vishay	T63YB501KT20
22	R7, R10	1 kΩ	Stackpole	RMCF0402FT1K00
23	R8, R9, R20	0 Ω	Yageo	RC0603JR-070RL
24	R11, R13, Rb2, Radj1, Radj2	0 Ω	Stackpole	RMCF0402ZT0R00
25	R12, R14, Rb1	Optional	–	–
26	R15, R16, R17, R18, R19	100 Ω	Stackpole	RMCF0603FG100R
27	Rg1	1 Ω	KOA Speer	SG73P1EWTTP1R0J
28	Rg2	2 Ω	KOA Speer	SR731ERTTP2R00F
29	Rin1+a, Rin1-a, Rin2+a, Rin2-a	28 kΩ	Panasonic	ERA-2APB2802X

#	Designator	Value	Manufacturer	Manufacturer part number
30	Rin1+abyp, Rin1-abyp, Rin2+abyp, Rin2-abyp	Optional	–	–
31	Rin1+b, Rin1-b, Rin2+b, Rin2-b	47 kΩ	Panasonic	ERA-2APB473X
32	S1, S2, S3, S4	M5x6 mm	B&F	MPMS 005 0006 PH
33	S5, S6, S7, S8	Spacer 15mm fem. M3	Würth Elektronik	970150321
34	S9, S10, S11, S12	Spacer 30mm male M3	Würth Elektronik	970300321
35	SMA1, SMA2	SMA jack	Würth Elektronik	60311002111526
36	U1	Dual XOR	Diodes Inc	74LVC2G86HK3-7
37	U2	Dual AND	Nexperia	74LVC2G08GS-Q100X
38	U3, U4	TDI EiceDriver™ for GaN	Infineon	1EDN7126G
39	U5	MCP9701AT-E/TT	Microchip Technology	MCP9701AT-E/TT
40	X1, X2, X3, X4	Redcube connector	Würth Elektronik	74655095R
41	X5	Screw terminal header	Würth Elektronik	691322110012
42	X6, X7, X8, X9, X10, X11	Screw terminal plugs	Würth Elektronik	691363110002
43	X12, X13	Jumpers	Würth Elektronik	609002115121

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Revision history

Document revision	Date	Description of changes
V 1.0	2024-07-17	Initial release
V 1.1	2024-12-12	Updated schematic figure
V 1.2	2025-04-03	Fixed naming

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