2EDL900G3 Evaluation Board user guide

Optimized for OptiMOS™ power MOSFETs

About this document

Figure 1 Overview of EVAL_HB_2EDL900G3_Si Evaluation Board

Scope and purpose

This user guide provides information about the EVAL_HB_2EDL900G3_Si Evaluation Board for Infineon's EiceDRIVER™ 2EDL900G3 gate driver, including the board's functionality, interfaces, jumper settings, assembled components, configurations through optional resistors and debugging options. In addition, it includes the default bill of materials (BOM), schematics and layout of the board.

Intended audience

This document is intended for anyone using the EVAL_HB_2EDL900G3_Si Evaluation Board.

About this product group

Target applications

AI server and SMPS applications.

Product family

Infineon's EiceDRIVER™ 2EDL90xG3 gate driver product family has two variants: 2EDL900G3 optimized for Si MOSFETs and the 2EDL901G3 optimized for driving MV GaN MOSFETs.

This evaluation board focuses on 2EDL900G3 that drives two OptiMOS™ devices.

Evaluation Board

This board is to be used during the design-in process for evaluating the 2EDL900G3 product features.

Note: PCB and auxiliary circuits are NOT optimized for final customer design.

Safety precautions

Note: *Please note the following warnings regarding the hazards associated with development systems.*

Table 1 **Safety precautions**

	**Caution:** *The heat sink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.*
	**Caution:** *Only personnel familiar with the drive, power electronics and associated machinery should plan, install, commission and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.*
	**Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	**Caution:** *A drive that is incorrectly applied or installed can lead to component damage or reduction in product lifetime. Wiring or application errors such as undersizing the motor, supplying an incorrect or inadequate AC supply, or excessive ambient temperatures may result in system malfunction.*
	**Caution:** *The evaluation or reference board is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials that are unnecessary for system installation may result in overheating or abnormal operating conditions.*

Table of contents

1 The board at a glance

Figure 2 shows the general-purpose evaluation board for Infineon's EiceDRIVER™ 2EDL900G3 gate driver, together with the OptiMOS™ ISC016N08NM8SC and ISC031N08NM6SC 80 V MOSFETs in a SuperSO8 DSC package. This board includes an optimized layout for a hard-switching half-bridge configuration, as well as waveform measurement points and other useful features that enable easy lab bench characterization of the gate driver and the power switches.

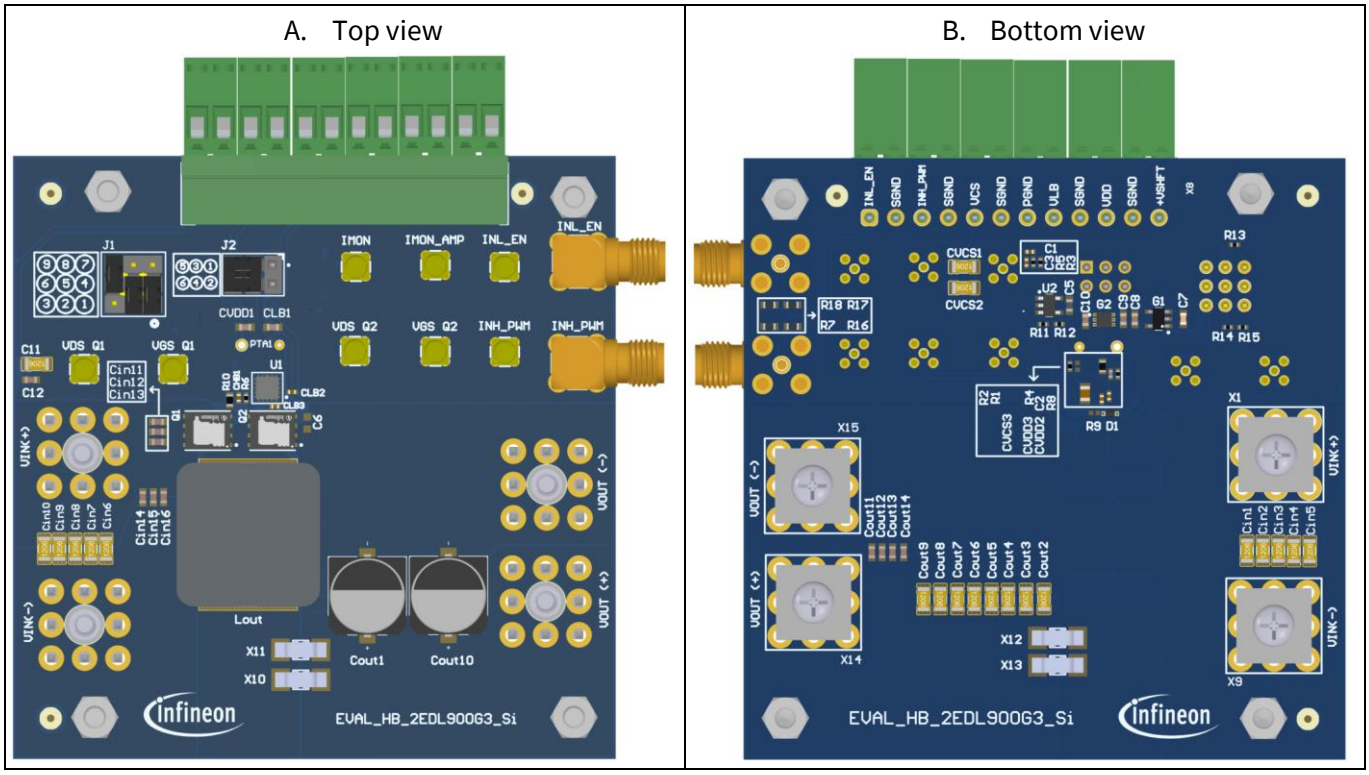

Figure 2 EVAL_HB_2EDL900G3_Si top (A) and bottom (B) view

1.1 Scope of supply

The EVAL_HB_2EDL900G3_Si board is an open-loop buck converter. It can be configured to operate as a typical half-bridge buck converter, wherein the buck converter's power ground (PGND) and signal ground (SGND) are at the same node. Circuitry such as the input supply of the gate driver, LDOs, input PWM, and IMON signals are referenced to SGND. In this user guide, this configuration is referred to as the "non-voltage-level-shifted" configuration.

On the other hand, the board can also be configured as a dual floating-gate drive via external connections. In this configuration, it is still a buck converter, but the PGND and SGND are at two different nodes. The PGND is shifted by a positive voltage, +V_SHFT, with respect to SGND. In this user guide, this is referred to as the "voltage-level-shifted" configuration.

See Section 3 for a detailed description on how to configure the board.

The board at a glance

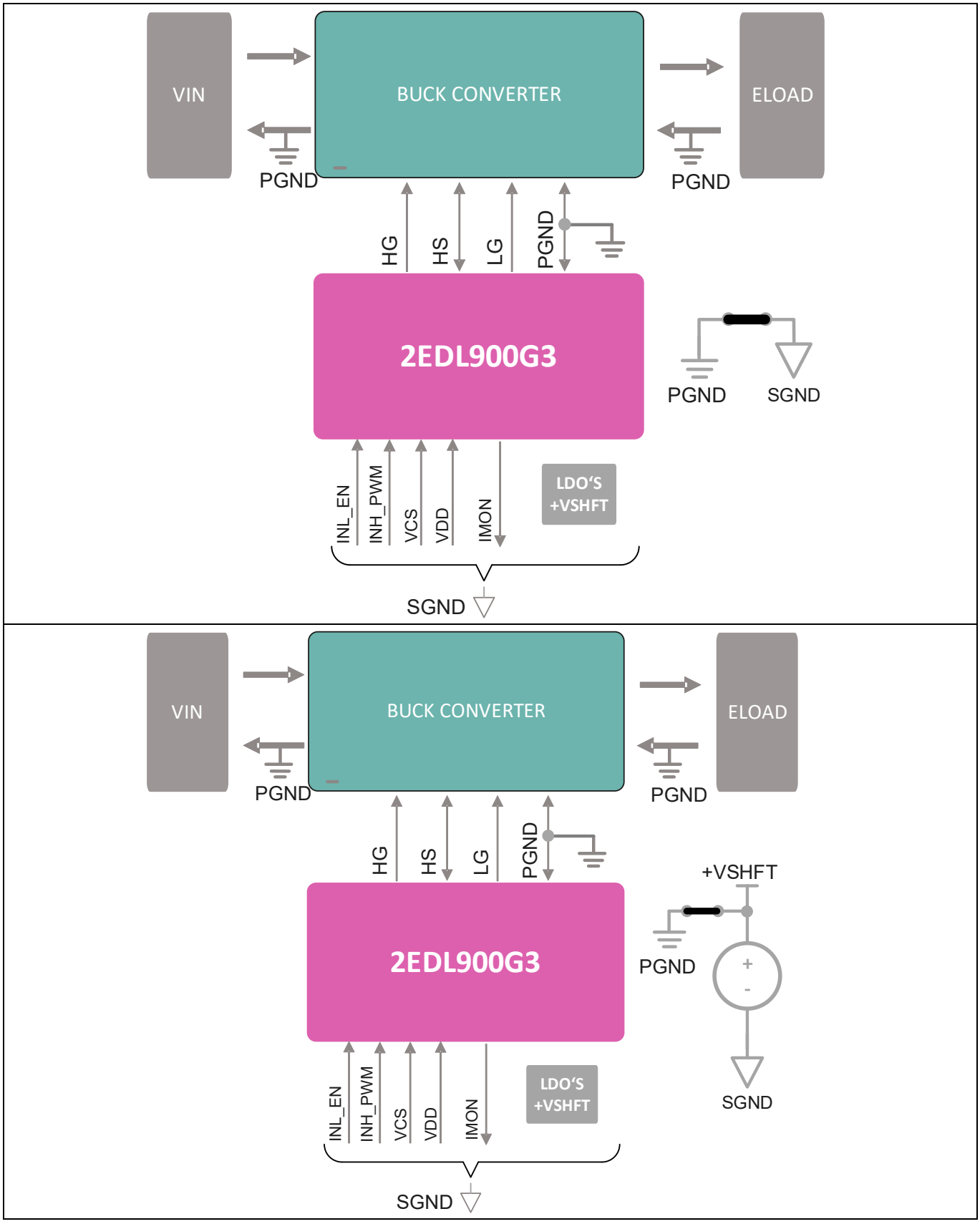

Figure 3 Configurations - Top: Non-voltage-level-shifted; bottom: Voltage-level-shifted

The board is also capable of probing the IMON signal, which senses the DC resistance of the output choke. The supply voltage for the VHB-HS domain is bootstrapped from VDD for non-voltage level-shifted configuration and from VLB-PGND for voltage-level-shifted configuration. When operated in voltage-level-shifted configuration, bootstrapping is done externally via D1, so populate R9 with 1R resistor. The source of the two PWM inputs of the driver and gate driver power supply for both input and the floating channel, VLB-PGND, are not part of the scope of this evaluation board and should be generated externally.

1.2 Block diagram

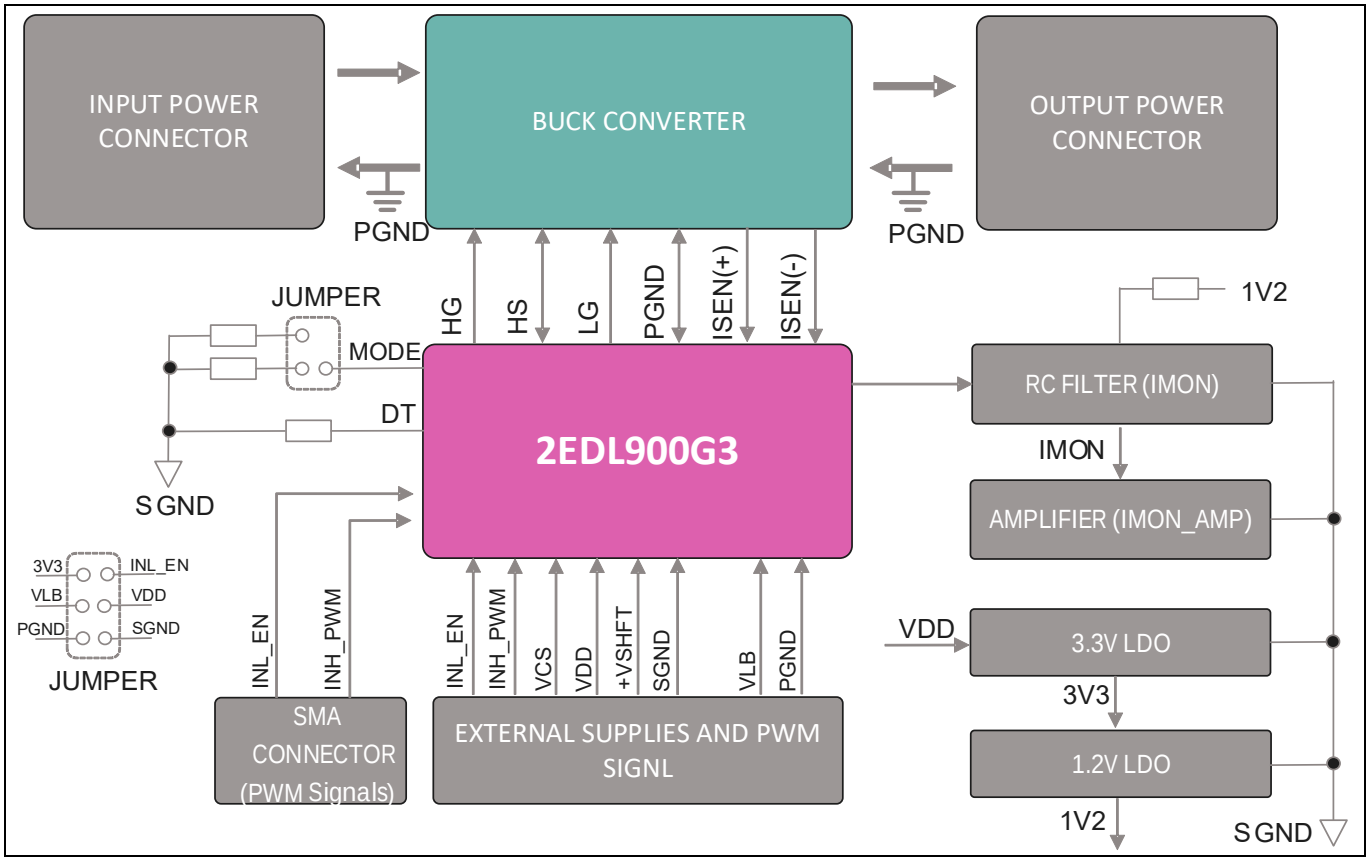

Figure 4 Block diagram of EVAL_HB_2EDL900G3_Si

1.3 Main features

- Configurable in either of the two configurations:
  - Non-voltage-level-shifted
  - Voltage-level-shifted via external connections
- Configurable into two modes of operation:
  - Tri-state single PWM mode
  - HI/LI Input mode
- IMON signal monitoring via DC resistance (DCR) current sensing of the output inductor
- Wide 5 V to 10 V gate driving voltage operating range
- Test points ready for waveforms measurements for evaluation

1.4 Board parameters and technical data

The table below specifies the board parameters and its technical data.

Table 2 Board parameters

Parameter	Symbol	Conditions	Value	Unit
Input voltage	VIN	Reference to PGND	0 to 60	V
Output voltage	VOUT	Non-voltage-level-shifted	35, maximum	V
		Voltage-level-shifted	35 –(+VSHFT), maximum	
VDD voltage	VDD	Reference to SGND	5 to 10	V
VLB voltage	VLB	Reference to PGND	5 to 10	V
Switching frequency	Fsw	—	200 to 300	kHz

Note: The evaluation board is optimized for operation with an input voltage (VIN) of 48 V, a duty cycle (D) of 25%, a switching frequency (fsw) of 200 kHz, and a load current of up to 15 A, without a fan and at room ambient temperature. The VDD and VLB is at 10 V.

Attention:

- ***Testing beyond the optimized duty cycle, fsw, ambient temperature, and output power for your specific evaluation requires monitoring of thermal performance of the power switches and inductor***
- ***Output inductor (Lout) is IHLP7575GZ: L = 3.3 µH, DC saturation current = 28 A (Lo to drop approximately to 20%). This needs to be considered when testing beyond a 15 A load***

2 System and functional description

2.1 Getting started

The following figure shows the top and bottom overview of the evaluation board and brief description per section.

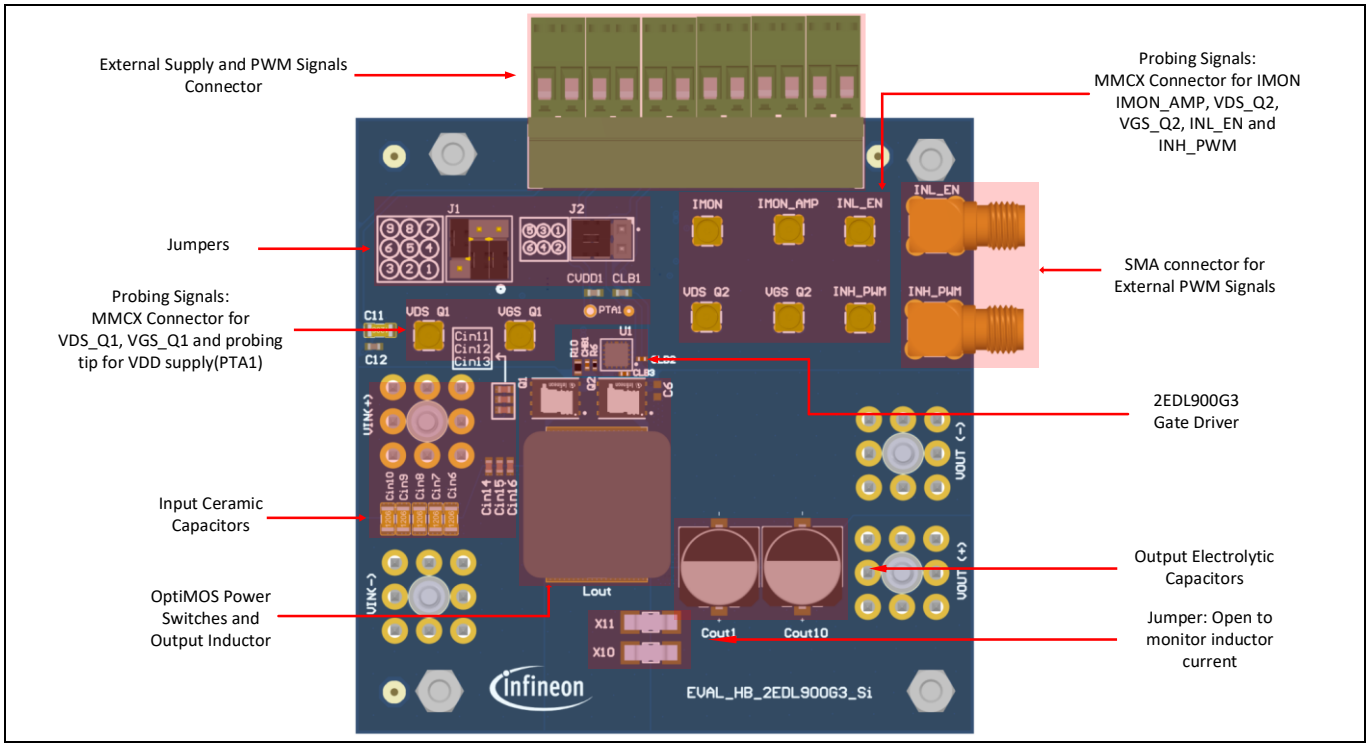

Figure 5 Board description – top layer

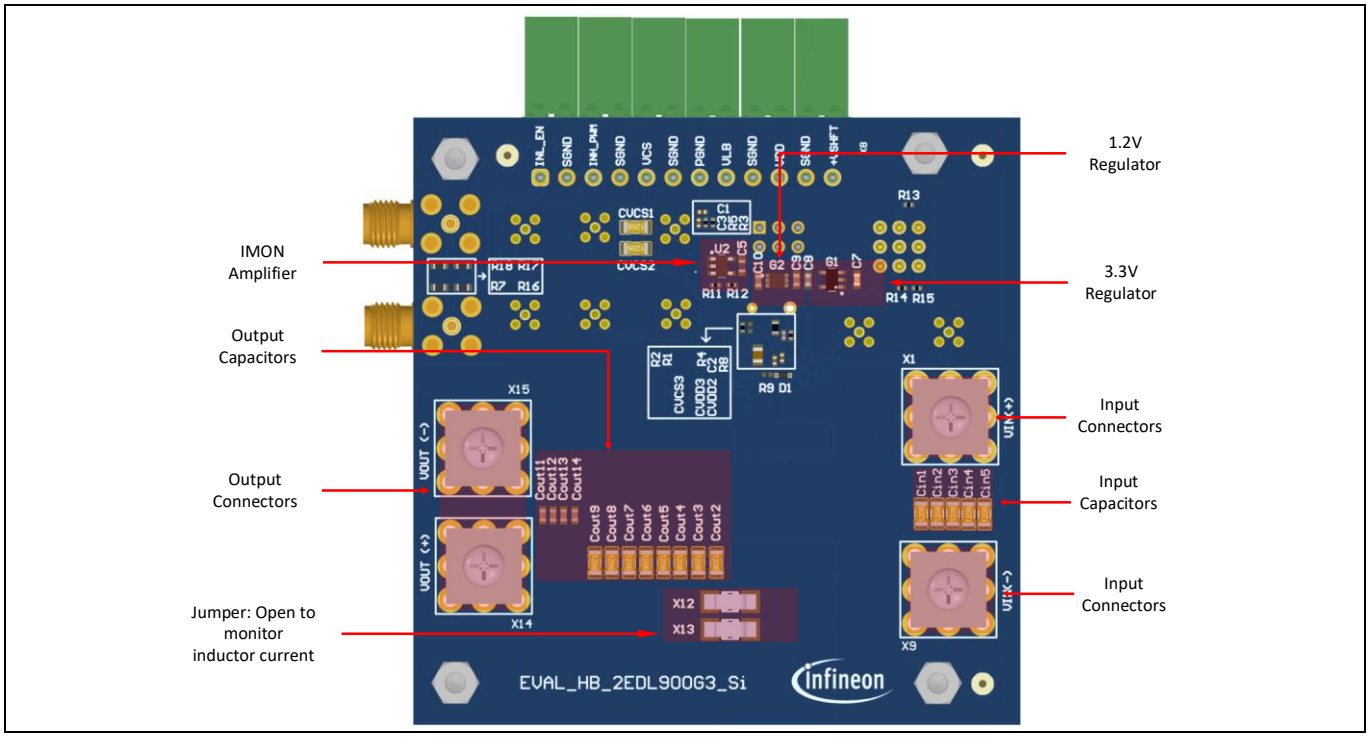

Figure 6 Board description – bottom layer

2.2 Jumpers

Jumpers J1 and J2 set two different functionalities for the gate drivers. Jumper J1 selects the mode of operation, either tri-state single PWM mode or HI/LI input mode. Meanwhile, jumper J2 configures the board for either a non-voltage-level-shifted or a voltage-level-shifted configuration.

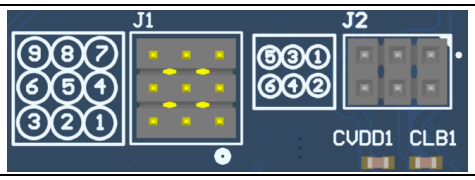

Figure 7 Jumpers J1 and J2

Table 3 Jumper settings

Configuration	MODE	J1	J2
Non-voltage-level-shifted	Tri-state single PWM	Short pins 1 and 4 Short pins 6 and 9	Short pins 3 and 5 Short pins 4 and 6
	HI/LI input	No shorted pins	Short pins 3 and 5 Short pins 4 and 6
Voltage-level-shifted-buck	Tri-state single PWM	Short pins 1 and 4 Short pins 6 and 9	No shorted pins
	HI/LI input	No shorted pins	No shorted pins

2.3 SMA terminals for PWM inputs

The SMA connectors are provided for use with external function generators that require a BNC-to-SMA cable to input the two PWM signals.

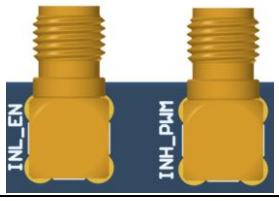

Figure 8 SMA connector terminals for input PWMs signals

2.4 Supply and signal terminals

The X8 connector provides supply and signal terminals, facilitating easy connection and testing during lab verification.

Figure 9 Connector for external power supply and PWM Signals

Table 4 X8 connector functional description

Name	Description
INL_EN	Input PWM of the gate driver for driving Q2 gate to source voltage
SGND	Signal ground (reference ground for the VDD, IMON, LDOs, input PWMs, VCS, +VSHFT)
INH_PWM	Input PWM of the gate driver for driving Q1 gate to source voltage
SGND	Signal ground (reference ground for the VDD, IMON, LDOs, input PWMs, VCS, +VSHFT)
VCS	Supply voltage of the integrated current sense amplifier
SGND	Signal ground (reference ground for the VDD, IMON, LDOs, input PWMs, VCS, +VSHFT)
PGND	Power ground (reference ground for VLB and Kelvin Source connected to Q2 source pin)
VLB	Supply voltage for the LG output channel
SGND	Signal ground (reference ground for the VDD, IMON, LDOs, input PWMs, VCS, +VSHFT)
VDD	Supply voltage for the input circuitry of the gate driver. Reference to SGND
SGND	Signal ground (reference ground for the VDD, IMON, LDOs, input PWMs, VCS, +VSHFT)
+VSHFT	Supply voltage when in voltage-level-shifted configuration. The voltage is the shifted voltage level

2.5 MMCX connectors, probe tip adapters, and jumpers for waveform measurements

The board features designated test points for easy connection to an oscilloscope, allowing for the measurement and analysis of waveforms.

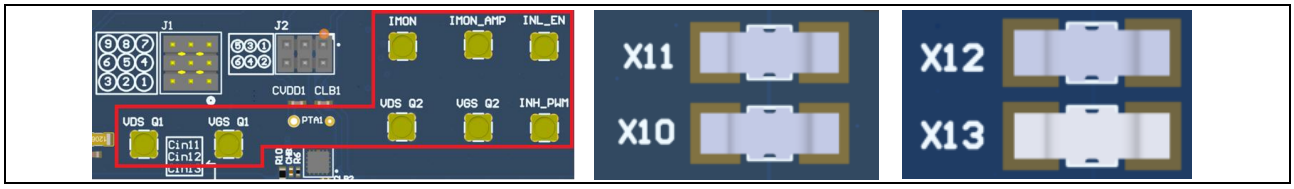

Figure 10 Test points available in the EVAL_HB_2EDL900G3_Si

Table 5 Functional description of the test points

Test points	Description
IMON	Current information sensed by the integrated current sense amplifier
IMON_AMP	Amplified signal of IMON with a gain of two
VDS_Q1	Drain to source voltage of Q1 (High-side MOSFET)
VGS_Q1	Gate to source voltage of Q1 (High-side MOSFET)
VDS_Q2	Drain to source voltage of Q2 (Low-side MOSFET)
VGS_Q2	Gate to source voltage of Q2 (Low-side MOSFET)
INL_EN	Input PWM of the gate driver for driving Q2
INH_PWM	Input PWM of the gate driver for driving Q1
X10, X11, X12, X13	For measuring inductor current. Open these jumpers and loop a current probe
PTA1	Probe tip point for VDD supply

2.6 Power input and output terminals

Use the terminals to connect power cables for the input voltage source and electronic load.

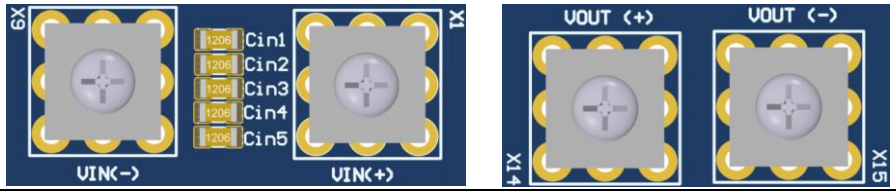

Figure 11 Input and output connector terminals

Table 6 Functional description of power terminals

Board label	Schematic designation	Description
VIN(-)	X9	Return ground of the converter's input voltage source
VIN(+)	X1	Positive terminals of the converter's input voltage source
VOUT (+)	X14	Positive terminals of the converter's output load
VOUT (-)	X15	Return ground of the converter's output load

3 Configuration

3.1 Non-voltage-level-shifted

In a non-voltage-level-shifted configuration, the evaluation board operates similarly to a typical half-bridge buck converter. The reference ground for the input PWM signal, VDD, IMON, LDOs, VCS, and +VSHFT is connected to the signal ground (SGND). In contrast, the reference ground for the power buck converter and VLB is connected to the power ground (PGND). To configure the board in this mode, use jumper J2 to short SGND and PGND together. J2 provides a convenient way to connect and disconnect SGND to PGND, as well as VDD to VLB.

When SGND and PGND are connected, and VDD and VLB are linked, the result is a common ground for both SGND and PGND, and a single external supply for VDD and VLB. This simplifies the board's configuration and allows for easier testing and evaluation.

The 2EDL900G3 gate driver features an integrated boot diode from VDD to HB pins. By default, resistor R9 is open, which means that the internal boot diode of 2EDL900G3 is used. However, if a test requires the use of an external boot diode, populate resistor R9 with a 1R resistor to enable the use of external diode D1. This flexibility allows users to choose between using the internal boot diode or an external one, depending on their specific testing needs.

Table 7 Jumper J2 settings for non-voltage-level-shifted configuration

J2 pin status	Description
Short pins 4 and 6	Shorting nodes SGND and PGND to have a common ground for SGND and PGND
Short pins 3 and 5	Shorting nodes VDD and VLB to have a single external voltage supply

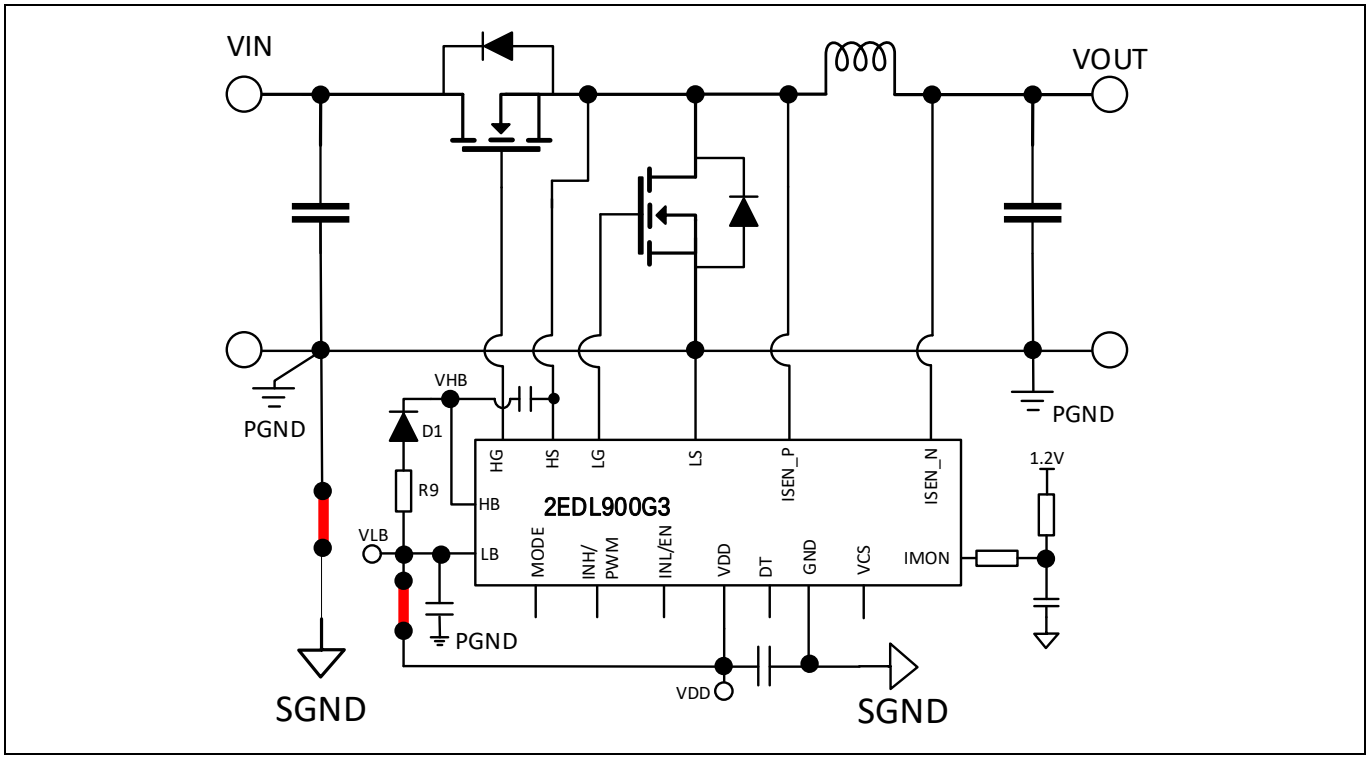

Figure 12 Effective circuit in non-voltage-level-shifted configuration

3.2 Voltage-level-shifted

In the voltage-level-shifted configuration, the evaluation board still operates as a buck converter, but with a key difference. The PGND is positively voltage-level-shifted with respect to the SGND. This voltage shift is achieved through an external supply, which is applied via the +VSHFT pin, referenced to SGND. The +VSHFT pin provides a convenient way to introduce the voltage shift, allowing users to control the level of shift and optimize the board's performance.

In this configuration, it's essential to note that VDD and VLB have different reference grounds. VDD is referenced to SGND, while VLB is referenced to PGND. As a result, all pins in jumper J2 must be kept floating to maintain the voltage level shift and prevent any unintended connections between the two grounds. By keeping J2 floating, users can ensure that the voltage level shift is preserved, and the board operates correctly.

To summarize, the key characteristics of the voltage-level-shifted configuration are:

- PGND is positively voltage-level-shifted with respect to SGND
- The voltage shift is achieved through an external supply applied via +VSHFT
- VDD and VLB have different reference grounds (SGND and PGND, respectively)
- All pins in jumper J2 must be kept floating to maintain the voltage level shift

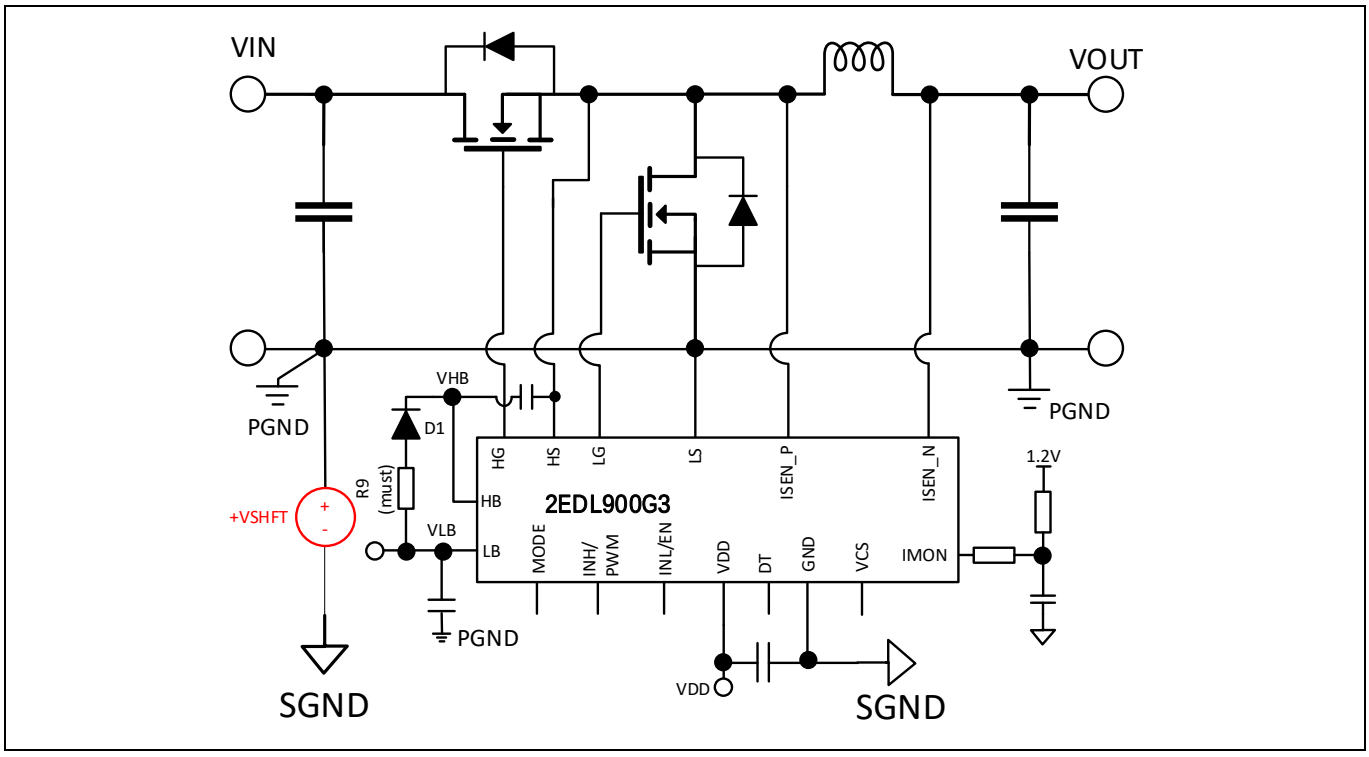

Figure 13 Effective circuit in voltage-level-shifted configuration

Table 8 Jumper J2 setting for voltage-level-shifted configuration

J2 pin status	Notes
All pins are floating	VDD-SGND and VLB-PGND must have a dedicated external supply in which its reference is not in common ground

Attention: In voltage-level-shifted configuration, external boot diode D1 MUST be used. Place R9 with 1R resistor.

3.3 Tri-state single PWM mode

To configure the evaluation board in tri-state single PWM mode, use the settings for Jumper J1 as follows.

Table 9 Jumper J1 setting for tri-state single PWM mode

J1 pin status	Description
Short pins 1 and 4	Shorting INL_EN to 3.3 V
Short pins 6 and 9	Shorting MODE pin of 2EDL900G3 to SGND

3.4 HI/LI input mode

To configure the evaluation board in HI/LI input mode, use the settings for Jumper J1 as follows.

Table 10 Jumper J1 setting for HI/LI mode

J1 pin status	Description
All pins are floating	MODE pin of 2EDL900G3 is set to high impedance

Note: There is a possibility to check the three other MODES of 2EDL900G3 (HSCC HS, HSCC LS, and HI/LI inverted), but it is not recommended because the timing sequence of this modes does not match with the buck converter timing. For the purpose of checking the timing sequence only, see Jumper J1 settings in Table 11.

Table 11 Jumper J1 settings for other modes of 2EDL900G3

Mode	J1 settings
HSCC HS	Short pins 3 and 6
HSCC LS	Short pins 5 and 8
HI/LI inverted	Short pins 2 and 5

4 Test setup sequence

4.1 Non-voltage-level-shifted configuration

1. Configure Jumper J2 per Table 7
2. Configure Jumper J1 depending on the preferred mode. For tri-state single PWM mode, see Table 9. For HI/LI input mode, see Table 10
3. Supply the following:
   - +10 V on VDD in reference to SGND in the X8 connector
   - +48 V on VCS in reference to SGND in the X8 connector
   - Input PWMs signal to the SMA connectors from a signal generator
4. Connect input voltage source for the buck converter with the positive terminal on VIN (+) and ground on VIN (-)
5. Connect electronic load for the buck converter with the positive terminal on VOUT (+) and ground on VOUT (-)

4.2 Voltage-level-shifted configuration

1. Configure Jumper J2 per Table 8
2. Configure Jumper J1 depending on the preferred mode. For tri-state single PWM, see Table 9 For HI/LI input mode, see Table 10
3. Supply the following:
   - +10 V on VDD to SGND in the X8 connector
   - +10 V on VLB to PGND in the X8 connector
   - Supply a positive +VSHFT voltage in reference to SGND in the X8 connector
   - +48V on VCS to SGND in the X8 connector
   - Input the PWM signal to the SMA connector from a signal generator
4. Connect R9 with 1R resistor
5. Connect the input voltage source for the buck converter with the positive terminal on VIN (+) and ground on VIN (-)
6. Connect an electronic load for the buck converter with the positive terminal on VOUT (+) and ground on VOUT (-)

5 System design

5.1 Schematics

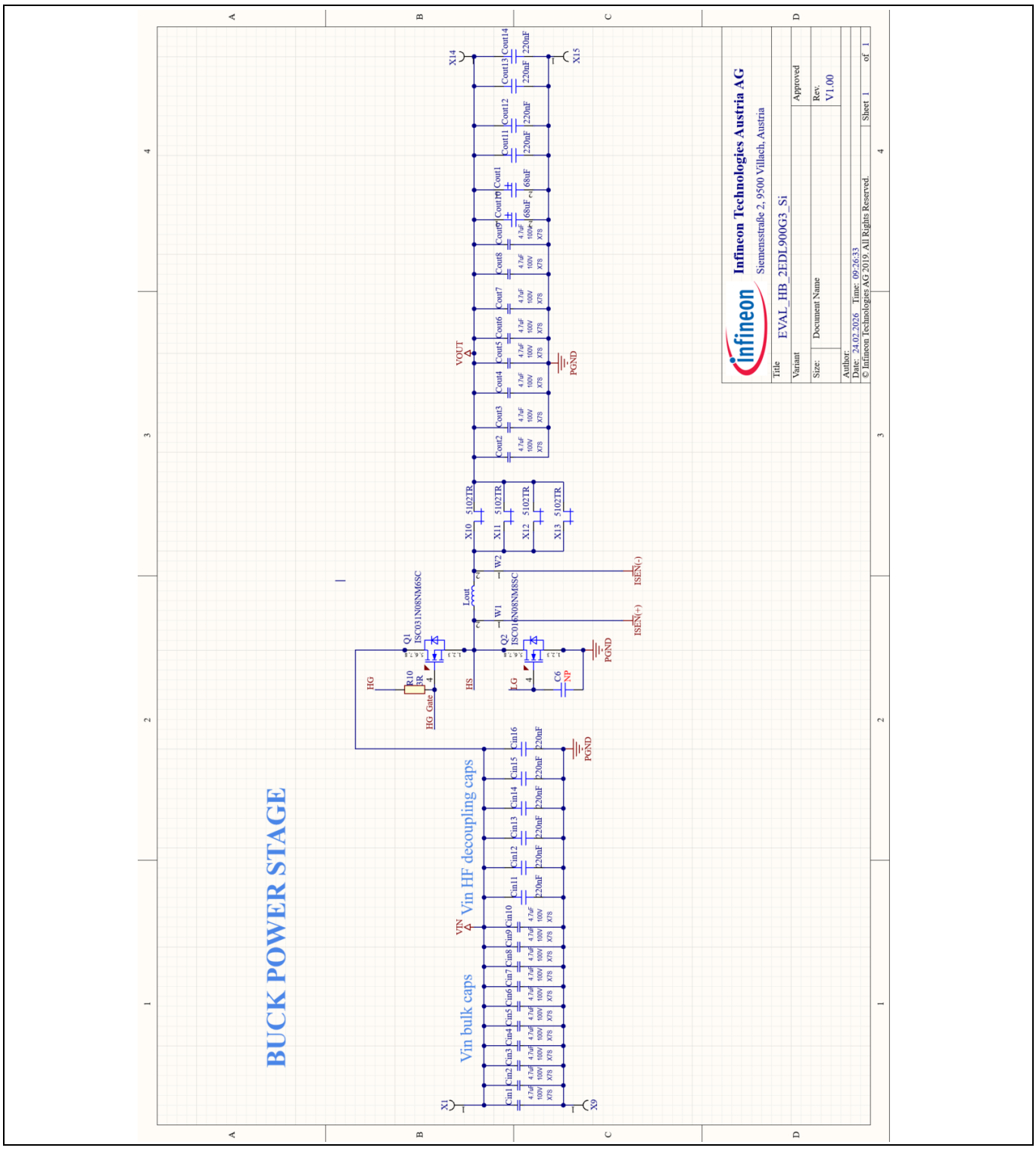

Figure 14 Schematic of the buck converter's power stage

Note: "NP" in the schematic means ''Not populated''.

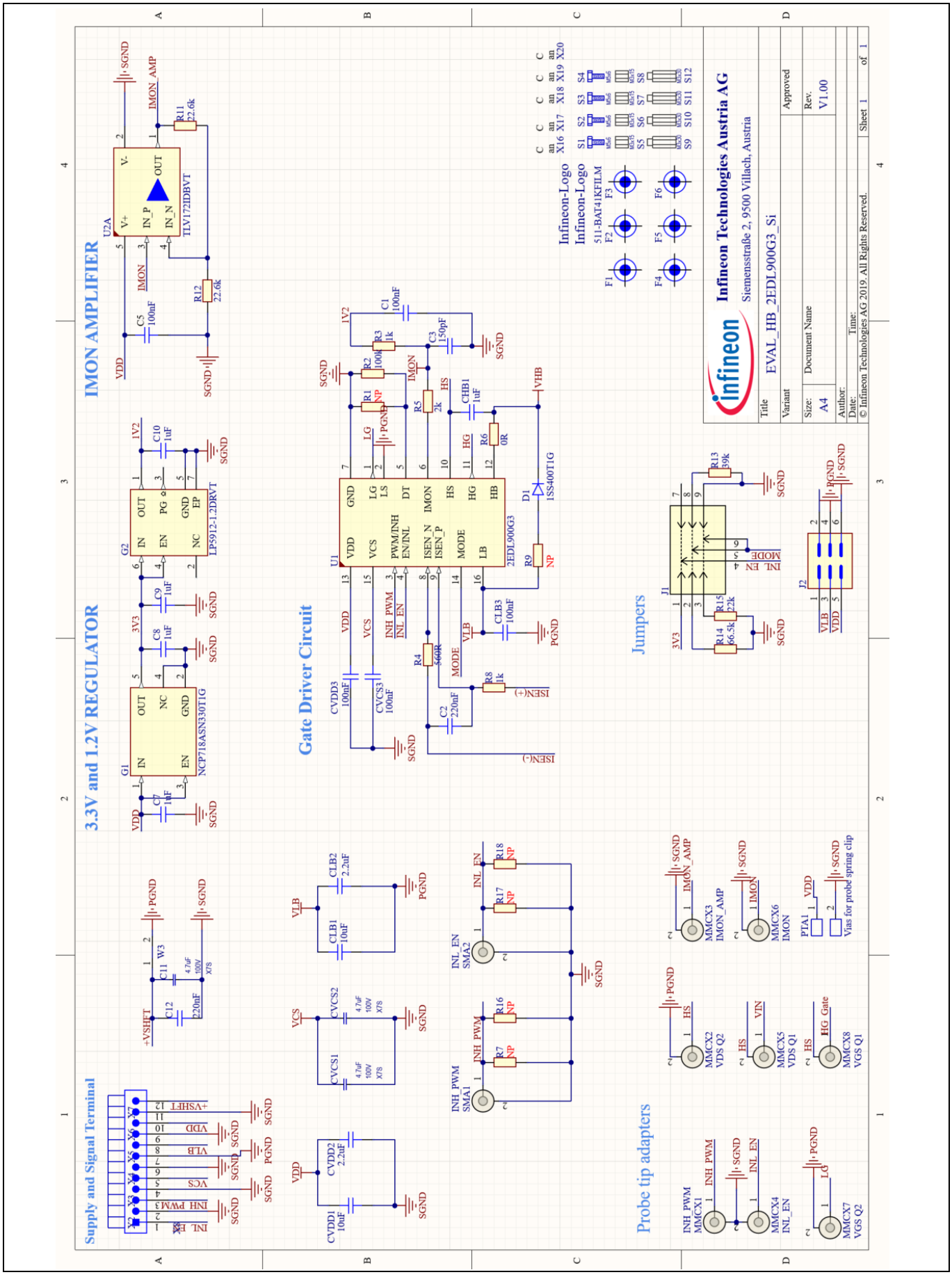

Figure 15 Schematic of the driver, LDOs, jumpers, connectors, IMON, and probing points

5.2 Layout

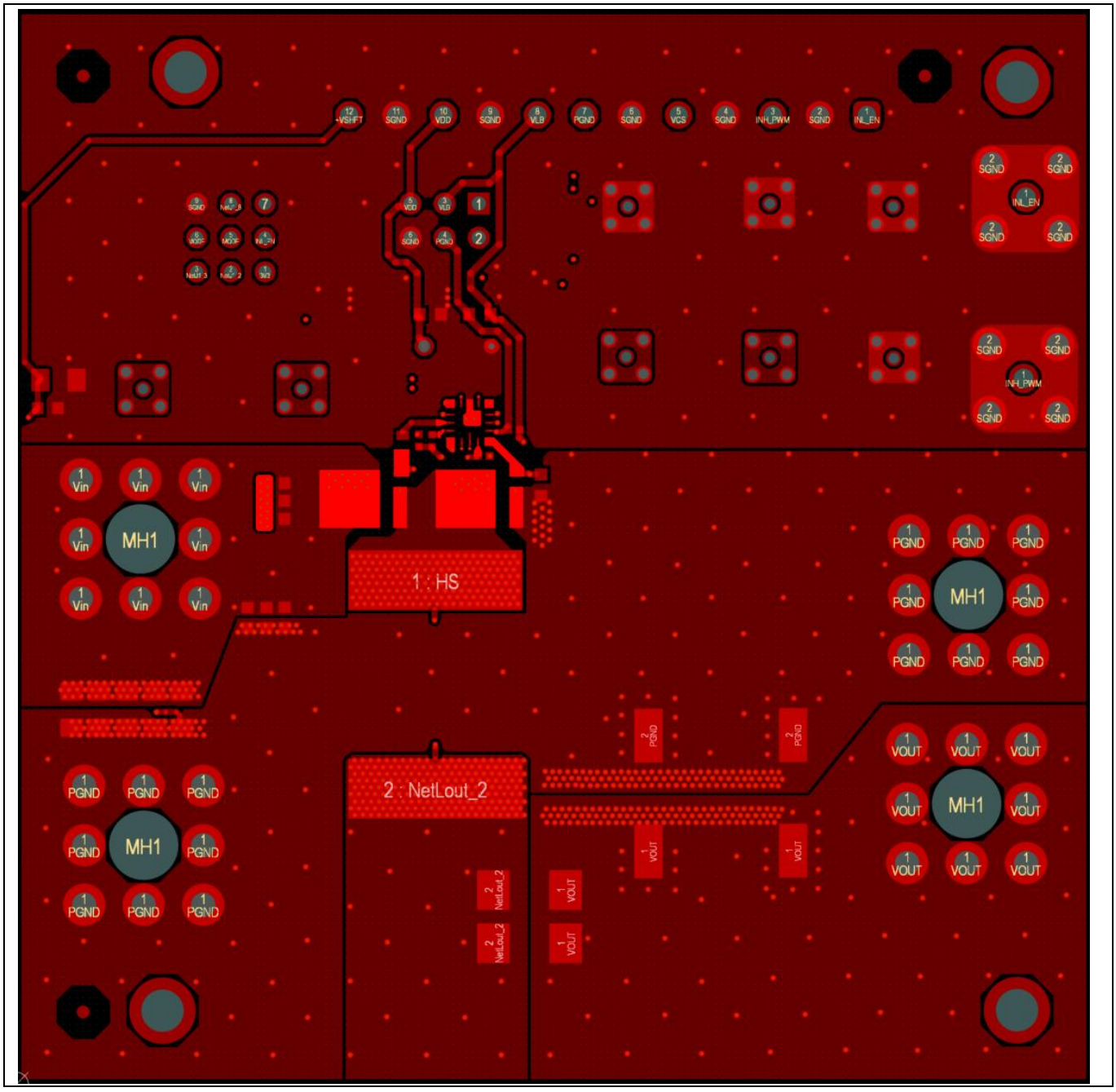

Figure 16 Top layer – Layer 1

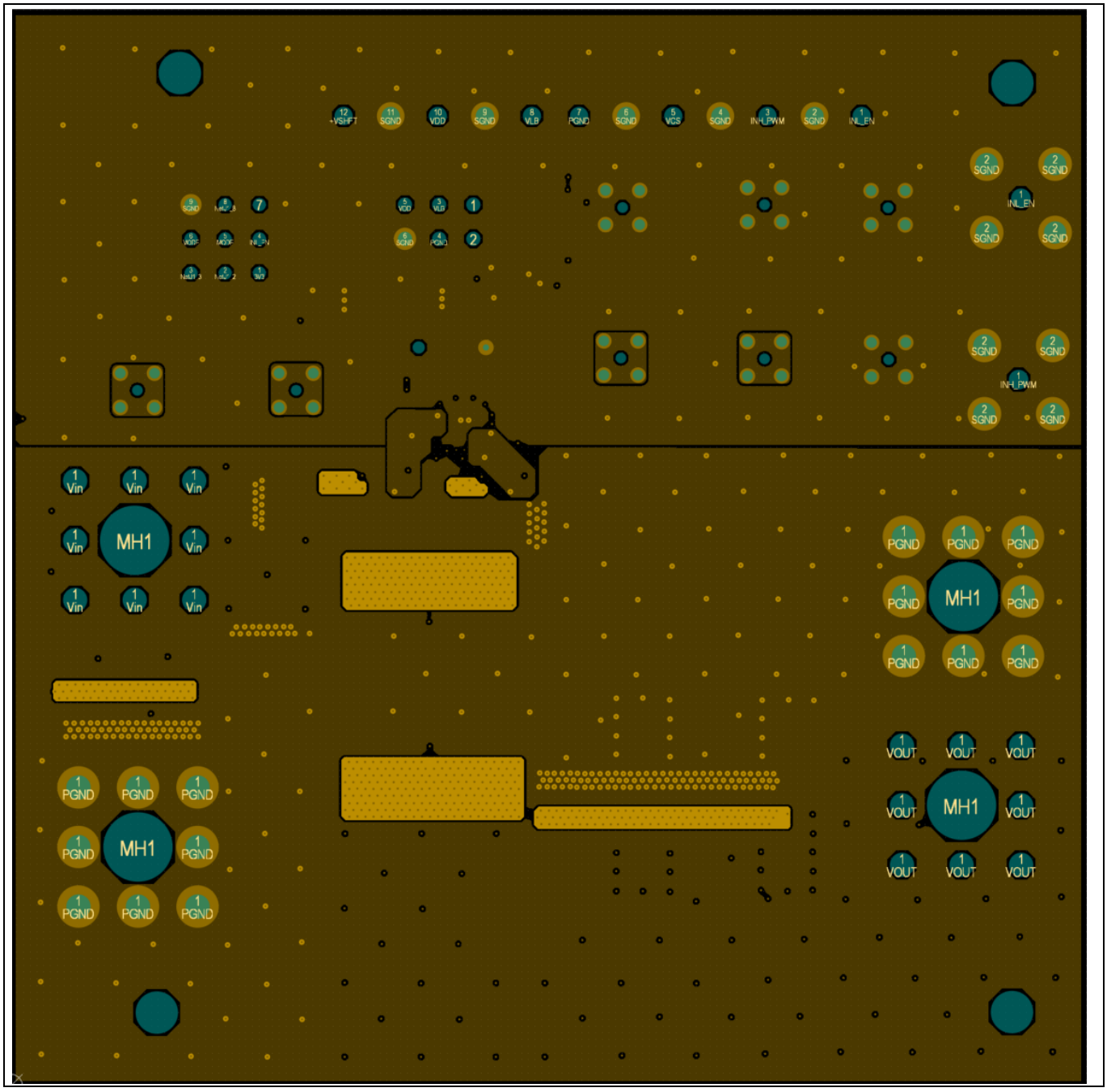

Figure 17 Layer 2

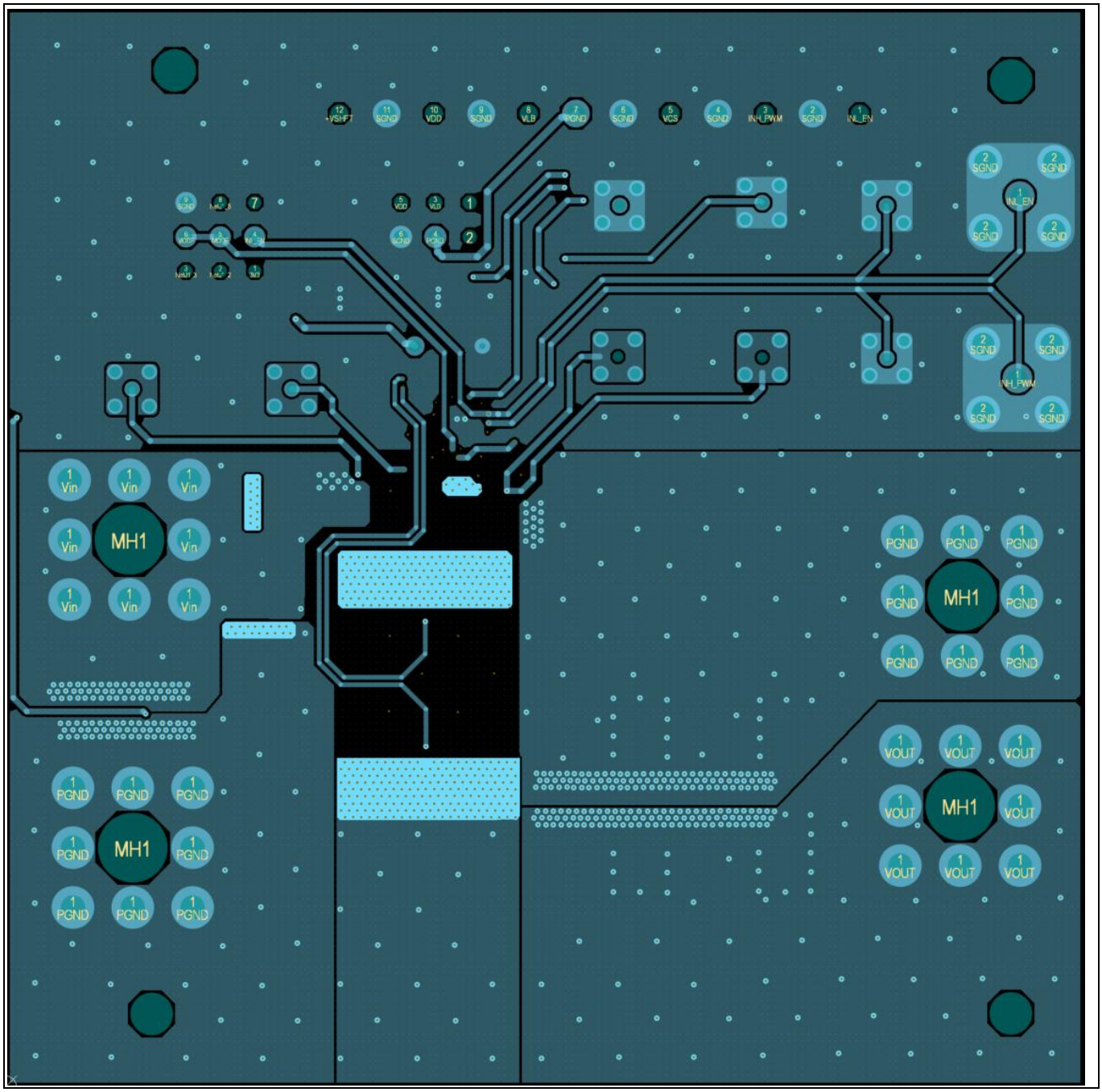

Figure 18 Layer 3

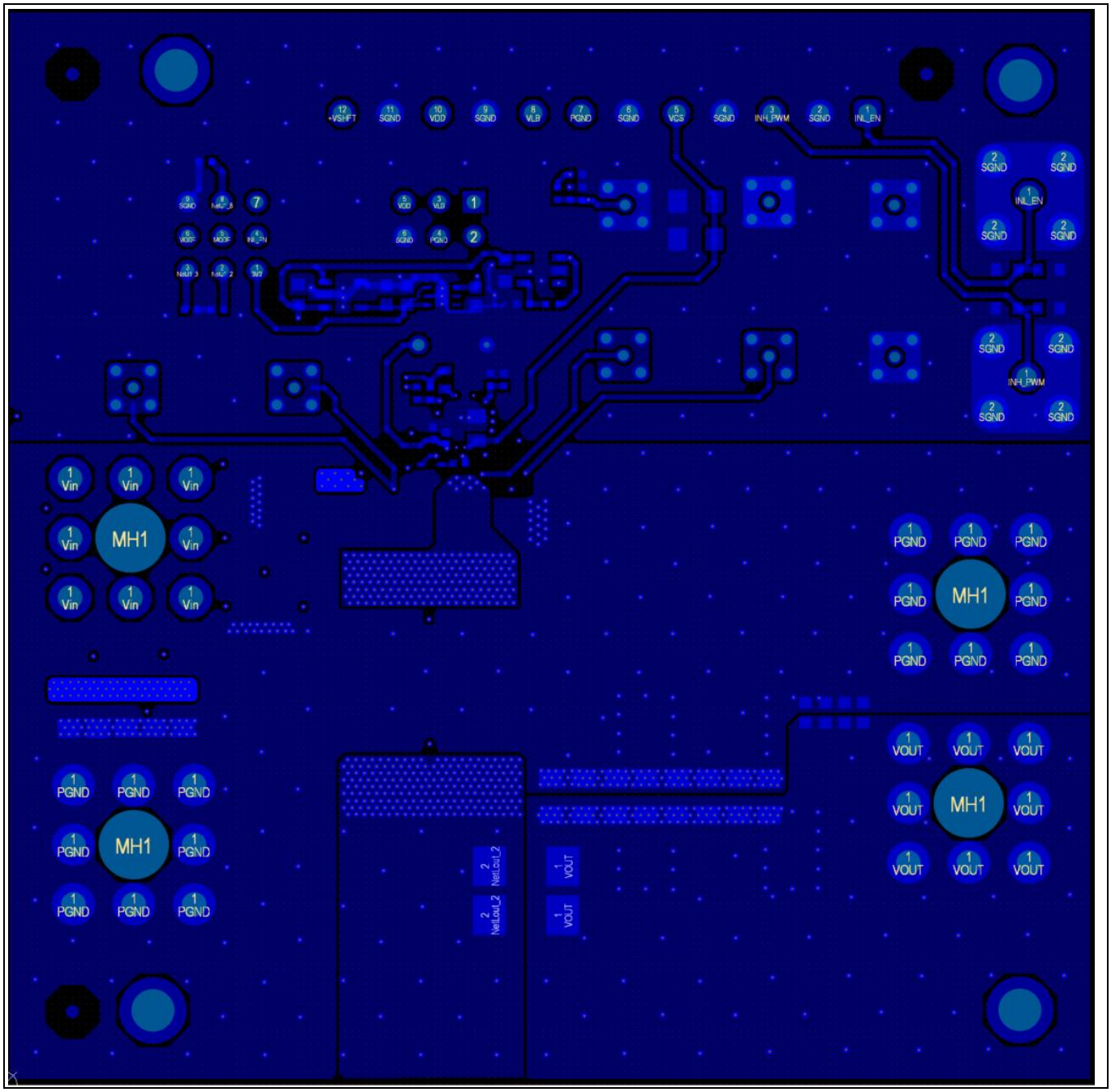

Figure 19 Bottom layer – Layer 4

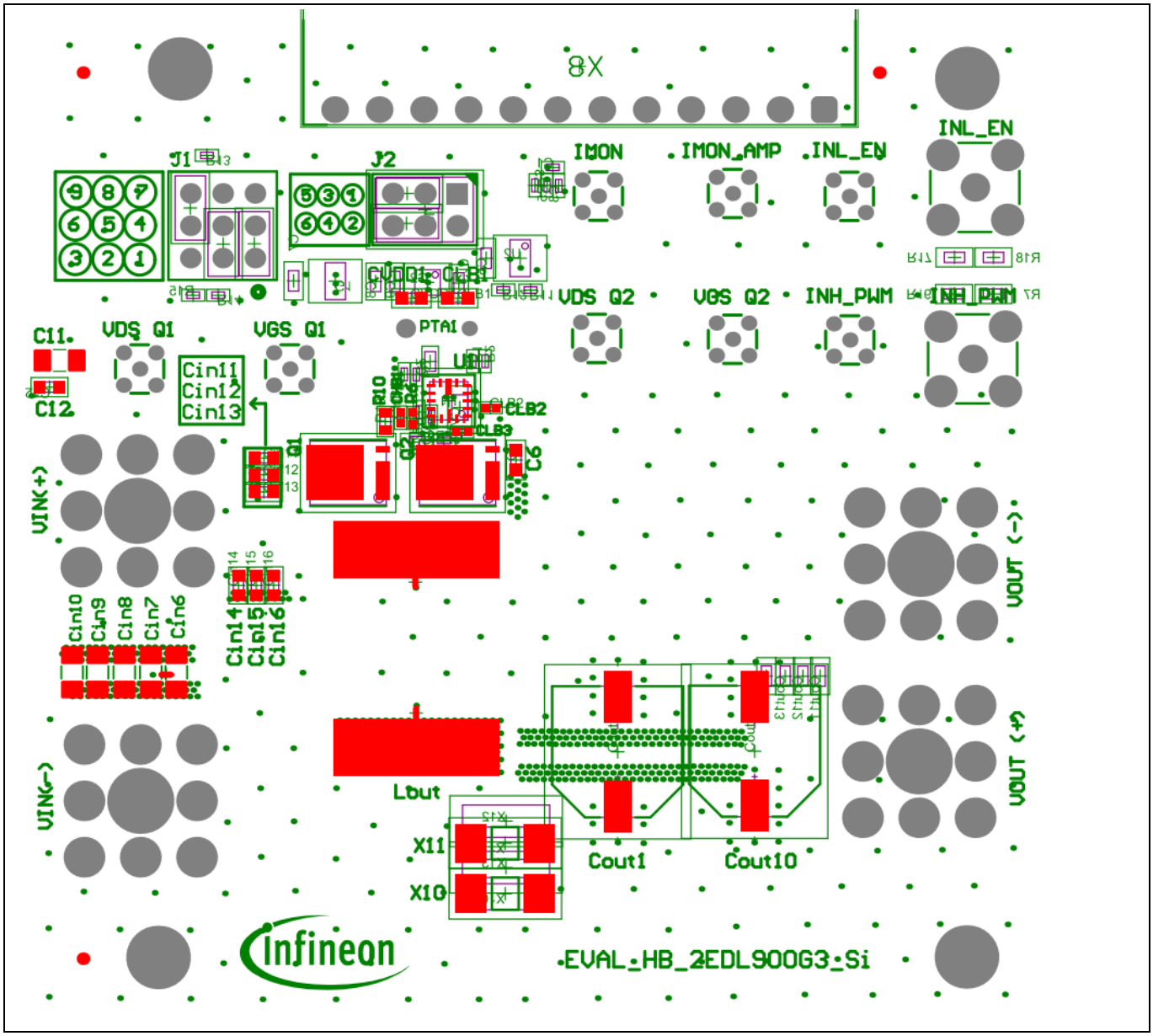

Figure 20 Component assembly – top side

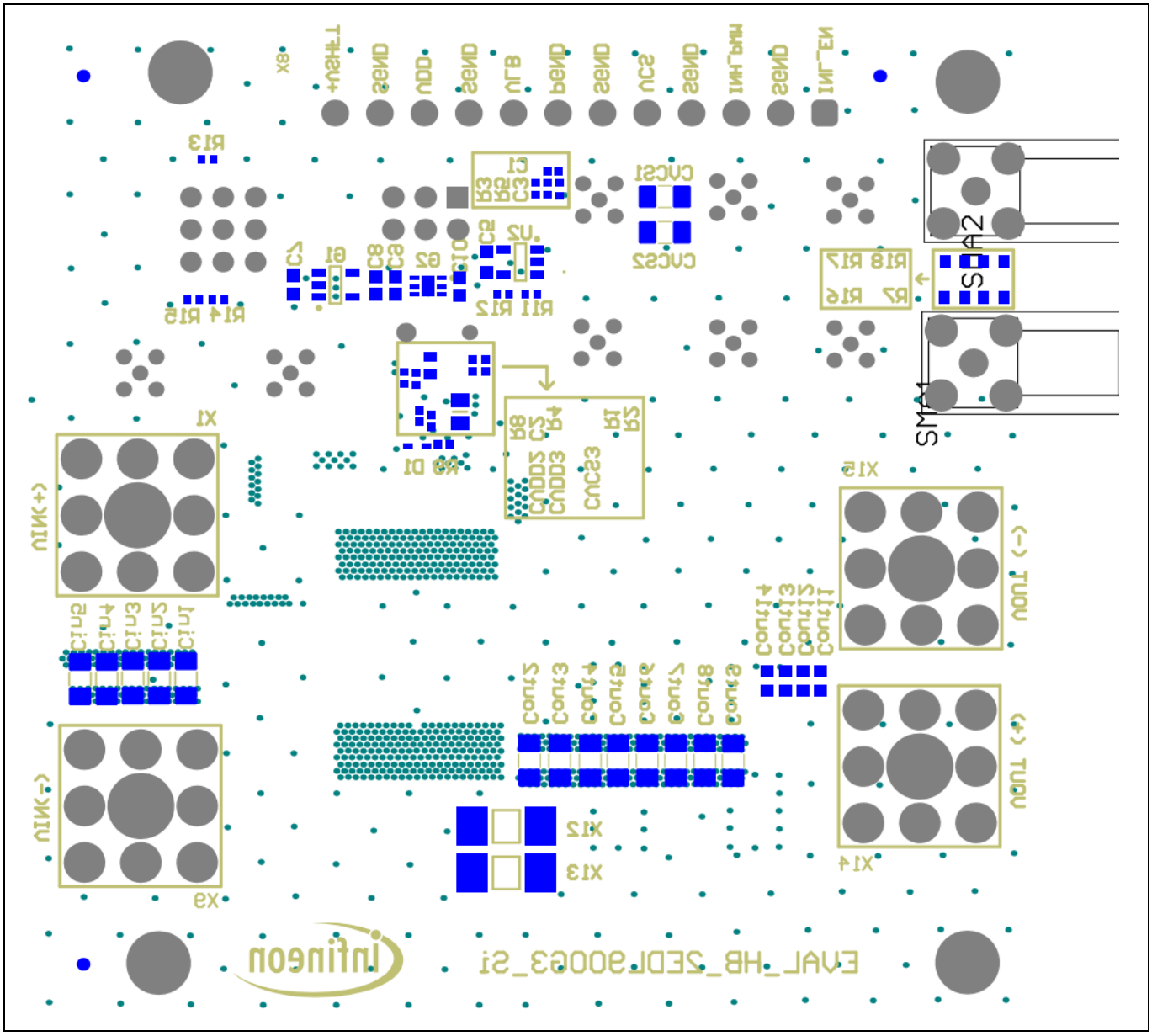

Figure 21 Component assembly – bottom side

5.3 Bill of materials

Table 12 BOM List

Quantity	Designator	Value	Manufacturer	Manufacturer part number/ Manufacturer order number
1	C1	100 nF	Murata	GRM152R61A104ME19D
1	C2	220 nF	TDK Corporation	CGA2B3X7R1E224K050BB
1	C3	150 pF	TDK	C1005C0G1H151G050BA
1	C5	100 nF	KEMET	C0603C104J3RACTU
1	C7	1 µF	Taiyo Yuden	MSASU168AB7105KTNA01
3	C8, C9, C10	1 µF	TDK Corporation	C1608X8L1C105K080AC
21	C11, Cin1, Cin2, Cin3, Cin4, Cin5, Cin6, Cin7, Cin8, Cin9, Cin10, Cout2, Cout3, Cout4, Cout5, Cout6, Cout7, Cout8, Cout9, CVCS1, CVCS2	4.7 µF	Murata	GRM31CC72A475ME11L
11	C12, Cin11, Cin12, Cin13, Cin14, Cin15, Cin16, Cout11, Cout12, Cout13, Cout14	220 nF	Taiyo Yuden	MCASH168SC7224KTCA01
1	CHB1	1 µF	MuRata	GRM155C81E105KE11D
2	CLB1, CVDD1	10 µF	Murata	GRM188R61E106MA73D
2	CLB2, CVDD2	2.2 µF	Murata	GRM155R61E225KE11
2	CLB3, CVDD3	100 nF	Murata	GRM155R71E104ME14D
2	Cout1, Cout10	68 µF	Nichicon	PCR1K680MCL1GS
1	CVCS3	100 nF	Murata	GRM21BR72A104JAC4K
1	D1		Onsemi or STMicroelectronics	1SS400T1G or BAT41KFILM
1	G1		ON Semiconductor	NCP718ASN330T1G
1	G2		Texas Instruments	LP5912-1.2DRVT
1	J1		Samtec	TSW-103-07-G-T
1	J2		Samtec	TSW-103-07-L-D
1	Lout	3.3 µH	Vishay	IHLP7575GZER3R3M5A
8	MMCX1, MMCX2, MMCX3, MMCX4, MMCX5, MMCX6, MMCX7, MMCX8	MMCX vertical jack	Würth Elektronik	66012002111503
1	Q1		Infineon Technologies	ISC031N08NM6SCATMA1

Quantity	Designator	Value	Manufacturer	Manufacturer part number/ Manufacturer order number
1	Q2		Infineon Technologies	ISC016N08NM8SC
1	R2	100k	Yageo	RC0402FR-07100KL
2	R3, R8	1k	Panasonic	ERJ-2RKF1001X
1	R4	560R	Vishay	CRCW0603560RFKEAC
1	R5	2k	Vishay	CRCW04022K00FKED
1	R6	0R	Yageo	RC0402JR-070RL
1	R10	3R	Vishay	CRCW06033R00FKEAC
2	R11, R12	22.6k	Vishay	CRCW040222K6FKED
1	R13	39k	Vishay	CRCW040239K0FKED
1	R14	66.5k	Vishay	CRCW040266K5FKED
1	R15	22k	Vishay	CRCW040222K0FKED
4	S1, S2, S3, S4		RS PRO	914-1510
4	S5, S6, S7, S8		Wuerth Elektronik	970150321
4	S9, S10, S11, S12		Wuerth Elektronik	971300321
2	SMA1, SMA2		Würth Elektronik	60311002111526
1	U1		Infineon Technologies	2EDL900G3
1	U2A		Texas Instruments	TLV172IDBVT
4	X1, X9, X14, X15		Würth Elektronik	74655095R
6	X2, X3, X4, X5, X6, X7		Würth Elektronik	691363110002
1	X8		Würth Elektronik	691322110012
4	X10, X11, X12, X13		Keystone Electronics Corp.	5102TR
5	X16, X17, X18, X19, X20		Würth Elektronik	609002115121

6 System performance

6.1 Test conditions

- VIN = 48 V
- D = 25%
- Maximum load current = 15 A
- Fsw = 200 kHz
- VDD and VLB = 10 V
- MODE: Tested at single PWM and HI/LI input modes
- CONFIGURATION: Non-voltage-level-shifted and voltage-level-shifted

Note: In voltage-level-shifted configuration, +VSHFT to SGND = +10 V.

6.2 Test waveforms

6.2.1 Non-voltage-level-shifted configuration

6.2.1.1 Tri-state single PWM mode

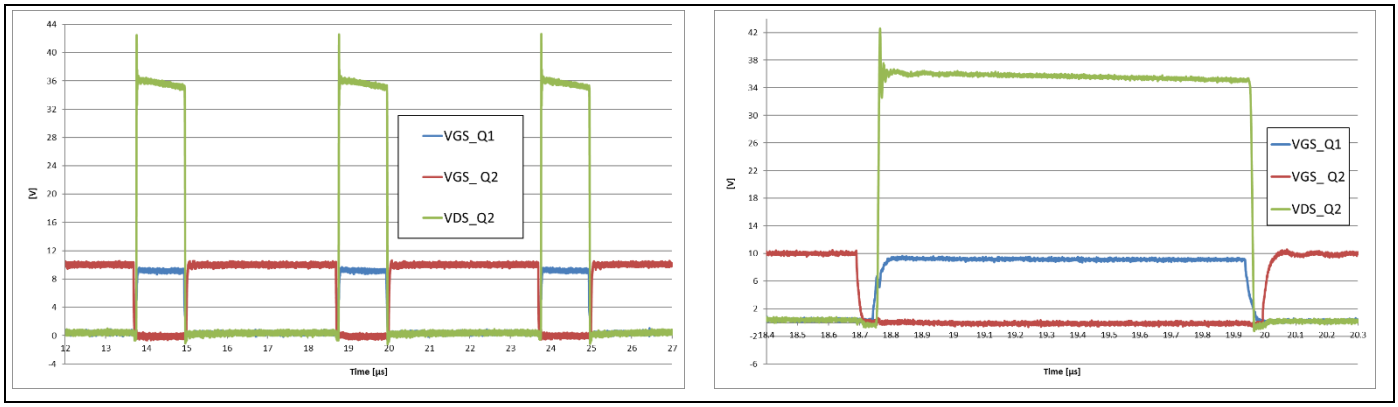

Figure 22 Gate-to-source voltage of Q1, Q2 and drain-to-source voltage of Q2 at Vin = 36 V, 15 A load current

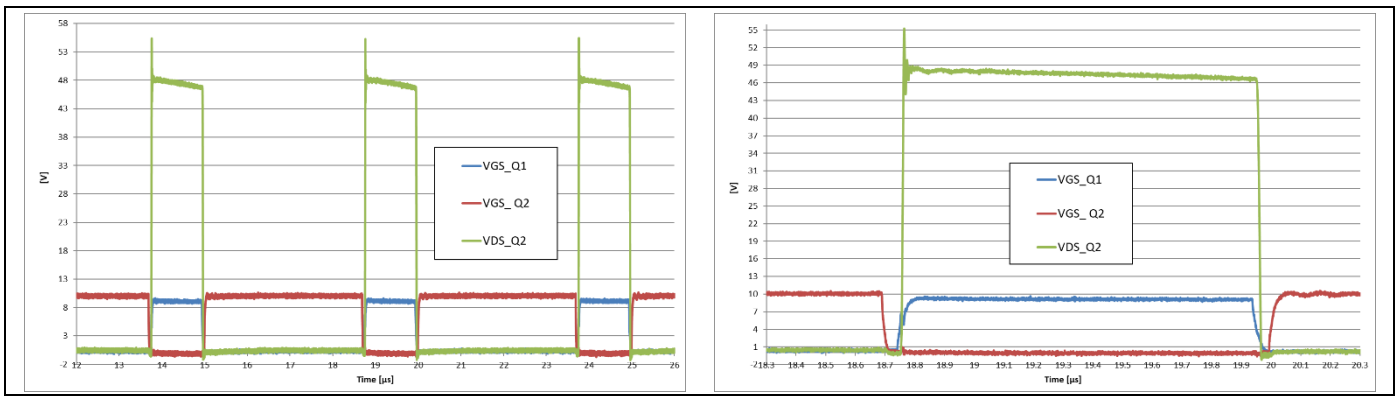

Figure 23 Gate-to-source voltage of Q1, Q2 and drain-to-source voltage of Q2 at Vin = 48 V, 15 A load current

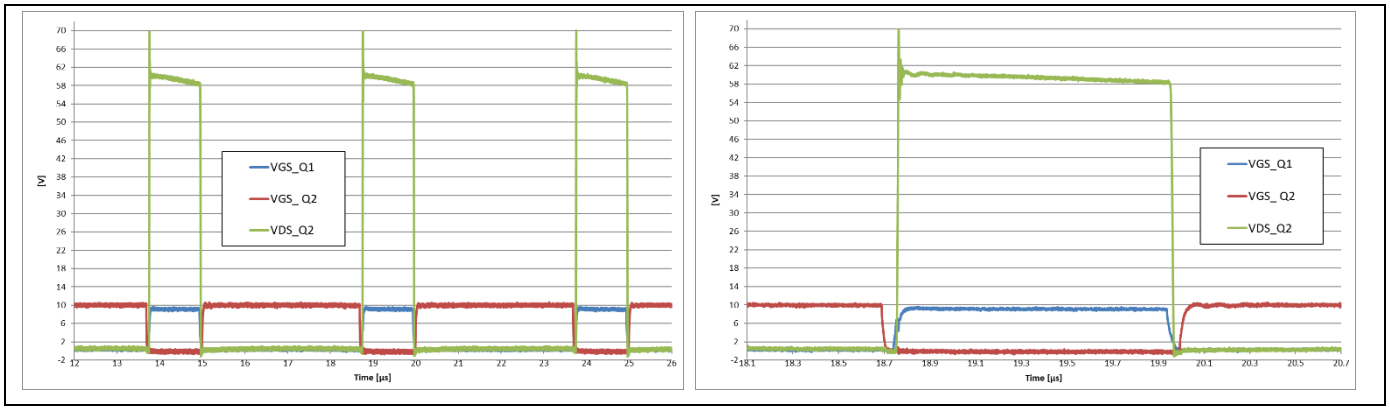

Figure 24 Gate-to-source voltage of Q1, Q2 and drain-to-source voltage of Q2 at Vin = 60 V, 15 A load current

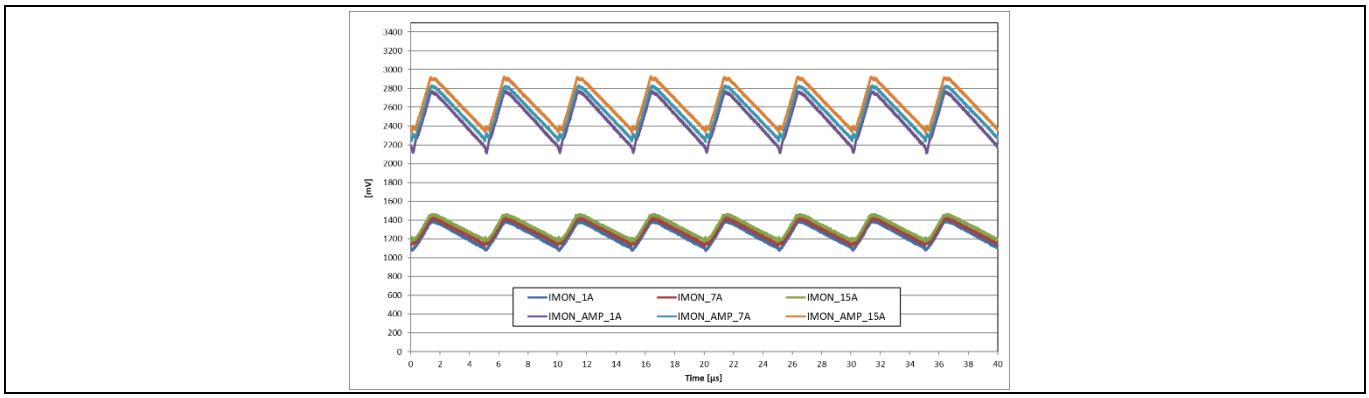

Figure 25 IMON and IMON_AMP signal at Vin = 36 V with different load currents

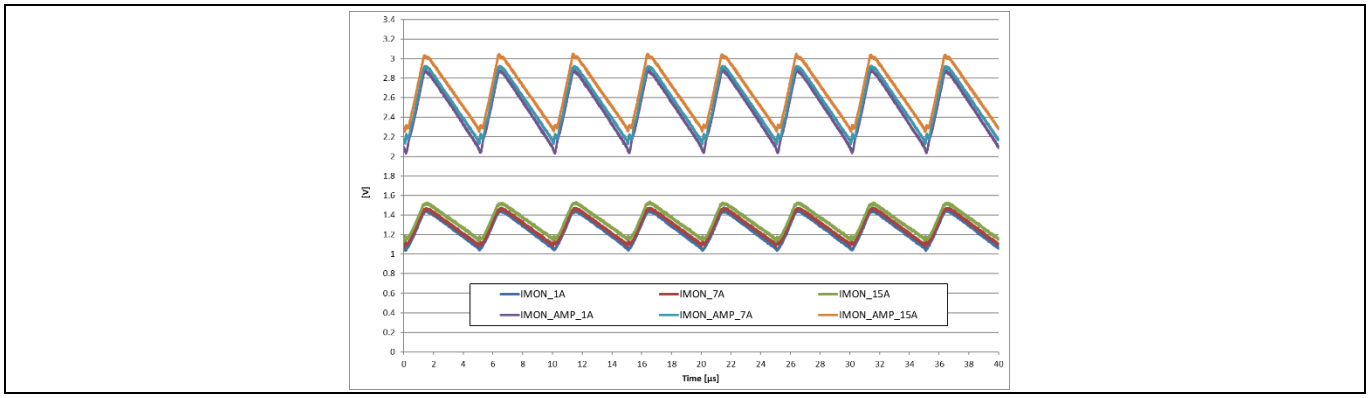

Figure 26 IMON and IMON_AMP signal at Vin = 48 V with different load currents

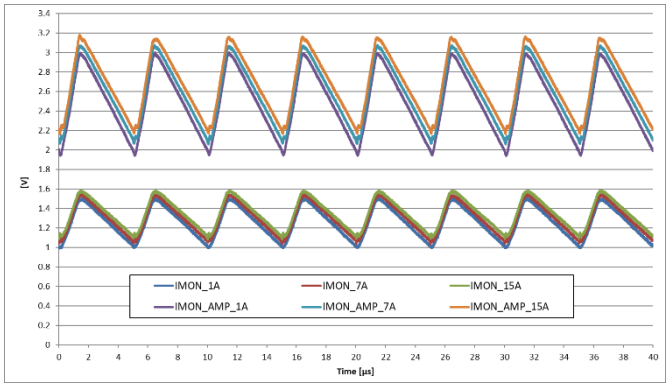

Figure 27 IMON and IMON_AMP signal at Vin = 60 V with different load currents

6.2.1.2 HI/LI input mode

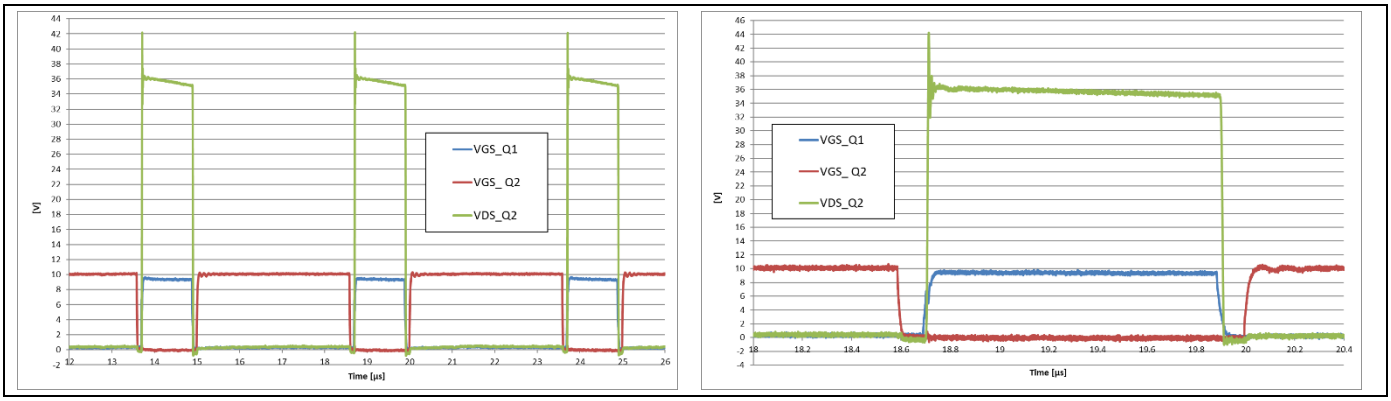

Figure 28 Gate-to-source voltage of Q1, Q2 and drain-to-source voltage of Q2 at Vin = 36 V, 15 A load current

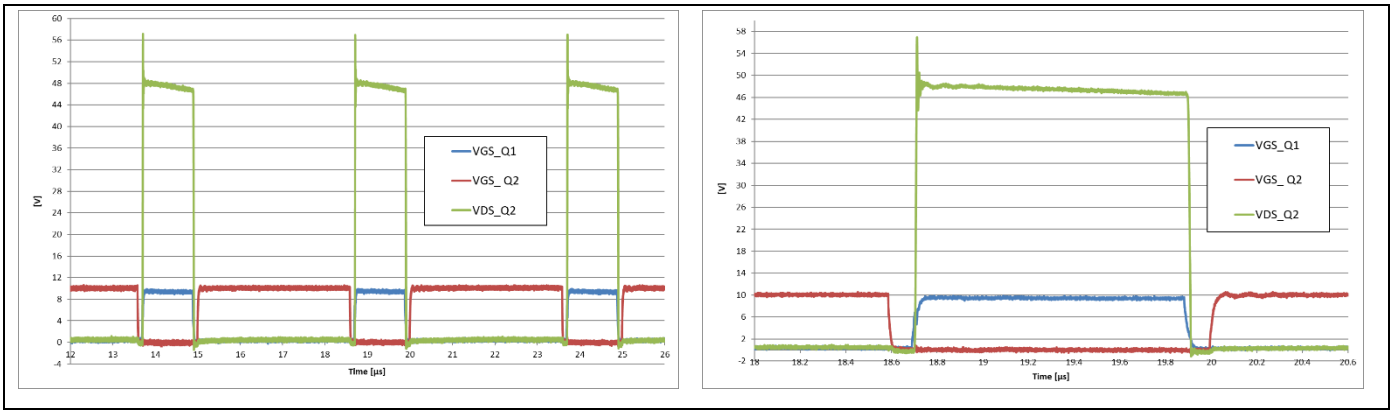

Figure 29 Gate-to-source voltage of Q1, Q2 and drain-to-source voltage of Q2 at Vin = 48 V, 15 A load current

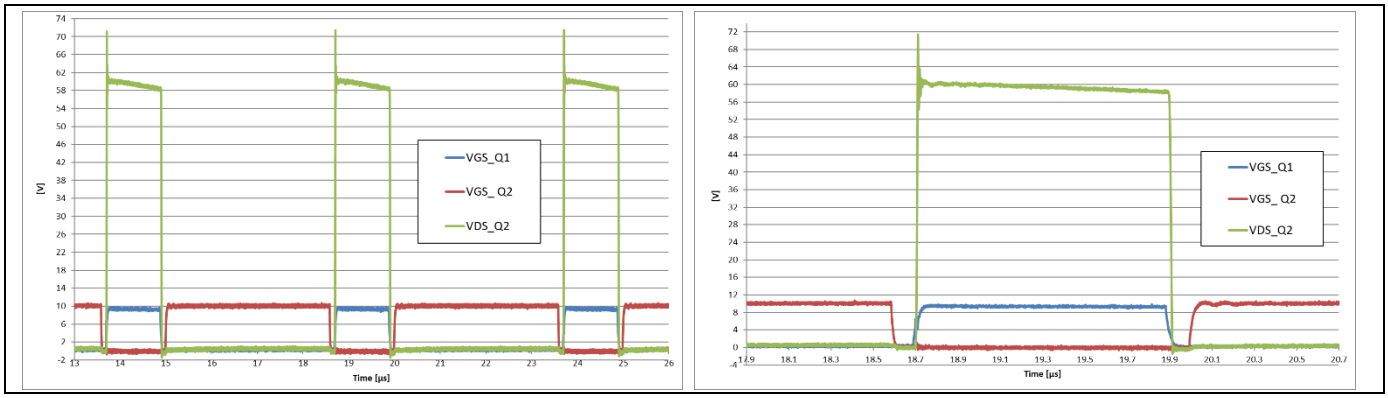

Figure 30 **Gate-to-source voltage of Q1, Q2 and drain-to-source voltage of Q2 at Vin = 60 V, 15 A load current**

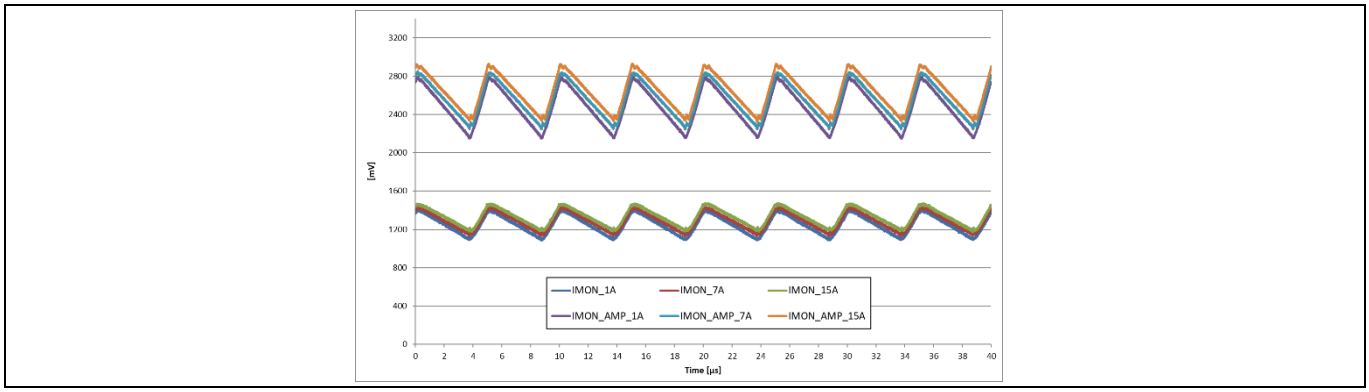

Figure 31 **IMON and IMON_AMP signal at Vin = 36 V with different load currents**

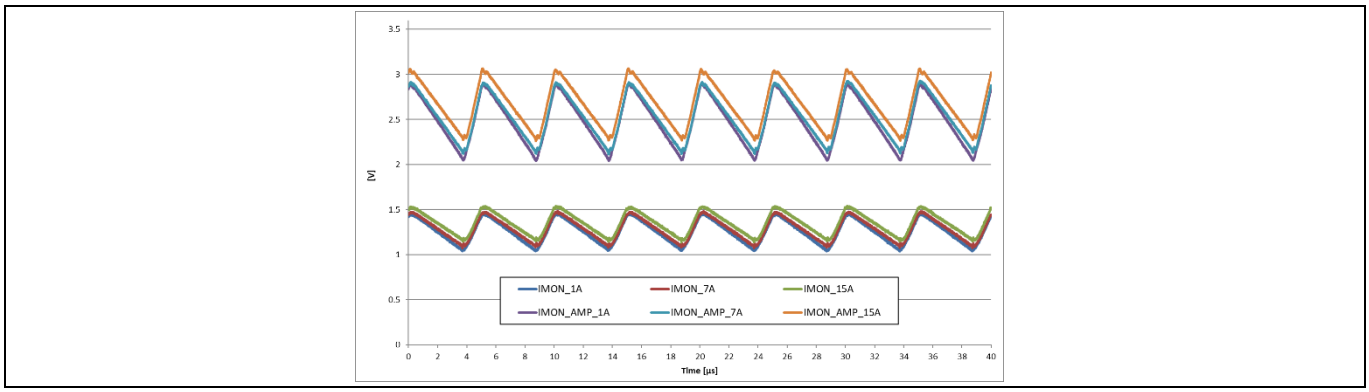

Figure 32 **IMON and IMON_AMP signal at Vin = 48 V with different load currents**

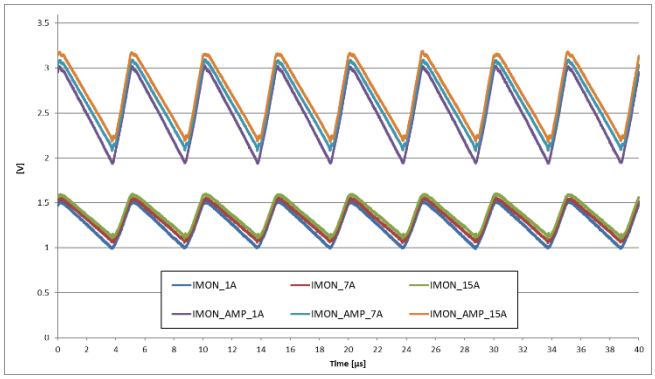

Figure 33 IMON and IMON_AMP signal at Vin = 60 V with different load currents

6.2.2 Voltage-level-shifted configuration

Note: In voltage-level-shifted configuration, the VDS _Q2 waveform is not included. Waveforms focus on the two output channels switching transition plus the IMON and IMON_AMP signals.

6.2.2.1 Tri-state single PWM mode

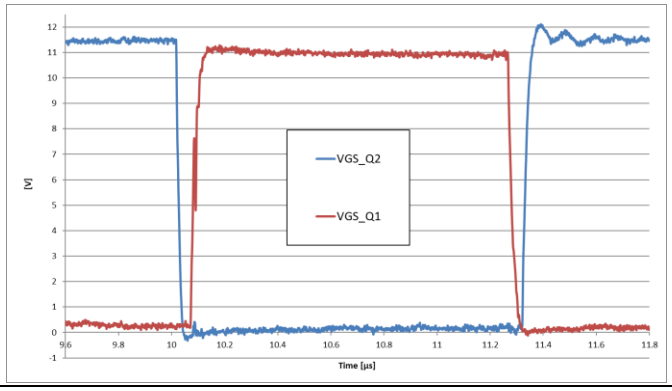

Figure 34 VGS_Q1 and VGS_Q2 at Vin = 36 V, 15 A load current

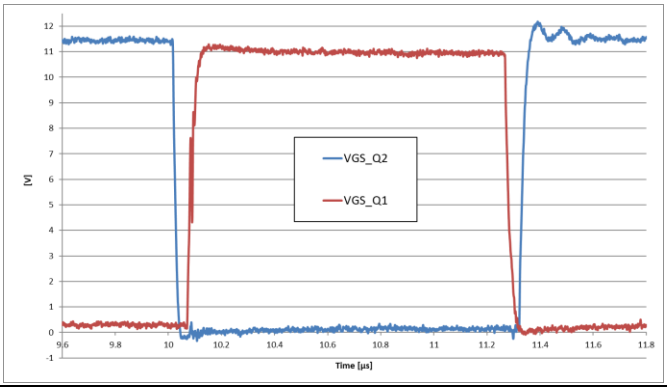

Figure 35 VGS_Q1 and VGS_Q2 at Vin = 48 V, 15 A load current

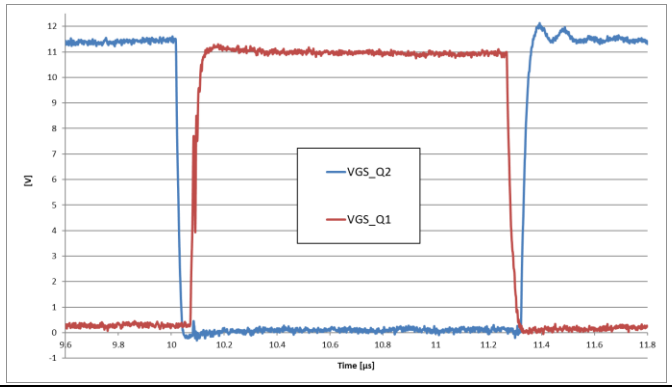

Figure 36 VGS_Q1 and VGS_Q2 at Vin = 60 V, 15 A load current

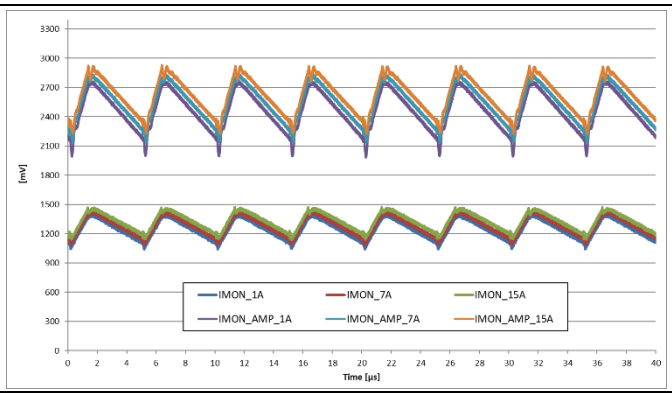

Figure 37 IMON and IMON_AMP signal at Vin = 36 V with different load currents

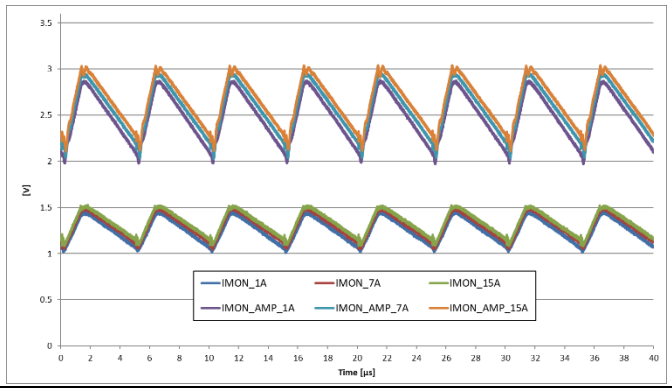

Figure 38 IMON and IMON_AMP Signal at 48 Vin with different load currents

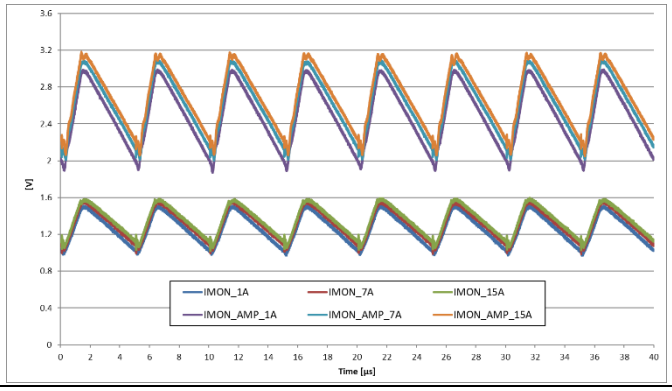

Figure 39 IMON and IMON_AMP Signal at Vin = 60 V with different load currents

6.2.2.2 HI/LI input mode

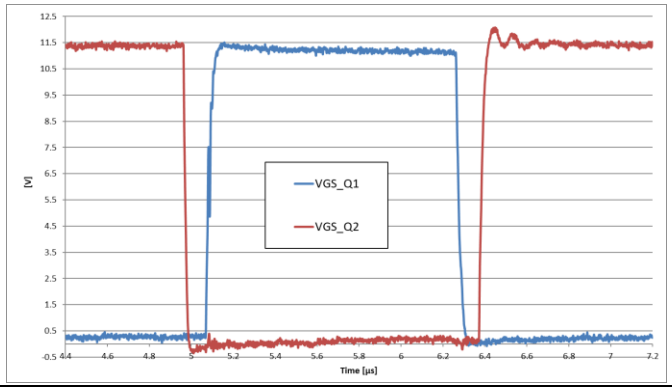

Figure 40 VGS_Q1 and VGS_Q2 at Vin = 36 V, 15 A load current

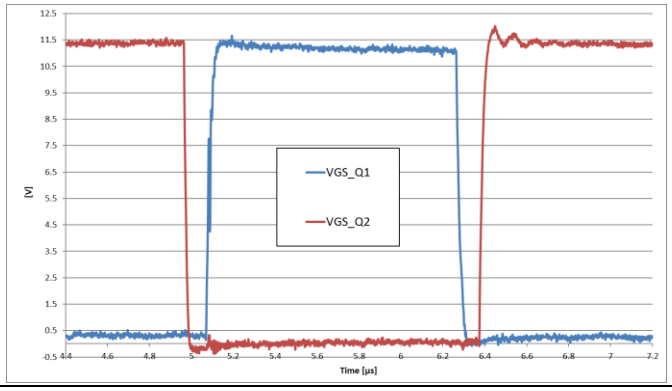

Figure 41 VGS_Q1 and VGS_Q2 at Vin = 48 V, 15 A load current

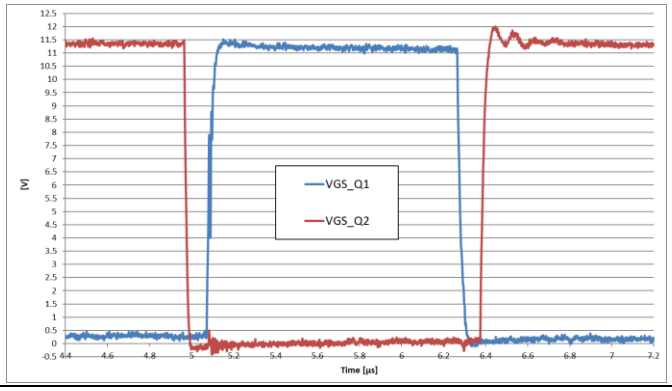

Figure 42 VGS_Q1 and VGS_Q2 at Vin = 60 V, 15 A load current

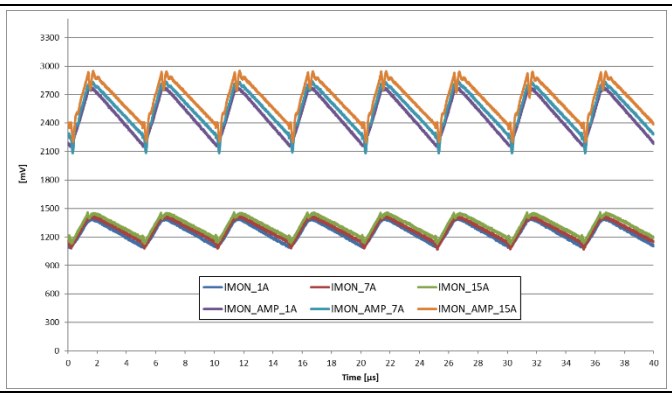

Figure 43 IMON_AMP signal at Vin = 36 V with different load currents

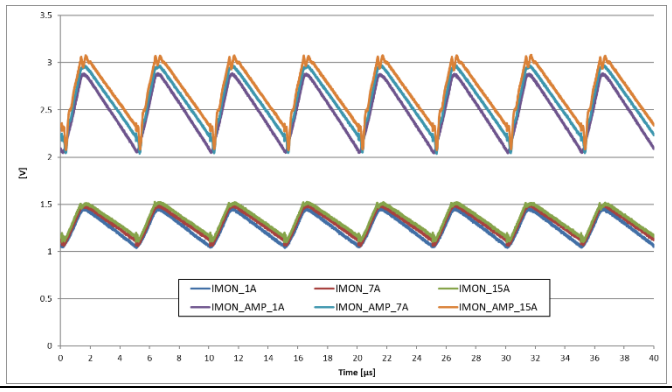

Figure 44 IMON_AMP signal at Vin = 48 V with different load currents

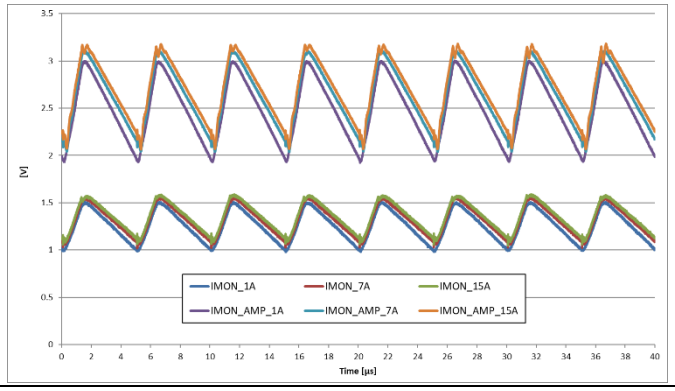

Figure 45 IMON_AMP signal at Vin = 60 V with different load currents

Related resources

- Gate driver ICs
- EVAL_HB_2EDL900G3_Si
- Developer Community forum

References

[1] Infineon Technologies AG: EiceDRIVER™ 2EDL900G3; Available online

Revision history

Document revision	Date	Description of changes
V 1.0	2026-04-17	Initial release

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