100 W AI server AUX power supply using CoolSET™ SiP ICE186LM-V101

EVAL_100W1S_ZVS_ICE186LM

About this document

Scope and purpose

This engineering report describes the EVAL_100W1S_ZVS_ICE186LM evaluation board for a flyback converter with an isolated 12 V, 8.33 A output using the latest Infineon CoolSET™ ICE186LM-V101 system-in-package (SiP) ZVS flyback integrated solution.

Highlights of this power supply:

- High efficiency to leverage to help the server efficiency requirements
- Small form factor to fit to the tiny space in the AI server power supply
- Simplified circuitry with high-level integration of power control and protection features
- Auto-restart protection scheme to minimize interruption and enhance the end user experience
- Zero voltage switching (ZVS) technology to boost efficiency performance

Intended audience

This document is intended for SMPS design/application engineers, students, etc., who wish to design a highly efficient auxiliary power supply for AI servers with high power density. Specifically, this guide is intended for those who wish to evaluate the performance of CoolSET™ ICE186LM-V101 system-in-package and to modify to their final auxiliary power board.

V 1.0
2026-02-20

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1 Introduction

This engineering report describes the EVAL_100W1S_ZVS_ICE186LM evaluation board designed in a zero-voltage switching (ZVS) quasi-resonant (QR) flyback converter using CoolSET™ ICE186LM-V101 system-in-package (SiP), Infineon's first fully integrated controller. The evaluation board provides 100 W output at 12 V and 8.33 A, with an input range of 300 VDC to 420 VDC, tapped from the PFC output of the system. The evaluation board can achieve 93.2% peak efficiency and 93 W/in^3 power density.

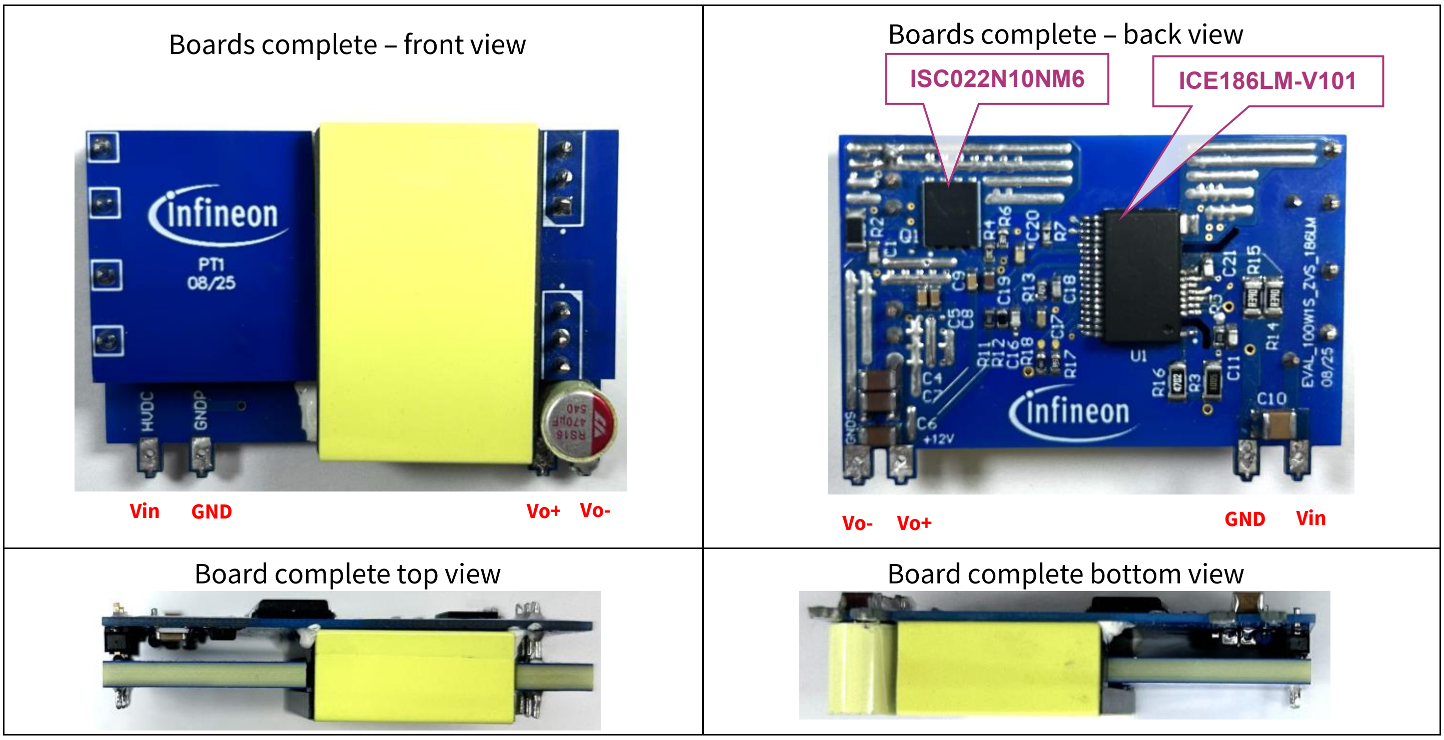
The CoolSET™ ICE186LM-V101 is SIP are ideally targeted for auxiliary power supplies for AI servers. The SiP integration includes an 800 V CoolMOS™ P7 MOSFET, primary and a secondary controller, and isolated communication. An advanced PWM switching pattern forces a zero-voltage switching (ZVS) quasi-resonant (QR) operation, reducing the turn-on switching losses and optimizing the EMI signature. A comprehensive set of protection features supports ease of design-in.

The board assembly comprises of two boards: control board and the planar transformer board. The board is targeted to deliver the power conversion only. The input and output power storage capacitors are to be supported by the main power supply board. The 12 V output supplies power is to supply the gate drive circuit, main power controller, auxiliary controllers and system hardware such as cooling fans.

Table 1 lists the AI server system requirements for auxiliary power supply and the Infineon solution using ICE186LM-V101.

Table 1 **General AI server supply requirement and reference design solution**

	General system requirement	**Reference design solution – ICE186LM-V101**
1	High efficiency to meet AI server efficiency requirements	Primary zero-voltage switching and secondary optimal synchronous rectifier (SR) control
2	Simplified circuitry with high-level integration	Primary 800 V MOSFET, primary and secondary controller, and communication integrated in a DSO-27 package
3	Minimize interruption to enhance user experience	All protections are defined to enter auto-restart mode

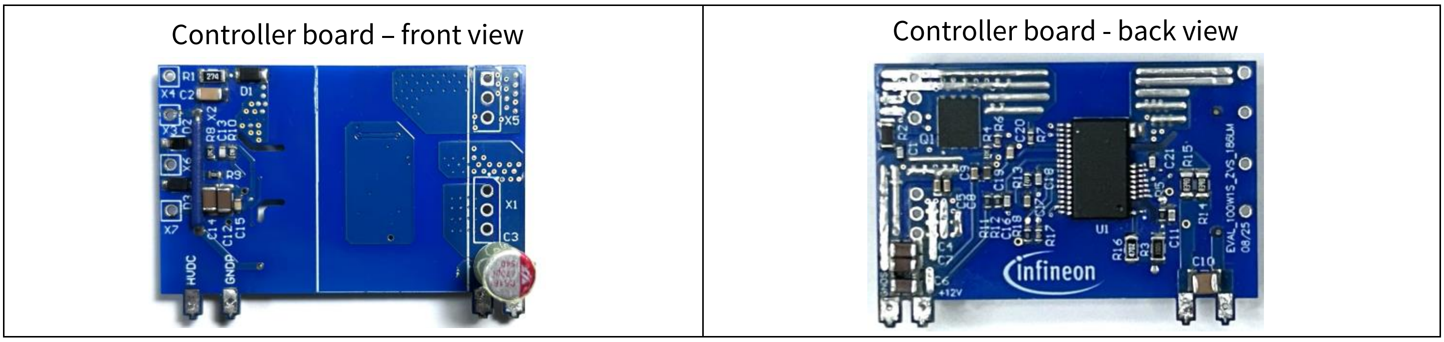

Boards complete – front view

Boards complete – back view

Board complete top view

Board complete bottom view

Figure 1 EVAL_100W1S_ZVS_ICE186LM board complete


Controller board – front view

Controller board - back view

Figure 2 EVAL_100W1S_ZVS_ICE186LM - control board


Planar transformer board – front view

Planar transformer board – back view

Figure 3 EVAL_100W1S_ZVS_ICE186LM - planar transformer board

2 Test setup

When testing the EVAL_100W1S_ZVS_ICE186LM board, add the following capacitors:

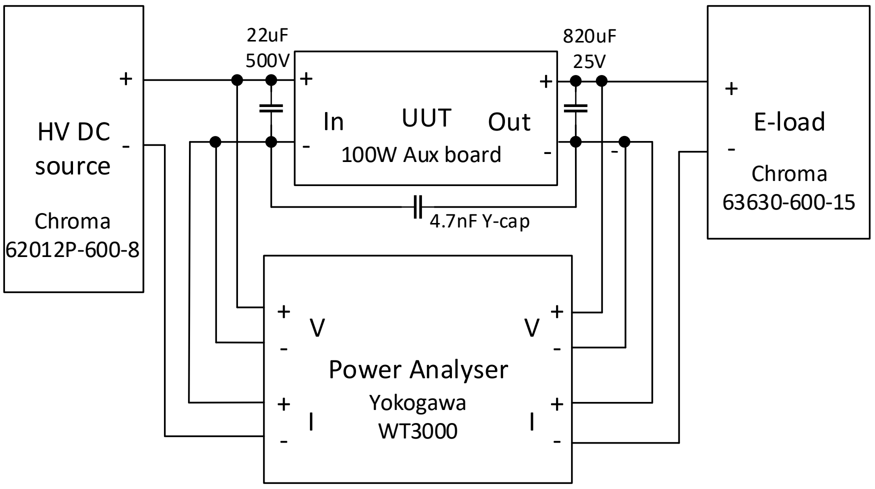
- At least one 22 µF 500 V input capacitor and a 820 µF 25 V output capacitor to the input and output terminals of the evaluation board
- One 4.7 nF Y-capacitor across the input ground and the output ground

Set up a cooling fan to blow to the board to avoid the board entering overtemperature protection during 100W load application because the copper area for both the primary side power switch (embedded in the ICE186LM-V101) and the secondary-side SR power switch are not sufficient for efficient heat transfer. When the load drops to 50%, the cooling fan is not needed

The EVAL_100W1S_ZVS_ICE186LM board is installed in a test jig for testing. The input is connected to a DC supply while the output is connected to an electronic load. The voltage and current are measured with a power analyser.

Equipment:

- Power analyser: Yokogawa WT3000
- DC power supply: Chroma 62012P-600-8
- Electronic load: Chroma 63630-600-15

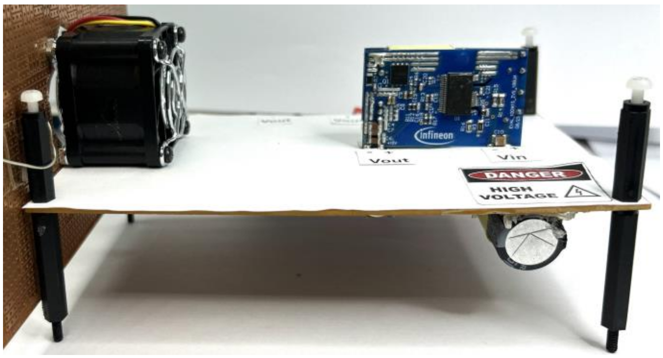


100W AI server board test setup diagram

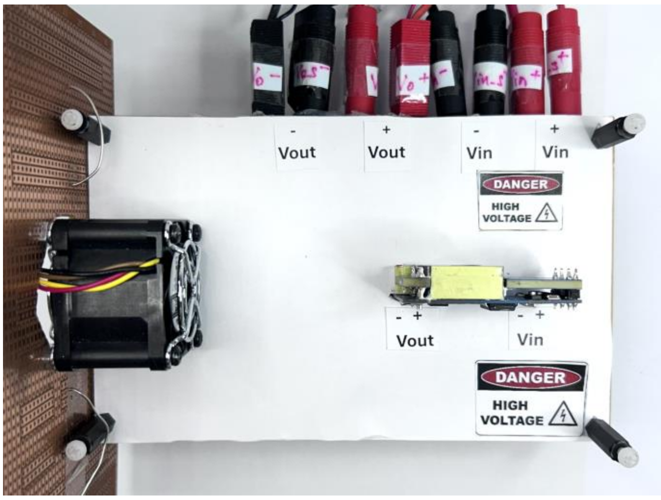
Figure 4 Test equipment connection diagram

Test setup:

- Cooling fan: SamAce40 9GA0412P3H01 placed at 6 cm from the UUT board
- Added external components: 22 µF 500 V capacitor for input, 820 µF 25 V capacitor for output and 4.7 nF Y1 across input and output negative



Side view



Top view

Figure 5 **Test setup photos**

3 Evaluation board specifications

Table 2 Specifications of EVAL_100W1S_ZVS_ICE186LM

Description	Symbol	Min.	Typ.	Max.	Units	Comments
Input Voltage	V_{IN}	300	390	420	VDC	For 100W
	V_{IN}	100	-	299	VDC	For 50W
Output Voltage	V_{OUT}	12			V	–
Output Current/output power	I_{OUT} / P_{OUT}	8.33 / 100			A/W	V_{IN} = 300 VDC ~ 420 VDC With forced convection
	I_{OUT}/ P_{OUT}	4.16 / 50			A/W	V_{IN} =100 VDC ~ < 299 VDC Natural cooling
Output voltage accuracy	–	< ±5%			%	–
Ambient temperature	T_{amb}	–20	–	50	°C	Forced convection, sea level
Size	–	48 × 30 × 12.3			mm^3	L × W × D
Safety distance between primary and secondary side	–	> 10			mm	–

Note: The table above represents the minimum acceptable performance of the design. Actual measurement results are listed in the test results section.

4 Circuit diagram

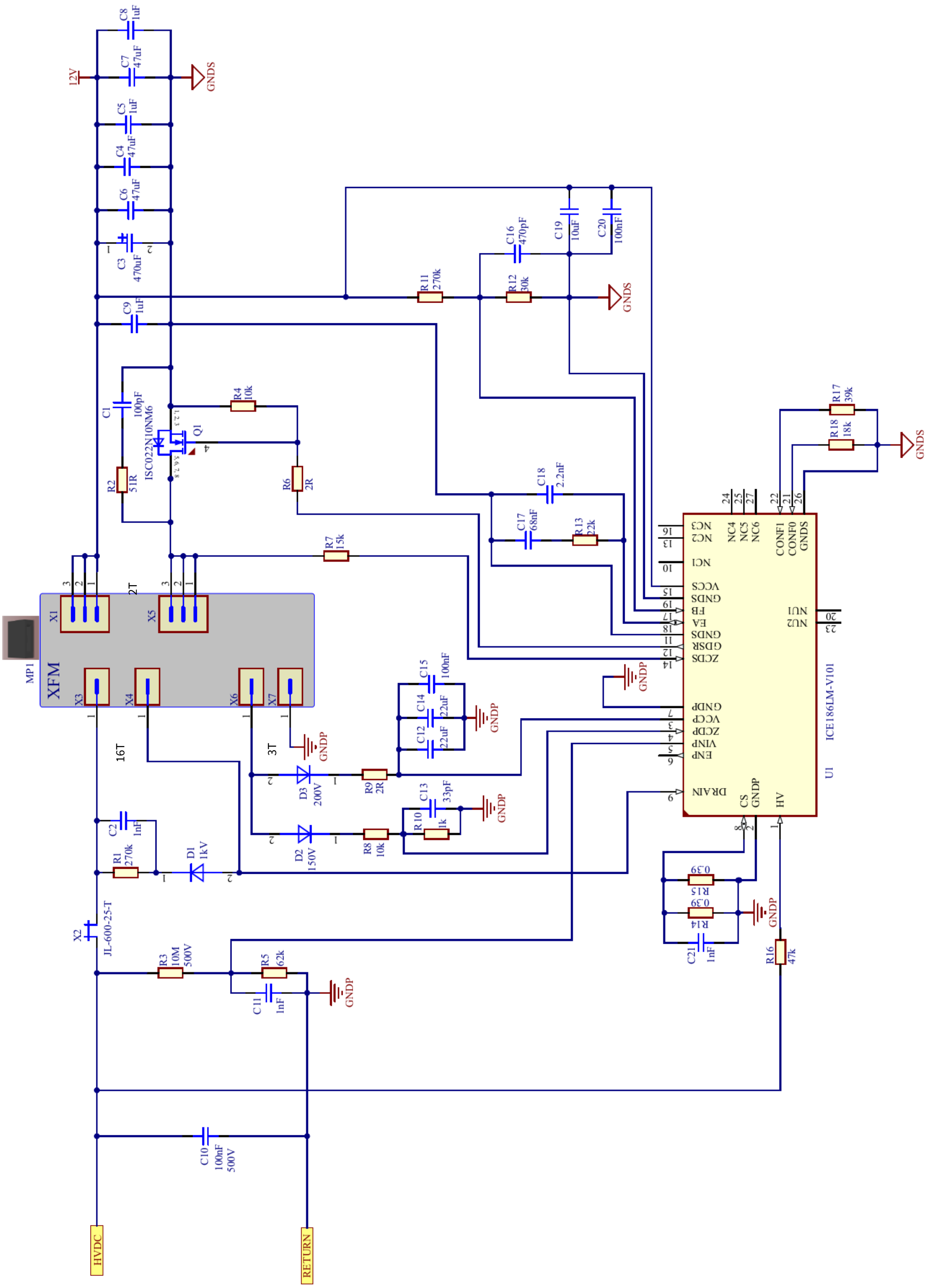


Figure 6 Schematic of EVAL_100W1S_ZVS_ICE186LM

5 Circuit description

This section briefly describes the reference design circuit by different functional blocks. For details of the design procedure and component selection for the flyback circuitry, check the IC datasheet [1] and design guide [2].

5.1 Input filter

The input circuit includes a filter capacitor (C10) because the input voltage is taken from the main power PFC output.

5.2 CoolSET™ SiP power stage

The flyback converter power stage consists of a power transformer, primary power MOSFET, secondary synchronous rectifier (SR) MOSFET, secondary output capacitors, and filtering component if possible.

Primary and secondary side power management are separated for isolated power supply domains (VCCP, GNDP and VCCS, GNDS). ICE186LM-V101 provides reinforced and safe isolated communication between primary and secondary sides.

5.2.1 CoolSET™ SiP primary side

The CoolSET™ ICE186LM-V101 SiP integrates a 950 V startup cell at the primary side. The IC self-starts through the startup resistor (R16) in series with this startup cell to charge the VCCP pin capacitors (C12, C14) when DC supply is applied. This startup resistor (R16), together with ZCDP pin external configuration resistor R_{ZCDPL} (R10), determine brown-in and brown-out protection, as shown in Table 3.

Table 3 Primary-side configuration options

Option	$R_{ZCDPL(min)}$; $R_{ZCDPL(max)}$	Brown-in current threshold I_{HV_BI}	Brown-out current threshold I_{HV_BO}	Internal shunt resistor $R_{HVshunt}$
1	[1.00 kΩ ; 1.05 kΩ]	2.00 mA	1.40 mA	0.5 kΩ
2	[1.87 kΩ ; 2.70 kΩ]	1.00 mA	0.70 mA	1.0 kΩ
3	[4.30 kΩ ; 5.00 kΩ]	0.67 mA	0.47 mA	1.5 kΩ
4	[9.20 kΩ ; 9.50 kΩ]	0.50 mA	0.35 mA	2.0 kΩ

If **Option 1** is selected with R_{ZCDPL} (R10) = 1 kΩ, the brown-in voltage can be estimated as:

$$\boxed{V_{BI} = (R_{HV} + R_{HVshunt}) \times I_{HV\_BI} = (47\ \text{k}\Omega + 0.5\ \text{k}\Omega) \times 2\ mA = 95\ V}$$

Equation 1

and the brown-out voltage can be estimated as:

$$\boxed{V_{BO} = (R_{HV} + R_{HVshunt}) \times I_{HV\_BO} = (47\ \text{k}\Omega + 0.5\ \text{k}\Omega) \times 1.4\ mA = 66.5\ V}$$

Equation 2

Moreover, R8 and R10 resistors offer zero-crossing detection during the soft-start period and primary-sensed output overvoltage protection.

$$V_{OUT\_OVP} = \left(\frac{(R_{ZCDPH}+R_{ZCDPL})\times V_{ZCDP\_OVP\_min}}{R_{ZCDPL}} + V_{Daux})\right)\times\frac{N_{SEC}}{N_{AUX}} - V_{Dsec}$$
$$= \left(\frac{(10\ k\Omega + 1\ k\Omega)\times 2.05\ V}{1\ k\Omega} + 0.3V\right)\times\frac{2}{3} - 0.1V \approx 14.9\ V$$

Equation 3

Where,

N_{SEC}: Number of secondary turns

N_{AUX}: Number of auxiliary turns

V_{Daux}: Diode forward voltage drop at auxiliary winding

V_{Dsec}: Voltage drop across SR MOSFET

$V_{ZCDP\_OVP\_min}$: Minimum voltage of the output overvoltage threshold

V_{OUT_OVP}: User-defined output overvoltage level

C13 is chosen to adjust the delay time which starts when the drain-source voltage falls below the bus voltage until the ZCDP voltage falls to $V_{ZCDPthr}$ (100 mV, typ.). Therefore, the power switch can be turned on at the valley point of the drain-source voltage. This is normally done through experimentation.

A 44 µF capacitor for C12, C14 are applied to ensure stable system operation and enough break time for auto-restart protection. The VCCP resistor (R9) is placed as noise attenuation in case of severe voltage spike coupling from the transformer during the surge test.

DC line overvoltage protection is detected by sensing the bus capacitor voltage through the VINP pin via the divider resistor R5. Once the VINP pin voltage is higher than the line overvoltage threshold V_{VINP_LOVP}, the controller enters the line overvoltage protection and releases the protection mode when the VINP pin voltage falls below V_{VINP_LOVP}.

Typical LOVP voltage is calculated as follows:

$$V_{BUS\_OVP} = V_{VINP\_LOVP}\times\frac{R3+R5}{R5} = 2.80\ V\times\frac{10\ M\Omega+62\ k\Omega}{62\ k\Omega} = 454\ V$$

Equation 4

A low-cost RCD clamp consisting of the D1 diode, R1 resistor, and the C2 capacitor is implemented to suppress the peak drain voltage when turning off the power switch inside U1. This passive snubber helps dissipate the energy stored in the transformer leakage inductance.

5.2.2 CoolSET™ SiP secondary side

The secondary side of CoolSET™ ICE186LM-V101 SiP starts to take over the PWM control when the output voltage reaches 95% of its regulation target. The ICE186LM-V101 PWM control is based on sensing the reflected voltage from the primary side via the ZCDS pin and the error amplifier (EA) output voltage. ICE186LM-V101 integrated PWM and SR control ensures that the timing of the SR power switch (Q1) and the primary-side power switch is well-synchronized, which avoids the cross conduction of the two switches and provides reliable synchronous rectification. In addition, the current injection function via the SR power switch (Q1) enables zero-voltage switching operation on the primary side.

R18 is connected to CONF0 and serves as R_{SET0}. The value of R18 is determined by the transformer turns ratio, which is a critical parameter in the design. According to Table 4, the transformer turns ratio is specified as 8. Based on this value, R18 is set as 18 kΩ.

Table 4 Resistance for R_{SET0}

Turns ratio N_{MIAN}/N_{SEC}	R_{SET0}
5	3.9 kΩ
6	6.8 kΩ
7	12.0 kΩ
8	18.0 kΩ
9	27.0 kΩ
10	39.0 kΩ

R17 is connected to CONF1 and serves as R_{SET1}, which is to preset the parameters relevant for operation. For this application, the R17 is **Option 6** in Table 5, which is set as 39 kΩ.

Table 5 Resistance for R_{SET1}

R_{SET1}	3.9 kΩ	6.8 kΩ	12.0 kΩ	18.0 kΩ	27.0 kΩ	39.0 kΩ
Minimum valley for high-line and low-line $N_{valley\_min\_highline}$, $N_{valley\_min\_lowline}$	1	1	1	1	1	1
Maximum valley for high-line and low-line $N_{valley\_max\_highline}$, $N_{valley\_max\_lowline}$	11	10	9	8	12	13
EA threshold to enter hysteretic mode V_{EA_EHM}	0.586 V	0.586 V	0.567 V	0.567 V	0.605 V	0.624 V
EA voltage for wakeup in hysteretic mode V_{EA_HMOn}	1.20 V	1.20 V	1.20 V	1.20 V	1.20 V	1.20 V
EA voltage for off-phase in hysteretic mode V_{EA_HMOff}	0.9 V	0.9 V	0.9 V	0.9 V	0.9 V	0.8 V
EA threshold to enter skip mode V_{EA_skip}	0.5 V	0.5 V	0.45 V	0.45 V	0.5 V	0.5 V
EA voltage during hysteretic mode $V_{EA\_PWM\_HM}$	0.8 V	0.8 V	0.7 V	0.7 V	0.9 V	0.9 V
FB overvoltage protection mode PM_FB_OVP	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled

A compensation network consisting of C17, C18, and R13 is implemented to stabilize the output voltage regulation. This network is carefully designed to ensure that the power supply's output voltage remains stable and within the desired range. For a detailed understanding of the compensation network's calculation, see the design guide. This resource provides a comprehensive explanation of the calculations.

To minimize output voltage ripple, the choice of output capacitors is crucial. For C3, low equivalent series resistance (ESR) type capacitor is recommended. In addition, capacitors C4, C5, C6, C7, C8, and C9 are added to suppress high frequency noise.

6 PCB layout

6.1 Controller board

6.1.1 Top side

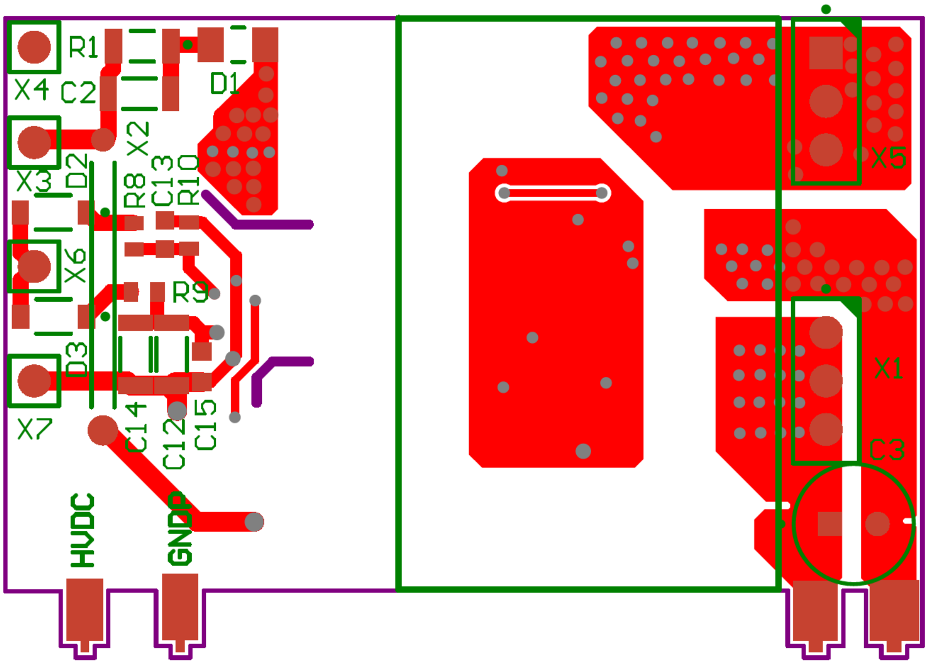


Figure 7 Top-side layout of controller board

6.1.2 Bottom side

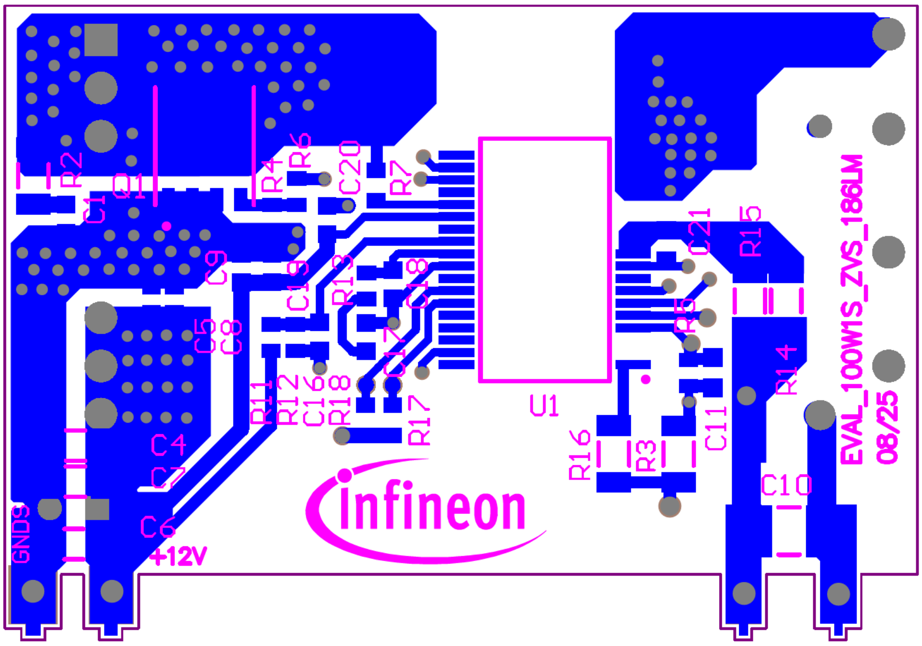


Figure 8 Bottom-side layout of controller board

6.2 Planar transformer board (MP1)

6.2.1 8-layer trace artwork

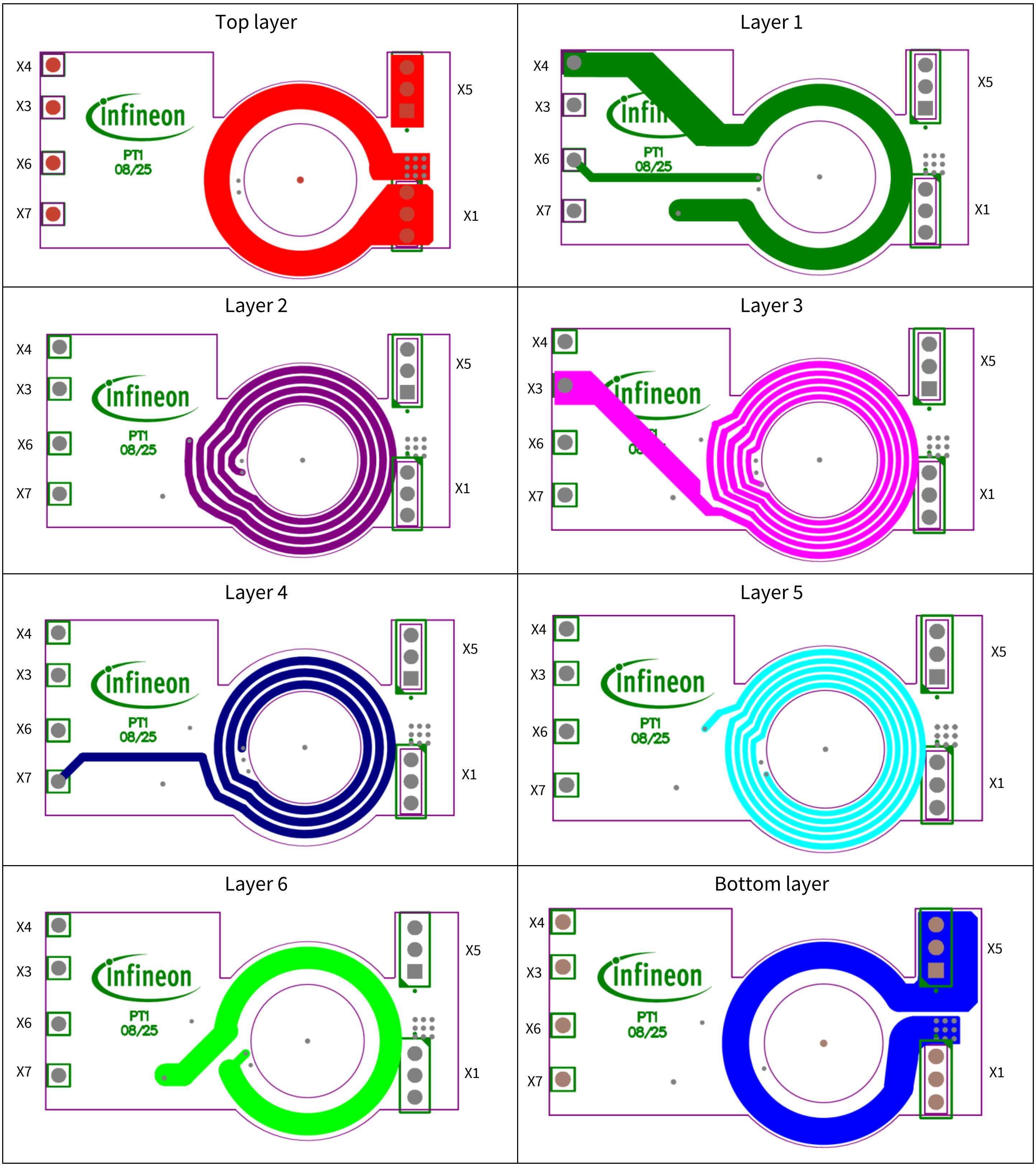


Figure 9 Trace artwork in different layers of planar transformer board

7 Bill of materials

Table 6 BOM

No	CKT Code	Description	Part Number	Manufacturer	Qty
1	C1	Ceramic capacitor 100 pF 100 V NPO 0603			1
2	C10	Ceramic capacitor 100 nF 500 V X7R 1210			1
3	C11, C21	Ceramic capacitor 1 nF 50 V NPO 0603			2
4	C12, C14	Ceramic capacitor 22 µF 35 V X7R 1206			2
5	C13	Ceramic capacitor 33 pF 50 V NPO 0603			1
6	C15, C20	Ceramic capacitor 100 nF 50 V X7R 0603			2
7	C16	Ceramic capacitor 470 pF 50 V COG 0603			1
8	C17	Ceramic capacitor 68 nF 25 V X7R 0603			1
9	C18	Ceramic capacitor 2.2 nF 50 V NPO 0603			1
10	C19	Ceramic capacitor 10 µF 25 V X5R 0603			1
11	C2	Ceramic capacitor 1 nF 500 V X7R 1206			1
12	C3	Aluminum polymer capacitor 470 µF 20% 16 V radial	NPXC0801C471MJTM	YMin	1
13	C4, C6, C7	Ceramic capacitor 47 µF 16 V X7R 1206			3
14	C5, C8, C9	Ceramic capacitor 1 µF 50 V X5R 0603			3
15	D1	SMD ultrafast power rectifier 1 kV	HS1MFL	Taiwan Semiconductor Corporation	1
16	D2	SMD ultrafast power rectifier 150 V	RB168MM150TR	ROHM	1
17	D3	SMD ultrafast power rectifier 200 V	S1DLW	Taiwan Semiconductor	1
18	MP1	Planar transformer ERI30	ER30/12/20F planar trf board, Lp=220 µH, 16T:2T:3T		1
19	Q1	OptiMOS 6 Power Transistor, 100V, 230A	ISC022N10NM6	Infineon Technologies	1
20	R1	SMD resistor 270 kΩ 1% 1/4 W 1206			1
21	R10	SMD resistor 1 kΩ 1% 1/10 W 0603			1
22	R11	SMD resistor 270 kΩ 1% 1/10 W 0603			1
23	R12	SMD resistor 20 kΩ 1% 1/10 W 0603			1
24	R13	SMD resistor 22 kΩ 1% 1/10 W 0603			1
25	R14, R15	SMD resistor 390 mΩ 1% 1/4 W 1206			2
26	R16	SMD resistor 47 kΩ 1% 1/4 W 1206			1
27	R17	SMD resistor 39 kΩ 1% 1/10 W 0603			1
28	R18	SMD resistor 18 kΩ 1% 1/10 W 0603			1
29	R2	SMD resistor 51 Ω 1% 1/4 W 1206			1
30	R3	SMD resistor 10 MΩ 1% 1/4 W 1206			1

No	CKT Code	Description	Part Number	Manufacturer	Qty
31	R4, R8	SMD resistor 10 kΩ 1% 1/10 W 0603			2
32	R5	SMD resistor 62 kΩ 1% 1/10 W 0603			1
33	R6	SMD resistor 2 Ω 1% 1/10 W 0603			1
34	R7	SMD resistor 15 kΩ 1% 1/10 W 0603			1
35	R9	SMD resistor 2 Ω 1% 1/10 W 0603			1
36	U1	CoolSET™ SiP ICE186LM-V101	ICE186LM_V101	Infineon Technologies	1
37	X1	Jumper wire			3
38	X5	Jumper wire			3
39	X2	Jumper wire			1
40	X3, X4, X6, X7	Header pin			4

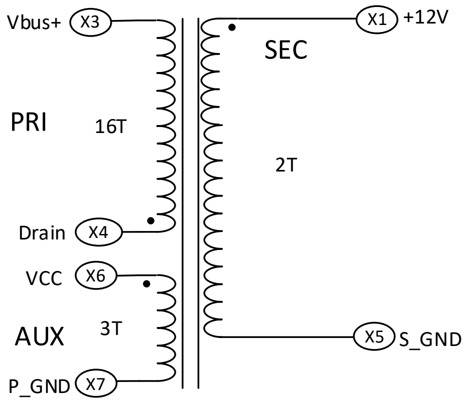
8 Transformer specification

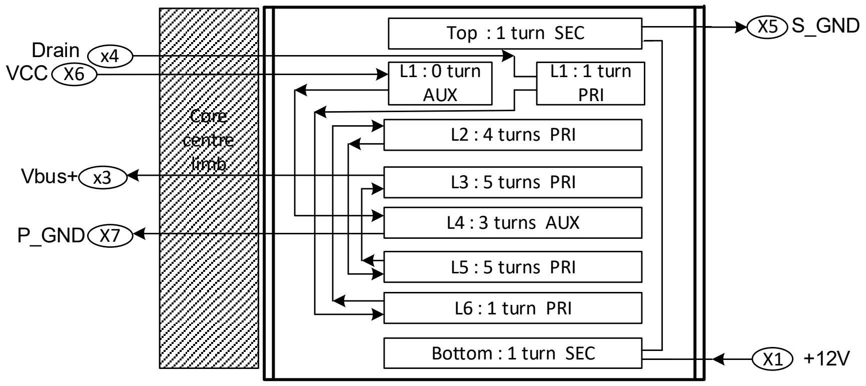
8.1 Electrical diagram and planar coil structure

Core and core material:

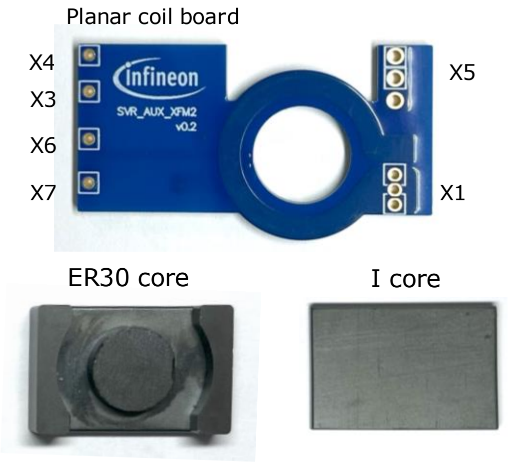
ER30 core + I core; ER30 core: TDG TPG33-A-ER30/12/20F and I core: Ferroxcube PLT30/20/3-3C95

L_p=220µH, 16T : 2T : 3T (N_p : N_{s1} : N_{aux})





Connections between layers through via



Layer	Windings	Start	End	Turn
Top	SEC	X1	Bottom	1
L1	AUX / PRI	X4 (PRI) / X6 (AUX)	PRI (L6) / AUX (L4)	1 (PRI) / 0 (AUX)
L2	PRI	L6	L5	4
L3	PRI	L5	X3	5
L4	AUX	L1	X7	3
L5	PRI	L2	L3	5
L6	PRI	L1	L2	1
Bottom	SEC	Top	X5	1

Figure 10 **Electrical diagram and planar coil structure**

9 Measurement data and graphs

All performance data is measured at room temperature Ta = 25°C unless otherwise specifically mentioned.

9.1 Efficiency

Table 7 Efficiency result

Input (VDC)	Load %	Pin (W)	Vout (V)	Iout (A)	Pout (W)	Eff. η
420	No load	0.0633	12.01	0.00	0.00	-
	5	6.13	12.00	0.42	5.01	81.77%
	10	11.49	11.99	0.83	10.00	86.99%
	15	16.52	11.99	1.25	15.00	90.90%
	25	27.32	11.99	2.08	24.99	91.49%
	50	54.01	12.00	4.17	50.00	92.55%
	75	80.49	11.99	6.25	74.95	93.13%
	80	85.85	11.99	6.67	79.94	93.13%
	100	107.47	11.98	8.33	99.83	92.88%
390	No load	0.0621	12.01	0.00	0.00	-
	5	6.08	11.99	0.42	5.01	82.23%
	10	11.47	11.99	0.83	9.99	87.31%
	15	16.50	11.99	1.25	15.00	90.83%
	25	27.19	11.99	2.08	24.96	91.83%
	50	53.89	11.99	4.17	49.98	92.78%
	75	80.38	11.99	6.25	74.94	93.23%
	80	85.72	11.99	6.67	79.91	93.25%
	100	107.44	11.98	8.34	99.85	92.93%
300	No load	0.0550	12.01	0.00	0.00	-
	5	5.995	12.00	0.42	5.00	83.35%
	10	11.151	11.99	0.83	10.00	89.67%
	15	16.446	11.99	1.25	15.04	91.43%
	25	27.085	12.00	2.08	25.00	92.30%
	50	53.6	12.00	4.17	50.00	93.29%
	75	80.262	11.99	6.25	74.96	93.39%
	80	85.5	11.99	6.67	79.92	93.43%
	100	107.564	11.98	8.33	99.87	92.87%
100	No load	0.0163	12.01	0.00	0.00	-
	5	5.73	12.00	0.42	5.01	87.45%
	10	10.90	11.99	0.83	10.00	91.72%
	15	16.22	11.99	1.25	15.02	92.60%
	25	26.85	11.99	2.08	24.99	93.08%

Input (VDC)	Load %	Pin (W)	Vout (V)	Iout (A)	Pout (W)	Eff. η
	50	53.48	11.99	4.17	49.96	93.41%

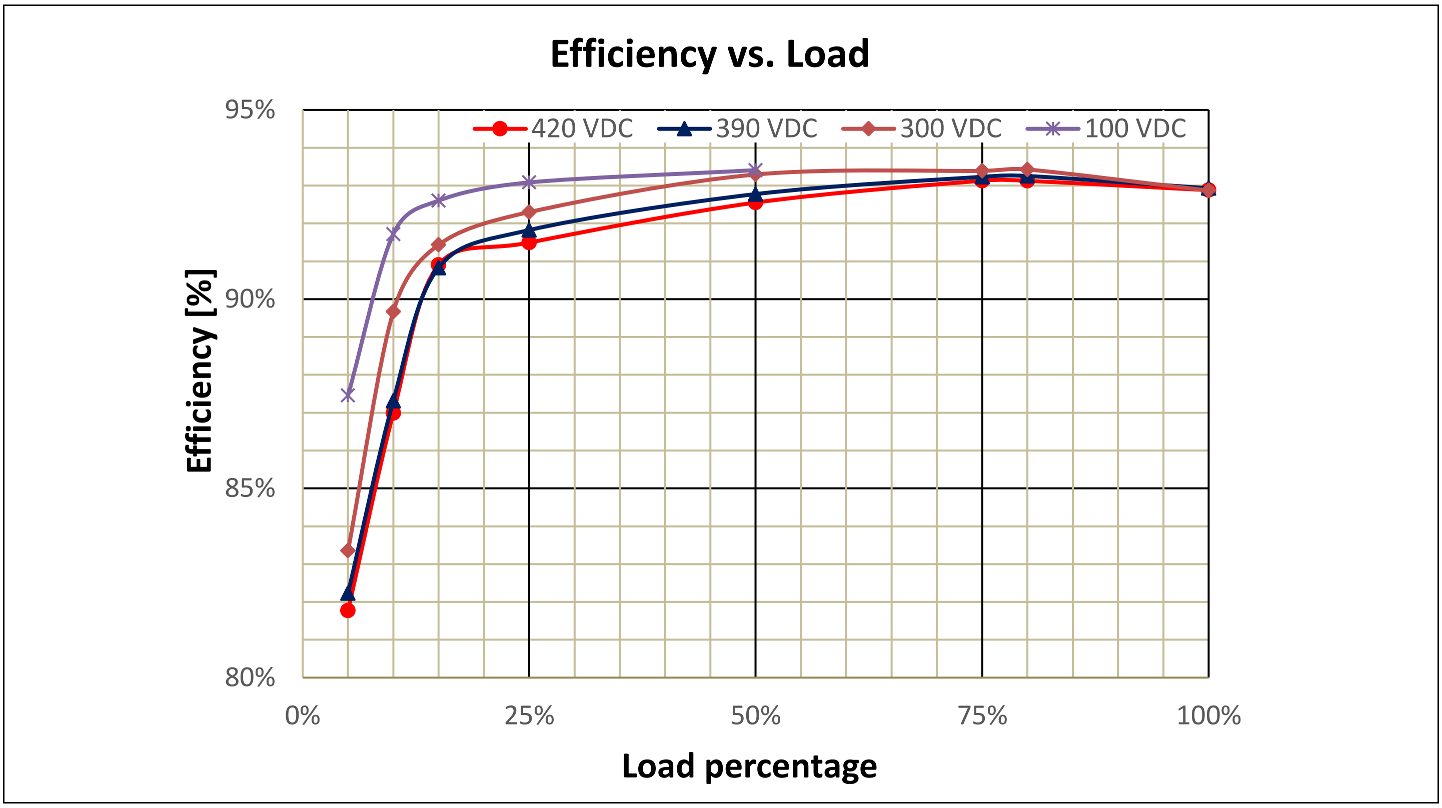


Figure 11 **Efficiency vs. DC-line input voltage**

9.2 Standby power

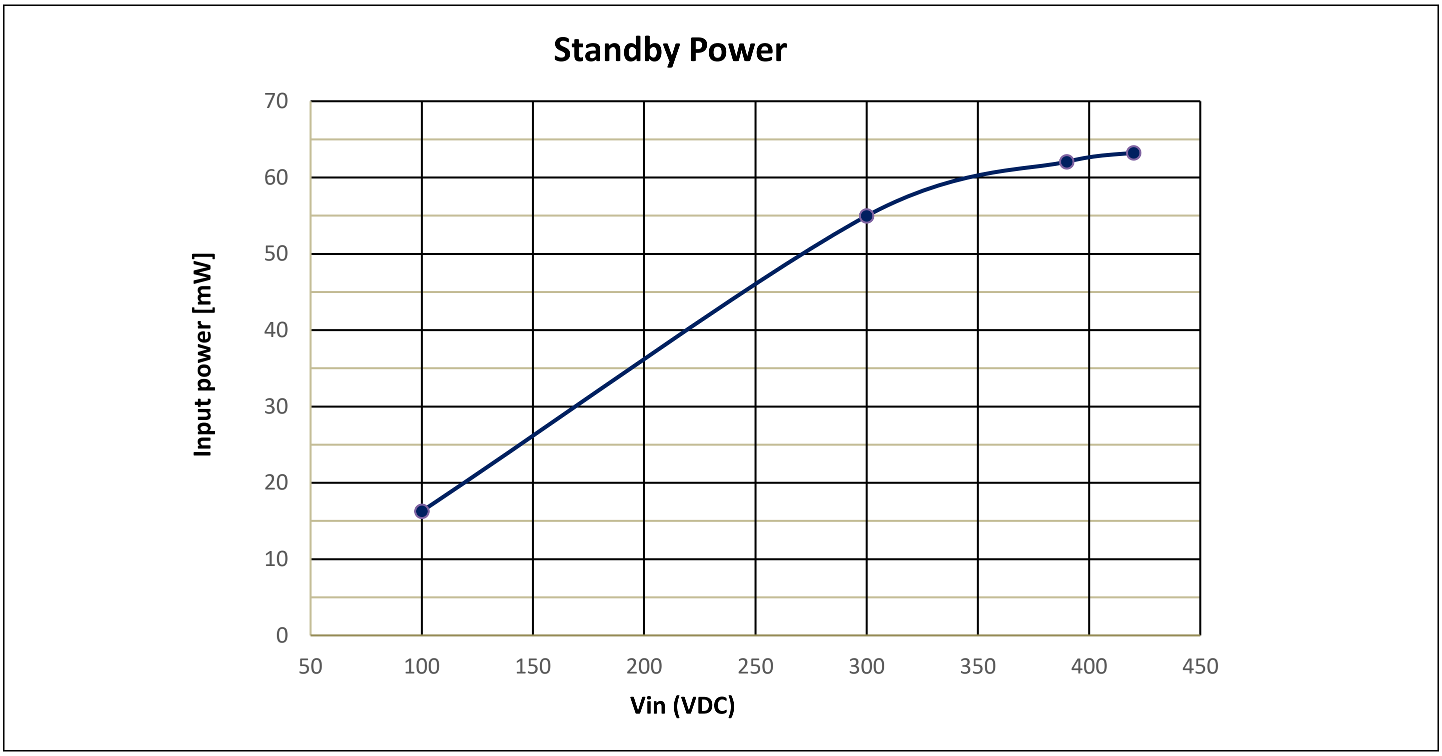


Figure 12 Standby power during no load

9.3 Line and load regulation

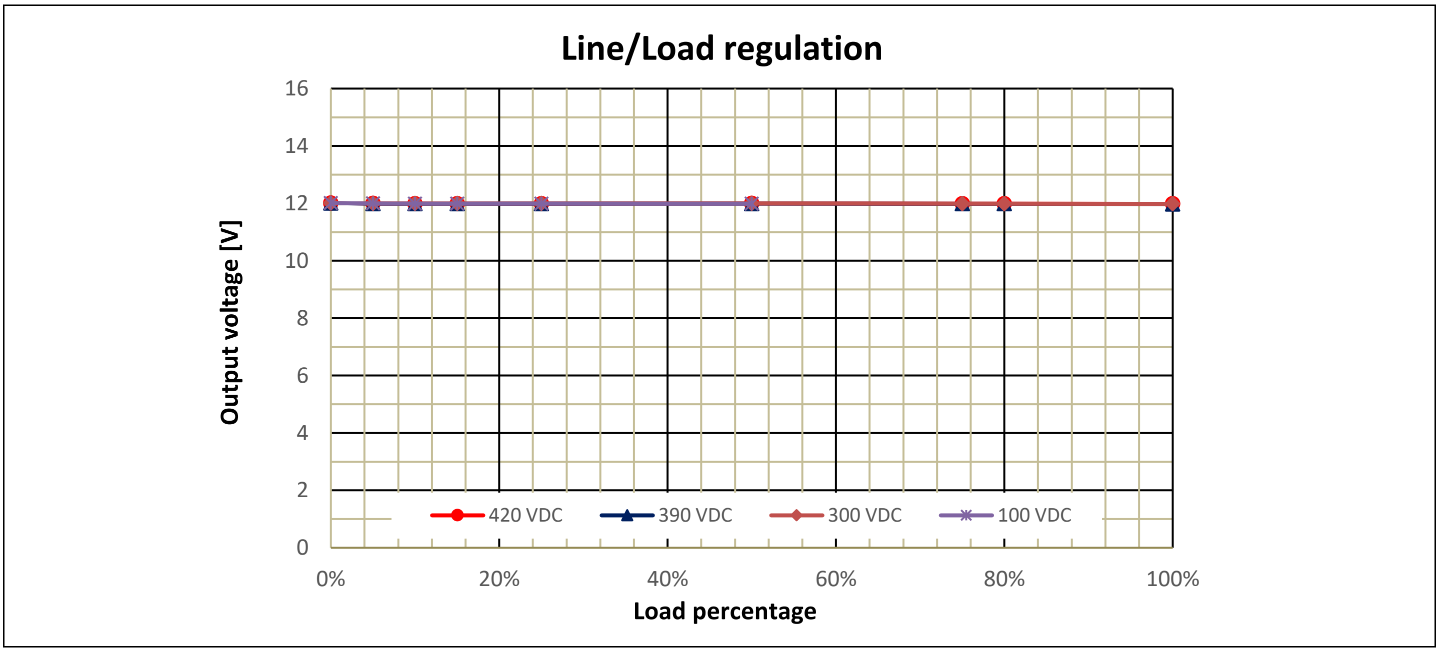


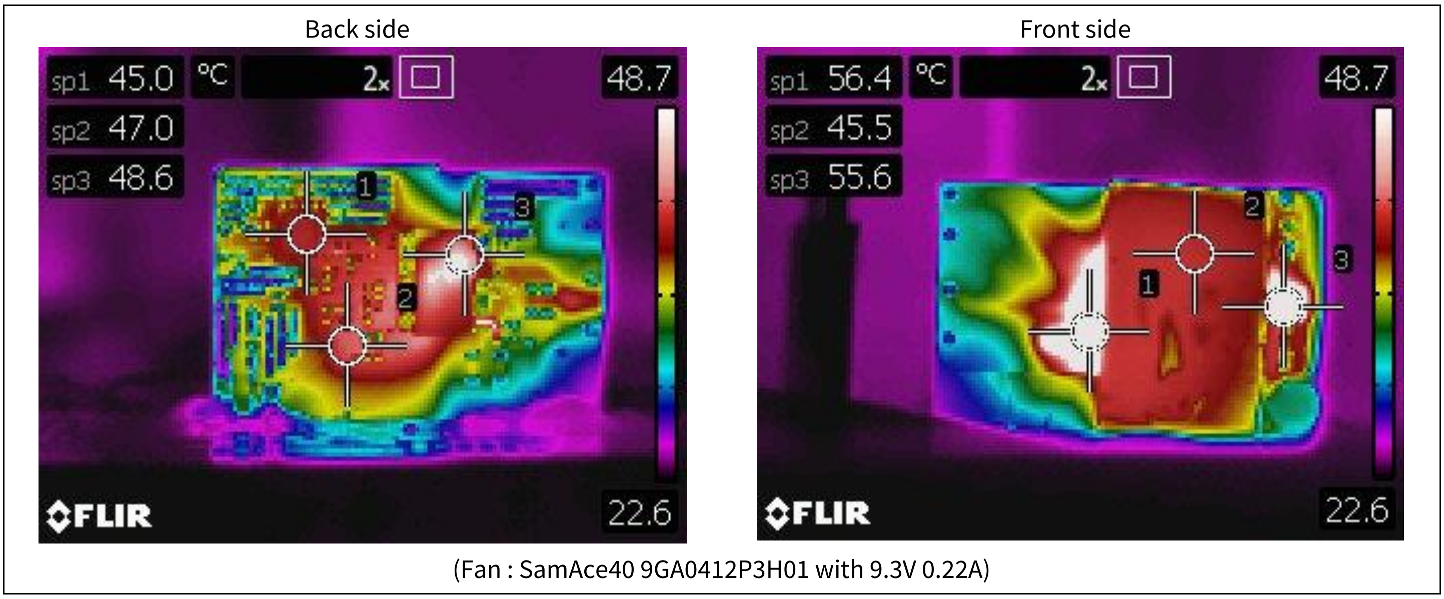
Figure 13 Line and load regulation

9.4 Thermal measurement

The thermal test of the open-frame evaluation board was done using an infrared thermography camera (FLIR-T420) at an ambient temperature of 22.6°C. The measurements were taken after one hour load running.

Table 8 **Temperature of critical components**

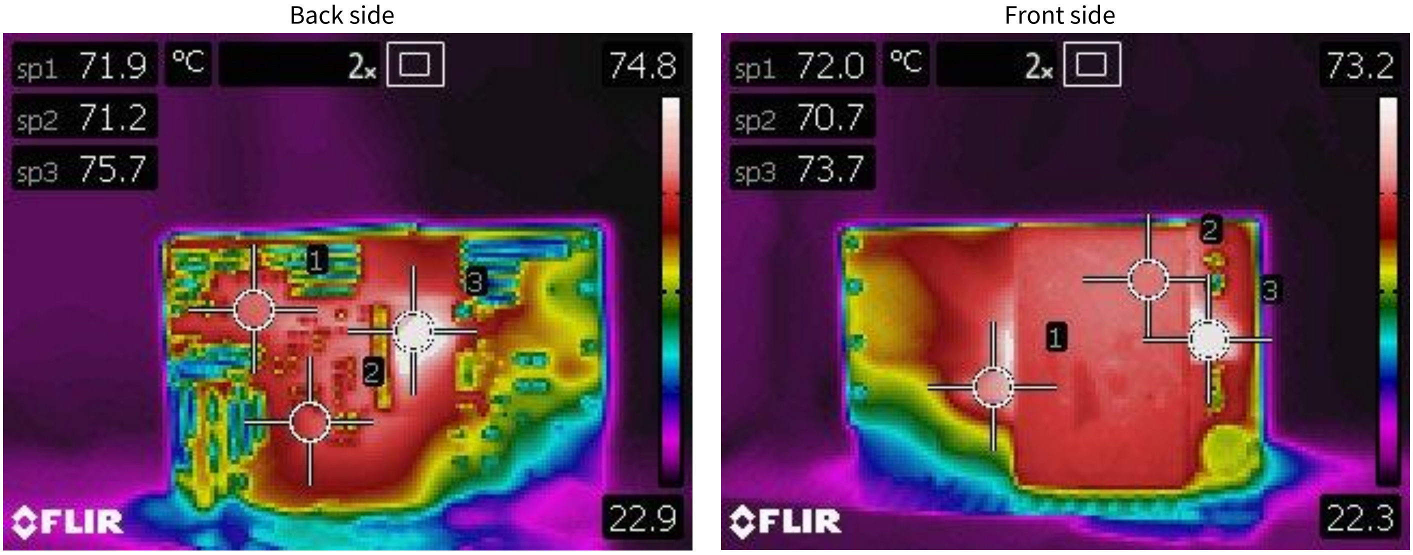
No.	Major component	390 V DC 100 W (°C) Forced ventilation	390 V DC 50 W (°C) Natural cooling
1	Q1 (SR MOSFET) - sp1 (back)	45.0 °C	71.9 °C
2	U1 (ICE186LM-V101) - sp3 (back)	48.6 °C	75.7 °C
3	MP1 core (Transformer) - sp2 (front)	45.5 °C	70.7 °C
4	MP1 trace (Transformer) - sp3 (front)	56.4 °C	73.7 °C
	Ambient	22.6 °C	22.6 °C


Back side

Front side

(Fan : SamAce40 9GA0412P3H01 with 9.3V 0.22A)

Figure 14 **Infrared thermal image. Input: 390 VDC; Output: 100 W at 12 V, 8.33 A with fan cooling, Ambient = 22.6 °C**



Back side

Front side

Figure 15 Infrared thermal image. Input: 390 VDC, Output: 50 W at 12 V with natural cooling, Ambient = 22.6°C

10 Waveforms and scope plots

All waveforms and scope plots were recorded with a Teledyne LeCroy 8054 oscilloscope.

10.1 Startup with maximum load

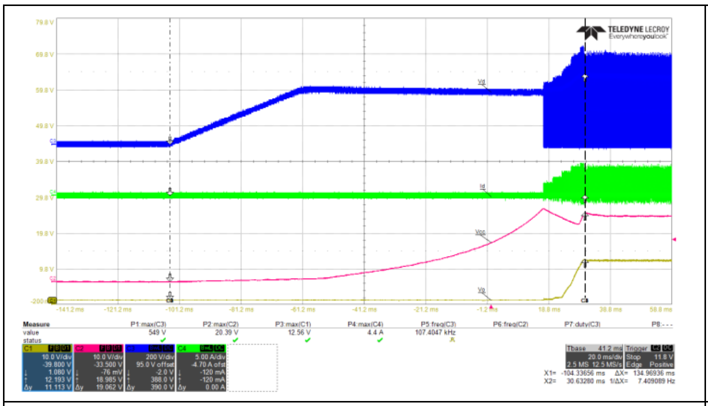
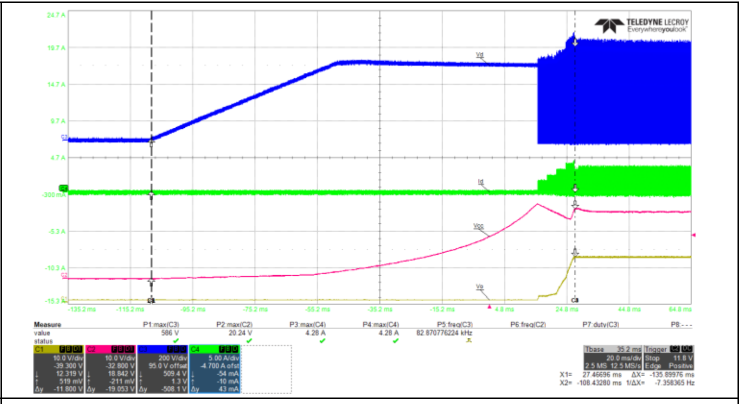
<table>
<tr><td></td><td></td></tr>
<tr><td>C3 (blue) : Drain voltage (V_{DRAIN})
C4 (green) : Drain current (I_{DRAIN})
C2 (red) : V_{CC} voltage (V_{CC})
C1 (yellow) : 12 V output voltage (V_{OUT})</td><td>C3 (blue) : Drain voltage (V_{DRAIN})
C4 (green) : Drain current (I_{DRAIN})
C2 (red) : V_{CC} voltage (V_{CC})
C1 (yellow) : 12 V output voltage (V_{OUT})</td></tr>
<tr><td>Start-up time at 300 VDC and Full load ≈ 0.135 s</td><td>Start-up time at 420 VDC and Full load ≈ 0.136 s</td></tr>
<tr><td colspan="2">The board can start up as expected over 300 VDC ~ 420 VDC, output voltage smoothly rises and regulates at 12 V.</td></tr>
</table>

Figure 16 Startup

10.2 Soft-start

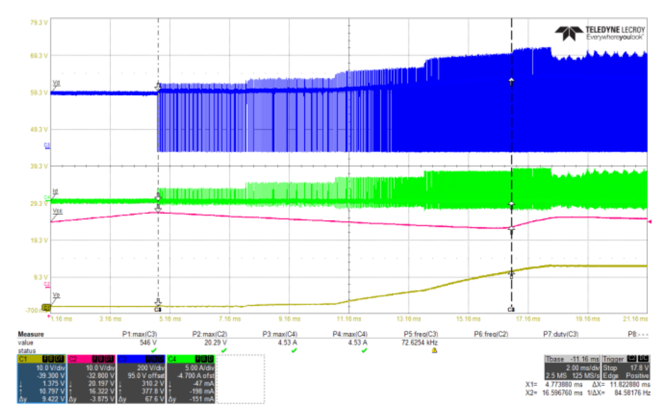
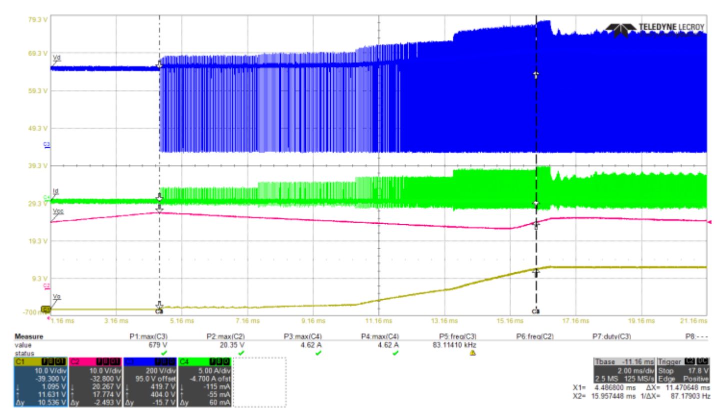
<table>
<tr><td></td><td></td></tr>
<tr><td>C3 (blue) : Drain voltage (V_{DRAIN})
C4 (green) : Drain current (I_{DRAIN})
C2 (red) : V_{CC} voltage (V_{CC})
C1 (yellow) : 12 V output voltage (V_{OUT})</td><td>C3 (blue) : Drain voltage (V_{DRAIN})
C4 (green) : Drain current (I_{DRAIN})
C2 (red) : V_{CC} voltage (V_{CC})
C1 (yellow) : 12 V output voltage (V_{OUT})</td></tr>
<tr><td>Soft-start time at 300 VDC and Full load ≈ 11.82 ms</td><td>Soft-start time at 420 VDC and Full load ≈ 11.47 ms</td></tr>
<tr><td colspan="2">The soft start time ends within 12 ms as per design.</td></tr>
</table>

Figure 17 Soft-start

10.3 Drain voltage and current at maximum load

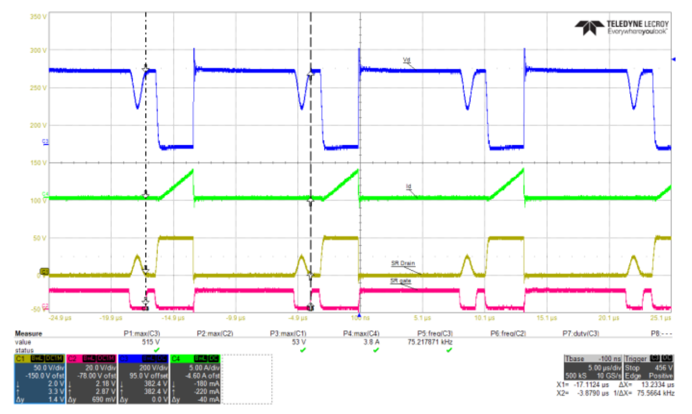
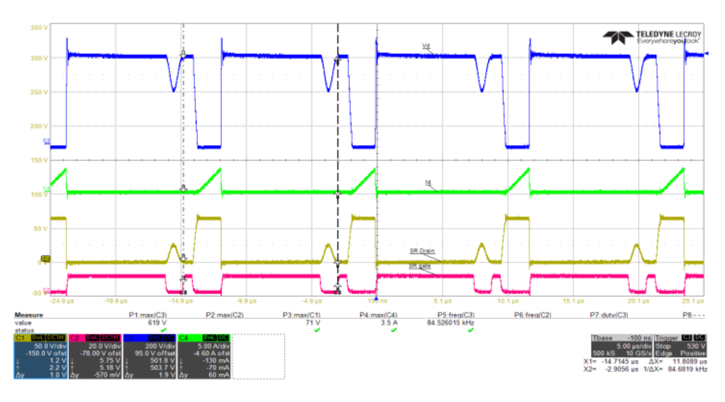
<table>
<tr><td></td><td></td></tr>
<tr><td>C3 (blue) : Drain voltage (V_{DRAIN})
C4 (green) : Drain current (I_{DRAIN})
C1 (yellow) : SR Drain (V_{SR_DRAIN})
C2 (red) : SR gate (V_{SR_gate})</td><td>C3 (blue) : Drain voltage (V_{DRAIN})
C4 (green) : Drain current (I_{DRAIN})
C1 (yellow) : SR Drain (V_{SR_DRAIN})
C2 (red) : SR gate (V_{SR_gate})</td></tr>
<tr><td>V_{Drain_peak} at 300 VDC 100W load ≈ 515 V
I_{DRAIN} at 300 V DC 100W load ≈ 3.8 A
V_{SR_Drain} at 300 VDC 100W load ≈ 53 V</td><td>V_{Drain_peak} at 420 VDC ≈ 619 V
I_{DRAIN} at 420 VDC ≈ 3.5 A
V_{SR_Drain} at 300 VDC 100W load ≈ 71 V</td></tr>
<tr><td colspan="2">ICE186LM-V101 operates at zero-voltage switching from 300 VDC to 420 VDC.</td></tr>
</table>

Figure 18 **Drain and CS voltage at maximum load**

10.4 Output ripple voltage at maximum load

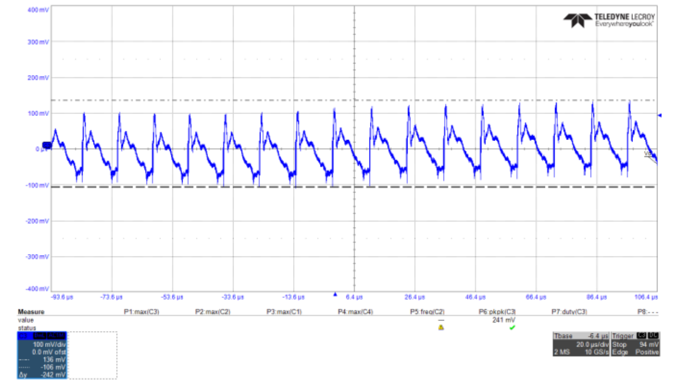
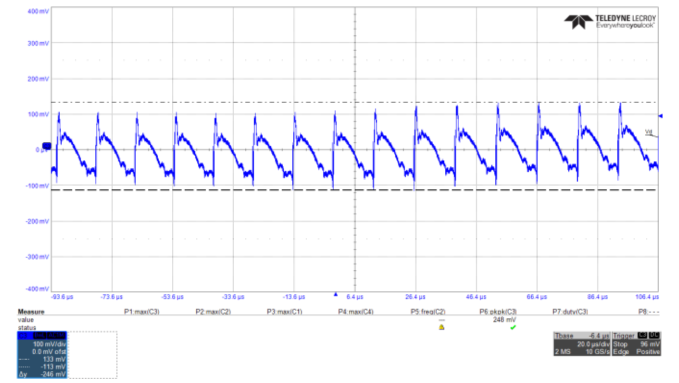
<table>
<tr><td></td><td></td></tr>
<tr><td>C3 (blue) : 12 V output ripple voltage (V_{O_ripple})</td><td>C3 (blue) : 12 V output ripple voltage (V_{O_ripple})</td></tr>
<tr><td>12 $V_{ripple\_pk\_pk}$ at 300 VDC ≈ 242 mV
Probe terminal with decoupling capacitor of 0.1 µF (ceramic) and 47 µF (electrolytic), 20 MHz BW</td><td>12 $V_{ripple\_pk\_pk}$ at 420 VDC ≈ 248 mV
Probe terminal with decoupling capacitor of 0.1 µF (ceramic) and 47 µF (electrolytic), 20 MHz BW</td></tr>
<tr><td colspan="2">The output ripple measured is around 2% of the output voltage.</td></tr>
</table>

Figure 19 **Output ripple voltage at maximum load**

10.5 Hysteretic mode operation

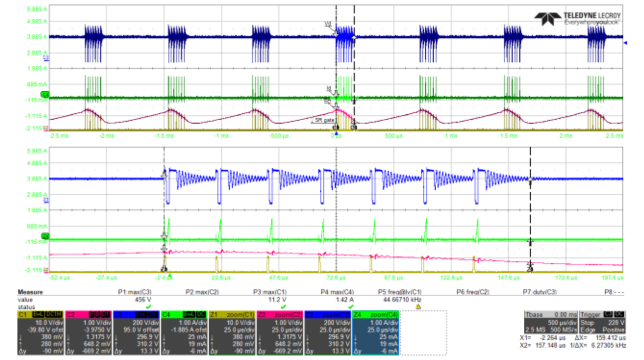
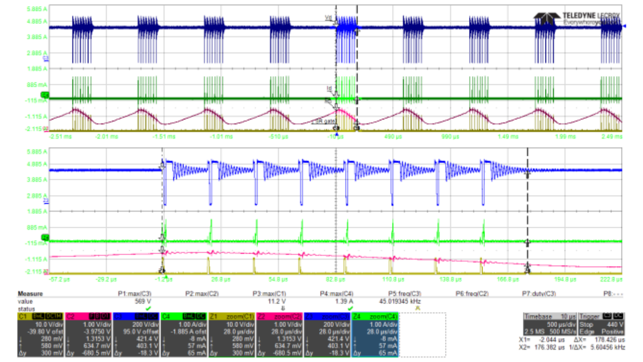
	
C3 (blue) : Drain voltage (V_{DRAIN}) C4 (green) : Drain current (I_{DRAIN}) C2 (red) : EA (V_{EA}) C1 (yellow) : SR Gate (V_{SR_gate})	C3 (blue) : Drain voltage (V_{DRAIN}) C4 (green) : Drain current (I_{DRAIN}) C2 (red) : EA (V_{EA}) C1 (yellow) : SR Gate (V_{SR_gate})
300 V DC, 1.51 W load Operation at f_{osc_ABM} = 44.6 kHz, I_{PK} = 1.42 A	420 V AC, 2.47 W load Operation at f_{osc_ABM} = 45 kHz, I_{PK} = 1.39 A
When the load reduces to < 3% load, the system enters the hysteretic mode to reduce the power loss.	

Figure 20 **Hysteretic mode operation**

10.6 Overload protection (auto-restart)

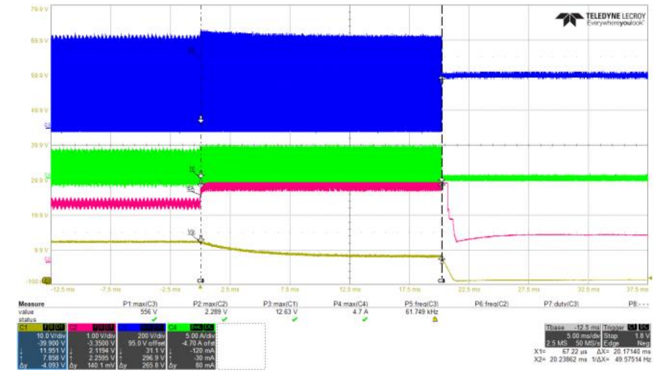
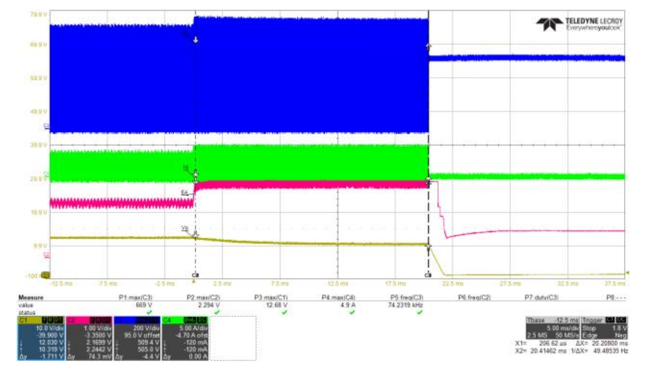
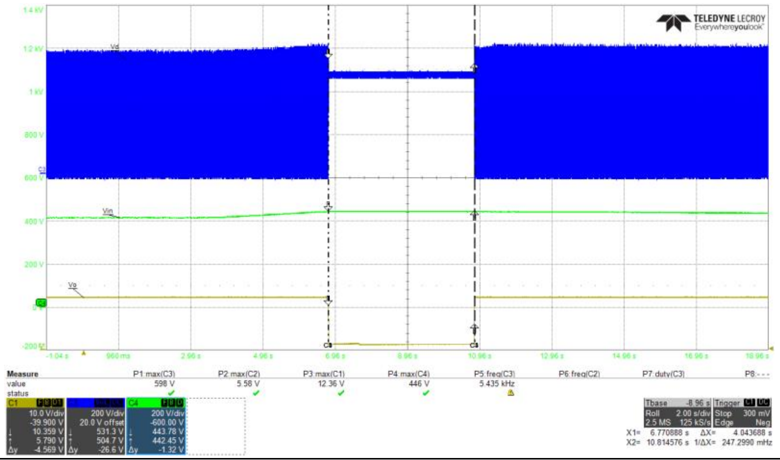
	
C3 (blue) : Drain voltage (V_{DRAIN}) C4 (green) : VCCP (V_{CC}) C2 (red) : EA (V_{EA}) C1 (yellow) : Vout (V_{OUT})	C3 (blue) : Drain voltage (V_{DRAIN}) C4 (green) : VCCP (V_{CC}) C2 (red) : EA (V_{EA}) C1 (yellow) : Vout (V_{OUT})
300 VDC, 100 W load steps to 120 W load. System enters Auto restart protection when V_{EA} > 2.2 V and blanking time 20.17 ms.	420 VDC, 100 W load steps to 120 W load. System enters Auto restart protection when V_{EA} > 2.2 V and blanking time 20.2 ms.
System enters overload protection as expected during load change from 100 W to 120 W.	

Figure 21 **Overload protection test**

10.7 Line OVP

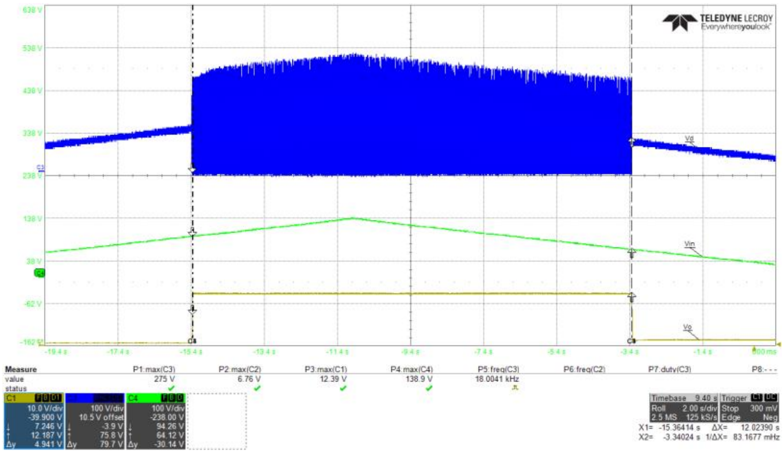


```
Measure   P1:max(C3)  P2:max(C2)  P3:max(C1)  P4:max(C4)  P5:freq(C3)  P6:freq(C2)  P7:duty(C3)  P8:- - -
value     598 V       5.58 V      12.36 V     446 V       5.435 kHz
status    ✓           ✓           ✓           ✓           ⚠

C1             C2                C4
  10.0 V/div     200 V/div         200 V/div
  -39.900 V      20.0 V offset     -600.00 V
↓ 10.359 V     ↓ 531.3 V         ↓ 443.78 V
↑ 5.790 V      ↑ 504.7 V         ↑ 442.45 V
Δy -4.569 V    Δy -26.6 V        Δy -1.32 V

Tbase  -8.96 s    Trigger
Roll   2.00 s/div Stop   300 mV
2.5 MS 125 kS/s   Edge   Neg
X1=  6.770888 s   ΔX=    4.043688 s
X2=  10.814576 s  1/ΔX=  247.2990 mHz
```

C2 (blue) : Drain voltage (V_{DRAIN})
C4 (green) : Vin (Vin)
C1 (yellow) : V_{OUT} (V_{OUT})

Figure 22 Line OVP test

10.8 Brown-in and brown-out



```
Measure   P1:max(C3)  P2:max(C2)  P3:max(C1)  P4:max(C4)  P5:freq(C3)  P6:freq(C2)  P7:duty(C3)  P8:- - -
value     275 V       6.76 V      12.39 V     138.9 V     18.0041 kHz
status    ✓           ✓           ✓           ✓

C1             C2                C4
  10.0 V/div     100 V/div         100 V/div
  -39.900 V      10.5 V offset     -238.00 V
↓ 7.246 V      ↓ -3.9 V          ↓ 94.26 V
↑ 12.187 V     ↑ 75.8 V          ↑ 64.12 V
Δy 4.941 V     Δy 79.7 V         Δy -30.14 V

Timebase  9.40 s    Trigger
Roll   2.00 s/div   Stop   300 mV
2.5 MS 125 kS/s     Edge   Neg
X1=  -15.36414 s    ΔX=    12.02390 s
X2=  -3.34024 s     1/ΔX=  83.1677 mHz
```

C2 (blue) : Drain voltage (V_{DRAIN})
C4 (green) : Vin (Vin)
C1 (yellow) : V_{OUT} (V_{OUT})

Figure 23 Brown-in and brown-out test

References

[1] Infineon Technologies AG: *Datasheet – CoolSET™ SiP*; Available online

[2] Infineon Technologies AG: *Design guide – Design Guide for ZVS QR flyback using CoolSET™ SiP*; Available online

Revision history

Document version	Date of release	Description of changes
V 1.0	2026-02-20	Initial release

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Edition 2026-02-20

Published by

Infineon Technologies AG
Am Campeon 1-15
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