XDP710 Hot-swap Controller PMBus Commands

Wide input voltage range (5.5 V to 80 V) system monitoring and protection IC

About this document

Scope and purpose

This document describes all the PMBus commands supported by the XDP710 system monitoring and protection IC.

Intended audience

The user manual is intended for XDP710 users.

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1 XDP710 PMBus commands

1.1 OPERATION

Address: 0x01
Reset: 0x80
Included in OTP

The OPERATION command is used to turn the unit on and off in conjunction with the input from the UV/EN pin.

Table 1 OPERATION command structure

	7	6	5	4	3	2	1	0
Read	ON							
Write								
Reset	1	0	0	0	0	0	0	0

Table 2 OPERATION command bits description

Field	Bits	Type	Reset	Description
RESERVED	[6:0]		0x00	
ON	7	rw	0x1 (Enable = 1 dec)	ON bit enables or disables the Hot swap output.

Table 3 ON bit description

ON	Name	Description
0x0	Disable	Hot swap output disabled
0x1	Enable	Hot swap output enabled

1.2 CLEAR_FAULTS

Address: 0x03
Reset: 0x0000

This command is used to clear any fault and warning bits that have been set. If the fault is still present when the bit is cleared, the fault bit is immediately set again.

Table 4 CLEAR_FAULTS command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	CLEAR_FAULTS															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5 CLEAR_FAULTS command bits description

Field	Bits	Type	Reset	Description
CLEAR_FAULTS	[15:0]	r	0x0000 (0 dec)	Clear any fault and warning bits that have been set

1.3 CAPABILITY

Address: 0x19
Reset: 0xD0

This read only command provides a way for a host system to determine some key capabilities of XDP710.

Table 6 CAPABILITY command structure

	7	6	5	4	3	2	1	0
Read	PCK_ERR_CHK	MAX_BUS_SPEED		SMBALERT	NUMERIC_FORMAT			
Write								
Reset	1	1	0	1	0	0	0	0

Table 7 CAPABILITY command bits description

Field	Bits	Type	Reset	Description
RESERVED	[2:0]		0x0	
NUMERIC_FORMAT	3	r	0x0 (0 = 0 dec)	Specifies the format of the numeric data
SMBALERT	4	r	0x1 (1 = 1 dec)	Specifies whether or not the device has an SMBALERT# pin and supports SMBus Alert Response protocol
MAX_BUS_SPEED	[6:5]	r	0x2 (10 = 2 dec)	Specifies the maximum speed of the bus
PCK_ERR_CHK	7	r	0x1 (1 = 1 dec)	Specifies whether or not the device supports Packet Error Check

Table 8 NUMERIC_FORMAT bit description

NUMERIC_FORMAT	Value	Description
0x0	0	Numeric data is in Direct format.
0x1	1	NA

Table 9 SMBALERT bit description

SMBALERT	Value	Description
0x0	0	NA
0x1	1	The device does support the SMBus Alert Response protocol.

Table 10 MAX_BUS_SPEED bits description

MAX_BUS_SPEED	Value	Description
0x0 (00 bin)	0	NA
0x1 (01 bin)	1	NA
0x2 (10 bin)	10	Maximum supported bus speed is 1MHz.
0x3 (11 bin)	11	NA

Table 11 PCK_ERR_CHK bit description

PCK_ERR_CHK	Value	Description
0x0	0	NA
0x1	1	Packet Error Checking is supported.

1.4 VOUT_OV_WARN_LIMIT

Address: 0x42
Reset: 0x0FFF
Included in OTP

The VOUT_OV_WARN_LIMIT command sets the value of the output voltage measured at the VOUT pin that causes an output overvoltage warning.

Table 12 VOUT_OV_WARN_LIMIT command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read					VOUT_OV_WARN_LIMIT											
Write																
Reset	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

Table 13 VOUT_OV_WARN_LIMIT bits description

Field	Bits	Type	Reset	Description
VOUT_OV_WARN_LIMIT	[11:0]	rw	0xFFF (4095 dec)	OOV warning can be programmed from 0 to 22, 0 to 44 or 0 to 88V (absolute value) depending on VTLM_RNG settings.
RESERVED	[15:12]		0x0	

1.5 VOUT_UV_WARN_LIMIT

Address: 0x43
Reset: 0x0000
Included in OTP

The VOUT_UV_WARN_LIMIT command sets the value of the output voltage measured at the VOUT pin that causes an output undervoltage warning.

Table 14 VOUT_UV_WARN_LIMIT command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read					VOUT_UV_WARN_LIMIT											
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 15 VOUT_UV_WARN_LIMIT command bits description

Field	Bits	Type	Reset	Description
VOUT_UV_WARN_LIMIT	[11:0]	rw	0x000 (0 dec)	OUV warning can be programmed from 0 to 22, 0 to 44 or 0 to 88V (absolute value) depending on VTLM_RNG settings.
RESERVED	[15:12]		0x0	

1.6 VOUT_UV_FAULT_LIMIT

Address: 0x44
Reset: 0x0000
Included in OTP

This command sets the value of the output voltage measured at the VOUT pin that causes an output undervoltage fault.

Table 16 VOUT_UV_FAULT_LIMIT command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read					VOUT_UV_FAULT_LIMIT											
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 17 VOUT_UV_FAULT_LIMIT command bits description

Field	Bits	Type	Reset	Description
VOUT_UV_FAULT_LIMIT	[11:0]	rw	0x000 (0 dec)	OUV fault can be programmed from 0 to 22, 0 to 44 or 0 to 88V (absolute value) depending on VTLM_RNG settings.
RESERVED	[15:12]		0x0	

1.7 IOUT_OC_WARN_LIMIT

Address: 0x4A
Reset: 0x0FFF
Included in OTP

The IOUT_OC_WARN_LIMIT command sets the level below the V_SNS_CS voltage measured at the ISNS_x pins that causes an output overcurrent warning.

Table 18 IOUT_OC_WARN_LIMIT command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read					IOUT_OC_WARN_LIMIT											
Write																
Reset	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

Table 19 IOUT_OC_WARN_LIMIT command bits description

Field	Bits	Type	Reset	Description
IOUT_OC_WARN_LIMIT	[11:0]	rw	0xFFF (4095 dec)	OC warning can be programmed as a fraction of V_SNS_CS.
RESERVED	[15:12]		0x0	

1.8 OT_FAULT_LIMIT

Address: 0x4F
Reset: 0x0FFF
Included in OTP

The OT_FAULT_LIMIT command sets the temperature of the FET, measured between TSNS_P and TSNS_N pins, at which the OT fault is triggered.

Table 20 OT_FAULT_LIMIT command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read					OT_FAULT_LIMIT											
Write																
Reset	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

Table 21 OT_FAULT_LIMIT command bits description

Field	Bits	Type	Reset	Description
OT_FAULT_LIMIT	[11:0]	rw	0xFFF (4095 dec)	OT limit for triggering the fault.
RESERVED	[15:12]		0x0	

1.9 OT_WARN_LIMIT

Address: 0x51
Reset: 0x0FFF
Included in OTP

The OT_WARN_LIMIT command sets the temperature of the FET, measured between TSNS_P and TSNS_N pins, at which the OT warning is triggered.

Table 22 OT_WARN_LIMIT command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read					OT_WARN_LIMIT											
Write																
Reset	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

Table 23 OT_WARN_LIMIT command bits description

Field	Bits	Type	Reset	Description
OT_WARN_LIMIT	[11:0]	rw	0xFFF (4095 dec)	OT limit for triggering the warning.
RESERVED	[15:12]		0x0	

1.10 VIN_OV_FAULT_LIMIT

Address: 0x55
Reset: 0x0FFF
Included in OTP

This command sets the value of the input voltage measured at the ISNS_P pin that causes an input overvoltage fault.

Table 24 VIN_OV_FAULT_LIMIT command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read					VIN_OV_FAULT_LIMIT											
Write																
Reset	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

Table 25 VIN_OV_FAULT_LIMIT command bits description

Field	Bits	Type	Reset	Description
VIN_OV_FAULT_LIMIT	[11:0]	rw	0xFFF (4095 dec)	OV fault can be programmed from 0 to 22, 0 to 44 or 0 to 88V (absolute value) depending on VTLM_RNG settings.
RESERVED	[15:12]		0x0	

1.11 VIN_OV_WARN_LIMIT

Address: 0x57
Reset: 0x0FFF
Included in OTP

The VIN_OV_WARN_LIMIT command sets the value of the input voltage measured at the ISNS_P pin that causes an input overvoltage warning.

Table 26 VIN_OV_WARN_LIMIT command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read					VIN_OV_WARN_LIMIT											
Write																
Reset	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

Table 27 VIN_OV_WARN_LIMIT command bits description

Field	Bits	Type	Reset	Description
VIN_OV_WARN_LIMIT	[11:0]	rw	0xFFF (4095 dec)	OV warning can be programmed from 0 to 22, 0 to 44 or 0 to 88V (absolute value) depending on VTLM_RNG settings.
RESERVED	[15:12]		0x0	

1.12 VIN_UV_WARN_LIMIT

Address: 0x58
Reset: 0x0000
Included in OTP

The VIN_UV_WARN_LIMIT command sets the value of the input voltage measured at the ISNS_P pin that causes an input undervoltage warning.

Table 28 VIN_UV_WARN_LIMIT command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read					VIN_UV_WARN_LIMIT											
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 29 VIN_UV_WARN_LIMIT command bits description

Field	Bits	Type	Reset	Description
VIN_UV_WARN_LIMIT	[11:0]	rw	0x000 (0 dec)	UV warning can be programmed from 0 to 22, 0 to 44 or 0 to 88V (absolute value) depending on VTLM_RNG settings.
RESERVED	[15:12]		0x0	

1.13 VIN_UV_FAULT_LIMIT

Address: 0x59
Reset: 0x0000
Included in OTP

This command sets the value of the input voltage measured at the ISNS_P pin that causes an input undervoltage fault.

Table 30 VIN_UV_FAULT_LIMIT command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read					VIN_UV_FAULT_LIMIT											
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 31 VIN_UV_FAULT_LIMIT command bits description

Field	Bits	Type	Reset	Description
VIN_UV_FAULT_LIMIT	[11:0]	rw	0x000 (0 dec)	UV fault can be programmed from 0 to 22, 0 to 44 or 0 to 88V (absolute value) depending on VTLM_RNG settings.
RESERVED	[15:12]		0x0	

1.14 PIN_OP_WARN_LIMIT

Address: 0x6B
Reset: 0x7FFF
Included in OTP

This command sets the value of the input power calculated as a product of VIN * IOUT that causes an input overpower warning.

Table 32 PIN_OP_WARN_LIMIT command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	PIN_OP_WARN_LIMIT															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 33 PIN_OP_WARN_LIMIT command bits description

Field	Bits	Type	Reset	Description
PIN_OP_WARN_LIMIT	[15:0]	rw	0xFFFF (65535 dec)	OP warning can be programmed from 0 to VTLM_RNG * OC. Maximum value of this bit field is 0x7FFF. If a value higher than this is programmed, it will be limited to 0x7FFF.

1.15 STATUS_BYTE

Address: 0x78
Reset: 0x40

The STATUS_BYTE command returns one byte of information with a summary of the most critical faults.

Table 34 STATUS_BYTE command structure

	7	6	5	4	3	2	1	0
Read		OFF		IOUT_OC_FAULT	VIN_UV_FAULT	TEMP	CML	NONE_OF_THE_ABOVE
Write								
Reset		1	0	0	0	0	0	0

Table 35 STATUS_BYTE command bits description

Field	Bits	Type	Reset	Description
NONE_OF_THE_ABOVE	0	rw	0x0 (0 = 0 dec)	This bit indicates if a fault or warning not listed in bits [6:1] has occurred.
CML	1	rw	0x0 (0 = 0 dec)	This bit indicates if a communications, memory or logic fault has occurred.
TEMP	2	rw	0x0 (0 = 0 dec)	This bit indicates if a temperature fault or warning has occurred.
VIN_UV_FAULT	3	rw	0x0 (0 = 0 dec)	This bit indicates if an input undervoltage fault has occurred.
IOUT_OC_FAULT	4	rw	0x0 (0 = 0 dec)	This bit indicates if an output overcurrent fault has occurred.
RESERVED	5		0x0	

(table continues...)

Table 35 (continued) STATUS_BYTE command bits description

Field	Bits	Type	Reset	Description
OFF	6	r	0x1 (1 = 1 dec)	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.
RESERVED	7		0x0	

Table 36 NONE_OF_THE_ABOVE bit description

NONE_OF_THE_ABOVE	Value	Description
0x0	0	Fault or warning has not ocurred
0x1	1	Fault or warning has occurred

Table 37 CML bit description

CML	Value	Description
0x0	0	Fault has not occurred
0x1	1	Fault has occurred

Table 38 TEMP bit description

TEMP	Value	Description
0x0	0	Fault or warning has not occurred
0x1	1	Fault or warning has occurred

Table 39 VIN_UV_FAULT bit description

VIN_UV_FAULT	Value	Description
0x0	0	Fault has not occurred
0x1	1	Fault has occurred

Table 40 IOUT_OC_FAULT bit description

IOUT_OC_FAULT	Value	Description
0x0	0	Fault has not occurred
0x1	1	Fault has occurred

Table 41 OFF bit description

OFF	Value	Description
0x0	0	Output is on
0x1	1	Output is off

1.16 STATUS_WORD

Address: 0x79
Reset: 0x0840

The STATUS_WORD command returns two bytes of information with a summary of the unit's fault condition. Based on the information in these bytes, the host can get more information by reading the appropriate status commands. The low byte of the STATUS_WORD is the same command as the STATUS_BYTE command.

Table 42 STATUS_WORD command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	VOUT	IOUT_POUT	INPUT		PG_STATUS#					OFF		IOUT_OC_FAULT	VIN_UV_FAULT	TEMP	CML	NONE_OF_THE_ABOVE
Write																
Reset	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0

Table 43 STATUS_WORD command bits description

Field	Bits	Type	Reset	Description
NONE_OF_THE_ABOVE	0	rw	0x0 (0 = 0 dec)	This bit indicates if a fault or warning not listed in bits [6:1] has occurred.
CML	1	rw	0x0 (0 = 0 dec)	This bit indicates if a communications, memory or logic fault has occurred.
TEMP	2	rw	0x0 (0 = 0 dec)	This bit indicates if a temperature fault or warning has occurred.
VIN_UV_FAULT	3	rw	0x0 (0 = 0 dec)	This bit indicates if an input undervoltage fault has occurred.
IOUT_OC_FAULT	4	rw	0x0 (0 = 0 dec)	This bit indicates if an output overcurrent fault has occurred.
RESERVED	5		0x0	
OFF	6	r	0x1 (1 = 1 dec)	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.
RESERVED	[10:7]		0X0	

(table continues...)

Table 43 (continued) STATUS_WORD command bits description

Field	Bits	Type	Reset	Description
PG_STATUS#	11	r	0x1 (1 = 1 dec)	The PG_STATUS# bit reflects the status of the PWR_GD signal. Note that this bit shows the status of the system power directly, while PWRGD_STATUS in STATUS_MFR_SPECIFIC command follows the PWRGD pin status regardless of its polarity with respect to the system power.
RESERVED	12		0x0	
INPUT	13	rw	0x0 (0 = 0 dec)	An input voltage, input current, or input power fault or warning has occurred.
IOUT_POUT	14	rw	0x0 (0 = 0 dec)	An output current or output power fault or warning has occurred.
VOUT	15	rw	0x0 (0 = 0 dec)	An output voltage fault or warning has occurred.

Table 44 NONE_OF_THE_ABOVE bit description

NONE_OF_THE_ABOVE	Value	Description
0x0	0	Fault or warning has not occurred
0x1	1	Fault or warning has occurred

Table 45 CML bit description

CML	Value	Description
0x0	0	Fault has not occurred
0x1	1	Fault has occurred

Table 46 TEMP bit description

TEMP	Value	Description
0x0	0	Fault or warning has not occurred
0x1	1	Fault or warning has occurred

Table 47 VIN_UV_FAULT bit description

VIN_UV_FAULT	Value	Description
0x0	0	Fault has not occurred
0x1	1	Fault has occcurred

Table 48 IOUT_OC_FAULT bit description

IOUT_OC_FAULT	Value	Description
0x0	0	Fault has not occurred
0x1	1	Fault has occurred

Table 49 OFF bit description

OFF	Value	Description
0x0	0	Output is on
0x1	1	Output is off

Table 50 PG_STATUS# bit description

PG_STATUS#	Value	Description
0x0	0	Output voltage is valid
0x1	1	Output voltage is not valid

Table 51 INPUT bit description

INPUT	Value	Description
0x0	0	Fault or warning has not occurred
0x1	1	Fault or warning has occurred

Table 52 IOUT_POUT bit description

IOUT_POUT	Value	Description
0x0	0	Fault or warning has not occurred
0x1	1	Fault or warning has occurred

Table 53 VOUT bit description

VOUT	Value	Description
0x0	0	Fault or warning has not occurred
0x1	1	Fault or warning has occurred

1.17 STATUS_VOUT

Address: 0x7A

Reset: 0x00

The STATUS_VOUT command returns one data byte with a summary of the output voltage faults and warnings.

Table 54 STATUS_VOUT command structure

	7	6	5	4	3	2	1	0
Read			VOUT_UV_WARN	VOUT_UV_FAULT				
Write								
Reset	0	0	0	0	0	0	0	0

Table 55 STATUS_VOUT command bits description

Field	Bits	Type	Reset	Description
RESERVED	[3:0]		0x0	
VOUT_UV_FAULT	4	rw	0x0 (0 = 0 dec)	An output undervoltage fault has occurred.
VOUT_UV_WARN	5	rw	0x0 (0 = 0 dec)	An output undervoltage warning has occurred.
RESERVED	6		0x0	
RESERVED	7		0x0	

Table 56 VOUT_UV_FAULT bit description

VOUT_UV_FAULT	Value	Description
0x0	0	Fault has not occurred
0x1	1	Fault has occurred

Table 57 VOUT_UV_WARN bit description

VOUT_UV_WARN	Value	Description
0x0	0	Warning has not occurred
0x1	1	Warning has occurred

1.18 STATUS_IOUT

Address: 0x7B
Reset: 0x00

The STATUS_IOUT command returns one data byte with a summary of the output current faults and warnings and device status.

Table 58 STATUS_IOUT command structure

	7	6	5	4	3	2	1	0
Read	IOUT_OC_FAULT		IOUT_OC_WARN			P_LIM_MODE		
Write								
Reset	0	0	0	0	0	0	0	0

Table 59 STATUS_IOUT command bits description

Field	Bits	Type	Reset	Description
RESERVED	[1:0]		0x0	
P_LIM_MODE	2	r	0x0 (0 = 0 dec)	This bit is set when the device is operating in I_REG mode.
RESERVED	[4:3]		0x0	
IOUT_OC_WARN	5	rw	0x0 (0 = 0 dec)	An output overcurrent warning has occurred.
RESERVED	6		0x0	
IOUT_OC_FAULT	7	rw	0x0 (0 = 0 dec)	An output overcurrent fault has occurred.

Table 60 P_LIM_MODE bit description

P_LIM_MODE	Value	Description
0x0	0	The device is not operating in I_REG mode
0x1	1	The device is operating in I_REG mode

Table 61 IOUT_OC_WARN bit description

IOUT_OC_WARN	Value	Description
0x0	0	Warning has not occurred
0x1	1	Warning has occurred

Table 62 IOUT_OC_FAULT bit description

IOUT_OC_FAULT	Value	Description
0x0	0	Fault has not occurred
0x1	1	Fault has occurred

1.19 STATUS_INPUT

Address: 0x7C
Reset: 0x00

The STATUS_INPUT command returns one data byte with a summary of the system input status.

Table 63 STATUS_INPUT command structure

	7	6	5	4	3	2	1	0
Read	VIN_OV_FAULT	VIN_OV_WARN	VIN_UV_WARN	VIN_UV_FAULT				
Write								
Reset	0	0	0	0	0	0	0	0

Table 64 STATUS_INPUT command bits description

Field	Bits	Type	Reset	Description
RESERVED	[3:0]		0x0	
VIN_UV_FAULT	4	rw	0x0 (0 = 0 dec)	An input undervoltage fault has occurred.
VIN_UV_WARN	5	rw	0x0 (0 = 0 dec)	An input undervoltage warning has occurred.
VIN_OV_WARN	6	rw	0x0 (0 = 0 dec)	An input overvoltage warning has occurred.
VIN_OV_FAULT	7	rw	0x0 (0 = 0 dec)	An input overvoltage fault has occurred.

Table 65 VIN_UV_FAULT bit description

VIN_UV_FAULT	Value	Description
0x0	0	Fault has not occurred
0x1	1	Fault has occurred

Table 66 VIN_UV_WARN bit description

VIN_UV_WARN	Value	Description
0x0	0	Warning has not occurred
0x1	1	Warning has occurred

Table 67 VIN_OV_WARN bit description

VIN_OV_WARN	Value	Description
0x0	0	Warning has not occurred
0x1	1	Warning has occurred

Table 68 VIN_OV_FAULT bit description

VIN_OV_FAULT	Value	Description
0x0	0	Fault has not occurred
0x1	1	Fault has occurred

1.20 STATUS_TEMPERATURE

Address: 0x7D
Reset: 0x00

The STATUS_TEMPERATURE command returns one data byte with a summary of the external temperature status.

Table 69 STATUS_TEMPERATURE command structure

	7	6	5	4	3	2	1	0
Read	OT_FAULT	OT_WARN						
Write								
Reset	0	0	0	0	0	0	0	0

Table 70 STATUS_TEMPERATURE command bits description

Field	Bits	Type	Reset	Description
RESERVED	[5:0]		0x0	
OT_WARN	6	rw	0x0 (0 = 0 dec)	An overtemperature warning has occurred.
OT_FAULT	7	rw	0x0 (0 = 0 dec)	An overtemperature fault has occurred.

Table 71 OT_WARN bit description

OT_WARN	Value	Description
0x0	0	Warning has not occurred
0x1	1	Warning has occurred

Table 72 OT_FAULT bit description

OT_FAULT	Value	Description
0x0	0	Fault has not occurred
0x1	1	Fault has occurred

1.21 STATUS_CML

Address: 0x7E

Reset: 0x00

The STATUS_CML command returns one data byte with a summary of the communication interface and memory status.

Table 73 STATUS_CML command structure

	7	6	5	4	3	2	1	0
Read	INVALID_CMD	INVALID_DATA	PEC_FAIL	MEM_FAULT			OTHER	
Write								
Reset	0	0	0	0	0	0	0	0

Table 74 STATUS_CML command bits description

Field	Bits	Type	Reset	Description
RESERVED	0		0x0	
OTHER	1	rw	0x0 (0 = 0 dec)	A Miscellaneous communications fault has occurred.
RESERVED	[3:2]		0x0	
MEM_FAULT	4	rw	0x0 (0 = 0 dec)	An OTP fault has occurred.
PEC_FAIL	5	rw	0x0 (0 = 0 dec)	Packet Error Check status.
INVALID_DATA	6	rw	0x0 (0 = 0 dec)	Invalid or unsupported data received.
INVALID_CMD	7	rw	0x0 (0 = 0 dec)	Invalid or unsupported command received.

Table 75 OTHER bit description

OTHER	Value	Description
0x0	0	No misc fault has occurred
0x1	1	Misc fault has occurred

Table 76 MEM_FAULT bit description

MEM_FAULT	Value	Description
0x0	0	Fault has not occurred
0x1	1	Fault has occurred

Table 77 PEC_FAIL bit description

PEC_FAIL	Value	Description
0x0	0	Packet Error Check hasn't failed
0x1	1	Packet Error Check failed

Table 78 INVALID_DATA bit description

INVALID_DATA	Value	Description
0x0	0	Invalid or unsupported data not received
0x1	1	Invalid or unsupported data received

Table 79 INVALID_CMD bit description

INVALID_CMD	Value	Description
0x0	0	Invalid or unsupported command not received
0x1	1	Invalid or unsupported command received

1.22 STATUS_MFR_SPECIFIC

Address: 0x80
Reset: 0x00

The STATUS_MFR_SPECIFIC command returns one data byte with a summary of the general device status.

Table 80 STATUS_MFR_SPECIFIC command structure

	7	6	5	4	3	2	1	0
Read	IOUT_UC_WARN	STATUS_LATCH_OFF	SOC_FAULT	WATCHDOG_FAULT	OTP_STATUS	GATE_STATUS		PWRGD_STATUS
Write								
Reset	0	0	0	0	0	0	0	0

Table 81 STATUS_MFR_SPECIFIC command bits description

Field	Bits	Type	Reset	Description
PWRGD_STATUS	0	rw	0x0 (0 = 0 dec)	PWRGD signal status. Note that this bit follows the PWRGD pin status, while PG_STATUS in STATUS_WORD command shows the status of the system power directly.
GATE_STATUS	1	r	0x0 (0 = 0 dec)	Shows the status of the GATE pin.
OTP_STATUS	3	rw	0x0 (0 = 0 dec)	OTP read or program error.
WATCHDOG_FAULT	4	rw	0x0 (0 = 0 dec)	A Turn-on Watchdog fault has occurred.
SOC_FAULT	5	rw	0x0 (0 = 0 dec)	An SOC fault has occurred.

(table continues...)

Table 81 (continued) STATUS_MFR_SPECIFIC command bits description

Field	Bits	Type	Reset	Description
STATUS_LATCH_OFF	6	r	0x0 (0 = 0 dec)	Device latch-off status.
IOUT_UC_WARN	7	rw	0x0 (0 = 0 dec)	An undercurrent warning has occurred.

Table 82 PWRGD_STATUS bit description

PWRGD_STATUS	Value	Description
0x0	0	PWRGD pin is deasserted
0x1	1	PWRGD pin is asserted

Table 83 GATE_STATUS bits description

GATE_STATUS	Value	Description
0x0 (00 bin)	0	GATE pin is low (GATE < 1 V)
0x1 (01 bin)	1	GATE pin is high (GATE > 7.8 V)
0x2 (10 bin)	10	1 V < GATE < 7.8 V
0x3 (11 bin)	11	RESERVED

Table 84 OTP_STATUS bit description

OTP_STATUS	Value	Description
0x0	0	No error detected
0x1	1	Error detected

Table 85 WATCHDOG_FAULT bit description

WATCHDOG_FAULT	Value	Description
0x0	0	Fault has not occurred
0x1	1	Fault has occurred

Table 86 SOC_FAULT bit description

SOC_FAULT	Value	Description
0x0	0	Fault has not occurred
0x1	1	Fault has occurred

Table 87 STATUS_LATCH_OFF bit description

STATUS_LATCH_OFF	Value	Description
0x0	0	Device is not in latch off status.
0x1	1	Device is in latch off status.

Table 88 IOUT_UC_WARN bit description

IOUT_UC_WARN	Value	Description
0x0	0	Warning has not occurred
0x1	1	Warning has occurred

1.23 READ_EIN

Address: 0x86
Reset: 0x000000000000

The READ_EIN command returns the input energy reading.

Table 89 READ_EIN command bits description

Field	Bits	Type	Reset	Description
ENERGY_COUNT	[15:0]	r	0x0000 (0 dec)	Output of an accumulator that continuously sums samples of the instantaneous input power
ROLLOVER_COUNT	[23:16]	r	0x00 (0 dec)	Unsigned integer that will periodically roll over from its maximum positive value to zero
SAMPLE_COUNT	[47:24]	r	0x000000 (0 dec)	Unsigned integer that counts the number of samples of the instantaneous input power

1.24 READ_VIN

Address: 0x88
Reset: 0x0000

The READ_VIN command returns the input voltage reading.

Table 90 READ_VIN command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read					READ_VIN											
Write																

(table continues...)

Table 90 (continued) READ_VIN command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 91 READ_VIN command bits description

Field	Bits	Type	Reset	Description
READ_VIN	[11:0]	r	0x000 (0 dec)	Input voltage reading in direct format.
RESERVED	[15:12]		0x0	

1.25 READ_VOUT

Address: 0x8B
Reset: 0x0000

The READ_VOUT command returns the output voltage reading.

Table 92 READ_VOUT command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read					READ_VOUT											
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 93 READ_VOUT command bits description

Field	Bits	Type	Reset	Description
READ_VOUT	[11:0]	r	0x000 (0 dec)	Output voltage reading in direct format.
RESERVED	[15:12]		0x0	

1.26 READ_IOUT

Address: 0x8C
Reset: 0x0000

The READ_IOUT command returns the reading of the current flow through the sense resistor.

Table 94 READ_IOUT command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read					READ_IOUT											
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 95 READ_IOUT command bits description

Field	Bits	Type	Reset	Description
READ_IOUT	[11:0]	r	0x000 (0 dec)	Current reading in direct format.
RESERVED	[15:12]		0x0	

1.27 READ_TEMPERATURE_1

Address: 0x8D
Reset: 0x0000

The READ_TEMPERATURE_1 command returns the reading of the external temperature measured between TSNS_P and TSNS_N pins.

Table 96 READ_TEMPERATURE_1 command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read					READ_TEMPERATURE_1											
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 97 READ_TEMPERATURE_1 command bits description

Field	Bits	Type	Reset	Description
READ_TEMPERATURE_1	[11:0]	r	0x000 (0 dec)	External temperature reading in direct format.
RESERVED	[15:12]		0x0	

1.28 READ_TEMPERATURE_2

Address: 0x8E
Reset: 0x0000

The READ_TEMPERATURE_2 command returns the reading of the On-chip temperature measured by the internal temperature sensor in direct format.

Table 98 READ_TEMPERATURE_2 command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read					READ_TEMPERATURE_2											
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 99 READ_TEMPERATURE_2 command bits description

Field	Bits	Type	Reset	Description
READ_TEMPERATURE_2	[11:0]	r	0x000 (0 dec)	Internal temperature reading in direct format.
RESERVED	[15:12]		0x0	

1.29 READ_PIN

Address: 0x97
Reset: 0x0000

The READ_PIN command returns the input power reading in direct format.

Table 100 READ_PIN command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	READ_PIN															
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 101 READ_PIN command bits description

Field	Bits	Type	Reset	Description
READ_PIN	[15:0]	r	0x0000 (0 dec)	Input power reading in direct format.

1.30 PMBUS_REVISION

Address: 0x98
Reset: 0x33

Stores the revision of the PMBus to which the device is compliant.

Table 102 PMBUS_REVISION command structure

	7	6	5	4	3	2	1	0
Read	PMBUS_P1_REVISION				PMBUS_P2_REVISION			
Write								
Reset	0	0	1	1	0	0	1	1

Table 103 PMBUS_REVISION command bits description

Field	Bits	Type	Reset	Description
PMBUS_P2_REVISION	[3:0]	r	0x3 (3 dec)	0x3 indicates part 2 is revision 1.3

(table continues...)

Table 103 (continued) PMBUS_REVISION command bits description

Field	Bits	Type	Reset	Description
PMBUS_P1_REVISION	[7:4]	r	0x3 (3 dec)	0x3 indicates part 1 is revision 1.3

1.31 MFR_ID

Address: 0x99
Reset: 0x004946

Manufacturer ID according to ISO/IEC 8859-1 [A05].

Table 104 MFR_ID command structure

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	MFR_ID																							
Write																								
Reset	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	1	0	1	0	0	0	1	1	0

Table 105 MFR_ID command bits description

Field	Bits	Type	Reset	Description
MFR_ID	[23:0]	r	0x004946 (18758 dec)	Manufacturer's ID

1.32 MFR_MODEL

Address: 0x9A
Reset: 0x0000000000000001

Table 106 MFR_MODEL command bits description

Field	Bits	Type	Reset	Description
MFR_MODEL	[63:0]	r	0x0000000000000001 (1 dec)	Manufacturer model

1.33 MFR_REVISION

Address: 0x9B
Reset: 0x0000

Table 107 MFR_REVISION command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	MFR_REVISION															
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 108 MFR_REVISION command bits description

Field	Bits	Type	Reset	Description
MFR_REVISION	[15:0]	r	0x0000 (0 dec)	Manufacturer revision

1.34 PMBUS_CFG

Address: 0xD0
Reset: 0x10
Included in OTP

Configuration command for PMbus device address and speed selection

Table 109 PMBUS_CFG command structure

	7	6	5	4	3	2	1	0
Read	PMBUS_SPEED	PMBUS_BASE_ADDR			PMBUS_DEVICE_ADDR			
Reset	0	0	0	1	0	0	0	0

Table 110 PMBUS_CFG command bits description

Field	Bits	Type	Reset	Description
PMBUS_DEVICE_ADDR	[3:0]	rw	0x0 (0 dec)	LSB part of the pmbus address [3:0]
PMBUS_BASE_ADDR	[6:4]	rw	0x1 (1 dec)	MSB part of the pmbus address [6:4]
PMBUS_SPEED	7	rw	0x0 (0 = 0 dec)	Operating PMbus speed

Table 111 PMBUS_SPEED configuration

PMBUS_SPEED	Value	Description
0x0	0	Fast Mode Plus
0x1	1	Standard or Fast Mode

1.35 MODE

Address: 0xD1

Reset: 0x7F
Included in OTP

Table 112 MODE command structure

	7	6	5	4	3	2	1	0
Read		MODE	FET_SELECT					
Write								
Reset	0	1	1	1	1	1	1	1

Table 113 MODE command bits description

Field	Bits	Type	Reset	Description
FET_SELECT	[5:0]	rw	0x3F (111111 = 63 dec)	FET_SELECT bits select FET and SOA curve to be used from a list of pre-programmed ones.
MODE	6	rw	0x1 (DIGITAL = 1 dec)	MODE bit selects the UV, OV and OUV fault sources in Fully Digital mode. Either analog comparators at the UV/EN, OV and FB pins are used to trigger the UV, OV and OUV faults; or ADC conversions results will be compared digitally with the VIN_UV_FAULT_LIMIT, VIN_OV_FAULT_LIMIT and VOUT_UV_FAULT_LIMIT to trigger the faults.
RESERVED	7		0x0	

Table 114 FET Selection

FET_SELECT	Value	Description
0x00 (00 0000 bin)	0	BSC027N10NS5ATMA1 – DC Line
0x01 (00 0001 bin)	1	BSC035N10NS5ATMA1 – DC Line
0x02 (00 0010 bin)	10	Reserved
0x03 (00 0011 bin)	11	IPT015N10N5ATMA1 – DC Line
0x04 (00 0100 bin)	100	IPB017N10N5ATMA1 – DC Line
0x05 (00 0101 bin)	101	IPB017N10N5LFATMA1 – DC Line
0x06 (00 0110 bin)	110	IPB020N10N5ATMA1 – DC Line
0x07 (00 0111 bin)	111	IPB020N10N5LFATMA1– DC Line
0x08 (00 1000 bin)	1000	IPB027N10N5ATMA1 – DC Line
0x09 (00 1001 bin)	1001	IPB032N10N5ATMA1 – DC Line
0x0A (00 1010 bin)	1010	IPB033N10N5LFATMA1 – DC Line
0x0B (00 1011 bin)	1011	Reserved

(table continues...)

Table 114 (continued) FET Selection

FET_SELECT	Value	Description
0x0C (00 1100 bin)	1100	IPB072N15N3 – DC Line
0x0D (00 1101 bin)	1101	IPB042N10 – DC Line
0x0E (00 1110 bin)	1110	IPT016N10NM5LF – DC Line
0x0F (00 1111 bin)	1111	Reserved
0x10 (01 0000 bin)	10000	Reserved
0x11 (01 0001 bin)	10001	Reserved
0x12 (01 0010 bin)	10010	Reserved
0x13 (01 0011 bin)	10011	Reserved
0x14 (01 0100 bin)	10100	Reserved
0x15 (01 0101 bin)	10101	Reserved
0x16 (01 0110 bin)	10110	Reserved
0x17 (01 0111 bin)	10111	Reserved
0x18 (01 1000 bin)	11000	Reserved
0x19 (01 1001 bin)	11001	Reserved
0x1A (01 1010 bin)	11010	Reserved
0x1B (01 1011 bin)	11011	Reserved
0x1C (01 1100 bin)	11100	Reserved
0x1D (01 1101 bin)	11101	Reserved
0x1E (01 1110 bin)	11110	Reserved
0x1F (01 1111 bin)	11111	Reserved
0x20 (10 0000 bin)	100000	BSC027N10NS5ATMA1 – 10ms Line
0x21 (10 0001 bin)	100001	BSC035N10NS5ATMA1 – 10ms Line
0x22 (10 0010 bin)	100010	Reserved
0x23 (10 0011 bin)	100011	IPT015N10N5ATMA1 – 10ms Line
0x24 (10 0100 bin)	100100	IPB017N10N5ATMA1 – 10ms Line
0x25 (10 0101 bin)	100101	IPB017N10N5LFATMA1 – 10ms Line
0x26 (10 0110 bin)	100110	IPB020N10N5ATMA1 – 10ms Line
0x27 (10 0111 bin)	100111	IPB020N10N5LFATMA1 – 10ms Line
0x28 (10 1000 bin)	101000	IPB027N10N5ATMA1 – 10ms Line
0x29 (10 1001 bin)	101001	IPB032N10N5ATMA1 – 10ms Line
0x2A (10 1010 bin)	101010	IPB033N10N5LFATMA1 – 10ms Line
0x2B (10 1011 bin)	101011	Reserved
0x2C (10 1100 bin)	101100	IPB072N15N3 – 10ms Line
0x2D (10 1101 bin)	101101	IPB042N10 – 10ms Line

(table continues...)

Table 114 (continued) FET Selection

FET_SELECT	Value	Description
0x2E (10 1110 bin)	101110	IPT016N10NM5LF – 10ms Line
0x2F (10 1111 bin)	101111	Reserved
0x30 (11 0000 bin)	110000	Reserved
0x31 (11 0001 bin)	110001	Reserved
0x32 (11 0010 bin)	110010	Reserved
0x33 (11 0011 bin)	110011	Reserved
0x34 (11 0100 bin)	110100	Reserved
0x35 (11 0101 bin)	110101	Reserved
0x36 (11 0110 bin)	110110	Reserved
0x37 (11 0111 bin)	110111	Reserved
0x38 (11 1000 bin)	111000	Reserved
0x39 (11 1001 bin)	111001	Reserved
0x3A (11 1010 bin)	111010	Reserved
0x3B (11 1011 bin)	111011	Reserved
0x3C (11 1100 bin)	111100	Reserved
0x3D (11 1101 bin)	111101	Reserved
0x3E (11 1110 bin)	111110	Reserved
0x3F (11 1111 bin)	111111	SOA OTP

Table 115 MODE configuration

MODE	Value	Description
0x0	ANALOG	Analog Comparators Mode (ACM)
0x1	DIGITAL	Digital Comparators Mode (DCM)

1.36 SOA

Address: 0xD2
Reset: 0x0000
Included in OTP

Configures SOA of FET in case it is not pre-programmed. This command is a 16 bit FIFO.

Table 116 SOA word structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read																

(table continues...)

Table 116 (continued) SOA word structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	SOA															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

How to enter data:

1. Write to SOA command with LSB SOA data where the first word contains bytes for 1V and 2V SOA data.
2. Continue filling FIFO until all 41 words are filled. The 41st word contains the I and P coefficients of control loop and gate current regulation IDAC_FS_SEL:

Table 117 SOA FIFO 41st word structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read																
Write									I_COEFF			P_COEFF			IDAC_FS_SEL	

Table 118 IDAC_FS_SEL bits description

IDAC_FS_SEL	Value	Description
0x0	0	31uA
0x1	1	62uA
0x2	2	124uA
0x3	3	248uA

3. Enter last word containing CRC16 code
4. CRC Code checked against data entered into the FIFO
5. Once the FIFO is full the SOA_FULL status byte is set to 1'b1
6. If the FIFO is full the CRC check is performed and the SOA_CRC status bit is set to 1'b1

CRC16 algoritm:
- The CRC16-CCITT algorithm is used.
- Width = 16 bits
- Truncated polynomial = 0x1021
- Initial value = 0xFFFF

Table 119 SOA word bits description

Field	Bits	Type	Reset	Description
SOA	[15:0]	w	0x0000 (0 dec)	

1.37 REG_CFG

Address: 0xD3
Reset: 0x0503
Included in OTP

Regulation configuration command.

Table 120 REG_CFG command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read						BOOSTMODE_DC		BOOSTMODE_TMR	BOOSTMODE_EN	RMS_EN	RSNS					
Write																
Reset	0	0	0	0	0	1	0	1	0	0	0	0	0	0	1	1

Table 121 REG_CFG command bits description

Field	Bits	Type	Reset	Description
RSNS	[5:0]	rw	0x03 (3 = 3 dec)	The RSNS bit field is used to set the ratio of the voltage at the current sense pins to the sensed current, in other words, the value of the sense resistor.
RMS_EN	6	rw	0x0 (Disable = 0 dec)	RMS_EN bit enables or disables the RMS calculation function of the overcurrent (OC) protection. If enabled, protection level will be based on RMS calculation instead of instant measurement. RMS is a sub-function of OC. Therefore, OC has to be enabled if RMS function is desired.
BOOSTMODE_EN	7	rw	0x0 (0 = 0 dec)	The BOOSTMODE_EN bit enables or disables the boost mode feature.
BOOSTMODE_TMR	8	rw	0x1 (1ms = 1 dec)	BOOSTMODE_TMR sets the time for which the current is to be regulated to 4*I_SOA in the second phase of the boost mode feature unless ROM target is 0, where 0.5A shall be the target.
BOOSTMODE_DC	[10:9]	rw	0x2 (10 = 2 dec)	BOOSTMODE_DC sets the duty cycle the current is to be regulated to smallest LSB in the third phase of the boost mode feature.
RESERVED	[15:11]		0x00	

Table 122 RSNS configuration

RSNS	Value	Description
0x00 (00 0000 bin)	0	0.25mΩ
0x01 (00 0001 bin)	1	0.3 mΩ
0x02 (00 0010 bin)	2	0.4 mΩ
0x03 (00 0011 bin)	3	0.5 mΩ
0x04 (00 0100 bin)	4	0.6 mΩ
0x05 (00 0101 bin)	5	0.7 mΩ
0x06 (00 0110 bin)	6	0.75 mΩ
0x07 (00 0111 bin)	7	0.8 mΩ
0x08 (00 1000 bin)	8	0.9 mΩ
0x09 (00 1001 bin)	9	1 mΩ
0x0A (00 1010 bin)	0a	1.1 mΩ
0x0B (00 1011 bin)	0b	1.2 mΩ
0x0C (00 1100 bin)	0c	1.25 mΩ
0x0D (00 1101 bin)	0d	1.3 mΩ
0x0E (00 1110 bin)	0e	1.4 mΩ
0x0F (00 1111 bin)	0f	1.5 mΩ
0x10 (01 0000 bin)	10	1.6 mΩ
0x11 (01 0001 bin)	11	1.7 mΩ
0x12 (01 0010 bin)	12	1.8 mΩ
0x13 (01 0011 bin)	13	1.9 mΩ
0x14 (01 0100 bin)	14	2 mΩ
0x15 (01 0101 bin)	15	2.1 mΩ
0x16 (01 0110 bin)	16	2.2 mΩ
0x17 (01 0111 bin)	17	2.3 mΩ
0x18 (01 1000 bin)	18	2.4 mΩ
0x19 (01 1001 bin)	19	2.5 mΩ
0x1A (01 1010 bin)	1a	2.6 mΩ
0x1B (01 1011 bin)	1b	2.7 mΩ
0x1C (01 1100 bin)	1c	2.8 mΩ
0x1D (01 1101 bin)	1d	3 mΩ
0x1E (01 1110 bin)	1e	3.1 mΩ
0x1F (01 1111 bin)	1f	3.2 mΩ
0x20 (10 0000 bin)	20	3.3 mΩ
0x21 (10 0001 bin)	21	3.4 mΩ

(table continues...)

Table 122 (continued) RSNS configuration

RSNS	Value	Description
0x22 (10 0010 bin)	22	3.5 mΩ
0x23 (10 0011 bin)	23	3.6 mΩ
0x24 (10 0100 bin)	24	3.7 mΩ
0x25 (10 0101 bin)	25	3.8 mΩ
0x26 (10 0110 bin)	26	3.9 mΩ
0x27 (10 0111 bin)	27	4 mΩ
0x28 (10 1000 bin)	28	4.1 mΩ
0x29 (10 1001 bin)	29	4.2 mΩ
0x2A (10 1010 bin)	2a	4.3 mΩ
0x2B (10 1011 bin)	2b	4.4 mΩ
0x2C (10 1100 bin)	2c	4.5 mΩ
0x2D (10 1101 bin)	2d	4.6 mΩ
0x2E (10 1110 bin)	2e	4.7 mΩ
0x2F (10 1111 bin)	2f	4.8 mΩ
0x30 (11 0000 bin)	30	4.9 mΩ
0x31 (11 0001 bin)	31	5 mΩ
0x32 (11 0010 bin)	32	5.2 mΩ
0x33 (11 0011 bin)	33	5.5 mΩ
0x34 (11 0100 bin)	34	5.8 mΩ
0x35 (11 0101 bin)	35	6 mΩ
0x36 (11 0110 bin)	36	6.2 mΩ
0x37 (11 0111 bin)	37	6.5 mΩ
0x38 (11 1000 bin)	38	6.8 mΩ
0x39 (11 1001 bin)	39	7 mΩ
0x3A (11 1010 bin)	3a	7.5 mΩ
0x3B (11 1011 bin)	3b	8 mΩ
0x3C (11 1100 bin)	3c	8.5 mΩ
0x3D (11 1101 bin)	3d	9 mΩ
0x3E (11 1110 bin)	3e	9.5 mΩ
0x3F (11 1111 bin)	3f	10 mΩ

Table 123 RMS_EN bit description

RMS_EN	Value	Description
0x0	Disable	RMS Disabled
0x1	Enable	RMS Enabled

Table 124 BOOSTMODE_EN bit description

BOOSTMODE_EN	Value	Description
0x0	0	Boost Mode disabled.
0x1	1	Boost Mode enabled.

Table 125 BOOSTMODE timer configuration

BOOSTMODE_TMR	Value	Description
0x0	100us	100us pulse
0x1	1ms	1 ms pulse

Table 126 BOOSTMODE duty cycle confiuration

BOOSTMODE_DC	Value	Description
0x0 (00 bin)	0	2 %
0x1 (01 bin)	1	5 %
0x2 (10 bin)	10	10 %
0x3 (11 bin)	11	20 %

1.38 V_SNS_CFG

Address: 0xD4
Reset: 0x28
Included in OTP

Voltage sense configuration command.

Table 127 V_SNS_CFG command structure

	7	6	5	4	3	2	1	0
Read			OVIN_FAULT_LIMIT				VTLM_RNG	
Write								
Reset	0	0	1	0	1	0	0	0

Table 128 V_SNS_CFG command bits description

Field	Bits	Type	Reset	Description
VTLM_RNG	[1:0]	rw	0x0 (0 = 0 dec)	VTLM_RNG sets monitored voltage range for input and output voltages.
RESERVED	[3:2]		0x2	
OVIN_FAULT_LIMIT	[5:4]	rw	0x2 (10 = 2 dec)	OVIN_FAULT_LIMIT bit field sets the value of the input voltage measured at the ISNS_P pin that causes input (OVin) overvoltage fault.
RESERVED	[7:6]		0x0	

Table 129 VTLM_RNG level configuration

VTLM_RNG	Value	Description
0x0 (00 bin)	0	88V
0x1 (01 bin)	1	44V
0x2 (10 bin)	10	22V
0x3 (11 bin)	11	RESERVED

Table 130 OVIN_FAULT_LIMIT configuration

OVIN_FAULT_LIMIT	Value	Description
0x0 (00 bin)	0	70V
0x1 (01 bin)	1	75V
0x2 (10 bin)	10	80V
0x3 (11 bin)	11	85V

1.39 I_SNS_CFG

Address: 0xD5
Reset: 0xB418
Included in MTP

Current Sense Configuration command.

Table 131 I_SNS_CFG command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	CS_RNG_TRIM								CS_RNG		SOC_FAULT_LIMIT			START_ILIM		
Reset	1	0	1	1	0	1	0	0	0	0	0	1	1	0	0	0

Table 132 I_SNS_CFG command bits description

Field	Bits	Type	Reset	Description
START_ILIM	[2:0]	rw	0x0 (0 = 0 dec)	START_ILIM bit field sets startup current (IST) limit.
SOC_FAULT_LIMIT	[5:3]	rw	0x3 (3 dec)	The SOC_FAULT_LIMIT bits set the level of the voltage drop on the sense resistor at which the SOC fault is triggered.
CS_RNG	[7:6]	rw	0x0 (0 = 0 dec)	CS_RNG bit field sets current sense differential voltage range
CS_RNG_TRIM	[15:8]	rw	0xB4 (180 dec)	The CS_RNG_TRIM bits set the level below the V_SNS_CS voltage measured at the ISNS_x pins that causes an output overcurrent fault. If RMS_EN bit in REG_CFG command is set, CS_RNG_TRIM bits specify the RMS current level (as a proportion of V_SNS_CS) at which the OC fault is triggered. Max value of this bit field is 0xB4. If a value higher than this is programmed, it will be limited to 0xB4.

Table 133 Startup current limit (in % of OC)

START_ILIM	Value	Description
0x0 (000 bin)	0	100% of OC
0x1 (001 bin)	1	87.5% of OC
0x2 (010 bin)	10	75% of OC
0x3 (011 bin)	11	62.5% of OC
0x4 (100 bin)	100	50% of OC
0x5 (101 bin)	101	37.5% of OC
0x6 (110 bin)	110	25% of OC
0x7 (111 bin)	111	12.5% of OC

Table 134 Configuration of SOC levels

SOC_FAULT_LIMIT	CS_RNG	
	2'b0x	2'b1x
0x0 (000 bin)	12.5 mV	25 mV
0x1 (001 bin)	18.75 mV	37.5 mV
0x2 (010 bin)	25 mV	50 mV
0x3 (011 bin)	37.5 mV	75 mV
0x4 (100 bin)	50 mV	100 mV

(table continues...)

Table 134 (continued) Configuration of SOC levels

0x5 (101 bin)	75 mV	150 mV
0x6 (110 bin)	100 mV	200 mV
0x7 (111 bin)	150 mV	300 mV

Table 135 Current sense differential voltage range

CS_RNG	Value	Description
0x0 (00 bin)	0	12.5 mV
0x1 (01 bin)	1	25 mV
0x2 (10 bin)	10	50 mV
0x3 (11 bin)	11	100 mV

1.40 I_SNS_OFFSET_COMP

Address: 0xD6
Reset: 0x0000
Included in OTP

This command specifies a systematic offset to compensate the current sense measurements in the application.

Table 136 I_SNS_OFFSET_COMP command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read						I_SNS_OFFSET_COMP										
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 137 I_SNS_OFFSET_COMP command bits description

Field	Bits	Type	Reset	Description
I_SNS_OFFSET_COMP	[10:0]	rw	0x000 (0 dec)	Value is a signed integer from -1023 to 1023, specified in 2's complement.
RESERVED	[15:11]		0x00	

1.41 TSNS_LVL_CTRL

Address: 0xD7
Reset: 0x078A
Included in OTP

Temperature calibration.

Table 138 TSNS_LVL_CTRL command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read					TSNS_LVL_CTRL											
Write																
Reset	0	0	0	0	0	1	1	1	1	0	0	0	1	0	1	0

Table 139 TSNS_LVL_CTRL command bits description

Field	Bits	Type	Reset	Description
TSNS_LVL_CTRL	[11:0]	rw	0x78A (1930 dec)	Always leave this command to its default value 0x078A.
RESERVED	[15:12]		0x0	

1.42 WATCHDOG_TMR

Address: 0xD8
Reset: 0x37
Included in OTP

Turn-on watchdog configuration.

Table 140 WATCHDOG_TMR command structure

	7	6	5	4	3	2	1	0
Read			EN_DG			WATCHDOG		
Write								
Reset	0	0	1	1	0	1	1	1

Table 141 WATCHDOG_TMR command bits description

Field	Bits	Type	Reset	Description
WATCHDOG	[2:0]	rw	0x7 (111 = 7 dec)	WATCHDOG sets an upper limit, in ms, on how long the unit can attempt to power up the output without fully enhancing the FET.
EN_DG	[5:3]	rw	0x6 (110 = 6 dec)	EN_DG bit field sets the deglitch time, in ms, from the moment when the UV/EN pin crosses the V_UVEN_UTH until the INIT_SOA_REG phase starts.
RESERVED	[7:6]		0x0	

Table 142 WATCHDOG timer configuration

WATCHDOG	Value	Description
0x0 (000 bin)	0	10 ms

(table continues...)

Table 142 (continued) WATCHDOG timer configuration

WATCHDOG	Value	Description
0x1 (001 bin)	1	20 ms
0x2 (010 bin)	10	50 ms
0x3 (011 bin)	11	100 ms
0x4 (100 bin)	100	200 ms
0x5 (101 bin)	101	500 ms
0x6 (110 bin)	110	1000 ms
0x7 (111 bin)	111	10000 ms

Table 143 Enable deglitch configuration

EN_DG	Value	Description
0x0 (000 bin)	0	0 ms
0x1 (001 bin)	1	4 ms
0x2 (010 bin)	10	8 ms
0x3 (011 bin)	11	16 ms
0x4 (100 bin)	100	32 ms
0x5 (101 bin)	101	64 ms
0x6 (110 bin)	110	128 ms
0x7 (111 bin)	111	256 ms

1.43 V_TMR

Address: 0xD9
Reset: 0x0FFF
Included in OTP

Voltage faults timers.

Table 144 V_TMR command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read		OVIN_TMR						OUV_TMR			OV_TMR			UV_TMR		
Write																
Reset	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

Table 145 V_TMR command bits description

Field	Bits	Type	Reset	Description
UV_TMR	[2:0]	rw	0x7 (111 = 7 dec)	UV_TMR specifies the amount of operating time in undervoltage conditions before fault is triggered.
OV_TMR	[5:3]	rw	0x7 (111 = 7 dec)	OV_TMR specifies the amount of operating time in overvoltage conditions before fault is triggered.
OUV_TMR	[8:6]	rw	0x7 (111 = 7 dec)	OUV_TMR specifies the amount of operating time in output-undervoltage conditions before fault is triggered.
RESERVED	[11:9]		0x7	
OVIN_TMR	[14:12]	rw	0x0 (0 = 0 dec)	OVIN_TMR specifies the amount of operating time in input-overvoltage conditions before fault is triggered.
RESERVED	15		0x0	

Table 146 UV_TMR configuration

UV_TMR	Value	Description
0x0 (000 bin)	0	0 ms
0x1 (001 bin)	1	1 ms
0x2 (010 bin)	10	5 ms
0x3 (011 bin)	11	10 ms
0x4 (100 bin)	100	50 ms
0x5 (101 bin)	101	100 ms
0x6 (110 bin)	110	500 ms
0x7 (111 bin)	111	1000 ms

Table 147 OV_TMR configuration

OV_TMR	Value	Description
0x0 (000 bin)	0	0 ms
0x1 (001 bin)	1	1 ms
0x2 (010 bin)	10	5 ms
0x3 (011 bin)	11	10 ms
0x4 (100 bin)	100	50 ms
0x5 (101 bin)	101	100 ms
0x6 (110 bin)	110	500 ms

(table continues...)

Table 147 (continued) OV_TMR configuration

OV_TMR	Value	Description
0x7 (111 bin)	111	1000 ms

Table 148 OUV_TMR configuration

OUV_TMR	Value	Description
0x0 (000 bin)	0	0 ms
0x1 (001 bin)	1	1 ms
0x2 (010 bin)	10	5 ms
0x3 (011 bin)	11	10 ms
0x4 (100 bin)	100	50 ms
0x5 (101 bin)	101	100 ms
0x6 (110 bin)	110	500 ms
0x7 (111 bin)	111	1000 ms

Table 149 OVIN_TMR configuration

OVIN_TMR	Value	Description
0x0 (000 bin)	0	0µs
0x1 (001 bin)	1	10µs
0x2 (010 bin)	10	20µs
0x3 (011 bin)	11	50µs
0x4 (100 bin)	100	100µs
0x5 (101 bin)	101	200µs
0x6 (110 bin)	110	500µs
0x7 (111 bin)	111	1000µs

1.44 PIN_POLARITY

Address: 0xDA
Reset: 0x01
Included in OTP

Configures polarity of PWRGD, FAULT and WARN pins.

Table 150 PIN_POLARITY command structure

	7	6	5	4	3	2	1	0
Read						WARN_POLARITY	FAULT_POLARITY	PWRGD_POLARITY
Write								
Reset	0	0	0	0	0	0	0	1

Table 151 PIN_POLARITY bits description

Field	Bits	Type	Reset	Description
PWRGD_POLARITY	0	rw	0x1 (1 = 1 dec)	Configures polarity of PWRGD pin.
FAULT_POLARITY	1	rw	0x0 (0 = 0 dec)	Configures polarity of FAULT pin.
WARN_POLARITY	2	rw	0x0 (0 = 0 dec)	Configures polarity of WARN pin.
RESERVED	[7:3]		0x0	

Table 152 PWRGD_POLARITY configuration

PWRGD_POLARITY	Value	Description
0x0	0	Active low
0x1	1	Active high

Table 153 FAULT_POLARITY configuration

FAULT_POLARITY	Value	Description
0x0	0	Active low
0x1	1	Active high

Table 154 WARN_POLARITY configuration

WARN_POLARITY	Value	Description
0x0	0	Active low
0x1	1	Active high

1.45 GPO_CFG

Address: 0xDB
Reset: 0x0000
Included in OTP

GPO configuration.

Table 155 GPO_CFG command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read									GPO3_CFG	GPO2_CFG	GPO1_CFG	GPO0_CFG	GPO3_ST	GPO2_ST	GPO1_ST	GPO0_ST
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 156 GPO_CFG command bits description

Field	Bits	Type	Reset	Description
GPO0_ST	0	rw	0x0 (0 = 0 dec)	ST bits set the state (high or low) of the pins when they are configured as GPOs. GPO0_ST bit doesn't have any effect when pin is configured as FAULT.
GPO1_ST	1	rw	0x0 (0 = 0 dec)	ST bits set the state (high or low) of the pins when they are configured as GPOs. GPO1_ST bit doesn't have any effect when pin is configured as WARN.
GPO2_ST	2	rw	0x0 (0 = 0 dec)	ST bits set the state (high or low) of the pins when they are configured as GPOs.
GPO3_ST	3	rw	0x0 (0 = 0 dec)	ST bits set the state (high or low) of the pins when they are configured as GPOs.
GPO0_CFG	4	rw	0x0 (0 = 0 dec)	Configures GPO0 as FAULT pin or general purpose output.
GPO1_CFG	5	rw	0x0 (0 = 0 dec)	Configures GPO1 as WARN pin or general purpose output.
GPO2_CFG	6	rw	0x0 (0 = 0 dec)	Enables or disables GPO2.
GPO3_CFG	7	rw	0x0 (0 = 0 dec)	Enables or disables GPO3.
RESERVED	[15:8]		0x0	

Table 157 GPO0 status

GPO0_ST	Value	Description
0x0	0	Output low.
0x1	1	Output high.

Table 158 GPO1 status

GPO1_ST	Value	Description
0x0	0	Output low.
0x1	1	Output high.

Table 159 GPO2 status

GPO2_ST	Value	Description
0x0	0	Output low.
0x1	1	Output high.

Table 160 GPO3 status

GPO3_ST	Value	Description
0x0	0	Output low.
0x1	1	Output high.

Table 161 GPO0 configuration

GPO0_CFG	Value	Description
0x0	0	Pin is configured as FAULT.
0x1	1	Pin is configured as GPO.

Table 162 GPO1 configuration

GPO1_CFG	Value	Description
0x0	0	Pin is configured as WARN.
0x1	1	Pin is configured as GPO.

Table 163 GPO2 configuration

GPO2_CFG	Value	Description
0x0	0	GPO functionality is disabled.
0x1	1	Pin is configured as GPO.

Table 164 GPO3 configuration

GPO3_CFG	Value	Description
0x0	0	GPO functionality is disabled.
0x1	1	Pin is configured as GPO.

1.46 IOUT_UC_WARN_LIMIT

Address: 0xDC

Reset: 0x0000
Included in OTP

The IOUT_UC_WARN_LIMIT command sets the level of current that causes an output undercurrent warning.

Table 165 IOUT_UC_WARN_LIMIT command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read		IOUT_UC_WARN_AVG			IOUT_UC_WARN_LIMIT											
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 166 IOUT_UC_WARN_LIMIT command bits description

Field	Bits	Type	Reset	Description
IOUT_UC_WARN_LIMIT	0	rw	0x000 (0 dec)	UC warning can be programmed as a fraction of V_SNS_CS.
IOUT_UC_WARN_AVG	12	rw	0x0 (0 = 0 dec)	The IOUT_UC_WARN_AVG field specifies number of samples to be averaged for UC warning limit.
RESERVED	15		0x0	

Table 167 IOUT_UC_WARN averaging configuration

IOUT_UC_WARN_AVG	Value	Description
0x0 (000 bin)	0	1
0x1 (001 bin)	1	2
0x2 (010 bin)	10	4
0x3 (011 bin)	11	8
0x4 (100 bin)	100	16
0x5 (101 bin)	101	32
0x6 (110 bin)	110	64
0x7 (111 bin)	111	128

1.47 ONCHIP_TSD_FAULT_LIMIT

Address: 0xDD
Reset: 0x03
Included in OTP

The ONCHIP_TSD_FAULT_LIMIT command set the temperature of the device, in degrees Celsius, measured by the internal temperature sensor, at which the On-chip thermal shut down fault is triggered.

Table 168 ONCHIP_TSD_FAULT_LIMIT command structure

	7	6	5	4	3	2	1	0
Read							ONCHIP_TSD_FAULT_LIMIT	
Write								
Reset	0	0	0	0	0	0	1	1

Table 169 ONCHIP_TSD_FAULT_LIMIT command bits description

Field	Bits	Type	Reset	Description
ONCHIP_TSD_FAULT_LIMIT	[1:0]	rw	0x3 (11 = 3 dec)	
RESERVED	[7:2]		0x0	

Table 170 ONCHIP_TSD_FAULT_LIMIT configuration

ONCHIP_TSD_FAULT_LIMIT	Value	Description
0x0 (00 bin)	0	130°C
0x1 (01 bin)	1	135°C
0x2 (10 bin)	10	140°C
0x3 (11 bin)	11	145°C

1.48 ENABLE_FAULTS

Address: 0xDE
Reset: 0x3EFF
Included in OTP

This command enables or disabled the faults.

Table 171 ENABLE_FAULTS command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read		OT	UR	UV	OV	OVIN	OUV		WD	OC	SOAR	SOC	TSD	FET_DS	FET_GD	FET_GS
Write																
Reset	0	0	1	1	1	1	1	0	1	1	1	1	1	1	1	1

Table 172 ENABLE_FAULTS command bits description

Field	Bits	Type	Reset	Description
FET_GS	0	rw	0x1 (1 = 1 dec)	Enables or disables FET_GS fault
FET_GD	1	rw	0x1 (1 = 1 dec)	Enables or disables FET_GD fault
FET_DS	2	rw	0x1 (1 = 1 dec)	Enables or disables FET_DS fault

(table continues...)

Table 172 (continued) ENABLE_FAULTS command bits description

Field	Bits	Type	Reset	Description
TSD	3	rw	0x1 (1 = 1 dec)	Enables or disables TSD fault
SOC	4	rw	0x1 (1 = 1 dec)	Enables or disables SOC fault
SOAR	5	rw	0x1 (1 = 1 dec)	Enables or disables SOAR fault
OC	6	rw	0x1 (1 = 1 dec)	Enables or disables OC fault
WD	7	rw	0x1 (1 = 1 dec)	Enables or disables WD fault
RESERVED	8		0x0	
OUV	9	rw	0x1 (1 = 1 dec)	Enables or disables OUV fault
OVIN	10	rw	0x1 (1 = 1 dec)	Enables or disables OVIN fault
OV	11	rw	0x1 (1 = 1 dec)	Enables or disables OV fault
UV	12	rw	0x1 (1 = 1 dec)	Enables or disables UV fault
UR	13	rw	0x1 (1 = 1 dec)	Enables or disables UR fault
OT	14	rw	0x0 (0 = 0 dec)	Enables or disables OT fault
RESERVED	15		0x0	

Table 173 FET_GS configuration

FET_GS	Value	Description
0x0	0	Fault is disabled.
0x1	1	Fault is enabled

Table 174 FET_GD configuration

FET_GD	Value	Description
0x0	0	Fault is disabled.
0x1	1	Fault is enabled

Table 175 FET_DS configuration

FET_DS	Value	Description
0x0	0	Fault is disabled.
0x1	1	Fault is enabled

Table 176 TSD configuration

TSD	Value	Description
0x0	0	Fault is disabled.

(table continues...)

Table 176 (continued) TSD configuration

TSD	Value	Description
0x1	1	Fault is enabled

Table 177 SOC configuration

SOC	Value	Description
0x0	0	Fault is disabled.
0x1	1	Fault is enabled

Table 178 SOAR configuration

SOAR	Value	Description
0x0	0	Fault is disabled.
0x1	1	Fault is enabled

Table 179 OC configuration

OC	Value	Description
0x0	0	Fault is disabled.
0x1	1	Fault is enabled

Table 180 WD configuration

WD	Value	Description
0x0	0	Fault is disabled.
0x1	1	Fault is enabled

Table 181 OUV configuration

OUV	Value	Description
0x0	0	Fault is disabled.
0x1	1	Fault is enabled

Table 182 OVIN configuration

OVIN	Value	Description
0x0	0	Fault is disabled.
0x1	1	Fault is enabled

(table continues...)

Table 182 (continued) OVIN configuration

OVIN	Value	Description

Table 183 OV configuration

OV	Value	Description
0x0	0	Fault is disabled.
0x1	1	Fault is enabled

Table 184 UV configuration

UV	Value	Description
0x0	0	Fault is disabled.
0x1	1	Fault is enabled

Table 185 UR configuration

UR	Value	Description
0x0	0	Fault is disabled.
0x1	1	Fault is enabled

Table 186 OT configuration

OT	Value	Description
0x0	0	Fault is disabled.
0x1	1	Fault is enabled

1.49 MASK_FAULTS

Address: 0xDF
Reset: 0x3EFF
Included in OTP

This command determines which faults are reflected in the FAULT pin.

Table 187 MASK_FAULTS command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read		OT	UR	UV	OV	OVIN	OUV		WD	OC	SOAR	SOC	TSD	FET_DS	FET_GD	FET_GS
Write																

(table continues...)

Table 187 (continued) MASK_FAULTS command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0	0	1	1	1	1	1	0	1	1	1	1	1	1	1	1

Table 188 MASK_FAULTS command bits description

Field	Bits	Type	Reset	Description
FET_GS	0	rw	0x1 (1 = 1 dec)	Masks FET_GS fault
FET_GD	1	rw	0x1 (1 = 1 dec)	Masks FET_GD fault
FET_DS	2	rw	0x1 (1 = 1 dec)	Masks FET_DS fault
TSD	3	rw	0x1 (1 = 1 dec)	Masks TSD fault
SOC	4	rw	0x1 (1 = 1 dec)	Masks SOC fault
SOAR	5	rw	0x1 (1 = 1 dec)	Masks SOAR fault
OC	6	rw	0x1 (1 = 1 dec)	Masks OC fault
WD	7	rw	0x1 (1 = 1 dec)	Masks WD fault
RESERVED	8		0x0	
OUV	9	rw	0x1 (1 = 1 dec)	Masks OUV fault
OVIN	10	rw	0x1 (1 = 1 dec)	Masks OVIN fault
OV	11	rw	0x1 (1 = 1 dec)	Masks OV fault
UV	12	rw	0x1 (1 = 1 dec)	Masks UV fault
UR	13	rw	0x1 (1 = 1 dec)	Masks UR fault
OT	14	rw	0x0 (0 = 0 dec)	Masks OT fault
RESERVED	15		0x0	

Table 189 FET_GS mask configuration

FET_GS	Value	Description
0x0	0	Fault is not reflected in the FAULT pin.
0x1	1	Fault is reflected in the FAULT pin.

Table 190 FET_GD mask configuration

FET_GD	Value	Description
0x0	0	Fault is not reflected in the FAULT pin.
0x1	1	Fault is reflected in the FAULT pin.

Table 191 FET_DS mask configuration

FET_DS	Value	Description
0x0	0	Fault is not reflected in the FAULT pin.
0x1	1	Fault is reflected in the FAULT pin.

Table 192 TSD mask configuration

TSD	Value	Description
0x0	0	Fault is not reflected in the FAULT pin.
0x1	1	Fault is reflected in the FAULT pin.

Table 193 SOC mask configuration

SOC	Value	Description
0x0	0	Fault is not reflected in the FAULT pin.
0x1	1	Fault is reflected in the FAULT pin.

Table 194 SOAR mask configuration

SOAR	Value	Description
0x0	0	Fault is not reflected in the FAULT pin.
0x1	1	Fault is reflected in the FAULT pin.

Table 195 OC mask configuration

OC	Value	Description
0x0	0	Fault is not reflected in the FAULT pin.
0x1	1	Fault is reflected in the FAULT pin.

Table 196 WD mask configuration

WD	Value	Description
0x0	0	Fault is not reflected in the FAULT pin.
0x1	1	Fault is reflected in the FAULT pin.

Table 197 OUV mask configuration

OUV	Value	Description
0x0	0	Fault is not reflected in the FAULT pin.
0x1	1	Fault is reflected in the FAULT pin.

Table 198 OVIN mask configuration

OVIN	Value	Description
0x0	0	Fault is not reflected in the FAULT pin.
0x1	1	Fault is reflected in the FAULT pin.

Table 199 OV mask configuration

OV	Value	Description
0x0	0	Fault is not reflected in the FAULT pin.
0x1	1	Fault is reflected in the FAULT pin.

Table 200 UV mask configuration

UV	Value	Description
0x0	0	Fault is not reflected in the FAULT pin.
0x1	1	Fault is reflected in the FAULT pin.

Table 201 UR mask configuration

UR	Value	Description
0x0	0	Fault is not reflected in the FAULT pin.
0x1	1	Fault is reflected in the FAULT pin.

Table 202 OT mask configuration

OT	Value	Description
0x0	0	Fault is not reflected in the FAULT pin.

(table continues...)

Table 202 (continued) OT mask configuration

OT	Value	Description
0x1	1	Fault is reflected in the FAULT pin.

1.50 STATUS_FAULTS

Address: 0xE0
Reset: 0x0000

This command summarizes the faults status.

Table 203 STATUS_FAULTS command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read		OT	UR	UV	OV	OVIN	OUV		WD	OC	SOAR	SOC	TSD	FET_DS	FET_GD	FET_GS
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 204 STATUS_FAULTS command bits description

Field	Bits	Type	Reset	Description
FET_GS	0	rw	0x0 (0 = 0 dec)	Specifies the status of FET_GS fault
FET_GD	1	rw	0x0 (0 = 0 dec)	Specifies the status of FET_GD fault
FET_DS	2	rw	0x0 (0 = 0 dec)	Specifies the status of FET_DS fault
TSD	3	rw	0x0 (0 = 0 dec)	Specifies the status of TSD fault
SOC	4	rw	0x0 (0 = 0 dec)	Specifies the status of SOC fault
SOAR	5	rw	0x0 (0 = 0 dec)	Specifies the status of SOAR fault
OC	6	rw	0x0 (0 = 0 dec)	Specifies the status of OC fault
WD	7	rw	0x0 (0 = 0 dec)	Specifies the status of WD fault
RESERVED	8		0x0	
OUV	9	rw	0x0 (0 = 0 dec)	Specifies the status of OUV fault
OVIN	10	rw	0x0 (0 = 0 dec)	Specifies the status of OVIN fault
OV	11	rw	0x0 (0 = 0 dec)	Specifies the status of OV fault
UV	12	rw	0x0 (0 = 0 dec)	Specifies the status of UV fault
UR	13	rw	0x0 (0 = 0 dec)	Specifies the status of UR fault
OT	14	rw	0x0 (0 = 0 dec)	Specifies the status of OT fault
RESERVED	15		0x0	

Table 205 FET_GS status

FET_GS	Value	Description
0x0	0	Fault is not present.
0x1	1	Fault is present.

Table 206 FET_GD status

FET_GD	Value	Description
0x0	0	Fault is not present.
0x1	1	Fault is present.

Table 207 FET_DS status

FET_DS	Value	Description
0x0	0	Fault is not present.
0x1	1	Fault is present.

Table 208 TSD status

TSD	Value	Description
0x0	0	Fault is not present.
0x1	1	Fault is present.

Table 209 SOC status

SOC	Value	Description
0x0	0	Fault is not present.
0x1	1	Fault is present.

Table 210 SOAR status

SOAR	Value	Description
0x0	0	Fault is not present.
0x1	1	Fault is present.

Table 211 OC status

OC	Value	Description
0x0	0	Fault is not present.

(table continues...)

Table 211 (continued) OC status

OC	Value	Description
0x1	1	Fault is present.

Table 212 WD status

WD	Value	Description
0x0	0	Fault is not present.
0x1	1	Fault is present.

Table 213 OUV status

OUV	Value	Description
0x0	0	Fault is not present.
0x1	1	Fault is present.

Table 214 OVIN status

OVIN	Value	Description
0x0	0	Fault is not present.
0x1	1	Fault is present.

Table 215 OV status

OV	Value	Description
0x0	0	Fault is not present.
0x1	1	Fault is present.

Table 216 UV status

UV	Value	Description
0x0	0	Fault is not present.
0x1	1	Fault is present.

Table 217 UR status

UR	Value	Description
0x0	0	Fault is not present.
0x1	1	Fault is present.

(table continues...)

Table 217 (continued) UR status

UR	Value	Description

Table 218 OT status

OT	Value	Description
0x0	0	Fault is not present.
0x1	1	Fault is present.

1.51 ENABLE_WARNS

Address: 0xE1
Reset: 0x0000
Included in OTP

This command enables or disables the warnings.

Table 219 ENABLE_WARNS command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read				COMM	OP	UV	OV	OUV	OOV	OOC	OUC	SOAR	OT	TSD	FET_GS	INEG
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 220 ENABLE_WARNS command bits description

Field	Bits	Type	Reset	Description
INEG	0	rw	0x0 (0 = 0 dec)	Enables or disables INEG warning
FET_GS	1	rw	0x0 (0 = 0 dec)	Enables or disables FET_GS warning
TSD	2	rw	0x0 (0 = 0 dec)	Enables or disables TSD warning
OT	3	rw	0x0 (0 = 0 dec)	Enables or disables OT warning
SOAR	4	rw	0x0 (0 = 0 dec)	Enables or disables SOAR warning
OUC	5	rw	0x0 (0 = 0 dec)	Enables or disables OUC warning
OOC	6	rw	0x0 (0 = 0 dec)	Enables or disables OOC warning
OOV	7	rw	0x0 (0 = 0 dec)	Enables or disables OOV warning
OUV	8	rw	0x0 (0 = 0 dec)	Enables or disables OUV warning
OV	9	rw	0x0 (0 = 0 dec)	Enables or disables OV warning
UV	10	rw	0x0 (0 = 0 dec)	Enables or disables UV warning
OP	11	rw	0x0 (0 = 0 dec)	Enables or disables OP warning
COMM	12	rw	0x0 (0 = 0 dec)	Enables or disables COMM warning
RESERVED	[15:13]		0x0	

(table continues...)

Table 220 (continued) ENABLE_WARNS command bits description

Field	Bits	Type	Reset	Description

Table 221 INEG configuration

INEG	Value	Description
0x0	0	Warning is disabled.
0x1	1	Warning is enabled.

Table 222 FET_GS configuration

FET_GS	Value	Description
0x0	0	Warning is disabled.
0x1	1	Warning is enabled.

Table 223 TSD configuration

TSD	Value	Description
0x0	0	Warning is disabled.
0x1	1	Warning is enabled.

Table 224 OT configuration

OT	Value	Description
0x0	0	Warning is disabled.
0x1	1	Warning is enabled.

Table 225 SOAR configuration

SOAR	Value	Description
0x0	0	Warning is disabled.
0x1	1	Warning is enabled.

Table 226 OUC configuration

OUC	Value	Description
0x0	0	Warning is disabled.
0x1	1	Warning is enabled.

Table 227 OOC configuration

OOC	Value	Description
0x0	0	Warning is disabled.
0x1	1	Warning is enabled.

Table 228 OOV configuration

OOV	Value	Description
0x0	0	Warning is disabled.
0x1	1	Warning is enabled.

Table 229 OUV configuration

OUV	Value	Description
0x0	0	Warning is disabled.
0x1	1	Warning is enabled.

Table 230 OV configuration

OV	Value	Description
0x0	0	Warning is disabled.
0x1	1	Warning is enabled.

Table 231 UV configuration

UV	Value	Description
0x0	0	Warning is disabled.
0x1	1	Warning is enabled.

Table 232 OP configuration

OP	Value	Description
0x0	0	Warning is disabled.
0x1	1	Warning is enabled.

Table 233 COMM configuration

COMM	Value	Description
0x0	0	Warning is disabled.

(table continues...)

Table 233 (continued) COMM configuration

COMM	Value	Description
0x1	1	Warning is enabled.

1.52 MASK_WARNS

Address: 0xE2
Reset: 0x0000
Included in OTP

This command determines which warnings are reflected in the WARN pin.

Table 234 MASK_WARNS command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read				COMM	OP	UV	OV	OUV	OOV	OOC	OUC	SOAR	OT	TSD	FET_GS	INEG
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 235 MASK_WARNS command bits description

Field	Bits	Type	Reset	Description
INEG	0	rw	0x0 (0 = 0 dec)	Masks INEG warning
FET_GS	1	rw	0x0 (0 = 0 dec)	Masks FET_GS warning
TSD	2	rw	0x0 (0 = 0 dec)	Masks TSD warning
OT	3	rw	0x0 (0 = 0 dec)	Masks OT warning
SOAR	4	rw	0x0 (0 = 0 dec)	Masks SOAR warning
OUC	5	rw	0x0 (0 = 0 dec)	Masks OUC warning
OOC	6	rw	0x0 (0 = 0 dec)	Masks OOC warning
OOV	7	rw	0x0 (0 = 0 dec)	Masks OOV warning
OUV	8	rw	0x0 (0 = 0 dec)	Masks OUV warning
OV	9	rw	0x0 (0 = 0 dec)	Masks OV warning
UV	10	rw	0x0 (0 = 0 dec)	Masks UV warning
OP	11	rw	0x0 (0 = 0 dec)	Masks OP warning
COMM	12	rw	0x0 (0 = 0 dec)	Masks COMM warning
RESERVED	[15:13]		0x0	

Table 236 INEG mask configuration

INEG	Value	Description
0x0	0	Warning is not reflected in the WARN pin.
0x1	1	Warning is reflected in the WARN pin.

Table 237 FET_GS mask configuration

FET_GS	Value	Description
0x0	0	Warning is not reflected in the WARN pin.
0x1	1	Warning is reflected in the WARN pin.

Table 238 TSD mask configuration

TSD	Value	Description
0x0	0	Warning is not reflected in the WARN pin.
0x1	1	Warning is reflected in the WARN pin.

Table 239 OT mask configuration

OT	Value	Description
0x0	0	Warning is not reflected in the WARN pin.
0x1	1	Warning is reflected in the WARN pin.

Table 240 SOAR mask configuration

SOAR	Value	Description
0x0	0	Warning is not reflected in the WARN pin.
0x1	1	Warning is reflected in the WARN pin.

Table 241 OUC mask configuration

OUC	Value	Description
0x0	0	Warning is not reflected in the WARN pin.
0x1	1	Warning is reflected in the WARN pin.

Table 242 OOC mask configuration

OOC	Value	Description
0x0	0	Warning is not reflected in the WARN pin.
0x1	1	Warning is reflected in the WARN pin.

Table 243 OOV mask configuration

OOV	Value	Description
0x0	0	Warning is not reflected in the WARN pin.
0x1	1	Warning is reflected in the WARN pin.

Table 244 OUV mask configuration

OUV	Value	Description
0x0	0	Warning is not reflected in the WARN pin.
0x1	1	Warning is reflected in the WARN pin.

Table 245 OV mask configuration

OV	Value	Description
0x0	0	Warning is not reflected in the WARN pin.
0x1	1	Warning is reflected in the WARN pin.

Table 246 UV mask configuration

UV	Value	Description
0x0	0	Warning is not reflected in the WARN pin.
0x1	1	Warning is reflected in the WARN pin.

Table 247 OP mask configuration

OP	Value	Description
0x0	0	Warning is not reflected in the WARN pin.
0x1	1	Warning is reflected in the WARN pin.

Table 248 COMM mask configuration

COMM	Value	Description
0x0	0	Warning is not reflected in the WARN pin.
0x1	1	Warning is reflected in the WARN pin.

1.53 STATUS_WARNS

Address: 0xE3
Reset: 0x0000

This command summarizes the warnings status.

Table 249 STATUS_WARNS command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read				COMM	OP	UV	OV	OUV	OOV	OOC	OUC	SOAR	OT	TSD	FET_GS	INEG
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 250 STATUS_WARNS command bits description

Field	Bits	Type	Reset	Description
INEG	0	rw	0x0 (0 = 0 dec)	Specifies the status of INEG warning
FET_GS	1	rw	0x0 (0 = 0 dec)	Specifies the status of FET_GS warning
TSD	2	rw	0x0 (0 = 0 dec)	Specifies the status of TSD warning

(table continues...)

Table 250 (continued) STATUS_WARNS command bits description

Field	Bits	Type	Reset	Description
OT	3	rw	0x0 (0 = 0 dec)	Specifies the status of OT warning
SOAR	4	rw	0x0 (0 = 0 dec)	Specifies the status of SOAR warning
OUC	5	rw	0x0 (0 = 0 dec)	Specifies the status of OUC warning
OOC	6	rw	0x0 (0 = 0 dec)	Specifies the status of OOC warning
OOV	7	rw	0x0 (0 = 0 dec)	Specifies the status of OOV warning
OUV	8	rw	0x0 (0 = 0 dec)	Specifies the status of OUV warning
OV	9	rw	0x0 (0 = 0 dec)	Specifies the status of OV warning
UV	10	rw	0x0 (0 = 0 dec)	Specifies the status of UV warning
OP	11	rw	0x0 (0 = 0 dec)	Specifies the status of OP warning
COMM	12	rw	0x0 (0 = 0 dec)	Specifies the status of COMM warning
RESERVED	[15:13]		0x0	

Table 251 INEG status

INEG	Value	Description
0x0	0	Warning is not present.
0x1	1	Warning is present.

Table 252 FET_GS status

FET_GS	Value	Description
0x0	0	Warning is not present.
0x1	1	Warning is present.

Table 253 TSD status

TSD	Value	Description
0x0	0	Warning is not present.
0x1	1	Warning is present.

Table 254 OT status

OT	Value	Description
0x0	0	Warning is not present.
0x1	1	Warning is present.

Table 255 SOAR status

SOAR	Value	Description
0x0	0	Warning is not present.
0x1	1	Warning is present.

Table 256 OUC status

OUC	Value	Description
0x0	0	Warning is not present.
0x1	1	Warning is present.

Table 257 OOC status

OOC	Value	Description
0x0	0	Warning is not present.
0x1	1	Warning is present.

Table 258 OOV status

OOV	Value	Description
0x0	0	Warning is not present.
0x1	1	Warning is present.

Table 259 OUV status

OUV	Value	Description
0x0	0	Warning is not present.
0x1	1	Warning is present.

Table 260 OV status

OV	Value	Description
0x0	0	Warning is not present.
0x1	1	Warning is present.

Table 261 UV status

UV	Value	Description
0x0	0	Warning is not present.

(table continues...)

Table 261 (continued) UV status

UV	Value	Description
0x1	1	Warning is present.

Table 262 OP status

OP	Value	Description
0x0	0	Warning is not present.
0x1	1	Warning is present.

Table 263 COMM status

COMM	Value	Description
0x0	0	Warning is not present.
0x1	1	Warning is present.

1.54 PWRGD_DG_TMR

Address: 0xE4
Reset: 0xF0
Included in OTP

The PWRGD_DG_TMR command sets the deglitch time after PWRGD signal assertion (bits [7:4]) and deassertion (bits [3:0]).

Table 264 PWRGD_DG_TMR command structure

	7	6	5	4	3	2	1	0
Read	PWRGD_DG_TMR				PWRGDN_DG_TMR			
Reset	1	1	1	1	0	0	0	0

Table 265 PWRGD_DG_TMR command bits description

Field	Bits	Type	Reset	Description
PWRGDN_DG_TMR	[3:0]	rw	0x0 (0 dec)	Programmable from 0 to 15ms in 1ms steps. 1 LSB = 1ms.
PWRGD_DG_TMR	[7:4]	rw	0xF (15 dec)	Programmable from 0 to 15ms in 1ms steps. 1 LSB = 1ms.

1.55 SOA_TMR

Address: 0xE5
Reset: 0x001F
Included in OTP

FET SOA protection timers.

Table 266 SOA_TMR command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read					RMS_SAMPLE_TMR		SOC_DG_TMR		SOC_TMR			SOAR_TMR			SOAD_TMR	
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1

Table 267 SOA_TMR command bits description

Field	Bits	Type	Reset	Description
SOAD_TMR	[1:0]	rw	0x3 (11 = 3 dec)	SOAD_TMR sets the deglitch time after OC or SOA violation conditions have been detected and before SOA regulation phase starts.
SOAR_TMR	[4:2]	rw	0x7 (111 = 7 dec)	SOAR_TMR specifies the operating time in OC or SOA regulation condition before fault is triggered.
SOC_TMR	[7:5]	rw	0x0 (0 = 0 dec)	SOC_TMR specifies the time the device operates in SOC condition before fault is triggered.
SOC_DG_TMR	[9:8]	rw	0x0 (0 = 0 dec)	SOC_DG_TMR specifies the deglitch time of the analog comparator that detects the SOC condition.
RMS_SAMPLE_TMR	[11:10]	rw	0x0 (0 = 0 dec)	RMS_SAMPLE_TMR specifies the number of samples taken for the RMS current protection calculation. In other words, the integration time.
RESERVED	[15:12]		0x0	

Table 268 SOAD_TMR configuration

SOAD_TMR	Value	Description
0x0 (00 bin)	0	0ms
0x1 (01 bin)	1	0.1ms
0x2 (10 bin)	10	1ms
0x3 (11 bin)	11	10ms

Table 269 SOAR_TMR configuration

SOAR_TMR	Value	Description
0x0 (000 bin)	0	0 ms

(table continues...)

Table 269 (continued) SOAR_TMR configuration

SOAR_TMR	Value	Description
0x1 (001 bin)	1	1 ms
0x2 (010 bin)	10	5 ms
0x3 (011 bin)	11	10 ms
0x4 (100 bin)	100	50 ms
0x5 (101 bin)	101	100 ms
0x6 (110 bin)	110	500 ms
0x7 (111 bin)	111	1000 ms

Table 270 SOC_TMR configuration

SOC_TMR	Value	Description
0x0 (000 bin)	0	0 ms
0x1 (001 bin)	1	0.01 ms
0x2 (010 bin)	10	0.1 ms
0x3 (011 bin)	11	1 ms
0x4 (100 bin)	100	10 ms
0x5 (101 bin)	101	100 ms
0x6 (110 bin)	110	500 ms
0x7 (111 bin)	111	1000 ms

Table 271 SOC_DG_TMR configuration

SOC_DG_TMR	Value	Description
0x0 (00 bin)	0	0 ns
0x1 (01 bin)	1	200 ns
0x2 (10 bin)	10	500 ns
0x3 (11 bin)	11	1000 ns

Table 272 RMS_SAMPLE_TMR configuration

RMS_SAMPLE_TMR	Value	Description
0x0 (00 bin)	0	1.64ms
0x1 (01 bin)	1	13.11ms
0x2 (10 bin)	10	104.86ms
0x3 (11 bin)	11	838.86ms

1.56 TURN_OFF_CTRL

Address: 0xE6
Reset: 0x0000
Included in OTP

2-step turn-off settings.

Table 273 TURN_OFF_CTRL command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read						GATE_PD_TMR								GATE_SLOW_PD		GATE_FAST_PD
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 274 TURN_OFF_CTRL command bits description

Field	Bits	Type	Reset	Description
GATE_FAST_PD	0	rw	0x0 (0 = 0 dec)	**GATE_FAST_PD sets the current level for the first phase of the 2-step turn-off.** • If GATE_FAST_PD = 0: GATE_SLOW_PD and GATE_PD_TMR are ignored. Gate discharges with a single continuous phase of 1.5A • If GATE_FAST_PD = 1: - When GATE_PD_TMR = 0: GATE_FAST_PD is ignored. Gate discharges with a single continuous phase of GATE_SLOW_PD. - When GATE_PD_TMR different than 0: Gate discharges with two step turn-off
GATE_SLOW_PD	[2:1]	rw	0x0 (0 = 0 dec)	Sets the current level of the regular turn-off and the second phase of the 2-step turn-off.
GATE_PD_TMR	[10:3]	rw	0x00 (0 dec)	GATE_PD_TMR sets the time of the first phase of the two step controlled turn-off. Allowed values for this timer are: - 0 ns. - From 250 ns to 6375 ns in 25 ns steps. When timer is set to 0 ns, gate discharges slowly with GATE_SLOW_PD.
RESERVED	[15:11]		0x00	

Table 275 Gate fast pull down configuration

GATE_FAST_PD	Value	Description
0x0	0	1.5A
0x1	1	200Ω

Table 276 Gate slow pull down configuration

GATE_SLOW_PD	Value	Description
0x0 (00 bin)	0	250uA
0x1 (01 bin)	1	500uA
0x2 (10 bin)	10	750uA
0x3 (11 bin)	11	1250uA

1.57 RETRY

Address: 0xE7
Reset: 0x3FBF
Included in OTP

Retry settings.

Table 277 RETRY command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read		GATE_REC_EN	MASK_WD	MASK_OUV	MASK_OC	MASK_SOC	MASK_SOAR	RETRY_COUNTER			RETD_TMR			COOLD_TMR		
Write																
Reset	0	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1

Table 278 RETRY command bits description

Field	Bits	Type	Reset	Description
COOLD_TMR	[2:0]	rw	0x7 (111 = 7 dec)	The COOLD_TMR bits set the cool down period, in seconds, between power-up retries.
RETD_TMR	[5:3]	rw	0x7 (111 = 7 dec)	The RETD_TMR bits set the retry ok deglitch timer in seconds, which controls the time, after PWRGD signal is achieved in a retry attempt, after which the retry counter is reset.

(table continues...)

Table 278 (continued) RETRY command bits description

Field	Bits	Type	Reset	Description
RETRY_COUNTER	[8:6]	rw	0x6 (110 = 6 dec)	The RETRY_COUNTER bits set the number of times the system will retry power-up after a retry configured fault has occurred.
MASK_SOAR	9	rw	0x1 (1 = 1 dec)	MASK_SOAR bit defines if the system is to retry power-up after a SOAR fault.
MASK_SOC	10	rw	0x1 (1 = 1 dec)	MASK_SOC bit defines if the system is to retry power-up after an SOC fault.
MASK_OC	11	rw	0x1 (1 = 1 dec)	MASK_OC bit defines if the system is to retry power-up after an OC fault.
MASK_OUV	12	rw	0x1 (1 = 1 dec)	MASK_OUV bit defines if the system is to retry power-up after an OUV fault.
MASK_WD	13	rw	0x1 (1 = 1 dec)	MASK_WDG bis defines if the system is to retry power-up after a watchdog fault.
GATE_REC_EN	14	rw	0x0 (0 = 0 dec)	GATE_REC_EN bit enables the gate fast recovery feature.
RESERVED	15		0x0	

Table 279 Cool down period timer configuration

COOLD_TMR	Value	Description
0x0 (000 bin)	0	0 s
0x1 (001 bin)	1	1 s
0x2 (010 bin)	10	2 s
0x3 (011 bin)	11	4 s
0x4 (100 bin)	100	8 s
0x5 (101 bin)	101	16 s
0x6 (110 bin)	110	32 s
0x7 (111 bin)	111	64 s

Table 280 Retry deglitch timer configuration

RETD_TMR	Value	Description
0x0 (000 bin)	0	0 s
0x1 (001 bin)	1	0.5 s
0x2 (010 bin)	10	1 s
0x3 (011 bin)	11	2 s
0x4 (100 bin)	100	3 s

(table continues...)

Table 280 (continued) Retry deglitch timer configuration

RETD_TMR	Value	Description
0x5 (101 bin)	101	4 s
0x6 (110 bin)	110	6 s
0x7 (111 bin)	111	8 s

Table 281 Retry counter configuration

RETRY_COUNTER	Value	Description
0x0 (000 bin)	0	0 (latch-off after the first retry fault)
0x1 (001 bin)	1	1
0x2 (010 bin)	10	2
0x3 (011 bin)	11	4
0x4 (100 bin)	100	8
0x5 (101 bin)	101	16
0x6 (110 bin)	110	32
0x7 (111 bin)	111	Infinite

Table 282 SOAR fault mask configuration

MASK_SOAR	Value	Description
0x0	0	Retry after SOAR fault disabled
0x1	1	Retry after SOAR fault enabled

Table 283 SOC fault mask configuration

MASK_SOC	Value	Description
0x0	0	Retry after SOC fault disabled
0x1	1	Retry after SOC fault enabled

Table 284 OC fault mask configuration

MASK_OC	Value	Description
0x0	0	Retry after OC fault disabled
0x1	1	Retry after OC fault enabled

Table 285 OUV fault mask configuration

MASK_OUV	Value	Description
0x0	0	Retry after OUV fault disabled
0x1	1	Retry after OUV fault enabled

Table 286 Watchdog fault mask configuration

MASK_WD	Value	Description
0x0	0	Retry after Watchdog fault disabled
0x1	1	Retry after Watchdog fault enabled

Table 287 Fast recovery configuration

GATE_REC_EN	Value	Description
0x0	0	Gate Fast Recovery disabled
0x1	1	Gate Fast Recovery enabled

1.58 TELEMETRY_EN

Address: 0xE8
Reset: 0x7600
Included in OTP

The TELEMETRY_EN command enables or disables each one of the telemetry features.

Table 288 TELEMETRY_EN command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	READ_EIN_EN	READ_VIN_EN	READ_VOUT_EN	READ_IOUT_EN	READ_TEMP_1_EN	READ_TEMP_2_EN	READ_PIN_EN	READ_VIN_PEAK_EN	READ_VOUT_PEAK_EN	READ_IOUT_PEAK_EN	READ_PIN_PEAK_EN	READ_TEMP_1_PEAK_EN	READ_VIN_VALLEY_EN	READ_VOUT_VALLEY_EN	READ_IOUT_VALLEY_EN	READ_TEMP_1_VALLEY_EN
Reset	0	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0

Table 289 TELEMETRY_EN command bits description

Field	Bits	Type	Reset	Description
READ_TEMP_1_VALLEY_EN	0	rw	0x0 (0 = 0 dec)	Enable/disable external temperature valley reading

(table continues...)

Table 289 (continued) TELEMETRY_EN command bits description

Field	Bits	Type	Reset	Description
READ_IOUT_VALLEY_EN	1	rw	0x0 (0 = 0 dec)	Enable/disable output current valley reading
READ_VOUT_VALLEY_EN	2	rw	0x0 (0 = 0 dec)	Enable/disable output voltage valley reading
READ_VIN_VALLEY_EN	3	rw	0x0 (0 = 0 dec)	Enable/disable input voltage valley reading
READ_TEMP_1_PEAK_EN	4	rw	0x0 (0 = 0 dec)	Enable/disable external temperature peak reading
READ_PIN_PEAK_EN	5	rw	0x0 (0 = 0 dec)	Enable/disable input power peak reading
READ_IOUT_PEAK_EN	6	rw	0x0 (0 = 0 dec)	Enable/disable output current peak reading
READ_VOUT_PEAK_EN	7	rw	0x0 (0 = 0 dec)	Enable/disable output voltage peak reading
READ_VIN_PEAK_EN	8	rw	0x0 (0 = 0 dec)	Enable/disable input voltage peak reading
READ_PIN_EN	9	rw	0x1 (1 = 1 dec)	Enable/disable input power calculation
READ_TEMP_2_EN	10	rw	0x1 (1 = 1 dec)	Enable/disable internal temperature reading
READ_TEMP_1_EN	11	rw	0x0 (0 = 0 dec)	Enable/disable external temperature reading
READ_IOUT_EN	12	rw	0x1 (1 = 1 dec)	Enable/disable output current reading
READ_VOUT_EN	13	rw	0x1 (1 = 1 dec)	Enable/disable output voltage reading
READ_VIN_EN	14	rw	0x1 (1 = 1 dec)	Enable/disable input voltage reading
READ_EIN_EN	15	rw	0x0 (0 = 0 dec)	Enable/disable energy calculation

Table 290 READ_TEMP_1_VALLEY_EN configuration

READ_TEMP_1_VALLEY_EN	Value	Description
0x0	0	Feature disabled
0x1	1	Feature enabled

Table 291 READ_IOUT_VALLEY_EN configuration

READ_IOUT_VALLEY_EN	Value	Description
0x0	0	Feature disabled
0x1	1	Feature enabled

Table 292 READ_VOUT_VALLEY_EN configuration

READ_VOUT_VALLEY_EN	Value	Description
0x0	0	Feature disabled
0x1	1	Feature enabled

Table 293 READ_VIN_VALLEY_EN configuration

READ_VIN_VALLEY_EN	Value	Description
0x0	0	Feature disabled
0x1	1	Feature enabled

Table 294 READ_TEMP_1_PEAK_EN configuration

READ_TEMP_1_PEAK_EN	Value	Description
0x0	0	Feature disabled
0x1	1	Feature enabled

Table 295 READ_PIN_PEAK_EN configuration

READ_PIN_PEAK_EN	Value	Description
0x0	0	Feature disabled
0x1	1	Feature enabled

Table 296 READ_IOUT_PEAK_EN configuration

READ_IOUT_PEAK_EN	Value	Description
0x0	0	Feature disabled
0x1	1	Feature enabled

Table 297 READ_VOUT_PEAK_EN configuration

READ_VOUT_PEAK_EN	Value	Description
0x0	0	Feature disabled
0x1	1	Feature enabled

Table 298 READ_VIN_PEAK_EN configuration

READ_VIN_PEAK_EN	Value	Description
0x0	0	Feature disabled
0x1	1	Feature enabled

Table 299 READ_PIN_EN configuration

READ_PIN_EN	Value	Description
0x0	0	Feature disabled
0x1	1	Feature enabled

Table 300 READ_TEMP_2_EN configuration

READ_TEMP_2_EN	Value	Description
0x0	0	Feature disabled
0x1	1	Feature enabled

Table 301 READ_TEMP_1_EN configuration

READ_TEMP_1_EN	Value	Description
0x0	0	Feature disabled
0x1	1	Feature enabled

Table 302 READ_IOUT_EN configuration

READ_IOUT_EN	Value	Description
0x0	0	Feature disabled
0x1	1	Feature enabled

Table 303 READ_VOUT_EN configuration

READ_VOUT_EN	Value	Description
0x0	0	Feature disabled
0x1	1	Feature enabled

Table 304 READ_VIN_EN configuration

READ_VIN_EN	Value	Description
0x0	0	Feature disabled

(table continues...)

Table 304 (continued) READ_VIN_EN configuration

READ_VIN_EN	Value	Description
0x1	1	Feature enabled

Table 305 READ_EIN_EN configuration

READ_EIN_EN	Value	Description
0x0	0	Feature disabled
0x1	1	Feature enabled

1.59 TELEMETRY_AVG

Address: 0xE9
Reset: 0x0000
Included in OTP

This command sets the number of averaging samples for reporting power (P_TELEMETRY_AVG), voltage (V_TELEMETRY_AVG) and current (I_TELEMETRY_AVG) telemetry.

Table 306 TELEMETRY_AVG command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read								P_TELEMETRY_AVG			V_TELEMETRY_AVG			I_TELEMETRY_AVG		
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 307 TELEMETRY_AVG command bits description

Field	Bits	Type	Reset	Description
I_TELEMETRY_AVG	[2:0]	rw	0x0 (0 = 0 dec)	Current telemetry averaging.
V_TELEMETRY_AVG	[5:3]	rw	0x0 (0 = 0 dec)	Voltage telemetry averaging.
P_TELEMETRY_AVG	[8:6]	rw	0x0 (0 = 0 dec)	Power telemetry averaging.
RESERVED	[15:9]		0x0	

Table 308 Current telemetry averaging configuration

I_TELEMETRY_AVG	Value	Description
0x0 (000 bin)	0	1
0x1 (001 bin)	1	2

(table continues...)

Table 308 (continued) Current telemetry averaging configuration

I_TELEMETRY_AVG	Value	Description
0x2 (010 bin)	10	4
0x3 (011 bin)	11	8
0x4 (100 bin)	100	16
0x5 (101 bin)	101	32
0x6 (110 bin)	110	64
0x7 (111 bin)	111	128

Table 309 Voltage telemetry averaging configuration

V_TELEMETRY_AVG	Value	Description
0x0 (000 bin)	0	1
0x1 (001 bin)	1	2
0x2 (010 bin)	10	4
0x3 (011 bin)	11	8
0x4 (100 bin)	100	16
0x5 (101 bin)	101	32
0x6 (110 bin)	110	64
0x7 (111 bin)	111	128

Table 310 Power telemetry averaging configuration

P_TELEMETRY_AVG	Value	Description
0x0 (000 bin)	0	1
0x1 (001 bin)	1	2
0x2 (010 bin)	10	4
0x3 (011 bin)	11	8
0x4 (100 bin)	100	16
0x5 (101 bin)	101	32
0x6 (110 bin)	110	64
0x7 (111 bin)	111	128

1.60 WRITE_OTP

Address: 0xEA
Reset: 0x00

Write OTP configuration command.

Table 311 WRITE_OTP command structure

	7	6	5	4	3	2	1	0
Read						SEL_SEC		
Write								WRITE_OTP
Reset	0	0	0	0	0	0	0	0

Table 312 WRITE_OTP command bits description

Field	Bits	Type	Reset	Description
WRITE_OTP	0	w	0x0 (DISABLE = 0 dec)	The WRITE_OTP bit, when set, writes the information into the selected section.
SEL_SEC	[2:1]	rw	0x0 (USER = 0 dec)	OTP is divided in three sections: User OTP, MTP, SOA. The SEL_SEC bits select the section to be written.
RESERVED	[7:3]		0x0	

Table 313 WRITE_OTP

WRITE_OTP	Value	Description
0x0	DISABLE	NO writing to OTP
0x1	ENABLE	Write OTP

Table 314 Section selection

SEL_SEC	Value	Description
0x0 (00 bin)	USER	User Programing OTP
0x1 (01 bin)	SOA	SOA Programing
0x2 (10 bin)	MTP	MTP Programing
0x3 (11 bin)	RESERVED	reserved

1.61 STATUS_MEM

Address: 0xEB
Reset: 0x00

Memory status command.

Table 315 STATUS_MEM command structure

	7	6	5	4	3	2	1	0
Read	PROG_BLOCK	OTP_FAIL	MTP_FULL	MTP_USER	OTP_USER	SOA_PRG	SOA_FULL	SOA_CRC
Write								
Reset	0	0	0	0	0	0	0	0

Table 316 STATUS_MEM command bits description

Field	Bits	Type	Reset	Description
SOA_CRC	0	r	0x0 (FAIL = 0 dec)	CRC check status on the data inside the FIFO
SOA_FULL	1	r	0x0 (EMPTY = 0 dec)	Indication if the FIFO (data + crc) is full or not
SOA_PRG	2	r	0x0 (VIRGIN = 0 dec)	SOA section of the OTP if it has been programmed or virgin
OTP_USER	3	r	0x0 (VIRGIN = 0 dec)	Indication if the configuration commands in OTP have been programmed or not
MTP_USER	4	r	0x0 (NOT_USED = 0 dec)	Indication if MTP is in use or not.
MTP_FULL	5	r	0x0 (NOT_FULL = 0 dec)	Indication if all the MTP memory has been used
OTP_FAIL	6	r	0x0 (PASS = 0 dec)	Indication if the programming or the readout of the OTP has been successful or not.
PROG_BLOCK	7	r	0x0 (ENABLE = 0 dec)	Indication if programming is allowed or if it has been blocked because of voltage or temperature out of range.

Table 317 SOA_CRC status

SOA_CRC	Value	Description
0x0	FAIL	CRC hasn't been performed or didn't pass.
0x1	PASS	CRC passed.

Table 318 SOA FIFO status

SOA_FULL	Value	Description
0x0	EMPTY	SOA FIFO not full.
0x1	FULL	SOA FIFO is full and CRC has been performed.

(table continues...)

Table 318 (continued) SOA FIFO status

SOA_FULL	Value	Description

Table 319 SOA FIFO programming status

SOA_PRG	Value	Description
0x0	VIRGIN	Section is Virgin
0x1	PROGRAMMED	Section has been programmed

Table 320 OTP status

OTP_USER	Value	Description
0x0	VIRGIN	Configuration commands have not been programmed.
0x1	PROGRAMMED	Configuration commands have been programmed.

Table 321 MTP use

MTP_USER	Value	Description
0x0	NOT_USED	MTP is not in use.
0x1	USED	MTP is in use.

Table 322 MTP status

MTP_FULL	Value	Description
0x0	NOT_FULL	Not all MTP has been used
0x1	FULL	All MTP has been used

Table 323 OTP programming status

PROG_BLOCK	OTP_FAIL	Meaning
0	0	OTP programming has succeeded.
0	1	OTP programming started but failed during programming because of OTP issue. Part must be discarded.
1	0	OTP programming has been blocked because temperature or VIN out of range.

(table continues...)

Table 323 (continued) OTP programming status

PROG_BLOCK	OTP_FAIL	Meaning
1	1	OTP programming started but failed during programming because temperature or voltage going out of range during programming. Part must be discarded.

1.62 READ_PIN_EXT

Address: 0xEC
Reset: 0x000000

The READ_PIN_EXT command returns the input power of the system as a product of VIN * IOUT.

Table 324 READ_PIN_EXT command structure

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	READ_PIN_EXT																							
Write																								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 325 READ_PIN_EXT command bits description

Field	Bits	Type	Reset	Description
READ_PIN_EXT	[23:0]	r	0x000000 (0 dec)	Returns the input power calculation in PMBus direct format.

1.63 READ_IOUT_RMS

Address: 0xED
Reset: 0x0000

This command retrieves the calculated squared RMS value of the current flow over the sense resistor. In order to enable and configure RMS calculation, RMS_EN bit in REG_CFG command and READ_IOUT_EN in TELEMETRY_EN command must be enabled and number of samples for the calculation can be configured by means of the RMS_SAMPLE_TMR in SOA_TMR command.

Table 326 READ_IOUT_RMS command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	READ_IOUT_RMS															

(table continues...)

Table 326 (continued) READ_IOUT_RMS command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 327 READ_IOUT_RMS command bits description

Field	Bits	Type	Reset	Description
READ_IOUT_RMS	[15:0]	r	0x0000 (0 dec)	RMS current measurment squared

1.64 READ_VIN_PEAK

Address: 0xEF
Reset: 0x0000

READ_VIN_PEAK stores the maximum VIN value read. The command is automatically cleared when the data is read.

Table 328 READ_VIN_PEAK command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read					READ_VIN_PEAK											
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 329 READ_VIN_PEAK command bits description

Field	Bits	Type	Reset	Description
READ_VIN_PEAK	[11:0]	r	0x000 (0 dec)	Stores the maximum VIN value read.
RESERVED	[15:12]		0x0	

1.65 READ_VOUT_PEAK

Address: 0xF0
Reset: 0x0000

READ_VOUT_PEAK stores the maximum VOUT value read. The command is automatically cleared when the data is read.

Table 330 READ_VOUT_PEAK command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read					READ_VOUT_PEAK											

(table continues...)

Table 330 (continued) READ_VOUT_PEAK command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 331 READ_VOUT_PEAK command bits description

Field	Bits	Type	Reset	Description
READ_VOUT_PEAK	[11:0]	r	0x000 (0 dec)	READ_VOUT_PEAK stores the maximum VOUT value read.
RESERVED	[15:12]		0x0	

1.66 READ_IOUT_PEAK

Address: 0xF1

Reset: 0x0000

READ_IOUT_PEAK stores the maximum IOUT value read. The command is automatically cleared when the data is read.

Table 332 READ_IOUT_PEAK command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read					READ_IOUT_PEAK											
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 333 READ_IOUT_PEAK command bits description

Field	Bits	Type	Reset	Description
READ_IOUT_PEAK	[11:0]	r	0x000 (0 dec)	READ_IOUT_PEAK stores the maximum IOUT value read.
RESERVED	[15:12]		0x0	

1.67 READ_PIN_PEAK

Address: 0xF2

Reset: 0x000000

READ_PIN_PEAK stores the maximum PIN value read. The command is automatically cleared when the data is read.

Table 334 READ_PIN_PEAK command structure

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	READ_PIN_PEAK																							
Write																								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 335 READ_PIN_PEAK command bits description

Field	Bits	Type	Reset	Description
READ_PIN_PEAK	[23:0]	r	0x000000 (0 dec)	Stores the maximum PIN value read.

1.68 READ_TEMP_1_PEAK

Address: 0xF3
Reset: 0x0000

READ_TEMP_1_PEAK stores the maximum FET temperature value read. The command is automatically cleared when the data is read.

Table 336 READ_TEMP_1_PEAK command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read					READ_TEMP_1_PEAK											
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 337 READ_TEMP_1_PEAK command bits description

Field	Bits	Type	Reset	Description
READ_TEMP_1_PEAK	0	r	0x000 (0 dec)	READ_TEMP_1_PEAK stores the maximum FET temperature value read.
RESERVED				

1.69 READ_VIN_VALLEY

Address: 0xF4
Reset: 0x0000

READ_VIN_VALLEY stores the minimum VIN value read. The command is automatically cleared when the data is read.

Table 338 READ_VIN_VALLEY command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read					READ_VIN_VALLEY											
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 339 READ_VIN_VALLEY command bits description

Field	Bits	Type	Reset	Description
READ_VIN_VALLEY	[11:0]	r	0x000 (0 dec)	READ_VIN_VALLEY stores the minimum VIN value read.
RESERVED	[15:12]		0x0	

1.70 READ_VOUT_VALLEY

Address: 0xF5
Reset: 0x0000

READ_VOUT_VALLEY stores the minimum VOUT value read. The command is automatically cleared when the data is read.

Table 340 READ_VOUT_VALLEY command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read					READ_VOUT_VALLEY											
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 341 READ_VOUT_VALLEY command bits description

Field	Bits	Type	Reset	Description
READ_VOUT_VALLEY	[11:0]	r	0x000 (0 dec)	READ_VOUT_VALLEY stores the minimum VOUT value read.
RESERVED	[15:12]		0x0	

1.71 READ_IOUT_VALLEY

Address: 0xF6
Reset: 0x0000

READ_IOUT_VALLEY stores the minimum IOUT value read. The command is automatically cleared when the data is read.

Table 342 READ_IOUT_VALLEY command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read					READ_IOUT_VALLEY											
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 343 READ_IOUT_VALLEY command bits description

Field	Bits	Type	Reset	Description
READ_IOUT_VALLEY	[11:0]	r	0x000 (0 dec)	READ_IOUT_VALLEY stores the minimum IOUT value read.
RESERVED	[15:12]		0x0	

1.72 READ_TEMP_1_VALLEY

Address: 0xF7
Reset: 0x0000

READ_TEMP_1_VALLEY stores the minimum FET temperature value read. The command is automatically cleared when the data is read.

Table 344 READ_TEMP_1_VALLEY command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read					READ_TEMP_1_VALLEY											
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 345 READ_TEMP_1_VALLEY command bits description

Field	Bits	Type	Reset	Description
READ_TEMP_1_VALLEY	[11:0]	r	0x000 (0 dec)	READ_TEMP_1_VALLEY stores the minimum temperature value read between the TSNS_P and TSNS_N pins.
RESERVED	[15:12]		0x0	

1.73 STATUS_MODE

Address: 0xF9
Reset: 0x0000

This command shows the operating mode, configured FET, device address and start-up current.

Table 346 STATUS_MODE command structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read				SELECTED_IST			SELECTED_DEVICE_ADDRESS				SELECTED_FET				STATUS_MODE	
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 347 STATUS_MODE command bits description

Field	Bits	Type	Reset	Description
STATUS_MODE	[1:0]	r	0x0 (0 = 0 dec)	Shows current operating mode
SELECTED_FET	[5:2]	r	0x0 (0 = 0 dec)	Shows configured FET
SELECTED_DEVICE_ADDRESS	[9:6]	r	0x0 (0 = 0 dec)	LSB part of the pmbus address [3:0]
SELECTED_IST	[12:10]	r	0x0 (0 = 0 dec)	Shows selected IST
RESERVED	[15:13]		0x0	

Table 348 Mode status

STATUS_MODE	Value	Description
0x0 (00 bin)	0	FDM with Digital comparators (DCM)
0x1 (01 bin)	1	FDM with Analog comparators (ACM)
0x2 (10 bin)	10	AADM
0x3 (11 bin)	11	Reserved

Table 349 Selected FET

SELECTED_FET	Value	Description
0x0 (0000 bin)	0	BSC027N10NS5ATMA1
0x1 (0001 bin)	1	BSC035N10NS5ATMA1
0x2 (0010 bin)	10	Reserved
0x3 (0011 bin)	11	IPT015N10N5ATMA1
0x4 (0100 bin)	100	IPB017N10N5ATMA1
0x5 (0101 bin)	101	IPB017N10N5LFATMA1
0x6 (0110 bin)	110	IPB020N10N5ATMA1
0x7 (0111 bin)	111	IPB020N10N5LFATMA1
0x8 (1000 bin)	1000	IPB027N10N5ATMA1

(table continues...)

Table 349 (continued) Selected FET

SELECTED_FET	Value	Description
0x9 (1001 bin)	1001	IPB032N10N5ATMA1
0xA (1010 bin)	1010	IPB033N10N5LFATMA1
0xB (1011 bin)	1011	Reserved
0xC (1100 bin)	1100	IPB072N15N3
0xD (1101 bin)	1101	IPB042N10
0xE (1110 bin)	1110	IPT016N10NM5LF
0xF (1111 bin)	1111	Programmed in MODE.FET_SELECT command bits

Table 350 Selected device address

SELECTED_DEVICE_ADDRESS	Value	Description
0x0 (0000 bin)	0	pmbus address [3:0] - 4'b0000
0x1 (0001 bin)	1	pmbus address [3:0] - 4'b0001
0x2 (0010 bin)	10	pmbus address [3:0] - 4'b0010
0x3 (0011 bin)	11	pmbus address [3:0] - 4'b0011
0x4 (0100 bin)	100	pmbus address [3:0] - 4'b0100
0x5 (0101 bin)	101	pmbus address [3:0] - 4'b0101
0x6 (0110 bin)	110	pmbus address [3:0] - 4'b0110
0x7 (0111 bin)	111	pmbus address [3:0] - 4'b0111
0x8 (1000 bin)	1000	pmbus address [3:0] - 4'b1000
0x9 (1001 bin)	1001	pmbus address [3:0] - 4'b1001
0xA (1010 bin)	1010	pmbus address [3:0] - 4'b1010
0xB (1011 bin)	1011	pmbus address [3:0] - 4'b1011
0xC (1100 bin)	1100	pmbus address [3:0] - 4'b1100
0xD (1101 bin)	1101	pmbus address [3:0] - 4'b1101
0xE (1110 bin)	1110	pmbus address [3:0] - 4'b1110
0xF (1111 bin)	1111	Programmed in PMBUS_CFG.PMBUS_DEVICE_ADDR command bits

Table 351 Selected IST

SELECTED_IST	Value	Description
0x0 (000 bin)	0	OC range 25 mV ; Start-up Current LIMIT : Set by START_ILIM bits in I_SNS_CFG command (100% of OC level by default)
0x1 (001 bin)	1	OC range 25 mV ; Start-up Current LIMIT : 50% of OC level
0x2 (010 bin)	10	OC range 25 mV ; Start-up Current LIMIT : 25% of OC level
0x3 (011 bin)	11	OC range 25 mV ; Start-up Current LIMIT : 12.5% of OC level
0x4 (100 bin)	100	OC range 12.5 mV ; Start-up Current LIMIT : 12.5% of OC level
0x5 (101 bin)	101	OC range 12.5 mV ; Start-up Current LIMIT : 25% of OC level
0x6 (110 bin)	110	OC range 12.5 mV ; Start-up Current LIMIT : 50% of OC level
0x7 (111 bin)	111	OC range 12.5 mV ; Start-up Current LIMIT : Set by START_ILIM bits in I_SNS_CFG command (100% of OC level by default) or in case of FDM

2 Revision history

Revision	Date	Subjects (major changes since last revision)
2.0	2022-11-22	First release.

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