CoolSiC™ JFET Evaluation Board user guide

About this document

Scope and purpose

This document serves as the user guide for CoolSiC™ JFET evaluation boards “EVAL_IJCQ75J1BB” and “EVAL_IJCQ120J1BB”, which features 750 V and 1200 V CoolSiC™ JFET devices, respectively. It outlines the hardware architecture of the evaluation boards, explains their key functional features, and provides step-by-step instructions for operating the boards and conducting laboratory experiments.

Intended audience

This document is intended for developers, researchers, and Power Electronics professionals who are evaluating the latest power semiconductor switches from Infineon Technologies for solid-state circuit breaker applications. The intended users must be trained in working with high-voltage equipment.

About this product group

Target applications

- Solid-state circuit breakers
- Motor control
- Battery disconnect switch
- E-Fuse

Product family

- 750 V and 1200 V CoolSiC™ JFET
- 750 V and 1200 V CoolSiC™ MOSFET
- 600 V CoolMOS™ MOSFET

Evaluation Board

This evaluation board is designed to assess the behavior and performance of transistors built on Infineon's cutting-edge CoolSiC™ technology, specifically for use in solid-state circuit breaker applications. It is important to note that this board is not intended to serve as a reference or demonstration platform. Instead, it is configured in a bi-directional common source back-to-back topology, enabling the voltage blocking in both DC and AC operating modes. Detailed design information and layout files are available through the Altium design package provided on Infineon website.

Note: PCB and auxiliary circuits are NOT optimized for final customer design.

Safety precautions

Note: *Please note the following warnings regarding the hazards associated with development systems*

Safety precautions

	**Warning:** *The DC link potential of this board is up to 1000 VDC. When measuring voltage waveforms by oscilloscope, high voltage differential probes must be used. Failure to do so may result in personal injury or death.*
	**Warning***: The evaluation or reference board contains DC bus capacitors which take time to discharge after removal of the main supply. Before working on the drive system, wait five minutes for capacitors to discharge to safe voltage levels. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Warning:** *The evaluation or reference board is connected to the grid input during testing. Hence, high-voltage differential probes must be used when measuring voltage waveforms by oscilloscope. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Warning:** *Remove or disconnect power from the drive before you disconnect or reconnect wires, or perform maintenance work. Wait five minutes after removing power to discharge the bus capacitors. Do not attempt to service the drive until the bus capacitors have discharged to zero. Failure to do so may result in personal injury or death.*
	**Caution:** *The heat sink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.*
	**Caution:** *Only personnel familiar with the drive, power electronics and associated machinery should plan, install, commission and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.*
	**Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	**Caution:** *A drive that is incorrectly applied or installed can lead to component damage or reduction in product lifetime. Wiring or application errors such as undersizing the motor, supplying an incorrect or inadequate AC supply, or excessive ambient temperatures may result in system malfunction.*
	**Caution:** *The evaluation or reference board is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials that are unnecessary for system installation may result in overheating or abnormal operating conditions.*

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1 The board at a glance

The JFET evaluation board serves as a platform to evaluate the performance of Infineon's latest CoolSiC™ technology switches in Q-DPAK packages, which meets the $R_{DS(on)}$ requirements for solid-state circuit breaker (SSCB) applications. This document focuses primarily on evaluating CoolSiC™ JFETs.

The evaluation kit contains two boards: a baseboard and a DUT board. The main functions of the baseboard include supplying power to the logic circuitry, providing adjustable voltage rails, and delivering control signals to the gate drivers. The DUT board is available in two versions: one featuring 750 V CoolSiC™ JFETs and other featuring 1200 V CoolSiC™ JFETs. Each DUT board can be assembled with up to four switches along with their corresponding Infineon gate drivers. At the end of this section, a complete description of the board parameters is provided.

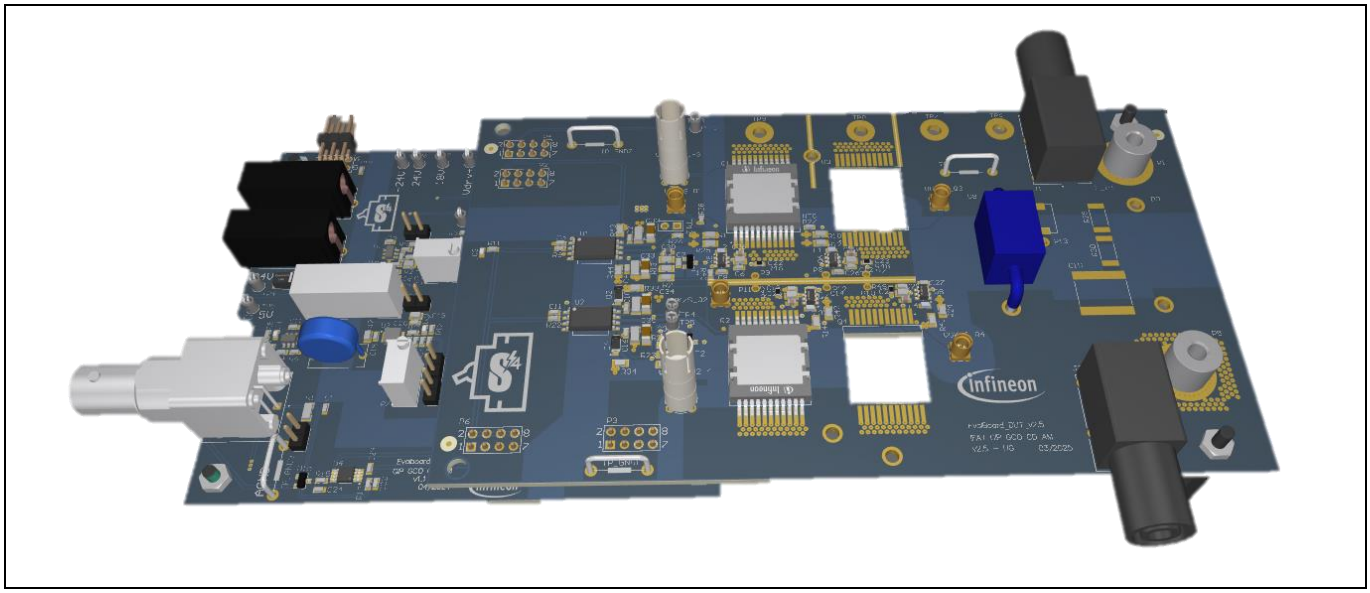


Figure 1 JFET evaluation board

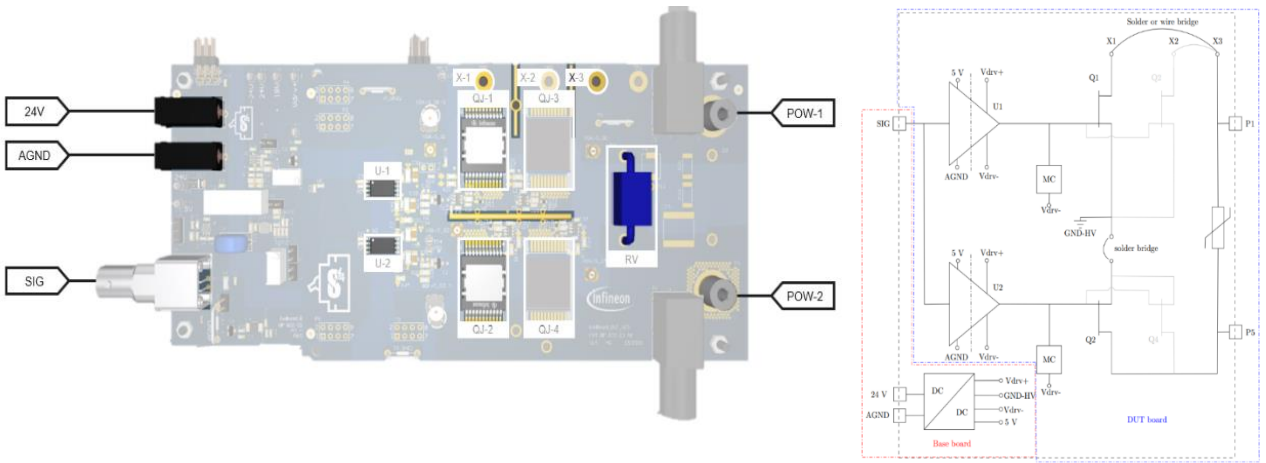
1.1 Scope of supply

The JFET evaluation board includes Infineon products listed below, as shown in Figure 1

- IJCQ120RM23J1 (noted as QJ-1 to QJ-4): 1200 V CoolSiC™ JFET in a Q-DPAK package with a typical
  $R_{DS(on)}$ = 2.3 mΩ (used on EVAL_IJCQ120J1BB board)
- IJCQ75RM16J1 (noted as QJ-1 to QJ-4): 750 V CoolSiC™ JFET in a Q-DPAK package with a typical $R_{DS(on)}$ = 1.61 mΩ (used on EVAL_IJCQ75J1BB board)
- IRFTS8342TRPBF: Active gate-clamping FET
- 1ED312xMU12H (noted as U-1 and U-2) Infineon EiceDRIVER™ single-channel isolated gate driver IC, providing 5.7 kV (rms) galvanic isolation with an active Miller clamp or separate output configuration

The JFET evaluation board focuses on evaluating the behavior of the switches. It is not designed to function as a complete solid-state breaker system. The board does not include passive components for modeling load impedances, nor does it incorporate sensing, control, or safety devices.

1.2 Block diagram



a)b)

Figure 2 The diagram shows a) the JFET evaluation board and b) its block diagram

1.3 Main features

- Evaluation of 750 V and 1200 V CoolSiC™ JFETs devices in Q-DPAK packages, tailored for solid-state power distribution applications
- Adjustable driving voltages on the evaluation board enable operation not only of CoolSiC™ JFETs but also CoolSiC™ and CoolMOS™ MOSFETs
- DC and AC operations are supported through the common-source (anti-series) configuration of the power semiconductors
- Suitable for testing single-pulse and repetitive inductive clamping, and application specific dv/dt ruggedness events
- Supports paralleling of two Q-DPAK devices
- Includes Miller clamp to prevent parasitic turn-on of CoolSiC™ JFETs during steep voltage transients
- Requires only one supply to power two gate drivers
- Provides single-pulse capability up to 2000 A

1.4 Board parameters and technical data

Table 1 Baseboard settings

Inputs	Connectors	Settings
Power supply	24 V/AGND	Supply voltage: 24 V Current limit: 500 mA
Input signal	Sig	Signal level: 0/5 V Use a load impedance 50 Ω or connect the J3 in the baseboard to activate a 50 Ω impedance load as introduced in Table 4

Table 2 DUT board maximum ratings

The board at a glance

Parameter	Symbol	Connectors	Conditions	Value	Unit
Maximum AC RMS voltage	$V_{max(AC)}$	P1 – P5	750 V CoolSiC™ JFET and S25K250 assembled (default configuration of board “EVAL_IJCQ75J1BB”)	250	Vrms
			1200 V CoolSiC™ JFET and S25K420 assembled (default configuration of board “EVAL_IJCQ120J1BB”)	440	
Maximum DC voltage (switches open)	$V_{max(DC)}$	P1 – P5	With provided MOV, when the switches are opened as: • 750 V CoolSiC™ JFET • 1200 V CoolSiC™ JFET	320 585	VDC
			Without clamping elements, when the switches are opened as: • 750 V CoolSiC™ JFET • 1200 V CoolSiC™ JFET	400 800	VDC
Maximum load current	I_{RMS}	P1 – P5	NA (see Note 1 below)	NA	Arms
Maximum current, single pulse	I_{AS}	–	limited by assembled semiconductor and assembled clamping element	716	A
Maximum inductive energy of circuit		–	limited by assembled clamping element as: • 750 V CoolSiC™ JFET • 1200 V CoolSiC™ JFET	345 710	J (2 ms)

Note:

1. *This board was not designed for continuous current flow but for pulse testing. Monitor the self-heating of the board and the components, in case of continuous current conduction.*
2. *Please check the voltage ratings of the capacitances used.*

2 System and functional description

2.1 Getting started

1. Unpack the evaluation board and check for visible damages
2. Make sure that the mounted device part number (MOV) matches the JFET voltage class shown in Table 3

Table 3 Clamping element selection based on CoolSiC™ JFET's voltage class

V_{BDSS}	Power switches	Clamping element
750 V	IJCQ75RM16J1	EPCOS S25K250E4R12
1200 V	IJCQ120RM23J1	EPCOS S25K420E4R12

3. Set the driving voltage by configuring the baseboard according to Table 4
4. Supply the baseboard with 24 V, where the voltage is between the board connectors named "24V" and "AGND" in Figure 3

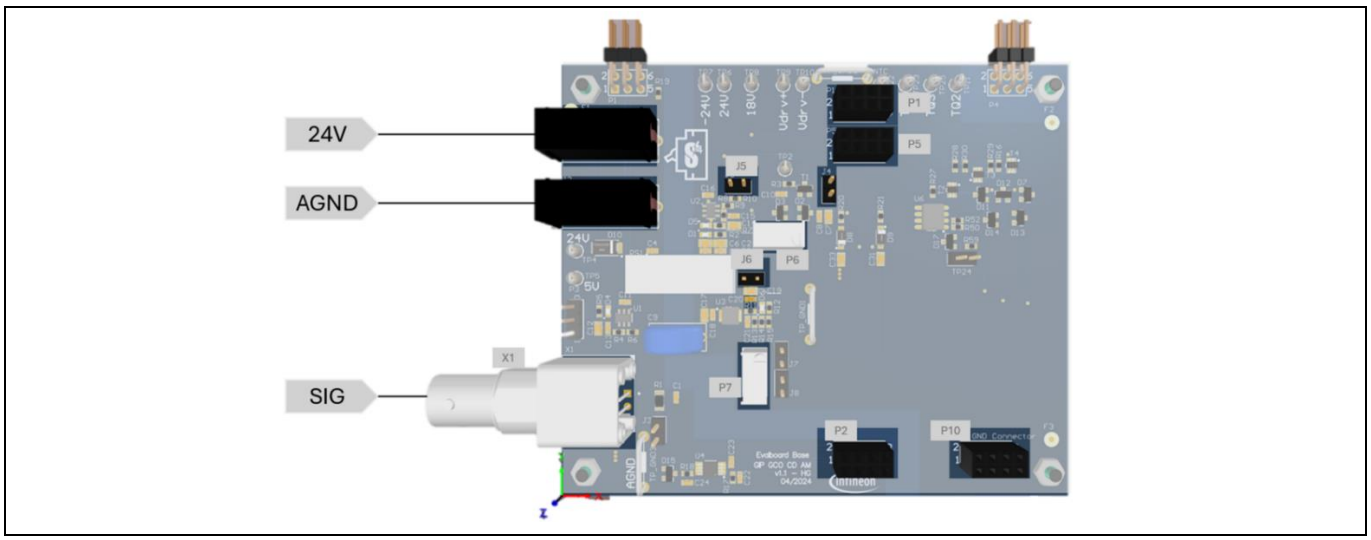


Figure 3 Baseboard PCB

Note: Keep in mind that JFET is a normally-on device, therefore, the VGS of the JFET needs to be supplied with –18 V initially.

5. Follow Table 4 to provide the adjustable voltages (V_{drv+} and $V_{drv–}$) based on the test type and the used switch

Table 4 Adjustment of driving voltages via baseboard settings

Device	Target driving voltage		Setting for V_{drv+}			Setting for V_{drv-}		
	V_{drv+}	V_{drv-}	P6	J4	J5	P7	J6	R 11
CoolSiC™ JFET 750 V and 1200 V	+2 V	–18 V	Adjust it to ~4.9 kΩ	DNP	connected	Adjust it to ~61 kΩ	DNP	connected
CoolSiC™ MOSFET	18 V	0 V	DNP	connected	connected	DNP	connect	Disassemble

Device	Target driving voltage		Setting for V_{drv+}			Setting for V_{drv-}		
	V_{drv+}	V_{drv-}	P6	J4	J5	P7	J6	R 11
CoolMOS™ MOSFET	12 V	0 V	Adjust it to ~29.4 kΩ	DNP	connected	DNP	connect	Disassemble

6. Provide input signal from the function generator to the BNC connector. One pulse is needed to meet the scenarios that emulate the application test scenarios discussed in the following sections. The signal travels from the baseboard through connector P2 to the DUT via connector P6. Connectors such as P2, P5, P10, and P11 interface with the DUT board. See Table 5 and Table 6 for more details
7. As shown in Figure 4, fill in the solder bridge S-3, which connects the source pins of the device pair QJ-1 /QJ-3 with the source pins of the device pair QJ-2/QJ-4
8. Additional steps are required to connect the drain pins of QJ-1 and QJ-3 to the power connector P1. This can be done in either of the following two ways:
   - Connect X-1 to X-3 and X-2, and X-4 with jumper wires. This option allows current measurement using a Rogowski current probe
   - Fill in solder bridges S-1 and S-2
9. Connect the baseboard to the DUT board using connectors P1, P2, P5, and P10. See Table 5 for more details

As the board is designed to be an evaluation platform for the solid-state circuit breaker switches, the previous steps are introduced to get the board ready.

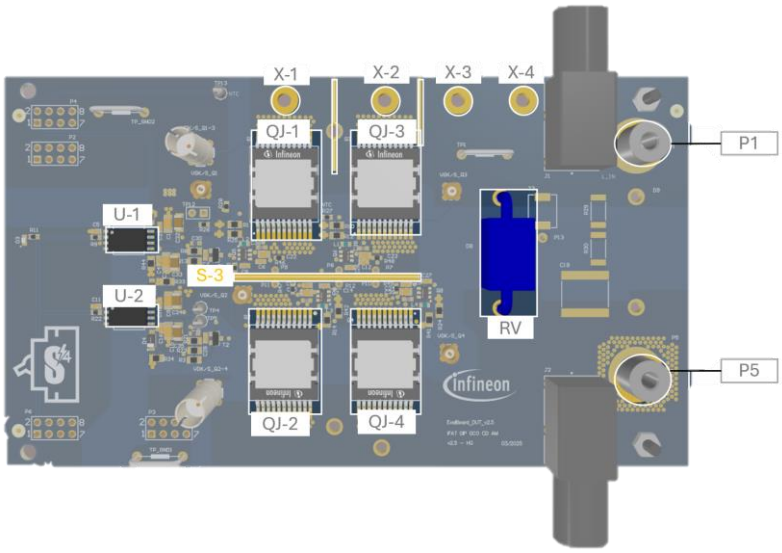


Figure 4 DUT board PCB

2.2 Description of the functional blocks

The architecture of the evaluation board consists of several key components, which are detailed in the subsequent sections. Specifically, the methodology for generating the driving voltages is elaborated in Section 2.2.1, whereas the functionality of the JFET driving circuit is addressed in Section 2.2.2.

2.2.1 Auxiliary supply (baseboard)

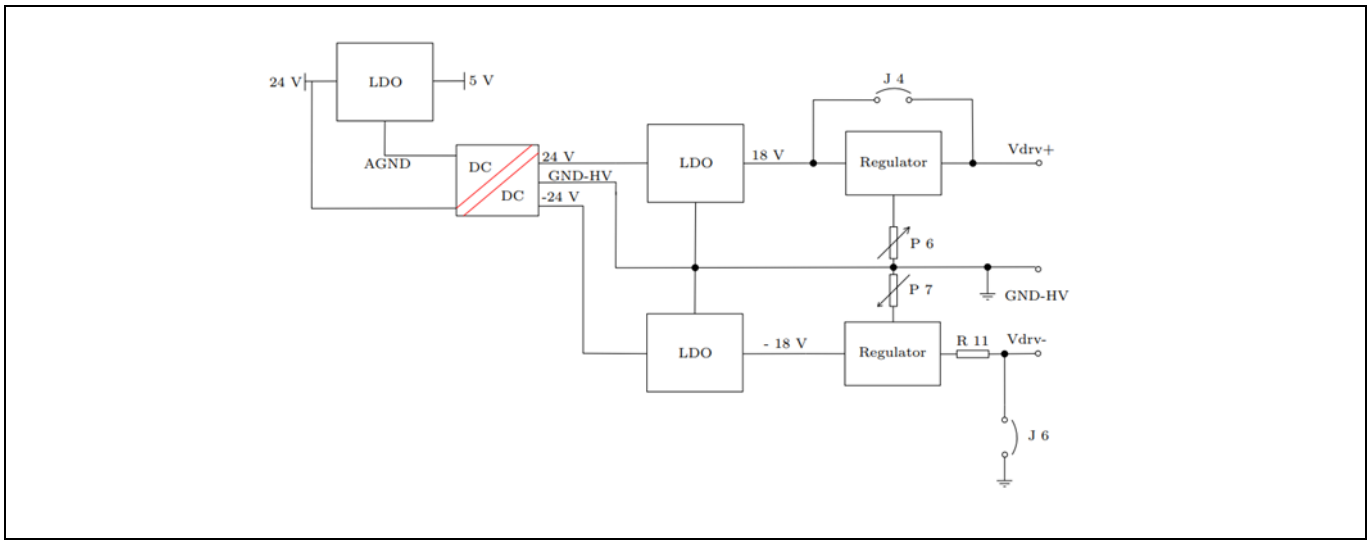


Figure 5 Baseboard block diagram

A main feature of the baseboard is its ability to provide isolated adjustable driving voltage levels V_{drv+} and V_{drv-} as shown in Figure 5, to the isolated gate drivers mounted in the DUT board. This flexibility enables the board to support a wide range of power semiconductor switches, including normally-on JFETs and normally-off MOSFETs. As shown in Figure 5, a Low-dropout (LDO) regulator is utilized to provide power to the low-voltage logic side of the gate driver by generating a stable 5 V_{DC} output. Furthermore, an isolated DC-DC converter is employed to provide galvanically isolated supply voltages for the output stage of the gate driver. The V_{drv+} and V_{drv-} voltages are then generated using linear regulators, which are crucial for the operation of the gate driver. For detailed instructions on adjusting the V_{drv+} and V_{drv-} levels, see Table 4.

2.2.2 Driving circuit (DUT board)

The JFET evaluation board utilizes Infineon's gate driver 1ED3124MU12H, which belongs to the EiceDRIVER™ Compact 1ED31xx (X3 compact) family. EiceDRIVER™ 1ED3124MU12H is a 14 A, 5.7 kV (RMS) single-channel gate driver with separate output, providing input-to-output isolation along with accurate and stable timing performance.

This driver features a galvanically isolated coreless transformer design, enabling it to operate with a bipolar supply and across a wide range of supply voltages. The input stage of the gate driver is powered by 5 VDC, while the output stage is supplied by V_{drv+} and V_{drv-}.

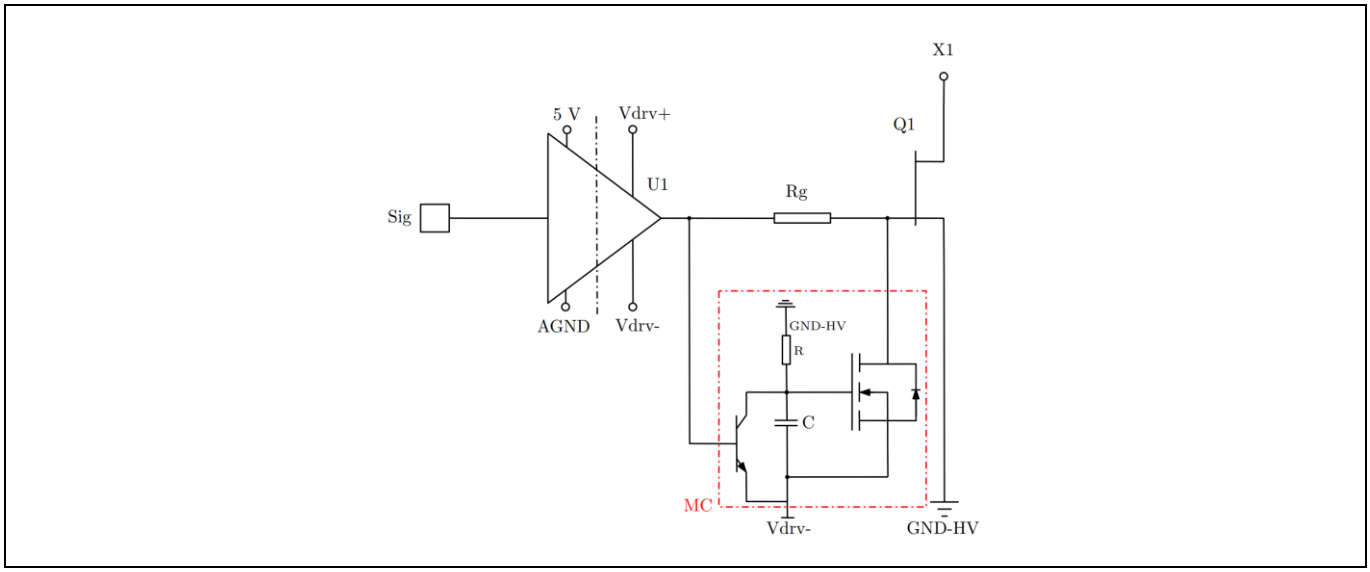


Figure 6 Gate driving circuit(simplified)

JFETs have a relatively high gate-drain capacitance (C_{GD}). As a result, the JFETs are affected by steep drain-to-source voltage rises, which can cause return-on behaviors during positive dv/dt transitions and gate-source voltage undershoots during negative dv/dt transitions. The gate clamping circuit is essential to ensure keeping JFETs successfully in off-state operation. Specifically, the clamp provides an extremely low-impedance connection to the turn-off gate voltage, while the power semiconductor is in the off state.

To reduce possible return-on behavior, a Miller clamping circuit is implemented using Infineon power MOSFET IRFTS8342TRPBF, as shown in Figure 6. In detail, the clamping FET is activated after a certain time, which is determined by the RC circuit.

In addition to the importance of using the clamping FET in the circuit, its body diode provides another significant protection mechanism. During negative dv/dt events, the body diode provides a path for the negative current to pass.

2.3 Application test setups

This section provides a comprehensive guide on operating the evaluation board in two distinct application scenarios. They are designed to assess and evaluate the performance of JFET switches under specific conditions. Section 2.3.1 includes inductive clamping application measurements and Section 2.3.2 shows the dv/dt robustness events in detail.

2.3.1 Inductive clamping application measurements

A fundamental feature of a solid-state circuit breaker is its ability to turn off high currents within a very short time, even when operating in an inductive circuit. This section explains how to use the evaluation board under such harsh conditions. Before starting with the single-pulse inductive clamping basic operation, follow the steps listed in Table 4 to configure the baseboard and set up the connections as shown in Figure 7.

The components required for the inductive clamping test are an external power inductor, a capacitor, and an HV-DC supply.

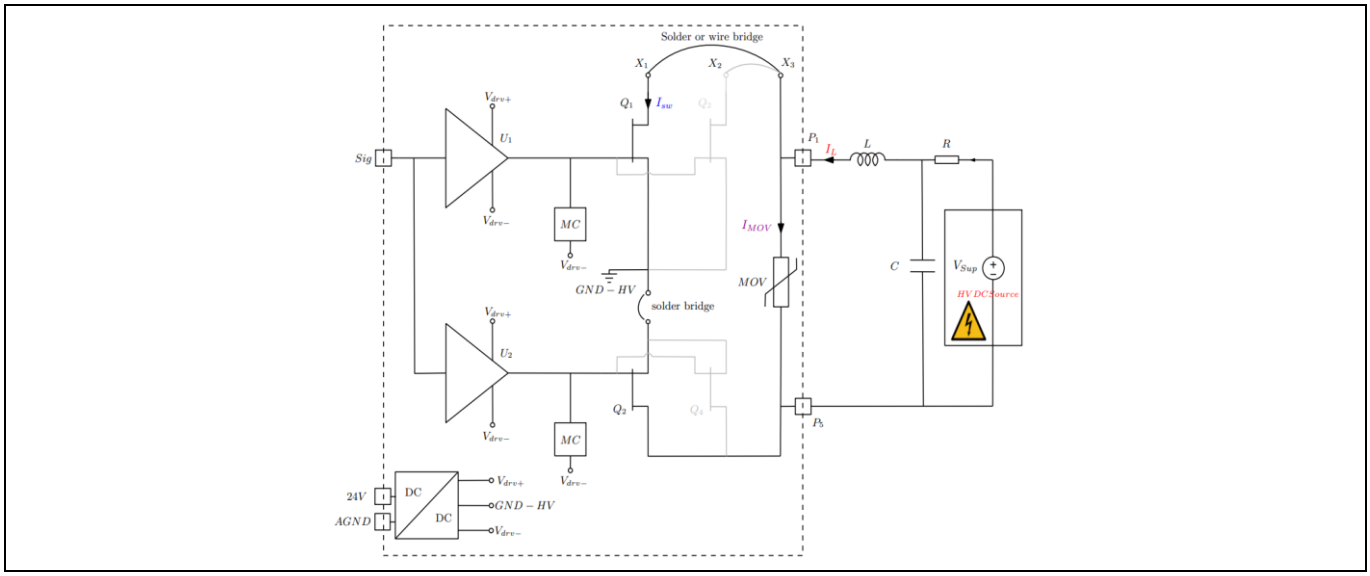


Figure 7 Pulse inductive clamping setup (simplified)

To perform the inductive clamping measurements, it is recommended to follow the following steps:

1. Configure the board according to Table 4
2. Prepare test setup as shown in Figure 7
3. Apply an input signal to the pin labeled “Sig”. The required pulse width can be calculated using the inductor formula (VL = L. $\Delta I_L/\Delta t$). To evaluate the JFETs’ avalanche currents, the value of “ΔI_L” is selected such that the resulting current reaches the single pulse avalanche current “I_{AS}” of the switch

Note: Another possible approach is to start with a short pulse width and gradually increase it until the desired current level is reached.

4. Capture waveforms of V_{GS}, V_{DS}, and I_D

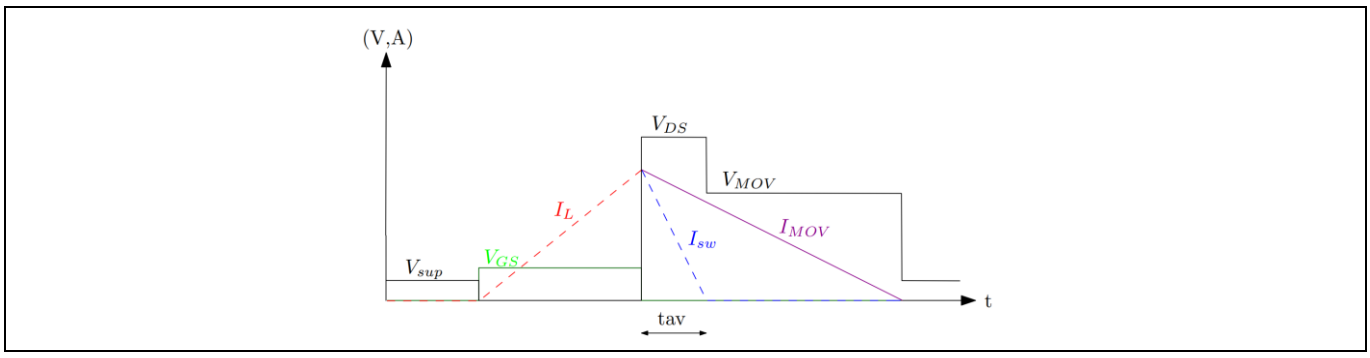


Figure 8 Avalanche waveforms(simplified)

The avalanche waveforms are shown in Figure 8. The inductor current increases until it reaches the desired value, determined by the width of the applied input pulse. While turning off the JFETs, the magnetic field in the inductor, which is considered as high energy cannot immediately diminish. As a result, the inductor current commutates from the JFET to the MOV and the MOV dissipates the magnetic energy stored in the inductor. During this commutation process, the high di/dt generates a significant voltage drop across the drain-to-source terminals of the JFETs. The MOV therefore plays a vital role in reducing the stress on the power semiconductor switches.

The parameters indicated in Figure 8 are defined as follows:

- V_{sup}: supply voltage
- V_{gs}: gate source voltage of the JFET
- I_L: Inductor current
- $V_{(BR)DSS}$: Drain-source breakdown voltage of the JFET
- V_{MOV}: Voltage across the MOV
- I_{sw}: switch current
- I_{MOV}: MOV current
- T_{av}: Avalanche period

2.3.2 dv/dt application measurements

Solid-state circuit breakers usually consist of a semiconductor switch and a series-connected airgap device. When the system is off, the air gap device blocks the entire voltage. Once the air-gap device turns-on, the drain-to-source voltage of the semiconductor rises rapidly. Without specific design considerations, this rapid voltage change can cause an unintended turn-on of the power semiconductor due to its Miller capacitance.

This section explains the dv/dt measurements and their influence on the performance of CoolSiC™ JFETs. Since the primary purpose of this test is to apply an external dv/dt to the evaluation board to assess the JFET behavior, an external switch is required. As shown in Figure 9, S_1 represents this external switch, which may be either a mechanical switch or a semiconductor switch.

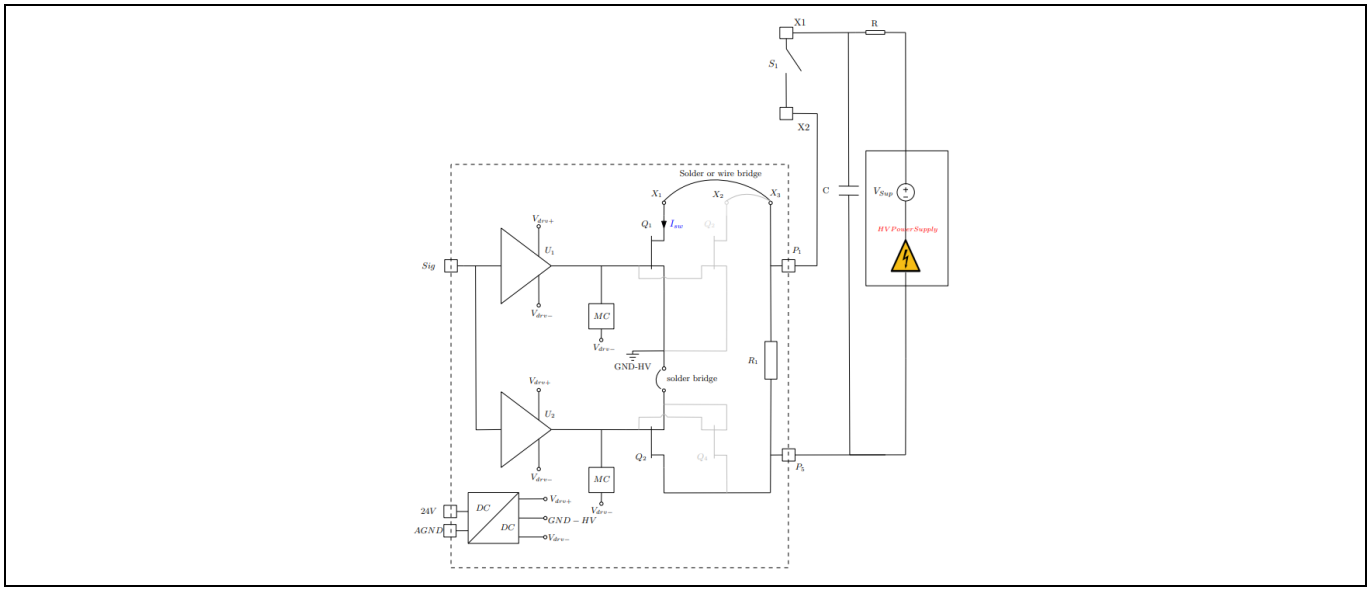


Figure 9 dv/dt setup (simplified)

To perform the dv/dt measurements, it is recommended to follow the steps below:

1. Configure the board according to Table 4
2. Prepare the test setup as shown in Figure 9
3. Adjust the signal (one pulse) from the function generator to a duration of 100 µs and apply it to the gate of the external switch S1. Additionally, the main gate drivers are pulled down to the voltage V_{drv-} to keep the device in off-state by connecting header P3

Note: In this test, the external switch is an Infineon product (CoolSiC™ AIMDQ75R008M1H)

4. Change the V_{sup} voltage to get different slew rate (100 V, 200 V, and so on)

Note: The test is performed at a maximum value V_{sup}= 400 V which results in having 10 V/ns that meets the requirements with SSCB

5. Capture waveforms of V_{GS}, V_{DS}, and I_D

Note: P3 header is introduced specially for dv/dt tests to pull down the input signal of the gate driver to 0 V, a connection between the two marked pins is highly recommended as shown in Figure 10.

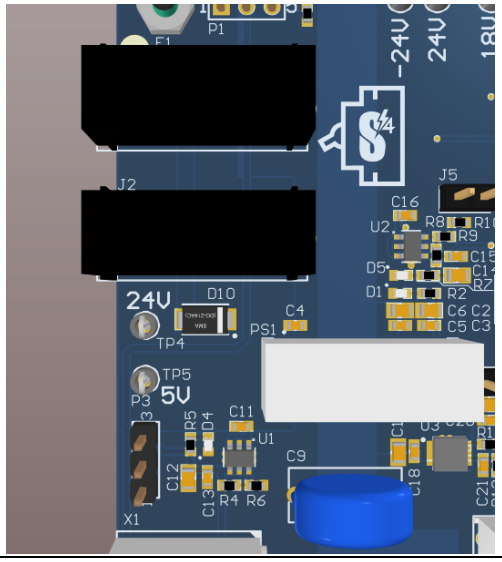


Figure 10 Pin connections on header P3 (Baseboard)

3 System design

3.1 Schematics

The baseboard schematic is shown in Figure 11.

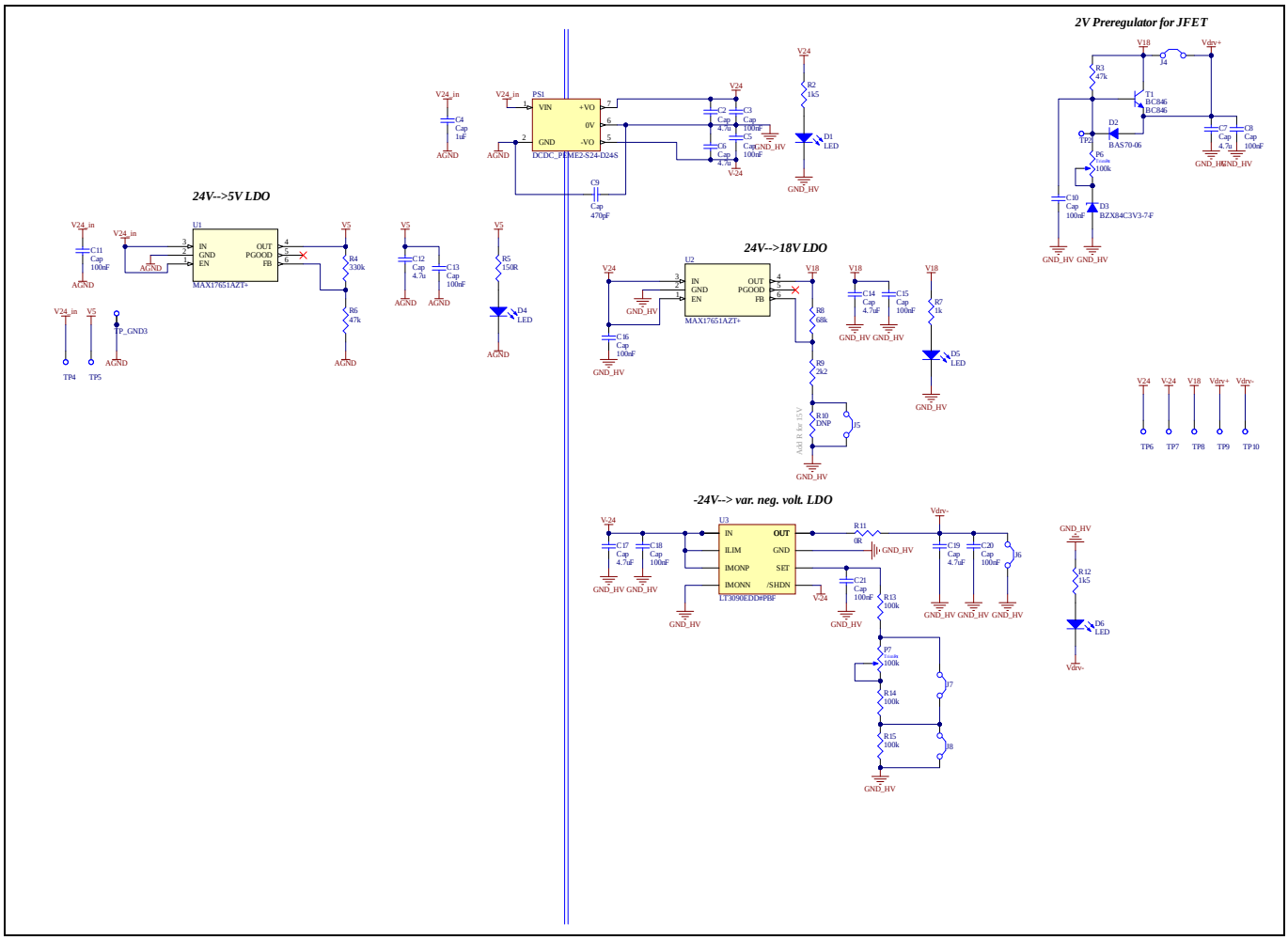


Figure 11 Baseboard Schematic

The DUT board schematic is shown in Figure 12.

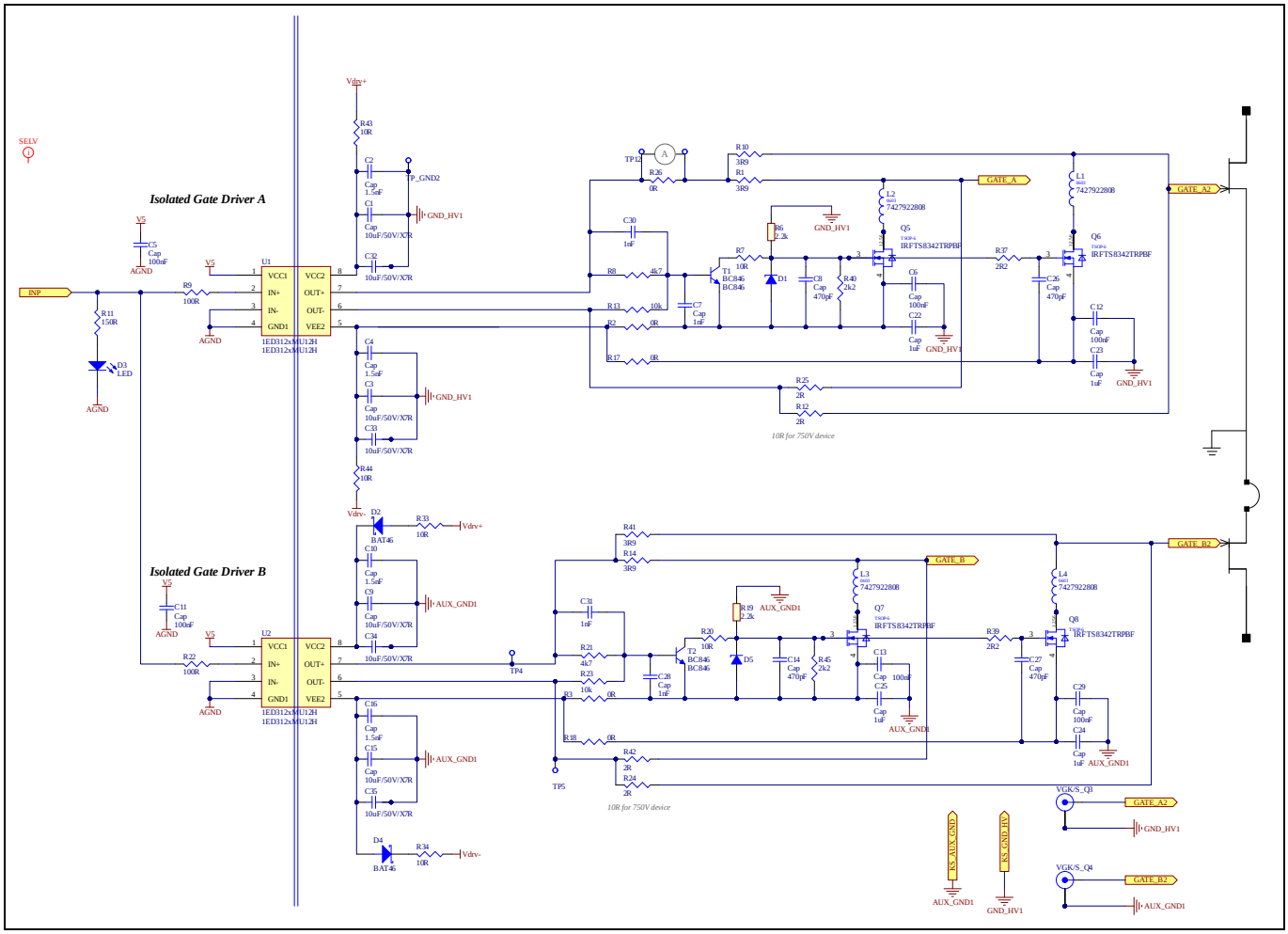


Figure 12 DUT board Schematic

3.2 Connector details

Table 5 Baseboard connectors and interfaces

Connectors and interfaces	Function
J1	Socket +24 V
J2	Socket AGND
X1	Sig

Table 6 DUT board connectors and interfaces

Connectors and interfaces	Function
P1	Power connector
P5	Power connector
J1	Power socket
J2	Power socket

4 Test results

This section presents the performed measurements of the CoolSiC™ 750 V into two subsections. Section 4.1 shows the resulted waveform of the inductive clamping measurements, while Section 4.2 provides the measurement outcomes of the dv/dt test. Furthermore, Section 4.3 highlights the crucial role of the clamping FET and its implications on the overall system performance.

4.1 Test points

This section describes example waveforms captured from the inductive clamping application test, as described in Section 2.3.1. Through this test, the cut-off current capability of JFET can be recorded and studied. During turn-off, the JFET takes over the energy until the cutting off voltage level of the MOV is reached. Once the MOV voltage cut-OFF is reached, the MOV takes over the rest of the energy. That helps to reduce the stress on the power electronics elements. As shown in Figure 13, the JFET operates under avalanche conditions and the switch waveforms VGS, ID, and VDS are captured. The switch is turned off at a current value close to the datasheet- specified avalanche pulse current, I_{AS} =716 A.

During avalanche events, when the switches are turning off, a steep -dv/dt in the drain-to-source voltage can induce oscillations on the gate-to-source voltage of the JFET. Therefore, it is a must to keep the undershoot voltage of the gate-to-source within the datasheet limits. To ensure stable operation, a small capacitor may be placed between the gate and source pins.

As shown in Figure 13, the V_{GS} waveform exhibits a safe undershoot that remains below the datasheet limit, and no signs of return-on behavior are observed in either the current or voltage waveforms.

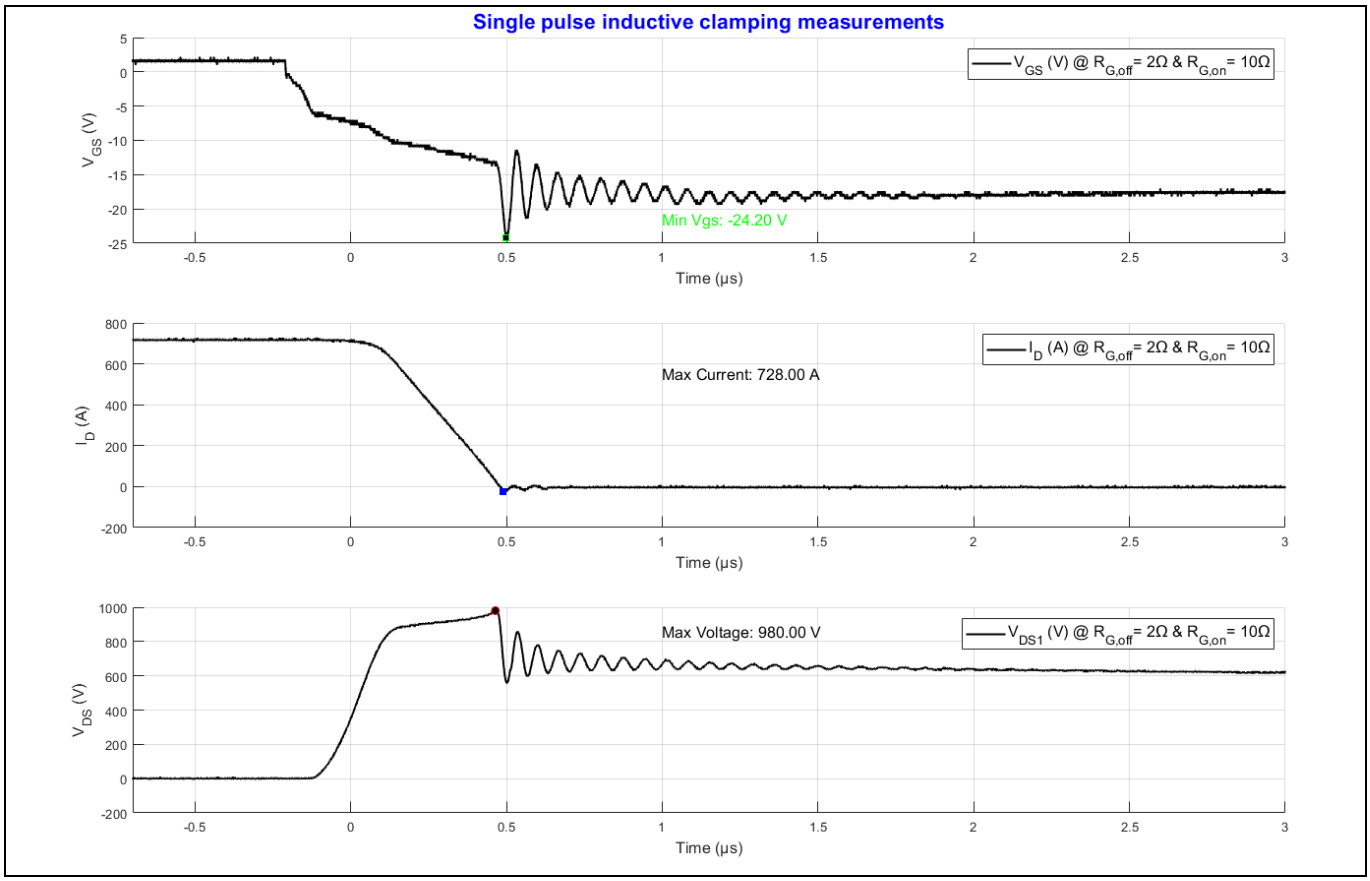


Figure 13 Single pulse inductive clamping waveforms acquired from Q1

4.2 dv/dt measurement results

This section shows examples of waveforms captured from the test setup introduced in Section 2.3.2. The dv/dt test is performed to determine whether a dv/dt-induced turn-on event can occur due to an external switch. This test emulates conditions similar to those present in the SSCB when actuated by the safety relay.

To conduct the test, the JFET is used as a passive device (fully OFF) with V_{GS}= –18 V. As described previously, S1 is required to generate a certain dv/dt. As shown in Figure 14, the measurements present the voltages and currents of Q1 as V_{GS}, V_{DS}, and I_D. The integration of the current ∫Id dt, is shown at the bottom of Figure 14 to help evaluate the possibility of an induced turn-on.

A return-on event may occur if the first peak value of the integrated current waveform exceeds the total gate charge (Q_G) of the JFET device. Producing different values of external dv/dt are required to evaluate the performance of the JFETs. Applying supply voltages (100 V, 200 V, 300 V, and 400 V) are conducted while using similar $R_{G,OFF}$. As shown in Figure 14, applying higher supply voltages results in proportionally higher external dv/dt. However, the gate-to-source voltage does not reach the threshold voltage, indicating no-sign of return-on in either the voltage or current waveforms.

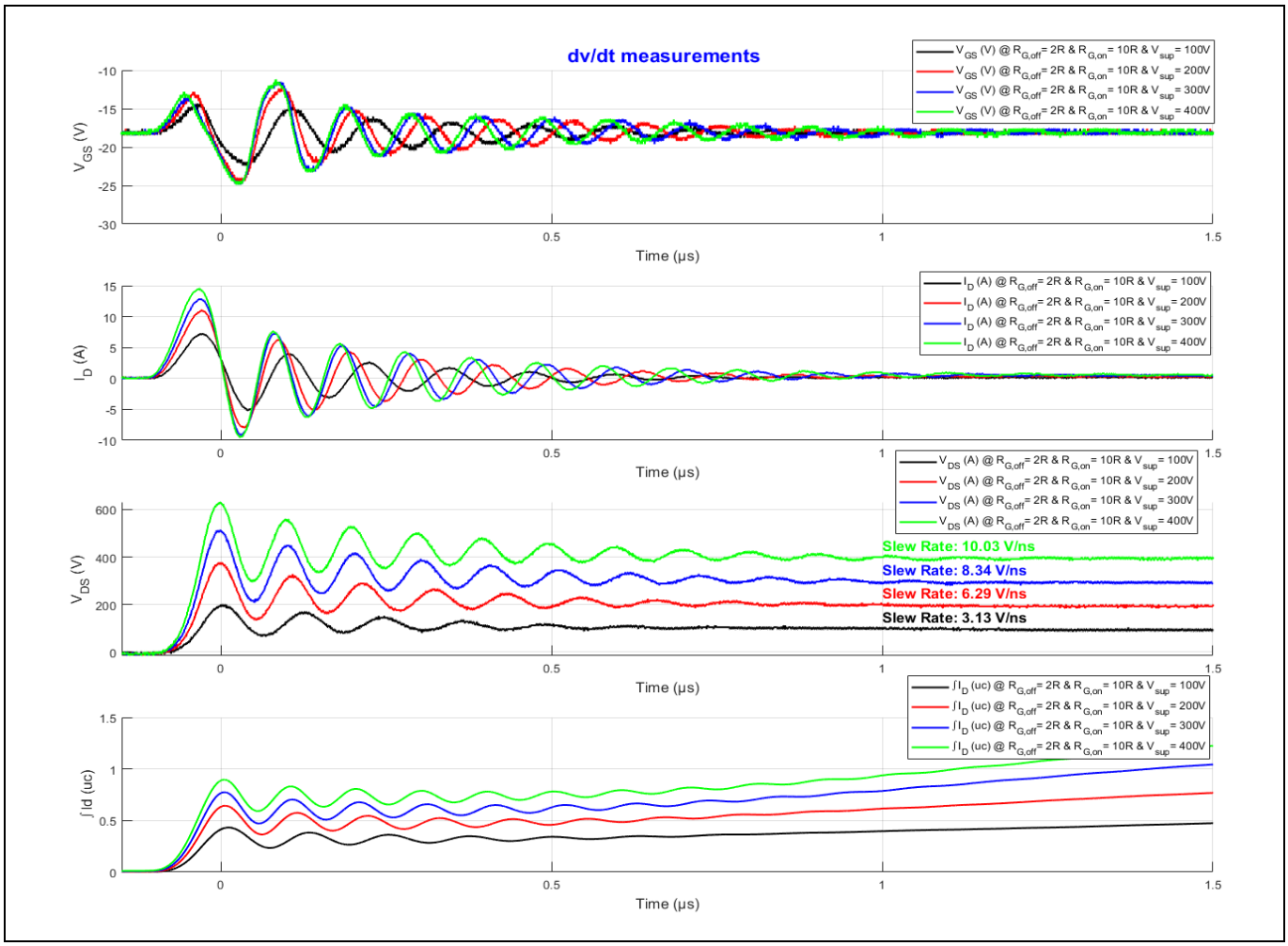


Figure 14 dv/dt measurements at R_{goff} = 2 Ω

4.3 Clamping FET optimization

The clamping FET is crucial to eliminate the return-on events caused by high dv/dt during turn-off, as discussed in Section 2.3.2. Figure 15 shows the working operation of the JFET during the turn-off event in single-pulse inductive clamping measurement performed without optimizing the clamping FET. A return-on phenomenon is clearly seen in gate-to-source voltage of the JFET.

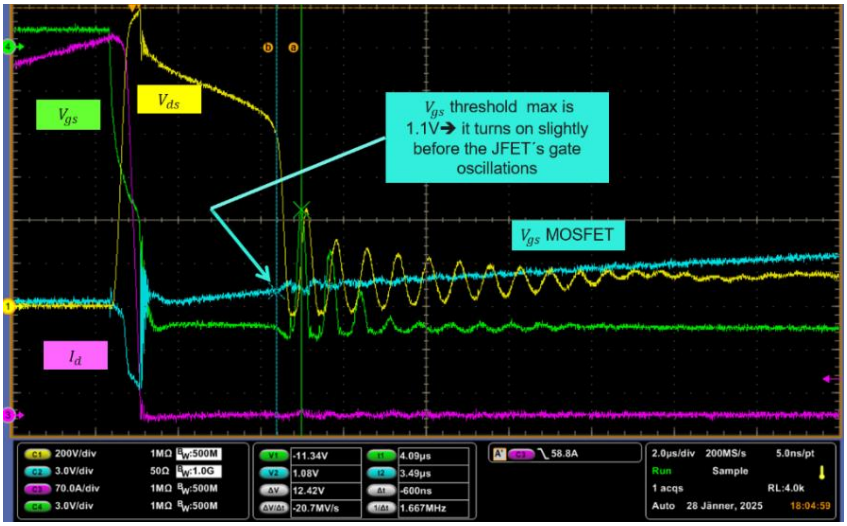


Figure 15 Inductive clamping measurements without gate clamping: Oscillations of the drain-to-source voltage can cause oscillations of the gate-to-source voltage after the inductor or load current has decayed to zero

Optimization of the gate clamping circuit has been done by controlling the turn-on timing of the clamping FET by adjusting the RC circuit introduced in Figure 6. After this optimization, the return-on issue resolved, as shown in Figure 16.

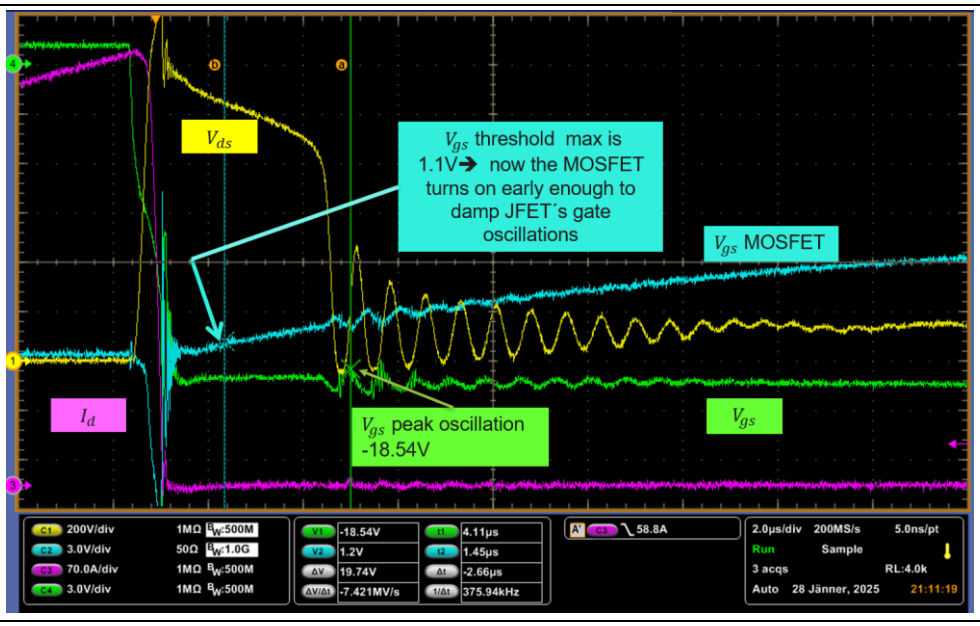


Figure 16 Eliminating return-on by implementing gate clamping FET: Stable gate-to-source voltage despite drain-to-source oscillations

Test results

There are still oscillations visible on the JFET's V_{DS} waveform after the current through the MOV reaches 0 A. These oscillations are caused by the interaction between the JFET's output capacitance and the line or load inductance. Also, corresponding V_{GS} oscillation is observed, influenced by the impedance between the JFET gate and the gate-clamp FET. Although this oscillation cannot be completely eliminated, it is important to note that the JFET's V_{GS} does not rise to its threshold voltage $V_{GS(th)}$, indicating that the gate-clamp FET is functioning as intended.

5 Related resources

- Silicon carbide CoolSiC™ MOSFETs
- Developer Community

References

[1] Infineon Technologies AG: CoolSiC™ JFET webpage; Available online

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[3] Infineon Technologies AG: Innovative top-side cooled package solution for high-voltage applications; Available online

Abbreviations or acronyms

Abbreviation	Expanded form
DNP	Do not populate
NA	Not applicable
SSCB	Solid state circuit breaker
DUT	Device under test

Revision history

Document revision	Date	Description of changes
V 1.0	2026-03-06	Initial release

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Do you have a question about this document?
Email: erratum@infineon.com

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