Half-bridge daughterboard series with different gate drive solutions for CoolGaN™ Transistors 650 V G5

Ordering code:

KIT_HB_GaN_ISO_TLL_A / KIT_HB_GaN_ISO_PFN_A / KIT_HB_GaN_BT_RC_TLL_A / KIT_HB_GaN_BT_RC_PFN_A / KIT_HB_GaN_BT_ML_TLL_A / KIT_HB_GaN_BT_ML_PFN_A

About this document

Scope and purpose

The KIT_HB_GaN series offers a portfolio of complete half-bridge daughterboard solutions for Infineon's CoolGaN™ Transistor 650 V G5 packaged with PG-LSON-8, and PG-HSOF-8, including several kinds of driver solutions:

- Isolated single-channel gate driver IC (EiceDRIVER™ 1EDB7275F) and a configurable isolated bias supply enabled by a simple single-channel non-isolated gate driver IC (EiceDRIVER™ 1EDN7511B)
- Dual-channel isolated gate driver IC with floating outputs (EiceDRIVER™ 2EDB7259Y)

The board enables driving CoolGaN™ Transistors with unipolar or bipolar gate-to-source voltages – compatible with gate injection transistor (GIT) products. It is an easy plug-in solution for designs with isolated single-channel or dual-channel gate driver ICs. The board can be configured with jumper wires without layout concerns.

Intended audience

This document targets power electronic engineers and designers interested in a configurable isolated bias supply or bootstrap driver for their GaN designs, featuring compactness, high efficiency, good regulation, and affordability.

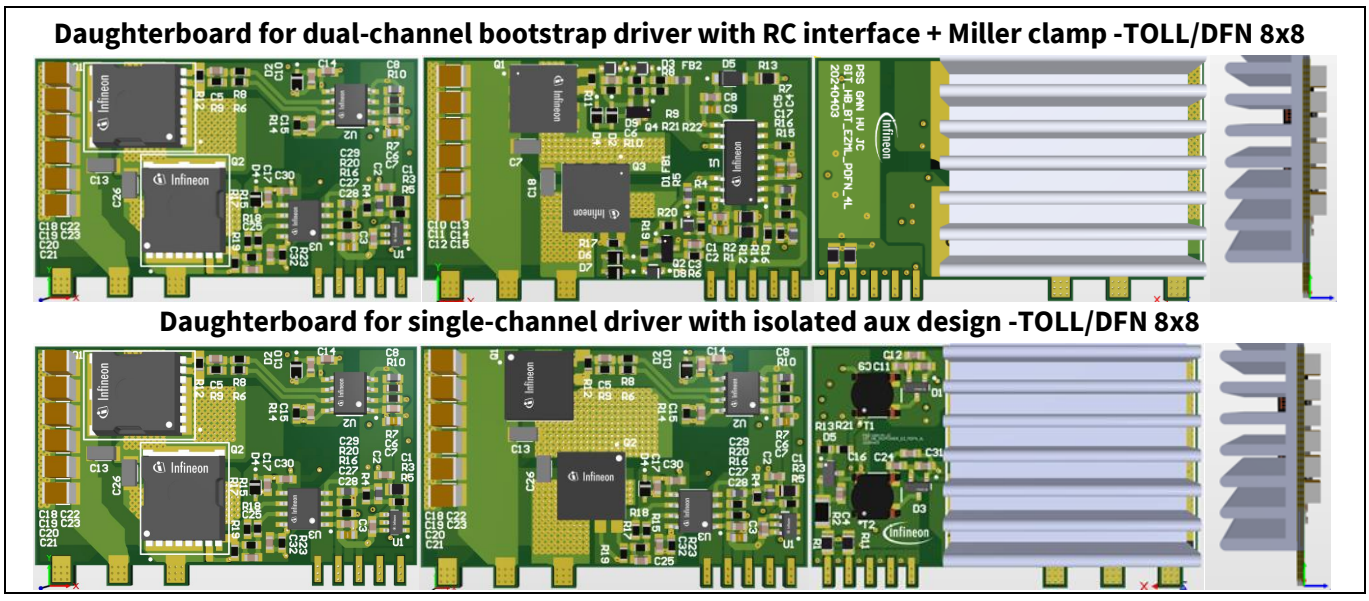

Figure 1 Front and back view of KIT_HB_ GaN series

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Safety precautions

Note: Please note the following warnings regarding the hazards associated with development systems.

Table 1 Safety precautions

	**Warning:** *The evaluation or reference board is connected to the grid input during testing. Hence, high-voltage differential probes must be used when measuring voltage waveforms by oscilloscope. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Caution:** *The heat sink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.*
	**Caution:** *Only personnel familiar with the drive, power electronics and associated machinery should plan, install, commission and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.*
	**Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	**Caution:** *The evaluation or reference board is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials that are unnecessary for system installation may result in overheating or abnormal operating conditions.*

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1 Introduction of the series board

Facing various application scenarios, CoolGaN™ Transistor can be paired with multiple driver solutions. This application manual introduces how to use CoolGaN™ Transistor with different driver solutions and explain their features. It also includes intuitive sub-board design to enable quick performance verification in actual systems.

The following sections will sequentially introduce the proposed driving solutions mentioned in this user guide, along with the experimental results.

1.1 RC interface for CoolGaN™ Transistor

RC interface circuit is the typical design choices for CoolGaN™ switches, for more in-depth design rules, see Gate drive configurations for GaN power transistors [10] document. The following figure shows the driver circuit for the EVBs:

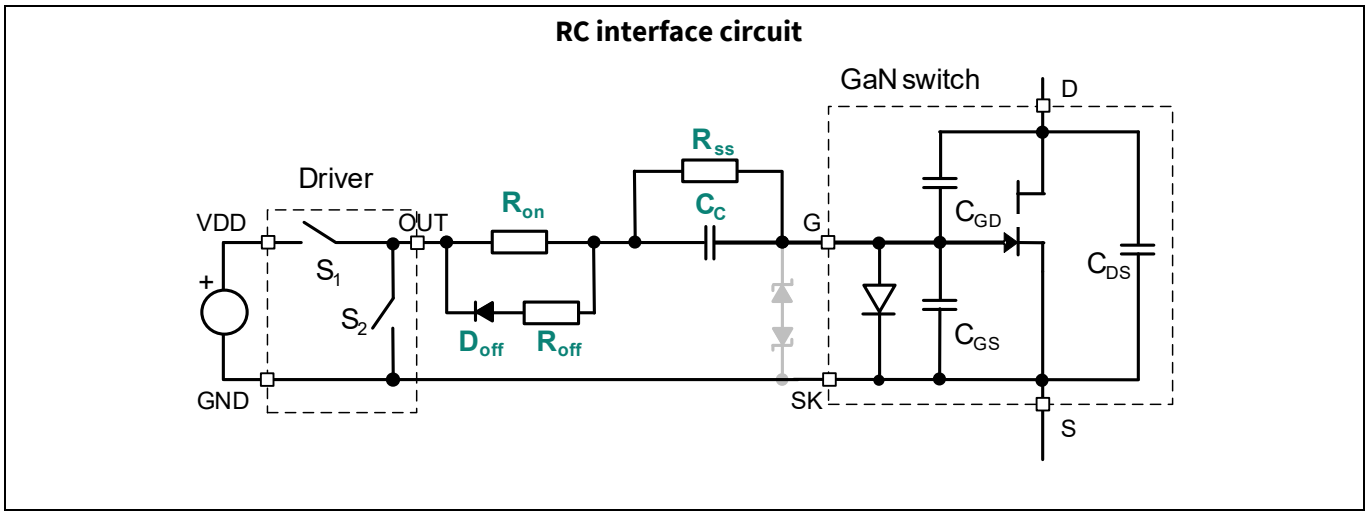

Figure 2 Typical RC interface for Infineon CoolGaN™ Transistor

The following list defines the parameters shown in Figure 2 (Reference: [10]):

- **R_{ss}:** Keeps the steady-state gate current I_{ss}
- **R_{on}, R_{off}:** Transient switching speed dv/dt tuning resistor
- **C_C:** Coupling capacitor as a charge pump to provide fast-switching transient and negative gate bias

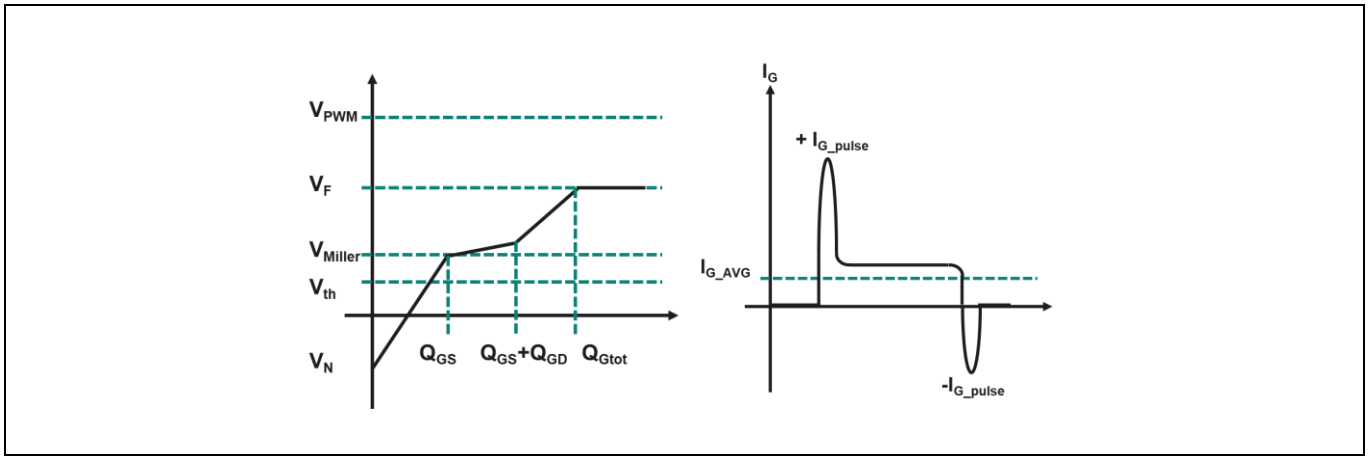

Figure 3 Typical switching waveform for GaN devices

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Miller clamp circuit with RC network

While designing high-speed switching circuits, the Miller clamp is a vital technology that effectively prevents field effect transistors (FET) from unintentionally turning on due to the Miller effect, reducing potential risks in the circuit. This technology is particularly suitable for applications with high switching frequencies or rapid voltage changes, such as SiC or GaN.

By stabilizing the gate voltage, the Miller clamp significantly improves the reliability and robustness of the system, effectively preventing device short circuit, which in turn optimizes the overall efficiency and performance. However, while incorporating a Miller clamp into a design, you must carefully consider various factors, such as circuit parasitics, PCB layout, high-frequency characteristics, and power supply requirements.

However, consider the following limitations to the external Miller clamp circuit design:

- The clamp circuit should be placed as close as possible to the FET's gate to ensure its effectiveness
- The selection of the clamp resistance and PNP BJT is critical
- The resistance value should not be too high, as excessive transient I_{GD} currents may cause the gate voltage, originally pulled low, to be raised again, which weakens the clamp's intended function
- Low V_{CE} (SAT) can make sure it provides enough pull-down capability

This article explores the application of Miller clamp circuits in more complex layouts, particularly in conjunction with GaN devices, providing practical design references to enhance the performance and reliability of high-frequency, high-efficiency circuits.

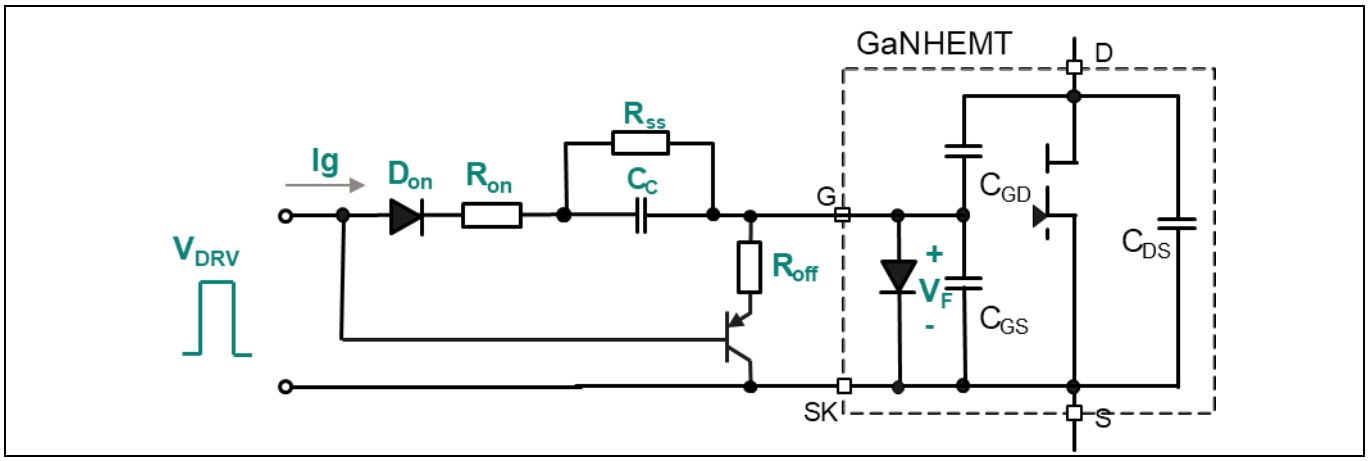

Figure 4 Miller clamp circuit with RC interface for Infineon CoolGaN™ Transistor

The following list defines the parameters shown in Figure 4:

- **R_{ss}:** keep the steady-state gate current I_{ss}
- **R_{on}, R_{off}:** transient switching speed dv/dt tuning resistor
- **C_C :** coupling capacitor as a charge pump to provide fast-switching transient as well as negative gate bias
- **D_{on} :** Separate the turn on and turn off loop

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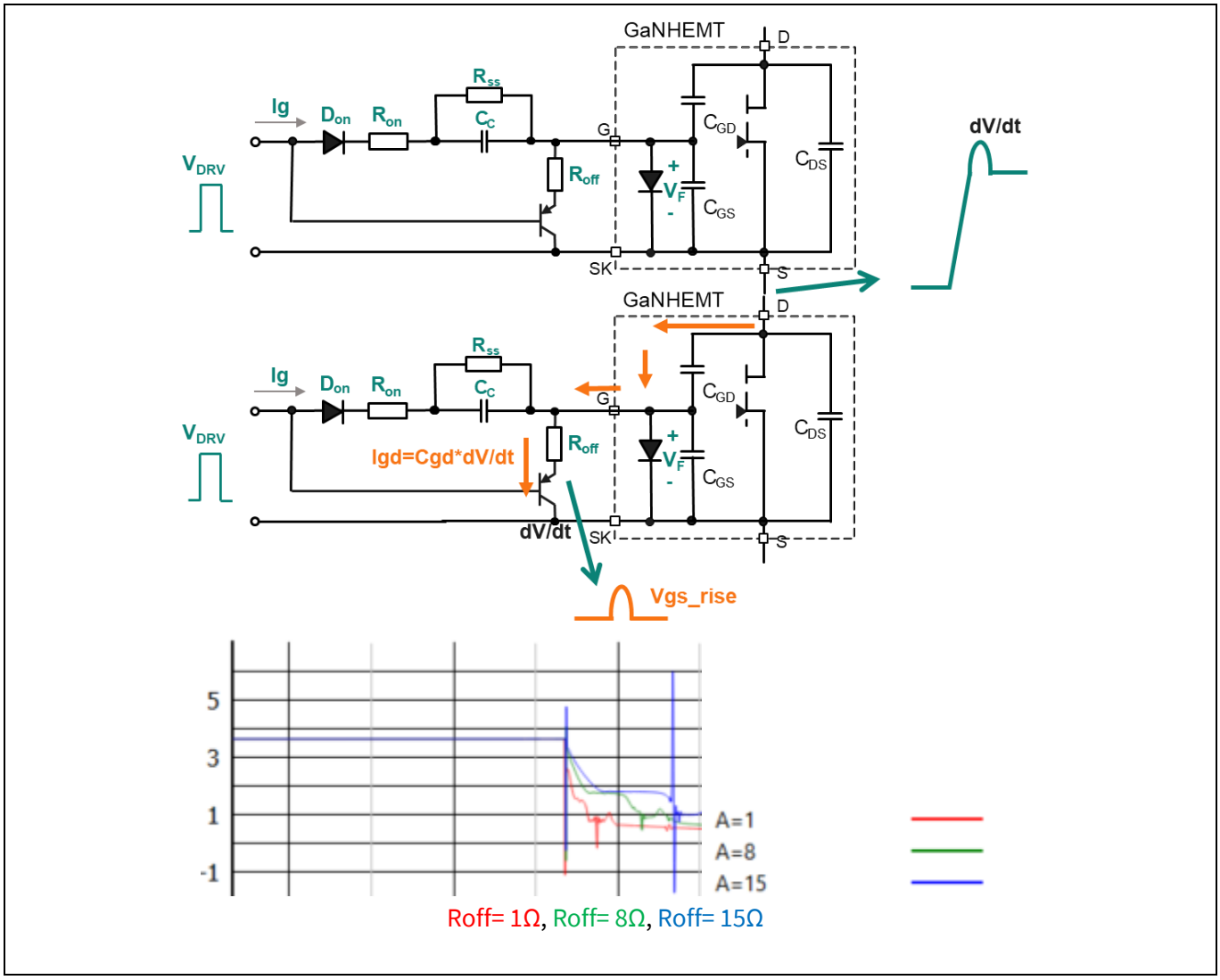


Figure 5 **Miller clamp circuit with RC interface for Infineon CoolGaN™ Transistor**

2 Board description

2.1 Function block and EVB family general description

The half-bridge daughterboard includes different driver solutions:

- **EiceDRIVER™ 1EDB7275F:** a single-channel isolated driver with a bias supply circuit based on EiceDRIVER™ 1EDN7511B, a single-channel non-isolated gate driver IC. This driver solution is optimized to drive high-side or low-side CoolGaN™ devices. It can provide a stable driving capability with a bias supply. For more design details, see KIT_1EDB_AUX_GaN
- **EiceDRIVER™ 2EDB7259Y:** a dual-channel isolated driver with a bootstrap structure for optimizing the layout area and component count. This driver solution combines the RC interface circuit with a miller clamping circuit for reliability improvement.

These boards enable CoolGaN™ devices with only minor modifications in some passive components and can cover the main popular device packages, such as TOLL and DFN 8x8. The functional block of the KIT_HB_ GaN series is shown in Figure 6.

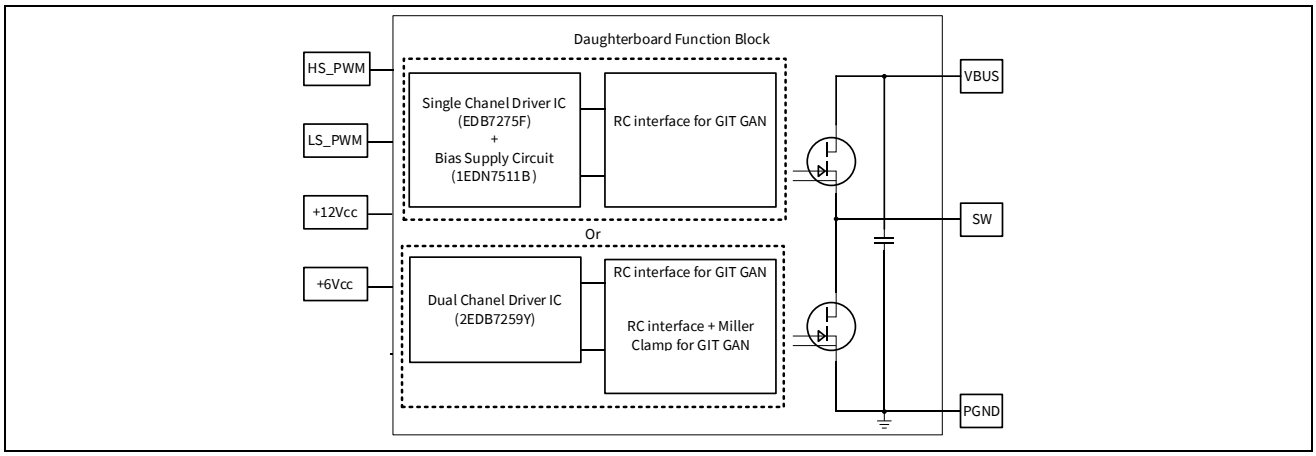


Figure 6 The functional block of the KIT_HB_ GaN series

The complete series is shown in the following table.

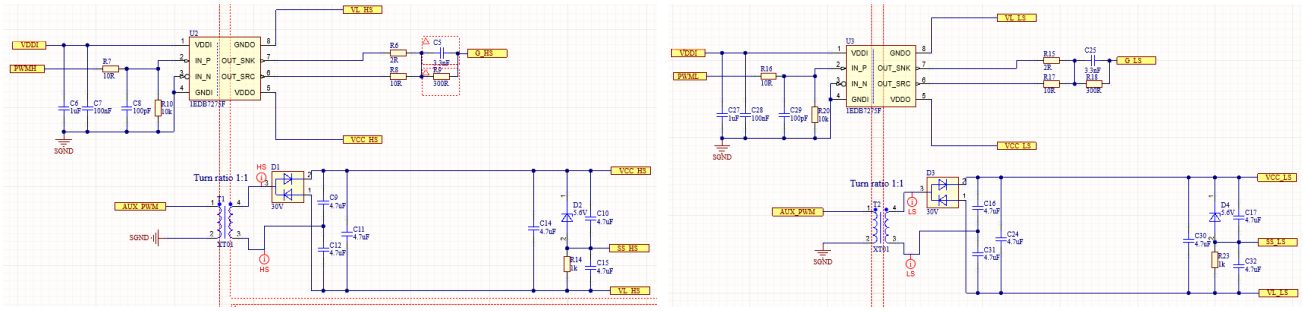
Table 2 KIT_HB_ GaN series item lists

	Series name	Function	Device	Feature
1	KIT_HB_GaN_ISO_TLL_A	1EDB7275 for ISO AUX power	TOLL_IGT65R055D2	RC interface (+4V / -4V)
2	KIT_HB_GaN_ISO_PFN_A	1EDB7275 for ISO AUX power	DFN 8x8_ IGLD65R055D2	RC interface (+4V / -4V)
3	KIT_HB_GaN_BT_RC_TLL_A	2EDB7259Y for Bootstrap Driver	TOLL_IGT65R055D2	RC interface (+4V / -4V)
4	KIT_HB_GaN_BT_RC_PFN_A	2EDB7259Y for Bootstrap Driver	DFN 8x8_ IGLD65R055D2	RC interface (+4V / -4V)
5	KIT_HB_GaN_BT_ML_TLL_A	2EDB7259Y for Bootstrap Driver	TOLL_IGT65R055D2	Miller Clamp (+4V / 0V)
6	KIT_HB_GaN_BT_ML_PFN_A	2EDB7259Y for Bootstrap Driver	DFN 8x8_ IGLD65R055D2	Miller Clamp (+4V / 0V)

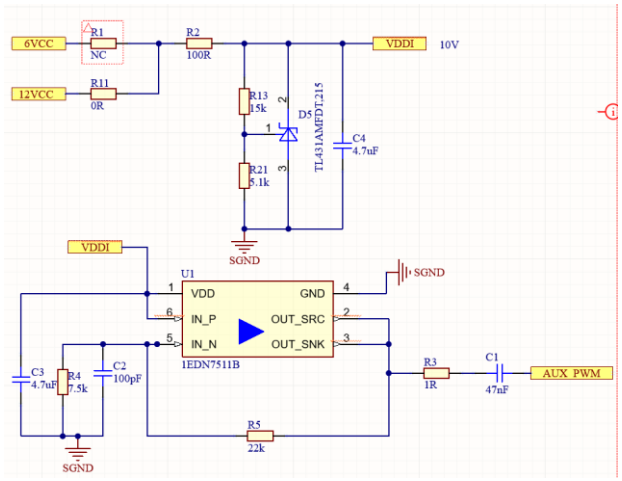
2.2 Schematic overview

The various schematics of the **KIT_HB_ GaN** series are shown in Figure 7.

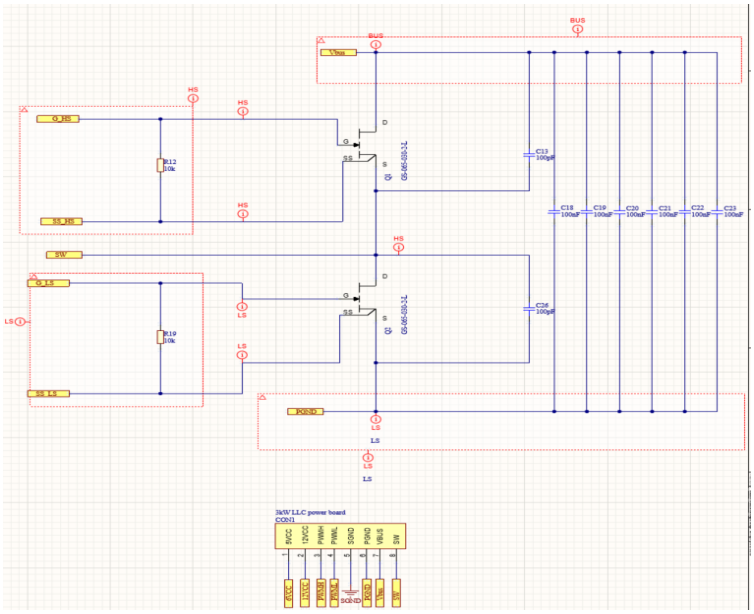
1. Single-channel isolated driver with a bias supply circuit



1.a. High-side and low-side driver circuit



1.b. Bias supply circuit



1.c. Power loop circuit

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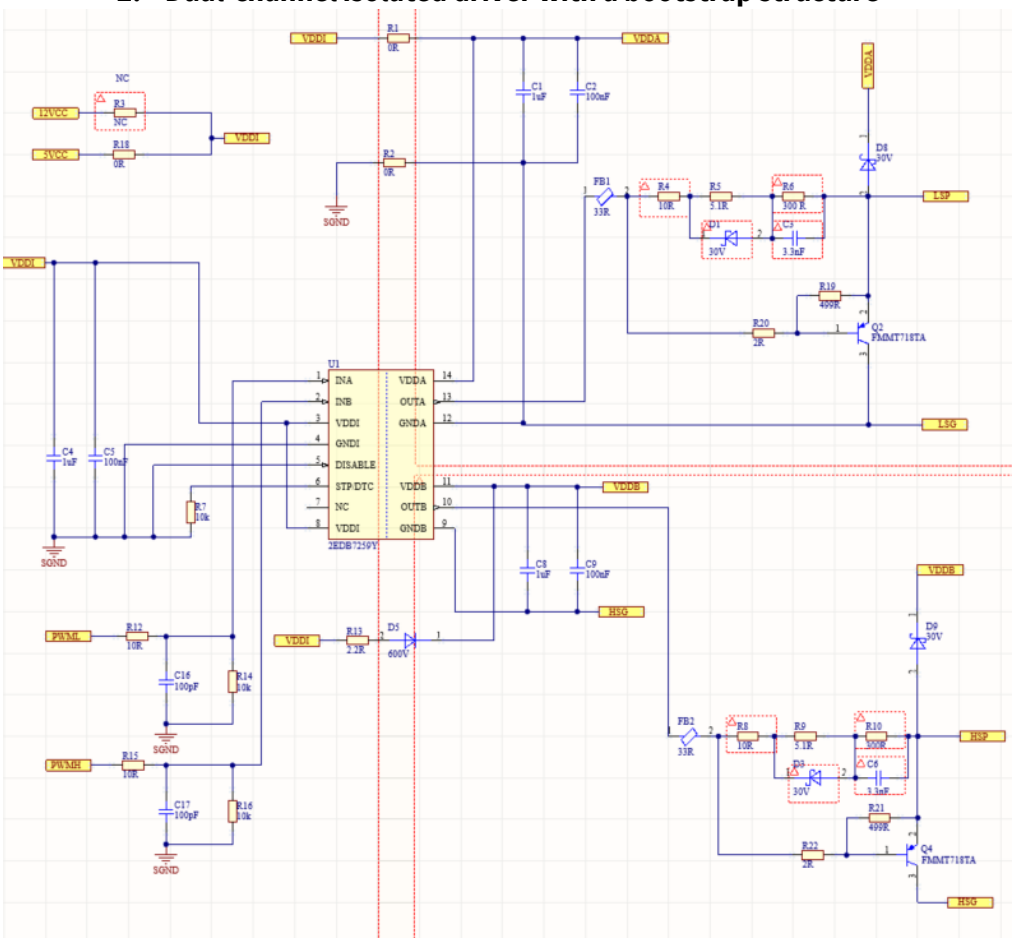
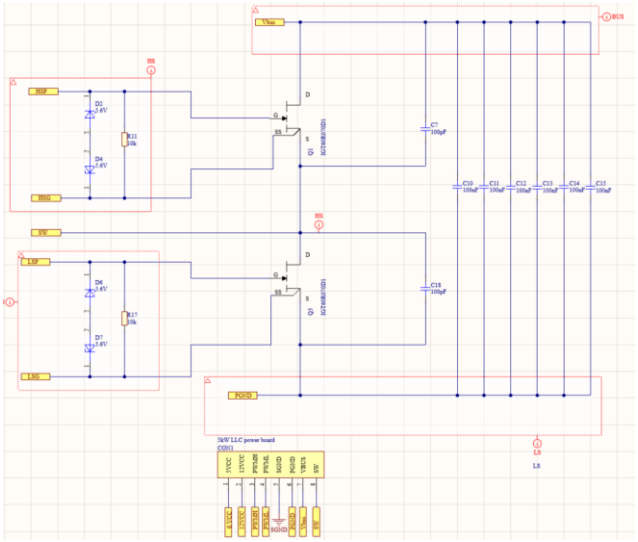
2. Dual-channel isolated driver with a bootstrap structure



2.a. Bootstrap driver circuit



2.b. Power loop circuit

Figure 7 KIT_HB_ GaN series schematics: Single-channel isolated driver with a bias supply circuit (1) and Dual-channel isolated driver with a bootstrap structure (2)

The board design is considered compatible with CoolGaN™ devices and with different driving solutions, so the modification table is as follows.

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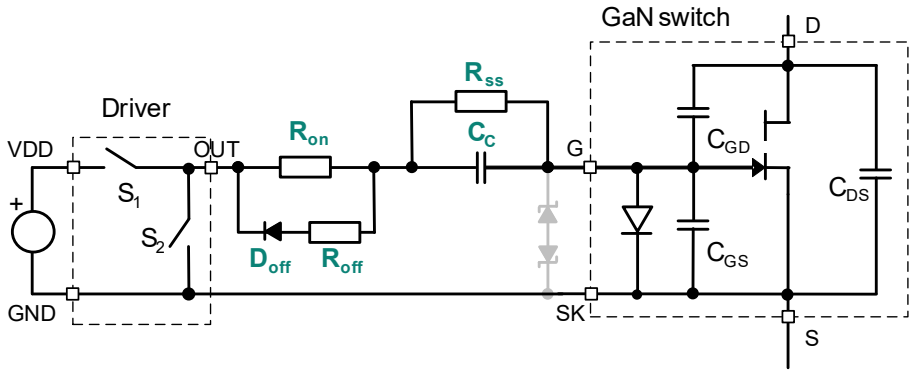
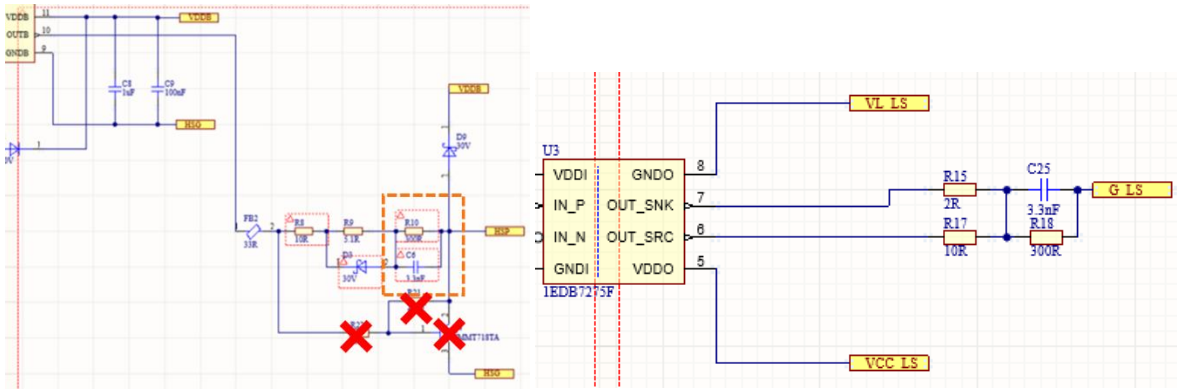
Table 3 Modifications for daughterboard configurations

Configuration	VCC	Turn on (V)/off (V)			
KIT_HB_GaN_ISO_TLL_A KIT_HB_GaN_ISO_PFN_A	12 V	Vgs (+4/-3)	R1 NC	R11 0 Ω	RC network 3.3 nF / 300 Ω
KIT_HB_GaN_BT_RC_TLL_A KIT_HB_GaN_BT_RC_PFN_A	12 V	Vgs (+4/-6)	Q2/Q4 / R1 / R19/ R20/R21/R22 NC	R11 0 Ω	RC network 3.3 nF / 300 Ω
KIT_HB_GaN_BT_ML_TLL_A KIT_HB_GaN_BT_ML_PFN_A	6 V	Vgs (+4/0)	R3/R5/R9 NC	R18 0 Ω	D1/D3 Opposite the Diode's direction RC network 3.3 nF/300 Ω

The following figure shows the various driver circuits and schematics for KIT_HB_ GaN devices.

(a)





(b)

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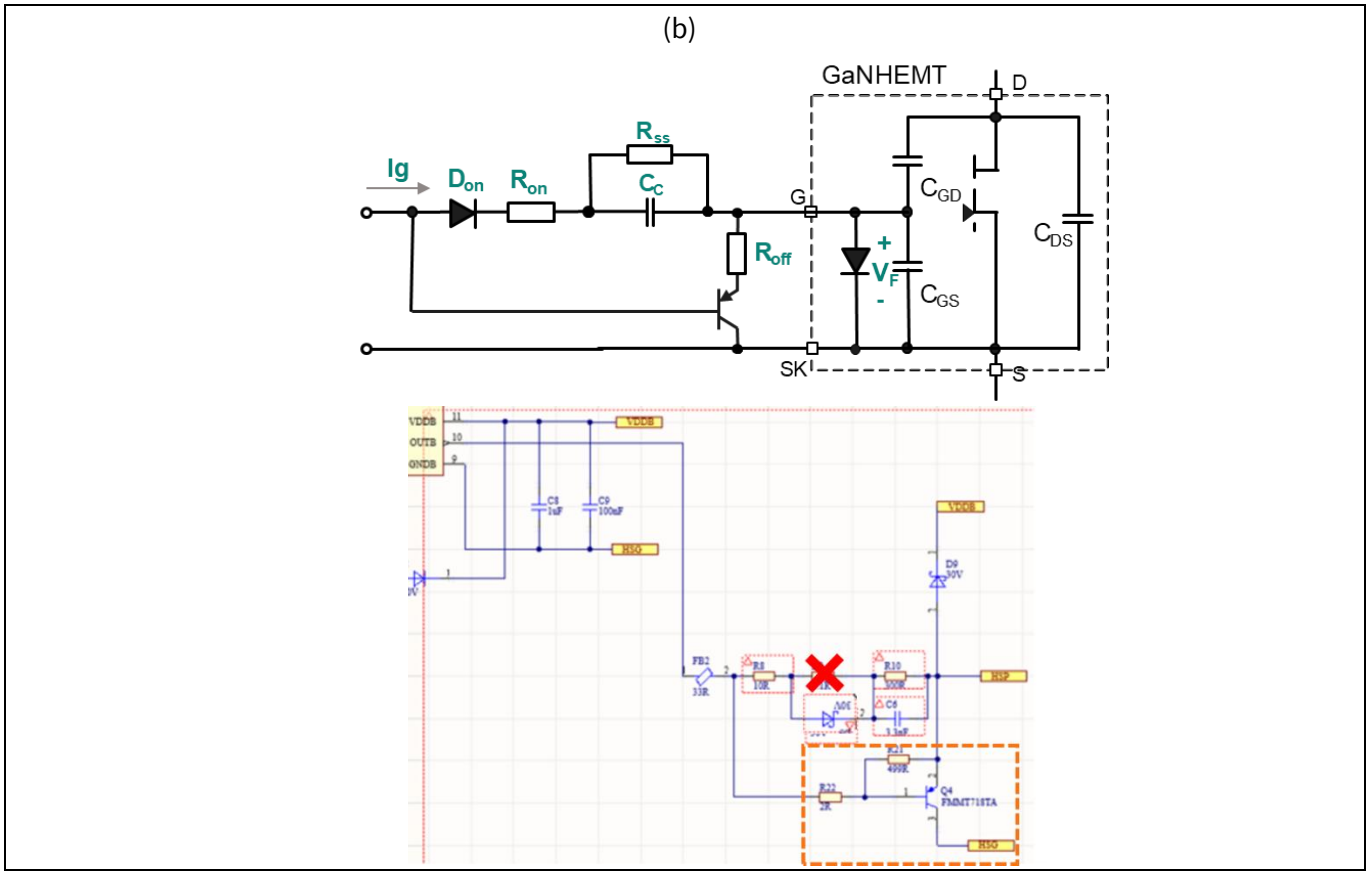

Figure 8 Driver circuits and schematics for KIT_HB_ GaN: RC interface for GIT GaN switch (a), and Miller clamp for GIT GaN switch (b)

2.3 Layout overview

The evaluation board is 1.6 mm thick, with four evenly spaced 2 oz thick copper layers. The layer stack-up is depicted below.

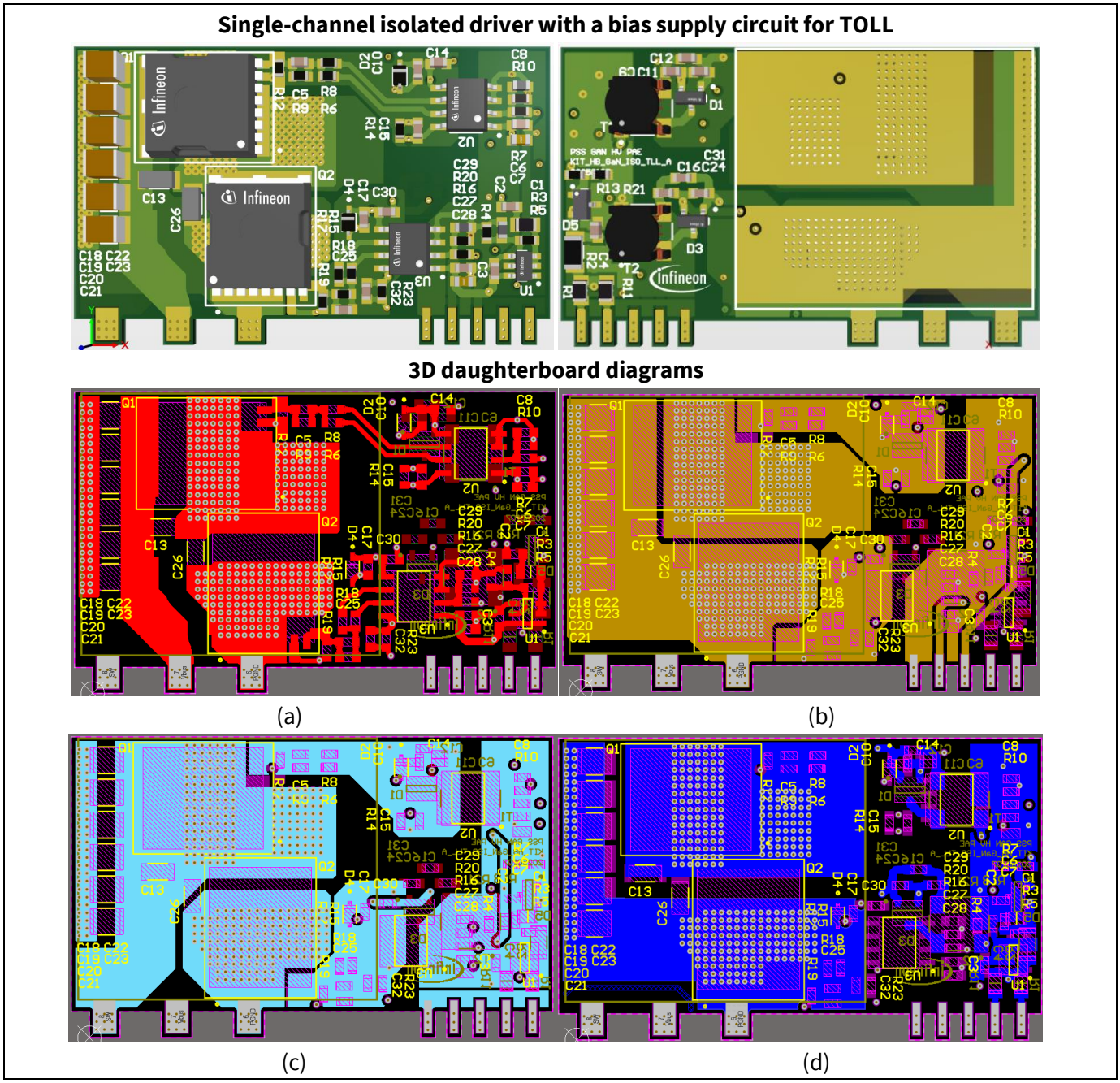

Figure 9 Single-channel isolated driver with a bias supply circuit for TOLL, showing 3D daughterboard diagrams (top image) and the various PCB layers

Figure 9 shows the layout of KIT_HB_GaN_ISO_TLL_A of the KIT_HB_ GaN series evaluation boards:

top layer (a), mid layer 1 (b), mid layer 2 (c), and bottom layer (d).

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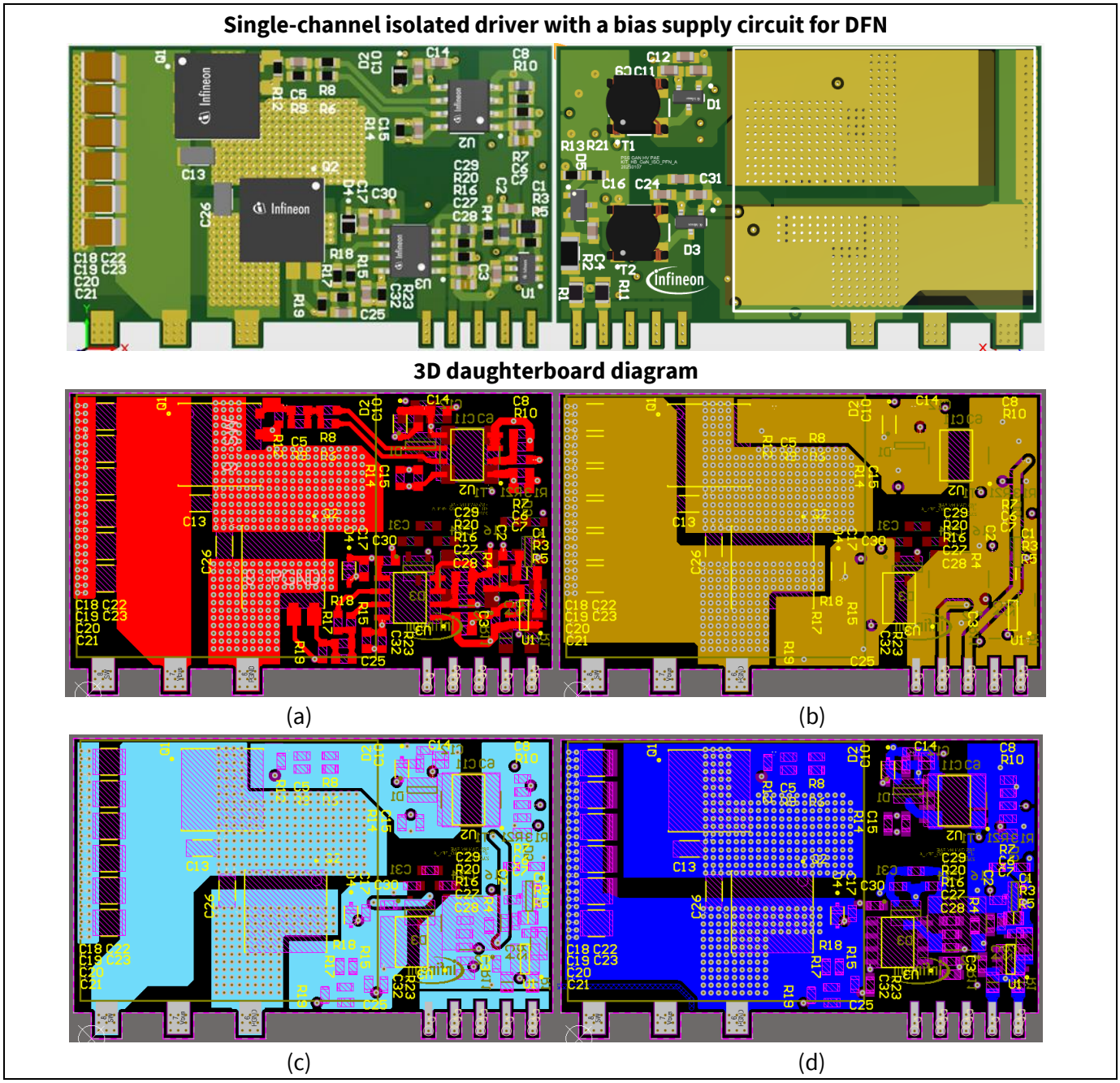

Figure 10 **Single-channel isolated driver with a bias supply circuit for DFN 8x8, showing 3D daughterboard diagrams (top image) and the various PCB layers**

Figure 10 shows the layout of KIT_HB_GaN_ISO_PFN_A of the KIT_HB_ GaN series evaluation boards: top layer (a), mid layer 1 (b), mid layer 2 (c), and bottom layer (d).

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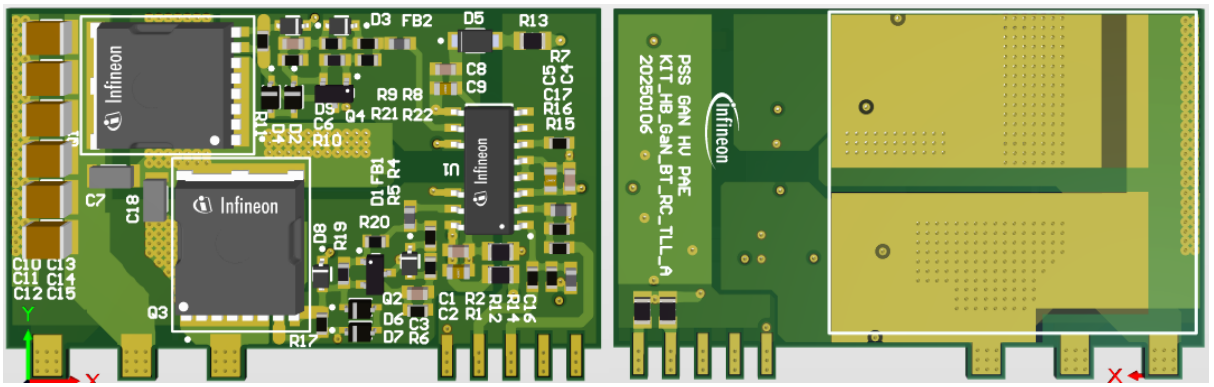
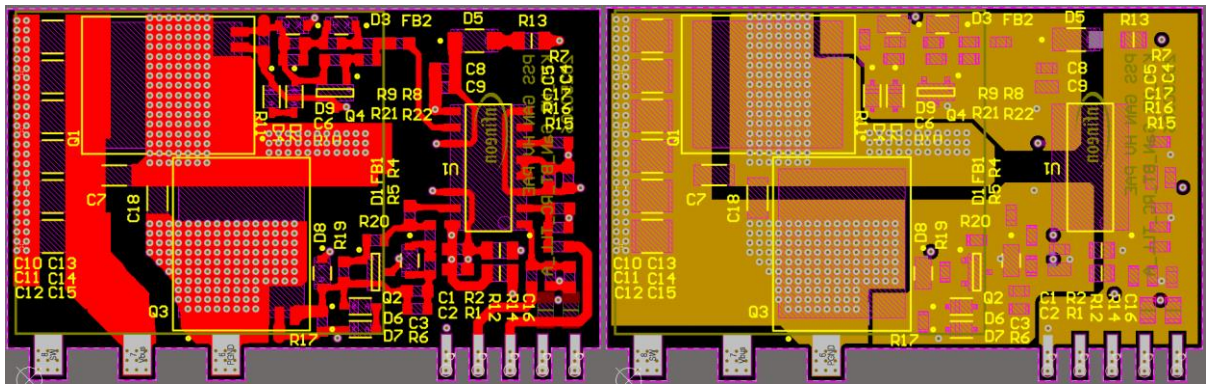
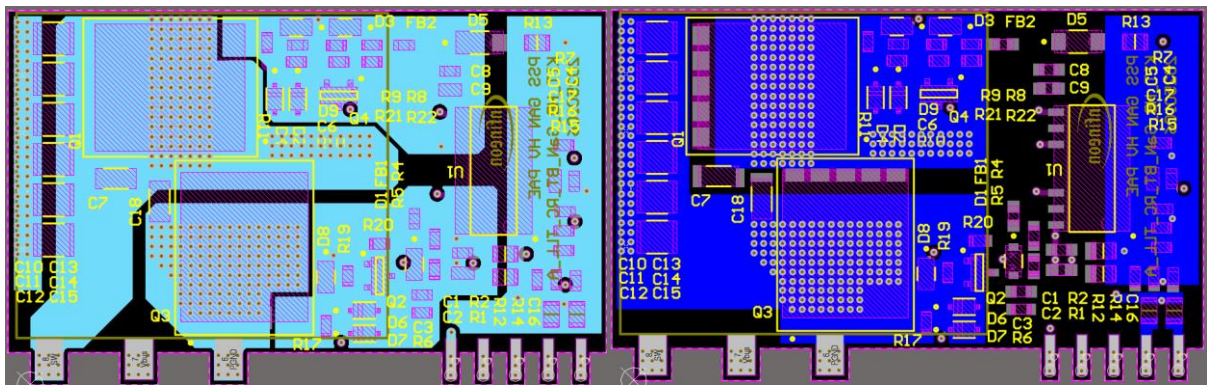
Dual-channel isolated driver with a bootstrap structure for TOLL



3D daughterboard diagram



(a) (b)



(c) (d)

Figure 11 Dual-channel isolated driver with a bootstrap structure for TOLL, showing 3D daughterboard diagrams (top image) and the various PCB layers

Figure 11 shows the layout of KIT_HB_GaN_BT_RC_TLL_A, KIT_HB_GaN_BT_ML_TLL_A of the KIT_HB_ GaN series of evaluation boards: top layer (a), mid layer 1 (b), mid layer 2 (c), and bottom layer (d).

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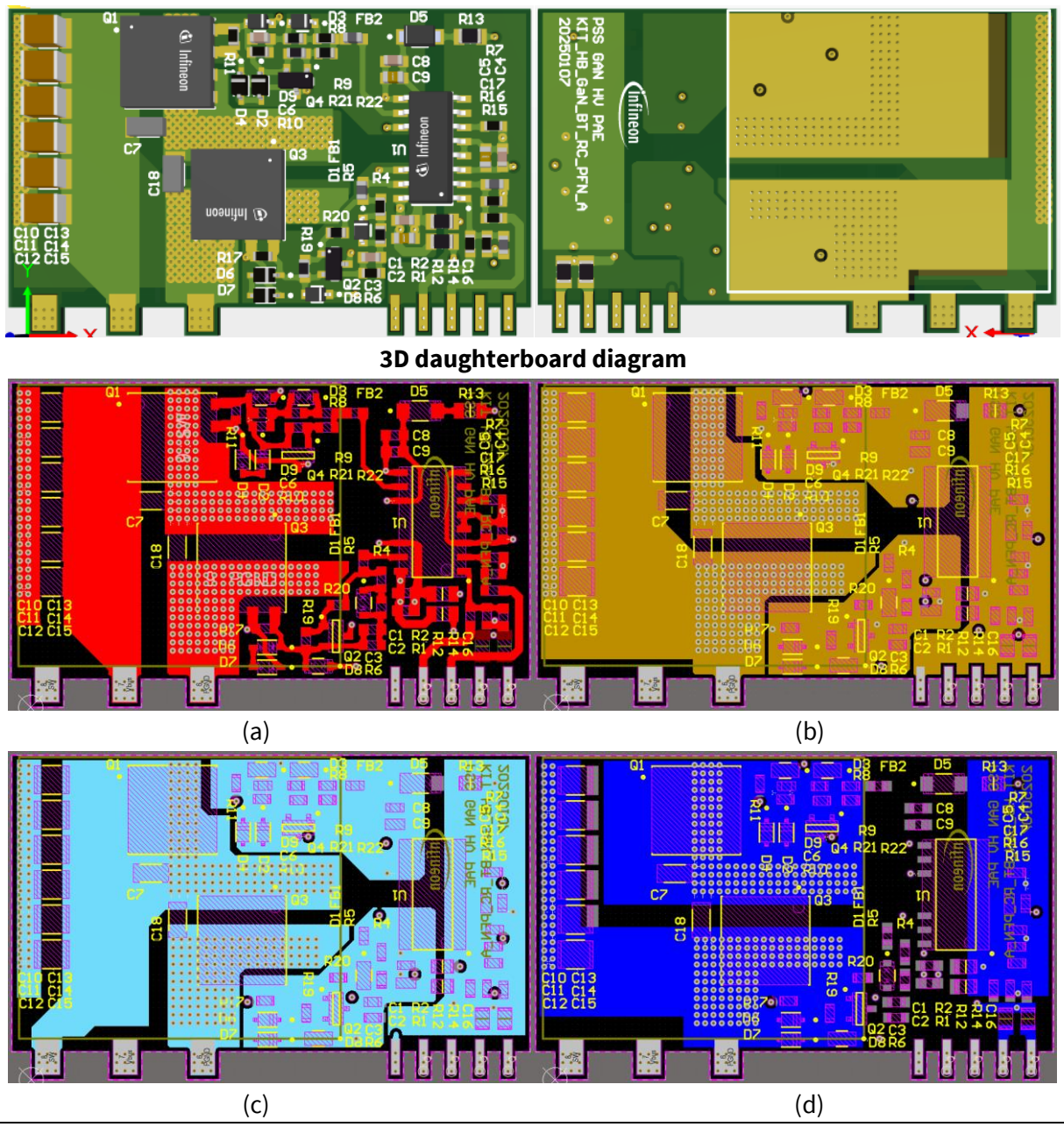

Figure 12 **Dual-channel isolated driver with a bootstrap structure for DFN 8x8, showing 3D daughterboard diagrams (top image) and the various PCB layers**

Figure 12 shows the layout of KIT_HB_GaN_BT_RC_PFN_A, KIT_HB_GaN_BT_ML_PFN_A of the KIT_HB_ GaN series of evaluation boards: top layer (a), mid layer 1 (b), mid layer 2 (c), and bottom layer (d).

2.4 Measurement suggestion

A long ground wire introduces unwanted inductance into the probe measurement path. This results in overshoot and ringing – associated with the rising and falling edges of the signals. Minimizing the length of the ground loop is especially important for CoolGaN™ devices– which has very fast rise and fall times – affected by the probe's ground inductance. Following are some examples of measurement setups:

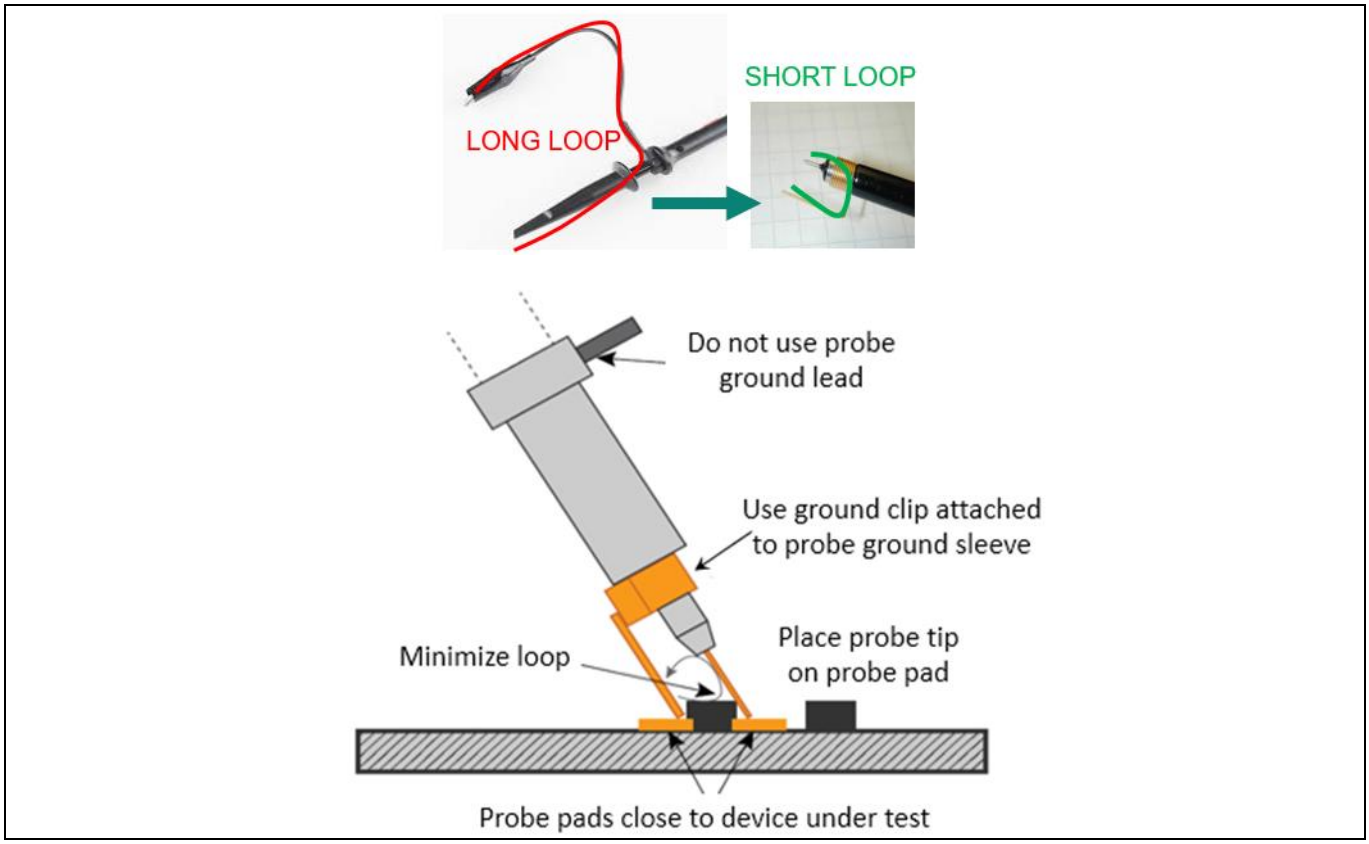

Figure 13 Examples of the scope probe with a short ground clip

3 Measurement results

3.1 Double pulse test with the daughterboard

For proper setup and connections for double pulse testing, provide 6 V or 12 V DC supply connections. The inductor also connects to the terminal block (Vdc+ and Vsw). It is recommend to use the air core for the inductor, as it can handle high pulse current without being saturated. No load is required for pulse testing – the inductor energy is dissipated in the freewheeling transistor.

Test conditions:

- Vdc+ = 400 V
- ID = 30 A (IGT65R055D2)
- V_{GS} = Depends on the driver solution (4 V/-3 V.)
- L = 400 uH (without RC snubber)
- T_J = 25 °C

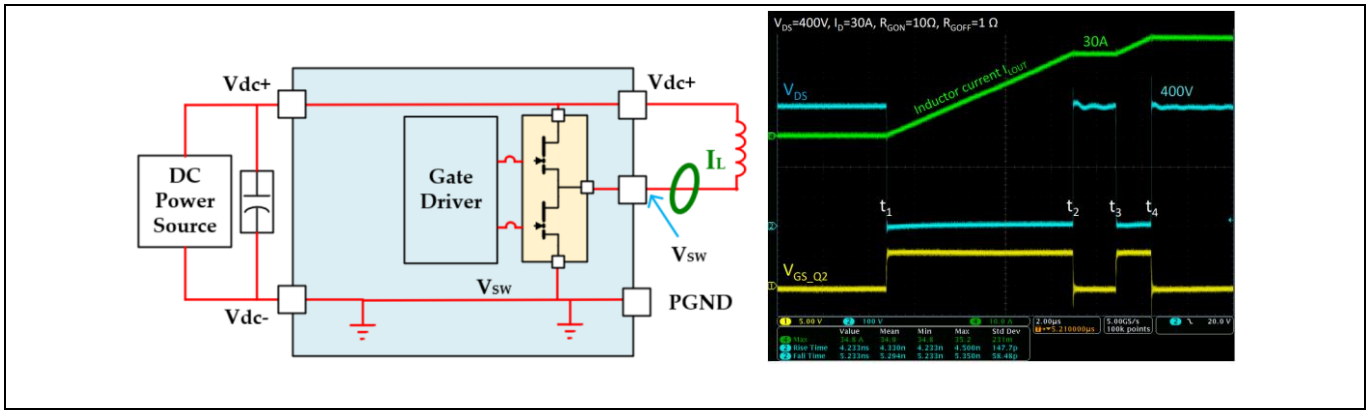

Figure 14 Double pulse function block and test waveform

This example shows how to set the board up for double pulse testing. In the first zone(t1~t2), a GaN transistor turns on and ramps up the inductor current to a test value. This GaN transistor then turns off and the current freewheels through the other GaN transistor, which acts as a synchronous rectifier. The second pulse(t3~t4), shows hard-switched turn-on performance on the leading edge (at the test current) and continues the ramp to a higher current level.

GaN devices perform particularly well on these tests because the freewheeling diode has zero reverse recovery characteristics. Double pulse testing is typically done one burst at a time (not continuously) to keep power dissipation low, even while testing the voltage and current limits of the device.

CoolGaN™ Transistor in TOLL package is used to demonstrate some of the driving solutions as below.

Table 4 lists the oscilloscope channels for Figure 15, Figure 16, and Figure 17.

Table 4 Description of oscilloscope channels

Channel	Description
CH 1 (blue)	Low-side GaN gate-to-source signal, 2 V/div
CH 2 (cyan)	Low-side GaN drain-to-source signal, 100 V/div
Ch 4 (green)	Inductor current, 10 A/div

3.1.1 CoolGaN™ Transistor with single-channel isolated driver IC and isolated standby aux power circuit

Measured peak V_{DS} = 552 V, V_{GS} = 4.96 V. Reliable hard-switching with IGT65R055D2 is achieved at full-rated current.

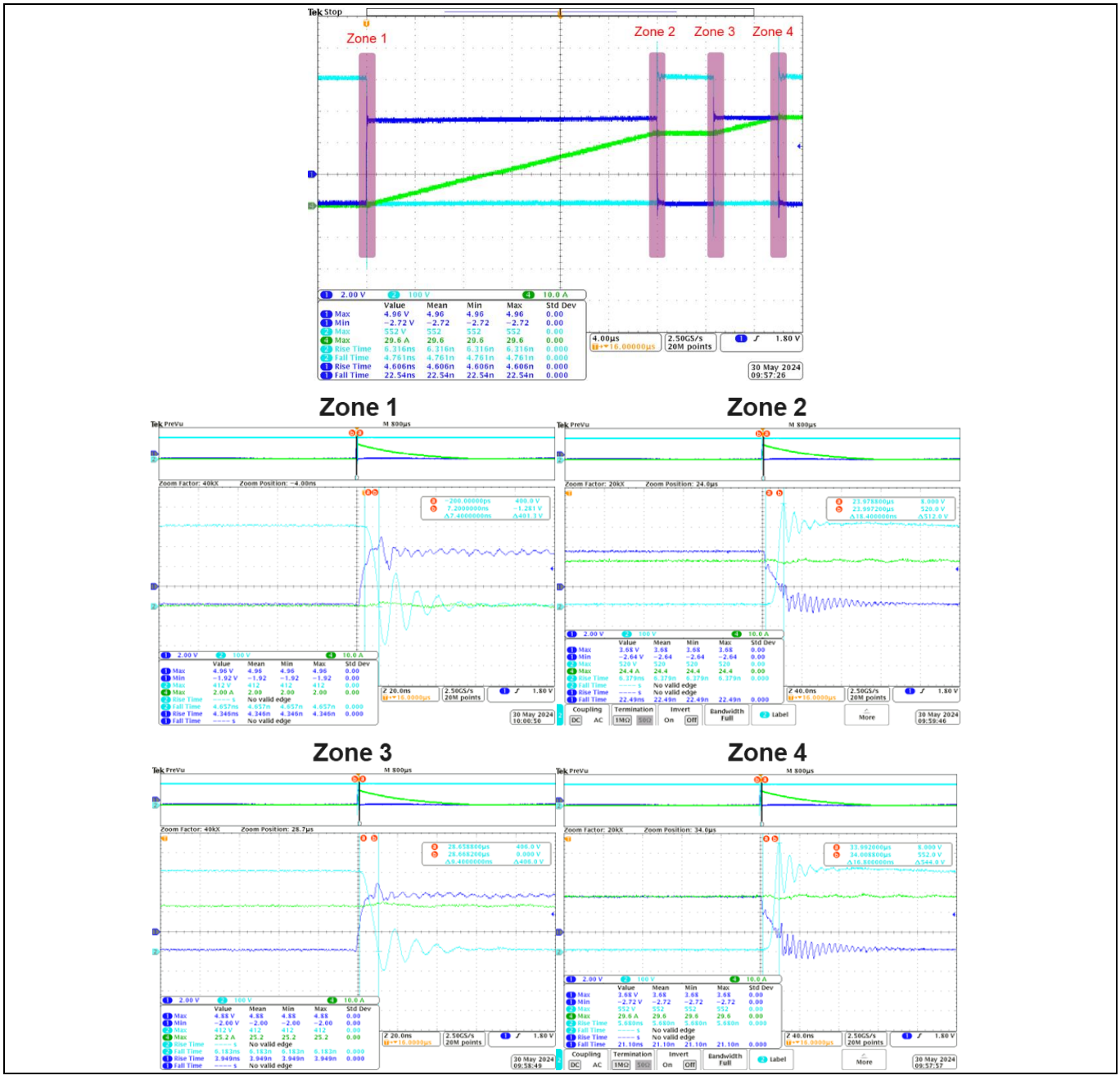

Figure 15 Double-pulse test waveform with single-channel isolated driver IC and isolated standby aux power circuit (IGT65R055D2)

3.1.2 CoolGaN™ Transistor with dual-channel isolated driver and miller clamp circuit

Measured peak V_{DS} = 564 V, V_{GS} = 3.6 V. Reliable hard-switching with IGT65R055D2 is achieved at full-rated current.

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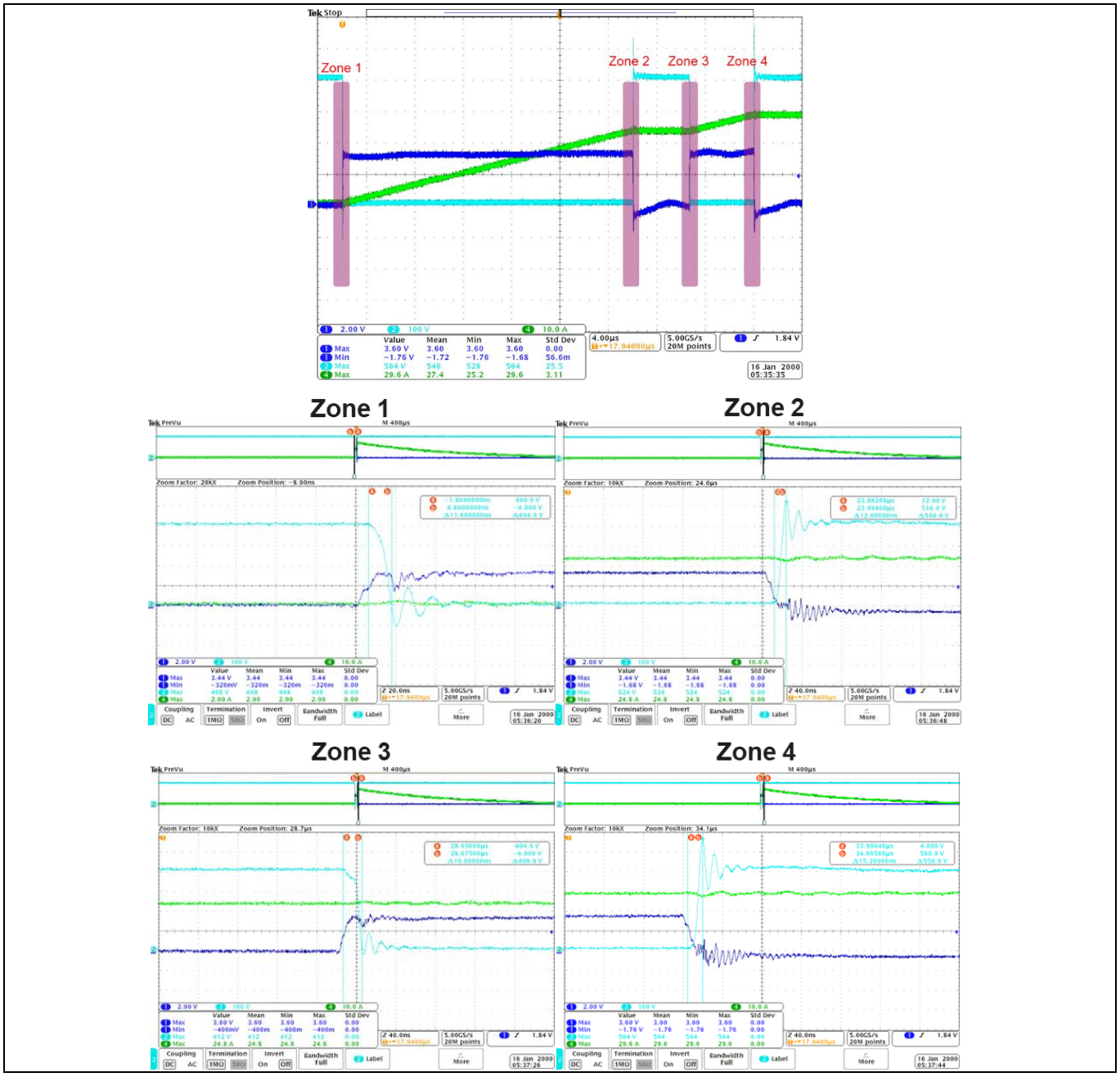

Figure 16 **Double pulse test waveform with dual-channel isolated driver and Miller clamp circuit (IGT65R055D2)**

3.1.3 CoolGaN™ Transistor with dual-channel isolated driver and RC interface circuit

Measured peak V_{DS} = 552 V, V_{GS} = 5.44 V. Reliable hard-switching with IGT65R055D2 is achieved at full-rated current.

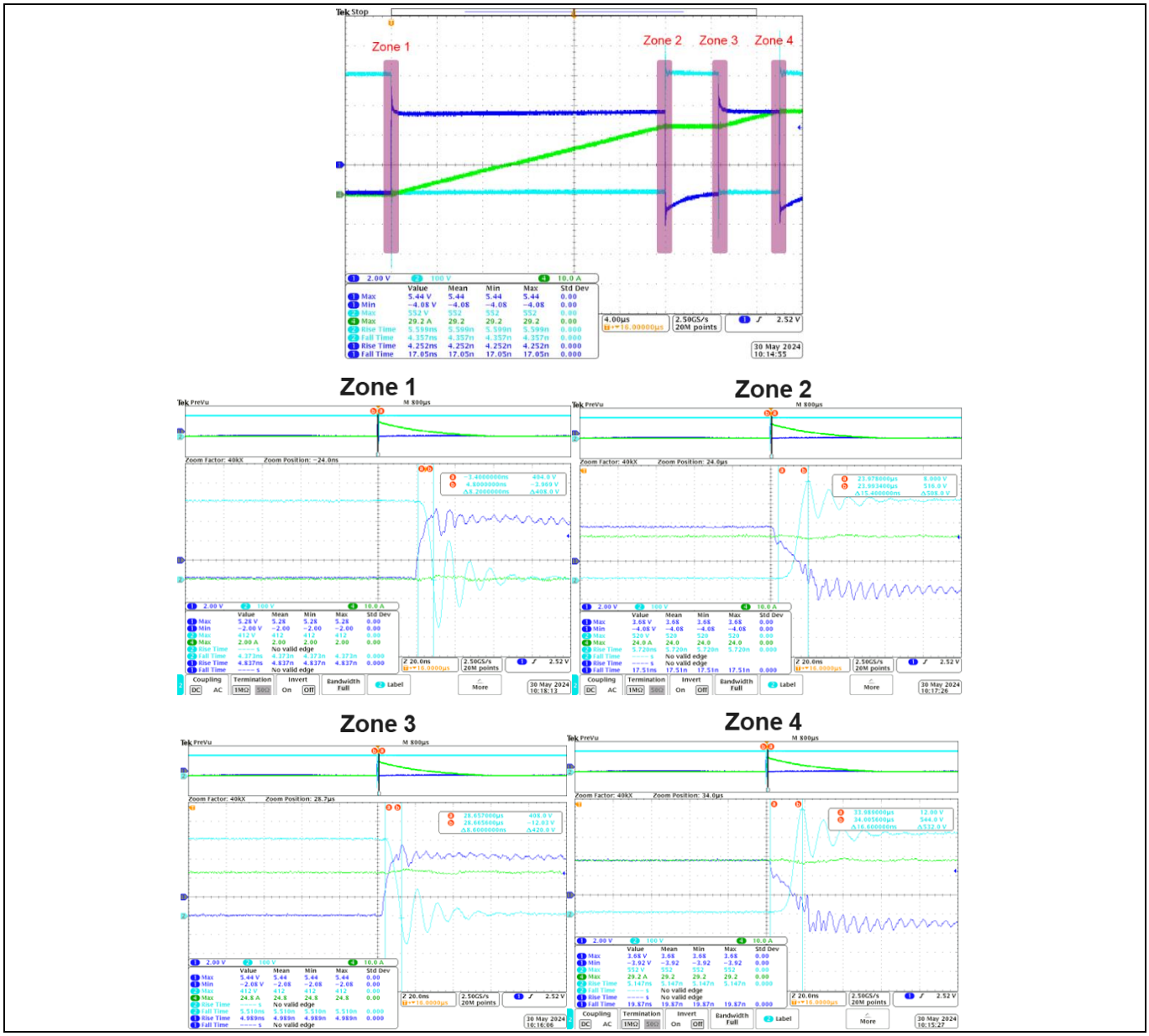

Figure 17 Double pulse test waveform with dual-channel isolated driver and RC interface circuit (IGT65R055D2)

4 Summary

These daughterboard series are high voltage, high power density, and drop into any half-bridge topology easily. There are several application environments are show as follows. Just choose a suitable package and the driver circuit needed. This allows for the validation of CoolGaN™ performance with minimal modifications and enables a more efficient evaluation of the extent to which CoolGaN™ improves the system. For more information, you can refer to the Power system topology selection.

Table 5 Topologies overview

Application	AC / DC	DC/DC	DC/AC
Industrial SMPS	– Totem Pole PFC	– HB / FB LLC – PS FB	-
DC EV Charging	– B6 – ANPC	– HB / FB LLC – DAB – CLLC – Buck-boost	-
Home applications / Solar		– DAB – CLLC	– B6 – Heric – Cyclo converter – PS FB + H4

References

Contact Infineon support to obtain the documents.

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Revision history

Document revision	Date	Description of changes
V 1.0	2026-05	Initial release

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