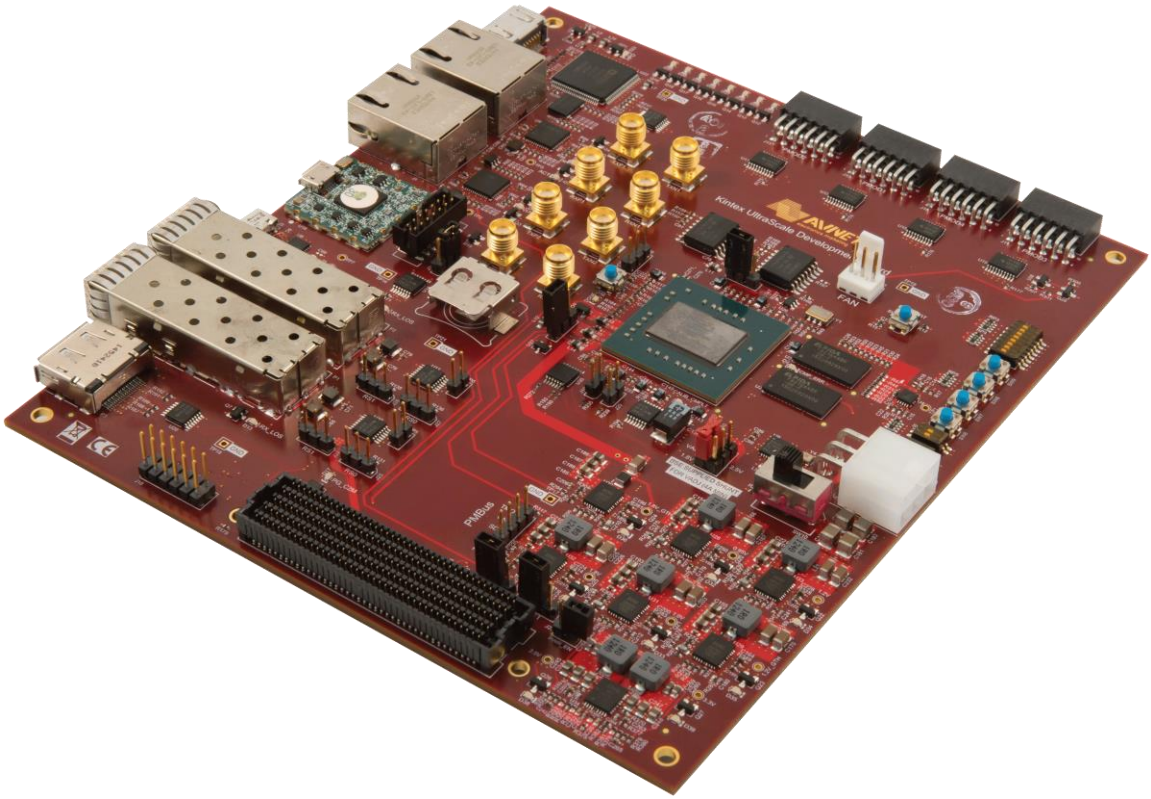
Kintex UltraScale
KU040 Development Board



Hardware User Guide

Version 1.0
12/17/2015

Table of Contents

1 INTRODUCTION 2

1.1 ORDERING INFORMATION 2
1.2 REFERENCE DESIGNS 2

2 FUNCTIONAL DESCRIPTION 3

2.1 XCKU040-1FBVA676 BANK PIN ASSIGNMENTS 4
2.2 BOARD I/O COUNT 5
2.3 250MHZ SYSTEM CLOCK INPUT 6
2.4 USB-UART PORT 6
2.5 CONFIGURATION QSPI INTERFACE 7
2.6 USER CODE/DATA QSPI INTERFACE 8
2.7 PROGRAMMABLE LVDS CLOCK SOURCE 9
2.8 GTH INTERFACES 10
2.8.1 GTH Reference Clocks 11
2.8.2 SFP+ Interfaces 11
2.8.3 SMA Interfaces 13
2.8.4 FMC HPC GTH Interfaces 13
2.9 LVDS TOUCH PANEL INTERFACE 15
2.9.1 XCKU040 Device Package Delay Compensation 16
2.10 HDMI INTERFACE 16
2.10.1 XCKU040 Device Package Delay Compensation 18
2.11 FMC HPC LA INTERFACE 18
2.11.1 XCKU040 Device Package Delay Compensation 21
2.12 DDR4 SDRAM INTERFACE 21
2.12.1 DDR4 VREF and VTT Generation 23
2.12.2 XCKU040 Device Package Delay Compensation 24
2.13 10/100/1000 ETHERNET PHY INTERFACES 24
2.13.1 10/100/1000 Ethernet PHY Strapping Resistors 27
2.13.2 Ethernet PHY LEDs 28
2.13.3 XCKU040 Device Package Delay Compensation 28
2.14 PMOD™-COMPATIBLE INTERFACES 28
2.15 DIP SWITCHES AND PUSH BUTTONS 29
2.16 USER LEDS 30
2.17 SYSTEM MONITOR (SYSMON) HEADER 30
2.18 BOARD JTAG CHAIN 31
2.19 BOARD POWER SUPPLY 32
2.19.1 Power Input – J21 and SW10 34
2.19.2 VADJ Selection 34
2.20 THERMAL MANAGEMENT 35

3 MECHANICAL 36

3.1 MECHANICAL DIMENSIONS 36

4 REVISION HISTORY 38

1 Introduction

The Kintex UltraScale Development Board is designed to be a development platform in a small form factor. The features provided by the Kintex UltraScale Development Board consist of:

- Xilinx XCKU040-1FBVA676 FPGA
- Memory
  - 1GB DDR4 SDRAM (x32 @ 1600Mbps)
  - 64MB of Configuration QSPI Flash (single QSPI x4)
  - 64MB of User Code/Data QSPI Flash (single QSPI x4)
- Interfaces
  - Two SFP+ Sockets (up to 12.5Gbps)
  - Two GTH SMA Interfaces (up to 11.25Gbps)
  - Two 10/100/1000 Ethernet Interfaces (RGMII)
  - HDMI Interface
  - LVDS Touch Panel Interface
  - FMC HPC Slot (VADJ of 1.8V, 2.5V, 3.3V) with 8 GTH lanes (up to 12.5Gbps)
  - Four Single Ended Pmod™-Compatible Sockets
  - USB-UART Interface
  - 8 User LEDs
  - 5 User Push Button Switches
  - 8 User Slide Dip Switches
  - Analog SYSMON Interface
- On-Board Clocks
  - Programmable LVDS Clock Source (GTH Reference Clock)
  - 250 MHz LVDS Oscillator (System Clock)
- Programming Interfaces
  - JTAG Programming Header
  - Digilent USB-JTAG Module (JTAG-SMT2)
- Power
  - International Rectifier IR38060 – Synchronous Buck Regulator with PMBus
  - International Rectifier IR3892 – SupIRBuck Synchronous Buck Regulator

1.1 Ordering Information

The following table lists the Kintex UltraScale Development Board orderable part number. For more information on the Kintex UltraScale Development Board please visit the website at http://www.em.avnet.com/ku040-dev.

Part Number	Hardware
AES-KU040-DB-G	• Xilinx Kintex UltraScale Development Board populated with a XCKU040 FBVA676 -1 Speed Grade device. • Kit includes 12V Power Supply and a Thermal Solution

1.2 Reference Designs

Reference designs that demonstrate some of the potential applications of the Kintex UltraScale Development Board can be downloaded from http://www.em.avnet.com/ku040-dev. The reference designs include all of the source code and project files necessary to implement the designs. See the PDF document included with each reference design for a complete description of the design and detailed instructions for running a demonstration on the development board. Check the DRC periodically for updates and new designs.

2 Functional Description

The Kintex UltraScale Development Board is designed to be utilized as a general-purpose hardware platform. It is a custom-built evaluation kit destined for professionals to be used at research and development facilities for such purposes. The Kintex UltraScale Development Board supports prototyping efforts in the following areas:

- Video applications using on-board HDMI and LVDS Touch Panel interfaces
- Networking applications using on-board Ethernet ports and SFP+ interfaces
- Analog interface using the SYSMON header
- General-purpose high-speed transceiver prototyping using the GTH SMA connectors
- Inclusion of application specific modules using the FMC and Pmod™-Compatible expansion slots

A high-level block diagram of the Kintex UltraScale Development board is shown below.

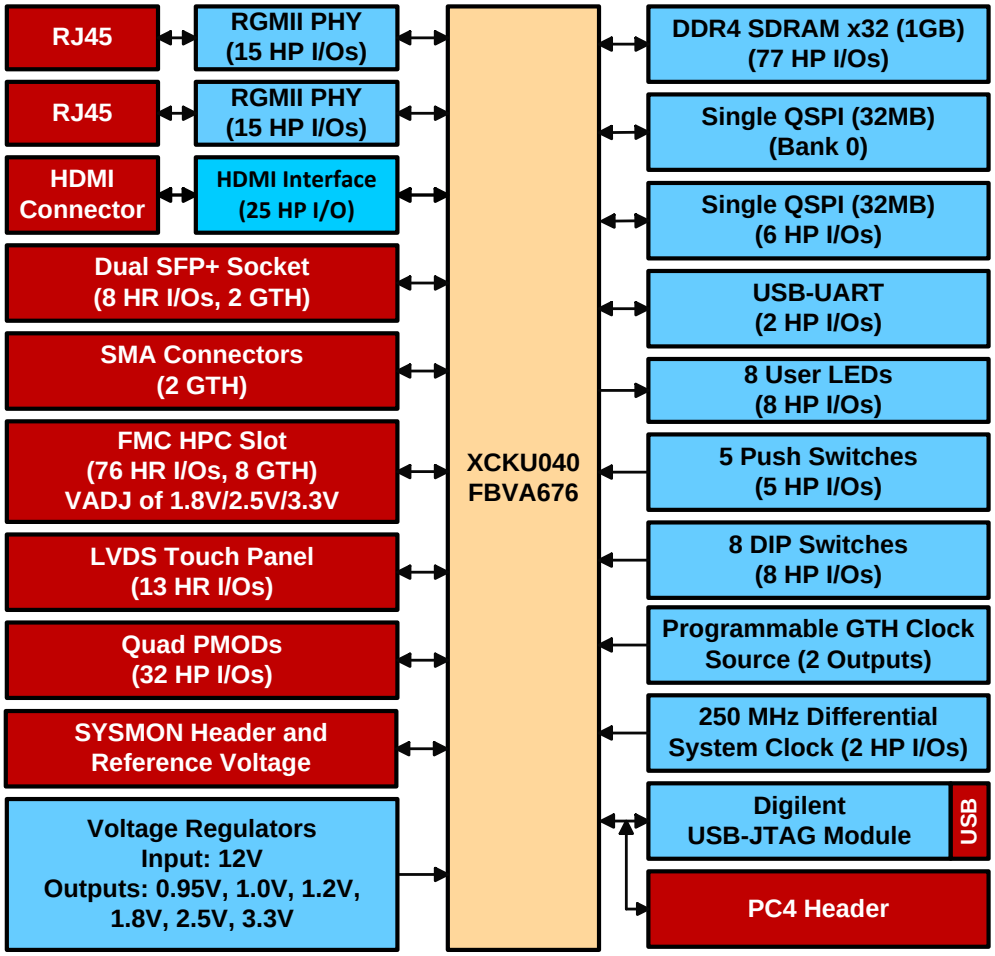


Figure 1 – Kintex UltraScale Development Board Block Diagram

The following figure depicts the physical locations of the various interfaces contained on the Kintex UltraScale Development board.

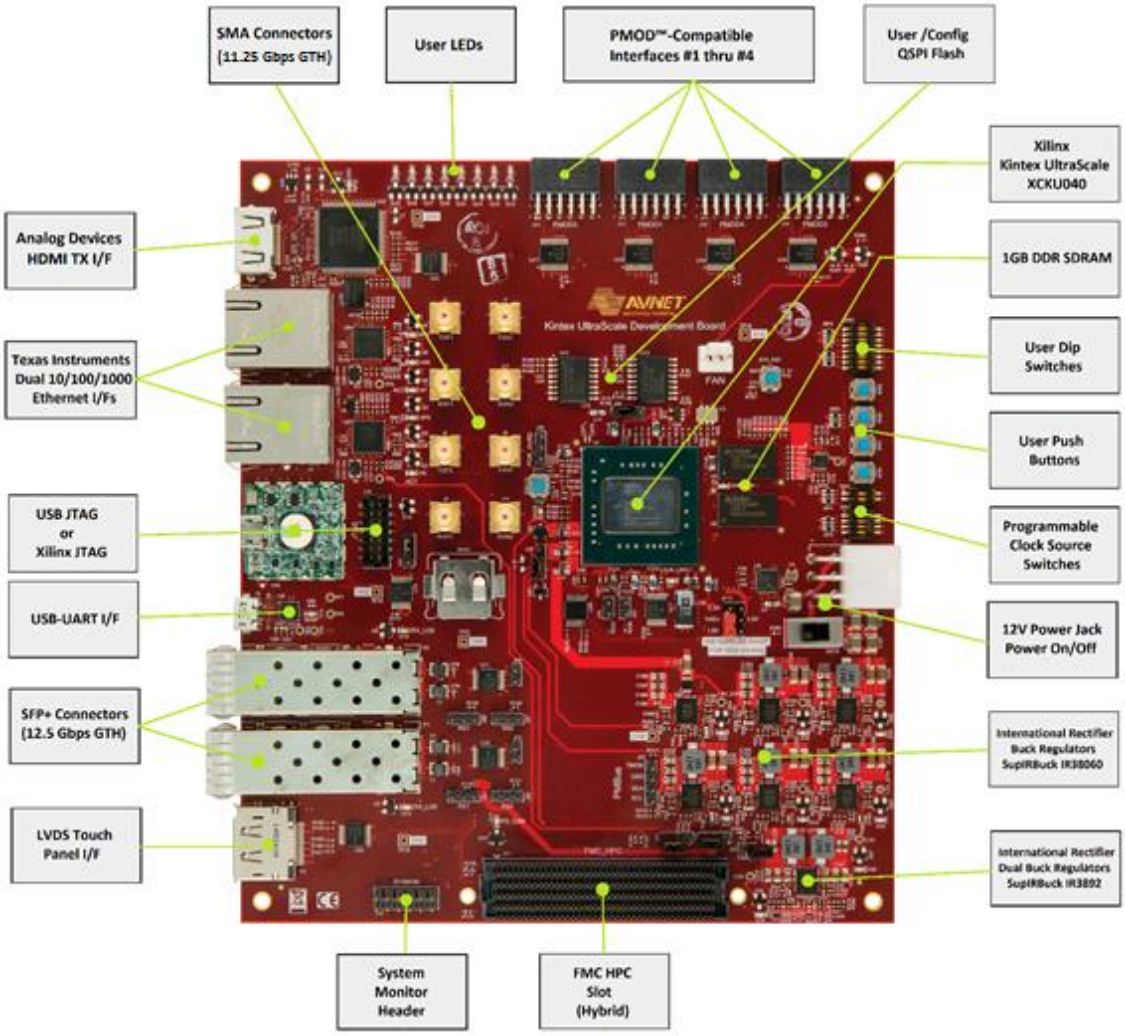


Figure 2 – Kintex UltraScale Development Board Interface Locations

2.1 XCKU040-1FBVA676 Bank Pin Assignments

The Kintex UltraScale Development Board uses the XCKU040-1FBVA676 device, which has 6 I/O banks along with 4 GTH banks. The following figure shows the bank pin assignments for the XCKU040 device on the Kintex UltraScale Development Board.

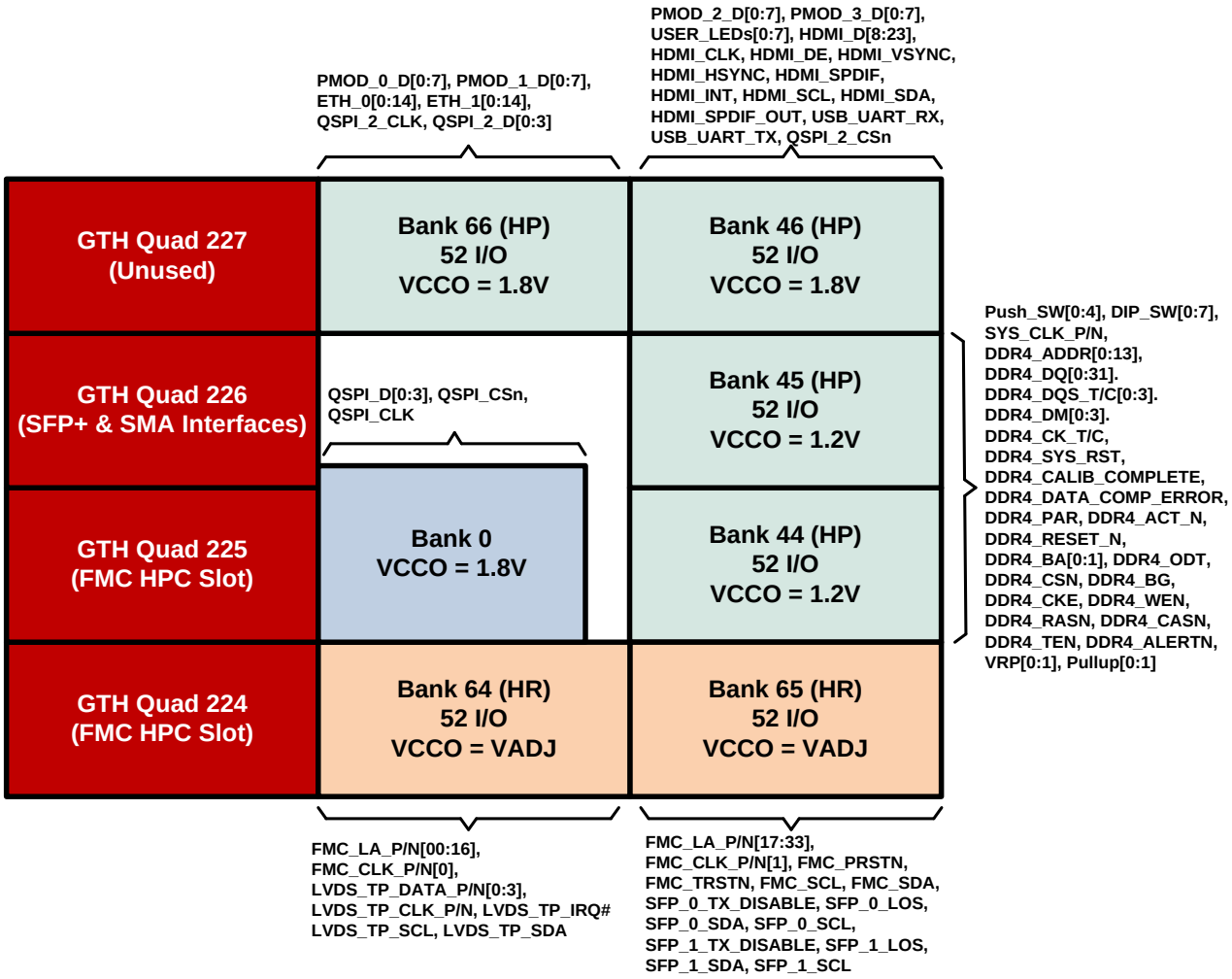


Figure 3 – XCKU040-1FBVA676 Bank Pin Assignments

2.2 Board I/O Count

The following table shows the overall I/O count for the Kintex UltraScale Development Board.

Table 1 – Kintex UltraScale Development Board I/O Count

Device	I/O Pins	Comments
FMC Slot	72	VADJ signal levels
FMC Slot Misc Signals	4	3.3V signal levels
DIP Switches	8	1.2V signal levels
Push Switches	5	1.2V signal levels
LEDs	8	1.8V signal levels
SFP Modules	8	3.3V signal levels
DDR4	77	1.2V signal levels
DDR4 Misc Signals	4	1.2V signal levels
USB-UART	2	1.8V signal levels
User QSPI	6	1.8V signal level
HDMI	25	1.8V signal levels
LVDS Touch Panel	10	VADJ signal levels
LVDS Touch Panel	3	3.3V signal levels
250 MHz System Clock	2	LVDS signal levels
ETH PHY(2)	30	1.8V signal levels
Quad PMODs	32	3.3V signal levels
Total I/O Count	**296**	**Total available I/O = 312**

2.3 250MHz System Clock Input

The following figure shows the system clock input on the Kintex UltraScale Development Board. The **Silicon Labs Si510/Si511** or compatible device can be used to generate the system clock input.

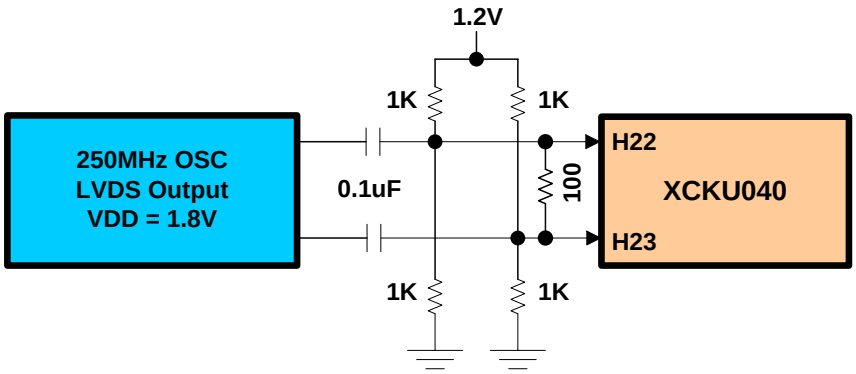


Figure 4 – 250MHz System Clock Input

The system clock is connected to Bank 45 of the XCKU040 device. The table below shows the connection that is made to the FPGA for the differential system clock.

Table 2 – Differential System Clock Pin Assignments

System Clock Interface	FPGA Bank	FPGA Pin
250MHZ_SYSCLK_P	45	H22
250MHZ_SYSCLK_N	45	H23

2.4 USB-UART Port

The Kintex UltraScale Development Board provide terminal communications through a USB-UART port. The **SiLabs CP2104** device is used to implement this interface as shown in the following figure.

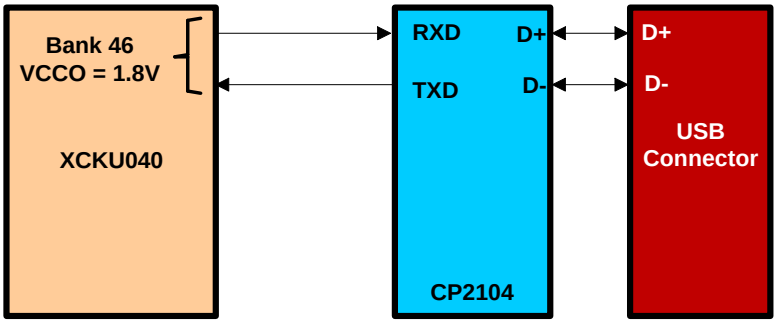


Figure 5 - USB-UART Interface

The **SiLabs CP2104** is powered from the USB interface it plugs into and the COM port will enumerate without the Kintex UltraScale Board being powered ON. The benefit of implementing the communication interface this way is that the COM ports will not be in a state of flux of the end user is power cycling the board during development.

An LED indicator on board the Kintex UltraScale Development Board, D12, will illuminate when the USB-UART interface is in a USB active-state. If the USB-UARTR interface enters the USB SUSPEND state, the LED will turn OFF.

The USB-UART Interface is connected to Bank 46 of the XCKU040 device. The table below shows the connection that is made to the FPGA for the USB-UART Interface.

Table 3 – USB-UART Pin Assignments

USB-UART Interface	FPGA Bank	FPGA Pin
USB_UART_TXD	46	D20
USB_UART_RXD	46	C19

Note: The TXD and RXD signals at the FPGA are already swapped to the right direction. TXD is the transmit data from the FPGA and RXD is the receive data to the FPGA.

2.5 Configuration QSPI Interface

The Kintex UltraScale development board implements a footprint suitable for housing a **Micron N25Q256A** or **Spansion S25FL256SAGMFIR0** Multi-bit (x4 data) QSPI Flash device that is used for configuration of the XCKU040 device. The selection of the Micron or Spansion device is accomplished via zero-ohm resistors that is a set at the factory depending on device availability. The Spansion device has separate rails for the VCC and VIO while the Micron device has a common VCC and VIO. The following figure shows the use of the Micron device.

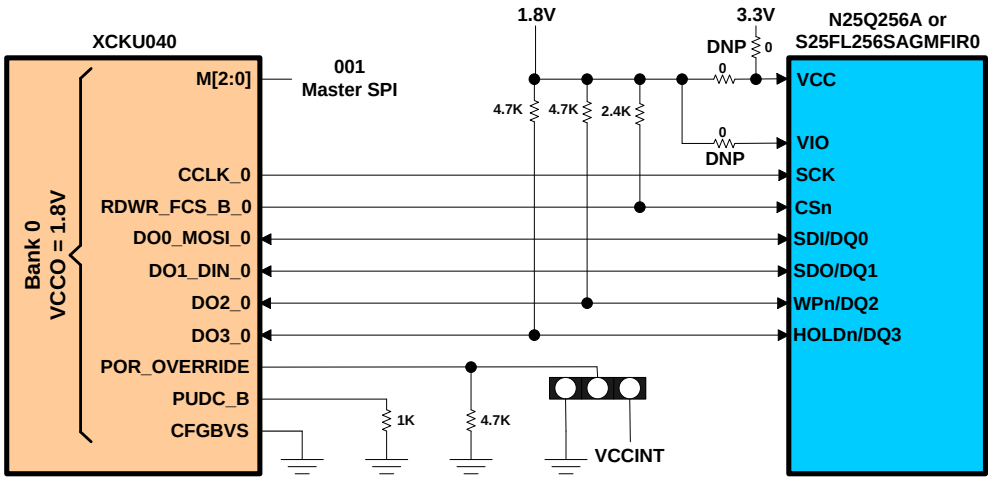


Figure 6 – Configuration QSPI Interface

The Configuration QSPI interface is 4-bits wide and is connected to Bank 0 of the XCKU040 device. The table below shows the connections to that are made to the FPGA for the Configuration QSPI Interface.

Table 4 – Configuration QSPI Pin Assignments

Configuration QSPI Interface	FPGA Pin
QSPI_1_DQ3	P7
QSPI_1_DQ2	R7
QSPI_1_DQ1	T7
QSPI_1_DQ0	U7
QSPI_1_CS	N7
QSPI_1_CLK	U9

2.6 User Code/Data QSPI Interface

The Kintex UltraScale development board implements a footprint suitable for housing a **Micron N25Q256A** or **Spansion S25FL256SAGMFIR0** Multi-bit (x4 data) QSPI Flash device for user code/data storage. The selection of the Micron or Spansion device is accomplished via zero-ohm resistors that is a set at the factory depending on device availability. The Spansion device has separate rails for the VCC and VIO while the Micron device has a common VCC and VIO. The following figure shows the use of the Micron device.

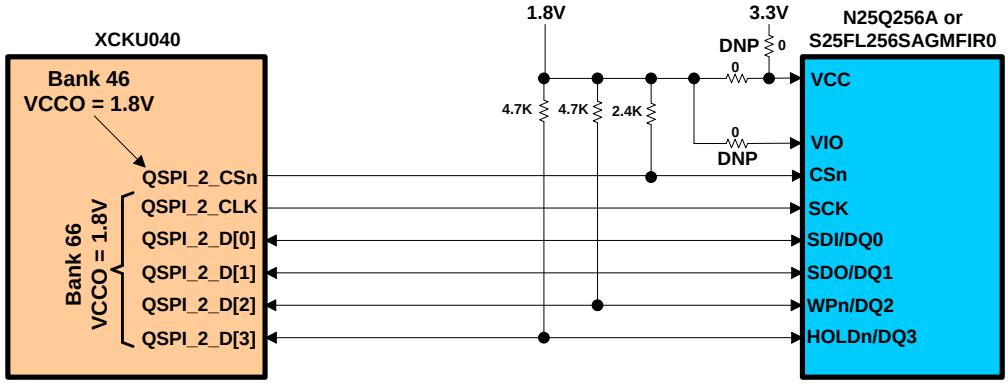


Figure 7 - User Code/Data QSPI Interface

The User Code/Data QSPI interface is 4-bits wide and is connected to Bank 66 and Bank 46 of the XCKU040 device. The table below shows the connections to that are made to the FPGA for the User Code/Data QSPI Interface.

Table 5 – User QSPI Pin Assignments

User QSPI Interface	FPGA Bank	FPGA Pin
QSPI_2_DQ3	66	H12
QSPI_2_DQ2	66	J11
QSPI_2_DQ1	66	H11
QSPI_2_DQ0	66	G11
QSPI_2_CS	46	D19
QSPI_2_CLK	66	F10

2.7 Programmable LVDS Clock Source

The Kintex UltraScale Development Board utilizes the **Texas Instruments CDCM61002** clock synthesizer to provide reference clock inputs to the Kintex UltraScale GTH ports as shown in the following figure. The OUT0 output of the clock synthesizer is used by the SFP+ and GTH SMA connectors. The OUT1 output of this clock synthesizer is the reference clock input to the GTH ports used by the FMC HPC interface.

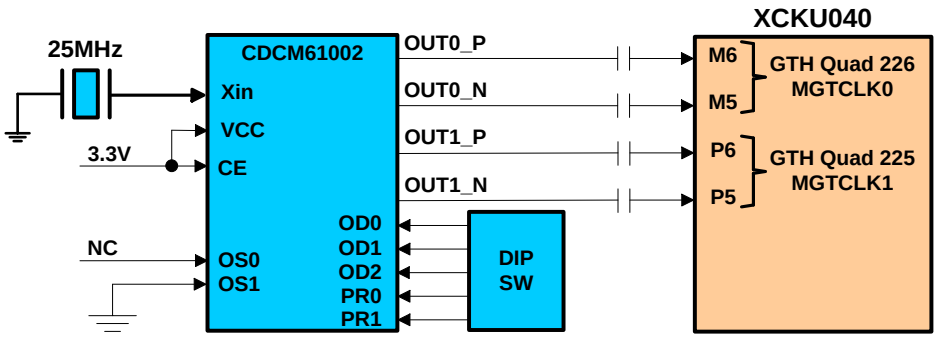


Figure 8 – GTH Programmable LVDS Clock Source

The clock synthesizer has two DIP switches, SW2 and SW3, implemented that is used to determine the synthesized frequency output from the **Texas Instruments CDCM61002.** The following table shows the DIP switch settings required to generate some common GTH frequencies. Other frequencies for the GTH can be set by consulting the datasheet for the CDCM61002 for the proper settings for the PR and OD inputs to the device.

Table 6 – CDCM61002 Dip Switch Settings

Output Freq (MHz)	PRESCALER FEEDBACK DIVIDER	OUTPUT DIVIDER	PR1 SW2 2:3	PR0 SW2 1:4	OD2 SW3 3:6	OD1 SW3 2:7	OD0 SW3 1:8
100.00	3 / 24	6	ON	ON	OFF	ON	OFF
125.00	4 / 20	4	OFF	OFF	ON	OFF	OFF
150.00	3 / 24	4	ON	ON	ON	OFF	OFF
156.25	3 / 25	4	OFF	ON	ON	OFF	OFF
200.00	3 / 24	3	ON	ON	ON	OFF	ON
250.00	4 / 20	2	OFF	OFF	ON	ON	OFF
312.50	3 / 25	2	OFF	ON	ON	ON	OFF
625.00	3 / 25	1	OFF	ON	ON	ON	ON

Note 1: Switch ON (Toggled away from the FPGA) = GND
Note 2: Switch OFF (Toggled towards the FPGA) = VCC

2.8 GTH Interfaces

The GTH transceiver is a full-duplex serial transceiver for point-to-point transmission applications. All GTH ports connected to the SFP+ socket, SMA connectors, and the FMC slot are design to support data rates up to 12.5Gbp.

The GTH transceivers are grouped into four transceivers per bank called a quad. Of the 4 GTH quads on the XCKU040 device, 3 GTH quads are implemented. Bank 224 and Bank 225 is dedicated to the FMC HPC connector. Bank 226 is designed to support SFP+ and SMA interfaces and Bank 227 is not implemented.

Each GTH bank or quad contains two reference clock inputs. Bank 224 implements on of the two reference clock inputs. The reference clock input is received from the FMC connector. Bank 225 implements two reference clock inputs. One port is tied to one of the ports on the **Texas Instruments CDCM61002** frequency synthesizer and the other clock input is received from the FMC connector. Bank 226 implemented one of the two reference clock inputs and is tied to one of the ports on the **Texas Instruments CDCM61002** frequency synthesizer.

The following figure shows the implementation of the GTH interfaces on the Kintex UltraScale Development Board.

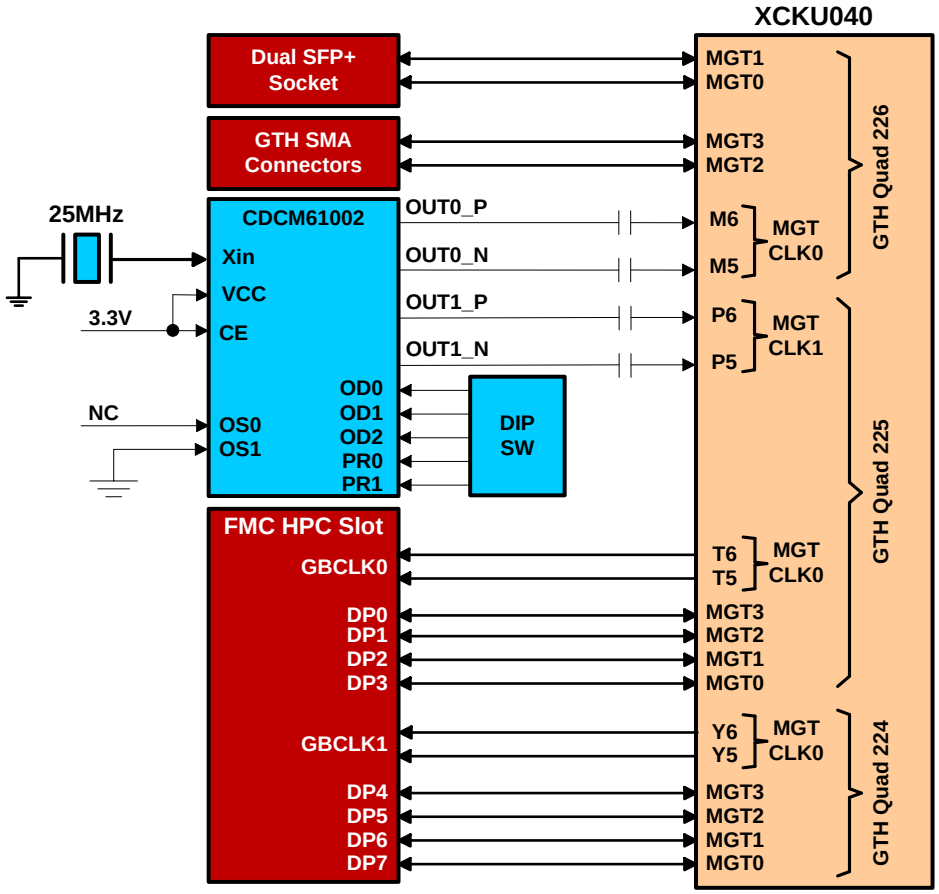


Figure 9 – Kintex UltraScale Development Board GTH Interfaces

Each of the GTH Interfaces is documented individual in other sections of this user guide. For more details about the SFP+ Sockets, please refer to the “SFP+ Interfaces” section of this user guide. For more details about the GTH SMA Connectors, please refer to the “SMA Connectors“

section of this user guide. For more information about the FMC HPC GTH connections, please refer to the “FMC HPC GTH Interfaces“ section of this user guide.

2.8.1 GTH Reference Clocks

The Kintex UltraScale Development Board gets its GTX reference clock inputs from two sources. One source is the LVDS clock synthesizer from **Texas Instruments**, the **CDCM61002.** The other source is from the FMC HPC connector, JX1. Please refer to the “Programmable LVDS Clock Source” section of this user guide for more details on the LVDS clock synthesizer.

The following table shows all of the possible reference clock options for the XCKU040 GTH Quads.

Table 7 – GTH Quad Reference Clock Pin Assignments

Quad Reference Clock	Interface	FPGA Quad	FPGA Pin
GCLK1_M2C_C_P	FMC HPC	224	Y6
GCLK1_M2C_C_N	FMC HPC	224	Y5
GCLK0_M2C_C_P	FMC HPC	225	T6
GCLK0_M2C_C_N	FMC HPC	225	T5
LVDS_CLK1_C_P	PROGRAMMABLE	225	P6
LVDS_CLK1_C_N	PROGRAMMABLE	225	P5
LVDS_CLK0_C_P	PROGRAMMABLE	226	M6
LVDS_CLK0_C_N	PROGRAMMABLE	226	M5

2.8.2 SFP+ Interfaces

The Kintex UltraScale Development Board provides two SFP+ module connectors that can be used to implement high-speed data links as well as low-speed links such as optical/copper Ethernet. The SFP+ connectors can be used to implement two lanes of high speed links that can operate up to 12.5Gbps per lane at PRBS-31..

The following tables show the FPGA Pin assignments to the transceiver Bank 226 and the IO Bank 65 of the Kintex UltraScale device for each of the SFP+ Ports.

Table 8 – SFP1+ Pin Assignments

SFP1+ Signals	FPGA Quad	FPGA Pin
SFP1_RX_P	226	M2
SFP1_RX_N	226	M1
SFP1_TX_P	226	N4
SFP1_TX_N	226	N3
SFP1_TX_DISABLE	65	AF24
SFP1_RX_LOS	65	AD26
SFP1_SDA	65	AF23
SFP1_SCL	65	AE26

Table 9 – Ethernet SFP2+ Pin Assignments

SFP2+ Signals	FPGA Quad	FPGA Pin
SFP2_RX_P	226	K3
SFP2_RX_N	226	K1
SFP2_TX_P	226	L4
SFP2_TX_N	226	L3
SFP2_TX_DISABLE	65	AE23
SFP2_RX_LOS	65	AD25
SFP2_SDA	65	AD23
SFP2_SCL	65	AC22

The following figure shows the interface between the Kintex UltraScale device and the SFP+ module. The Kintex UltraScale Development Board is designed to support data rates up to 12.5Gbps data rate for each of the SFP+ interfaces.

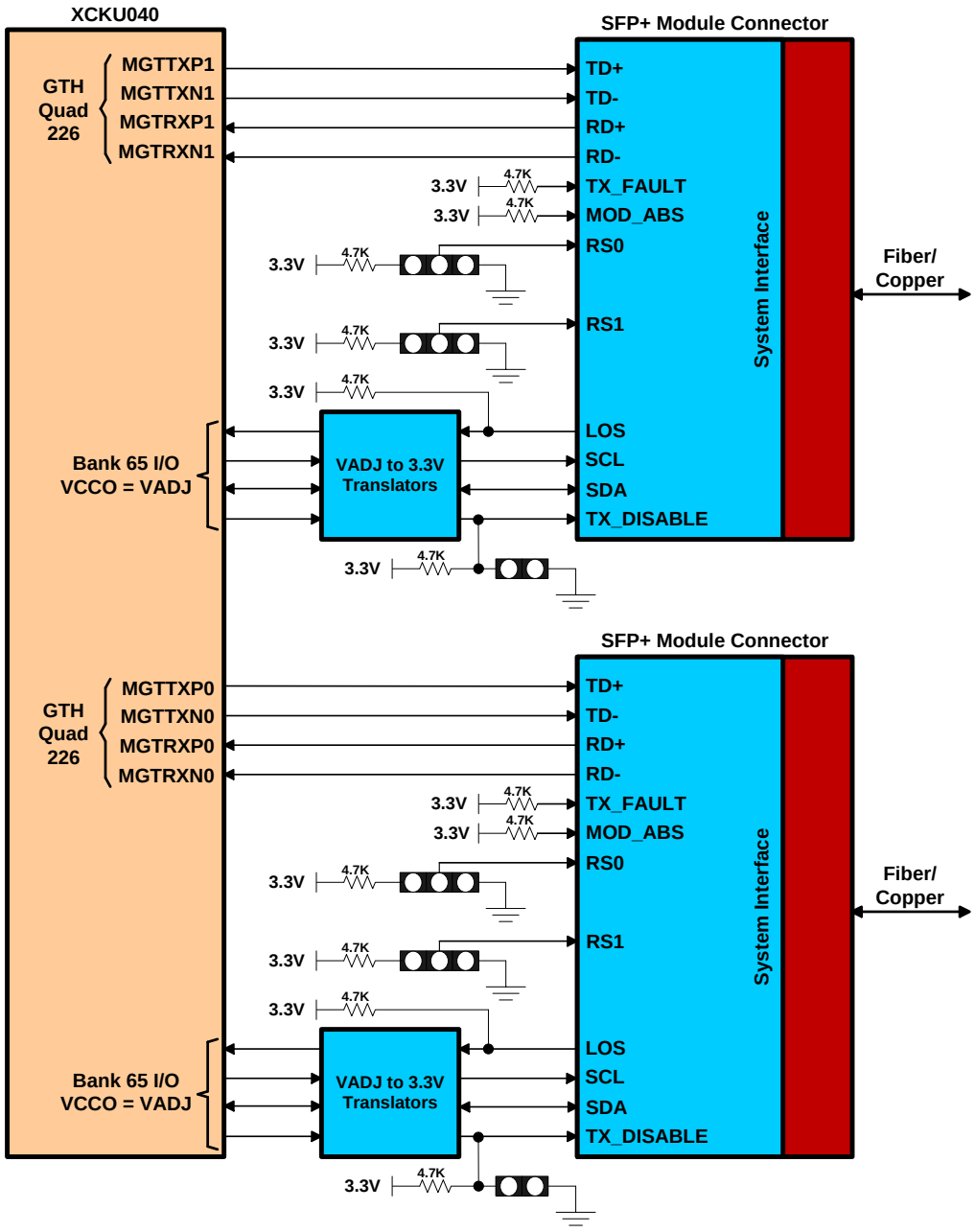


Figure 10 – Kintex UltraScale Development Board SFP+ Interfaces

The MGT Reference Clock used by the MGT Bank 226 on the XCKU040 is generated by one of the outputs of an on-board frequency synthesizer. The on-board frequency synthesizer is implemented with the **Texas Instruments CDCM61002.** Setting the frequency synthesizer up to generate the desired output frequency for the proper interface data rates is discussed in detail in the **Programmable LVDS Clock Source** section of this user guide.

The SFP+ interfaces contains three physical on-board jumpers used to control the rates select lines RS0 and RS1 as well as the TX Disable pin on the SFP+ module. The following tables list the jumpers with their respective jumper options.

Table 10 – SFP1+ Jumper Options

SFP1+ Signal	Function	Option
SFP1_TX_DISABLE	Optical Output Disabled	JP5: Installed
SFP1_TX_DISABLE	Optical Output Enabled	JP5: Not Installed
SFP1_RS1	Rate Select High (10.3125 Gb/s)	J24: Installed 1:2
SFP1_RS1	Rate Select Low (1.25 Gb/s)	J24: Installed 2:3
SFP1_RS0	Rate Select High (10.3125 Gb/s)	J25: Installed 1:2
SFP1_RS0	Rate Select Low (1.25 Gb/s)	J25: Installed 2:3

Table 11 – SFP2+ Jumper Options

SFP2+ Signal	Function	Option
SFP2_TX_DISABLE	Optical Output Disabled	JP6: Installed
SFP2_TX_DISABLE	Optical Output Enabled	JP6: Not Installed
SFP2_RS1	Rate Select High (10.3125 Gb/s)	J26: Installed 1:2
SFP2_RS1	Rate Select Low (1.25 Gb/s)	J26: Installed 2:3
SFP2_RS0	Rate Select High (10.3125 Gb/s)	J27: Installed 1:2
SFP2_RS0	Rate Select Low (1.25 Gb/s)	J27: Installed 2:3

Each SFP+ interface also contains an SFP+ Receive Loss of Signal LED. These LEDs illuminate when the associated SFP_RX_LOS is actively driven by the XCKU040. LED, D13, is associated with the SFP1+ interface and the LED, D14, is associated with SFP2+ interface.

2.8.3 SMA Interfaces

The Kintex UltraScale Development board four pairs of SMA connectors for differential TX and RX Data connections to the XCKU040 devices GTH transceivers. The SMA connectors can be used to implement two lanes of high speed links that can operate up to 11.25Gbps per lane at PRBS-31 when utilized with the proper SMA cables. The SMA connectors can also be operated at 12.5Gbps at PRBS-7 and PRBS-9 which is sufficient for supporting transmission schemes utilizing 8b/10b encoding at the maximum data rate of the GTH transceivers.

The following table shows the FPGA pin assignments to the transceivers in GTH Quad 226 of the XCKU040 device for each of the GTH lanes associated with the SMA connectors.

Table 12 – SMA Connector Pin Assignments

SMA Signals	FPGA Quad	FPGA Pin
SMA1_TX_P	226	J4
SMA1_TX_N	226	J3
SMA1_RX_P	226	H2
SMA1_RX_N	226	H1
SMA2_TX_P	226	G4
SMA2_TX_N	226	G3
SMA2_RX_P	226	F2
SMA2_RX_N	226	F1

2.8.4 FMC HPC GTH Interfaces

The Kintex UltraScale development board provides an FMC HPC slot with 1.8V, 2.5V or 3.3V VADJ to support FMC plug-in modules. The following figure shows how the FMC interface connects to the XCKU040 device. It should be noted that only FMC HPC LA signals are populated on the Kintex UltraScale Development Board. The board provides 8 GTH ports along

with the LA signals which should provide sufficient I/O ports for most applications. The FMC GTH ports can be used to implement eight lanes of high speed links that can operate up to 12.5Gbps per lane at PRBS-31.

The LA signals are described in more detail in the FMC HPC LA Interface section of this user guide.

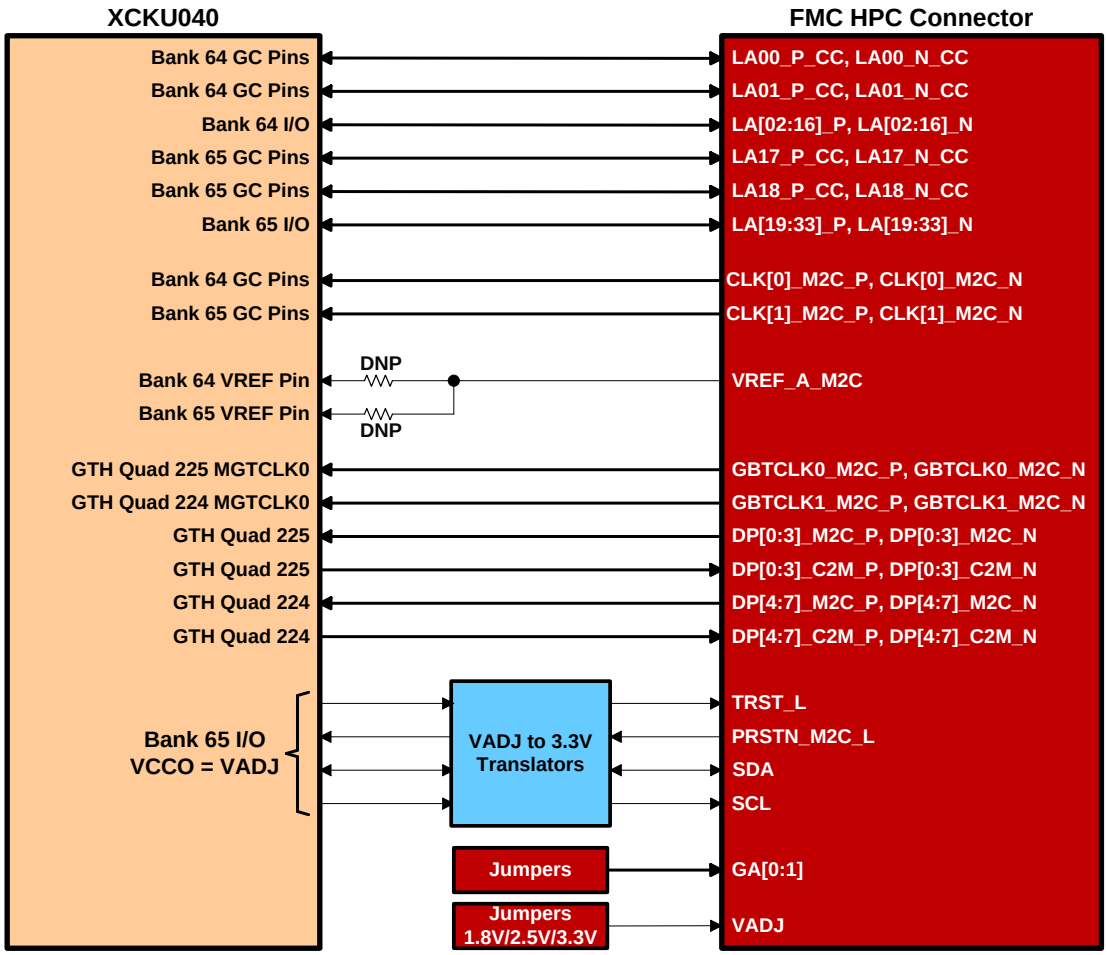


Figure 11 – FMC HPC Interface

The FMC HPC GTH signals are connected to GTH Quad 224 and GTH Quad 225 of the XCKU040 device. The table below shows the connections that are made to the FPGA for the FMC HPC GTH transceivers.

Table 13 – FMC HPC GTH Pin Assignments

FMC HPC GTH Signal	FPGA Quad	FPGA Pin
DP0_C2M_P	225	AA4
DP0_C2M_N	225	AA3
DP0_M2C_P	225	Y2
DP0_M2C_N	225	Y1
DP1_C2M_P	225	W4
DP1_C2M_N	225	W3
DP1_M2C_P	225	V2
DP1_M2C_N	225	V1
DP2_C2M_P	225	U4
DP2_C2M_N	225	U3
DP2_M2C_P	225	T2
DP2_M2C_N	225	T1
DP3_C2M_P	225	R4
DP3_C2M_N	225	R3
DP3_M2C_P	225	P2
DP3_M2C_N	225	P1
FMC HPC GTH Signal	FPGA Quad	FPGA Pin
DP4_C2M_P	224	AF6
DP4_C2M_N	224	AF5
DP4_M2C_P	224	AF2
DP4_M2C_N	224	AF1
DP5_C2M_P	224	AD6
DP5_C2M_N	224	AD5
DP5_M2C_P	224	AE4
DP5_M2C_N	224	AE3
DP6_C2M_P	224	AC4
DP6_C2M_N	224	AC3
DP6_M2C_P	224	AD2
DP6_M2C_N	224	AD1
DP7_C2M_P	224	AB6
DP7_C2M_N	224	AB5
DP7_M2C_P	224	AB2
DP7_M2C_N	224	AB1

2.9 LVDS Touch Panel Interface

The Kintex UltraScale Development Board supports LVDS touch panels through the Avnet designed ALI3 display interface. The ALI3 connector part number is **Tyco TE-2040451-1**.

The Avnet 7-inch Touch Display Kit provides engineers with everything needed to develop products with interactive GUIs and touchscreen capabilities. The kit combines an 800 x 480 WVGA TFT-LCD display with an industrial projective capacitive touch sensor, I2C-based touch controller, LED backlight supply and all the necessary cables.

The following figure depicts the implementation of the LVDS Touch Panel Interface and its physical connections to the XCKU040 device through Bank 64.

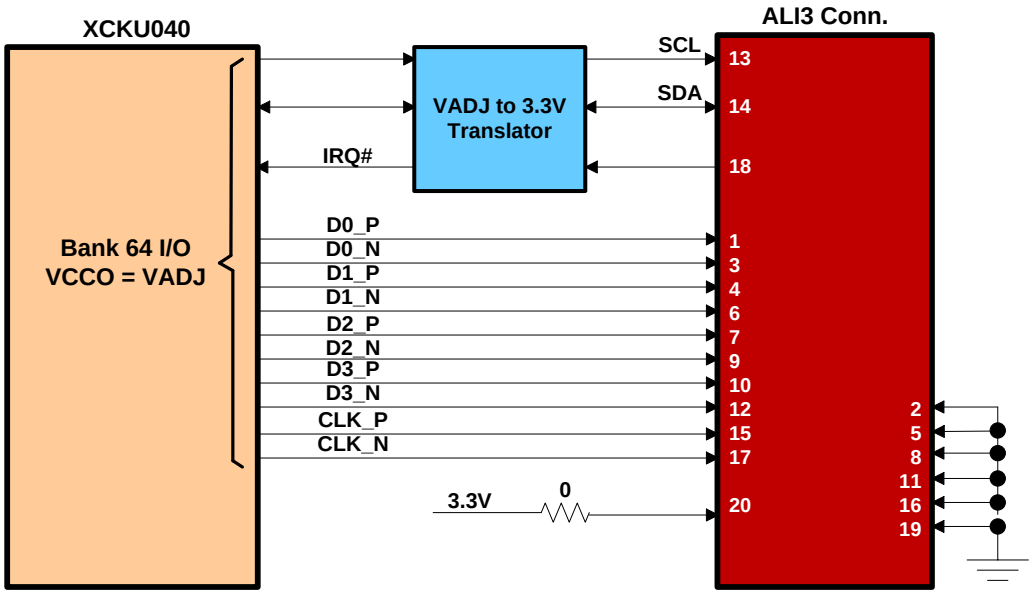


Figure 12 – LVDS Touch Panel Interface Implementation

Note: When the LVDS Touch Panel is used, the **VADJ** rail must be set to **2.5V** to support LVDS_25 signaling. The **VADJ** rail provides power to the XCKU040 banks 64 and 65. Bank 64 and Bank 65 is primarily used for the FMC HPC interface. If the FMC HPC interface is used with the LVDS Touch Panel interface, the FMC HPC add-on card should support a VADJ of 2.5V.

The following tables show the FPGA Pin assignments to the IO Bank 64 of the Kintex UltraScale device for the LVDS Touch Panel Interface.

Table 14 – LVDS Touch Panel Interface Pin Assignments

Touch Panel Interface	FPGA Pin
TP_D0_P	AA10
TP_D0_N	AA9
TP_D1_P	Y11
TP_D1_N	Y10
TP_D2_P	Y8
TP_D2_N	AA8
TP_D3_P	V12
TP_D3_N	V11
TP_SCL	Y12
TP_SDA	W10
TP_IRQ_N	W11
CLK_P	W9
CLK_N	W8

2.9.1 XCKU040 Device Package Delay Compensation

The XCKU040 device package delay is accommodated for in layout of the LVDS Touch Panel Interface signal trace lengths. The average of min and max values for package delay is utilized to compensate for the flight time caused by the delay associated with this package.

2.10 HDMI Interface

The Kintex UltraScale Development Board has an HDMI video interface that supports up to HDMI v1.4 and resolutions up to 1080p. An Analog Devices **ADV7511** low power HDMI

transmitter is used to drive the interface. The ADV7511 used both 1.8V and 3.3V to power the device with the I/O logic level at 1.8V.

The ADV7511 is a high speed High Definition Multimedia Interface (HDMI) transmitter that is capable of supporting an input data rate up to 165MHz (1080p @ 60Hz, UXGA @ 60Hz) and an output data rate up to 225MHz. Deep Color to 36 bits per pixel is supported to 1080p at 60Hz.

The following figure shows the HDMI interface on the Kintex UltraScale development board. The **Analog Devices ADV7511KSTZ** device will provide the HDMI interface.

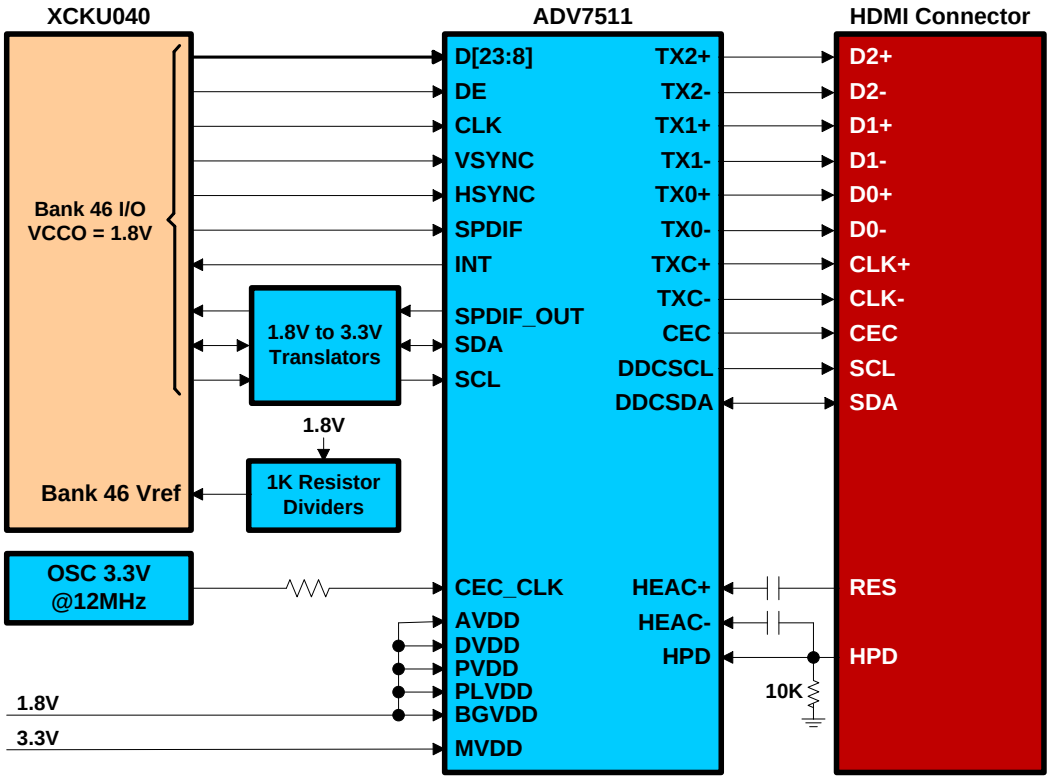


Figure 13 – Kintex UltraScale Development Board HDMI Interface

The HDMI digital interface is 16-bits wide and is connected to Bank 46 of the XCKU040 device. The table below shows the connections to that are made to the FPGA for the HDMI Interface.

Table 15 – HDMI Interface Pin Assignments

HDMI Interface	FPGA Pin
HDMI_D23	A25
HDMI_D22	A24
HDMI_D21	E23
HDMI_D20	D26
HDMI_D19	D25
HDMI_D18	B25
HDMI_D17	B24
HDMI_D16	C23
HDMI_D15	D23
HDMI_D14	C24
HDMI_D13	D24
HDMI_D12	B26
HDMI_D11	C26
HDMI_D10	A23
HDMI_D9	A22
HDMI_D8	A20
HDMI_DE	B22
HDMI_CLK	B21
HDMI_VSYNC	C22
HDMI_HSYNC	C21
HDMI_SPDIF	B20
HDMI_SPDIFOUT	E20
HDMI_SDA	E22
HDMI_SCL	D21
HDMI_INT	E21

2.10.1 XCKU040 Device Package Delay Compensation

The XCKU040 device package delay is accommodated for in layout of the HDMI Interface signal trace lengths. The average of min and max values for package delay is utilized to compensate for the flight time caused by the delay associated with this package.

2.11 FMC HPC LA Interface

The Kintex UltraScale development board provides an FMC HPC slot with 1.8V, 2.5V or 3.3V VADJ to support FMC plug-in modules. The following figure shows how the FMC interface connects to the XCKU040 device. It should be noted that only FMC HPC LA signals are populated on the Kintex UltraScale Development Board. The board provides 8 GTH ports along with the LA signals which should provide sufficient I/O ports for most applications. The GTH ports are described in more detail in the FMC HPC GTH Interface section of this user guide.

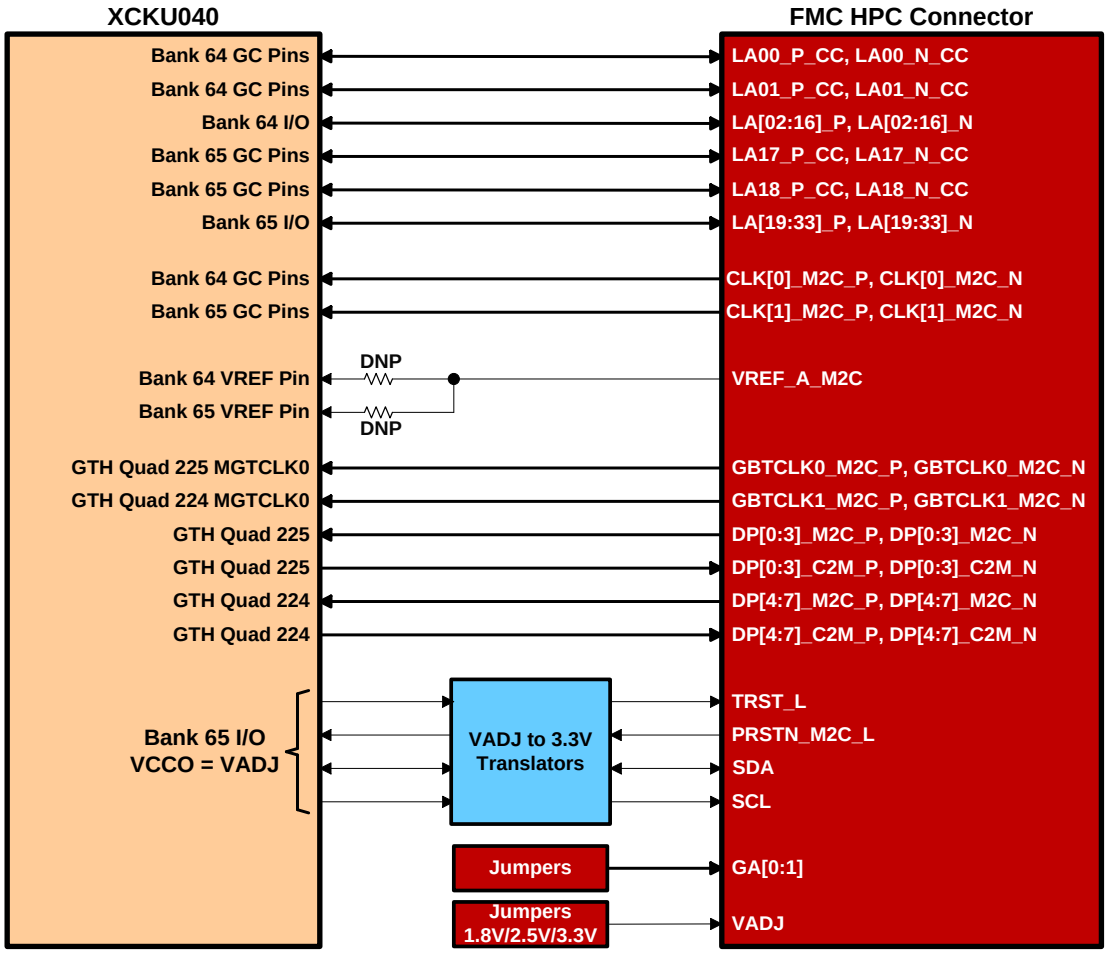


Figure 14 – FMC HPC Interface

The FMC HPC LA signals are connected to Bank 64 and Bank 65 of the XCKU040 device. The table below shows the connections that are made to the FPGA for the FMC HPC LA signals.

Table 16 – FMC HPC LA Pin Assignments

FMC HPC LA Signal	FPGA Bank	FPGA Pin
LA16_N	64	AF15
LA16_P	64	AE16
LA15_N	64	AF13
LA15_P	64	AF14
LA14_N	64	AE15
LA14_P	64	AD15
LA13_N	64	AF12
LA13_P	64	AE12
LA12_N	64	AC13
LA12_P	64	AC14
LA11_N	64	AD13
LA11_P	64	AD14
LA10_N	64	AB15
LA10_P	64	AA15
LA09_N	64	Y15
LA09_P	64	W15
LA08_N	64	AB14

LA08_P	64	AA14
LA07_N	64	W13
LA07_P	64	W14
LA06_N	64	AA12
LA06_P	64	AA13
LA00_CC_N	64	AB11
LA00_CC_P	64	AB12
CLK0_M2C_N	64	AC11
CLK0_M2C_P	64	AC12
LA01_CC_N	64	AE11
LA01_CC_P	64	AD11
LA05_N	64	AD9
LA05_P	64	AC9
LA04_N	64	AF10
LA04_P	64	AE10
LA03_N	64	AD8
LA03_P	64	AC8
LA02_N	64	AB9
LA02_P	64	AB10
FMC HPC LA Signal	**FPGA Bank**	**FPGA Pin**
LA33_N	65	AD16
LA33_P	65	AC16
LA32_N	65	AC17
LA32_P	65	AB17
LA31_N	65	AE18
LA31_P	65	AE17
LA30_N	65	AF20
LA30_P	65	AF19
LA29_N	65	AD18
LA29_P	65	AC18
LA28_N	65	AF18
LA28_P	65	AF17
LA27_N	65	Y16
LA27_P	65	W16
LA26_N	65	Y21
LA26_P	65	W21
LA25_N	65	W19
LA25_P	65	W18
LA24_N	65	V19
LA24_P	65	V18
LA23_N	65	Y18
LA23_P	65	Y17
LA17_CC_N	65	Y20
LA17_CC_P	65	W20
CLK1_M2C_N	65	AA20
CLK1_M2C_P	65	AA19
LA18_CC_N	65	AB20
LA18_CC_P	65	AB19
LA22_N	65	AD19
LA22_P	65	AC19
LA21_N	65	AE21
LA21_P	65	AE20
LA20_N	65	AC21
LA20_P	65	AB21
LA19_N	65	AD21
LA19_P	65	AD20

2.11.1 XCKU040 Device Package Delay Compensation

The XCKU040 device package delay is accommodated for in layout of the FMC HPC Interface signal trace lengths. The average of min and max values for package delay is utilized to compensate for the flight time caused by the delay associated with this package.

2.12 DDR4 SDRAM Interface

The Kintex UltraScale Development Board provides 1GB of DDR4 memory (256M x 32) as shown in the following figure. The **Micron EDY4016AABG-DR-F** device is used to implement the DDR4 SDRAM interface. The following figure shows the Micron DD4 Memory implementation with respect to the Kintex UltraScale Bank 44 and Bank45 that the devices are interfaced to.

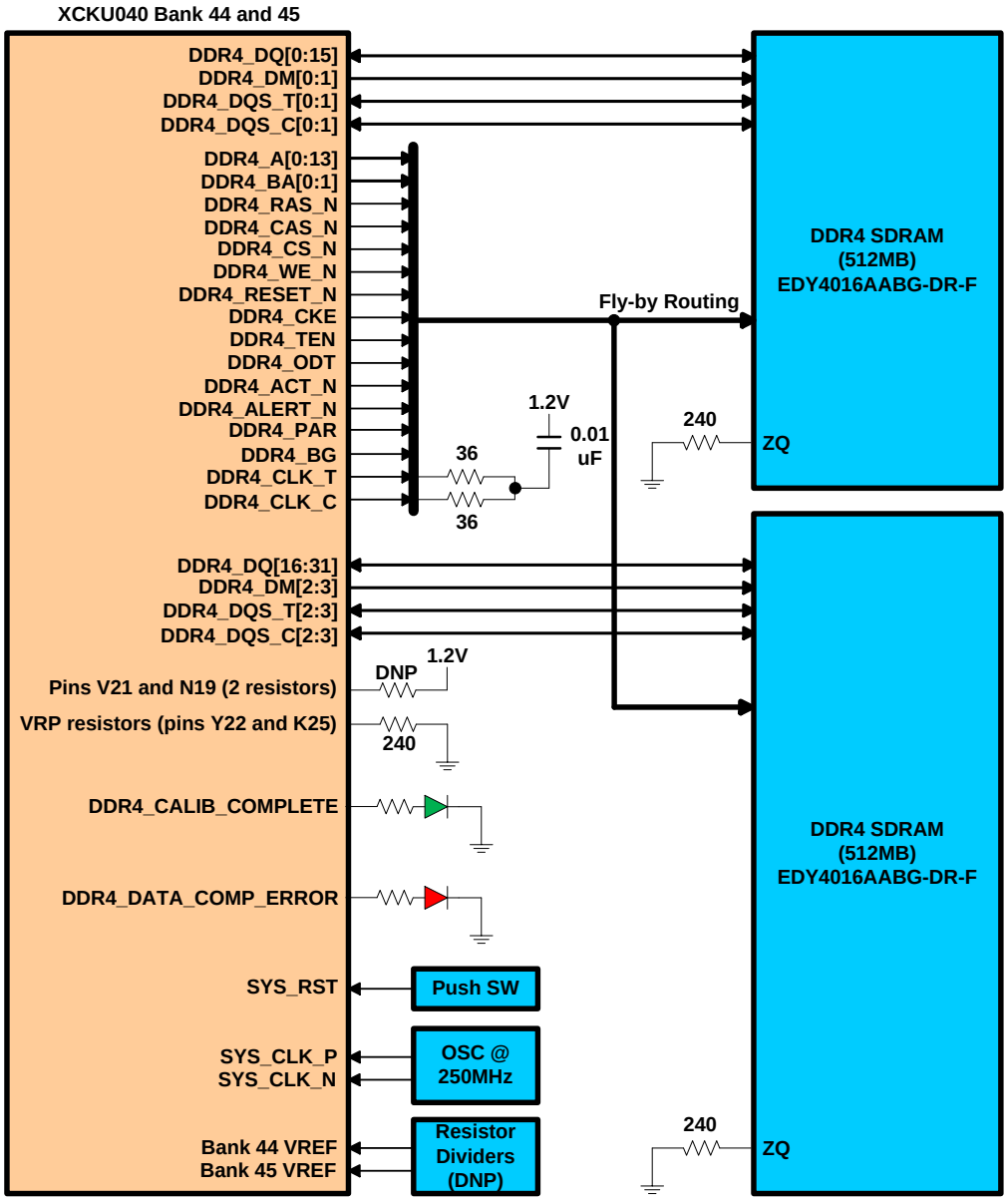


Figure 15 –Micron DDR4 Memory Interface Implementation

The following table shows the DDR4 interface pinout for the Kintex UltraScale based on results from **MIG (Memory Interface Generator) Version 6.1 for UltraScale Architecture (Vivado 2014.4)**. The XCKU040 banks 44 and 45 are used to implement the DDR4 interface.

Table 17 – DDR4 Interface Pin Out

DDR4 Signal	FPGA Pin
DDR4_A0	AA24
DDR4_A1	AB24
DDR4_A2	AB26
DDR4_A3	AC26
DDR4_A4	AA22
DDR4_A5	AB22
DDR4_A6	Y23
DDR4_A7	AA23
DDR4_A8	AC23
DDR4_A9	AC24
DDR4_A10	W23
DDR4_A11	W24
DDR4_A12	W25
DDR4_A13	W26
DDR4_BA0	V26
DDR4_BA1	U24
DDR4_BG	V24
DDR4_CAS_N	Y26
DDR4_RAS_N	U26
DDR4_WE_N	Y25
DDR4_CKE	V23
DDR4_CS_N	V22
DDR4_ODT	U25
DDR4_CK_T	AA25
DDR4_CK_C	AB25
DDR4_DM_DBI_N[3]	E25
DDR4_DM_DBI_N[2]	N23
DDR4_DM_DBI_N[1]	R18
DDR4_DM_DBI_N[0]	T23
DDR4_DQS3_T	F22
DDR4_DQS3_C	F23
DDR4_DQS2_T	K26
DDR4_DQS2_C	J26
DDR4_DQS1_T	T19
DDR4_DQS1_C	T20
DDR4_DQS0_T	R22
DDR4_DQS0_C	R23
DDR4_DQ31	G24
DDR4_DQ30	H24
DDR4_DQ29	J25
DDR4_DQ28	J24
DDR4_DQ27	F25
DDR4_DQ26	G25
DDR4_DQ25	G26
DDR4_DQ24	H26
DDR4_DQ23	L25
DDR4_DQ22	M25
DDR4_DQ21	M22
DDR4_DQ20	N22
DDR4_DQ19	L24
DDR4_DQ18	M24
DDR4_DQ17	M26

DDR4_DQ16	N26
DDR4_DQ15	U21
DDR4_DQ14	U20
DDR4_DQ13	R20
DDR4_DQ12	P20
DDR4_DQ11	P19
DDR4_DQ10	P18
DDR4_DQ9	R21
DDR4_DQ8	P21
DDR4_DQ7	R25
DDR4_DQ6	P25
DDR4_DQ5	P24
DDR4_DQ4	P23
DDR4_DQ3	R26
DDR4_DQ2	P26
DDR4_DQ1	U22
DDR4_DQ0	T22
DDR4_TEN	N21
DDR4_ALERTN	M21
DDR4_CALIB_COMPLETE	T18
DDR4_DATA_COMP_ERROR	V21
DDR4_RESETN	T25
DDR4_SYS_RST	N24
DDR4_PAR	J19
DDR4_ACTN	T24
SYSCLK_P (250 MHz LVDS Clock Source)	H22
SYSCLK_N (250 MHz LVDS Clock Source)	H23
VRP DCI resistor (bank 44 and 45)	Y22, K25
Pull-up resistor (bank 44 and 45)	V21, N19
VREF (bank 44 and 45)	U19, N18

2.12.1 DDR4 VREF and VTT Generation

The Kintex UltraScale Development Board uses the **Texas Instruments TPS51200** device to generate the DDR4 VREF and VTT rails. The VTT supply is used to terminate the DDR4 Address and Control signals group while the VREF supply provides the reference voltage to the DDR4 devices for the Address and Control signal group. The Kintex UltraScale Development Board is populated with resistor dividers to provide optional VREF input to the bank 44 and 45 as shown in the following figure.

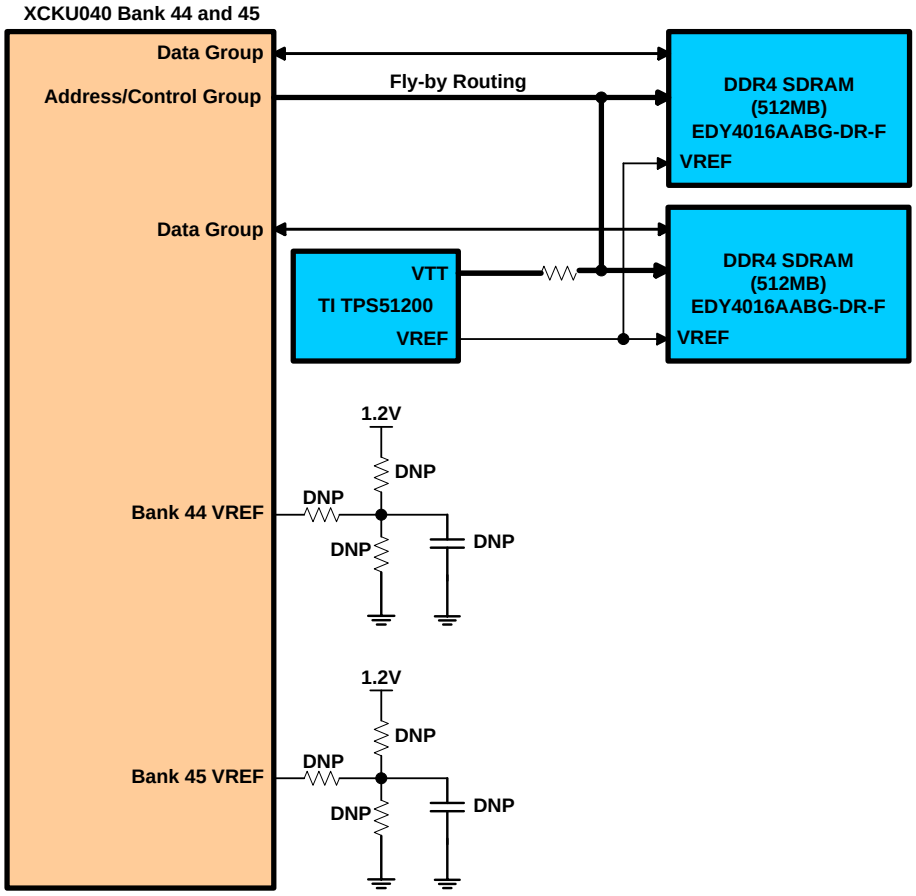


Figure 16 – DDR4 VREF and VTT Supplies

Note: VREF for DDR4 DQ and Kintex UltraScale banks 44 and 45 is generated internally. However, as shown in the above figure, the optional resistor dividers are provided in order to generate the Kintex UltraScale VREF input externally, if needed.

2.12.2 XCKU040 Device Package Delay Compensation

The XCKU040 device package delay is accommodated for in layout of the DDR4 signal trace lengths. The average of min and max values for package delay is utilized to compensate for the flight time caused by the delay associated with this package.

2.13 10/100/1000 Ethernet PHY Interfaces

The Kintex UltraScale Development Board provides two 10/100/1000 Ethernet ports. The **Texas Instruments DP83867** device is used to implement this interface. Both of the Ethernet PHYs connect to the XCKU040 device through Bank 66.

The following tables show the FPGA Pin assignments to Bank 66 of the Kintex UltraScale device for each of the Ethernet Ports.

Table 18 – Ethernet PHY1 Pin Assignments

Ethernet PHY 1 Signals	FPGA Pin
PHY1_MDIO	C8
PHY1_MDC	C9
PHY1_RX_D3	C11
PHY1_RX_D2	B11
PHY1_RX_D1	B10
PHY1_RX_D0	A10
PHY1_RX_CTRL	D11
PHY1_RX_CLK	E11
PHY1_TX_D3	J10
PHY1_TX_D2	J9
PHY1_TX_D1	H9
PHY1_TX_D0	H8
PHY1_TX_CTRL	G9
PHY1_GTX_CLK	G10
PHY1_RESET_N	D9

Table 19 – Ethernet PHY2 Pin Assignments

Ethernet PHY 2 Signals	FPGA Pin
PHY2_MDIO	C8
PHY2_MDC	C9
PHY2_RX_D3	C11
PHY2_RX_D2	B11
PHY2_RX_D1	B10
PHY2_RX_D0	A10
PHY2_RX_CTRL	D11
PHY2_RX_CLK	E11
PHY2_TX_D3	J10
PHY2_TX_D2	J9
PHY2_TX_D1	H9
PHY2_TX_D0	H8
PHY2_TX_CTRL	G9
PHY2_GTX_CLK	G10
PHY2_RESET_N	D9

A high-level block diagram of the 10/100/1000 Ethernet interface is shown in the following figure.

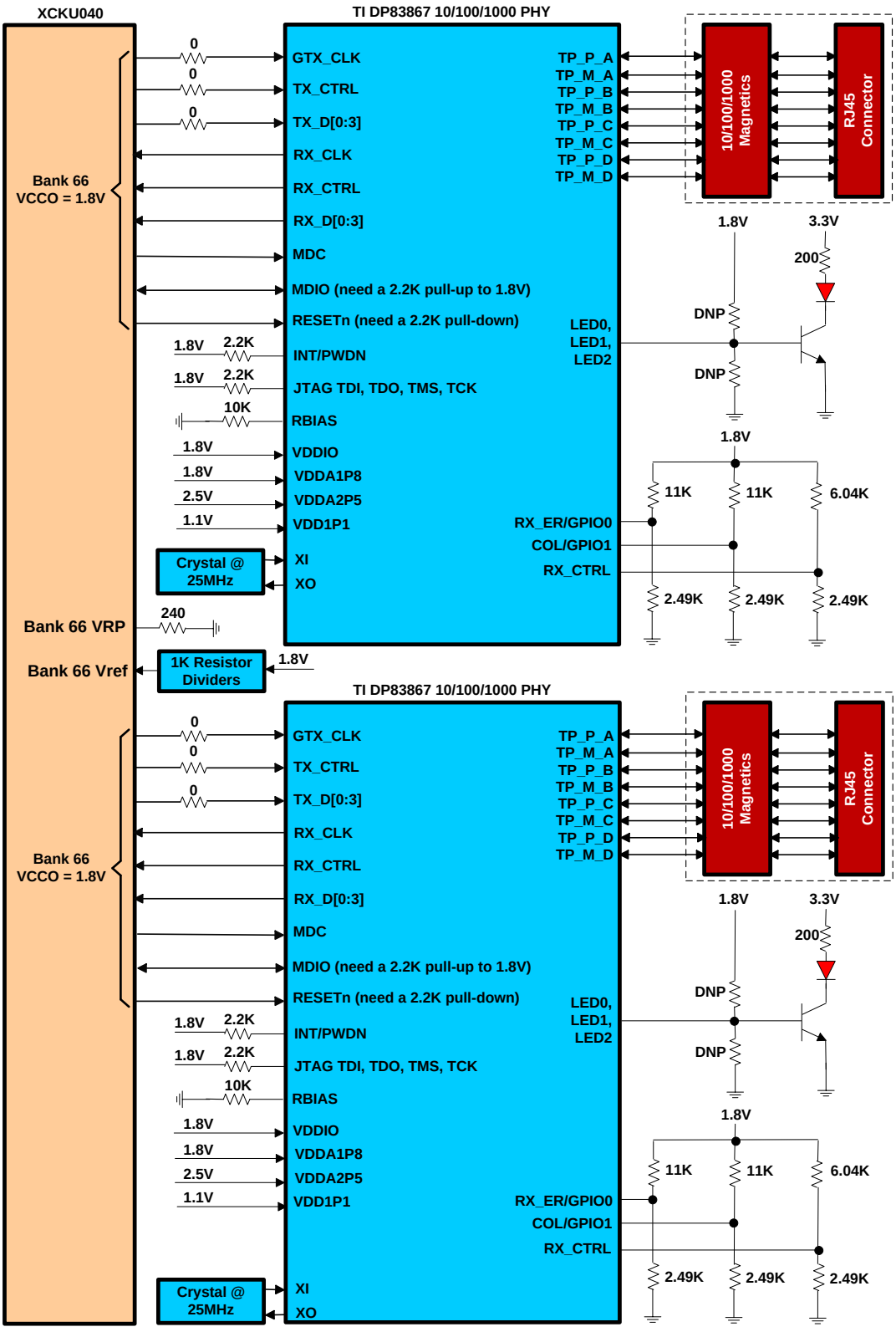
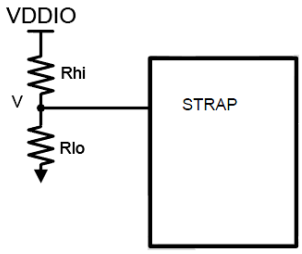


Figure 17 –Ethernet Interface Implementation

2.13.1 10/100/1000 Ethernet PHY Strapping Resistors

The **Texas Instruments DP83867** device that is utilized to implement the Ethernet PHY functionality contains many setup options that can be implemented through strapping resistors physically on the PCB rather than through register accesses in software. These strapping resistors allow the Ethernet PHYs to be active without user interaction.

The following figure shows the strapping circuit and the possible resistor combinations that set the proper mode.



Strap Resistor Ratios

Mode	Ideal Rhi (kΩ)	Ideal Rlo (kΩ)
1	OPEN	OPEN
2	11	2.49
3	6.04	2.49
4	2.49	OPEN

Figure 18 – PHY Strapping Circuit and Modes

The following table lists the various strapping options that are available for both PHYs on the Kintex UltraScale Development Board and the default mode that they are strapped too. For a definition of what other options are available by changing the default mode settings, please refer to the **Texas Instruments DP83867** data sheet.

Table 20 – Ethernet PHY1 Strapping Configuration

PHY1 Strap Function	PHY1 Pin Name	Mode Set	Function Value
PHYADD[1:0]	RX_D0	2	"01"
PHYADD[3:2]	RX_D2	1	"00"
EEE Disable / Autoneg Disable	RX_CTRL	3	"10"
RGMII Clock Skew RX[0]	GPIO_0	1	"0"
RGMII Clock Skew RX[2:1]	GPIO_1	2	"01"
RGMII Clock Skew TX[1:0]	LED_2	3	"10"
SPEED_SEL / RGMII Clock Skew TX[2]	LED_1	1	"00"
Mirror Enable / SGMII Enable	LED_0	1	"00"

This set PHY1 ADDRESS to "0001", RGMII RX Clock Skew to "001" for 1.0ns skew, RGMII TX Clock Skew to "001" for 1.0ns skew, and SPEED SEL to "0" for Tri-Mode Ethernet.

Table 21 – Ethernet PHY2 Strapping Configuration

PHY2 Strap Function	PHY1 Pin Name	Mode Set	Function Value
PHYADD[1:0]	RX_D0	4	"11"
PHYADD[3:2]	RX_D2	1	"00"
EEE Disable / Autoneg Disable	RX_CTRL	3	"10"
RGMII Clock Skew RX[1]	GPIO_0	1	"0"
RGMII Clock Skew RX[2:0]	GPIO_1	2	"01"
RGMII Clock Skew TX[0:1]	LED_2	3	"10"
SPEED_SEL / RGMII Clock Skew TX[2]	LED_1	1	"00"
Mirror Enable / SGMII Enable	LED_0	1	"00"

This set PHY2 ADDRESS to "0011", RGMII RX Clock Skew to "001" for 1.0ns skew, RGMII TX Clock Skew to "001" for 1.0ns skew, and SPEED SEL to "0" for Tri-Mode Ethernet.

As of the writing of this user guide, the table in the Texas Instruments DP83867 datasheet incorrectly list the RGMII Clock Skew bit [1] to be RGMII Clock Skew bit [0] and RGMII Clock Skew bit [0] to be RGMII Clock Skew bit [1] for both the RX and TX RGMII Clock Skews.

2.13.2 Ethernet PHY LEDs

The Kintex UltraScale Development Board contains Ethernet PHY controlled LEDs both on board the PCB and within the RJ45 Ethernet Jack for both of the Ethernet Interfaces. The LEDs functions implemented include LINK, SPEED, and ACTIVITY for the on board LEDs and SPEED and ACTIVITY for the RJ45 Ethernet Jacks.

2.13.3 XCKU040 Device Package Delay Compensation

The XCKU040 device package delay is accommodated for in layout of the each of the Ethernet PHY signal trace lengths. The average of min and max values for package delay is utilized to compensate for the flight time caused by the delay associated with this package.

2.14 PMOD™-Compatible Interfaces

The Kintex UltraScale Development Board provides 4 PMOD™-Compatible Interfaces as shown in the following figure. Each pair of PMOD™-Compatible interfaces are placed in a single bank in order to optimize the FPGA resources used for a dual PMOD™-Compatible design.

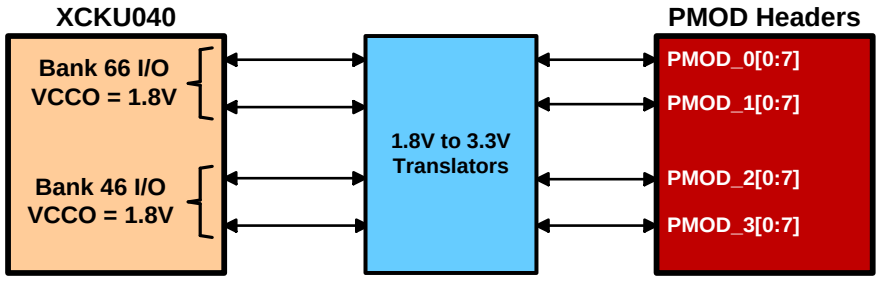


Figure 19 – PMOD Interfaces

The PMOD™-Compatible Interfaces are 8-bits wide and are connected to Bank 66 and Bank 46 of the XCKU040 device. The table below shows the connections to that are made to the FPGA for each of the four PMOD™-Compatible Interfaces.

Table 22 – PMOD™-Compatible Pin Assignments

PMOD™-Compatible Interface	FPGA Bank	FPGA Pin
PMOD1_0	66	J13
PMOD1_1	66	H13
PMOD1_2	66	A13
PMOD1_3	66	A12
PMOD1_4	66	C12
PMOD1_5	66	B12
PMOD1_6	66	D13
PMOD1_7	66	C13
PMOD™-Compatible Interface	FPGA Bank	FPGA Pin
PMOD2_0	66	F9
PMOD2_1	66	F8
PMOD2_2	66	E8
PMOD2_3	66	D8
PMOD2_4	66	E10
PMOD2_5	66	D10
PMOD2_6	66	G12
PMOD2_7	66	F12
PMOD™-Compatible Interface	FPGA Bank	FPGA Pin
PMOD3_0	46	F18
PMOD3_1	46	F19
PMOD3_2	46	G17
PMOD3_3	46	F17
PMOD3_4	46	G19
PMOD3_5	46	F20
PMOD3_6	46	C17
PMOD3_7	46	B17
PMOD™-Compatible Interface	FPGA Bank	FPGA Pin
PMOD4_0	46	C16
PMOD4_1	46	B16
PMOD4_2	46	B19
PMOD4_3	46	A19
PMOD4_4	46	A17
PMOD4_5	46	A18
PMOD4_6	46	D18
PMOD4_7	46	C18

2.15 DIP Switches and Push Buttons

The Kintex UltraScale Development Board provides an 8-position User DIP Switch, 4 User Push Button Switches, and 1 System Reset (SYS_RST) Push Button Switch.

The Dip Switches and Push Button Interfaces are connected to Bank 45 of the XCKU040 device. The table below shows the connection that are made to the FPGA for the Dip Switches, Push Buttons, and System Reset Interfaces.

Table 23 – DIP Switch Pin Assignments

DIP Switch Interface	FPGA Bank	FPGA Pin
SW8	45	J21
SW7	45	H21
SW6	45	G21
SW5	45	G22
SW4	45	L22
SW3	45	K22
SW2	45	H19
SW1	45	G20

Table 24 – Push Button Pin Assignments

Push Button Interface	FPGA Bank	FPGA Pin
PB4	45	K20
PB3	45	K21
PB2	45	L18
PB1	45	K18

Table 25 – System Reset Pin Assignment

System Reset Button	FPGA Bank	FPGA Pin
SYS_RST	45	N24

2.16 User LEDs

The Kintex UltraScale Development Board provides 8 user LEDs connected to Bank 46 of the XCKU040 device. The LED signals require the FPGA to drive the I/O high in order to illuminate them. The table below shows the connection that are made to the FPGA for the User LEDs.

Table 26 – User LED Pin Assignments

User LED Interface	FPGA Bank	FPGA Pin
LED7	46	H17
LED6	46	H18
LED5	46	E16
LED4	46	E17
LED3	46	E18
LED2	46	H16
LED1	46	G16
LED0	46	D16

2.17 System Monitor (SYSMON) Header

The UltraScale Architecture supports an on-chip system monitor. SYSMON monitors the physical environment via on-chip temperature and supply sensors, up to 17 external analog inputs, and an integrated analog-to-digital converter (ADC). An overview of the System Monitor primitive, SYSMON, is provided by Xilinx User Guide **UG580 - UltraScale Architecture System Monitor.**

The Kintex UltraScale Development Board supports System Monitor functionality via an on-board SYSMON header, J18 and selectable reference voltages via jumpers J28 and J29. The following figure depicts the implementation of the system monitor on the Kintex UltraScale Development Board.

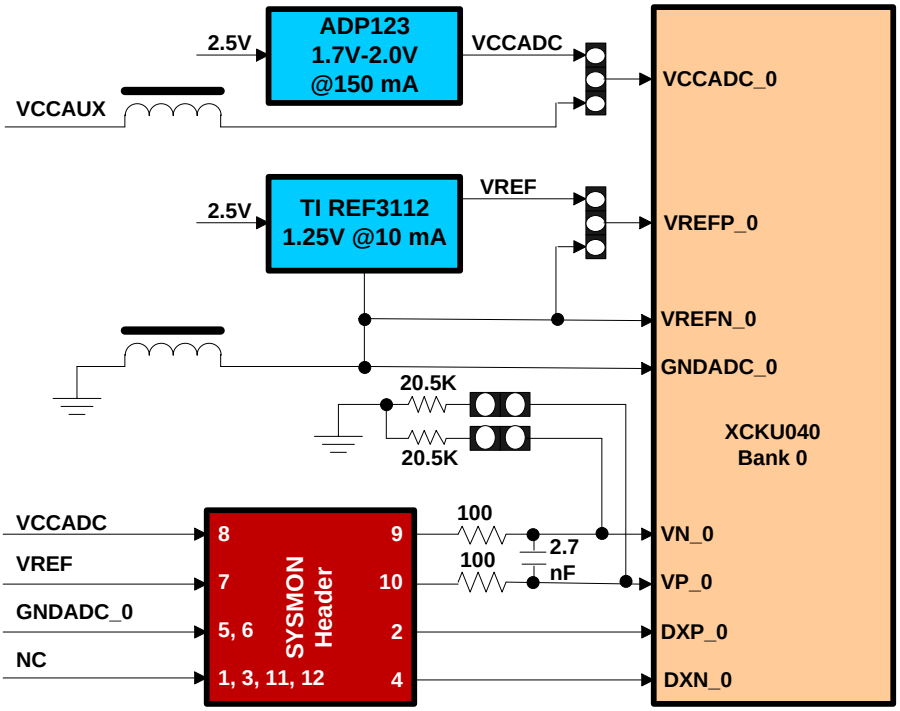


Figure 20 – Kintex UltraScale SYSMON Support Circuitry

Note 1: The JP28 jumper selects between a fixed VCCADC_0 of 1.8V (VCCAUX) or a variable VCCADC_0 of 1.7V to 2.0V using the Analog Devices ADP123 regulator.

Note 2: The JP29 jumper can be used to set the VREFP for external (output of the REF3112) or Internal operation.

Note 3: The SYSMON header is a 12 pin (2 x 6), 2.54mm male jumper header/connector.

Note 4: The J19 and J20 jumpers can be used to pull down ADC_V_N and ADC_V_P.

2.18 Board JTAG Chain

The Kintex UltraScale Development Board provides a couple methods for programming the XCKU040 device. There is an on-board **Digilent JTAG-SMT2** module for programming and configuration as well as a standard Xilinx JTAG header that accepts Xilinx programming cables.

A push button switch on the PCB, SW4, is implemented to allow the user to initiate a board reconfiguration by toggling the PROG_B. This push button is implemented near the blue DONE LED, D16. The blue DONE LED is an indicator to the operator that the FPGA has completed its configuration/programming cycle.

The JTAG jumper, J33 allows the FMC HPC module to be taken out of the JTAG chain in cases where the FMC HPC is not utilized or the FMC HPC module does not properly implement a JTAG solution. The following table show the configuration options for the JTAG jumper.

Table 27 – JTAG Jumper Options

JTAG JUMPER	FMC HPC In-Chain/ Not In-Chain
J33: Pins 1-2	FMC HPC In-Chain
J33: Pins 2-3	FMC HPC Not In-Chain

The following figure shows the JTAG chain on the Kintex UltraScale Development Board.

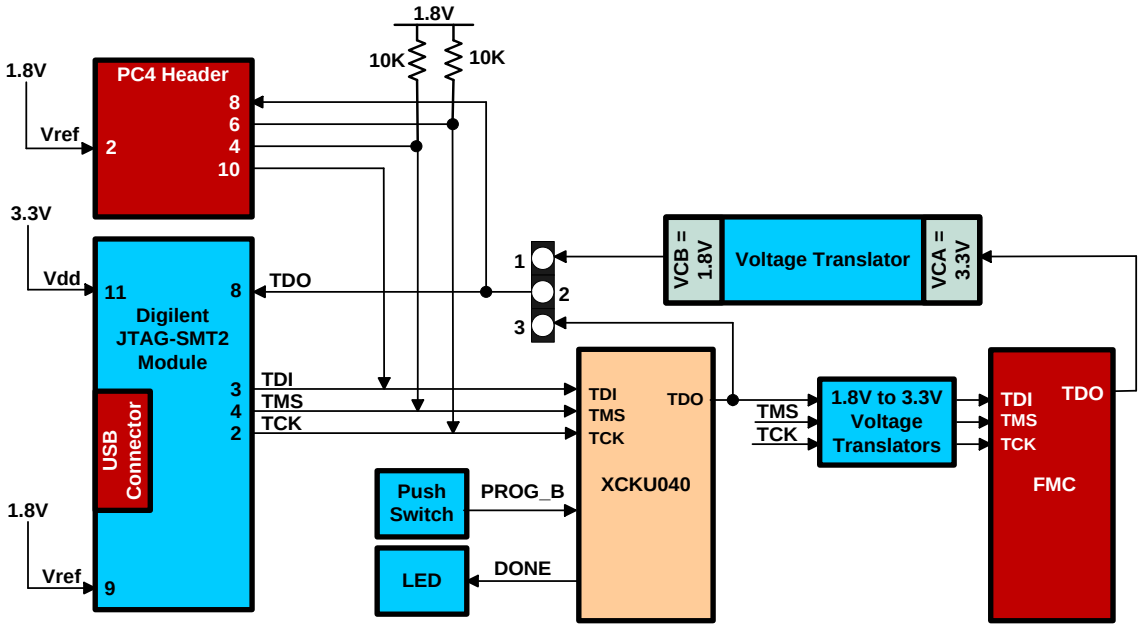


Figure 21 – Kintex UltraScale Development Board JTAG Chain

2.19 Board Power Supply

The Kintex UltraScale Development Board supplies the voltage rails listed in the following table. Sense feedback is implemented for all power rails.

Table 28 – Board Power Supply Requirements

Voltage Rails	Usage	Supported Current
0.95V	VCCINT, VCCBRAM, and VCCINT_IO	5A
1.2V	DDR4 and VCCO	4A
1.8V	VCCAUX, MGTVCCAUX, VCCAUX_IO, VCCO, and FMC slot	5A
2.5V	VCCO, on-board devices, DDR4 VPP, and FMC slot	5A
3.3V	VCCO, on-board devices, and FMC slot	5A
1.0V (Analog)	MGTAVCC	5A
1.2V (Analog)	MGTAVTT, MGTAVTTRCAL	4A

The following figure shows the power connections on the Kintex UltraScale development board.

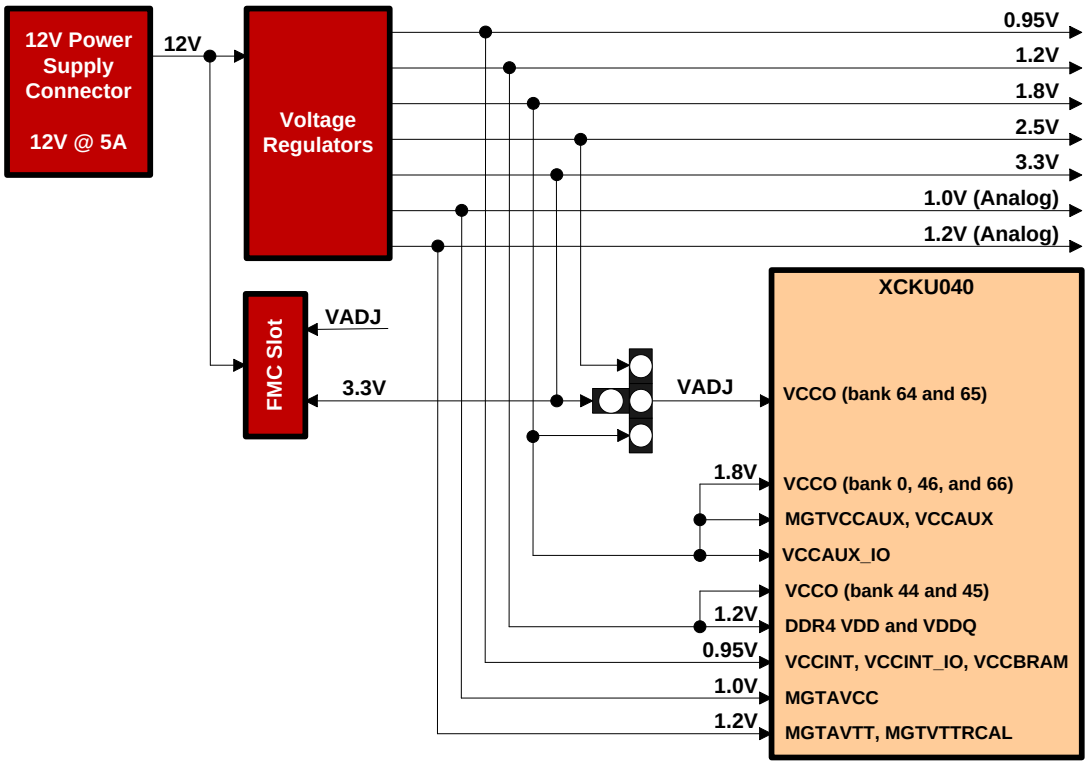


Figure 22 – Kintex UltraScale Development Board Power Supply

The voltage rails provided on the Kintex UltraScale Development Board are powered by **International Rectifier** devices.

Many of the rails are implemented using the **IR38060 SupIRBuck™**. This device is a highly integrated 6A synchronous buck regulator with PMBUS Interface. These devices are programmable through the PMBUS Interface, but are each initially programmed at the factory with the required voltages. The voltage and current of these devices are capable of being monitored by the **International Rectifier PowIRCenter**.

In order to program/monitor the **IR38060 SupIRBuck™** through the **PowIRCenter** a jumper shunts needs to be installed and several jumper shunts need to be removed.

For programming:

Jumper J22 – Shunt installed: Disable the **International Rectifier** power regulators.
Jumper J34 / J35 / J36 – Shunts removed: Remove the **International Rectifier** PMBUS signals from FPGA.

For normal operation:

Jumper J22 – Shunt removed: Enable the **International Rectifier** power regulators.
Jumper J34 / J35 / J36 – Shunts installed: Add the **International Rectifier** PMBUS signals to FPGA for monitoring PMBUS Interface.

The 2.5V and 3.3V rails are implemented using the **IR3892 SupIRBuck™.** This device is a highly integrated dual output 6A/phase synchronous buck regulator.

Each of the individual rails that are implemented on the Kintex UltraScale Development Board power an indicator LED that illuminates when the rail is valid. Please review to the schematic and PCB to identify the LEDs and the rails that are associated with them.

2.19.1 Power Input – J21 and SW10

The Kintex UltraScale Development Board is powered by attaching a compatible 12V power supply to power connector, J21, with control via the power switch, SW10.

Sliding power switch, SW10, to the ON position as labelled on the PCB will pass the 12V from the power supply to the board. Sliding the power switch, SW10, to the OFF position as labelled on the PCB will remove the 12V power supply from the board and effectively turn OFF all power to the board except for the provided by the USB-UART through VIO.

J21 is a 12V 2x3 6-pin connector which is NOT ATX COMPATIBLE. It is recommended that the maximum input voltage not exceed 13.2V, (12V + 10%) to minimize the component stress and thereby increasing product operational life.

The power supply shipped from Avnet is Avnet part number AES-SLP-12V5A-G. This power supply is rated at 12V, 5.0 Amps and is recommended for use with the Kintex UltraScale Development Board.

2.19.2 VADJ Selection

The Kintex UltraScale Development Board supports a configurable VADJ voltage via a multi-position jumper. The VADJ voltage powers Bank 64 and Bank 65 on the XCKU040 device. Proper selection of this voltage is necessary to ensure the interfaces that exist on these FPGA banks operate correctly.

The configurable VADJ voltage is selected via a shunt placed on the on-board jumper, JP13. This jumper allows the user to configure VADJ to 1.8V, 2.5V, or 3.3V depending on the desire application. A major driver of the selection of this voltage will be the use of the LVDS Display interface and the FMC HPC interface.

The following figure is a snippet from the schematic depicting the options for setting VADJ. Included is a special RED SHUNT which is specific to shunting VADJ as it is capable of supporting the current requirements of the FMC HPC VADJ rail. Please ensure that this special shunt is installed in the correct position.

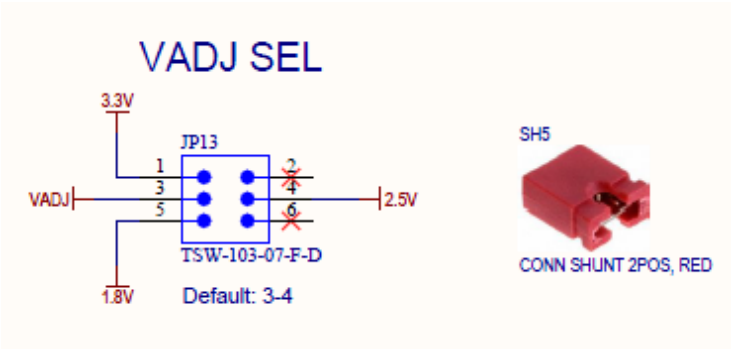


Figure 23 – VADJ Voltage Selection and Shunt

The following table illustrates the required shunt position to versus the desired voltage output for VADJ.

Table 29 – VADJ Select Jumper Options

VADJ Jumper	VADJ Voltage
JP13: Pins 3-1	3.3V
JP13: Pins 3-4	2.5V
JP13: Pins 3-5	1.8V

2.20 Thermal Management

An active heat sink is used to dissipate heat from the XCKU040 device on the Kintex UltraScale Development Board. A Cool Innovations heat sink (PN: **3-121202UBFA**) and a Sunon 5V fan (PN: **MC30100V1-000U-A99**) are assembled together and shipped with the Kintex UltraScale Development Board.

The active heat sink is powered by connecting a three position connector to the 5V fan mating connector on the Kintex UltraScale Development Board at JP1. This 3-pin keyed connector is .100” pitch and has the 5V conductor as pin 2 on the connector. The fan supplied with the Kintex UltraScale Development Boards mates correctly to JP1.

For aggressive applications that utilize large amounts of XCKU040 FPGA fabric resources it is recommended that an accurate worst-case power analysis be performed to avoid the pitfalls of overdesigning or under designing your product’s power or cooling system, using the Xilinx Power Estimator (XPE).

3 Mechanical

The following figure shows the approximate component placements of the Kintex UltraScale Development Board. The component placements provide optimal PCB routing based on the bank pin assignments used on the Kintex UltraScale Development Board.

Note: The FMC slot extends away from the Kintex UltraScale Development Board.

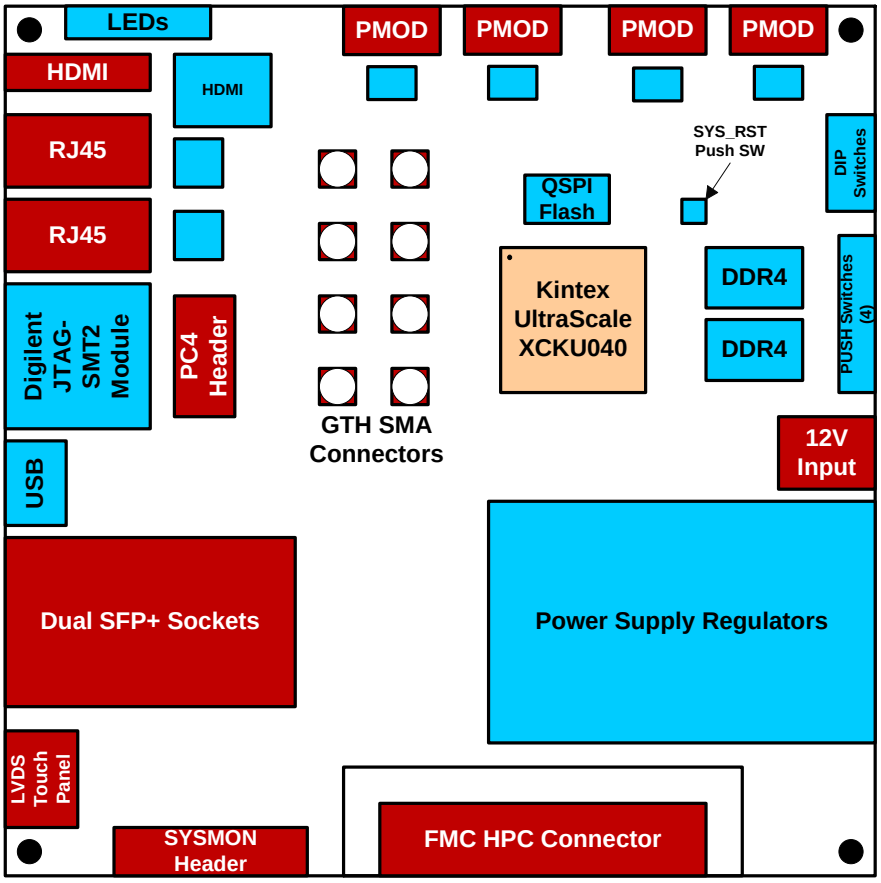


Figure 24 – Board Component Placement

3.1 Mechanical Dimensions

The Kintex UltraScale Development Board measures 6.9” x 6.0” (175.26mm x 152.4mm). Other pertinent dimensions are presented in the following figure.

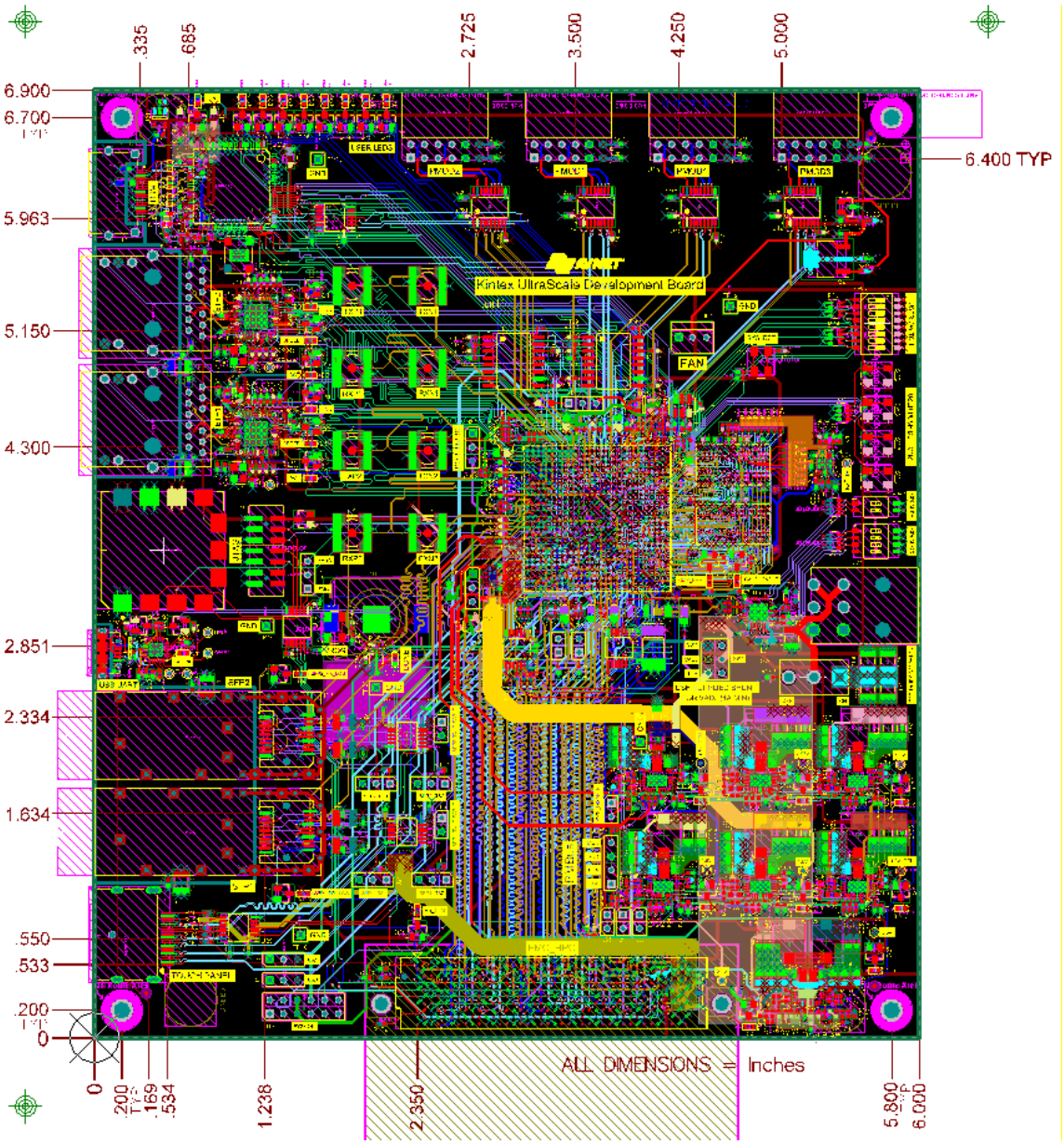


Figure 25 – Board Mechanical Dimensions - Top

4 Revision History

Revision Date	Revision #	Reason for Change
12/17/2015	1.0	Initial Release