65 W PAG2P-2S HF-ACF (REF_65W_HFACF_PAG2_PA) adapter board test report

Devices – CYPAP212A1-14SXI and CYPAS212A1-32LQXQ

About this document

Scope and purpose

This document provides power management test results of the 65 W PAG2P-2S HF-ACF REV3 Solution Demo Board. The tests were performed on REV3 HF-ACF board, which is equipped with Infineon CYPAP212A1-14SXI on the primary, and CYPAS212A1-32LQXQ on the secondary section of the converter.

Intended audience

This document is intended for customers and FAEs using the EZ-PD™ PAG2P/PAG2S high-frequency active clamp flyback REF_65W_HFACF_PAG2_PA hardware.

Table of contents

1 Introduction

This test report captures the performance of PAG2S (power adapter generation 2 – secondary controller) PAG2P (primary controller) high-frequency active clamp flyback (ACF)-based USB PD, 65-W adapter solution demo kit. This is a high power-dense form-factor (32 W/in^3) and an efficient (>94.5%) adapter solution kit.

EZ-PD™ PAG2P CYPAP212A1-14SXI (power adapter generation 2 primary) is Infineon's second-generation integrated primary-side start-up controller for AC/DC applications targeting the mobile power adapter segment. PAG2P interfaces with the AC mains rectified output on the primary side and receives the necessary PWM signal from the secondary side to provide a regulated output voltage. PAG2P is designed to complement a secondary controlled AC/DC flyback converter topology. In this topology, the secondary controller (PAG2S) performs the voltage and current regulation. PAG2P is responsible for initiating the start-up function, driving the primary side FET, and responding to fault conditions.

EZ-PD™ PAG2S CYPAS212A1-32LQXQ is an integrated secondary-side PWM controller and USB Power Delivery (USB PD) controller. PAG2S integrates the secondary side synchronous rectifier (SR), pulse-width modulator (PWM), and active clamp flyback (ACF) control. PAG2S is targeted towards USB-C chargers; it fits well into high-efficiency AC-DC flyback designs with USB PD, Qualcomm Quick Charge, and other standard charging protocols. PAG2S CYPAS212 also supports USB PD Extended Power Range (EPR) mode.

Figure 1 shows the application diagram for an adapter in a secondary-side-controlled flyback converter topology together with ACF operation. In addition to being the secondary controller, PAG2S also controls ACF operation to achieve higher efficiency and get ZVS operation. PWM and ACF signals are transferred to the primary side through the same pulse-edge transformer. PAG2S uses time multiplexing to transfer PWM and ACF signals. The following are the benefits of integrating the ACF on the secondary side over the traditional primary side control:

- Programmable ON time for high side FET to achieve optimized efficiency for different solutions.
- Achieve non-complementary ACF operation.
- Programmable high side ON time to reach true ZVS operation.

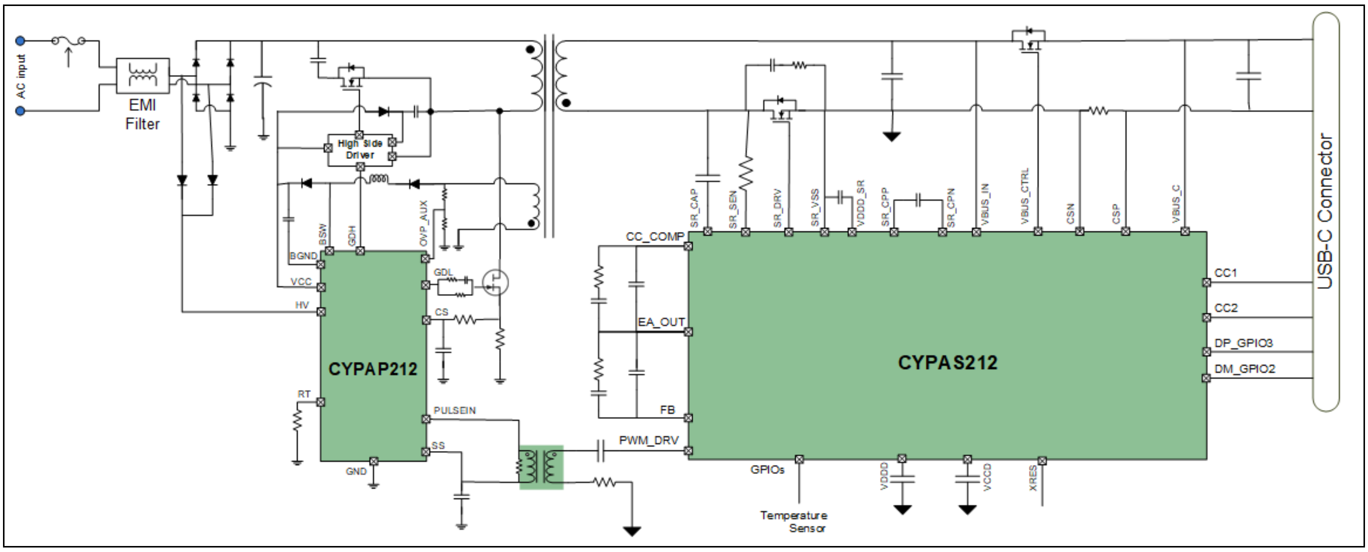


Figure 1 Application diagram for a power adapter in a secondary-side-controlled flyback converter topology together with ACF operation

2 Test setup

2.1 Device under test (DUT)

The device under test is the 65 W PAG2P-2S HF-ACF Solution Demo Board.

Table 1 DUT hardware and software configurations

DUT contents	Description
Hardware – configuration	
PAG2P+PAG2S HFACF 65 W Solution Board V3	Rev. 3
Firmware	
Firmware repo	vach_hf_pa_ver4

Dimensions (in mm): 34.29 × 31.97 × 30.46 (L × W × H)

Figure 2 65 W HF-ACF solution board – Isometric view

Figure 3 65 W HF-ACF solution board – Top view

2.2 DUT setup

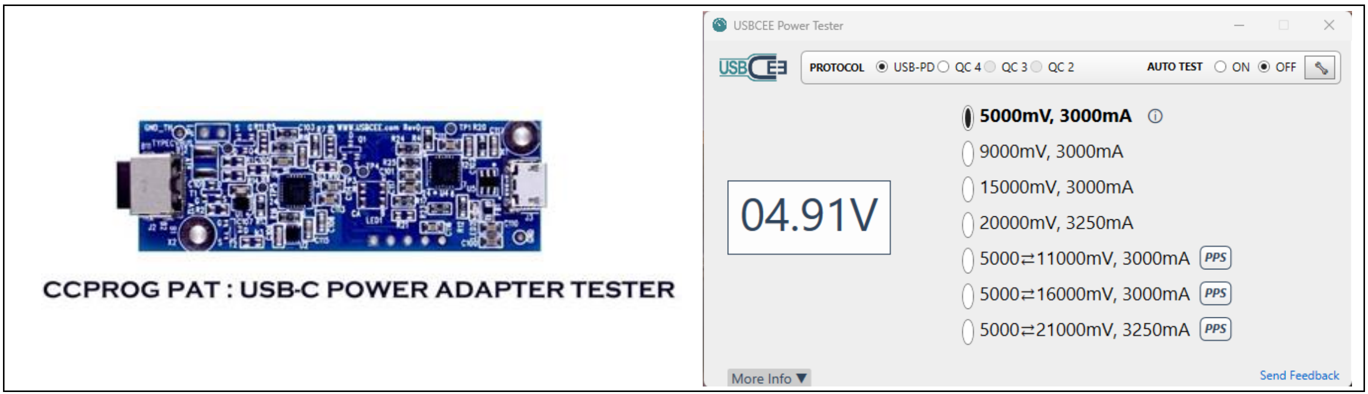


Figure 4 Physical CCGPROG PAT and Power Tester UI

The DUT is connected to a power adapter tester (PAT) (CCPROG PAT) through a USB Type-C cable. After successful connection, the PAT UI performs a PDO discovery and displays the same on the UI. The solution kit is pre-configured with the following 4 PDOs:

- PDO 1: 5 V, 3 A FIXED
- PDO 2: 9 V, 3 A FIXED
- PDO 3: 15 V, 3 A FIXED
- PDO 4: 20 V, 3.25 A FIXED

Choose the suitable pre-configured PDO or configure newly using Infineon's USB EZ-PD™ Configuration Utility. Tests in the following sections use the pre-configured PDOs.

For more information on PAT tester, see USBCEE.

2.3 Test equipment

Table 2 lists the test equipments to measure the efficiency, ripple, regulation, and transient response.

Table 2 Test equipments

Test setup	Description
Oscilloscope name	Tektronix MDO 034
Power meter	Yokogawa WT310E/Chroma 66205
Digital multimeter (V_o & I_o)	Keysight 34465A
Programmable AC source	Chroma 61501/61502
Electronic load	Chroma 63113A/63103
Thermal camera	Flir E75
Automation software	LabView

3 Power management test results

Note: All the tests mentioned in this report are carried out under the open-frame condition.

3.1 Efficiency and no-load consumption

Table 3 Efficiency and no-load consumption results

Parameter	Standard (minimum value)		Unit	Test condition	Test result	
	DoE Level VI	CoCv5 Tier 2			115 V_{ac}, 60 Hz	230 V_{ac}, 50 Hz
Four-point average efficiency (average of 25%, 50%, 75%, 100% load)	81.39	81.84	%	V_o = 5 V_{dc}, I_o = 3 A	92.42	91.19
	86.62	87.30	%	V_o = 9 V_{dc}, I_o = 3 A	93.50	93.42
	87.73	88.85	%	V_o = 15 V_{dc}, I_o = 3 A	93.69	94.26
	88	89	%	V_o = 20 V_{dc}, I_o = 3.25 A	93.72	94.52
CoCv5 Tier 2 10% load efficiency	-	72.48	%	V_o = 5 V_{dc}, I_o = 0.3 A	89.59	82.80
	-	77.30	%	V_o = 9 V_{dc}, I_o = 0.3 A	90.27	87.75
	-	78.85	%	V_o = 15 V_{dc}, I_o = 0.3 A	89.84	88.19
	-	79	%	V_o= 20 V_{dc}, I_o= 0.325 A	90.28	89.59
	Standard (maximum value)					
No load consumption	100	75	mW	No USB sink attached	24	29

Note:

1. *Peak efficiency: 94.86% (at 230 V_{ac}-50 Hz, 20 V-3.25 A)*
2. *Full load efficiency at 90 V_{ac}: 92.71% (at 90 V_{ac}-47 Hz, 20 V-3.25 A)*
3. *V_{out} for efficiency calculations is measured across V_{bus_C} at board end with 15 minutes warmup.*
4. *Variation of ±0.5% in efficiency can be observed across units.*

Table 4 lists the instruments used to capture the efficiency data.

Table 4 Instruments

Instruments	Model number
AC source	GWinstek ASR2100
Power meter	Hioki PW3335
Input current (I_{IN} and I_{OUT}) measurement shunt	Vishay Y14730R00500B0R
Electronic load	GwINSTEK PEL-3021
Data logger (I_{IN}, V_{IN}, V_{BUS}, and I_{OUT})	Keysight 34970 A

Table 5 EuP Lot6 V1

Parameter	Test condition	Max P_{in} (W)	Test result			
			115 V_{ac}, 60 Hz		230 V_{ac}, 50 Hz	
			P_{in} (W)	Efficiency (%)	P_{in} (W)	Efficiency (%)
Efficiency at 250 mW load	$V_o = 5\ V_{dc}$ $I_o = 50$ mA	480	0.321	78.197	0.332	75.642
	$V_o = 9\ V_{dc}$ $I_o = 27.78$ mA		0.348	73.004	0.342	74.204
	$V_o = 15\ V_{dc}$ $I_o = 16.67$ mA		0.365	72.237	0.354	74.439
	$V_o = 20\ V_{dc}$ $I_o = 12.5$ mA		0.378	68.783	0.358	72.330

Table 6 EuP Lot6 V2

Parameter	Test condition	Max P_{in} (W)	Test result			
			115 V_{ac}, 60 Hz		230 V_{ac}, 50 Hz	
			P_{in} (W)	Efficiency (%)	P_{in} (W)	Efficiency (%)
Efficiency at 180 mW load	$V_o = 5\ V_{dc}$ $I_o = 36$ mA	300	0.247	73.606	0.255	71.434
	$V_o = 9\ V_{dc}$ $I_o = 20$ mA		0.257	71.739	0.283	65.624
	$V_o = 15\ V_{dc}$ $I_o = 12$ mA		0.269	67.751	0.264	69.205
	$V_o = 20\ V_{dc}$ $I_o = 9$ mA		0.283	65.961	0.271	68.829

Table 7 Efficiency from 1% to 10% load at 115 V_{ac}, 60 Hz

Load %	V_{ac} (V)	Frequency (Hz)	P_{in} (W)	V_{out} (V)	I_{out} (A)	P_o (W)	Efficiency (%)
1	115	60	0.887	19.929	0.033	0.652	73.47
2			1.721	19.925	0.065	1.301	75.59
3			2.381	19.927	0.097	1.938	81.37
4			3.070	19.925	0.131	2.604	84.84
5			3.730	19.924	0.163	3.240	86.87
6			4.420	19.923	0.195	3.891	88.03
7			5.100	19.923	0.227	4.530	88.83
8			5.800	19.924	0.261	5.194	89.56
9			6.480	19.922	0.292	5.826	89.91
10			7.180	19.923	0.325	6.480	90.25

Table 8 Efficiency from 10% to 100% load at 115 V_{ac}, 60 Hz

Load %	V_{ac} (V)	Frequency (Hz)	P_{in} (W)	V_{out} (V)	I_{out} (A)	P_o (W)	Efficiency (%)
10	115	60	7.183	19.927	0.325	6.480	90.21
20			13.908	19.925	0.651	12.967	93.23
30			20.855	19.923	0.977	19.458	93.30
40			27.783	19.918	1.302	25.941	93.37
50			34.610	19.915	1.628	32.420	93.67
60			41.480	19.912	1.954	38.902	93.78
70			48.350	19.910	2.278	45.363	93.82
80			55.250	19.909	2.604	51.850	93.85
90			62.140	19.907	2.930	58.325	93.86
100			69.080	19.904	3.255	64.797	93.80

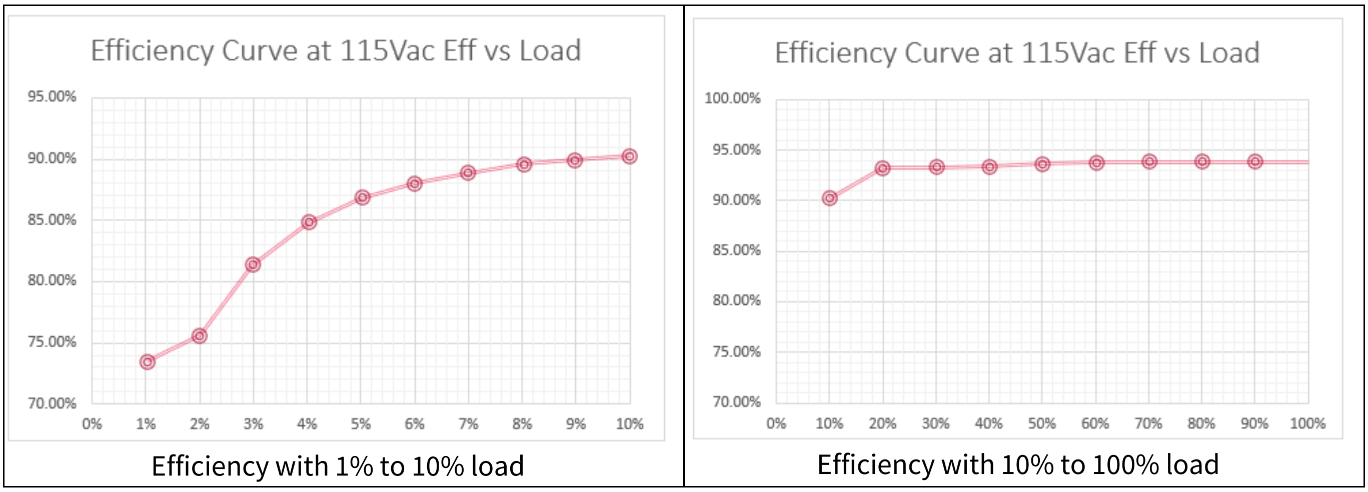


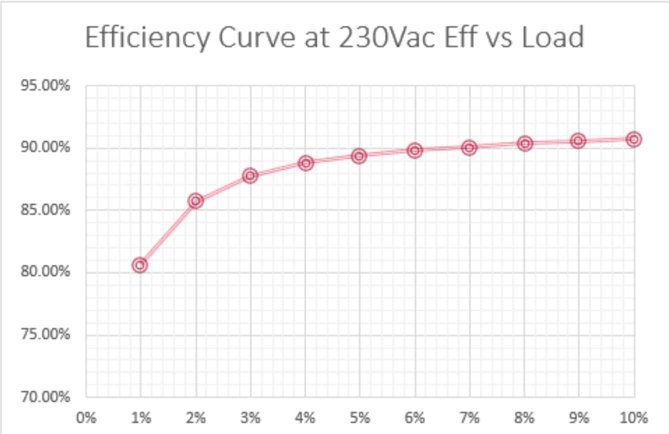
Figure 5 Efficiency curve at 115 V_{ac}, 60 Hz

Table 9 Efficiency from 1% to 10% load at 230 V_{ac}, 50 Hz

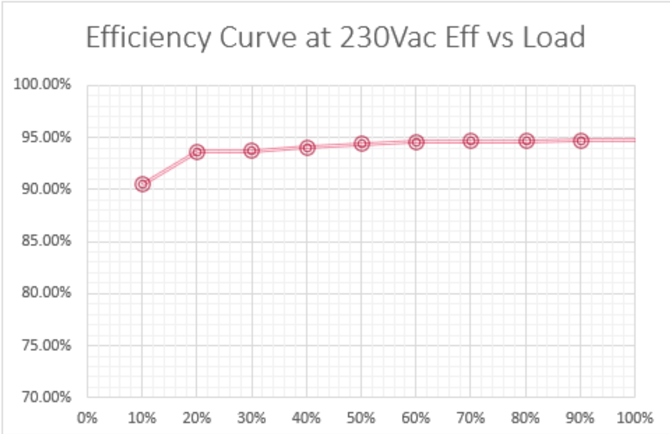
Load %	V_{ac} (V)	Frequency (Hz)	P_{in} (W)	V_{out} (V)	I_{out} (A)	P_o (W)	Efficiency (%)
1	230	50	0.799	19.928	0.032	0.644	80.64
2			1.510	19.923	0.065	1.294	85.72
3			2.206	19.924	0.097	1.936	87.74
4			2.927	19.922	0.130	2.599	88.79
5			3.615	19.922	0.162	3.232	89.40
6			4.325	19.922	0.195	3.885	89.83
7			5.021	19.920	0.227	4.522	90.05
8			5.740	19.921	0.260	5.188	90.39
9			6.430	19.919	0.292	5.821	90.53
10			7.140	19.920	0.325	6.477	90.72

Table 10 Efficiency from 10% to 100% load at 230 V_{ac} 50 Hz

Load %	V_{ac} (V)	Frequency (Hz)	P_{in} (W)	V_{out} (V)	I_{out} (A)	P_o (W)	Efficiency (%)
10	230	50	7.170	19.929	0.325	6.486	90.46
20			13.850	19.924	0.651	12.969	93.64
30			20.770	19.921	0.977	19.458	93.68
40			27.590	19.917	1.302	25.942	94.03
50			34.350	19.914	1.628	32.422	94.39
60			41.150	19.912	1.954	38.902	94.54
70			47.930	19.909	2.278	45.361	94.64
80			54.790	19.907	2.605	51.851	94.64
90			61.570	19.906	2.930	58.327	94.73
100			68.360	19.903	3.256	64.801	94.79



Efficiency with 1% to 10% load



Efficiency with 10% to 100% load

Figure 6 Efficiency curve at 230 V_{ac}, 50 Hz

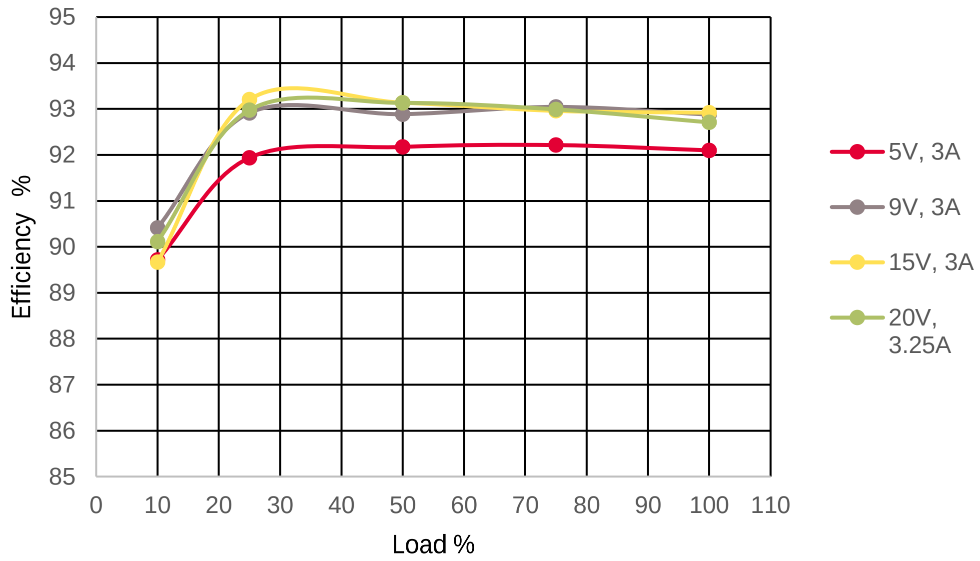


Figure 7 **Efficiency at 90 V_{ac}, 47 Hz**

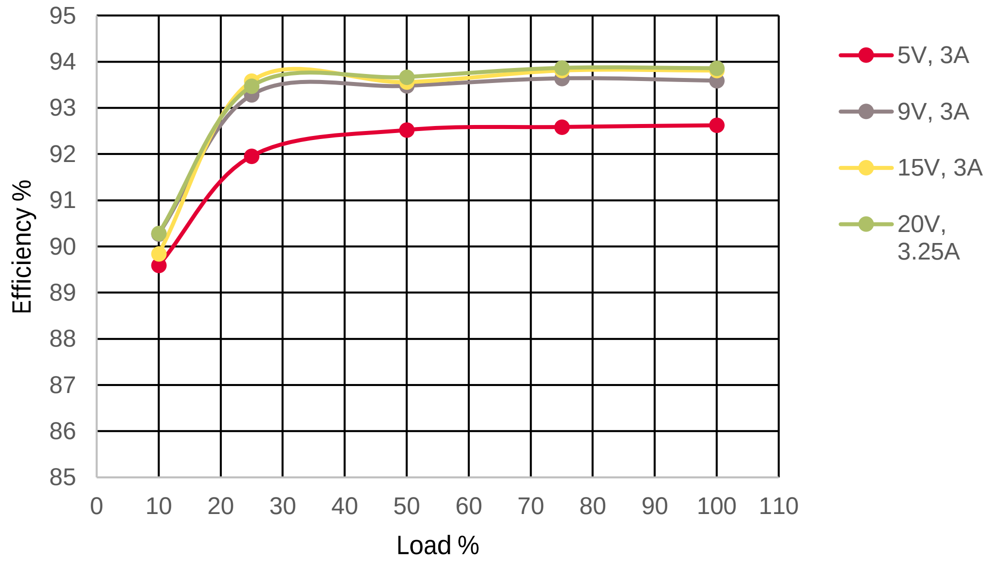


Figure 8 **Efficiency at 115 V_{ac}, 60 Hz**

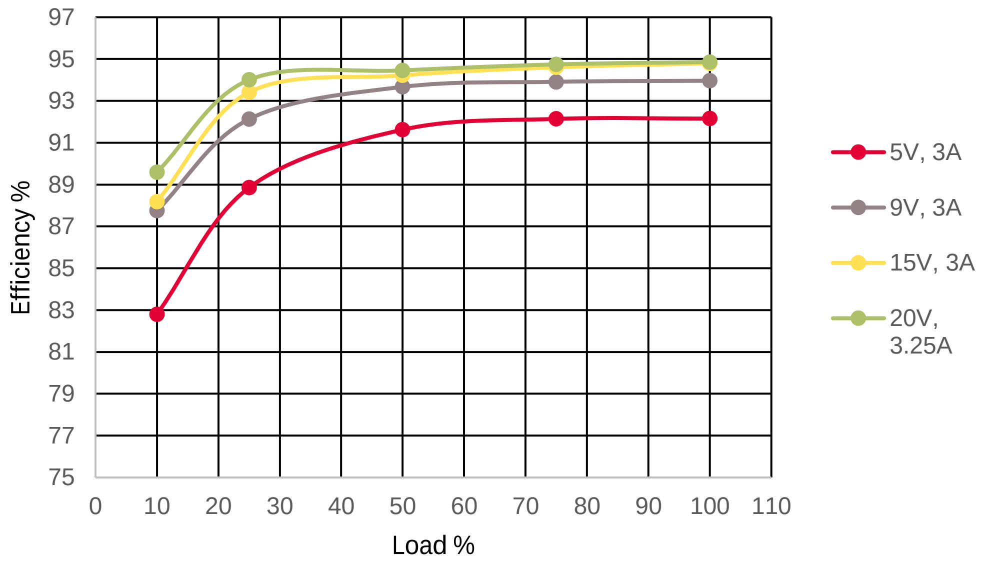


Figure 9 **Efficiency at 230 V_{ac}, 50 Hz**

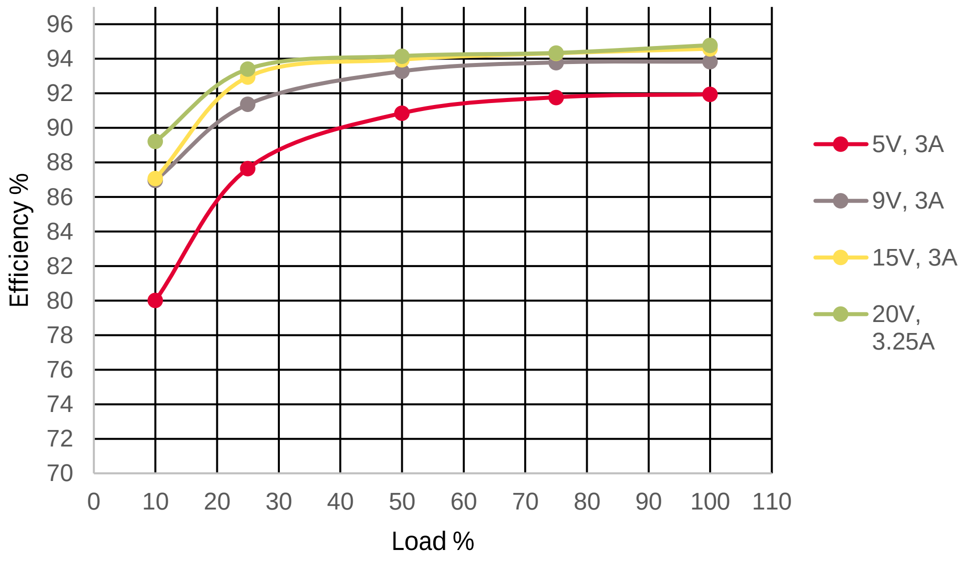


Figure 10 **Efficiency at 265 V_{ac}, 63 Hz**

Note:

1. *CoC Tier 2 limit for four-point average is 89%.*
2. *CoC Tier 2 limit for 10% load is 79%.*

Table 11 Full load efficiency at different line conditions

Sl.no	V_{ac} (V)	Frequency (Hz)	P_{in} (W)	V_{out} (V)	I_{out} (A)	P_o (W)	Efficiency (%)	Four-point average efficiency (%)	CoC Tier2	DOE Level VI	Full load switching frequency (kHz)
1	90	47	7.211	19.968	0.325	6.498	90.11	-	79	-	110
2	90	47	17.474	19.970	0.814	16.246	92.98	92.951	89	88	
3	90	47	34.900	19.962	1.628	32.503	93.13				
4	90	47	52.390	19.953	2.442	48.718	92.99				
5	90	47	70.040	19.944	3.256	64.933	92.71				
6	115	60	7.195	19.971	0.325	6.496	90.284	-	79	-	135
7	115	60	17.369	19.965	0.813	16.235	93.470	93.716	89	88	
8	115	60	34.69	19.959	1.628	32.493	93.668				
9	115	60	51.89	19.951	2.441	48.707	93.866				
10	115	60	69.17	19.942	3.255	64.922	93.858				
11	230	50	7.25	19.972	0.325	6.495	89.589	-	79	-	120
12	230	50	17.27	19.966	0.813	16.235	94.005	94.517	89	88	
13	230	50	34.4	19.960	1.628	32.493	94.456				
14	230	50	51.41	19.952	2.441	48.708	94.745				
15	230	50	68.43	19.941	3.255	64.913	94.860				
16	264	63	7.28	19.971	0.325	6.495	89.214	-	79	-	124
17	264	63	17.38	19.967	0.813	16.234	93.408	94.172	89	88	
18	264	63	34.51	19.959	1.628	32.493	94.155				
19	264	63	51.63	19.952	2.441	48.708	94.340				
20	264	63	68.49	19.943	3.255	64.919	94.786				

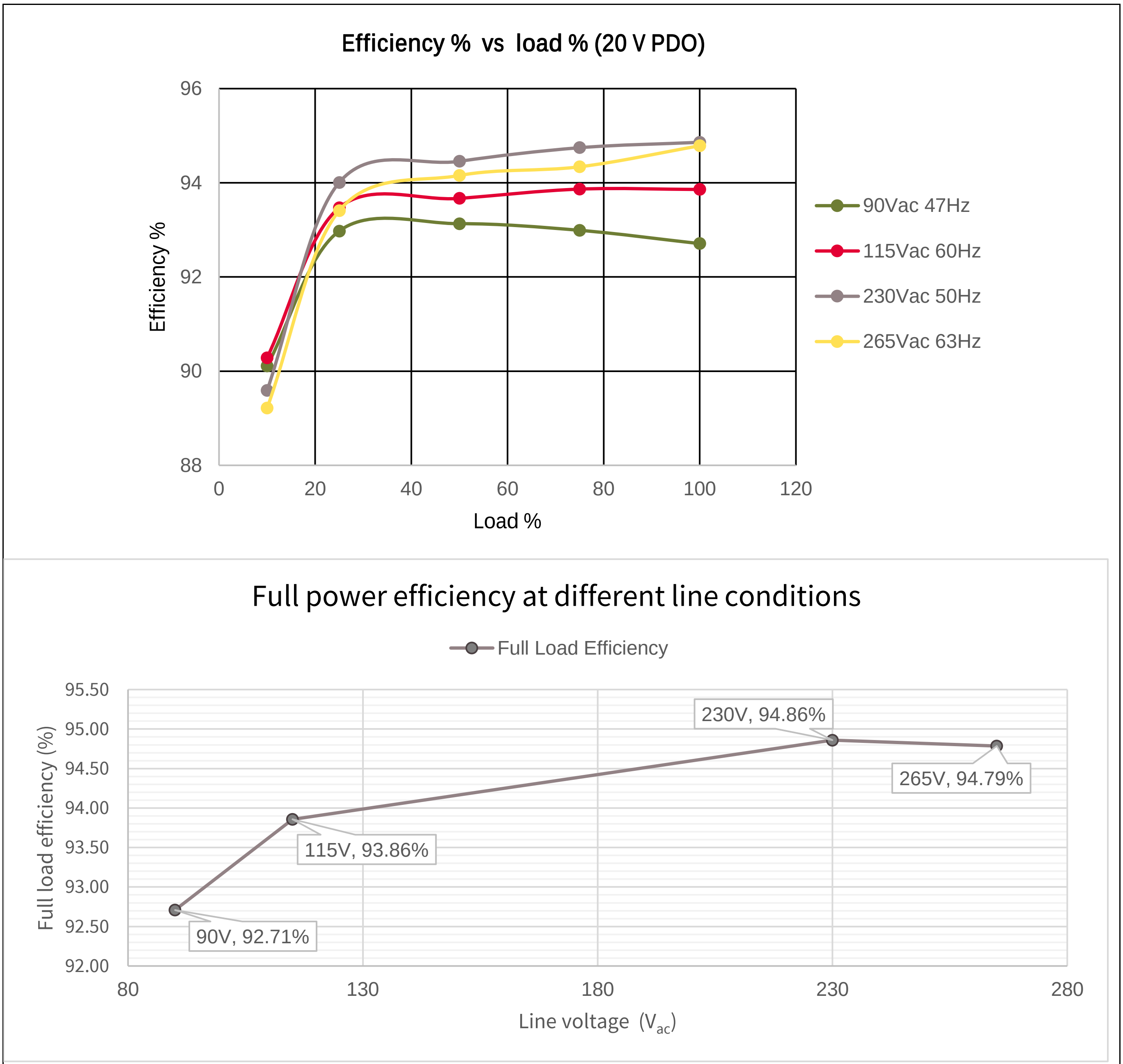


Figure 11 Full power efficiency at different line conditions

3.2 Standby power consumption

Table 12 Standby power consumption across line conditions

V_{in} (V_{ac})	90 V_{ac}, 47 Hz	115 V_{ac}, 60 Hz	230 V_{ac}, 50 Hz	265 V_{ac}, 63 Hz
Input power (mW)	24 mW	24 mW	29 mW	29 mW

Note: There should be 15 minutes of warmup time before starting to measure standby power.

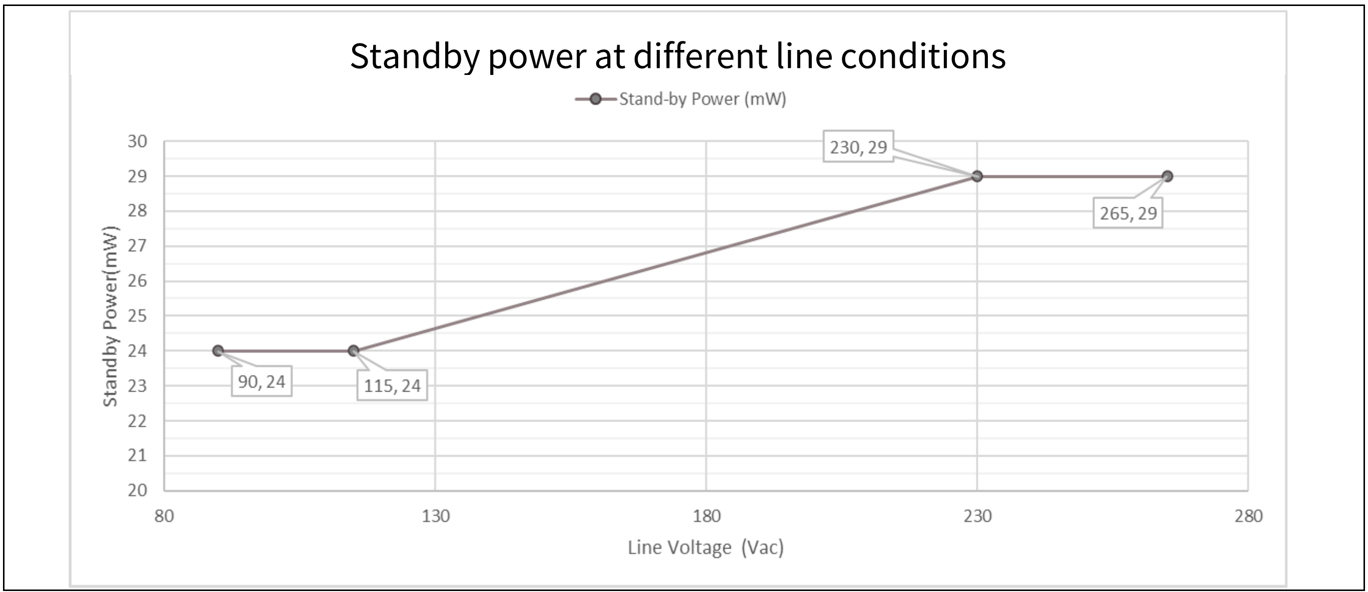


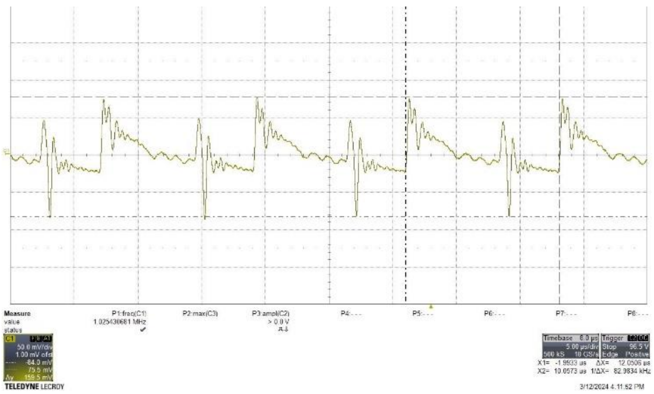
Figure 12 Standby power consumption

Note: The measurement was taken using the WTViewerEfree software with line filter ON.

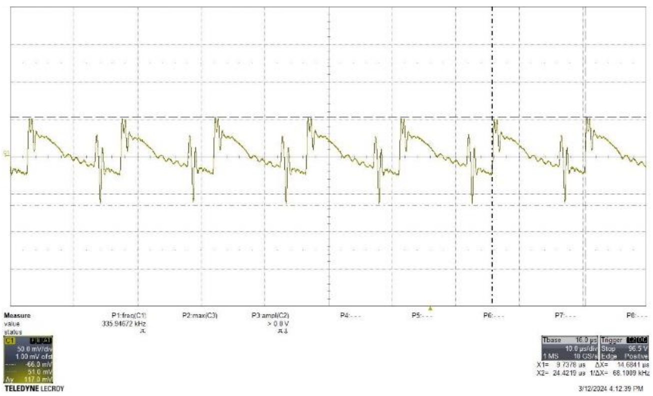
3.3 Output voltage ripple peak-to-peak

Note: 1. The ripple measurement is done at board end using a lecroy probe. Refer PK6-5MM-105.

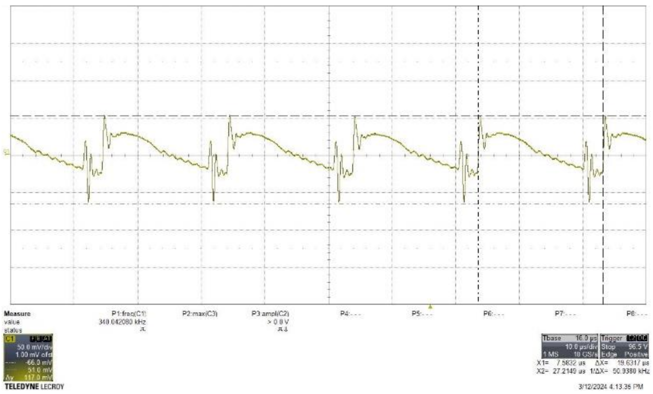
2. The waveforms are recorded while keeping the oscilloscope within the 20 MHz bandwidth limitation.



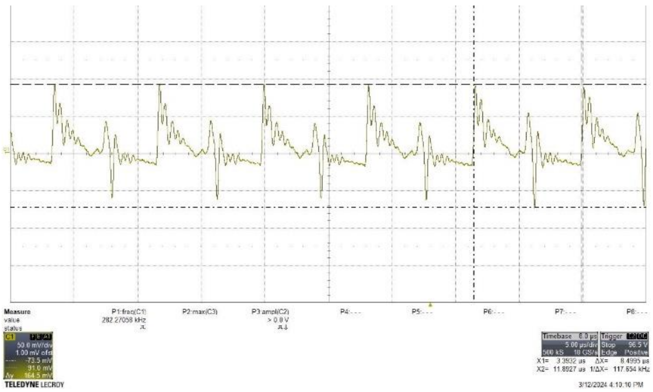
90 V_{ac}, 5 V, 3 A, ripple (p-p) = 159.5 mV



90 V_{ac}, 9 V, 3 A, ripple (p-p) = 117 mV

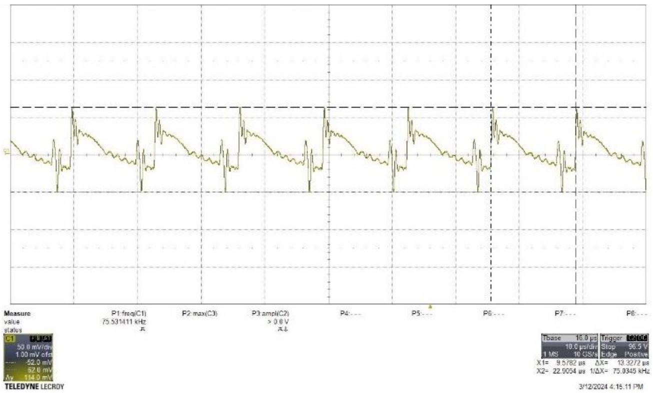


90 V_{ac}, 15 V, 3 A, ripple (p-p) = 117 mV

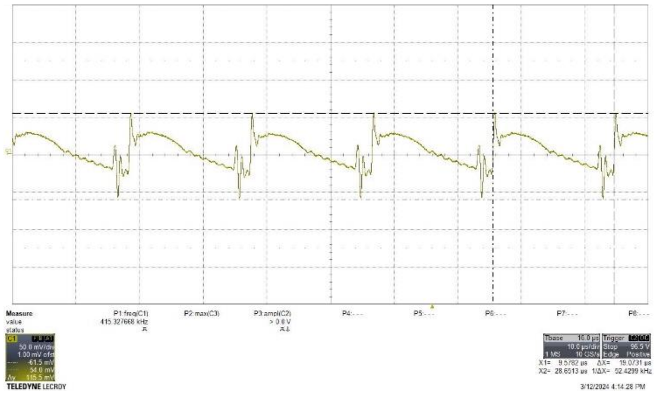


90 V_{ac}, 20 V, 3.25 A, ripple (p-p) = 164.5 mV

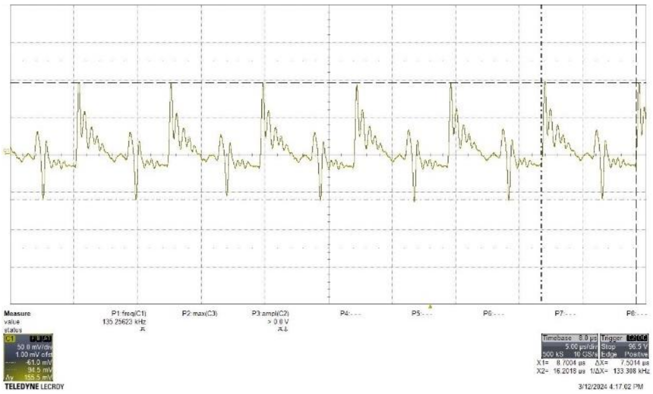
Figure 13 Ripple at 90 V_{ac}, 47 Hz (CH1: V_{bus_C})



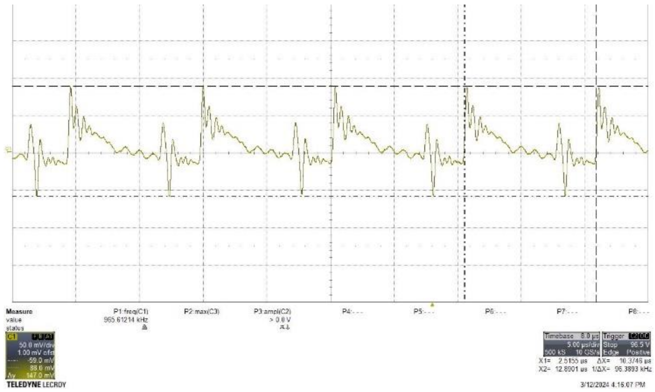
115 V_{ac}, 5 V, 3 A, ripple (p-p) = 114 mV



115 V_{ac}, 9 V, 3 A, ripple (p-p) = 115.5 mV



115 V_{ac}, 15 V, 3 A, ripple (p-p) = 155.5 mV



115 V_{ac}, 20 V, 3.25 A, ripple (p-p) = 147 mV

Figure 14 Ripple at 115 V_{ac}, 60 Hz (CH3: V_{bus_c})

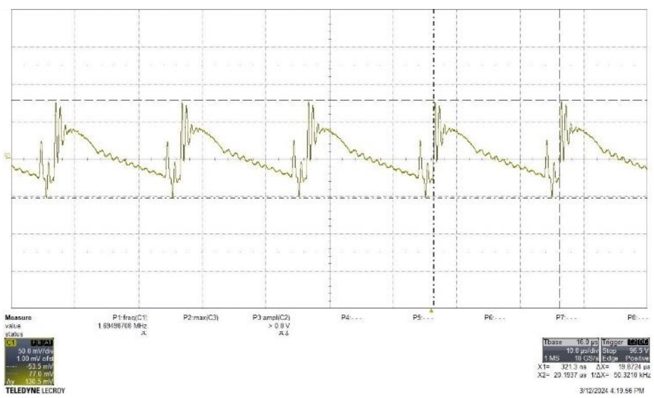
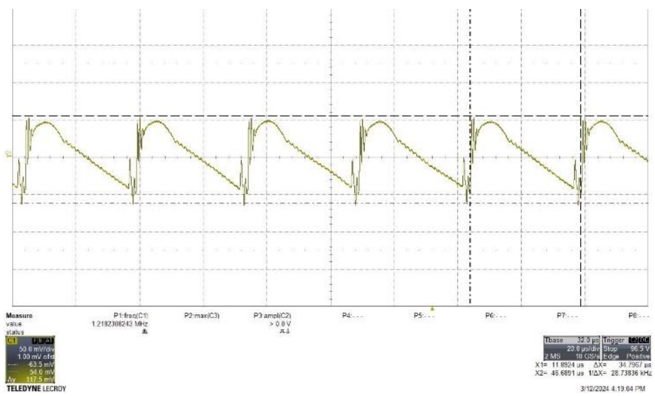
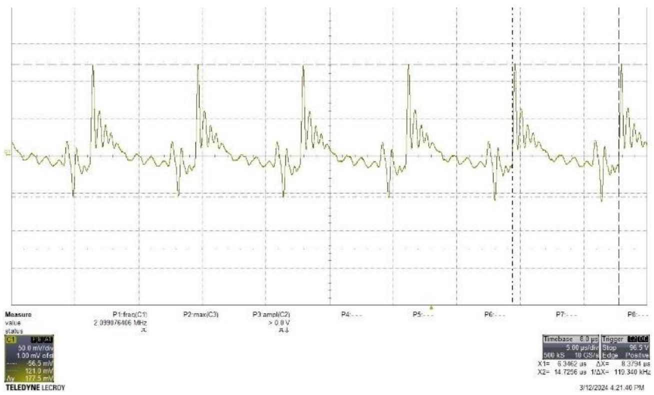
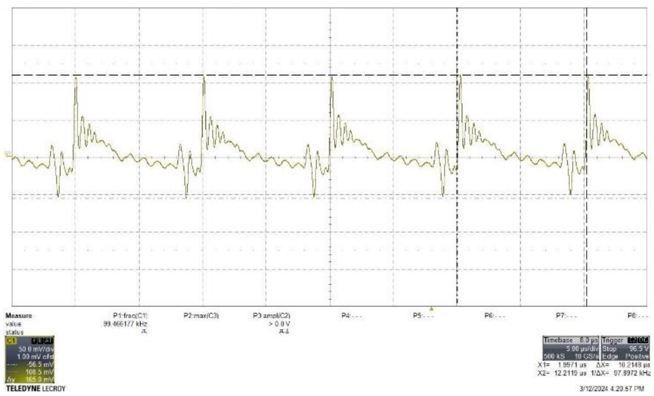
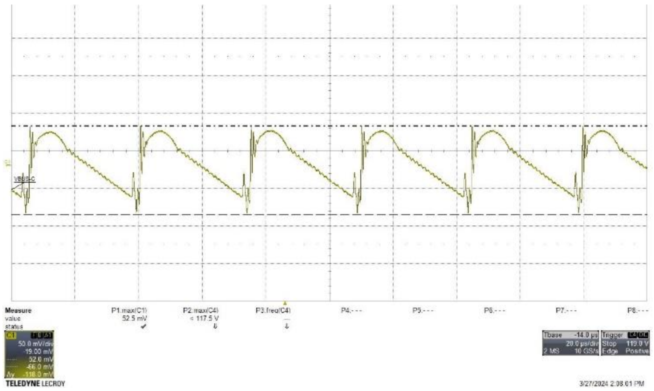
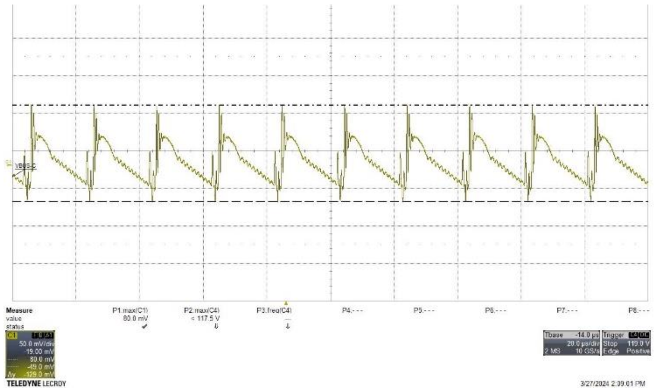
 5 V, 3 A, ripple (p-p) = 130.5 mV	 9 V, 3 A, ripple (p-p) = 117.5 mV
	
15 V, 3 A, ripple (p-p) = 177.5 mV	20 V, 3.25 A, ripple (p-p) = 165 mV

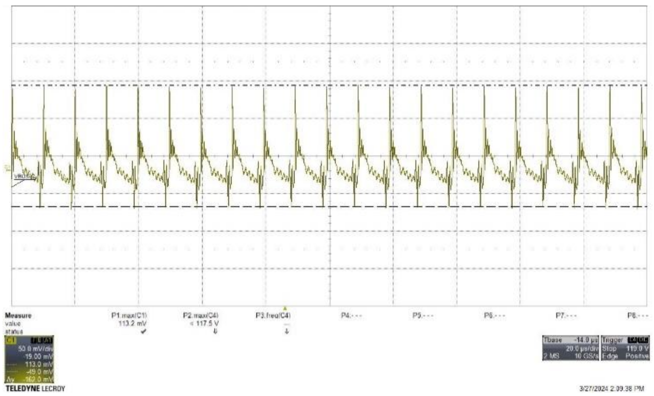
Figure 15 Ripple at 230 V_{ac}, 50 Hz (CH3: V_{bus_c})



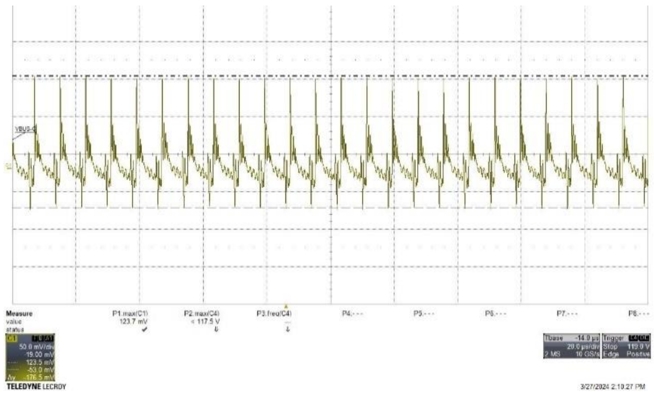
5 V, 3 A, ripple (p-p) = 118 mV



9 V, 3 A, ripple (p-p) = 129 mV



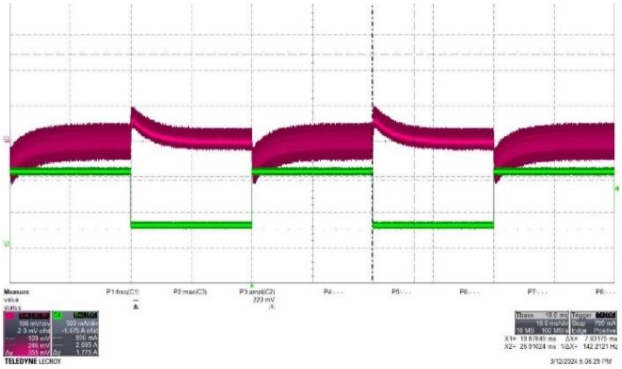
15 V, 3 A, ripple (p-p) = 162 mV



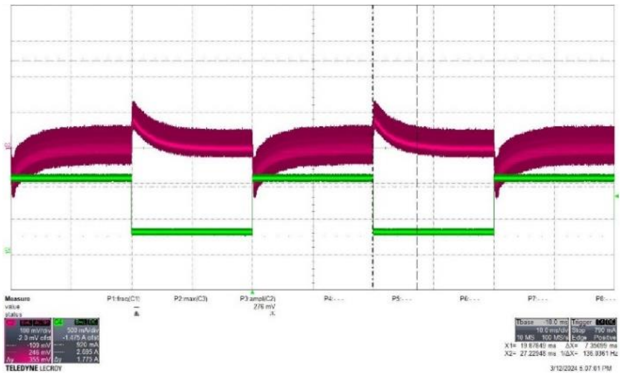
20 V, 3.25 A, ripple (p-p) = 176.5 mV

Figure 16 Ripple at 265 V_{ac}, 63 Hz (CH3: V_{bus_c})

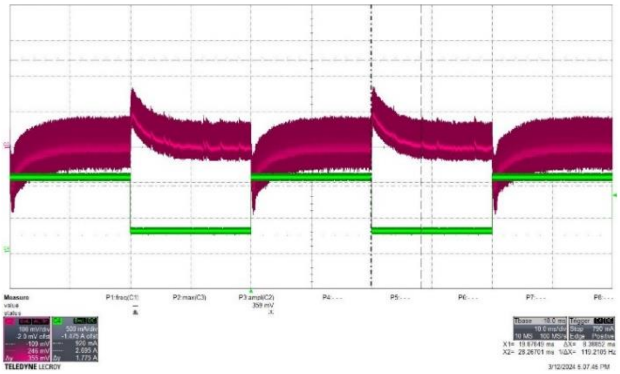
3.4 Output dynamic response settling time



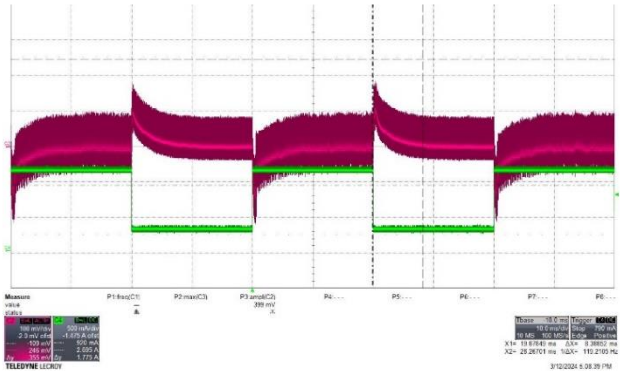
5 V – 0.3 A to 1.05 A, settling time = 7.03 ms



9 V – 0.3 A to 1.05 A, settling time = 7.35 ms

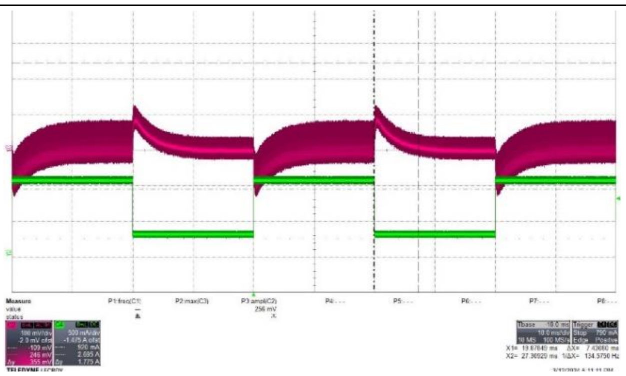


15 V – 0.3 A to 1.05 A, settling time = 8.38 ms

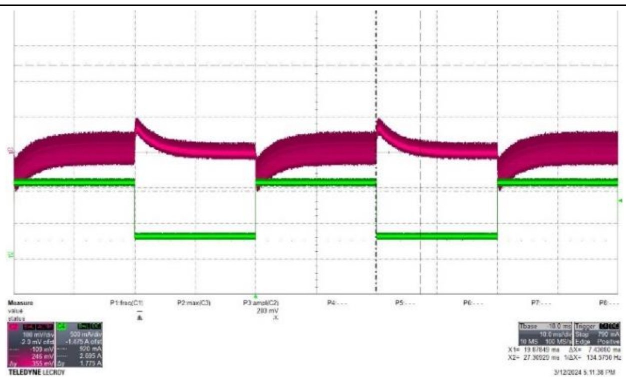


20 V – 0.3 A to 1.05 A, settling time = 8.388 ms

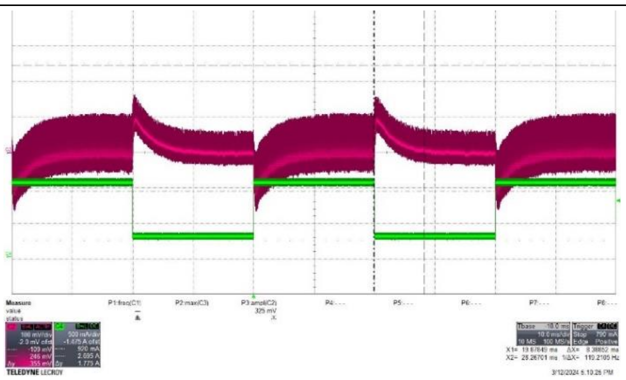
Figure 17 Settling time for 115 V_{ac}, 60 Hz; load transition - 10% to 35% load (CH3: V_{bus_c}, CH4: I_{out})



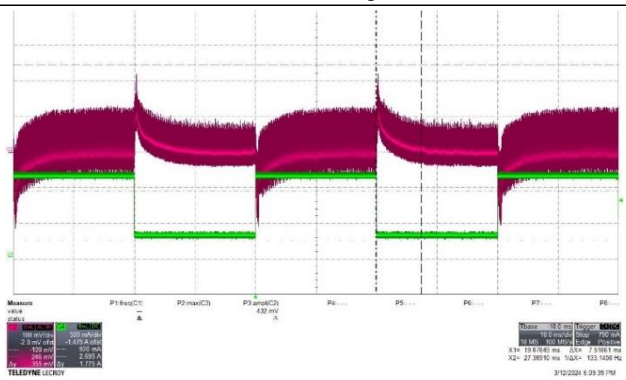
5 V – 0.3 A to 1.05 A, settling time = 7.43 ms



9 V – 0.3 A to 1.05 A, settling time = 7.43 ms

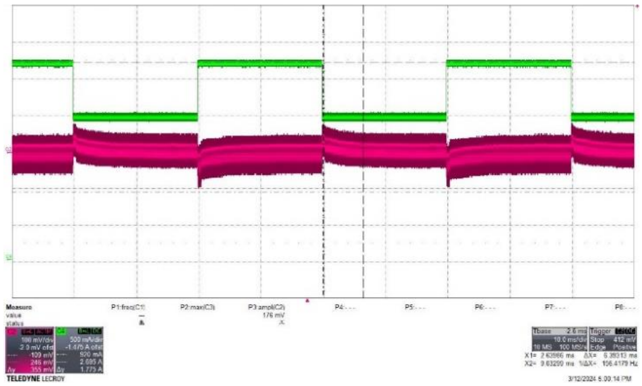


15 V – 0.3 A to 1.05 A, settling time = 8.38 ms

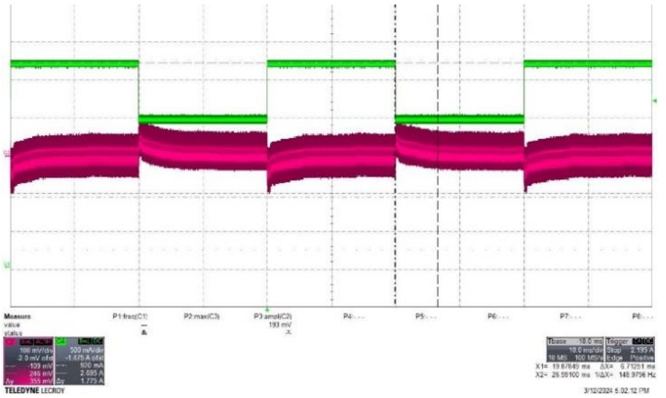


20 V – 0.325 A to 1.14 A, settling time = 7.51 ms

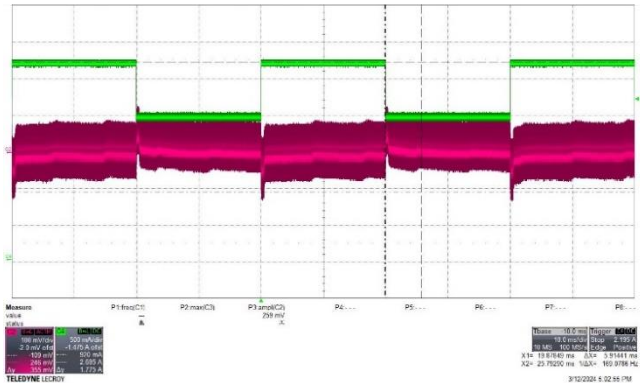
Figure 18 Settling time for 230 V_{ac}, 50 Hz; load transition - 10% to 35% load (CH3: V_{bus_c}, CH4: I_{out})



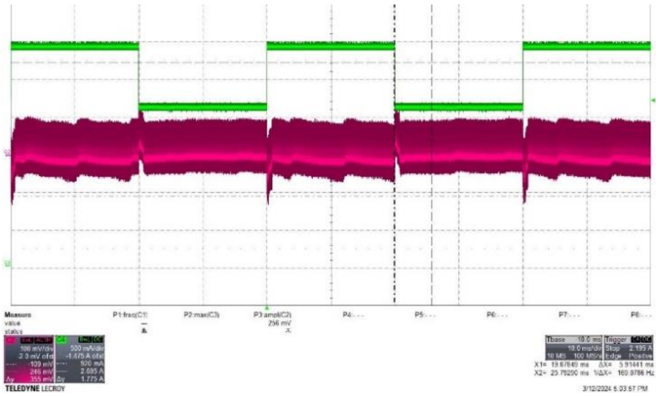
5 V – 1.95 A to 2.7 A, settling time = 6.393 ms



9 V – 1.95 A to 2.7 A, settling time = 6.712 ms

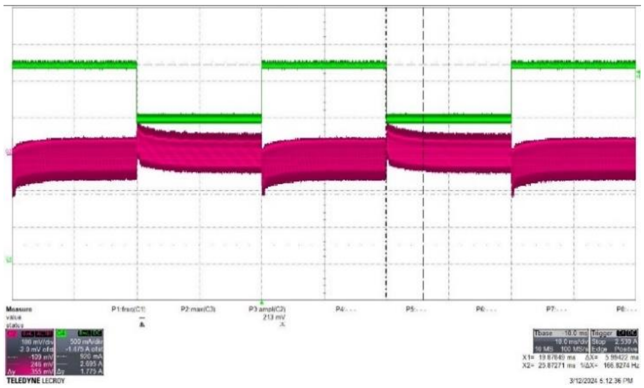


15 V – 1.95 A to 2.7 A, settling time = 5.91 ms

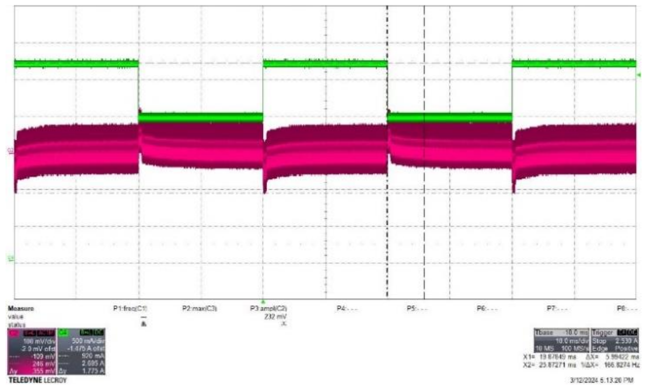


20 V – 1.95 A to 2.7 A, settling time = 5.914 ms

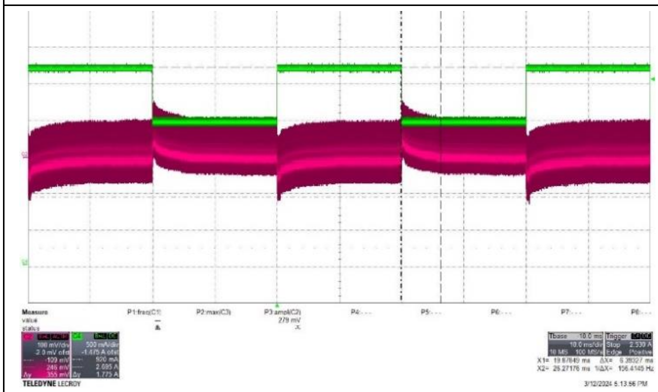
Figure 19 Settling time for 115 V_{ac}, 60 Hz; load transition - 65% to 90% load (CH3: V_{bus_c}, CH4: I_{out})



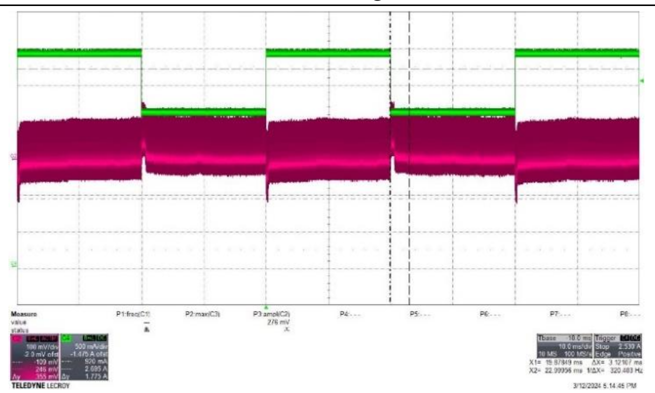
5 V – 1.95 A to 2.7 A, settling time = 5.99 ms



9 V – 1.95 A to 2.7 A, settling time = 5.994 ms



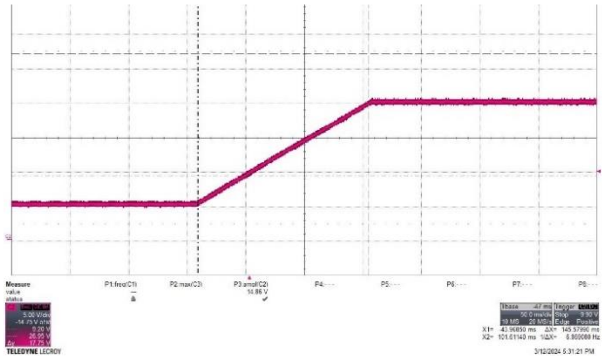
15 V – 1.95 A to 2.7 A, settling time = 6.39 ms



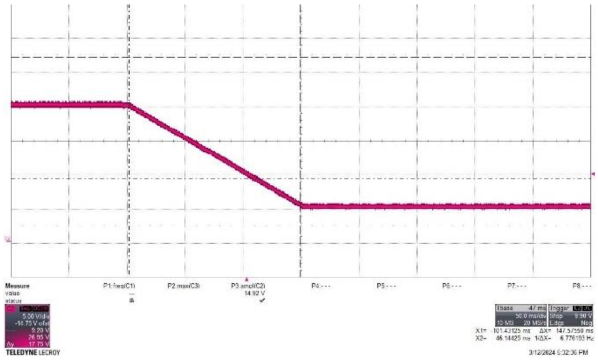
20 V – 2.11 A to 2.93 A, settling time = 3.12 ms

Figure 20 Settling time for 230 V_{ac}, 50 Hz; load transition - 65% to 90% load (CH2: V_{bus_c}, CH4: I_{out})

3.5 Output voltage transfer transition

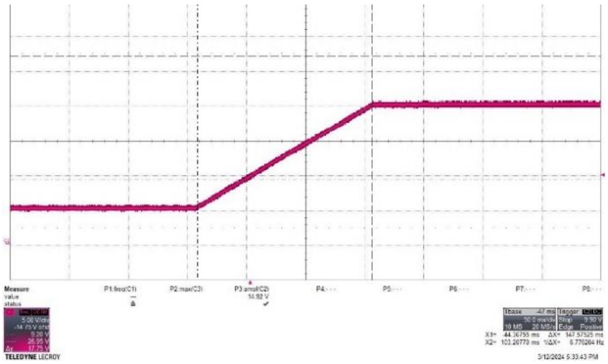


V_{out} = 5 V to 20 V, I_{out} = 0 A
Transition time: 145.5 ms
Slew rate: 0.10309 V/ms

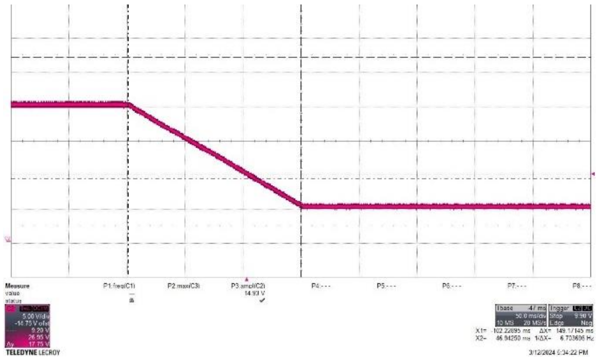


V_{out} = 20 V to 5 V, I_{out} = 0 A
Transition time: 147.575 ms
Slew rate: -0.10164 V/ms

Figure 21 Output voltage transition for 115 V_{ac}, 60 Hz; (CH1: V_{bus_c})



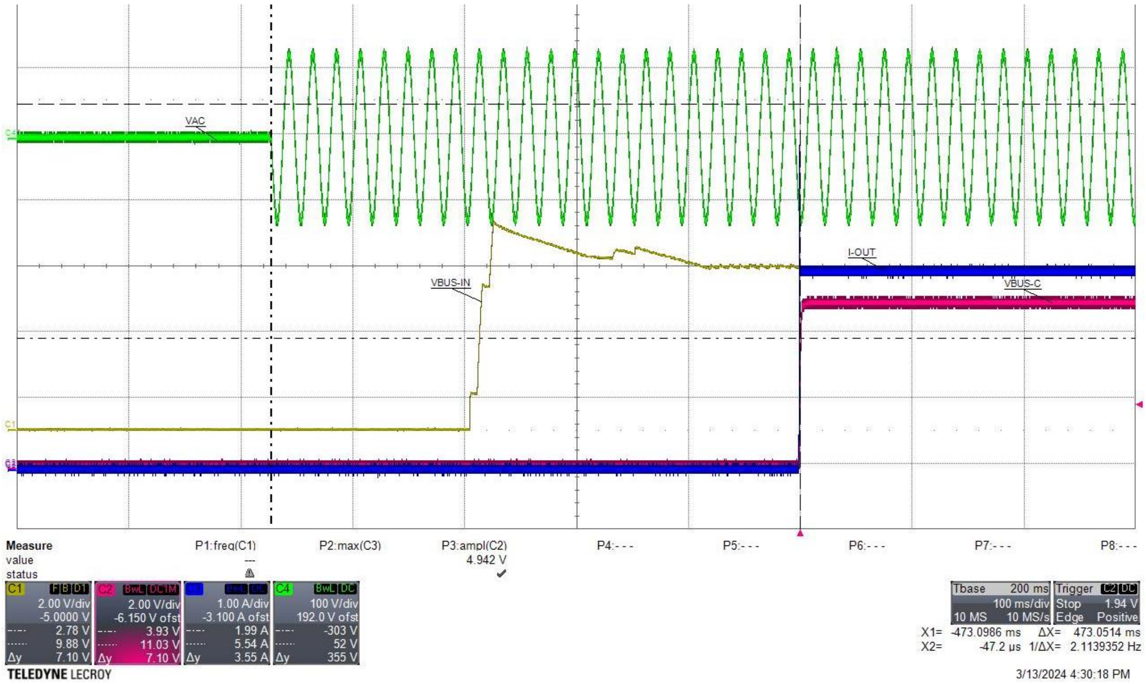
V_{out} = 5 V to 20 V, I_{out} = 0 A
Transition time: 147.575 ms
Slew rate: 0.10164 V/ms



V_{out} = 20 V to 5 V, I_{out} = 0 A
Transition time: 149.17 ms
Slew rate: -0.10055 V/ms

Figure 22 Output voltage transition for 230 V_{ac}, 50 Hz; (CH1: V_{bus_c})

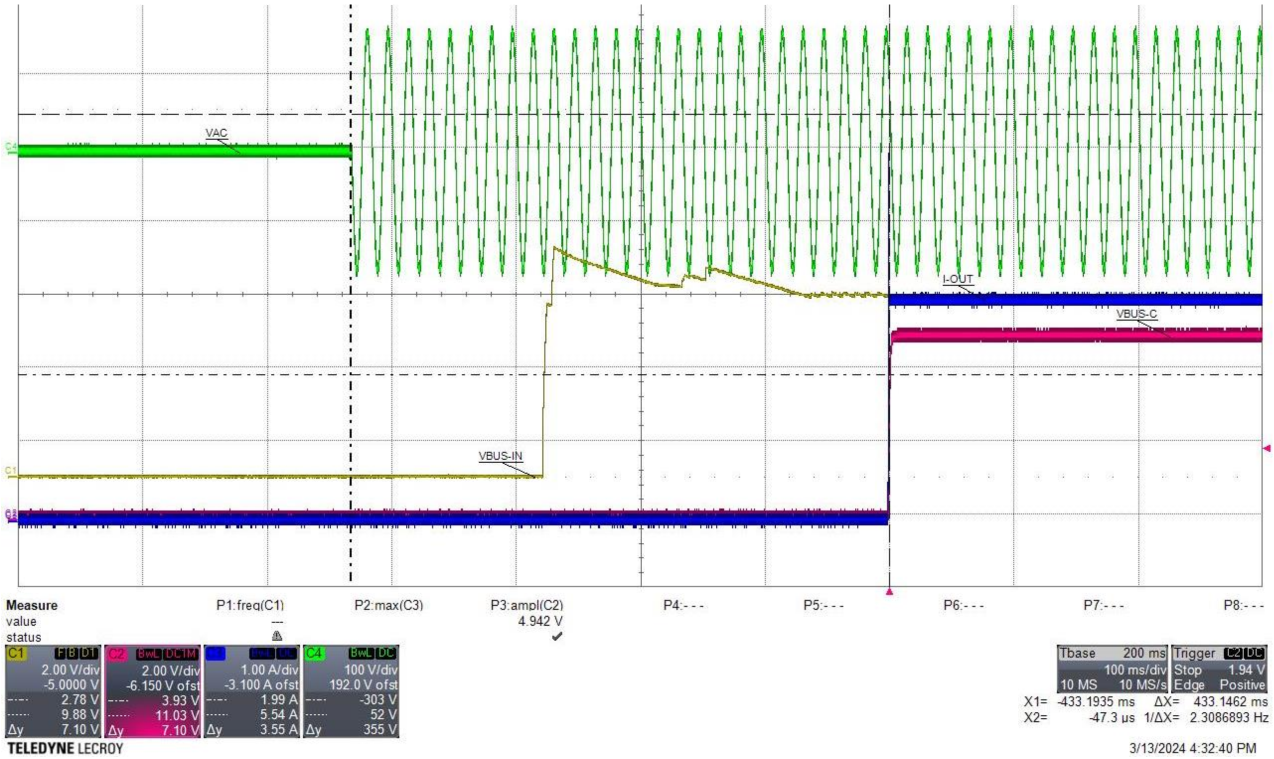
3.6 Start-up turn-on delay and start-up rise time



V_{out} = 5 V, I_{out} = 3 A, start-up delay time = 473.05 ms

Start-up rise time = 2.09 ms

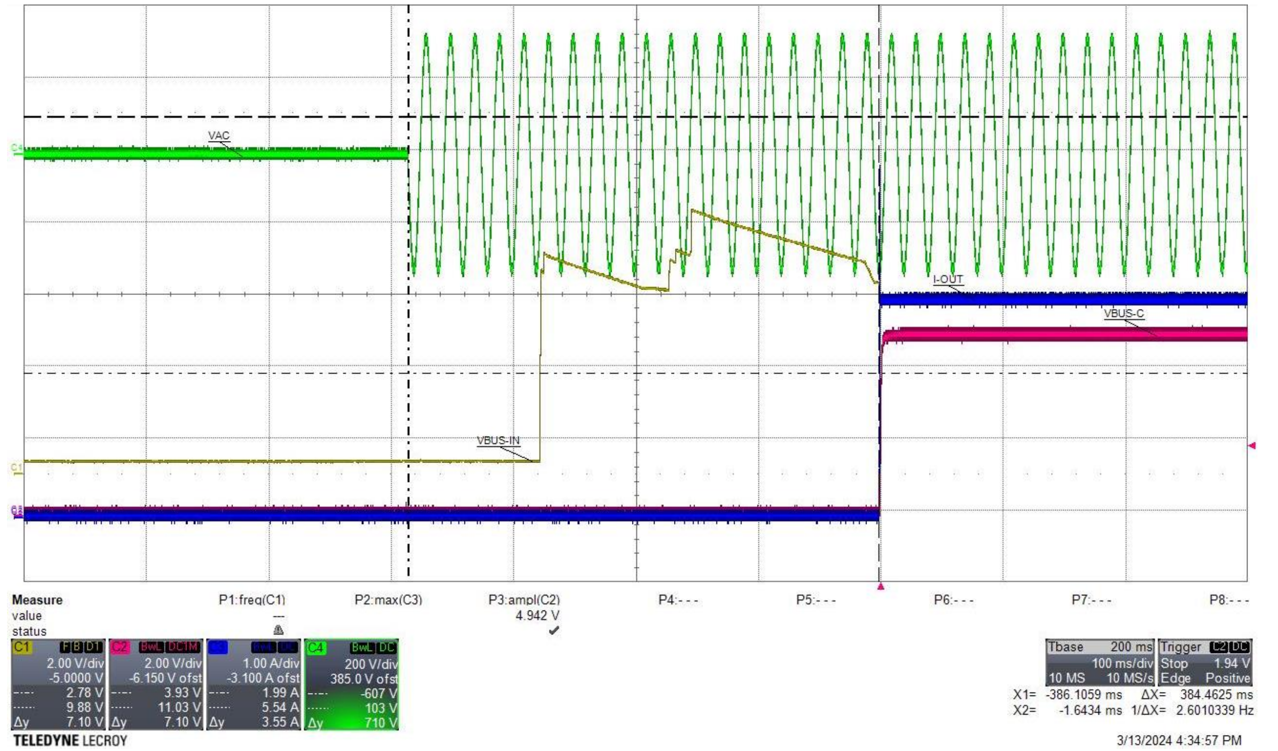
Figure 23 Start-up turn-on delay at 90 V_{ac}, 47 Hz (CH1: V_{bus_in}, CH2: V_{o+}, CH3: I_{out}, CH4: V_{in_ac})



V_{out} = 5 V, I_{out} = 3 A, start-up delay time = 433.146 ms

Start-up rise time = 2.09 ms

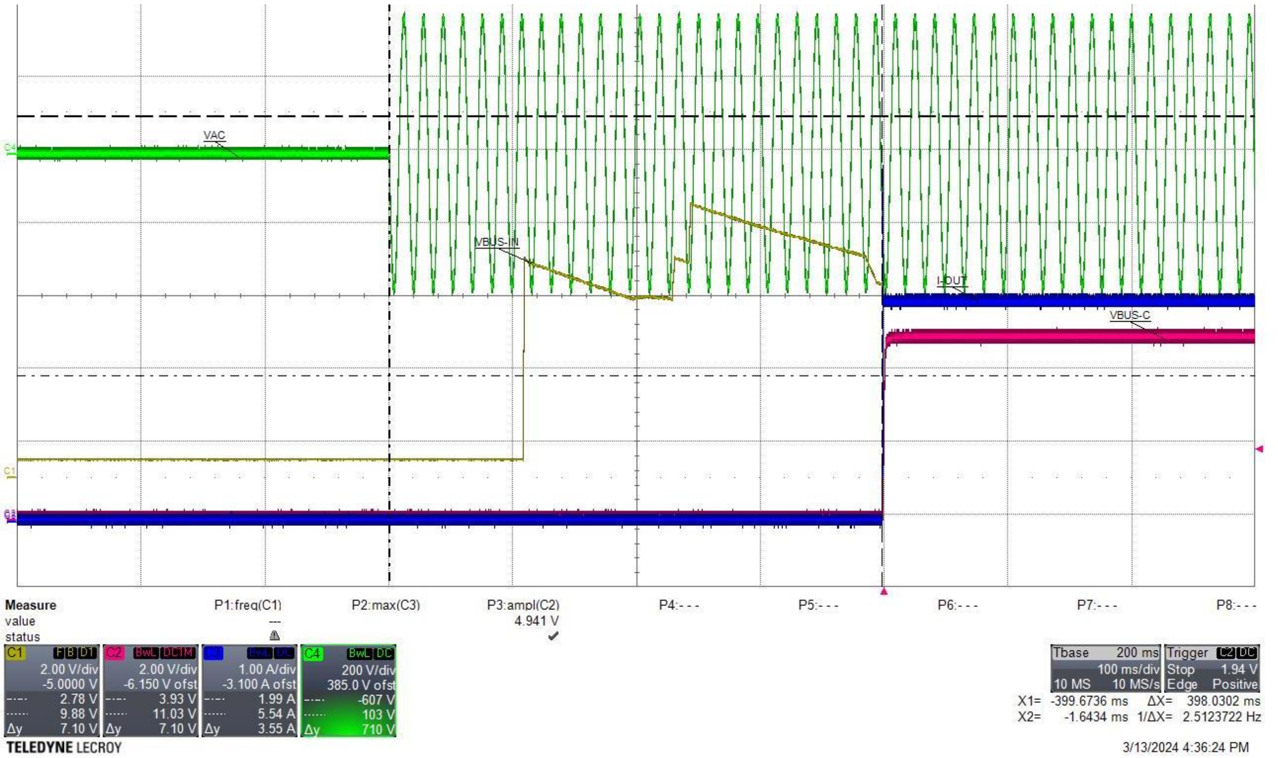
Figure 24 Start-up turn-on delay at 115 V_{ac}, 60 Hz (CH1: V_{bus_in}, CH2: V_{o+}, CH3: I_{out}, CH4: V_{in_ac})



V_{out} = 5 V, I_{out} = 3 A, start-up delay time = 384.46 ms

Start-up rise time = 1.92 ms

Figure 25 Start-up turn-on delay at 230 V_{ac}, 50 Hz (CH1: V_{bus_in}, CH2: V_{o+}, CH3: I_{out}, CH4: V_{in_ac})

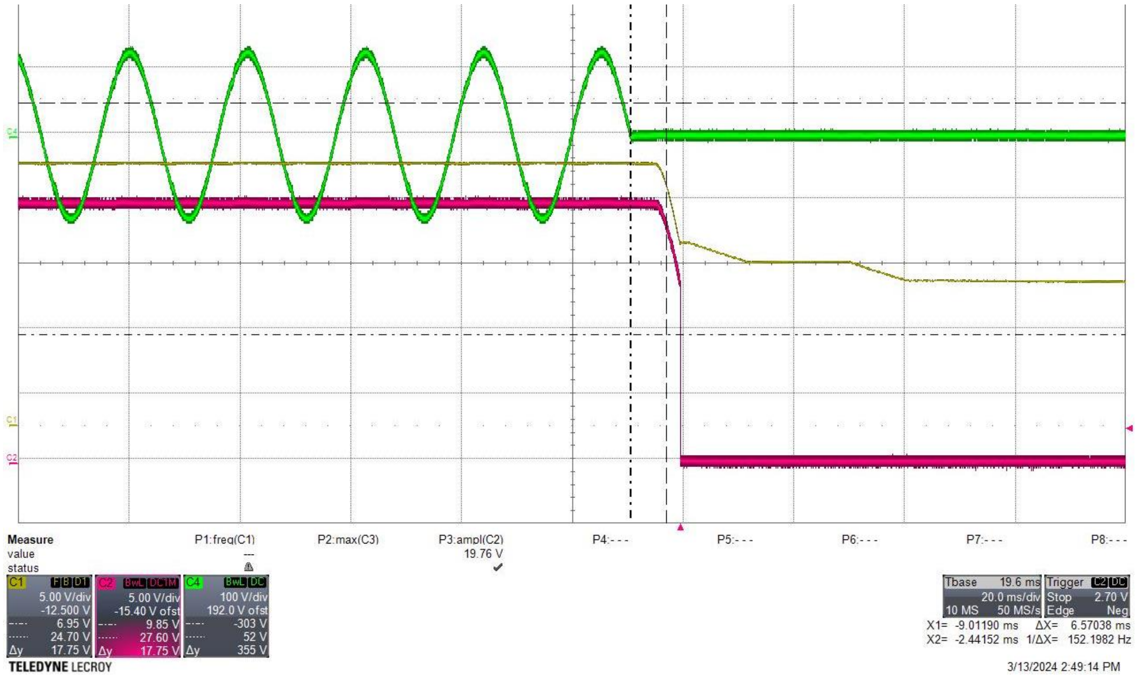


V_{out} = 5 V, I_{out} = 3 A, start-up delay time = 398.03 ms

Start-up rise time = 2 ms

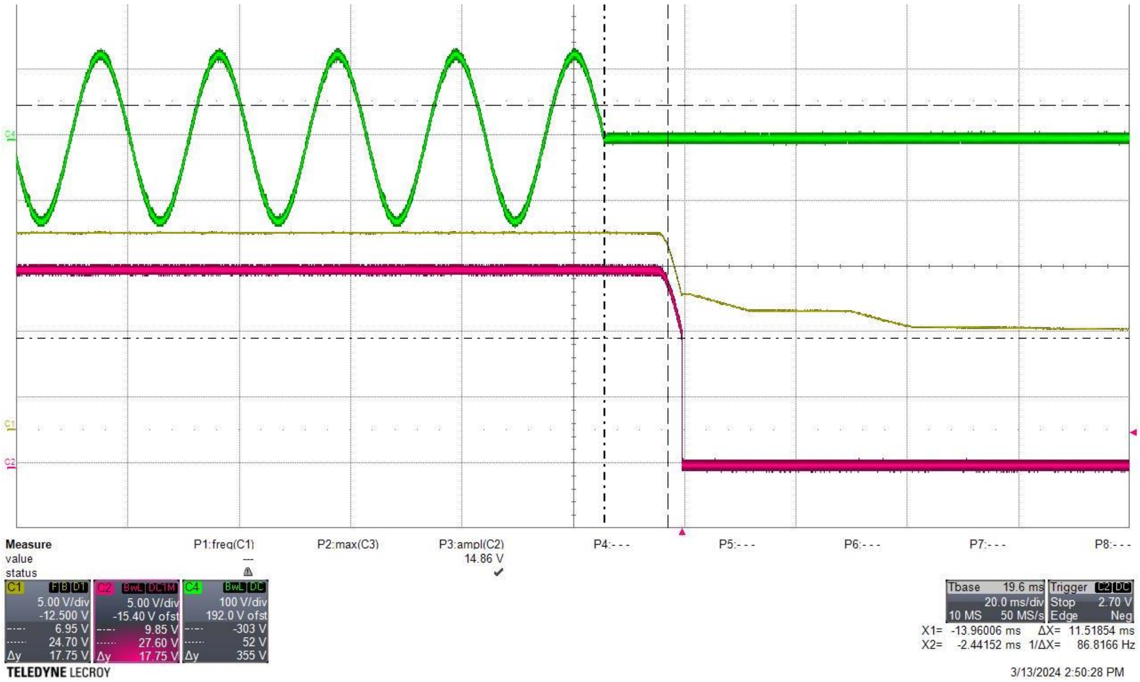
Figure 26 Start-up turn-on delay at 265 V_{ac}, 63 Hz (CH1: V_{bus_in}, CH2: V_{o+}, CH3: I_{out}, CH4: V_{in_ac})

3.7 Hold-up time



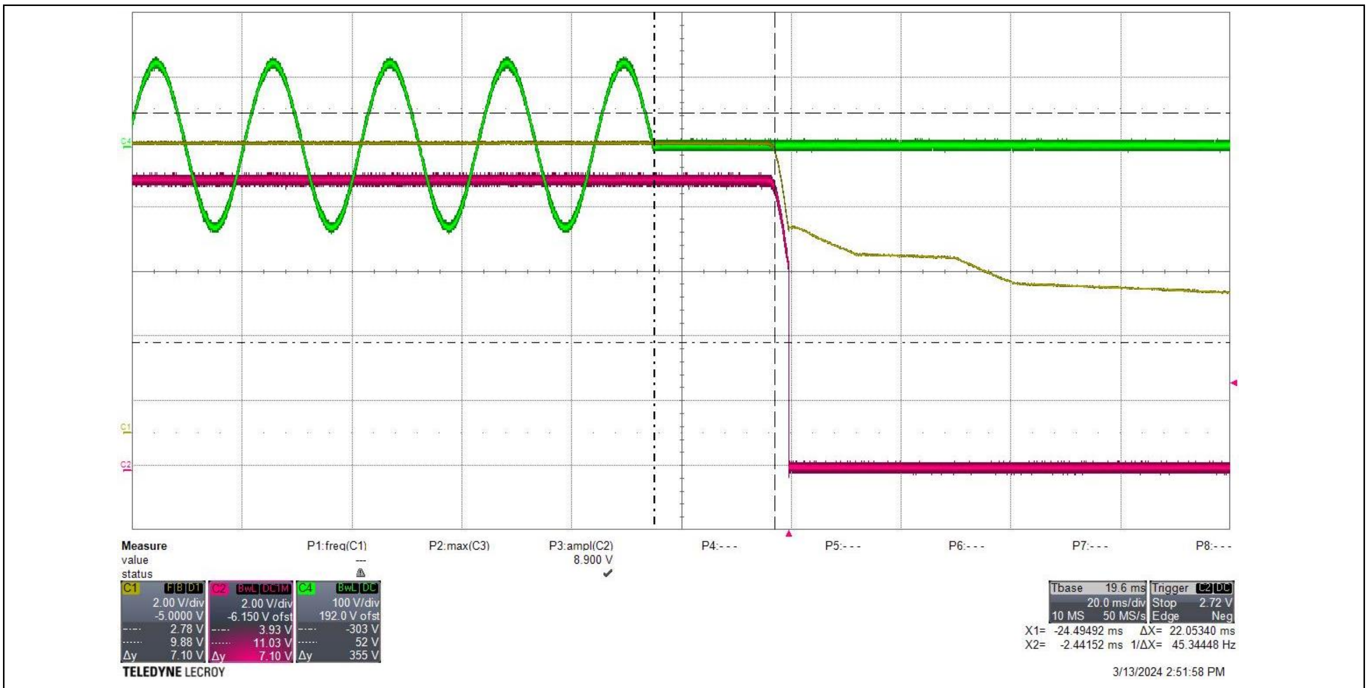
V_{out} = 20 V, I_{out} = 3.25 A, hold-up time = 6.57 ms

Figure 27 Hold-up time at 90 V_{ac}, 47 Hz (CH1: V_{bus_in}, CH2: V_{bus_c}, CH4: V_{in_ac})



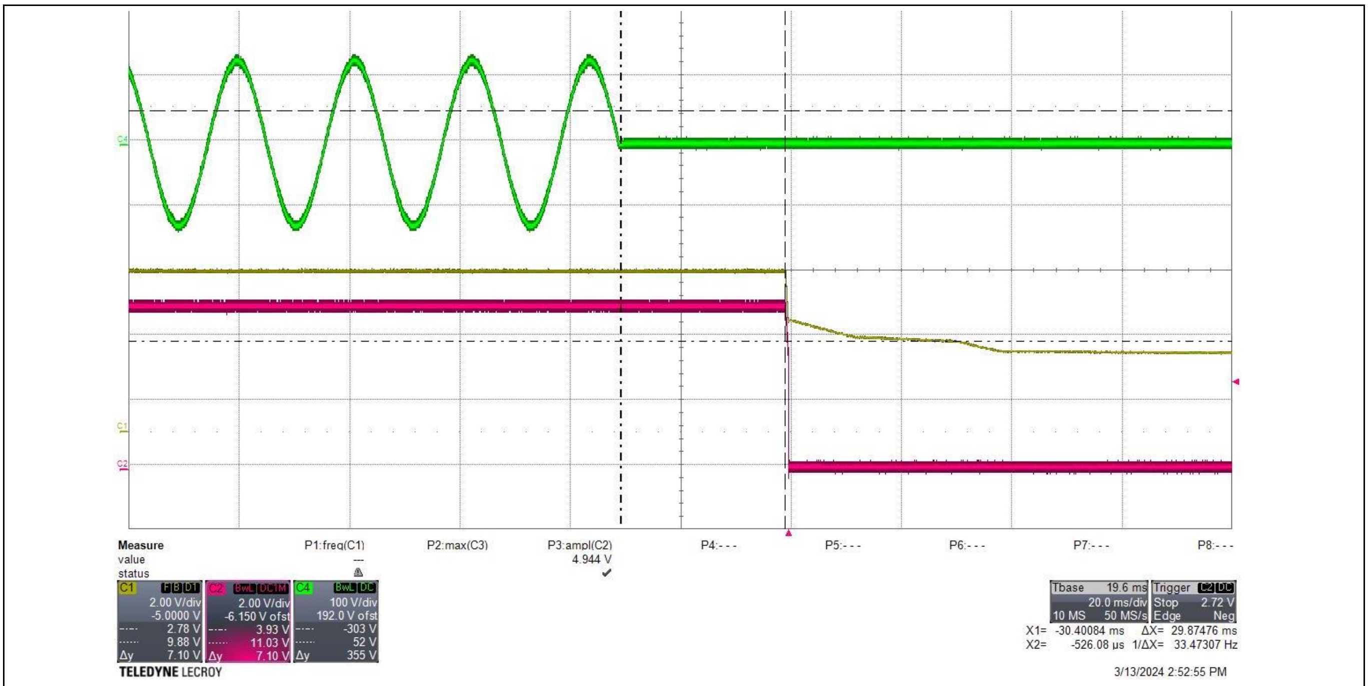
V_{out} = 15 V, I_{out} = 3.00 A, hold-up time = 11.518 ms

Figure 28 Hold-up time at 90 V_{ac}, 47 Hz (CH1: V_{bus_in}, CH2: V_{bus_c}, CH4: V_{in_ac})



V_{out} = 9.0 V, I_{out} = 3.00 A, hold-up time = 22.05 ms

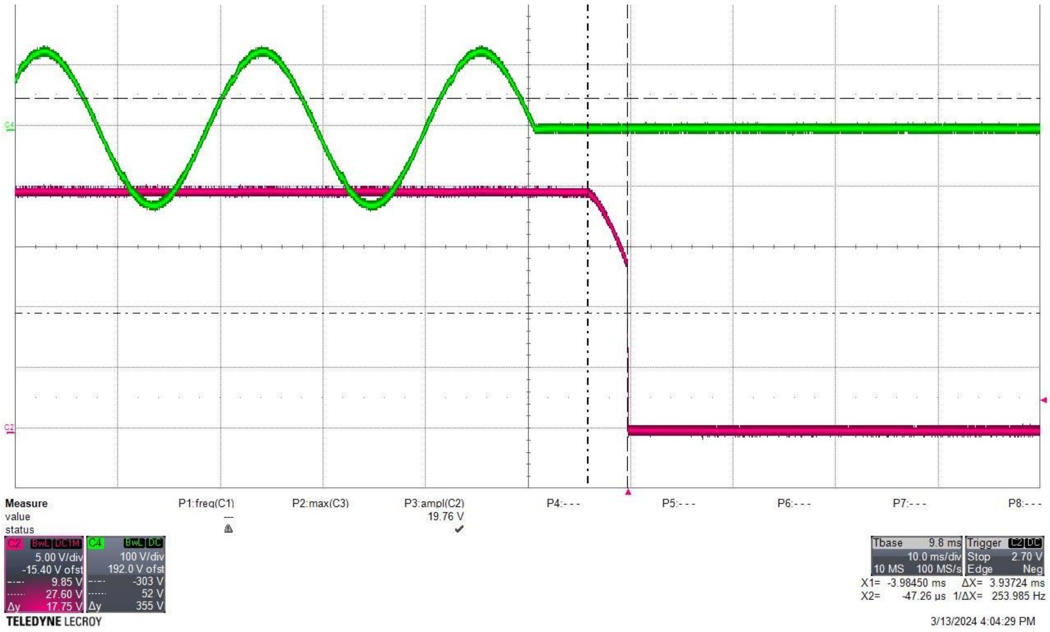
Figure 29 Hold-up time at 90 V_{ac}, 47 Hz (CH1: V_{bus_in}, CH2: V_{bus_c}, CH4: V_{in_ac})



V_{out} = 5.0 V, I_{out} = 3.00 A, hold-up time = 29.874 ms

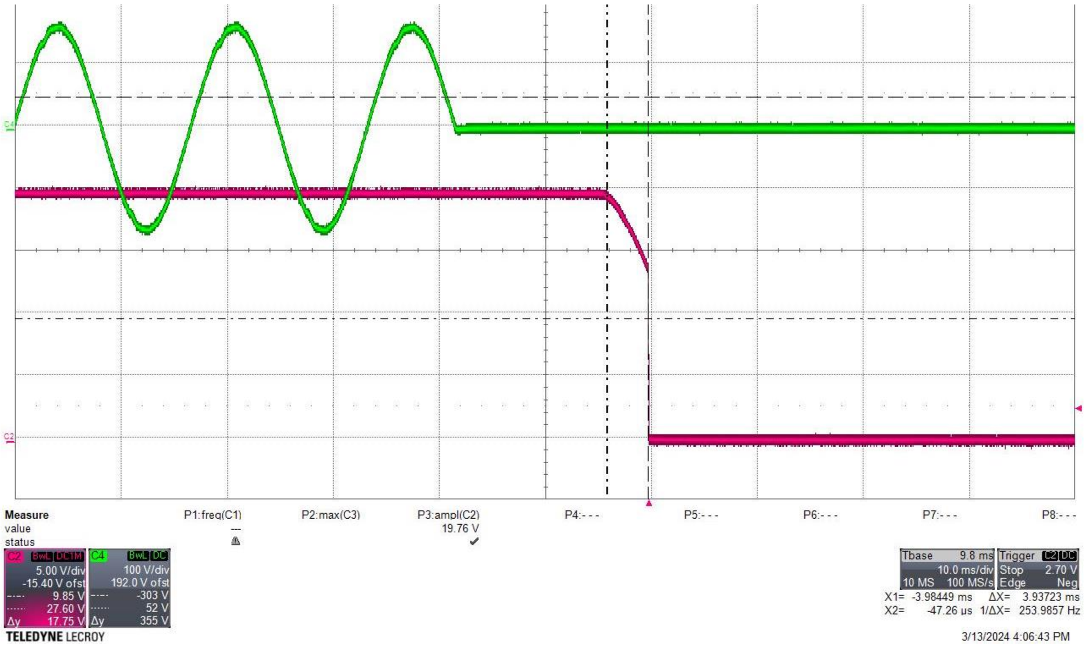
Figure 30 Hold-up time at 90 V_{ac}, 47 Hz (CH1: V_{bus_in}, CH2: V_{bus_c}, CH4: V_{in_ac})

3.8 Shut-down fall time



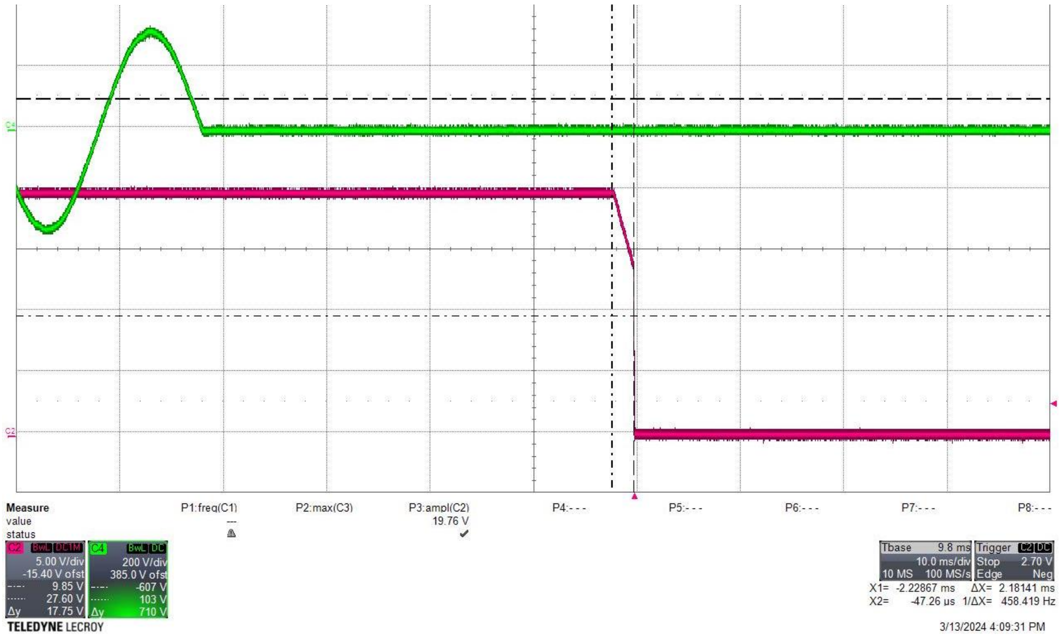
V_{out} = 20 V, I_{out} = 3.25 A, shut-down fall time = 3.937 ms

Figure 31 Shut-down fall time at 90 V_{ac}, 47 Hz (CH2: V_{bus_c}, CH3: V_{in_ac})



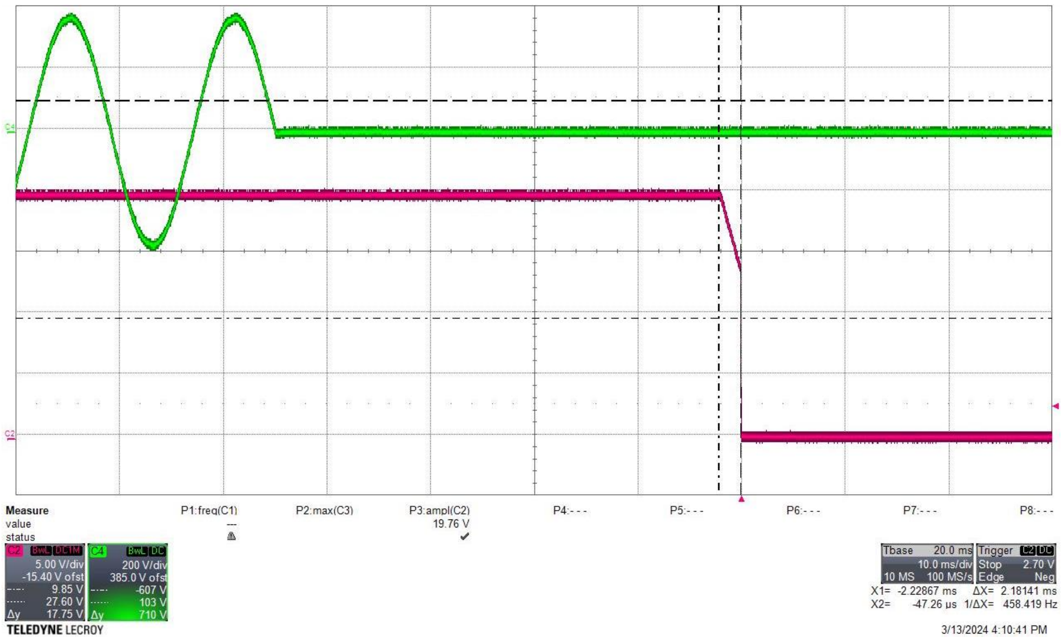
V_{out} = 20 V, I_{out} = 3.25 A, shut-down fall time = 3.937 ms

Figure 32 Shut-down fall time at 115 V_{ac}, 60 Hz (CH2: V_{bus_c}, CH3: V_{in_ac})



V_{out} = 20 V, I_{out} = 3.25 A, shut-down fall time = 2.18 ms

Figure 33 Shut-down fall time at 230 V_{ac}, 50 Hz (CH: V_{bus_c}, CH3: V_{in_ac})

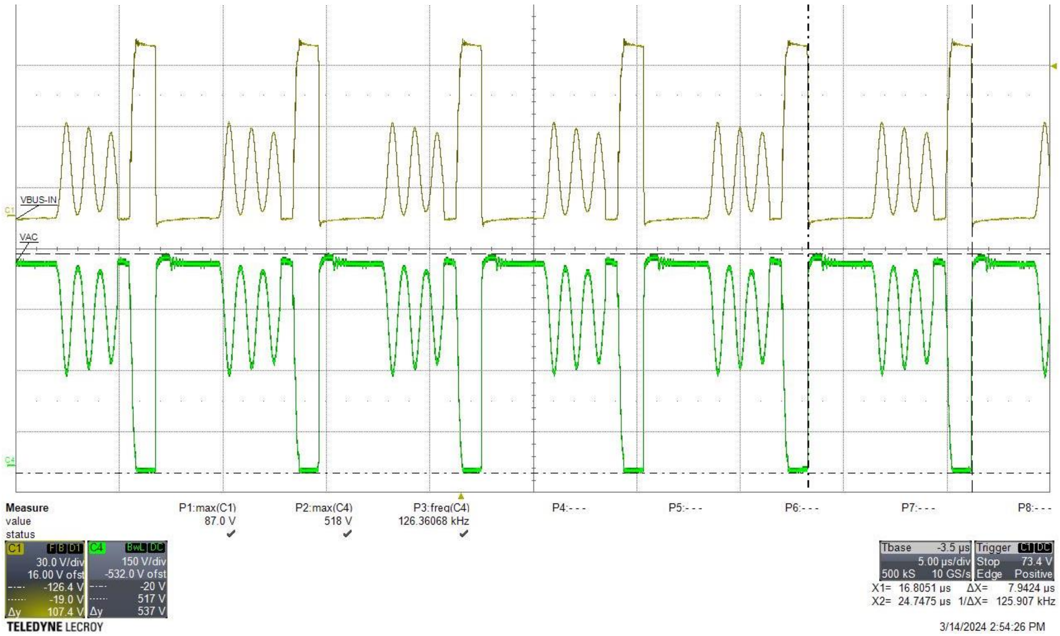


V_{out} = 20 V, I_{out} = 3.25 A, shut-down fall time = 2.18 ms

Figure 34 Shut-down fall time at 265 V_{ac}, 63 Hz (CH2: V_{bus_c}, CH3: V_{in_ac})

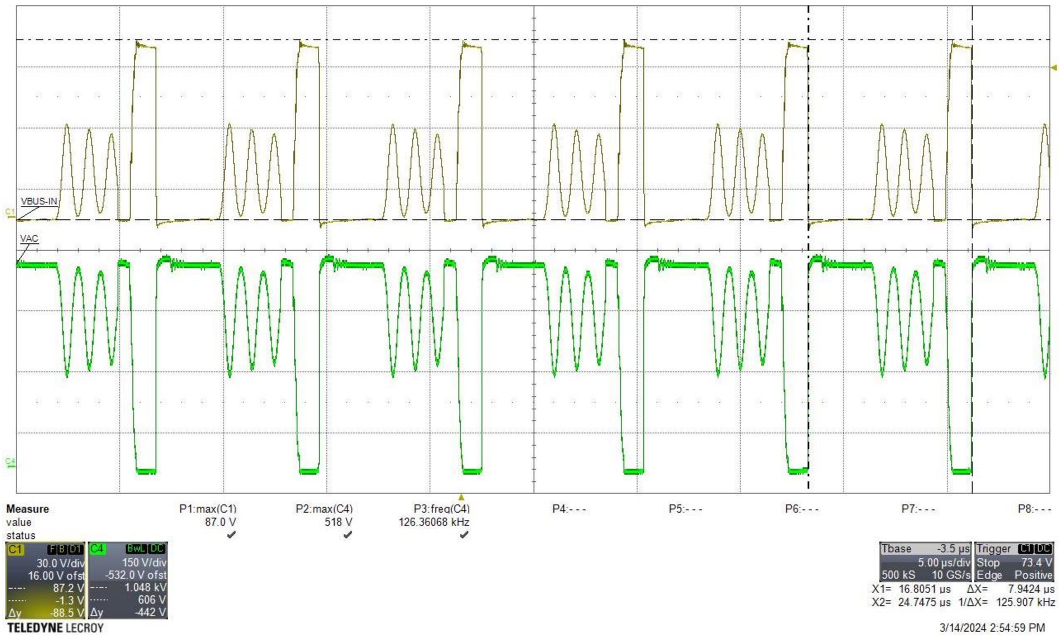
3.9 Switch voltage stress

Test condition: V_{in} = 265 V_{ac}, 63 Hz, V_{out} = 20 V, I_{out} = 3.25 A



V_{pri_drain} = 537 V

Figure 35 Switch voltage stress on primary FET (CH1: V_{sr_sec}, CH4: V_{pri_drain})

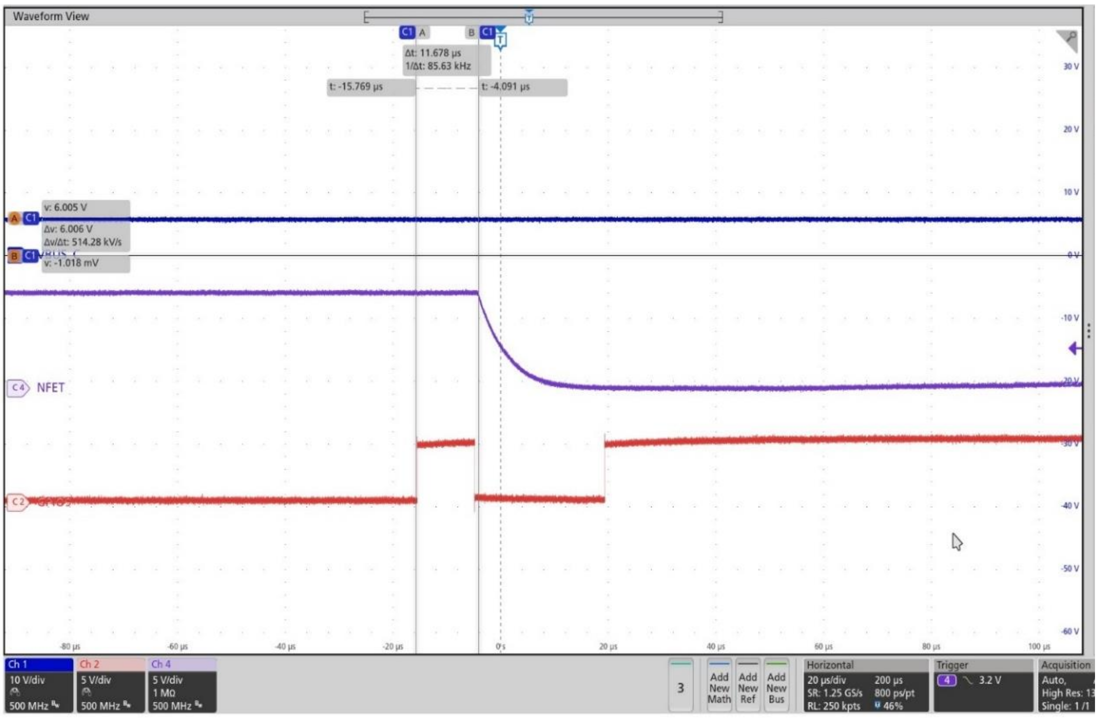


V_{sr_drain} = 88.5 V

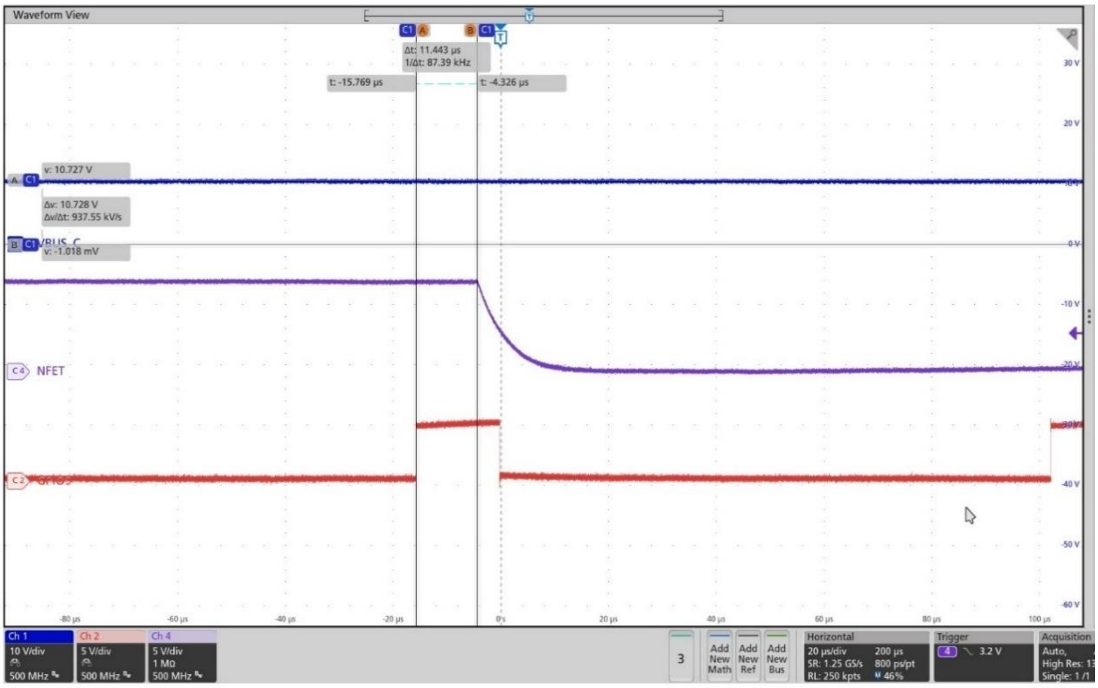
Figure 36 Switch voltage stress on secondary FET (CH1: V_{sr_sec}, CH4: V_{pri_drain})

3.10 Overvoltage protection (OVP)

OVP tested at 115 V_{ac}, 60 Hz:



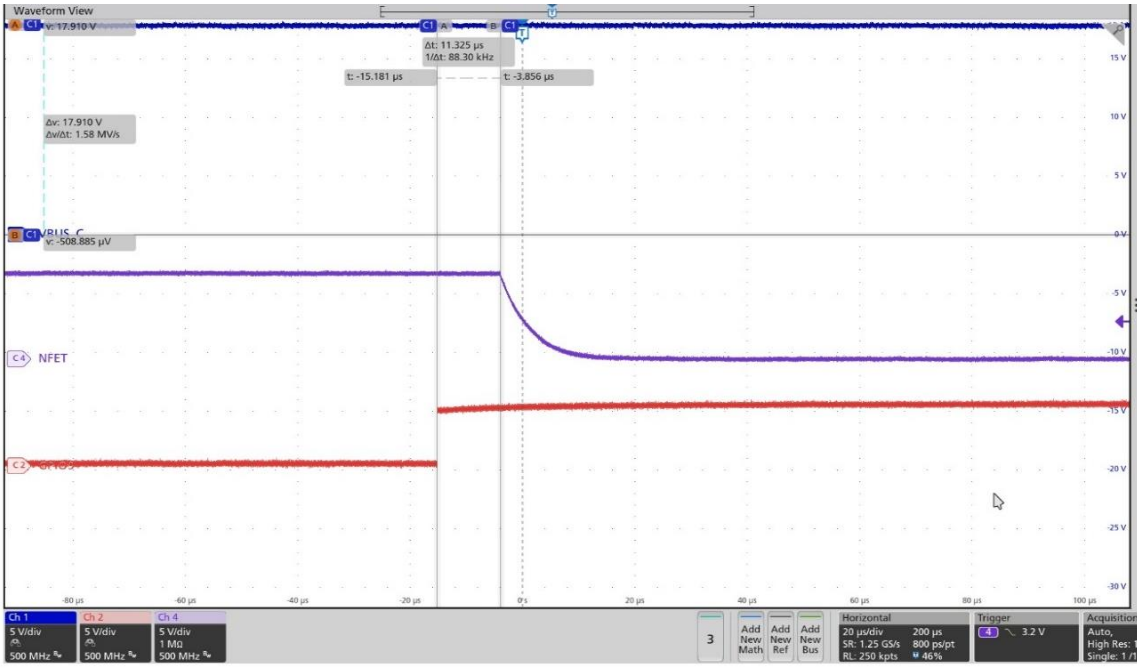
V_{out} = 5 V, OVP_limit = 6 V, OVP_response time = 11.6 µs



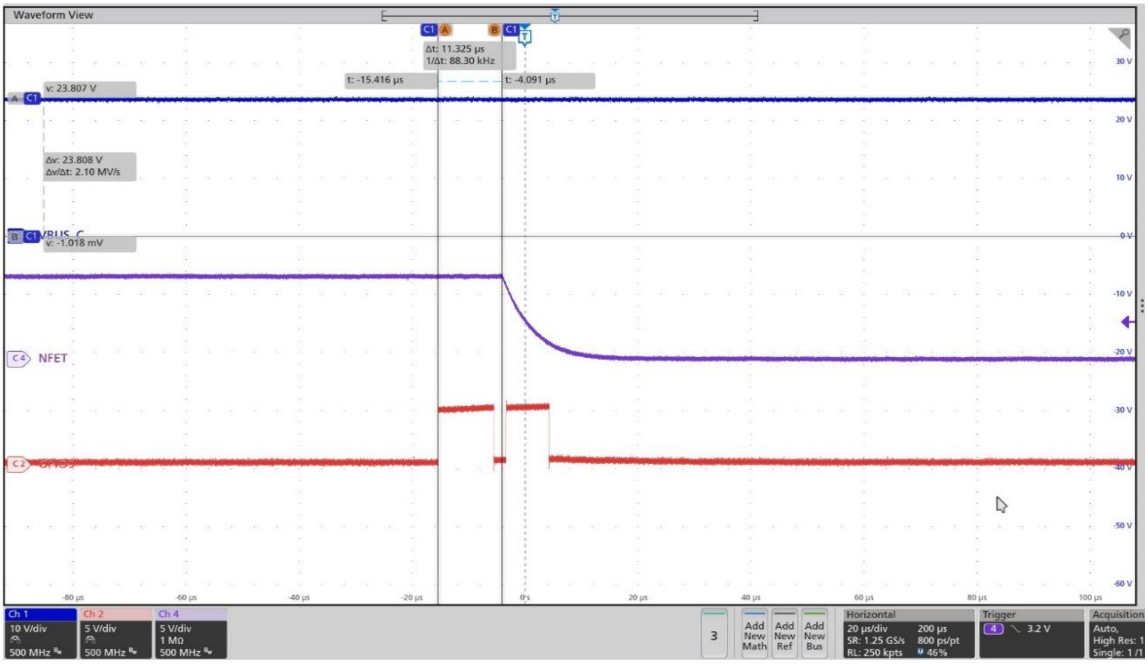
V_{out} = 9 V, OVP_limit = 10.7 V, OVP_response time = 11.4 µs

Figure 37 OVP at 115 V_{ac}, 60 Hz (CH3: NFET[1]; CH2: GPIO9; CH1: V_{bus_c}) (1 of 2)

[1] NFET - Provider FET (Q2) gate to source waveform.



V_{out} = 15 V, OVP_limit = 17.9 V, OVP_response time = 11.3 µs

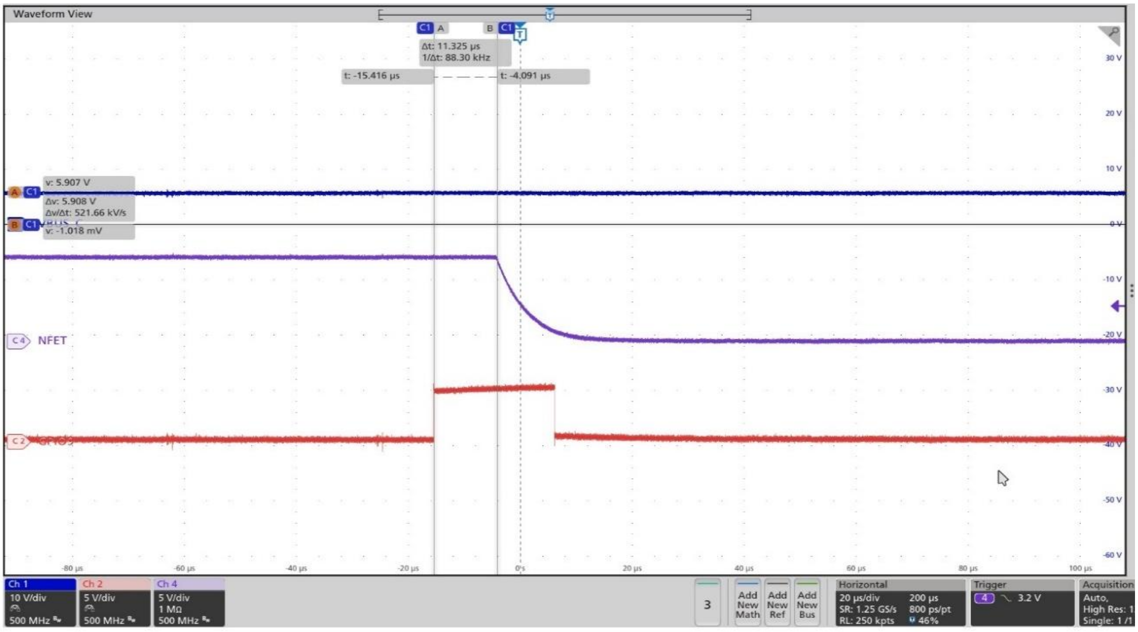


V_{out} = 20 V, OVP_limit = 23.8 V, OVP_response time = 11.3 µs

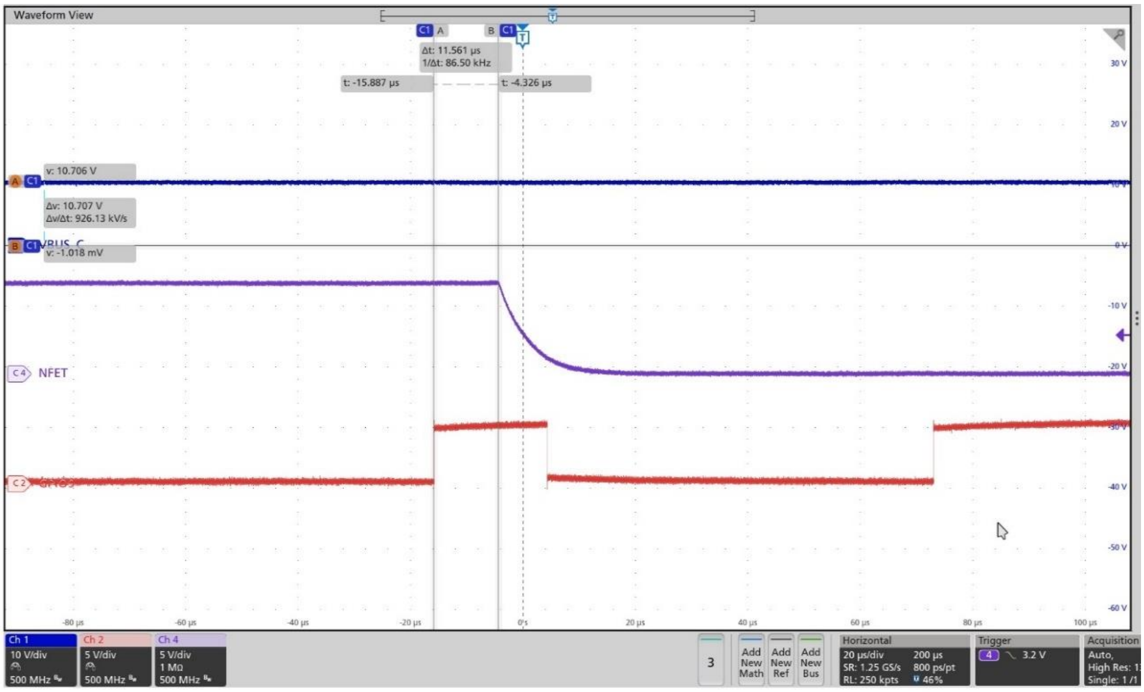
Figure 38 OVP at 115 V_{ac}, 60 Hz (CH3: NFET[2]; CH2: GPIO9; CH1: V_{bus_c}) (2 of 2)

[2] NFET - Provider FET (Q2) gate to source waveform.

OVP tested at 230 V_{ac}, 50 Hz:



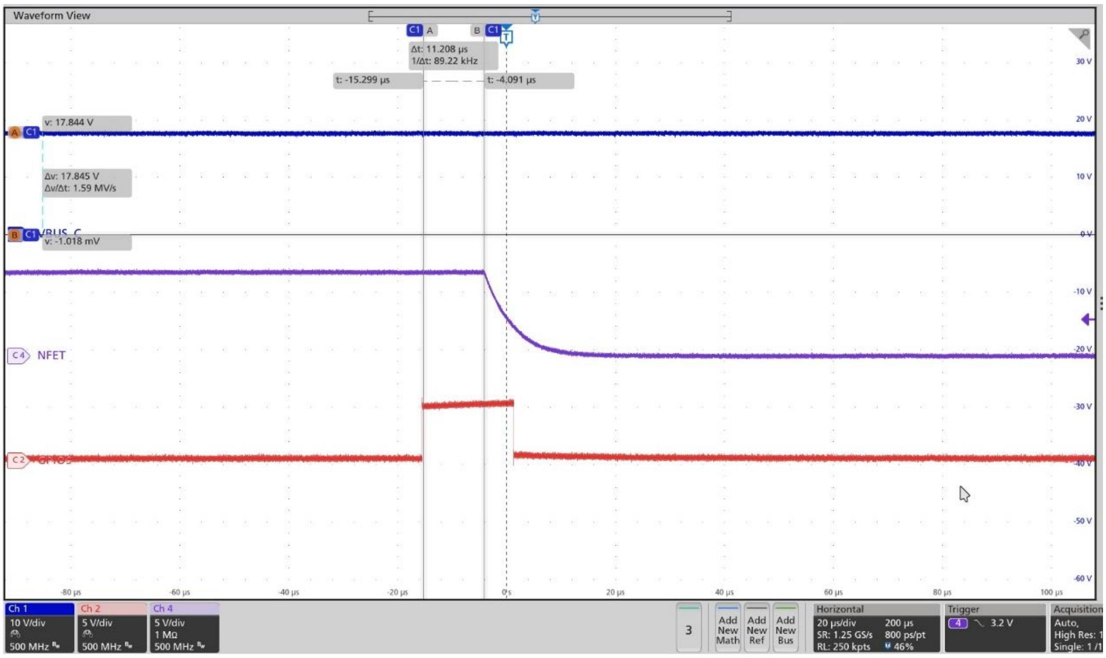
V_{out} = 5 V, OVP_limit = 5.9 V, OVP_response time = 11.3 µs



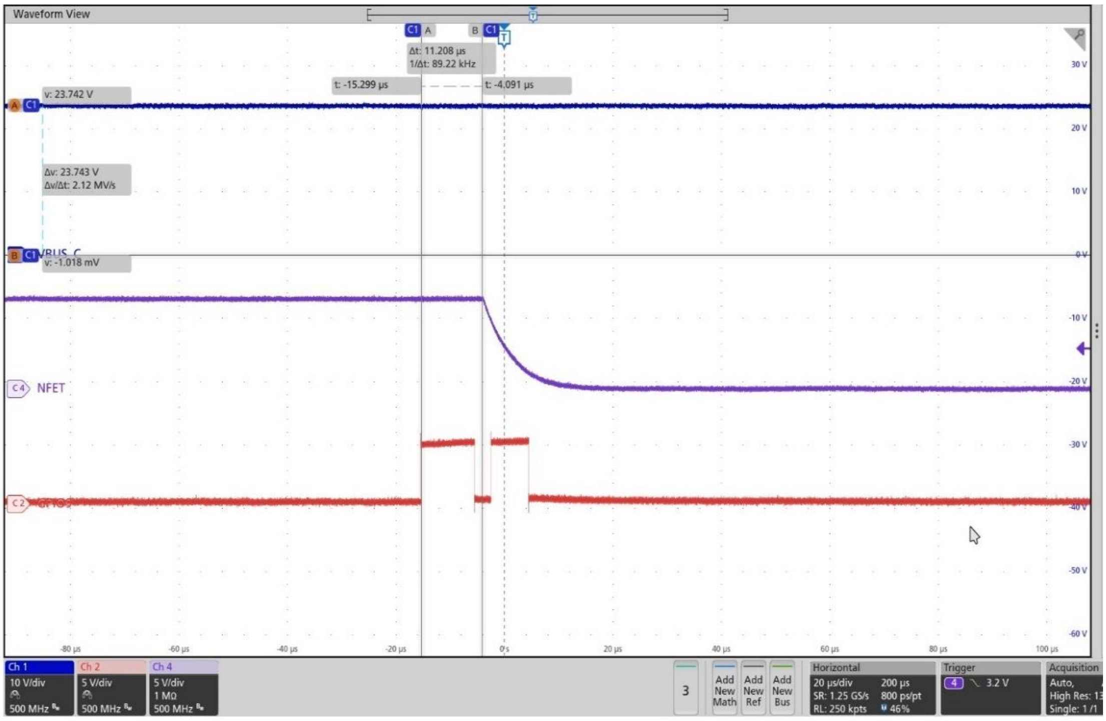
V_{out} = 9 V, OVP_limit = 10.8 V, OVP_response time = 11.5 µs

Figure 39 OVP at 230 V_{ac}, 50 Hz (CH3: NFET[3]; CH2: GPIO9; CH1: V_{bus_c}) (1 of 2)

[3] NFET - Provider FET (Q2) gate to source waveform.



V_{out} = 15 V, OVP_limit = 17.9 V, OVP_response time = 11.2 µs



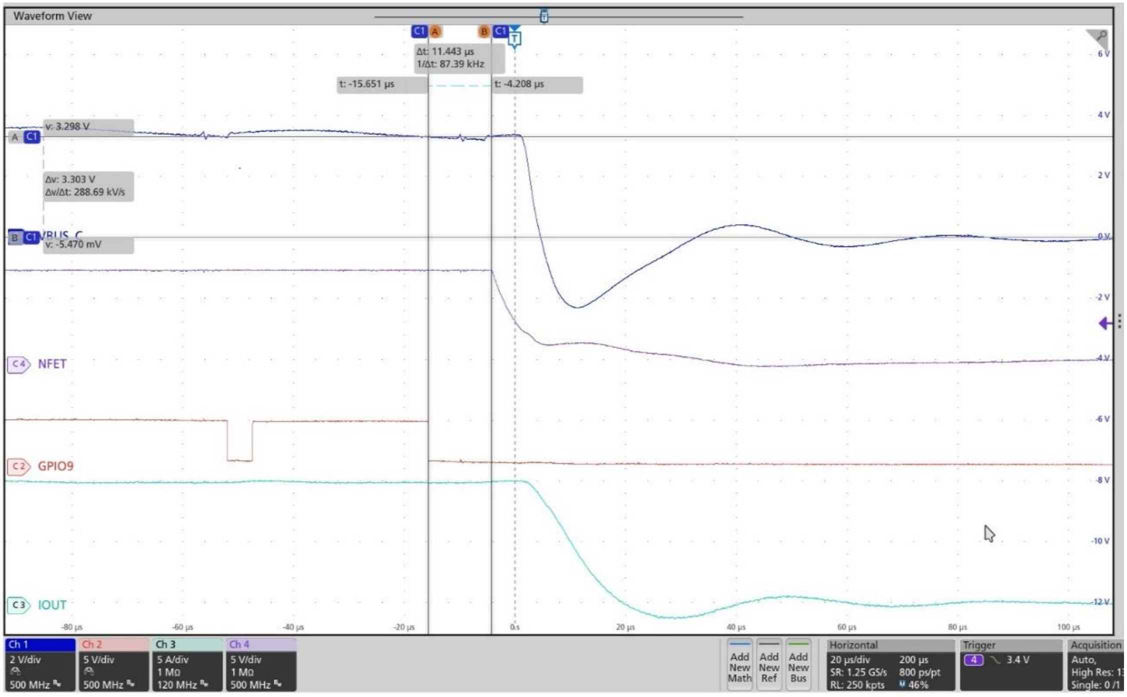
V_{out} = 20 V, OVP_limit = 23.8 V, OVP_response time = 11.2 µs

Figure 40 OVP at 230 Vac, 50 Hz (CH3: NFET[4] ; CH2: GPIO9; CH1: Vbus_C) (2 of 2)

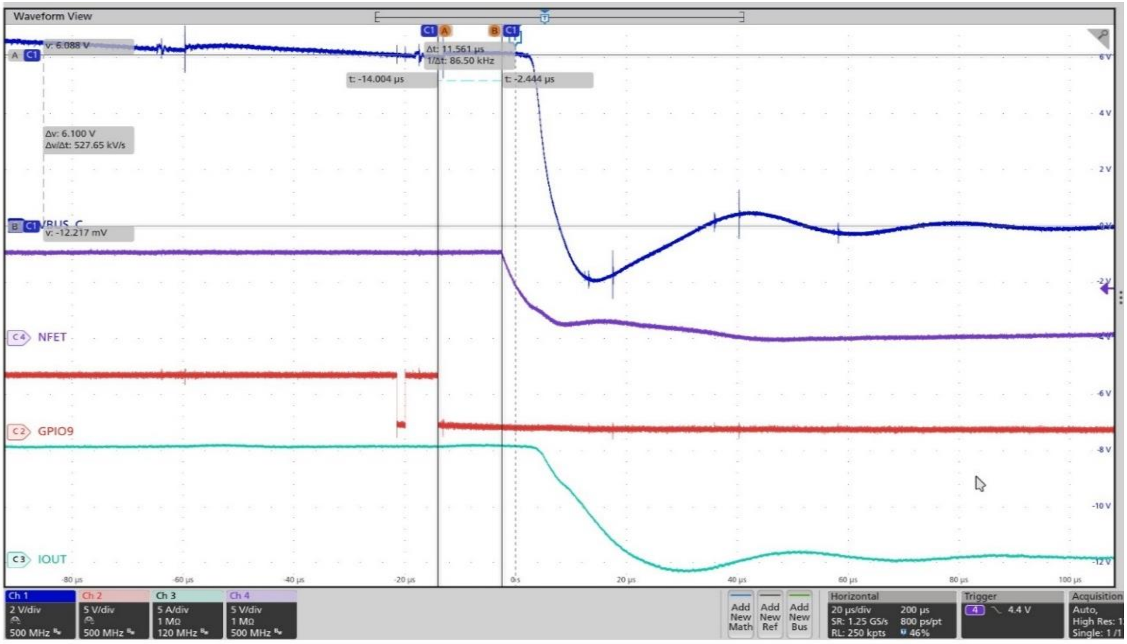
[4] NFET - Provider FET (Q2) gate to source waveform.

3.11 Undervoltage protection (UVP)

UVP tested at 115 V_{ac}, 60 Hz:



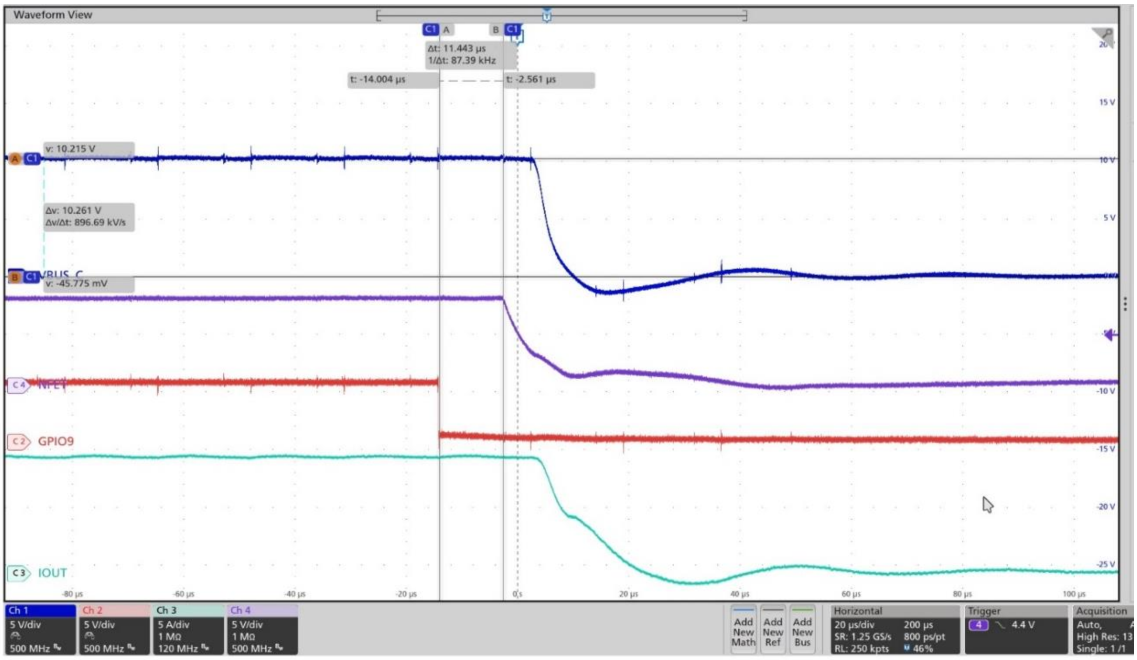
V_{out} = 5 V, UVP_limit = 3.29 V, UVP_response time = 11.4 µs



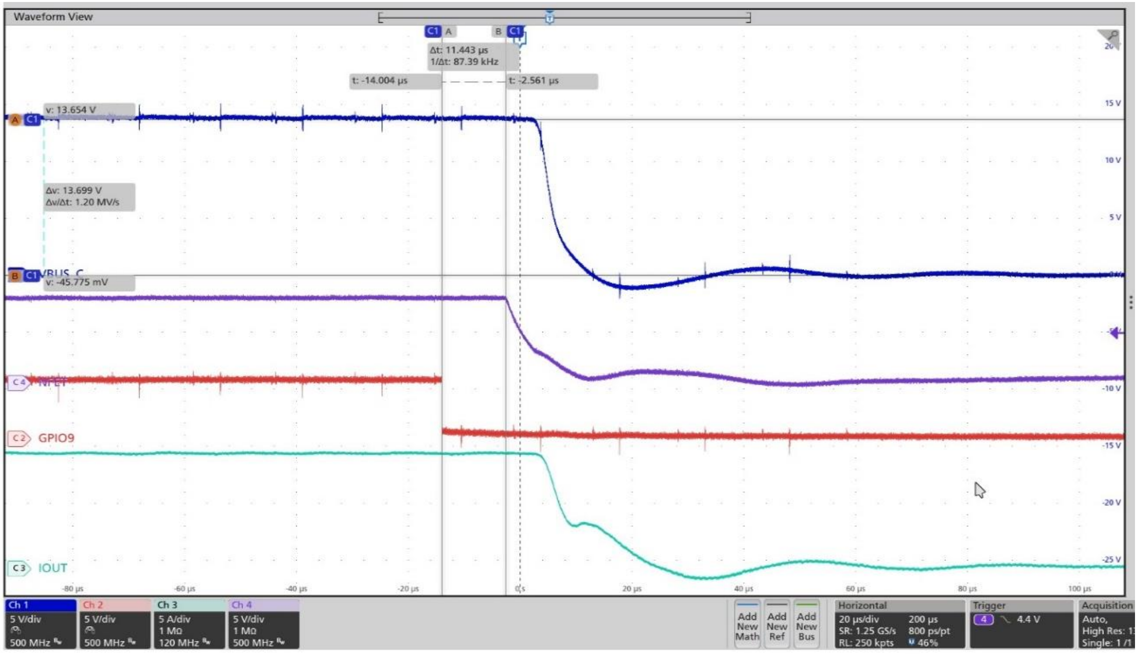
V_{out} = 9 V, UVP_limit = 6.1 V, UVP_response time = 11.5 µs

Figure 41 UVP at 115 V_{ac}, 60 Hz (CH4: NFET[5]; CH2: GPIO9; CH1: V_{bus_c}; CH3: I_{out}) (1 of 2)

[5] NFET - Provider FET (Q2) gate to source waveform.



V_{out} = 15 V, UVP_limit = 10.21 V, UVP_response time = 11.4 µs

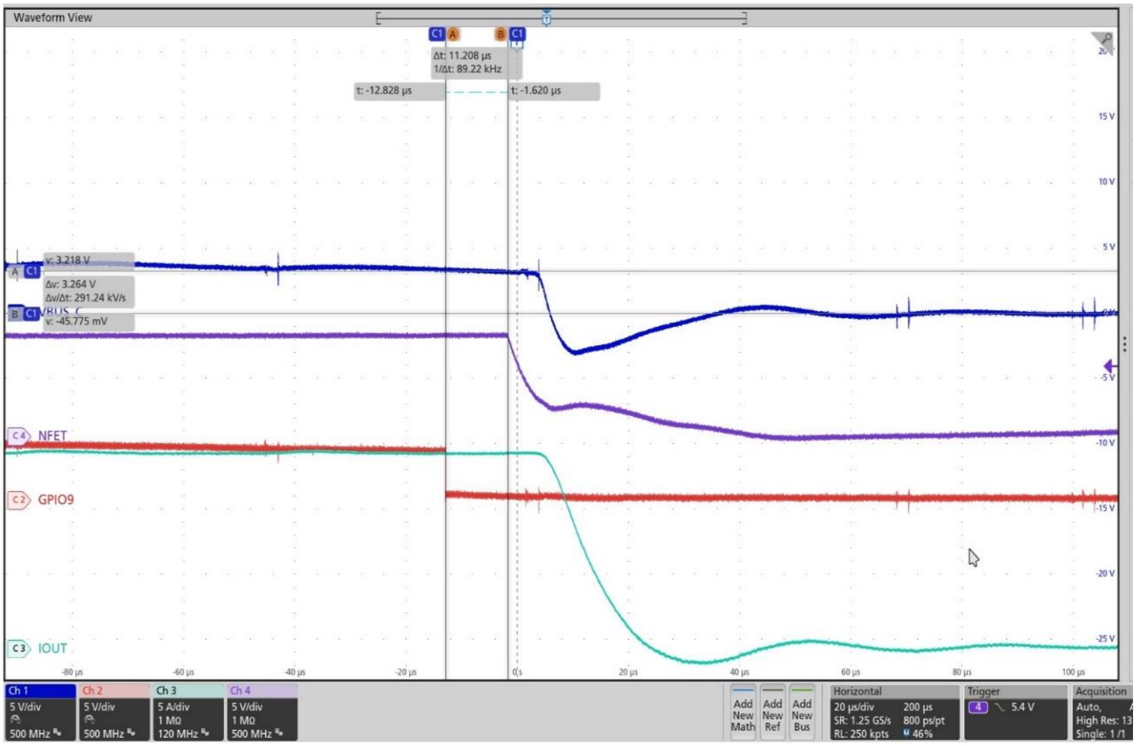


V_{out} = 20 V, UVP_limit = 13.65 V, UVP_response time = 11.4 µs

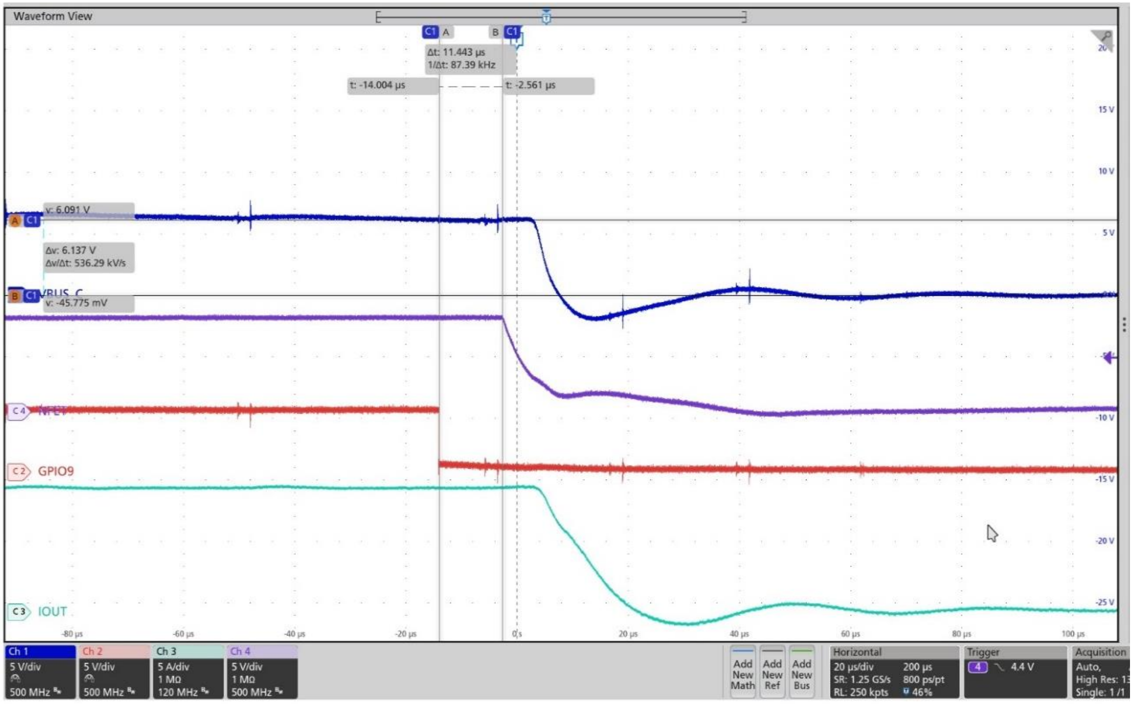
Figure 42 UVP at 115 V_{ac}, 60 Hz (CH4: NFET[6] ; CH2: GPIO9; CH1: V_{bus_c}; CH3: I_{out}) (2 of 2)

[6] NFET - Provider FET (Q2) gate to source waveform.

UVP tested at 230 V_{ac}, 50 Hz:



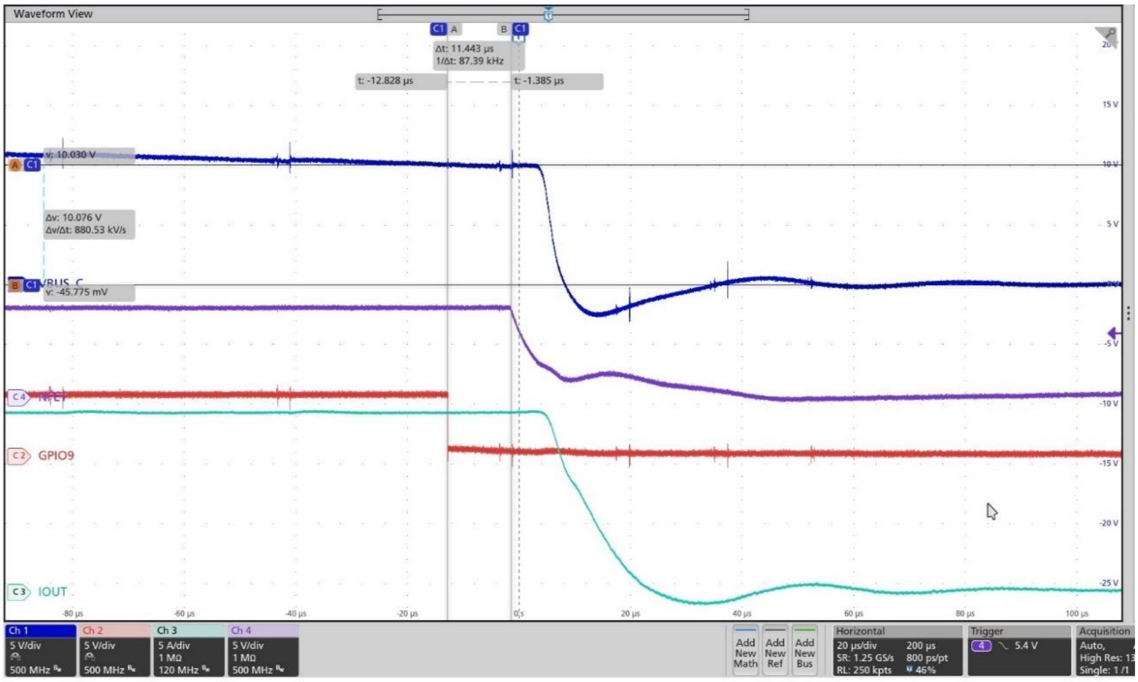
V_{out} = 5 V, UVP_limit = 3.21 V, UVP_response time = 11.2 µs



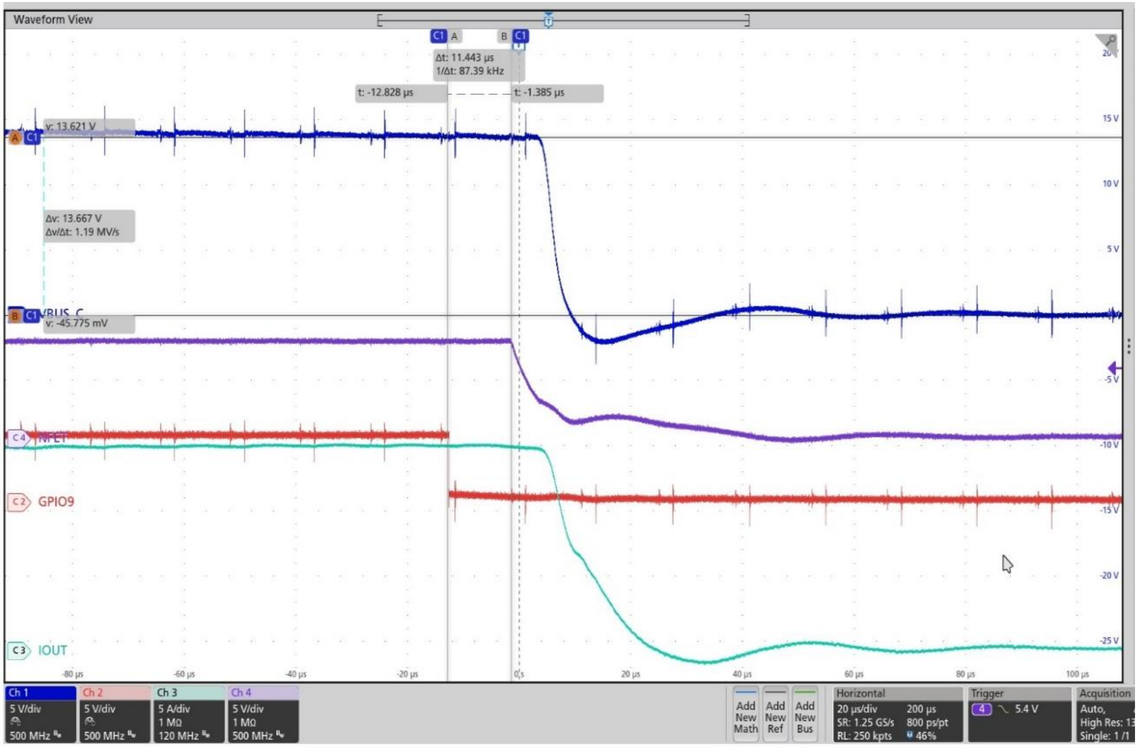
V_{out} = 9 V, UVP_limit = 6.09 V, UVP_response time = 11.4 µs

Figure 43 UVP at 230 V_{ac}, 50 Hz (CH4: NFET[7]; CH2: GPIO9; CH1: V_{bus_c}; CH3: I_{out}) (1 of 2)

[7] NFET - Provider FET (Q2) gate to source waveform.



V_{out} = 15 V, UVP_limit = 10.03 V, UVP_response time = 11.4 µs



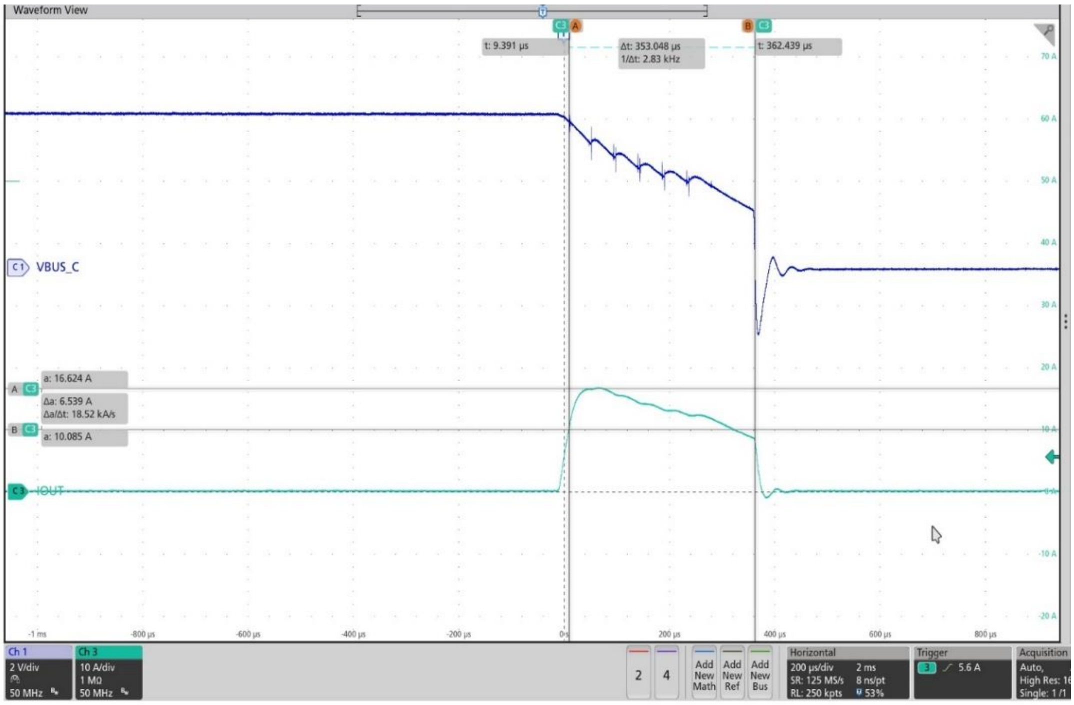
V_{out} = 20 V, UVP_limit = 13.6 V, UVP_response time = 11.4 µs

Figure 44 UVP at 230 V_{ac}, 50 Hz (CH4: NFET[8] ; CH2: GPIO9; CH1: V_{bus_c}; CH3: I_{out}) (2 of 2)

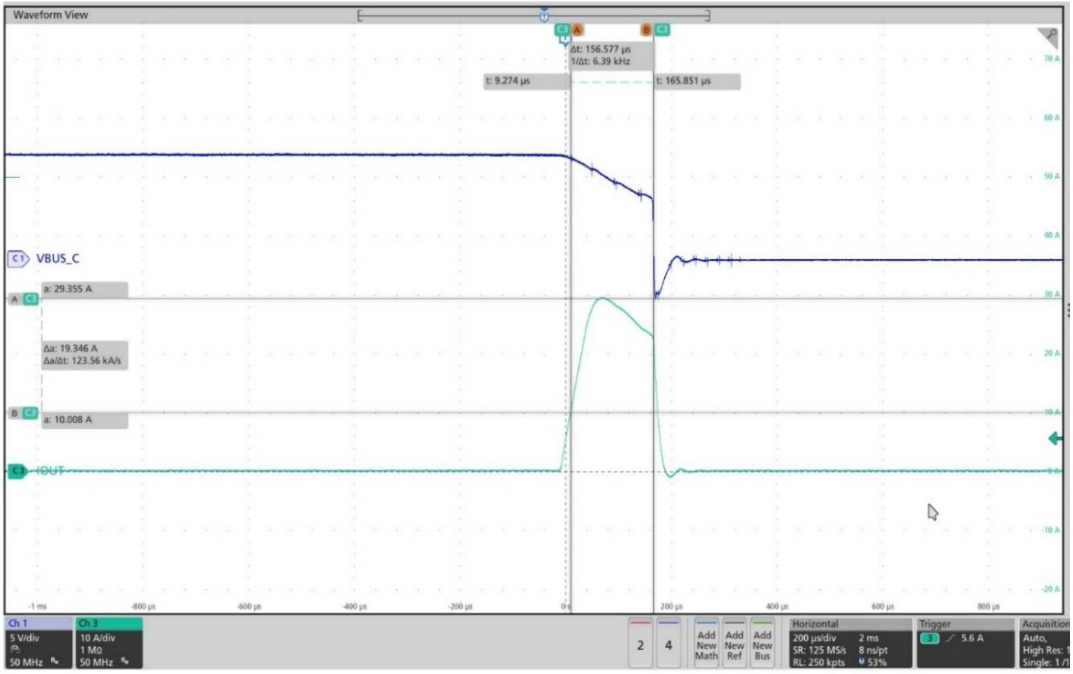
[8] NFET - Provider FET (Q2) gate to source waveform.

3.12 Short-circuit protection (SCP)

SCP tested at 115 V_{ac}, 60 Hz:



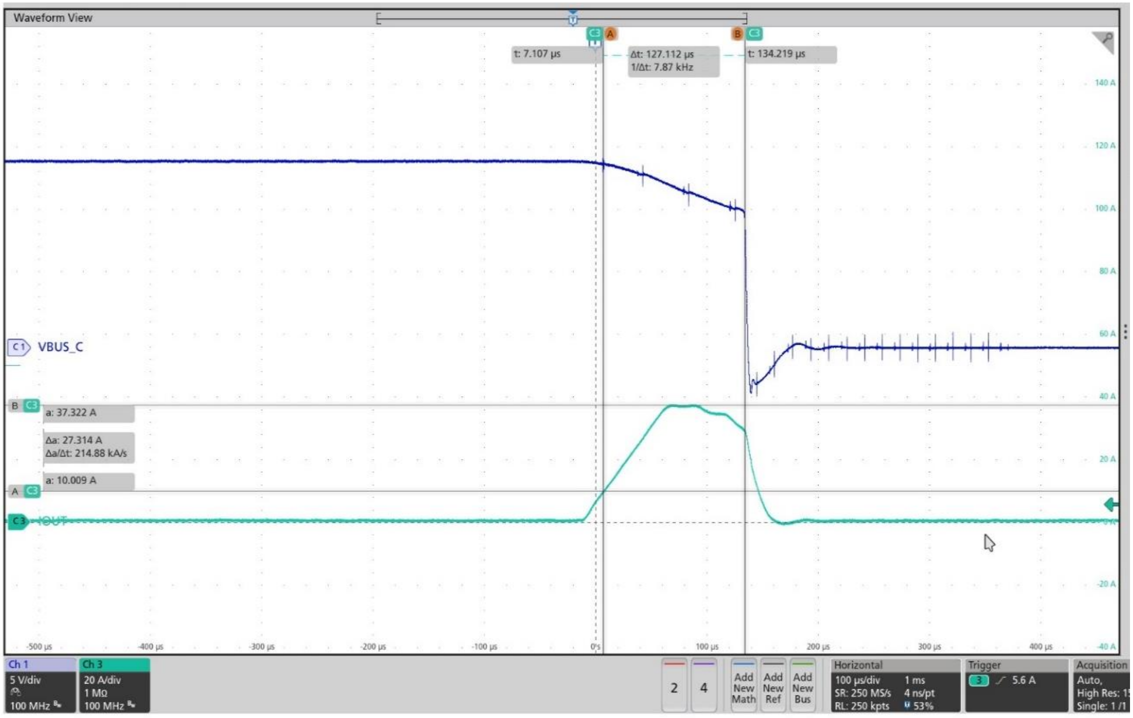
Fixed PDO = 5 V, 3 A; SCP_trip point = 10 A; SCP_response time[9] = 353.04 µs



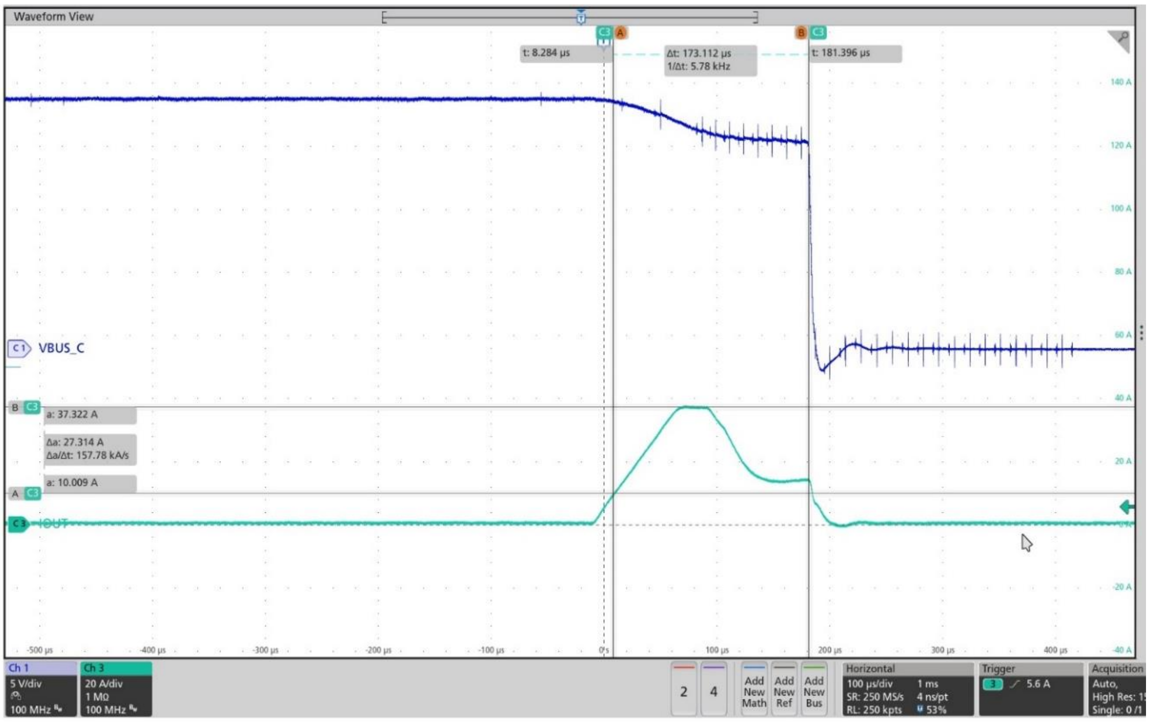
Fixed PDO = 9 V, 3 A; SCP_trip point = 10 A; SCP_response time[9] = 156.57 µs

Figure 45 SCP at 115 V_{ac}, 60 Hz (CH1: V_{bus_c}; CH3: I_{out}) (1 of 2)

[9] The SCP response time is increased due to the presence of the RC filter at the current sense resistor.



Fixed PDO = 15 V, 3 A; SCP_trip point = 10 A; SCP_response time[10] = 127.11 µs

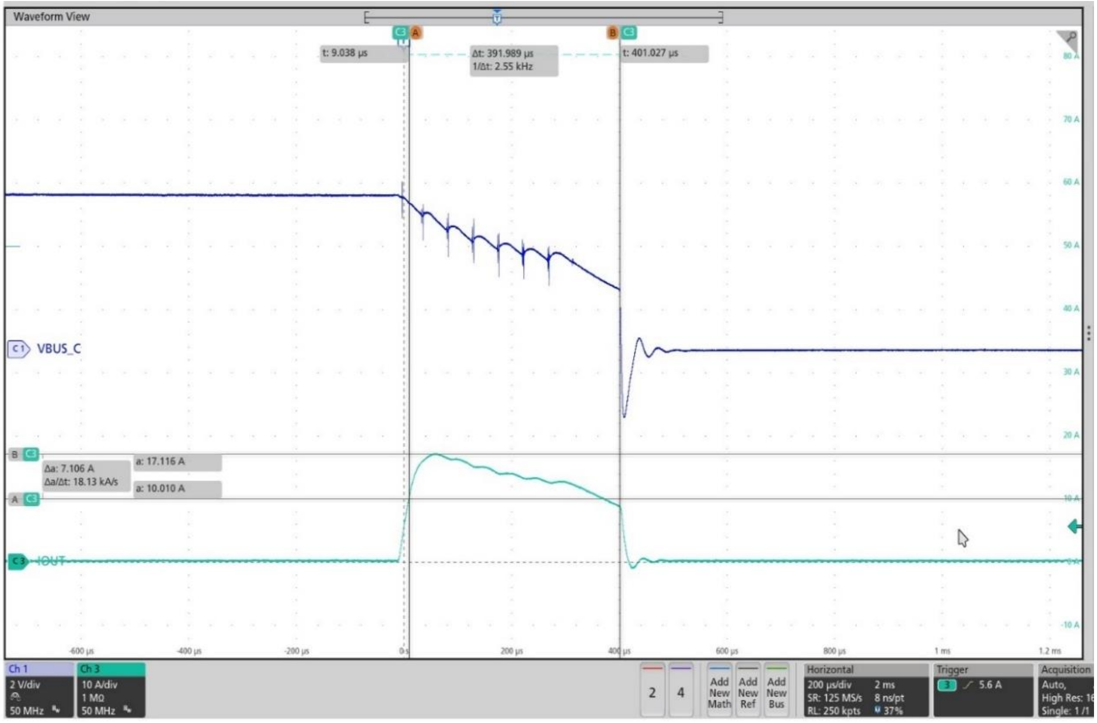


Fixed PDO = 20 V, 3.25 A; SCP_trip point = 10 A; SCP_response time[10] = 173.11 µs

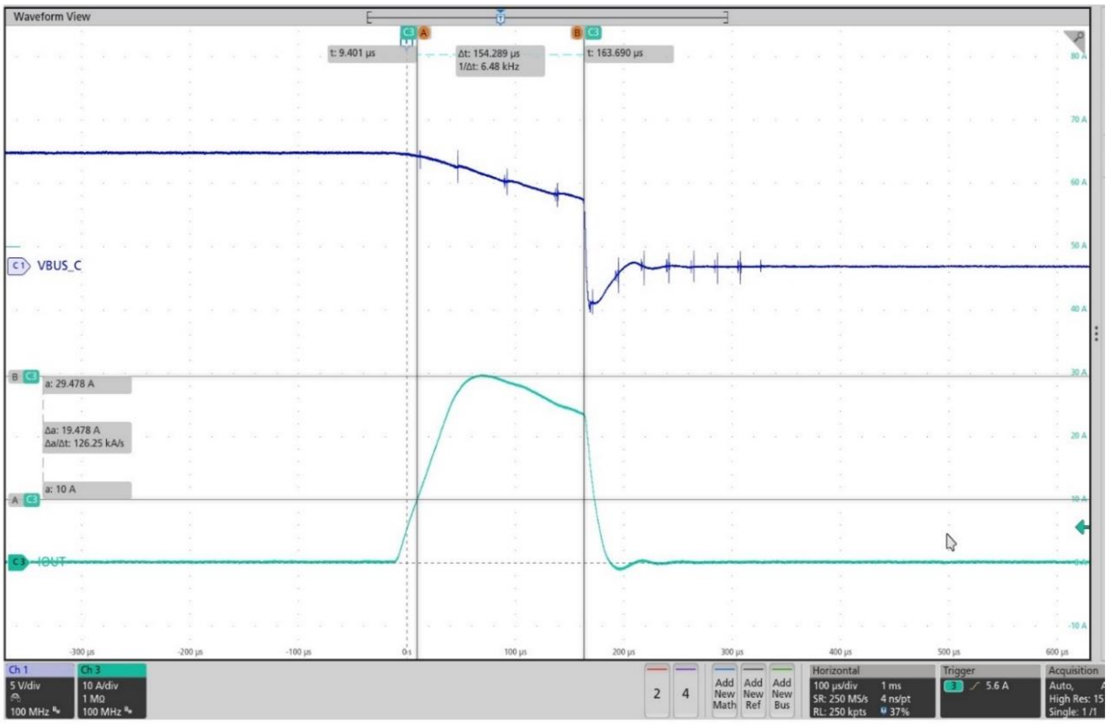
Figure 46 SCP at 115 V_{ac}, 60 Hz (CH1: V_{bus_c}; CH3: I_{out}) (2 of 2)

[10] The SCP response time is increased due to the presence of the RC filter at the current sense resistor.

SCP tested at 230 V$_{ac}$, 50 Hz:



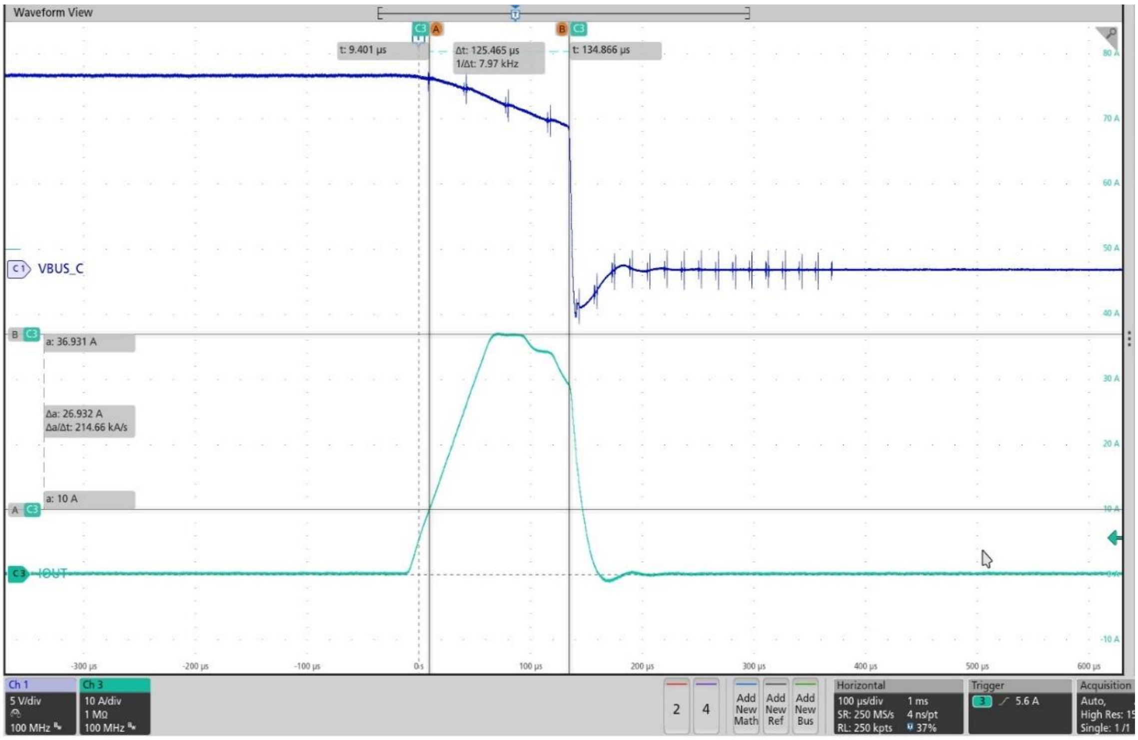
Fixed PDO = 5 V, 3 A; SCP_trip point = 10 A; SCP_response time[11] = 391.98 µs



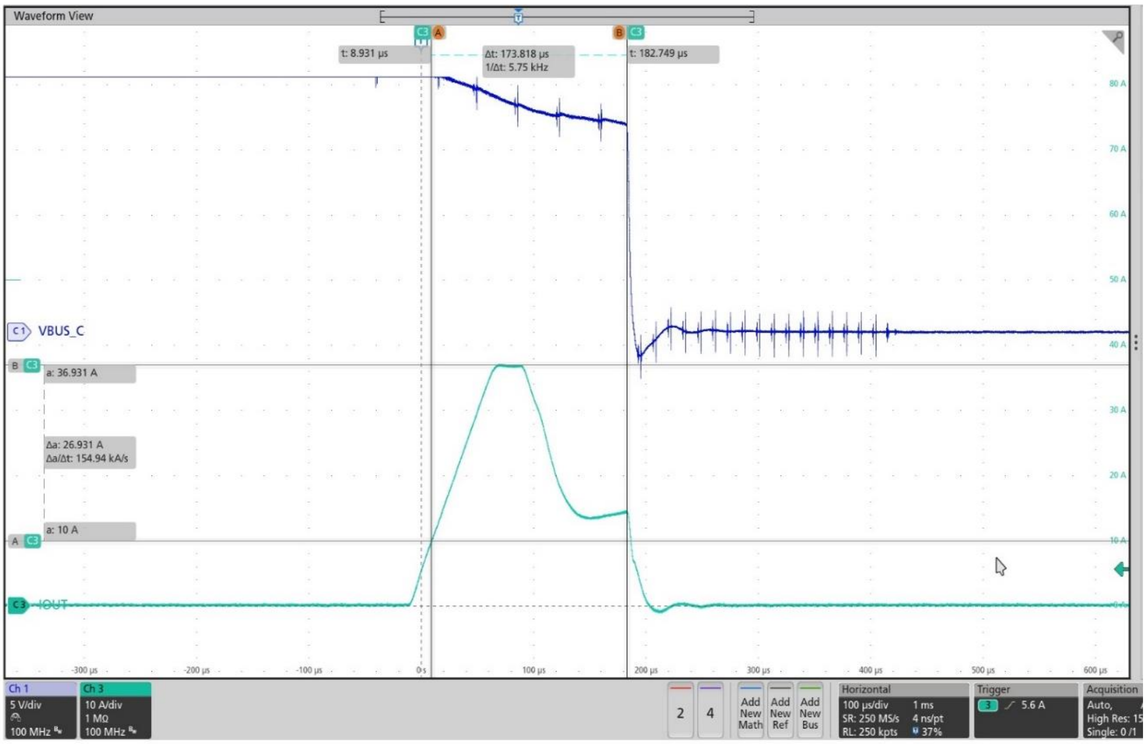
Fixed PDO = 9 V, 3 A; SCP_trip point = 10 A; SCP_response time[11] = 154.28 µs

Figure 47 SCP at 230 V$_{ac}$, 50 Hz (CH1: V$_{bus_c}$; CH3: I$_{out}$) (1 of 2)

[11] The SCP response time is increased due to the presence of the RC filter at the current sense resistor.



Fixed PDO = 15 V, 3 A; SCP_trip point = 10 A; SCP_response time[12] = 125.46 µs



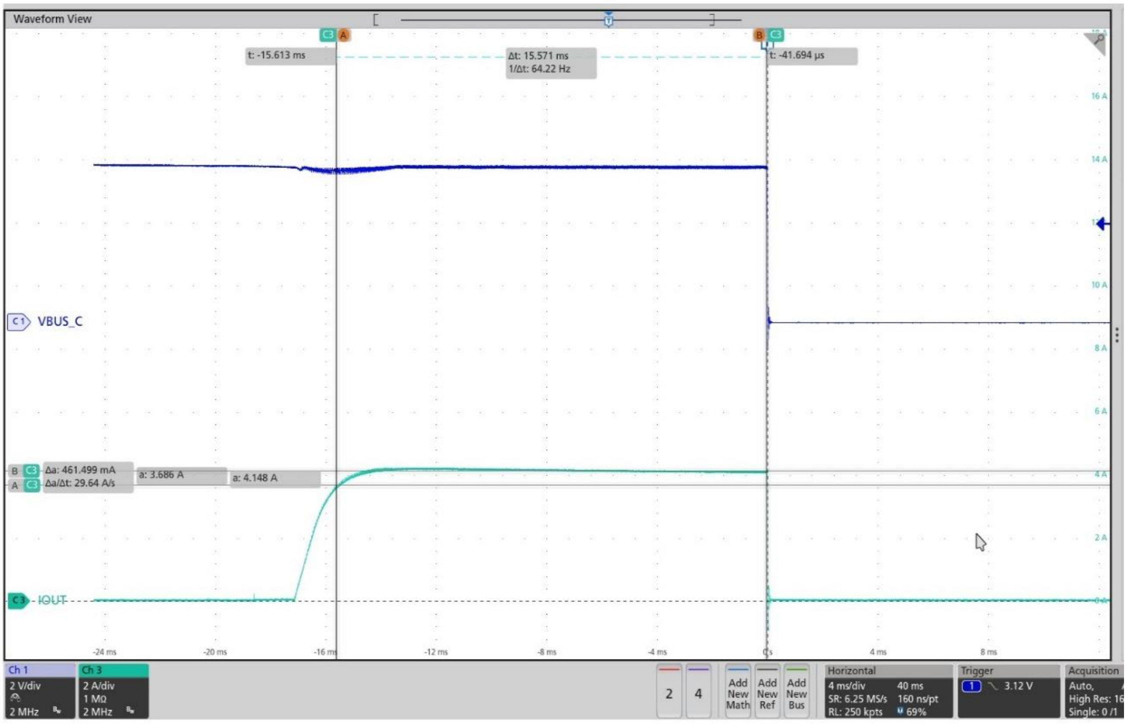
Fixed PDO = 20 V, 3.25 A; SCP_trip point = 10 A; SCP_response time[12] = 173.81 µs

Figure 48 SCP at 230 V_{ac}, 50 Hz (CH1: V_{bus_c}; CH3: I_{out}) (2 of 2)

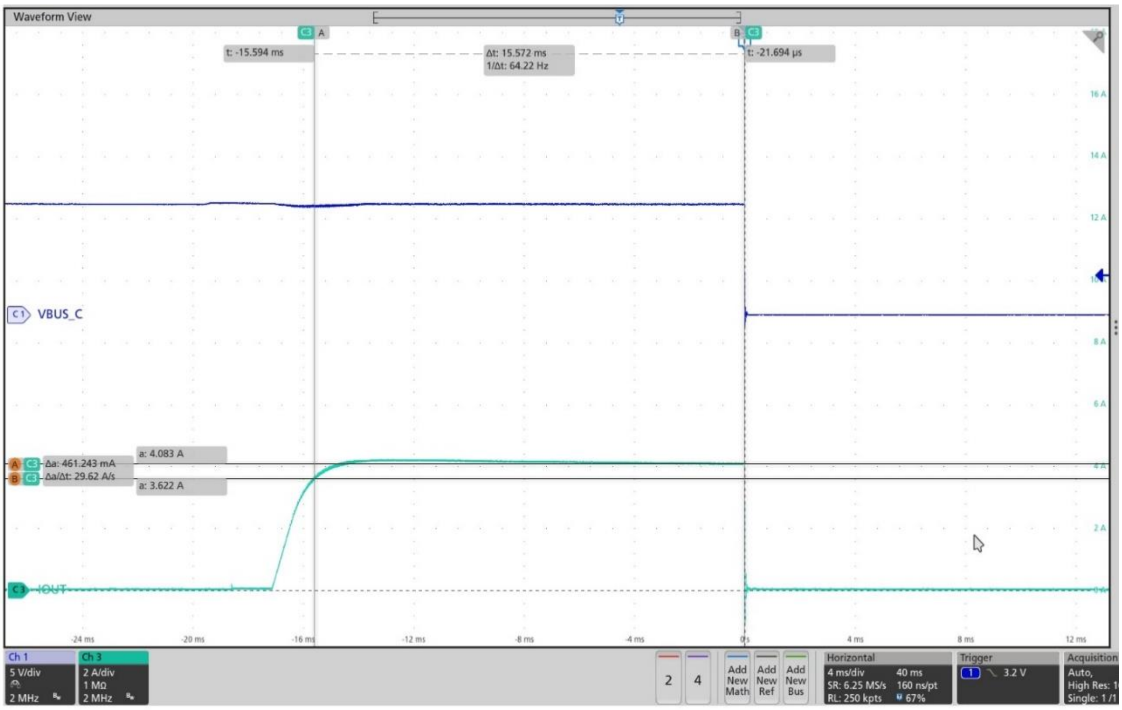
[12] The SCP response time is increased due to the presence of the RC filter at the current sense resistor.

3.13 Overcurrent protection (OCP)

OCP tested at 115 V_{ac}, 60 Hz:

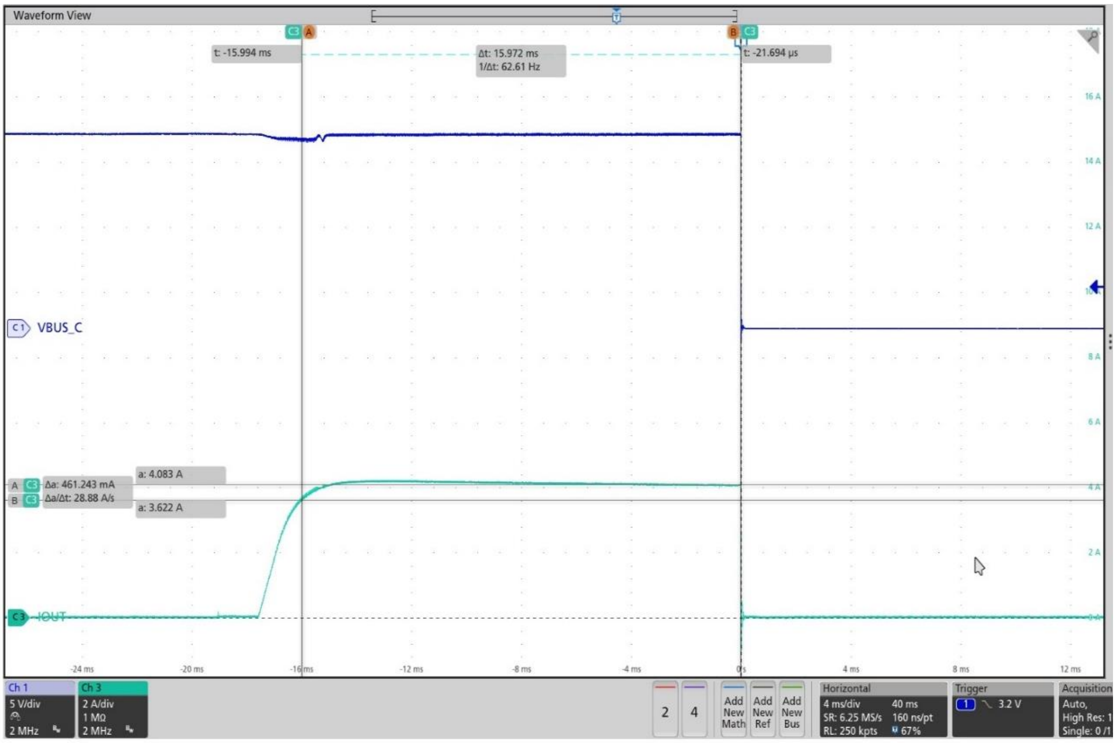


Fixed PDO: 5 V, 3 A; OCP_trip point = 3.69 A; OCP_response time = 15.5 ms

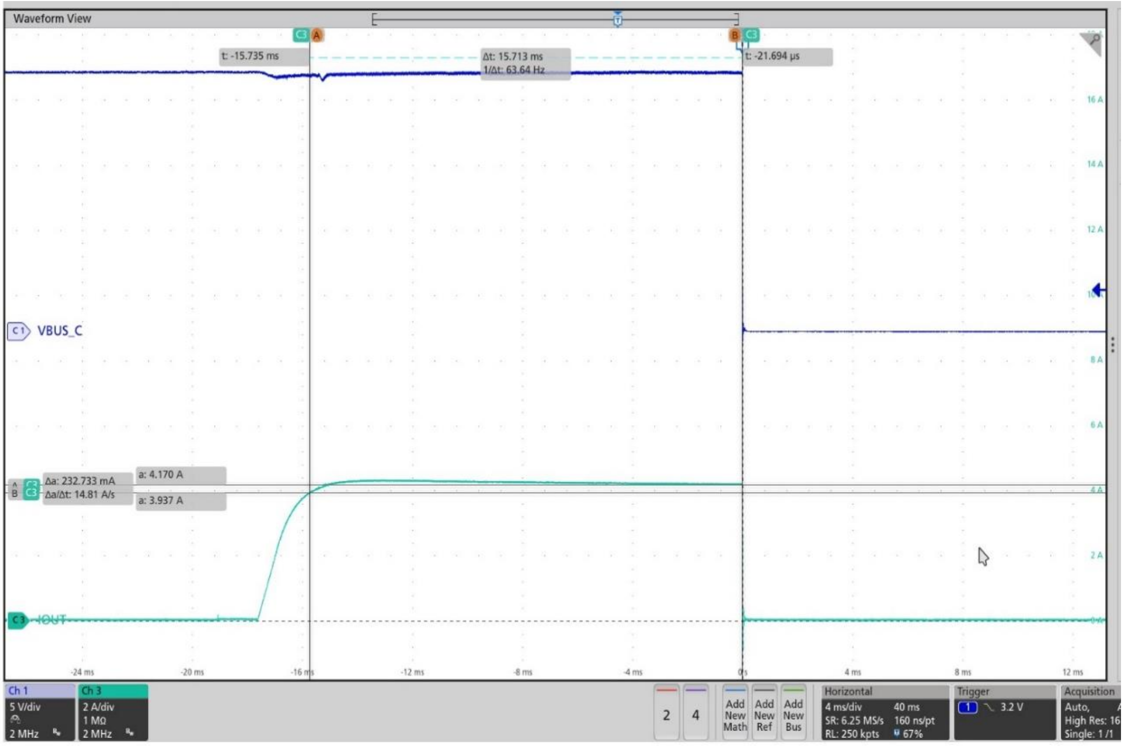


Fixed PDO: 9 V, 3 A; OCP_trip point = 3.62 A; OCP_response time = 15.75 ms

Figure 49 OCP at 115 V_{ac}, 60 Hz (CH1: V_{bus_c}; CH3: I_{out}) (1 of 2)



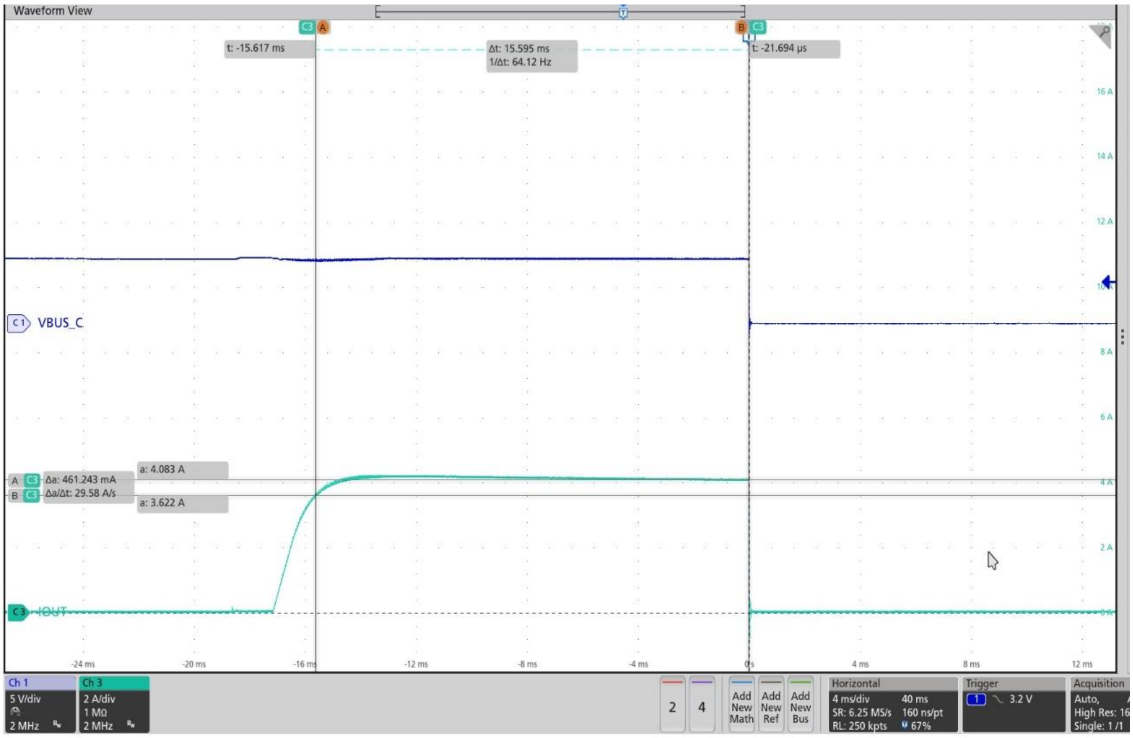
Fixed PDO: 15 V, 3 A; OCP_trip point = 3.62 A; OCP_response time = 15.97 ms



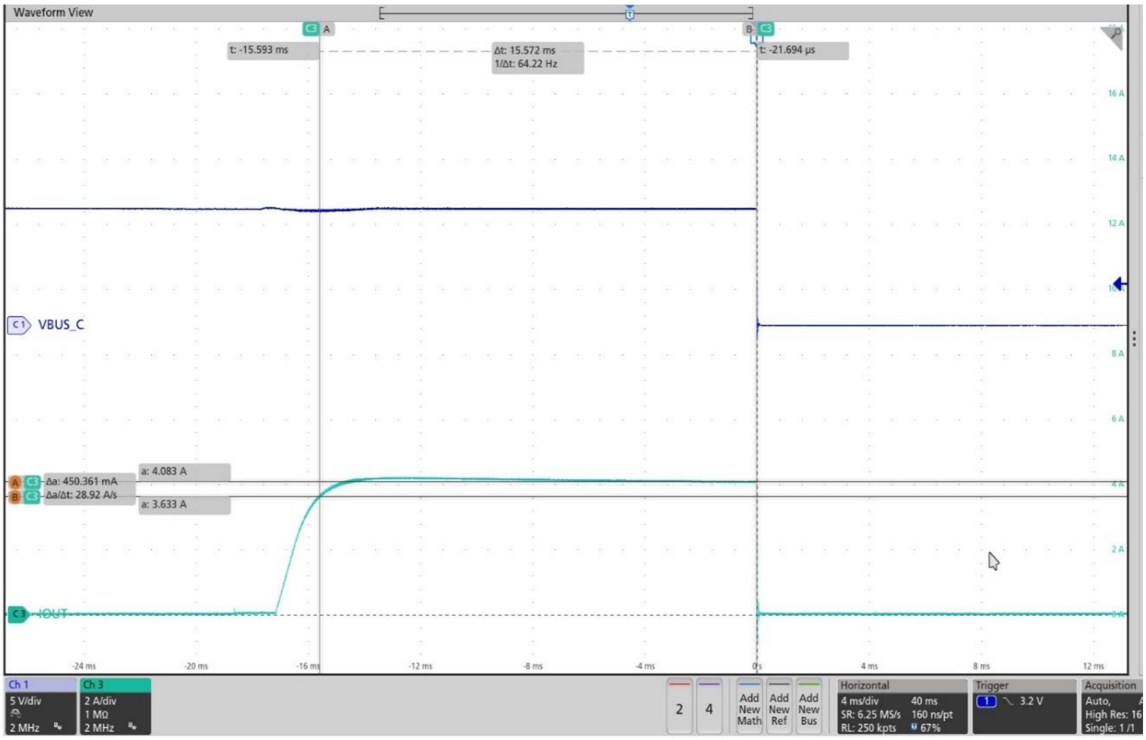
Fixed PDO: 20 V, 3.25 A; OCP_trip point = 3.94 A; OCP_response time = 15.71 ms

Figure 50 OCP at 115 V_{ac}, 60 Hz (CH1: V_{bus_c}; CH3: I_{out}) (2 of 2)

OCP tested at 230 V_{ac}, 50 Hz:

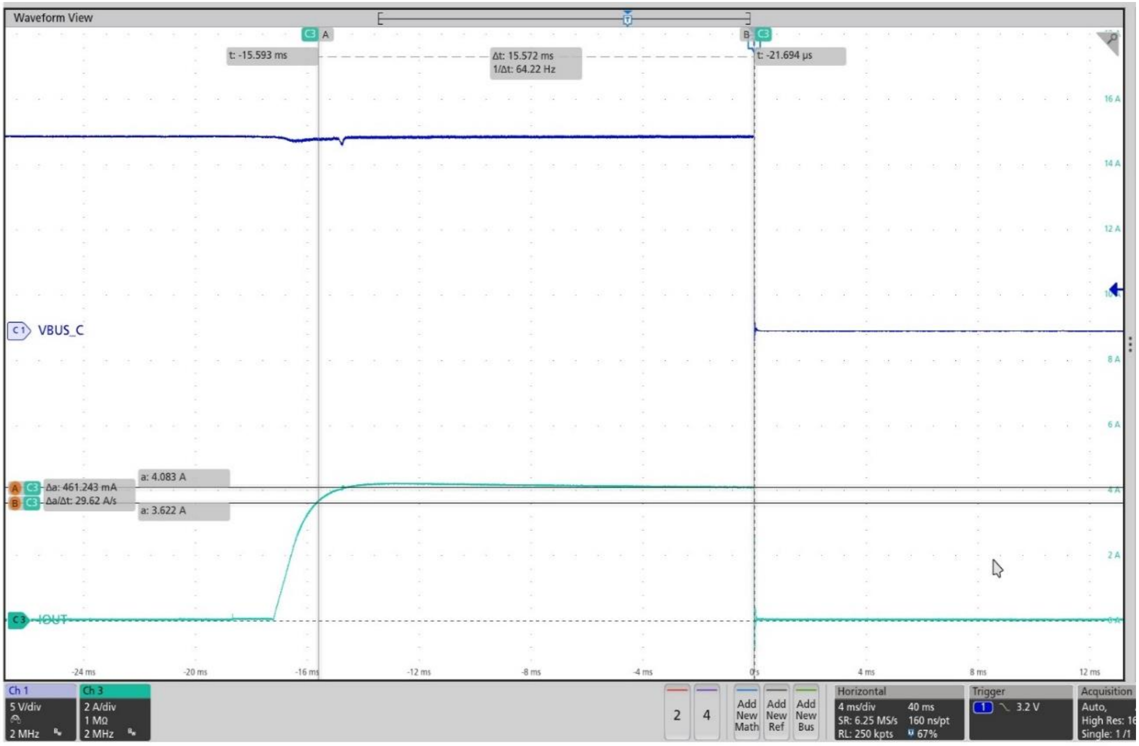


Fixed PDO: 5 V, 3 A; OCP_trip point = 3.62 A; OCP_response time = 15.10 ms

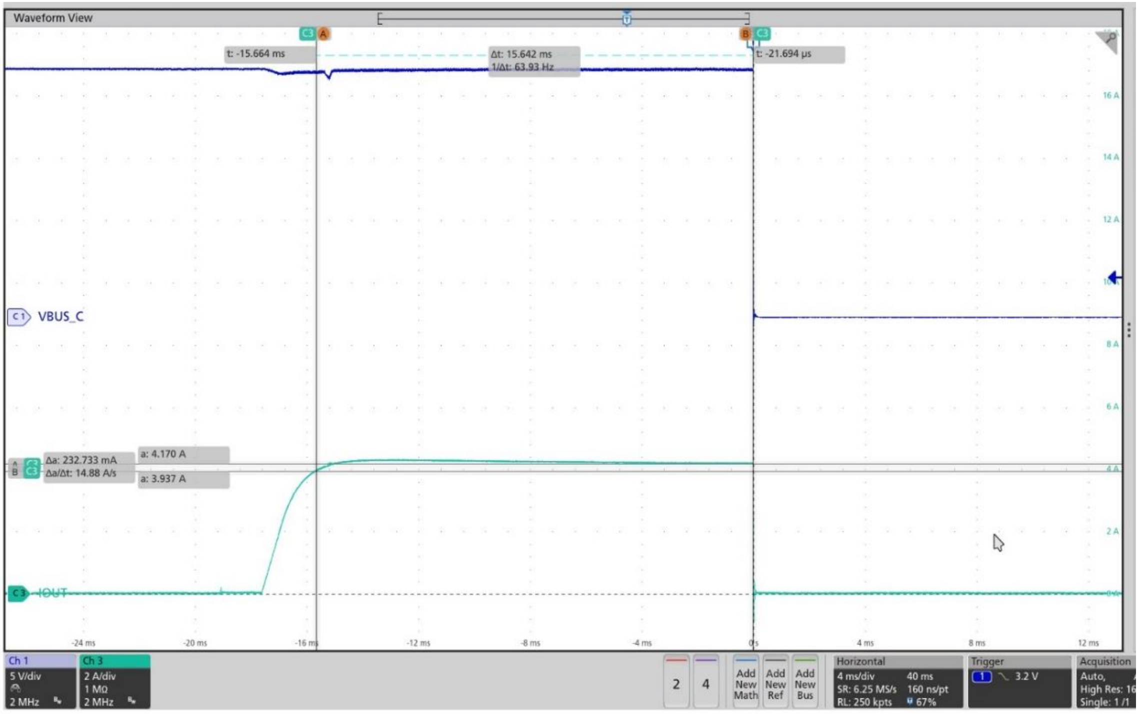


Fixed PDO: 9 V, 3 A; OCP_trip point = 3.63 A; OCP_response time = 15.57 ms

Figure 51 OCP at 230 V_{ac}, 50 Hz (CH1: V_{bus_c}; CH3: I_{out}) (1 of 2)



Fixed PDO: 15 V, 3 A; OCP_trip point = 3.62 A; OCP_response time = 15.57 ms



Fixed PDO: 20 V, 3.25 A; OCP_trip point = 3.94 A; OCP_response time = 15.64 ms

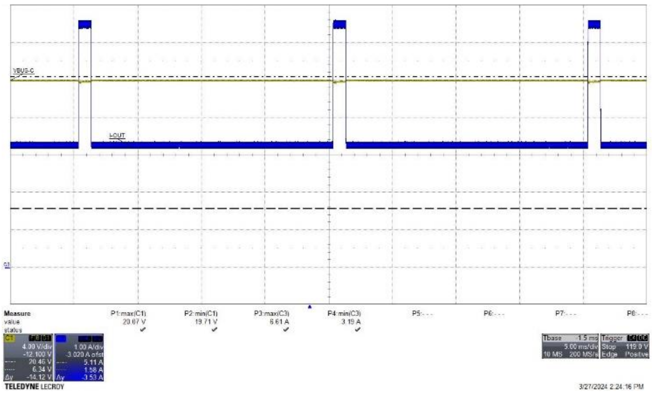
Figure 52 OCP at 230 V_{ac}, 50 Hz (CH1: V_{bus_c}; CH3: I_{out}) (2 of 2)

3.14 Peak overload test

- **Test condition:** V_{in_ac} = 90 V_{ac}, 47 Hz/115 V_{ac}, 60 Hz/230 V_{ac}, 50 Hz, V_{out} = 20 V, I_{out} = dynamic
- **Lab ambient temperature:** 23°C and in open frame
- **Pass/fail:** ±10% of 20 V (18.0 V–22.0 V)

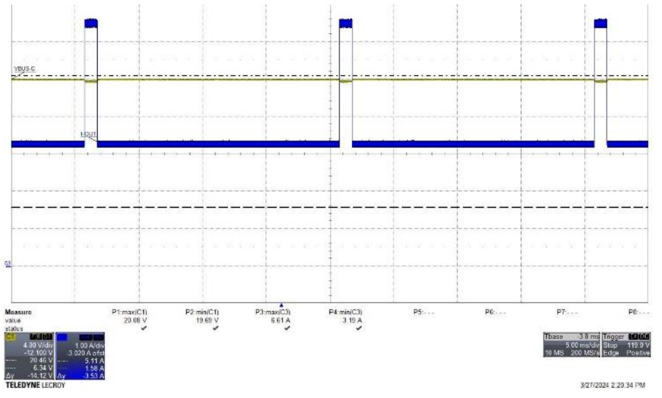
Case 1 (load transient)

- V_o = 20 V; (3.25 A) 100% load (19 ms) – (6.5 A) 200% load (1 ms)
- Slew rate = 500 mA/µs
- **Result = Pass**



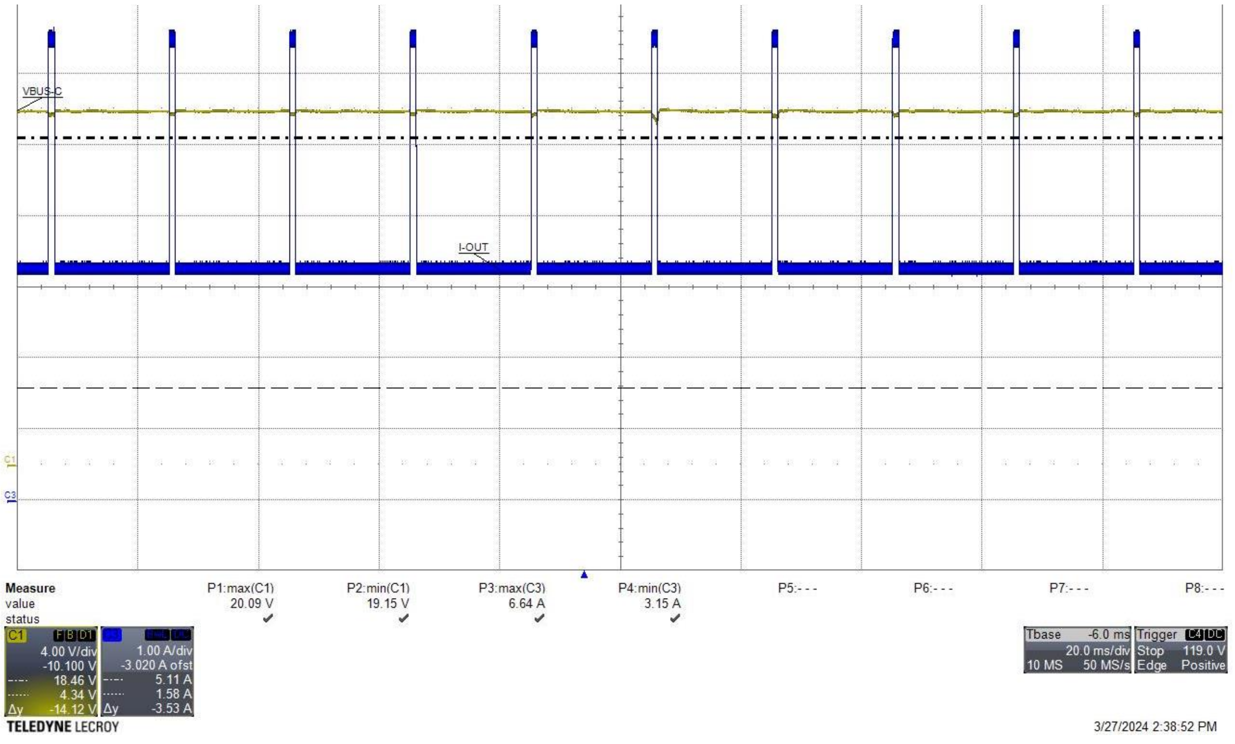
230 V_{ac}, 50 Hz, 20 V, 3.25 A (19 ms) – 6.5 A (1 ms)

V_{o-max} = 20.07 V; V_{o-min} = 19.71 V



115 V_{ac}, 60 Hz, 20 V, 3.25 A (19 ms) – 6.5 A (1 ms)

V_{o-max} = 20.08 V; V_{o-min} = 19.69 V



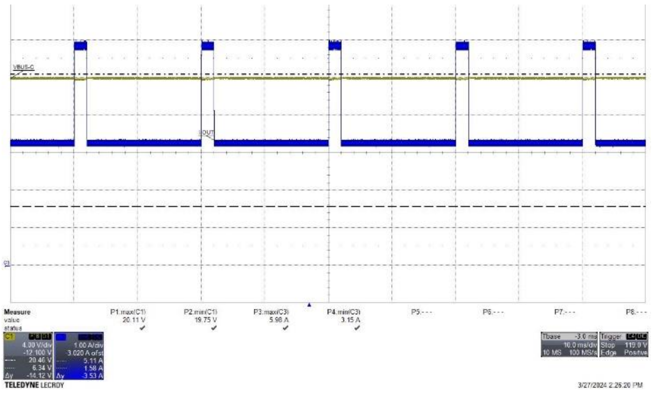
90 V_{ac} 47 Hz, 20 V 3.25 A (19 ms) – 6.5 A (1 ms)

V_{o-max} = 20.09 V; V_{o-min} = 19.15 V

Figure 53 Peak overload test for Case 1

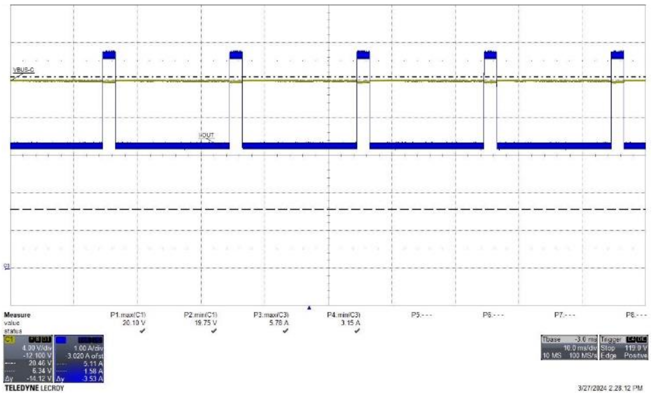
Case 2 (load transient)

- V_o = 20 V; (3.25 A) 100% load (18 ms) – (5.68 A) 175% load (2 ms)
- Slew rate = 500 mA/µs
- **Result = Pass**



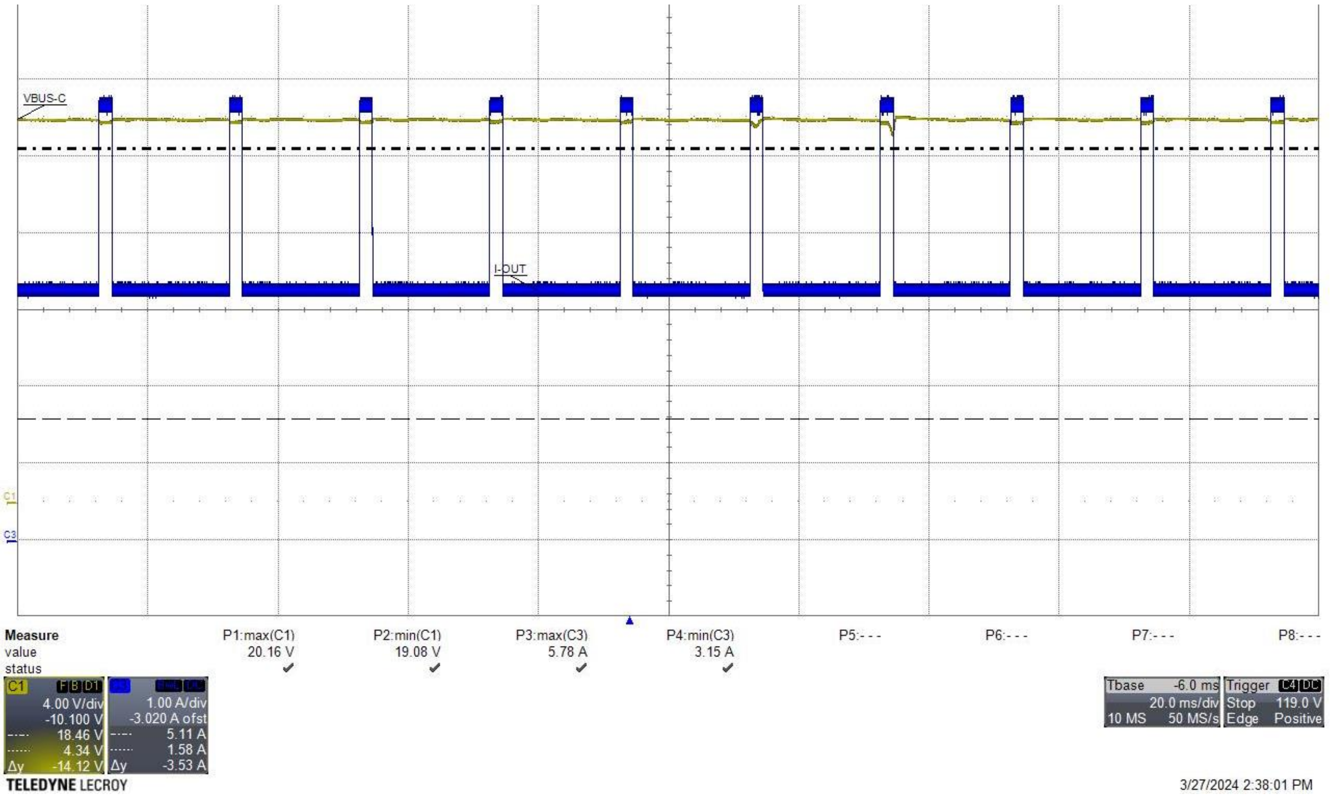
230 V$_{ac}$, 50 Hz, 20 V, 3.25 A (18 ms) – 5.68 A (2 ms)

$V_{o\text{-}max}$ = 20.11 V; $V_{o\text{-}min}$ = 19.75 V



115 V$_{ac}$, 60 Hz, 20 V, 3.25 A (18 ms) – 5.68 A (2 ms)

$V_{o\text{-}max}$ = 20.10 V; $V_{o\text{-}min}$ = 19.75 V



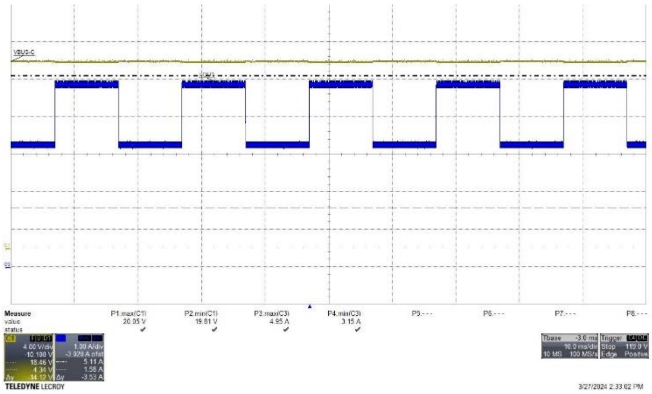
90 V$_{ac}$, 47 Hz, 20 V, 3.25 A (18 ms) – 5.68 A (2 ms)

$V_{o\text{-}max}$ = 20.16 V; $V_{o\text{-}min}$ = 19.08 V

Figure 54 Peak overload test for Case 2

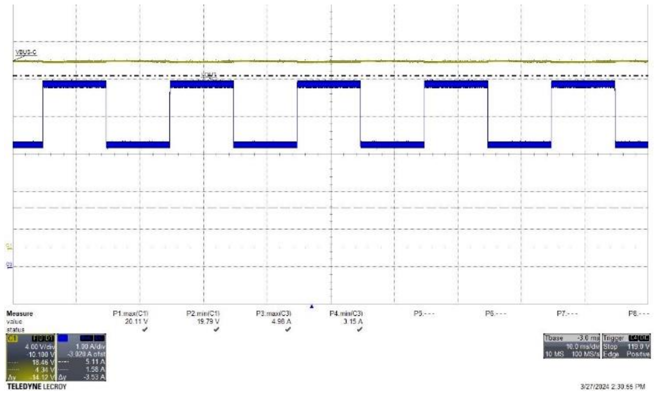
Case 3 (load transient)

- V_o = 20 V; (3.25 A) 100% load (10 ms) – (4.87 A) 150% load (10 ms)
- Slew rate = 500 mA/µs
- **Result = Pass**



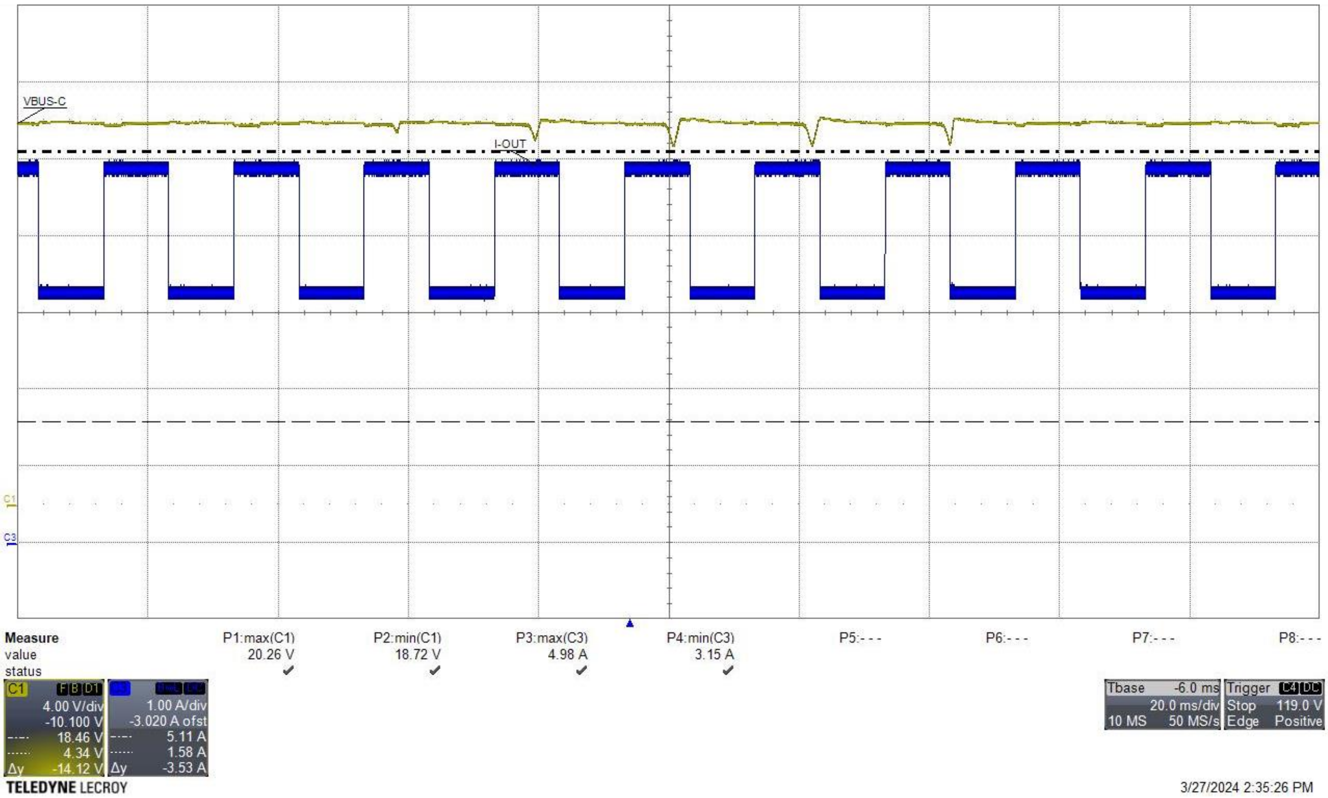
230 V_{ac}, 50 Hz, 20 V, 3.25 A (18 ms) – 5.68 A (2 ms)

$V_{o\text{-}max}$ = 20.05 V; $V_{o\text{-}min}$ = 19.81 V



115 V_{ac}, 60 Hz, 20 V, 3.25 A (18 ms) – 5.68 A (2 ms)

$V_{o\text{-}max}$ = 20.11 V; $V_{o\text{-}min}$ = 19.79 V



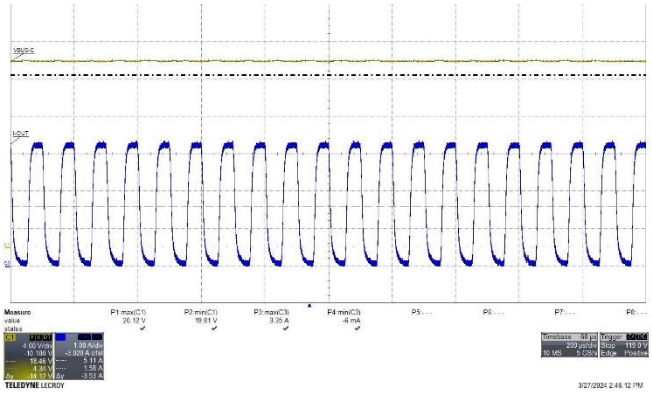
90 V_{ac} 47 Hz, 20 V, 3.25 A (18 ms) – 5.68 A (2 ms)

$V_{o\text{-}max}$ = 20.26 V; $V_{o\text{-}min}$ = 18.72 V

Figure 55 Peak overload test for Case 3

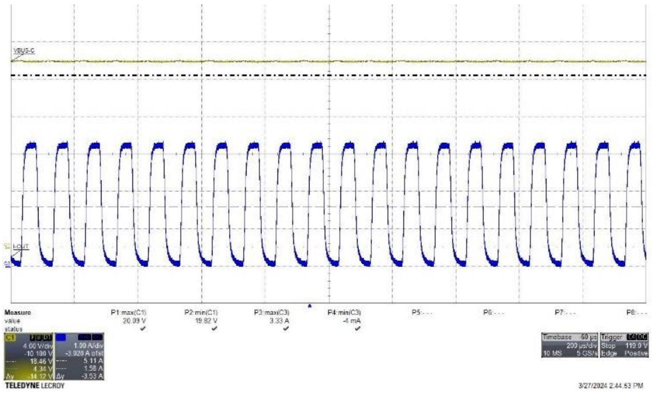
Case 4 (load transient)

- V_o = 20 V; (3.25 A) 100% load (50 µs) – (0.00 A) 0% load (50 µs)
- Slew rate = 500 mA/µs
- **Result = Pass**



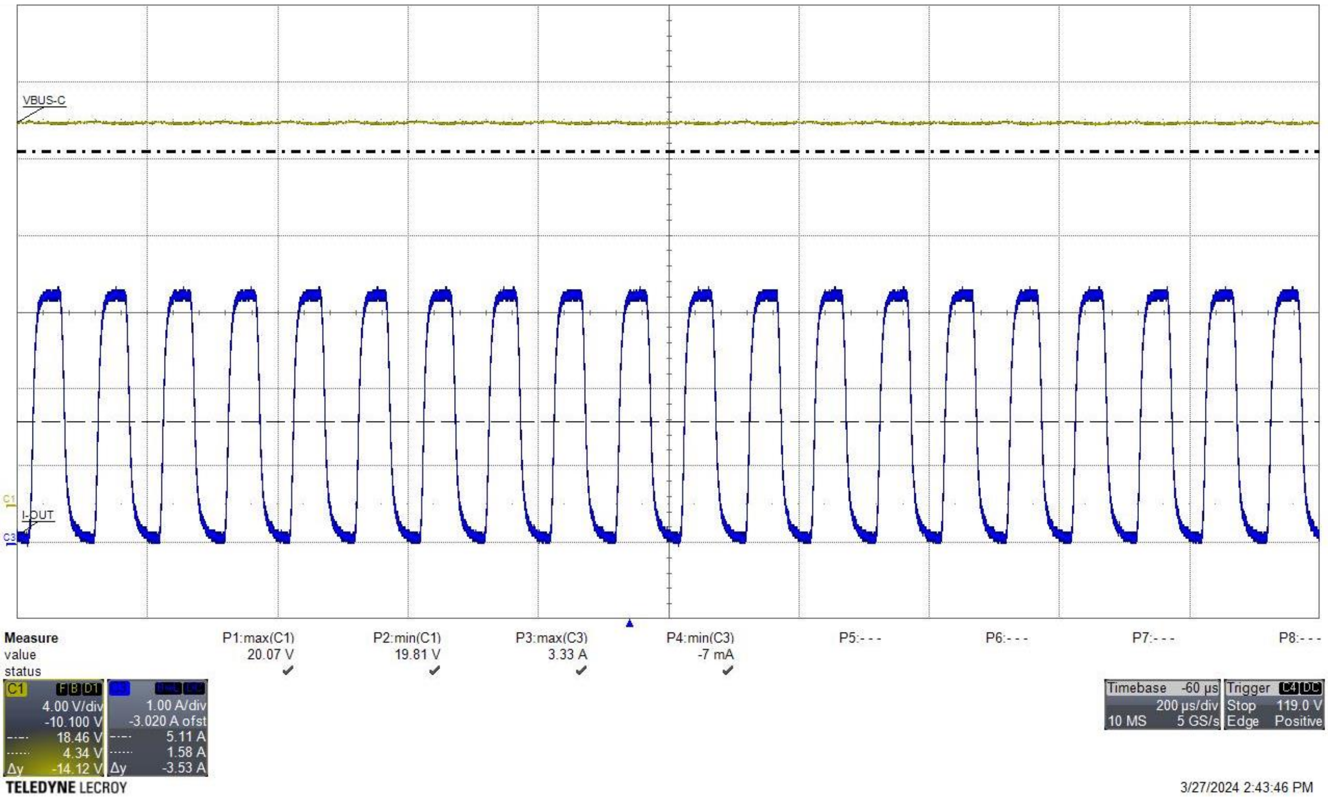
230 V_{ac}, 50 Hz, 20 V, 3.25 A (18 ms) – 5.68 A (2 ms)

$V_{o\text{-}max}$ = 20.12 V; $V_{o\text{-}min}$ = 19.81 V



115 V_{ac}, 60 Hz, 20 V, 3.25 A (18 ms) – 5.68 A (2 ms)

$V_{o\text{-}max}$ = 20.09 V; $V_{o\text{-}min}$ = 19.82 V



90 V_{ac}, 47 Hz, 20 V, 3.25 A (18 ms) – 5.68 A (2 ms)

$V_{o\text{-}max}$ = 20.07 V; $V_{o\text{-}min}$ = 19.81 V

Figure 56 Peak overload test for Case 4

3.15 Thermal stress

- **Test condition:** V_{in_ac} = 90 V_{ac}, 47 Hz, V_{out} = 20 V, I_{out} = 3.25 A
- **Lab ambient temperature:** 23°C and in open frame
- **Run time:** 60 minutes

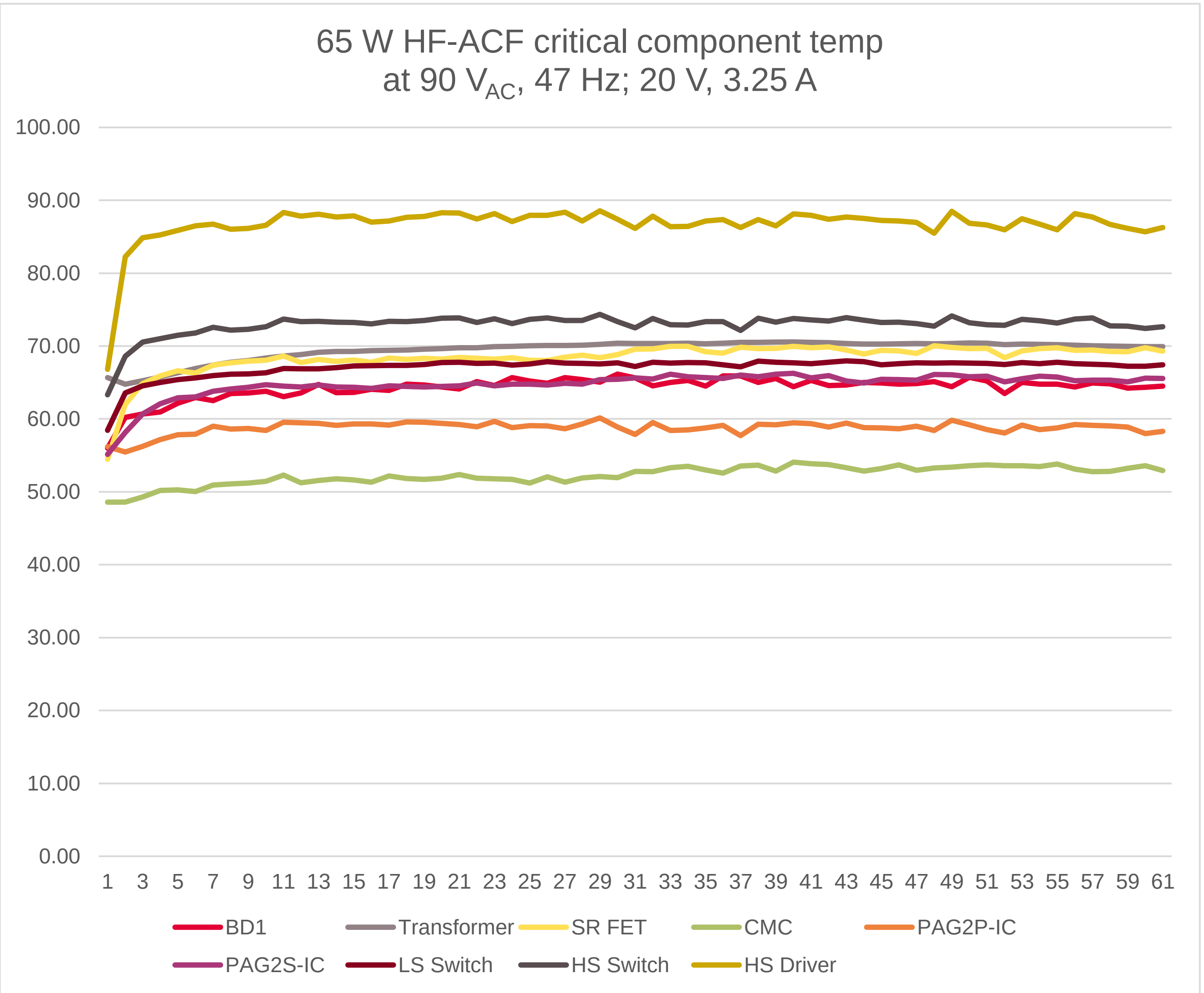


Figure 57 Thermal data logging of various components with time at 90 V_{ac}, 47 Hz; 20 V, 3.25 A

Table 13 Thermal data logging of various components at the end of 60 mins at 90 V_{ac}, 47 Hz; 20 V, 3.25 A

Sl. No.	Component	Max temp in °C at the end of 60 mins
1	Bridge rectifier	89.83
2	SR FET	76.99
3	CMC	72.59
4	Transformer	69.21
5	PAG2P (primary IC)	69.22
6	PAG2S (secondary IC)	67.30
7	Low side switch	95.37
8	High side switch	89.11
9	High side driver	88.09

- **Test condition:** V_{in_ac} = 265 V_{ac}, 63 Hz, V_{out} = 20 V, I_{out} = 3.25 A
- **Lab ambient temperature:** 23°C and in open frame
- **Run time:** 60 minutes

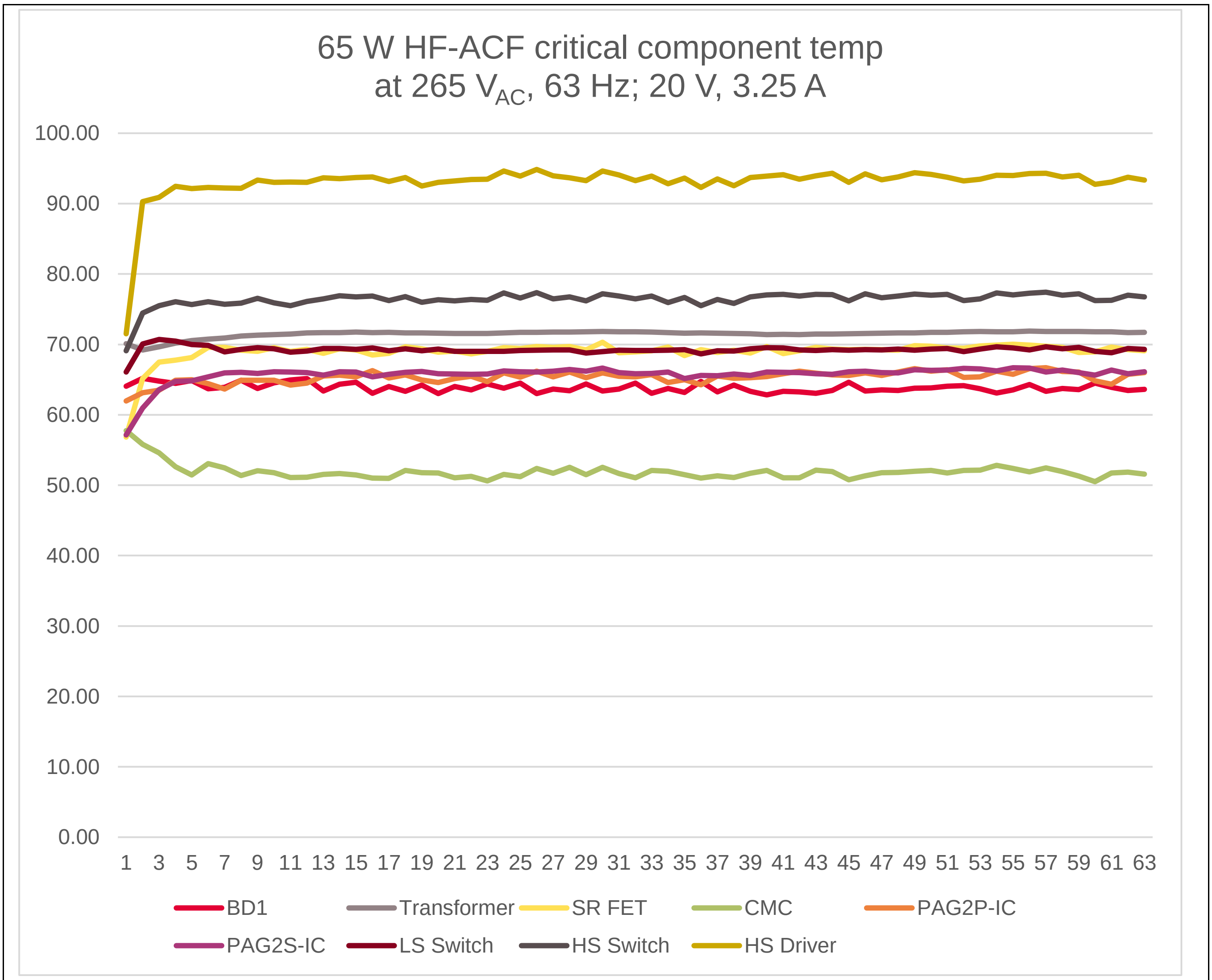


Figure 58 Thermal data logging of various components with time at 265 V_{ac}, 63 Hz; 20 V, 3.25 A

Table 14 Thermal data logging of various components at the end of 60 mins at 265 V_{ac}, 63 Hz; 20 V, 3.25 A

Sl. No.	Component	Max temp in °C at the end of 60mins
1	Bridge rectifier	63.89
2	SR FET	71.80
3	CMC	69.63
4	Transformer	51.74
5	PAG2P (primary IC)	64.33
6	PAG2S (secondary IC)	66.35
7	Low side switch	68.83
8	High side switch	76.26
9	High side driver	93.05

- **Test condition:** V_{in_ac} = 115 V_{ac}, 60 Hz, V_{out} = 20 V, I_{out} = 3.25 A
- **Lab ambient temperature:** 23°C and in open frame
- **Run time:** 60 minutes

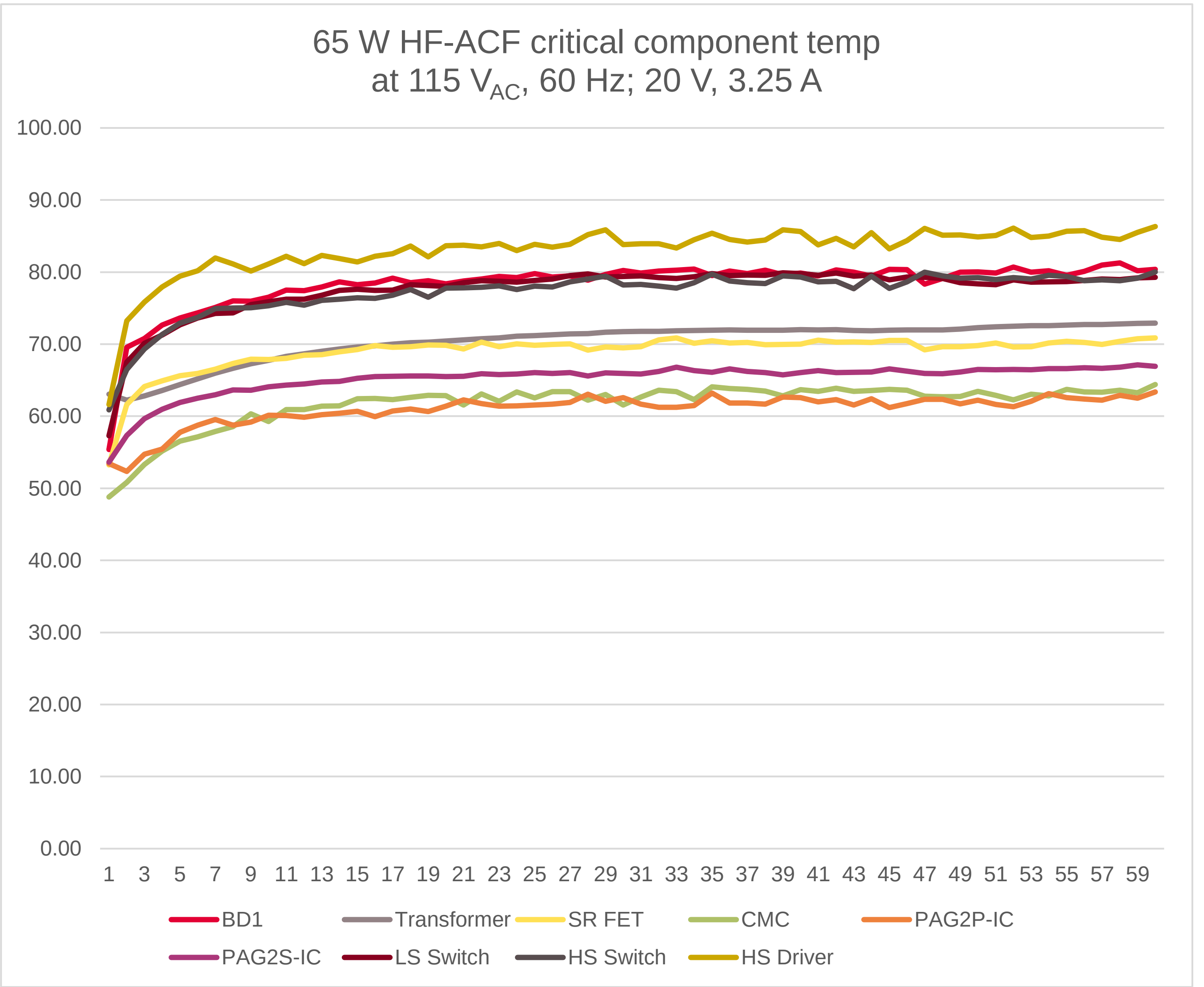


Figure 59 Thermal data logging of various components with time at 115 V_{ac}, 60 Hz; 20 V, 3.25 A

Table 15 Thermal data logging of various components at the end of 60 mins at 115 V_{ac}, 60 Hz; 20 V, 3.25 A

Sl. No.	Component	Max temp in °C at the end of 60 mins
1	Bridge rectifier	80.36
2	SR FET	72.92
3	CMC	70.85
4	Transformer	64.40
5	PAG2P (primary IC)	63.37
6	PAG2S (secondary IC)	66.93
7	Low side switch	79.26
8	High side switch	80.02
9	High side driver	86.32

- **Test condition:** V_{in_ac} = 230 V_{ac}, 50 Hz, V_{out} = 20 V, I_{out} = 3.25 A
- **Lab ambient temperature:** 23°C and in open frame
- **Run time:** 60 minutes

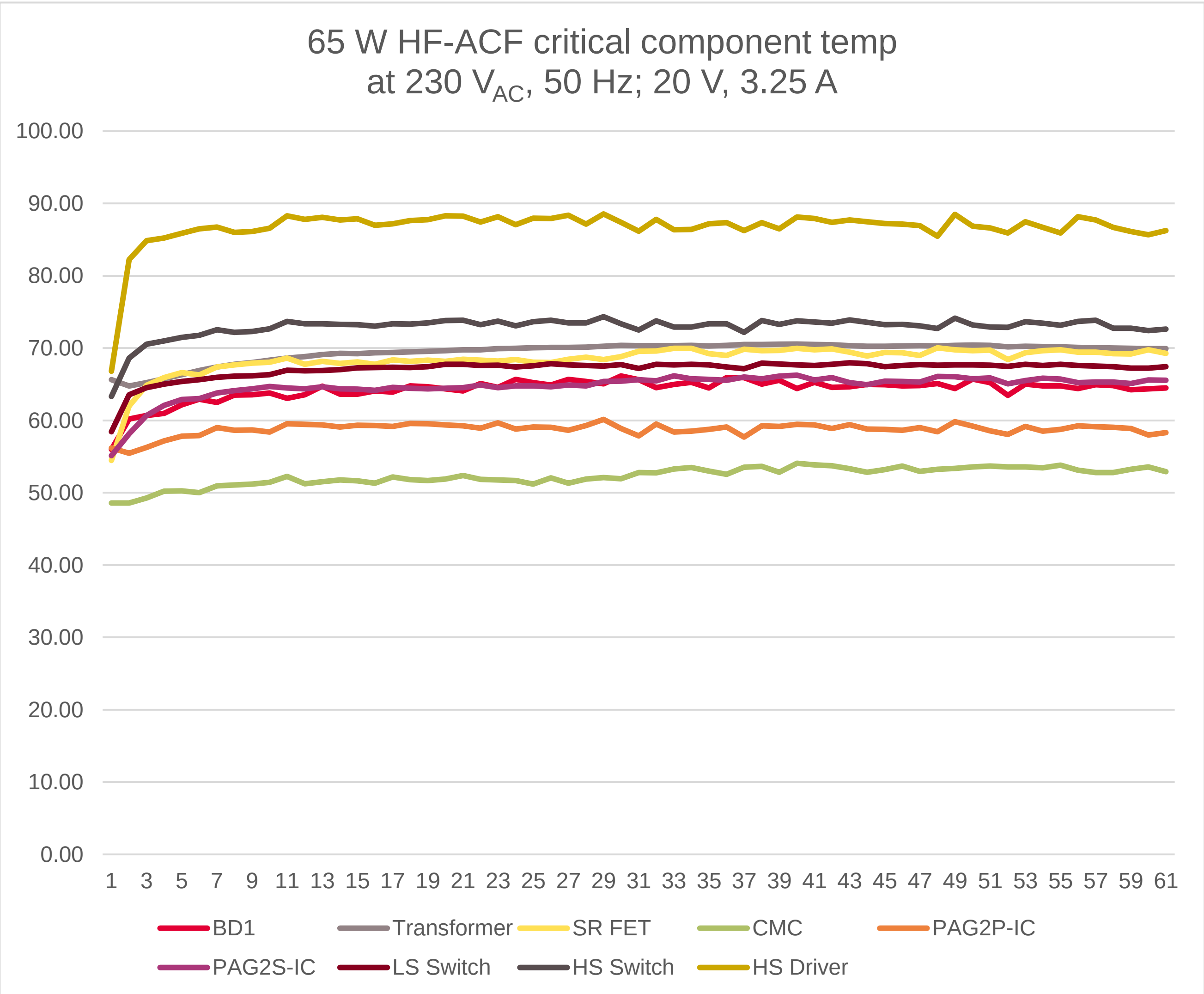


Figure 60 Thermal data logging of various components with time at 230 V_{ac}, 50 Hz; 20 V, 3.25 A

Table 16 Thermal data logging of various components at the end of 60 mins at 265 V_{ac}, 63 Hz; 20 V, 3.25 A

Sl. No.	Component	Max temp in °C at the end of 60 mins
1	Bridge rectifier	64.51
2	SR FET	69.93
3	CMC	69.29
4	Transformer	52.93
5	PAG2P (primary IC)	58.30
6	PAG2S (secondary IC)	65.54
7	Low side switch	67.42
8	High side switch	72.64
9	High side driver	86.27

3.16 EMI/EMC

3.16.1 Conducted emission (CE)

Conducted emission (CE) on 115 V_{ac} and 230 V_{ac} mains port, spectral diagram, 0.15 – 30 MHz.

Note: *The CE results are recorded with an additional shield on the transformer and terminated to primary GND. The X-Cap and CMC are shielded but not grounded.*

Conducted emission L1 at 230 V_{ac}, 50 Hz:

	Frequency [MHz]	Avg [dBµV]	Limit 55032bav [dBµV]	Delta [dB]	QPeak [dBµV]	Limit 55032bqp [dBµV]	Delta [dB]
1	0.238	42.83	52.17	---	53.37	62.17	-8.80
2	0.242	44.18	52.03	-7.85	55.40	62.03	-6.63
3	0.246	39.75	51.89	---	56.64	61.89	-5.25
4	0.486	37.35	46.24	-8.89	37.87	56.24	---

QP: 5.25 dB - Pass

Figure 61 CE at 230 V_{ac}, 20 V full load with trace L1

Conducted emission L2 at 230 V_{ac}, 50 Hz:

	Frequency [MHz]	Avg [dBµV]	Limit 55032bav [dBµV]	Delta [dB]	QPeak [dBµV]	Limit 55032bqp [dBµV]	Delta [dB]
1	0.242	45.49	52.03	-6.54	54.70	62.03	-7.33
2	0.246	42.93	51.89	-8.96	55.79	61.89	-6.10
3	0.25	21.83	51.76	---	53.59	61.76	-8.17
4	0.486	38.55	46.24	-7.69	38.64	56.24	---

QP: 6.1 dB - Pass

Figure 62 CE at 230 V_{ac}, 20 V full load with trace L2

Conducted emission L1 at 115 V_{ac}, 60 Hz:

	Frequency [MHz]	Avg [dBµV]	Limit 55032bav [dBµV]	Delta [dB]	QPeak [dBµV]	Limit 55032bqp [dBµV]	Delta [dB]
1	0.258	37.62	51.50	---	53.48	61.50	-8.02
2	0.262	34.47	51.37	---	54.36	61.37	-7.01
3	0.266	33.18	51.24	---	54.73	61.24	-6.51
4	0.27	33.27	51.12	---	54.81	61.12	-6.31
5	0.274	34.36	51.00	---	54.99	61.00	-6.01
6	0.278	38.14	50.88	---	55.24	60.88	-5.64
7	0.282	36.52	50.76	---	55.32	60.76	-5.44
8	0.286	28.98	50.64	---	55.16	60.64	-5.48
9	24.022	41.72	50.00	-8.28	41.95	60.00	---

QP: 3.2 dB - Pass

Figure 63 CE at 115 V_{ac}, 20 V full load with trace L1

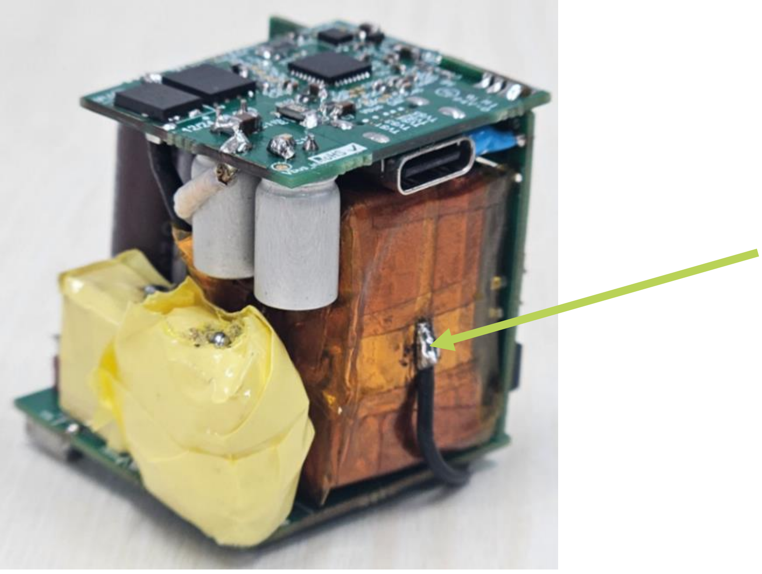
Conducted emission L2 at 115 V_{ac}, 60 Hz:

	Frequency [MHz]	Avg [dBµV]	Limit 55032bav [dBµV]	Delta [dB]	QPeak [dBµV]	Limit 55032bqp [dBµV]	Delta [dB]
1	0.258	37.35	51.50	---	53.45	61.50	-8.05
2	0.262	34.97	51.37	---	54.26	61.37	-7.11
3	0.266	34.21	51.24	---	54.63	61.24	-6.61
4	0.27	34.51	51.12	---	54.76	61.12	-6.36
5	0.274	35.88	51.00	---	54.91	61.00	-6.09
6	0.278	38.70	50.88	---	55.17	60.88	-5.71
7	0.282	36.41	50.76	---	55.15	60.76	-5.61
8	0.286	27.53	50.64	---	53.16	60.64	-7.48

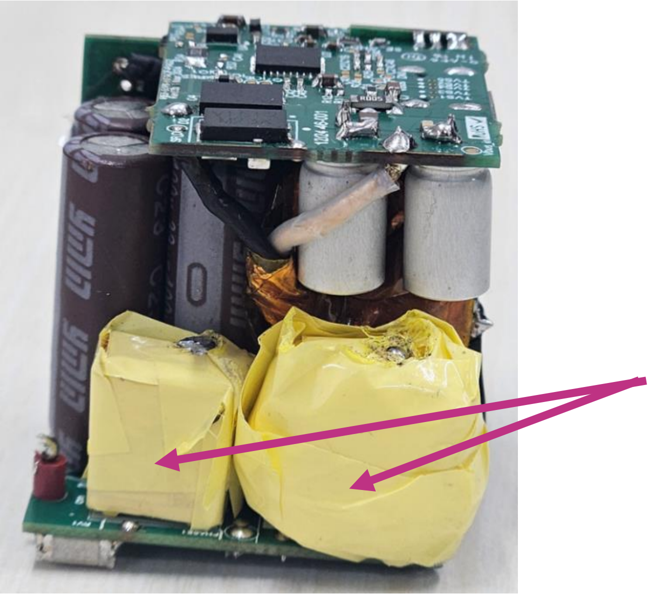
QP: 5.61 dB - Pass

Figure 64 CE at 115 V_{ac}, 20 V full load with trace L2

Figure 65 shows the shielding required to pass the conducted EMI.



Transformer is wrapped with a copper tape and terminated to primary ground.



X-Cap and CMC are both wrapped with copper tape and are not grounded.

Figure 65 Shielding required to pass conducted EMI

3.16.2 Surge

IEC61000-4-5, ±2kV DM, Criteria A (auto-recovery)

3.16.3 ESD

IEC61000-4-2 level 4; ±8kV contact, ±16kV air, Criteria A

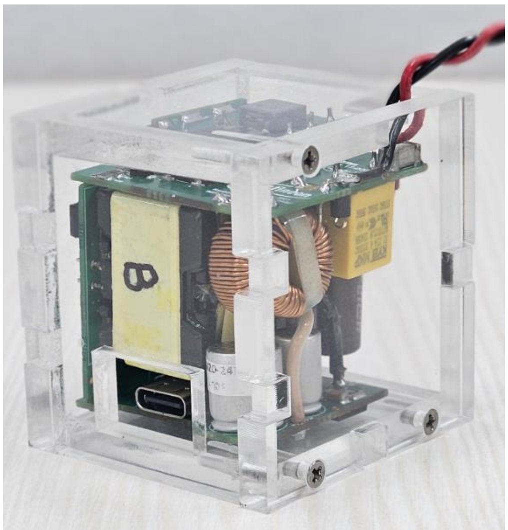


Figure 66 Device setup for ESD test

4 USB PD source test results (using Quadramax)

4.1 Test setup

Figure 67 Quadramax tester

- QuadDraw Version: 0.9.8594
- QM#108 HWRev:1.4.4 FWST:0.0.1376 FWCCG1:0.10

4.2 Test results

Test input voltage conditions: 115 V_{ac}, 60 Hz and 230 V_{ac}, 50 Hz

Table 17 Test results

Test	Description	Result
TD SPT. 1	Load test	Pass
TD SPT. 2	Capabilities test	Pass
TD SPT. 3	Hard reset test	Pass

5 Appendix

5.1 Schematics

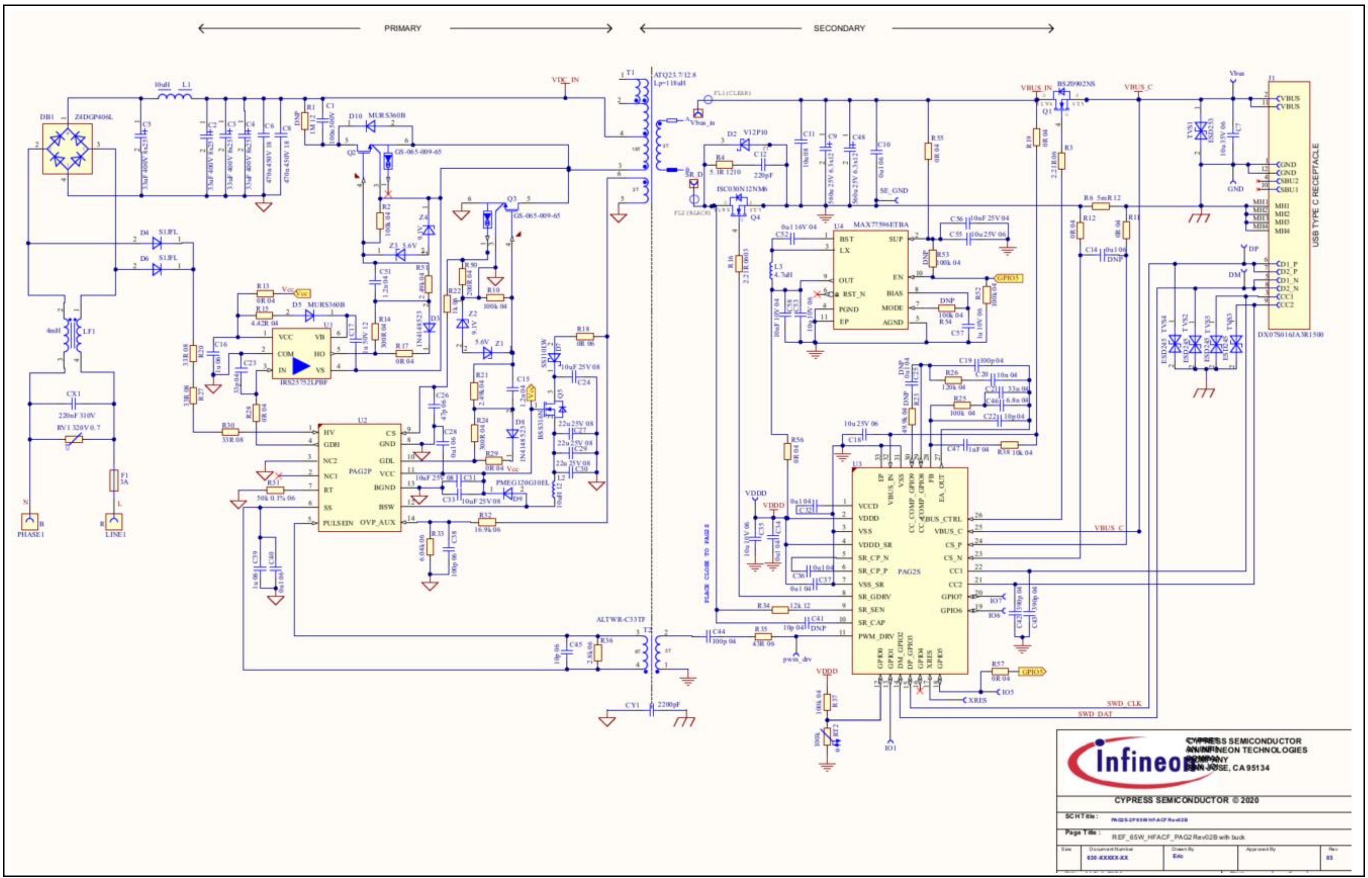


Figure 68 Schematic diagram of 65 W PAG2P_PAG2S_HF ACF_Rev3_GaN system _SCH

5.2 Bill of materials (BOM)

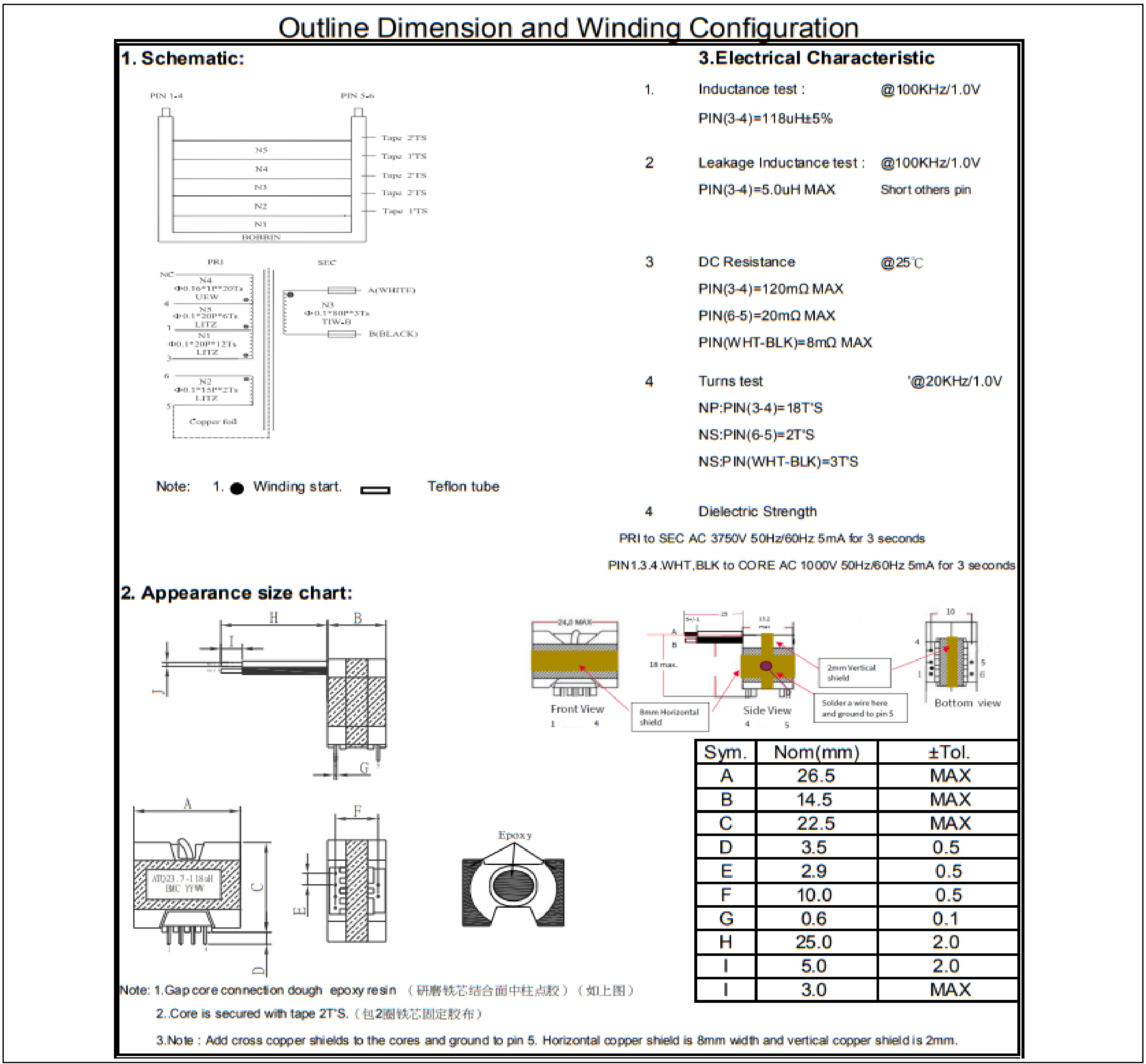
Table 18 Bill of materials (BOM)

Designator	Qty	Comment	Value	Manufacturer order number	Manufacturer
C1	1	100n 500V	100n 500V	C1210C104KCRACTU	Kemet
C2, C3, C4, C5	4	33uF 400V 8x25	33uF 400V 8x25	KCX 33u1F 400V 8X25	Rubycon
C6, C8	2	470n 450V 18	470n 450V 18	CGA8N4X7T2W474M230KA	TDK Corporation
C7	1	10u 35V 06	10u 35V 06	GRM188R6YA106MA73D	Murata
C9, C48	2	560u 25V 6.3x12	560u 25V 6.3x12	NPX 470uF 25V 6.3 x 12	Sh-ymin
C10	1	0u1 06	0u1 06	CGA3E2X8R1E104K080AA	TDK Corporation
C11	1	10u 08	10u 08	GRM21BR61H106KE43K	Murata
C12	1	220pF	220pF	1206B221K201CT	Walsin Technology
C14	1	330nF 06	330nF 06	GRM188R71A334KA61	Murata
C15, C51	2	1.2n 04	1.2n 04	GRM155R71H122JA01	Murata
C16	1	1u 06	1u 06	CGA3E3X5R1H105K080AB	TDK Corporation
C17	1	680n 50V 12	680n 50V 12	GCM31MR71H684JA55	Murata
C18, C55	2	10u 25V 06	10u 25V 06	885012106031	Würth Elektronik
C19	1	33pF 04	33pF 04	GRM1555C1E330GA01	Murata
C20	1	47nF 04	47nF 04	GRM155R61C473JA01	Murata
C21, C25, C41, C47	4	DNP 04	DNP 04	DNP	Murata
C22	1	4.7pF 04	4.7pF 04	GRM1555C1E4R7WA01J	Murata
C23	1	33p 04	33p 04	CGA2B2NP01H330J050BA	TDK Corporation
C24	1	22uF 35V 08	22uF 35V 08	C2012X5R1V226M125AC	TDK Corporation
C26	1	47p 06	47p 06	GRM1885C1H470GA01	Murata
C27, C29, C30	3	22u 25V 08	22u 25V 08	GRM21BR61E226ME44	Murata
C28	1	0u1 06	0u1 06	06035C104JAT2A	AVX
C31, C33	2	10uF 25V 08	10uF 25V 08	GRM21BR61E106KA73	Murata
C32, C34	2	0u1 04	0u1 04	GRM152R61A104KE19	Murata
C35, C53	2	10u 10V 06	10u 10V 06	ZRB18AD71A106KE01L	Murata
C36, C37	2	0u1 04	0u1 04	GCM155R71C104KA55	Murata
C38	1	100p 06	100p 06	06033A101JAT2A	AVX
C39	1	1u 06	1u 06	GRM185R61A105KE26	Murata
C40	1	0u1 06	0u1 06	C0603C104J8RAC	Kemet
C42, C43	2	390p 04	390p 04	GRM1555C1E391JA01	Murata
C44	1	100p 04	100p 04	GRM1555C1E101JA01	Murata
C45	1	10p 06	10p 06	C0603C100K5GACAUTO	Kemet
C46	1	6.8n 04	6.8n 04	GRM155R71E682JA01	Murata
C52	1	0u1 16V 04	0u1 16V 04	GCM155R71C104KA55	Murata
C56	1	10nF 25V 04	10nF 25V 04	GRM155R71E103JA01	Murata
C57	1	1u 10V 06	1u 10V 06	GRM185R61A105KE26	Murata
C58	1	10nF 10V 04	10nF 10V 04	GRM155R61A103KA01	Murata
CX1	1	220nF 310V	220nF 310V	PX224K2C0702T	KYET
CY1	1	1000pF	1nF 250V	DE1E3RA102MN4AN01F	Murata
D2	1	V15P12	V15P12	V15P12-M3/H	Vishay

Designator	Qty	Comment	Value	Manufacturer order number	Manufacturer
D3, D8	2	1N4148 523	1N4148 523	1N4148WT-7	Diodes Incorporated
D4, D6	2	S1JFL	S1JFL	S1JFL	ON Semiconductor
D5, D10	2	MURS360B	MURS360B	MURS360BT3G	ON Semiconductor
D7	1	SS110LW	SS110LW	SS110LW	Taiwan Semiconductor
D9	1	PMEG120G10EL	PMEG120G10EL	PMEG120G10ELRX	Nexperia
D11	1	DNP SOD923	DNP SOD923	DNP	Onsemi
DB1	1	Z4DGP406L	Z4DGP406L	Z4DGP406L-HF	Comchiptech
DM, DP, GND, IO1, IO5, IO6, IO7, pwm_drv, SE_GND, Vbus, VDDD, XRES	12	test pad	test pad	-	-
F1	1	3A	3A	TR1-2410TD3-R	Bussmann
J1	1	DX07S016JA3R1500	DX07S016JA3R1500	DX07S016JA3R1500	JAE
L1	1	10uH	10uH	74437346100	Würth Elektronik
L2	1	10uH 12	10uH 12	LSQCA322525T100KR	Taiyo Yuden
L3	1	4.7uH	4.7uH	LSBHB1608KKT4R7M	Taiyo Yuden
LF1	1	6mH	6mH	T38 core, 2 x 30T Φ0.544mm	EPCOS
LINE1	1	R	R	5000	Keystone Electronics Corp.
PHASE1	1	B	B	5001	Keystone Electronics Corp.
Q1	1	BSZ0902NS	BSZ0902NS	BSZ0902NS	Infineon Technologies
Q2, Q3	2	GS-065-009-65	GS-065-009-65	GS-065-009-65	Infineon Technologies
Q4	1	ISC030N12NM6	ISC030N12NM6	ISC030N12NM6	Infineon Technologies
Q5	1	BSS316N	BSS316N	BSS316N H6327	Infineon Technologies
R1	1	DNP 12	DNP 12	DNP	Vishay
R2, R10, R52	3	100k 04	100k 04	RC0402FR-07100KL	Yageo
R3	1	2.21R 06	2.21R 06	CRCW06032R21FK	Vishay
R4	1	5.1R 1210	5.1R 1210	ERJ-14YJ5R1U	Panasonic
R6	1	5mR 12	5mR 12	CSRF1206FT5L00	Stackpole Electronics
R11, R12	2	499R 04	499R 04	CRCW0402499RFK	Vishay
R13, R28, R55, R56, R57	5	0R 04	0R 04	CRCW04020000Z0	Vishay
R14, R24	2	300R 04	300R 04	CRCW0402300RFK	Vishay
R15	1	4.42R 04	4.42R 04	CRCW04024R42FK	Vishay
R16, R18	2	0R 06	0R 06	CRCW06030000Z0EA	Vishay
R17, R29	2	0R 04	0R 04	RC0402JR-070RL	Yageo
R19	1	0R 04	0R 04	RC0402FR-070RL	Yageo

Designator	Qty	Comment	Value	Manufacturer order number	Manufacturer
R20, R27, R30	3	33R 08	33R 08	CRCW080533R0FKEAHP	Vishay
R21, R51	2	2.49k 04	2.49k 04	CRCW04022K49FK	Vishay
R22	1	1k 06	1k 06	AC0603JR-071KL	Yageo
R23	1	DNP 04	DNP 04	DNP	TE Connectivity
R25	1	499k 04	499k 04	CRCW0402499KFK	Vishay
R26	1	69.8k 04	69.8k 04	CRCW040269K8FK	Vishay
R31	1	50k 0.1% 06	50k 0.1% 06	RT0603BRD0750KL	Yageo
R32	1	16.9k 06	16.9k 06	CRCW060316K9FK	Vishay
R33	1	6.04k 06	6.04k 06	CRCW06036K04FK	Vishay
R34	1	12k 12	12k 12	CRCW120612K0FK	Vishay
R35	1	43R 06	43R 06	CRCW060343R0FK	Vishay
R36	1	2.8k 06	2.8k 06	MCR03EZPFX2801	ROHM Semiconductors
R37	1	100k 04	100k 04	CRCW0402100KFK	Vishay
R38	1	DNP 04	DNP 04	DNP	Vishay
R50	1	200R 04	200R 04	CRCW0402200RFK	Vishay
R53, R54, R58	3	DNP 04	DNP 04	DNP	Yageo
RT2	1	100k	100k	NCU18WF104J60RB	Murata
RV1	1	320V 0.7	320V 0.7	B72207S2321K101	Epcos
SR_D, Vbus_in	2	tet pad	tet pad	-	-
T1	1	ATQ23.7/12.8	ATQ23.7/12.8	ATQ23.7/12.8	Better Magnetic
T2	1	ALTWR-C33TF	ALTWR-C33TF	ALTWR-C33TF	Sunlord
TVS1	1	ESD253	ESD253	ESD253-B1-W0201	Infineon Technologies
TVS2, TVS3, TVS4, TVS5	4	ESD245	ESD245	ESD245-B1-W0201	Infineon Technologies
U1	1	IRS25752LPBF	IRS25752LPBF	IRS25752LPBF	Infineon Technologies
U2	1	PAG2P	PAG2P	CYPAP212A1-14SXI	Infineon Technologies
U3	1	PAG2S	PAG2S	CYPAS212A1-32LQXQ	Infineon Technologies
U4	1	MAX77596ETBA	MAX77596ETBA	MAX77596ETBA+	Analog Devices
Z1, Z3	2	5.6V	5.6V	DZ9F5V6S92	Diodes Incorporated
Z2, Z4	2	9.1V	9.1V	DZ9F9V1S92-7	Diodes Incorporated

5.3 Transformer specification (T1)



Outline Dimension and Winding Configuration

1. Schematic:

Note: 1. ● Winding start. ▭ Teflon tube

3.Electrical Characteristic

1. Inductance test : @100KHz/1.0V
PIN(3-4)=118uH±5%

2 Leakage Inductance test : @100KHz/1.0V
PIN(3-4)=5.0uH MAX Short others pin

3 DC Resistance @25℃
PIN(3-4)=120mΩ MAX
PIN(6-5)=20mΩ MAX
PIN(WHT-BLK)=8mΩ MAX

4 Turns test '@20KHz/1.0V
NP:PIN(3-4)=18T'S
NS:PIN(6-5)=2T'S
NS:PIN(WHT-BLK)=3T'S

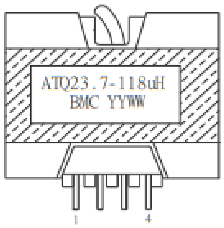
4 Dielectric Strength
PRI to SEC AC 3750V 50Hz/60Hz 5mA for 3 seconds
PIN1.3.4.WHT,BLK to CORE AC 1000V 50Hz/60Hz 5mA for 3 seconds

2. Appearance size chart:

Sym.	Nom(mm)	±Tol.
A	26.5	MAX
B	14.5	MAX
C	22.5	MAX
D	3.5	0.5
E	2.9	0.5
F	10.0	0.5
G	0.6	0.1
H	25.0	2.0
I	5.0	2.0
I	3.0	MAX

Note: 1.Gap core connection dough epoxy resin （研磨铁芯结合面中柱点胶）（如上图）
2..Core is secured with tape 2T'S.（包2圈铁芯固定胶布）
3.Note : Add cross copper shields to the cores and ground to pin 5. Horizontal copper shield is 8mm width and vertical copper shield is 2mm.

Figure 69 Transformer specification (T1)

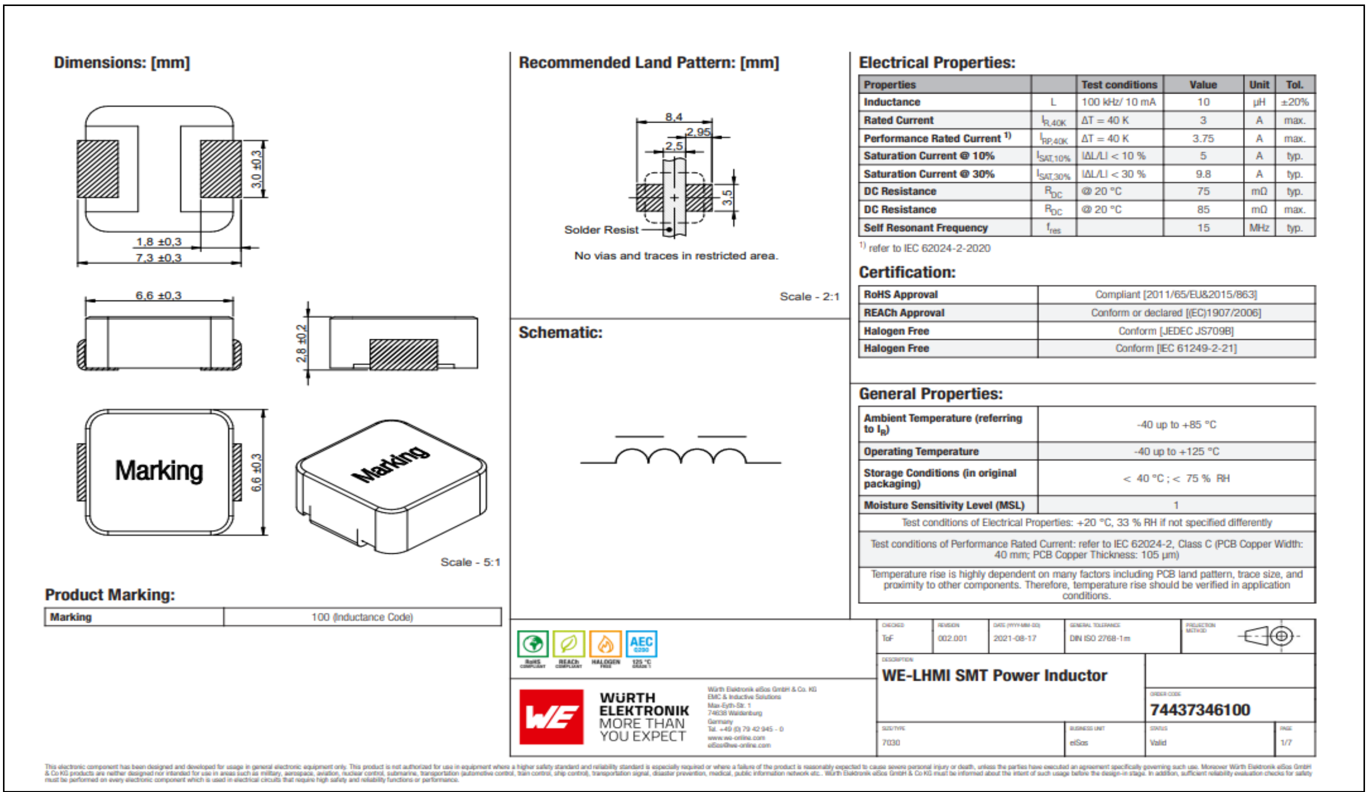


All materials listed are in compliance with RoHS requirements

No.	Name	Description	Rating	Approval	Maker
1	Core	Ferrite core ATQ23.7/12.8/17.8 NH97 or equivalent			LIANFENG
2	Bobbin	Phenolic PM-9630 UL 94V-0	150℃	E41429	SUMITOMO
3	Wire	Polyurethane enamelled copper Wire UEW MW75-C Ø0.1*20P,Ø0.1*15P Ø0.16	130℃ 130℃	E339217 E201757	WEIHAN PACIFIC
		Triple insulated wire TIW-B Ø0.1X80P or equivalent	130℃	E357240	KAIZHONGHEDONG
4	Tape	Polyester tape #1350F-1 or #CT280	130℃ 130℃	E17385 E165111	3M YA HUA
5	Tube	CB-HFT ND-LL	125℃ 200℃	E180908 E350651	CHANGYUAN NANDIAN
6	Copper foil	0.05(T)*8mm 0.05(T)*3mm			HAIYU DETAI
7	Epoxy	2050 2041			CHENGGE CHENGGE
8	Varnish	BC-359 WP-2952F-2G(Y)	180℃ 130℃	E317427 E72979	DOLPH HITACHI

Figure 70 ATQ23.7-118 µH (NH97)

5.4 Inductor specification (L1)



Product Marking:

Marking	100 (Inductance Code)

Electrical Properties:

Properties		Test conditions	Value	Unit	Tol.
Inductance	L	100 kHz/ 10 mA	10	µH	±20%
Rated Current	$I_{R,40K}$	ΔT = 40 K	3	A	max.
Performance Rated Current [1]	$I_{RP,40K}$	ΔT = 40 K	3.75	A	max.
Saturation Current @ 10%	$I_{SAT,10\%}$	|ΔL/L| < 10 %	5	A	typ.
Saturation Current @ 30%	$I_{SAT,30\%}$	|ΔL/L| < 30 %	9.8	A	typ.
DC Resistance	R_{DC}	@ 20 °C	75	mΩ	typ.
DC Resistance	R_{DC}	@ 20 °C	85	mΩ	max.
Self Resonant Frequency	f_{res}		15	MHz	typ.

[1] refer to IEC 62024-2-2020

Certification:

RoHS Approval	Compliant [2011/65/EU&2015/863]
REACh Approval	Conform or declared [(EC)1907/2006]
Halogen Free	Conform [JEDEC JS709B]
Halogen Free	Conform [IEC 61249-2-21]

General Properties:

Ambient Temperature (referring to I_R)	-40 up to +85 °C
Operating Temperature	-40 up to +125 °C
Storage Conditions (in original packaging)	< 40 °C ; < 75 % RH
Moisture Sensitivity Level (MSL)	1

Test conditions of Electrical Properties: +20 °C, 33 % RH if not specified differently

Test conditions of Performance Rated Current: refer to IEC 62024-2, Class C (PCB Copper Width: 40 mm; PCB Copper Thickness: 105 µm)

Temperature rise is highly dependent on many factors including PCB land pattern, trace size, and proximity to other components. Therefore, temperature rise should be verified in application conditions.

Checked	Revision	Date (YYYY-MM-DD)	General Tolerance
ToF	002.001	2021-08-17	DIN ISO 2768-1m

Description	Order code	Size/Type	Business unit	Status	Page
WE-LHMI SMT Power Inductor	74437346100	7030	eiSos	Valid	1/7

Figure 71 Fixed IND 10 µH 3 A 85 MΩ SMD Würth Elektronik

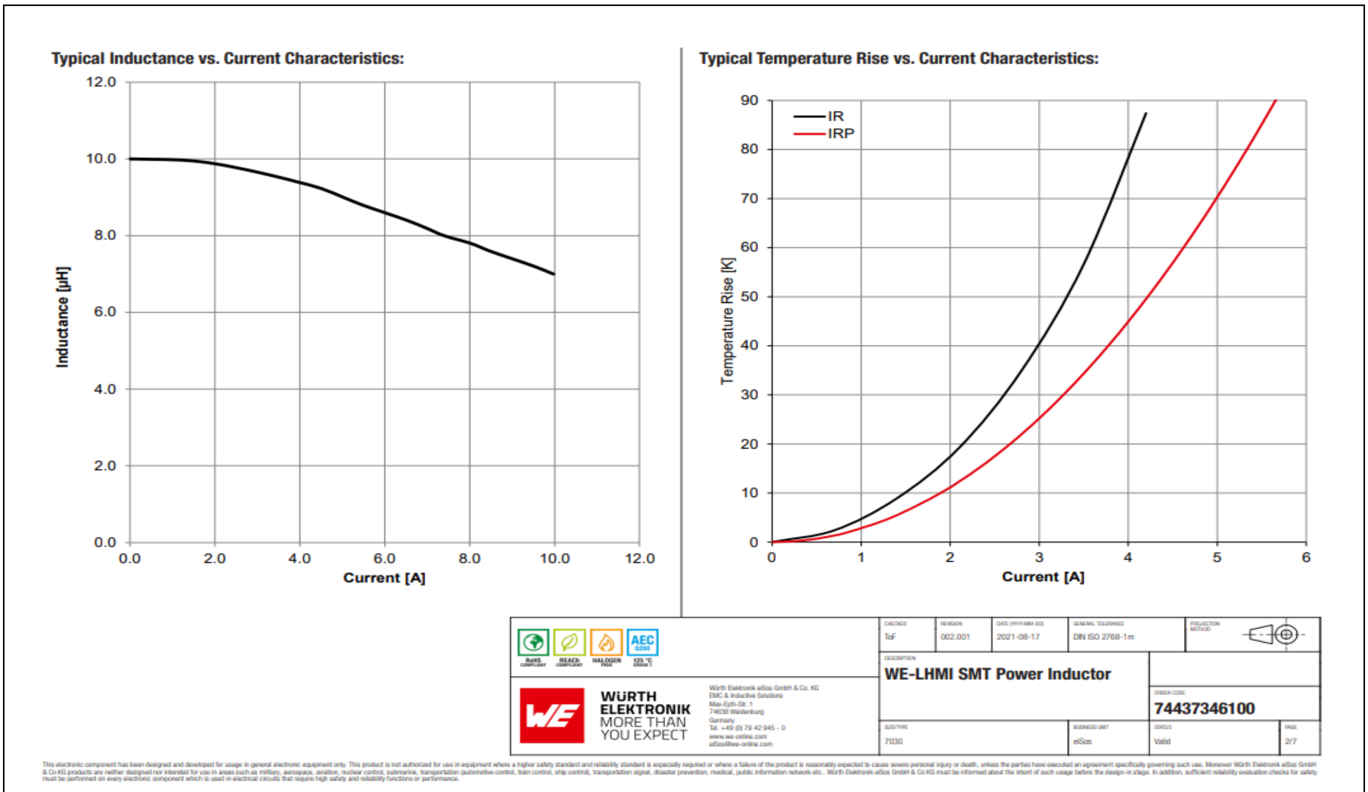


Figure 72 L1 Fixed IND 10 µH 3 A 85 MΩ SMD Würth Elektronik inductor specifications

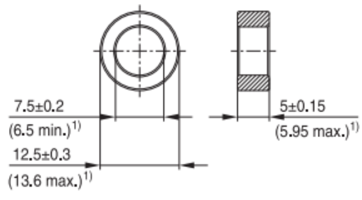
5.5 Common mode choke specification (LF2)

TDK

R 12.5 × 7.50 × 5.00 **B64290L0044**

- Epoxy coating

R 12.5 × 7.50 × 5.00 (mm)
R 0.492 × 0.295 × 0.197 (inch)



Dimensions

d_a (mm)	d_i (mm)	Height (mm)	d_a (inch)	d_i (inch)	Height (inch)	
12.5 ±0.3	7.5 ±0.2	5.00 ±0.15	0.492 ±0.012	0.295 ±0.008	0.197 ±0.005	uncoated 1)
13.6 max.	6.5 min.	5.95 max.	0.535 max.	0.256 min.	0.234 max.	coated

Characteristics and ordering codes

Material	A_L value nH	μ_i (approx.)	Ordering code	Magnetic characteristics $\Sigma l/A$ mm^{-1}	l_e mm	A_e mm^2	V_e mm^3	Approx. weight g
N49	660 ±25%	1300	B64290L0044X049	2.46	30.09	12.23	368	1.8
N87	1120 ±25%	2200	B64290L0044X087					
N30	2200 ±25%	4300	B64290L0044X830					
T65	2400 ±30%	4700	B64290L0044X065					
T35	3060 ±25%	6000	B64290L0044X035					
T37	3320 ±25%	6500	B64290L0044X037					
T38	5110 ±30%	10000	B64290L0044X038					

Figure 73 Common mode choke specification

Note: *Turns: 30, L = 6.6 mH, R_{dc} = 66 mΩ*

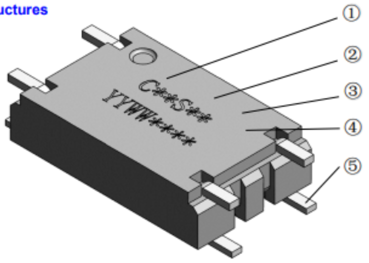
5.6 Pulse transformer specification (T2)

Sunlord www.sunlordinc.com

Proposal Of Pulse Transformer For Automobiles(ALTWR-C33TF)	Issued By	Checked By	Prepared By
	Xiangping Qu	**Xiangping Qu**	**Liangming Bin**
	2023/1/16	2023/1/16	2023/1/16

Note: This is a preliminary proposal for communication.The product reliability is being test,and the final product P/N, Structure, Shape and Dimensions, Electrical Characteristics may be changed. You are requested to confirm and approve our spec.

1.Structures

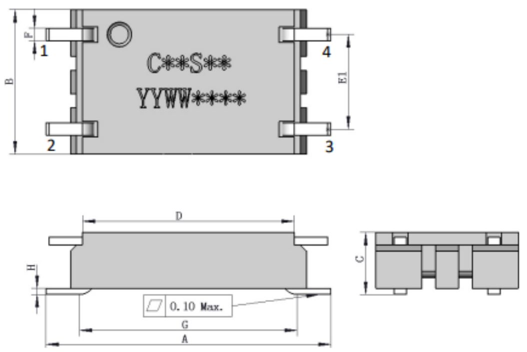


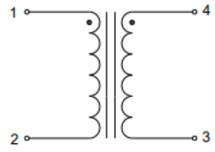
No.	Part Name	Material
①	Case	Plastics
②	Glue	Silicon Glue
③	Core	Ferrite soft magnetism
④	Wire	Polyurethane system enameled copper wire
⑤	Terminal	Cu+Ni+Sn plating

2.Shape and dimensions (mm)

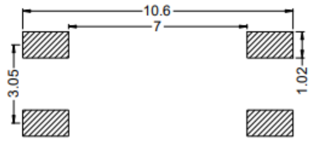
Unit:mm

Items	A	B	C	D Ref.	E1	F	G Ref.	H Ref.
Sunlord Design	9.3±0.30	4.90 Max.	2.00+0.20/-0.10	6.9±0.50	3.05±0.13	0.50±0.13	7.10	0.25





Topological diagram

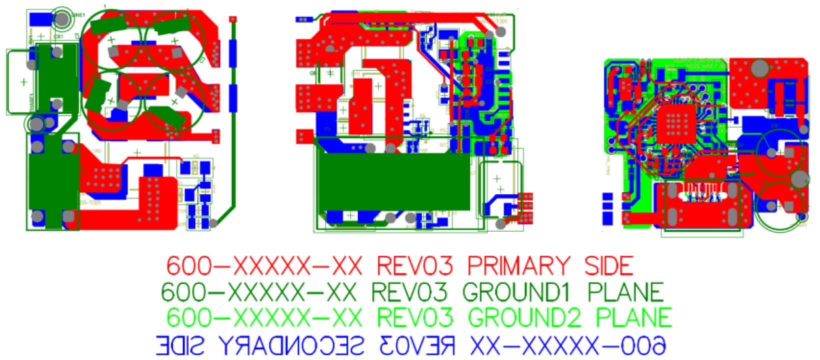


Recommend pad patterm (mm)

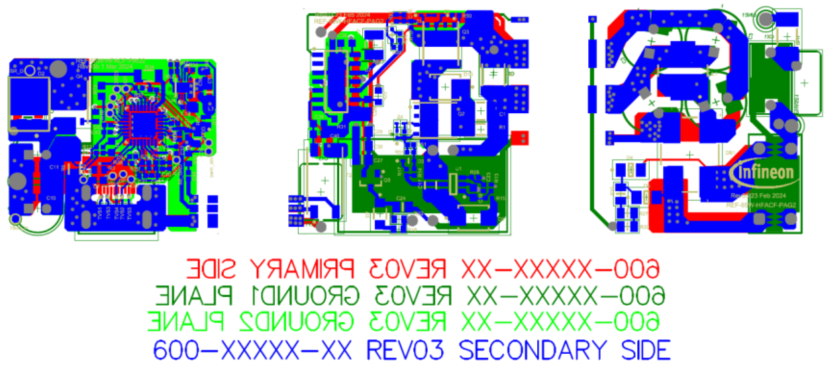
Shenzhen Sunlord Electronics Co.,Ltd. Page1/

Figure 74 Pulse transformer specification

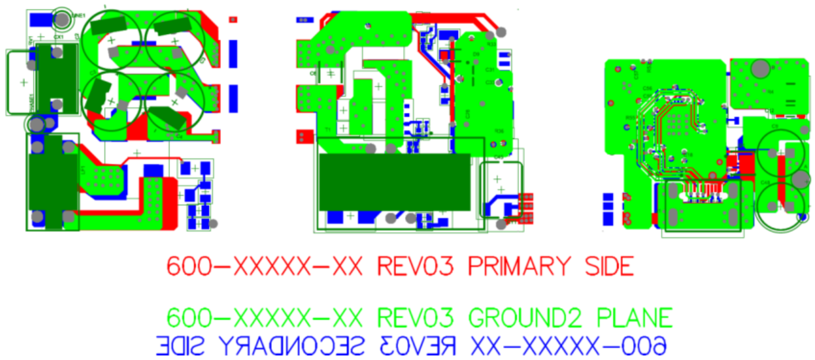
5.7 PCB layout



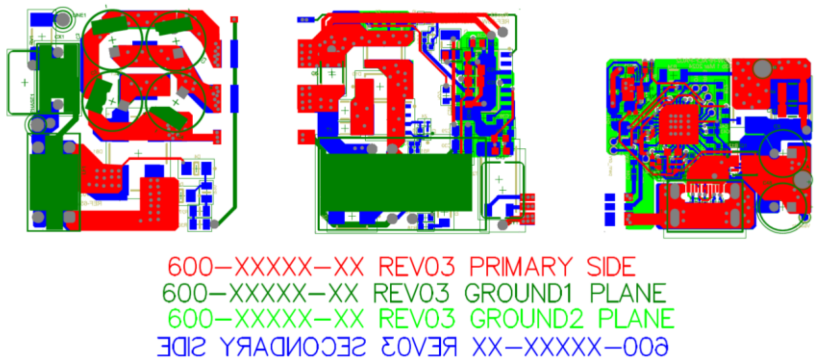
Top side copper – layer 1



Bottom solder copper – layer 4



Inner layer – layer 2



Inner layer – layer 3

Figure 75 **PCB layout**

5.8 EZ-PD™ Configuration Utility

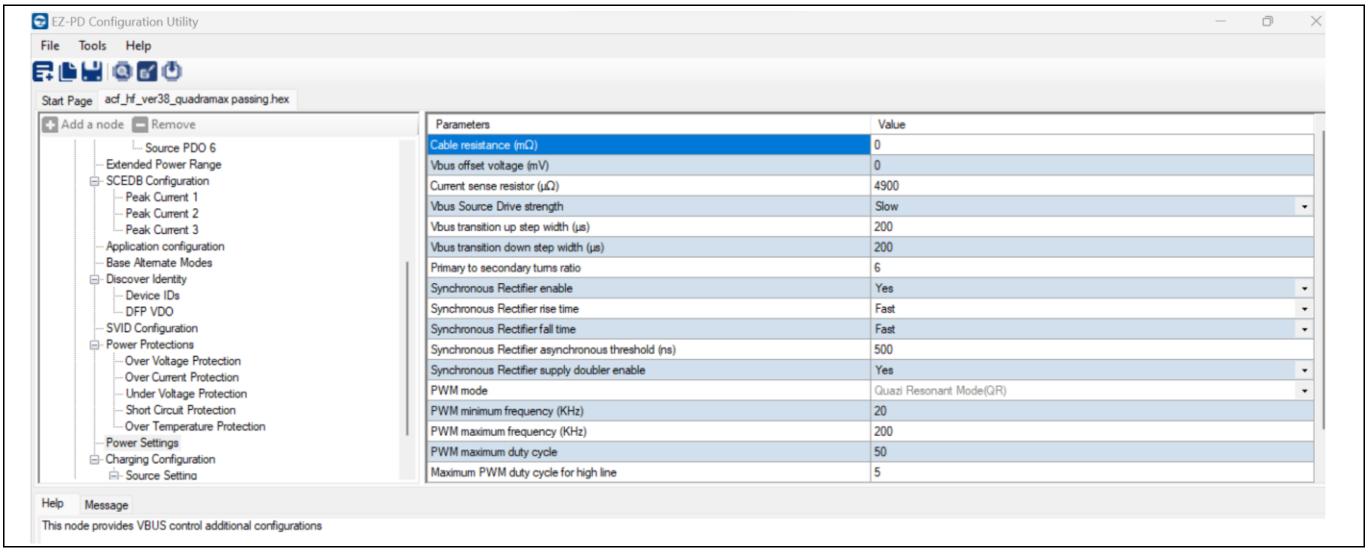


Figure 76 EZ-PD™ Configuration Utility

Infineon's EZ-PD™ PAG2S controller is a highly configurable and programmable solution. The chip can be configured using parameters stored in the internal flash memory. These parameters are to be chosen and programmed by Infineon customers according to their use cases and requirements.

The graphical user interface (GUI) of EZ-PD™ Configuration Utility allows to instinctively select and configure the parameters for applications.

Table 19 lists the default configured values with respect to power settings and power protections.

Table 19 Default configuration values

Parameters	Values
Power settings	
Cable resistance (mΩ)	0
V_{bus} offset voltage (mV)	0
Current sense resistor (µΩ)	5100
V_{bus} source drive strength	Slow
V_{bus} transition up step width (µs)	200
V_{bus} transition down step width (µs)	200
Primary to secondary turns ratio	6
Synchronous rectifier enable	Yes
Synchronous rectifier rise time	Fast
Synchronous rectifier fall time	Fast
Synchronous rectifier async threshold (ns)	500
Synchronous rectifier doubler enable	Yes
PWM mode	Quasi resonant mode (QR)
PWM minimum frequency (kHz)	22
PWM maximum frequency (kHz)	200

Parameters	**Values**
PWM maximum duty cycle at minimum frequency (%)	21
Maximum PWM duty cycle for high line	5
V_{bus} transition up step width for transitions below 5 V (µs)	1
V_{bus} transition down step width for transitions below 5 V (µs)	1
Power protections	
Overvoltage protection (OVP)	
Enable	Yes
OVP threshold (%)	20
Debounce period (µs)	10
Retry count	2
Overcurrent protection (OCP)	
Enable	Yes
OCP threshold (%)	20
Debounce period (ms)	10
Retry count	2
Undervoltage protection (UVP)	
Enable	Yes
UVP threshold (%)	70
Debounce period (µs)	10
Retry count	2
Short-circuit protection (SCP)	
Enable	Yes
SCP threshold (%)	10
Debounce period (µs)	2
Retry count	2
Overtemperature protection	
Enable	Yes
Thermistor type 1	NTC
Cut-off value 1	255
Restart value 1	909
Debounce period (ms)	10
Enable thermistor 2	Yes
Thermistor type 2	NTC
Cut-off value 2	255
Restart value 2	909

References

[1] USB Implementers Forum, Inc.: Document library

[2] USB Implementers Forum, Inc.: USB Type-C and connector specification (release 2.3)

[3] Infineon Technologies AG: USB EZ-PD™ Configuration Utility

[4] Infineon Technologies AG: EZ-PD™ PAG2P primary-side startup controller *(Document number: 002-34772 Rev. *F), 2022-06-13*

[5] Infineon Technologies AG: EZ-PD™ PAG2S-AC integrated USB PD and secondary-side ACF controller *(Document number: 002-37370 Rev. *A), 2023-07-27*

Acronyms

Table 20 Acronyms used in this document

Abbreviation	Definition
ACF	active clamp flyback
HF	high frequency
CC-CV	constant current - constant voltage
CE	conducted emission
CH'x'	oscilloscope channel numbers
CR Mode	constant resistance mode in electronic Load
DCM	discontinuous current mode
DP/DM	USB data positive/data negative lines
DUT/EUT	device under test/equipment under test
FET	MOSFET (metal oxide semiconductor field effect transistor)
GUI	graphical user interface
I_o/I_{OUT}	output current of the DUT
NGDO	NFET gate driver output
OCP	overcurrent protection
OVP	overvoltage protection
P-P	peak-to-peak
PAT	power adaptor tester
PDO	power delivery output
PPS	programmable power supply
SCP	short-circuit protection
USB PD	Universal Serial Bus Power Delivery
V_{BUS_C}/V_{OUT}	output voltage of the DUT
V_{AC}/V_{IN_AC}	input DC voltage to the DUT

Revision history

Document revision	Date	Description of changes
**	2024-05-03	Initial release

Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

Edition 2024-05-03

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about this document?

Email:

erratum@infineon.com

Document reference

002-39822 Rev. **