2EDL6014AC-G2D Evaluation Board user guide

Optimized for OptiMOS™ power MOSFETs

About this document

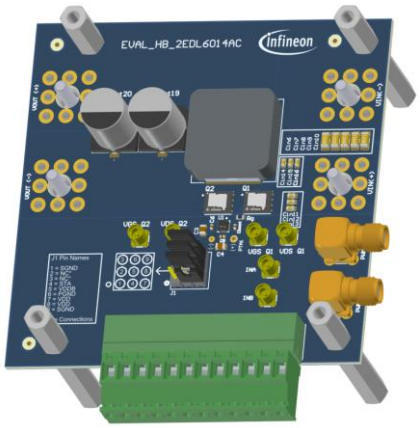

Figure 1 Overview of EVAL_HB_2EDL6014AC Evaluation Board

Scope and purpose

This user guide provides information about the EVAL_HB_2EDL6014AC Evaluation Board for Infineon's EiceDRIVER™ 2EDL6014AC-G2D gate driver, including the board's functionality, interfaces, jumper settings, assembled components, configurations and debugging options. In addition, it includes the default bill of materials (BOM), schematics, and layout of the board.

Intended audience

This document is intended for anyone using the EVAL_HB_2EDL6014AC Evaluation Board.

About this product group

Target applications

- Intermediate bus converter (IBC)/server and datacenter applications for AI power supplies

Product family

Infineon's EiceDRIVER™ 2EDL6014AC-G2D optimized for Si MOSFETs.

This evaluation board focuses on 2EDL6014AC-G2D that drives two OptiMOS™ devices in half-bridge configuration.

Evaluation board

This board is to be used during the design-in process for evaluating the Infineon's EiceDRIVER™ 2EDL6014AC-G2D product features.

Note: PCB and other circuits are NOT optimized for final customer design.

Safety precautions

Note: Please note the following warnings regarding the hazards associated with development systems.

Safety precautions

	**Caution:** *The heat sink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.*
	**Caution:** *Only personnel familiar with the drive, power electronics and associated machinery should plan, install, commission and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.*
	**Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	**Caution:** *A drive that is incorrectly applied or installed can lead to component damage or reduction in product lifetime. Wiring or application errors such as undersizing the motor, supplying an incorrect or inadequate AC supply, or excessive ambient temperatures may result in system malfunction.*
	**Caution:** *The evaluation or reference board is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials that are unnecessary for system installation may result in overheating or abnormal operating conditions.*

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1 The board at a glance

Figure 2 shows the general-purpose evaluation board for Infineon's EiceDRIVER™ 2EDL6014AC-G2D gate driver, together with the OptiMOS™ ISC016N08NM8SC and ISC031N08NM6SC 80 V MOSFETs in a SuperSO8 DSC package. This board includes an optimized layout for a hard-switching half-bridge configuration, as well as waveform measurement points and other useful features that enable easy lab bench characterization of the gate driver and power switches.

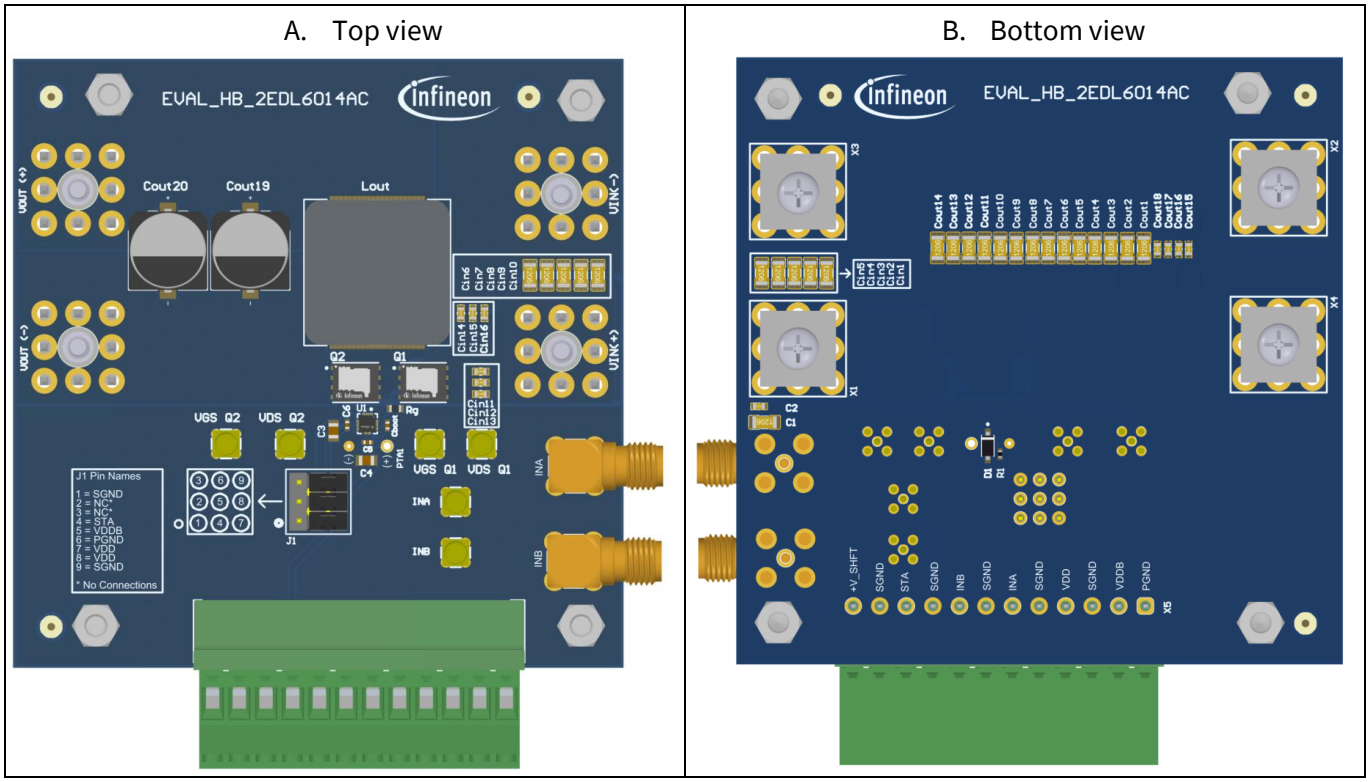

Figure 2 EVAL_HB_2EDL6014AC top (A) and bottom (B) view

1.1 Scope of supply

The EVAL_HB_2EDL6014AC board is an open-loop buck converter. It can be configured to operate as a typical half-bridge buck converter, wherein the buck converter's power ground (PGND) and signal ground (SGND) are at the same node. Circuitry such as the input supply of the gate driver (VDD), STA pin, and input PWMs are referenced to SGND. In this user guide, this configuration is referred to as the "non-voltage-level-shifted" configuration.

On the other hand, the board can also be configured as a dual floating-gate drive via external connections. In this configuration, it is still a buck converter, but the PGND and SGND are at two different nodes. The PGND is shifted by a positive voltage, +V_SHFT, with respect to SGND. In this user guide, this is referred to as the "voltage-level-shifted" configuration.

See Section 3 for a detailed description on how to configure the board.

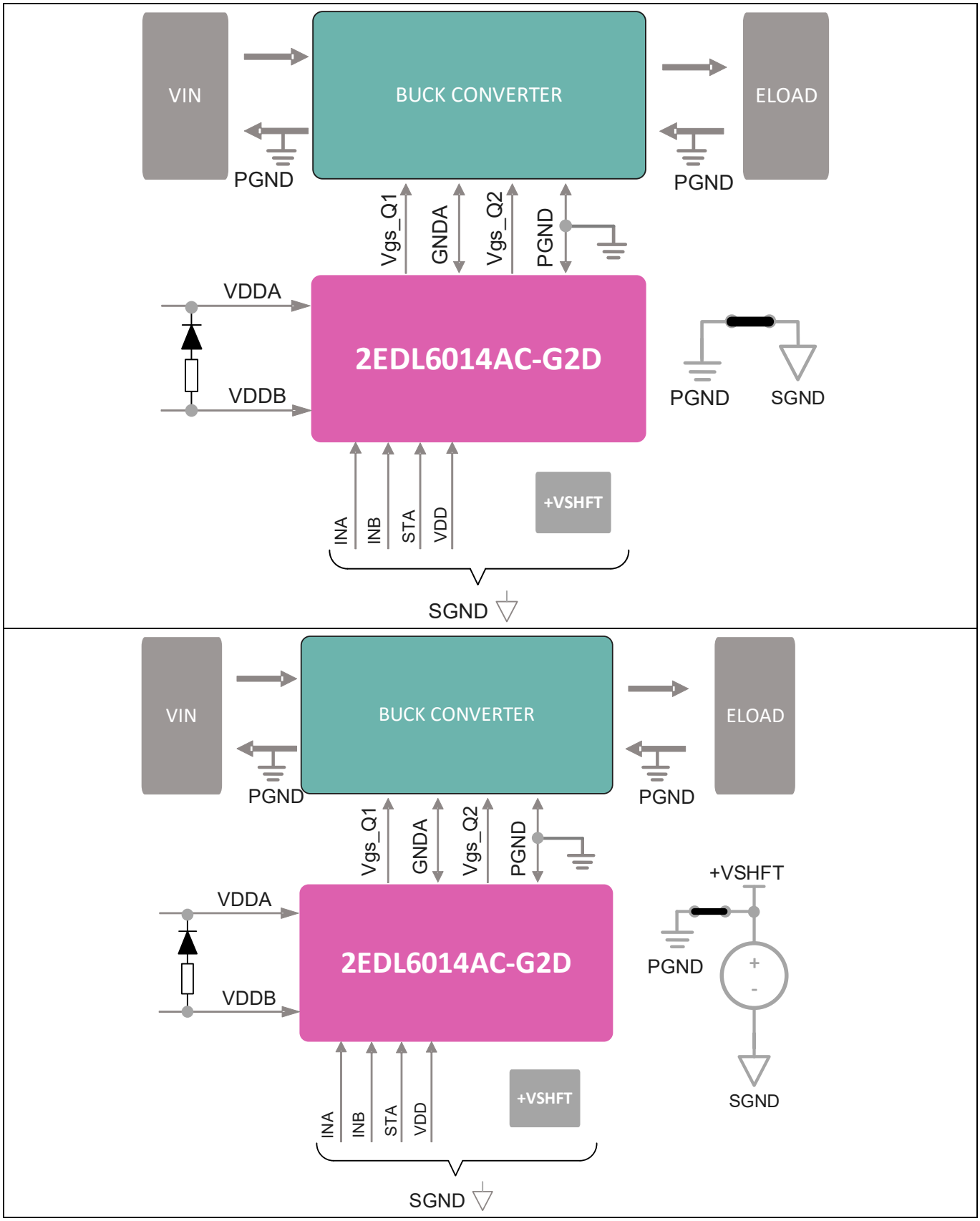

Figure 3 Configurations - Top: Non-voltage-level-shifted; bottom: Voltage-level-shifted

The STA pin of the 2EDL6014AC-G2D gate driver controls the turn-on driving current capability of the OUTA output. The evaluation board provides two methods to modify the state of the STA pin:

- **Jumper selection**: The state of the STA pin can be changed using jumper J1
- **External signal application**: Alternatively, an external signal can be applied to the STA pin via the X5 connector

The supply voltage for the VDDA-GNDA domain is bootstrapped from VDDB-PGND, supporting both non-voltage level-shifted and voltage-level-shifted configurations. This bootstrapping function is performed externally using diode D1.

Note that the following components are not included within the scope of this evaluation board and must be generated externally:

- Sources of the two PWM inputs
- Gate driver input power supply (VDD-SGND)
- Floating-channel supply (VDDB-PGND)

1.2 Block diagram

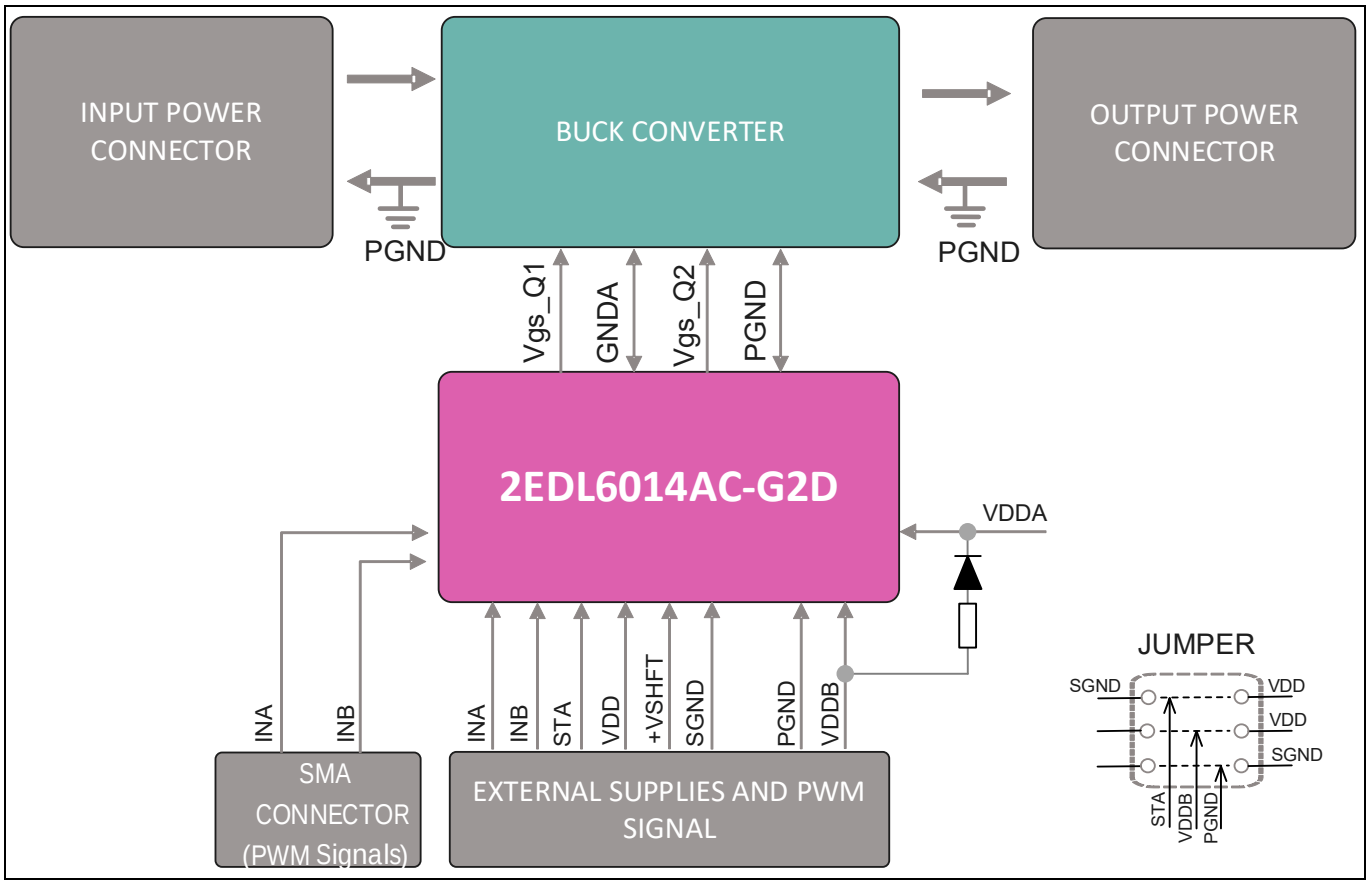

Figure 4 Block diagram of EVAL_HB_2EDL6014AC

1.3 Main features

- Configurable in either of the two configurations:
  - Non-voltage-level-shifted
  - Voltage-level-shifted via external connections
- Configurable STA conditions
- Wide 6 V to 12 V gate driving voltage operating range
- Test points ready for waveforms measurements for evaluation

1.4 Board parameters and technical data

The table below specifies the board parameters and its technical data.

Table 1 Board parameters

Parameter	Symbol	Conditions	Value	Unit
Input voltage	VIN	Reference to PGND	0 to 60	V
VDD voltage	VDD	Reference to SGND	3.3 to 5.5	V
VDDB voltage	VDDB	Reference to PGND	6 to 12	V
Switching frequency	fsw	–	200 to 300	kHz

Note: The evaluation board is optimized for operation with an input voltage (VIN) of 48 V, a duty cycle (D) of 25%, a switching frequency (fsw) of 200 kHz, and a load current of up to 15 A, without a fan and at room ambient temperature.

Attention:

- ***Testing beyond the optimized duty cycle, fsw, ambient temperature, and output power for your specific evaluation requires monitoring of thermal performance of the power switches and inductor***
- ***Output inductor (Lout) is IHLP7575GZ: L = 3.3 µH, DC saturation current = 28 A (Lo to drop approximately to 20%). This needs to be considered when testing beyond a 15 A load***
- ***When in voltage-level-shifted configuration, VOUT and +V_SHFT must be set accordingly so that they do not exceed the recommended voltage ratings of the driver IC***

2 System and functional description

2.1 Getting started

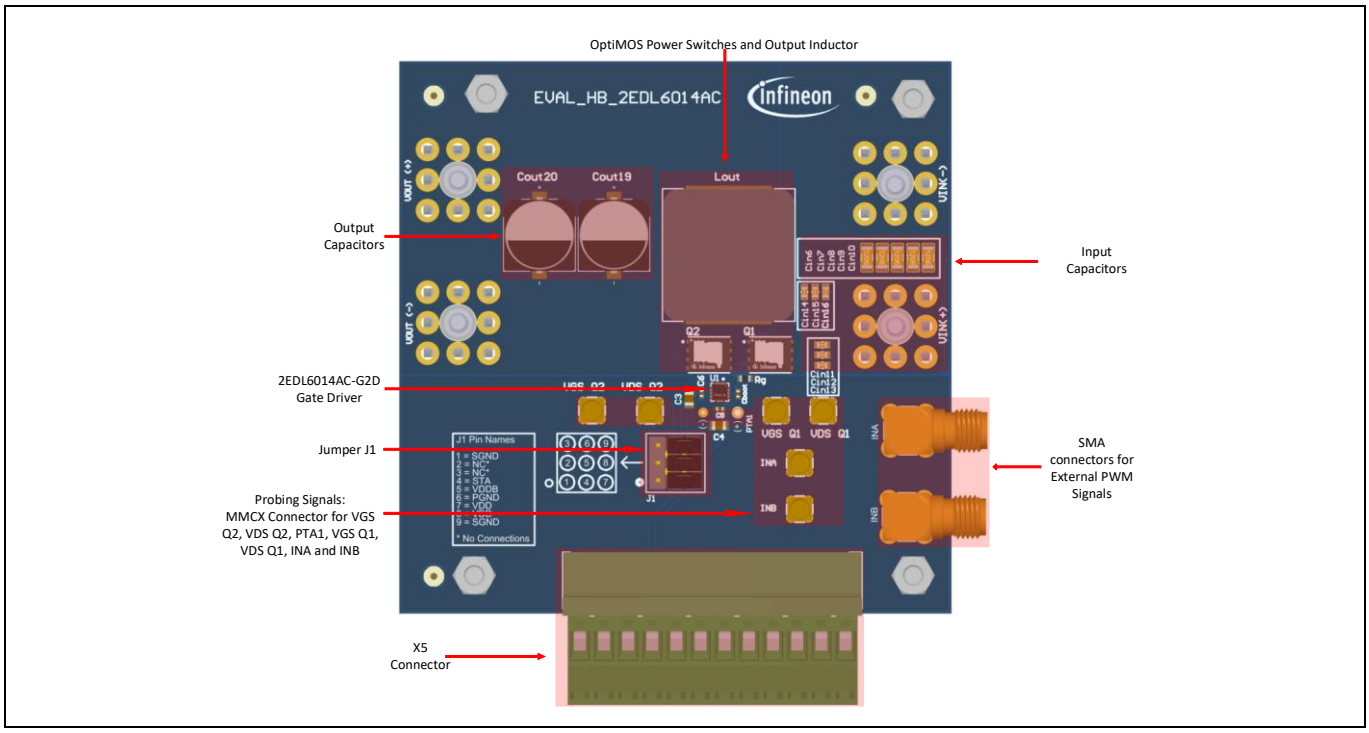

Figure 5 Board description – top layer

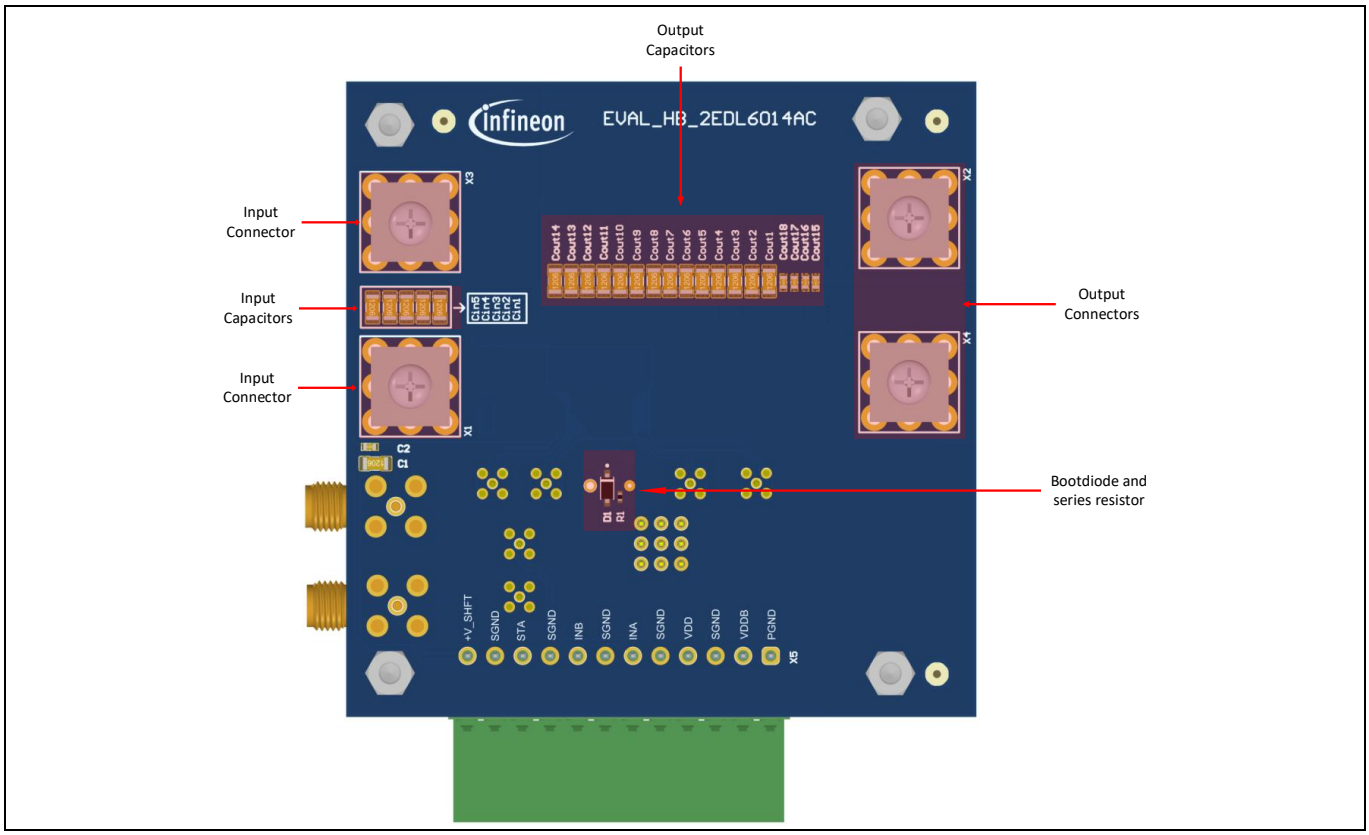

Figure 6 Board description – bottom layer

2.2 Jumper

Jumper J1 has two functionalities. Firstly, it allows manual setting of the STA condition, either tied to VDD or to SGND. Secondly, it configures the board for either a non-voltage-level-shifted or a voltage-level-shifted configuration.

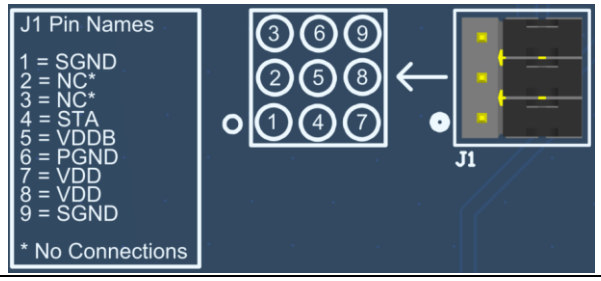

Figure 7 Jumper J1

Table 2 Jumper J1 settings

Configuration		STA condition	
Non-voltage-level shifted	**Voltage-level-shifted**	**Low**	**High**
Short pins 6 and 9	Float pins 6 and 9	Short pins 1 and 4	Short pins 4 and 7

2.3 SMA terminals for PWM inputs

The SMA connectors are provided for use with external function generators that require a BNC-to-SMA cable to input the two PWM signals.

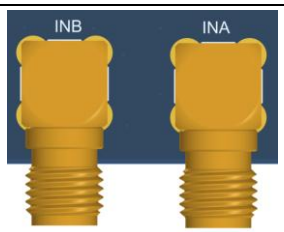

Figure 8 SMA connector terminals for input PWMs signals

2.4 Supply and signal terminals

The X5 connector provides supply and signal terminals, facilitating easy connection and testing during lab verification.

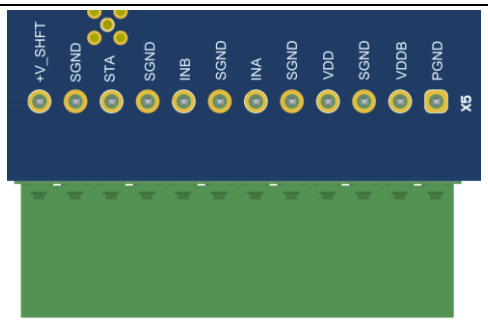

Figure 9 X5 Connector for external power supply and signals

Table 3 X5 connector functional description

Name	Description
+V_SHFT	Supply voltage when in voltage-level-shifted configuration. The voltage is the shifted voltage level
SGND	Signal ground (reference ground for the VDD, STA, INA, INB and +V_SHFT)
STA	Connector pin for STA if an external signal is required for testing. To use an external STA signal, keep pin 4 of Jumper J1 open
SGND	Signal ground (reference ground for the VDD, STA, INA, INB and +V_SHFT)
INB	Input PWM of the gate driver for driving Q2 gate to source voltage
SGND	Signal ground (reference ground for the VDD, STA, INA, INB and +V_SHFT)
INA	Input PWM of the gate driver for driving Q1 gate to source voltage
SGND	Signal ground (reference ground for the VDD, STA, INA, INB and +V_SHFT)
VDD	Input circuitry supply voltage. Reference to SGND
SGND	Signal ground (reference ground for the VDD, STA, INA, INB and +V_SHFT)
VDDB	Supply voltage for the OUTB output channel
PGND	Power ground (reference ground for VDDB and Kelvin Source connected to Q2 source pin)

2.5 MMCX connectors and probe tip adapters for waveform measurements

The board features designated test points for easy connection to an oscilloscope, allowing for the measurement and analysis of waveforms.

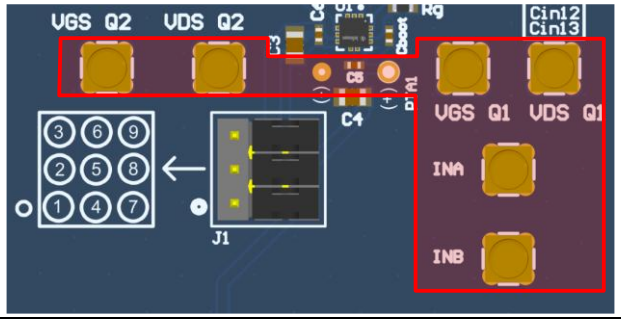

Figure 10 Test points available in EVAL_HB_2EDL6014AC

Table 4 Functional description of the test points

Test points	Description
VGS Q2	Gate to source voltage of Q2 (Low-side MOSFET)
VDS Q2	Drain to source voltage of Q2 (Low-side MOSFET)
PTA1	Probe tip point for VDD supply
VGS Q1	Gate to source voltage of Q1 (High-side MOSFET)
VDS Q1	Drain to source voltage of Q1 (High-side MOSFET)
INA	Input PWM of the gate driver for driving Q1
INB	Input PWM of the gate driver for driving Q2

2.6 Power input and output terminals

Use the terminals to connect power cables for the input voltage source and electronic load.

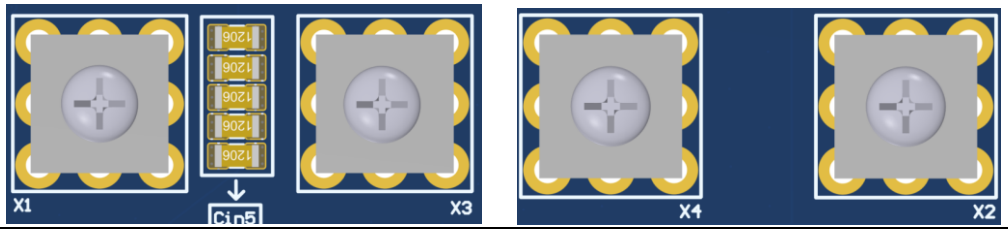

Figure 11 Input and output connector terminals

Table 5 Functional description of power terminals

Board label	Schematic designation	Description
VIN(-)	X3	Return ground of the converter's input voltage source
VIN(+)	X1	Positive terminals of the converter's input voltage source
VOUT (+)	X2	Positive terminals of the converter's output load
VOUT (-)	X4	Return ground of the converter's output load

3 Configuration

3.1 Non-voltage-level-shifted

In a non-voltage-level-shifted configuration, the evaluation board operates similarly to a typical half-bridge buck converter. The reference ground for the INA, INB, VDD and STA is connected to the signal ground (SGND). In contrast, the reference ground for the power buck converter and VDDB is connected to the power ground (PGND). To configure the board in this mode, use jumper J1 to short SGND and PGND together. J1 provides a convenient way to connect and disconnect SGND to PGND.

When SGND and PGND are connected, the result is a common ground for both SGND and PGND. This simplifies the board's configuration and allows for easier testing and evaluation.

Table 6 Jumper J1 settings for non-voltage-level-shifted configuration

J1 pin status	Description
Short pins 6 and 9	Shorting nodes SGND and PGND to have a common ground

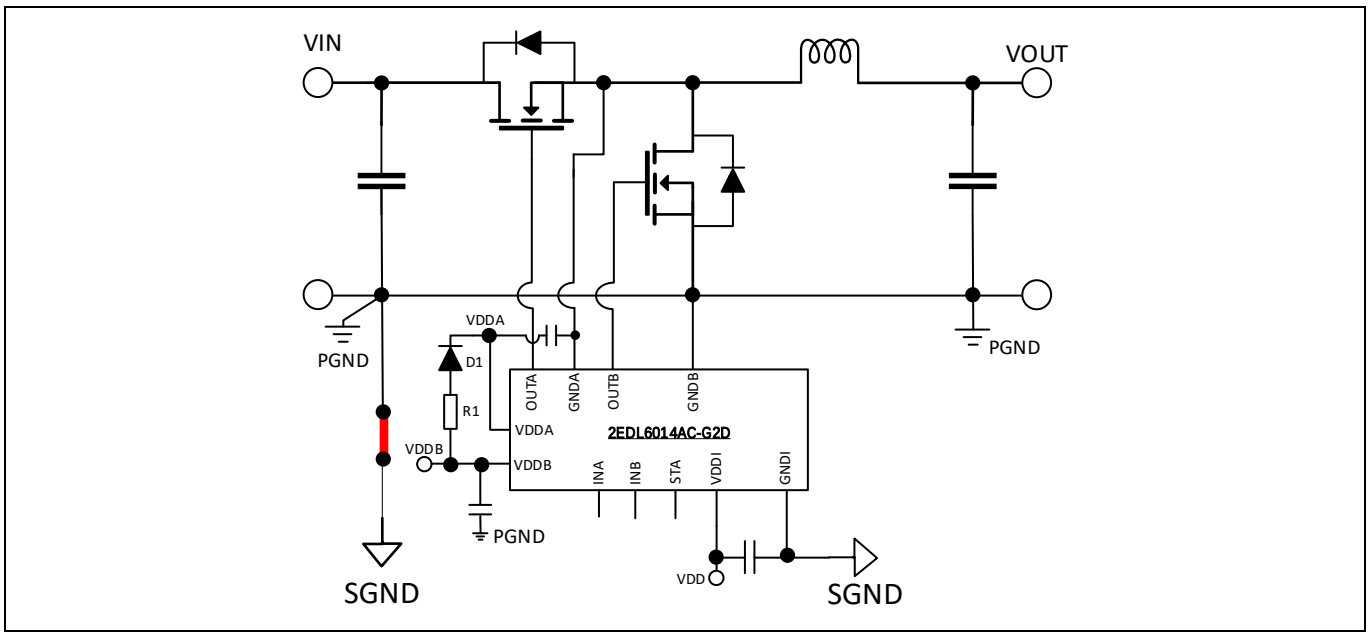

Figure 12 Effective circuit in non-voltage-level-shifted configuration

3.2 Voltage-level-shifted

In the voltage-level-shifted configuration, the evaluation board still operates as a buck converter, but with a key difference. The PGND is positively voltage-level-shifted with respect to the SGND. This voltage shift is achieved through an external supply, which is applied via the +V_SHFT pin, referenced to SGND. The +V_SHFT pin provides a convenient way to introduce the voltage shift, allowing users to control the level of shift and optimize the board's performance.

In this configuration, it's essential to note that VDD and VDDB have different reference grounds. VDD is referenced to SGND, while VDDB is referenced to PGND. As a result, pins 6 and 9 in jumper J1 must be kept floating to maintain the voltage level shift and prevent any unintended connections between the two grounds. By keeping these pins floating, users can ensure that the voltage level shift is preserved, and the board operates correctly.

To summarize, the key characteristics of the voltage-level-shifted configuration are:

- PGND is positively voltage-level-shifted with respect to SGND
- The voltage shift is achieved through an external supply applied via +V_SHFT
- VDD and VDDB have different reference grounds (SGND and PGND, respectively)
- Pins 6 and 9 in jumper J1 must be kept floating to maintain the voltage level shift

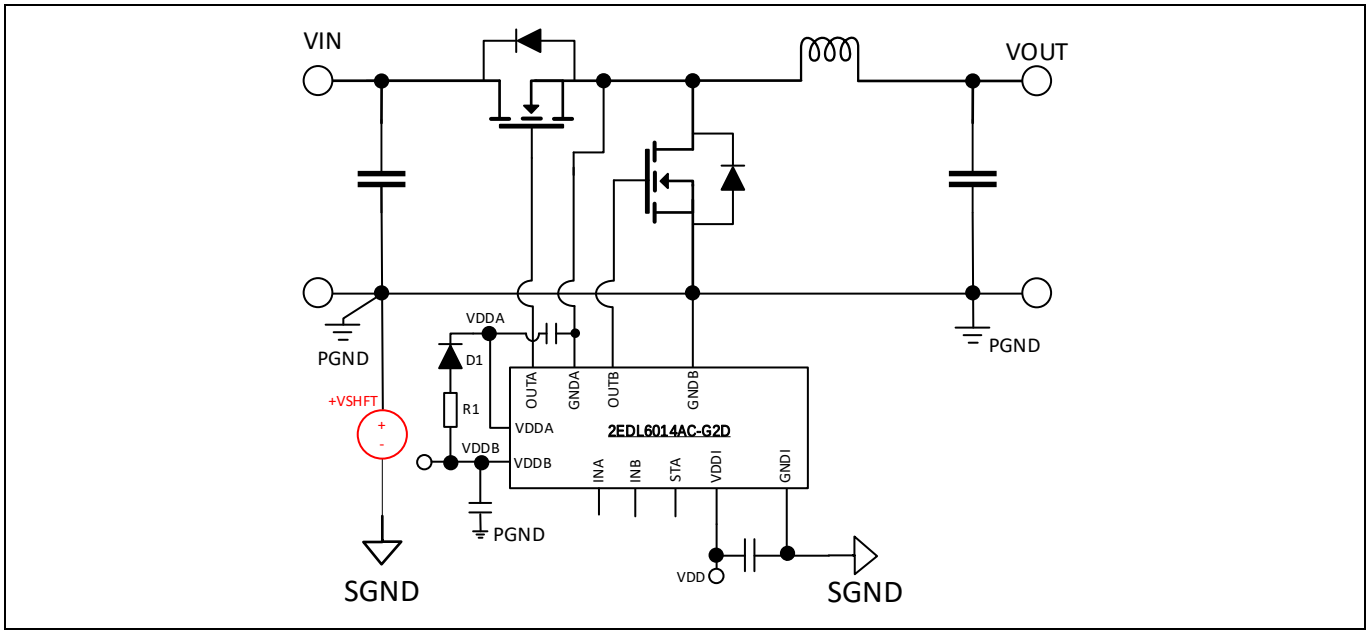

Figure 13 Effective circuit in voltage-level-shifted configuration

Table 7 Jumper J1 setting for voltage-level-shifted configuration

J1 pin status	Notes
Float pins 6 and 9	VDD-SGND and VDDB-PGND must have a dedicated external supply in which its reference is not in common ground

3.3 STA function

The STA pin allows programming of the peak source driving current capability of OUTA into two distinct levels:

- **Low current mode:** When the STA pin is tied to SGND (low), the peak source current is limited to 500 mA
- **High current mode:** When the STA pin is tied to VDD (high) or left floating, the peak source current is increased to 4 A

To ensure optimal noise immunity, it is recommended to connect the STA pin to a stable DC signal, such as VDD. This provides a more reliable and noise-resistant configuration.

Table 8 Jumper J1 setting for STA conditions

STA Condition	J1 pin status	Description
Low	Short pins 1 and 4	Shorting STA pin to SGND
High	Short pins 4 and 7	Shorting STA pin to VDD

4 Test setup sequence

4.1 Non-voltage-level-shifted configuration

1. Configure Jumper J1 per Table 6
2. Configure Jumper J1 depending on the preferred STA conditions per Table 8
3. Supply the following:
   - VDD to SGND in the X5 connector
   - VDDB to PGND in the X5 connector
   - Input PWMs signal to the SMA connectors from a signal generator
4. Connect input voltage source for the buck converter with the positive terminal on VIN (+) and ground on VIN (-)
5. Connect electronic load for the buck converter with the positive terminal on VOUT (+) and ground on VOUT (-)

4.2 Voltage-level-shifted configuration

1. Configure Jumper J1 per Table 7
2. Configure Jumper J1 depending on the preferred STA conditions per Table 8
3. Supply the following:
   - VDD to SGND in the X5 connector
   - VDDB to PGND in the X5 connector
   - Supply a positive +V_SHFT voltage in reference to SGND in the X5 connector
   - Input the PWM signal to the SMA connector from a signal generator
4. Connect the input voltage source for the buck converter with the positive terminal on VIN (+) and ground on VIN (-)
5. Connect an electronic load for the buck converter with the positive terminal on VOUT (+) and ground on VOUT (-)

5 System design

5.1 Schematics

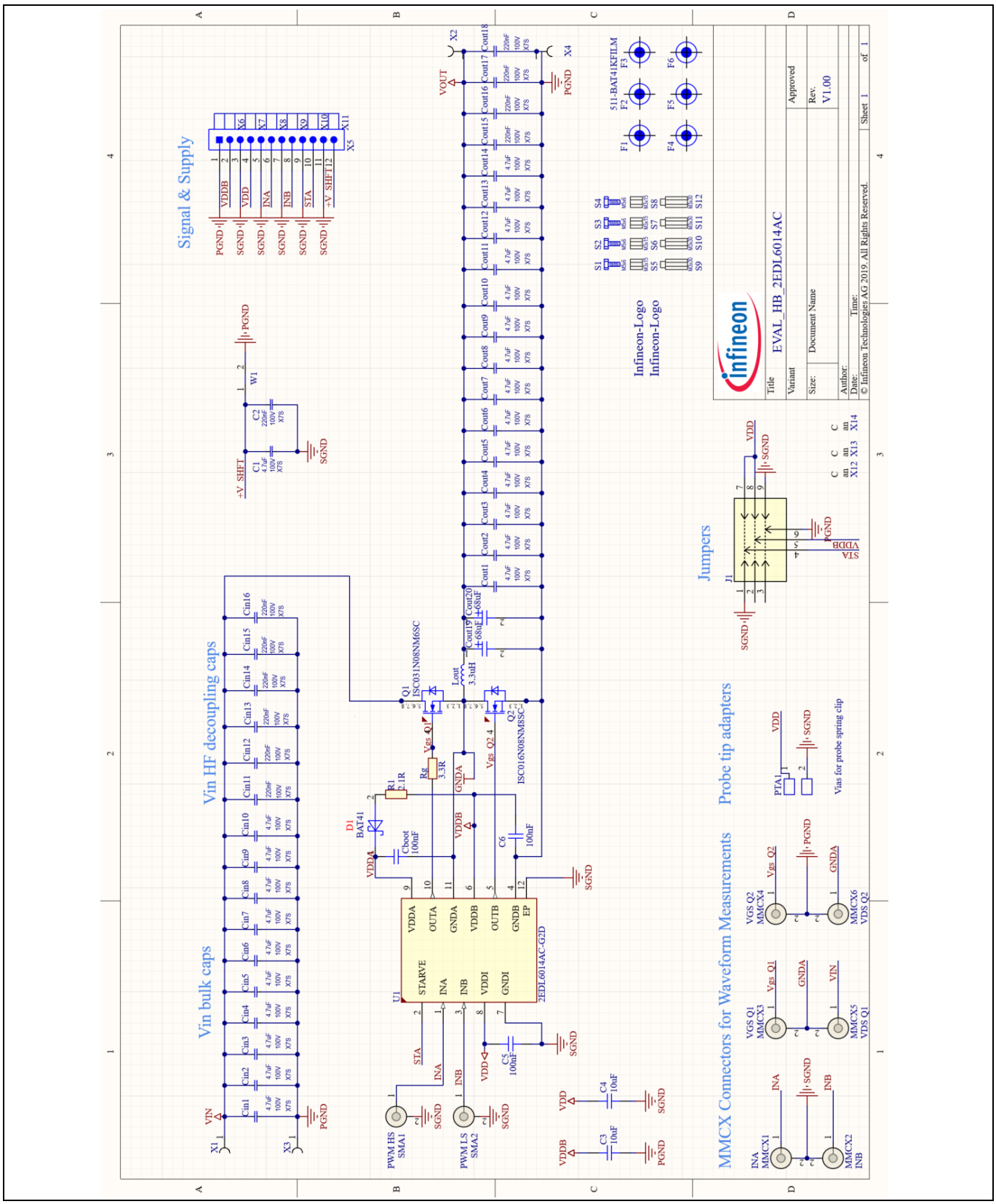

Figure 14 Schematic of the buck converter's power stage

5.2 Layout

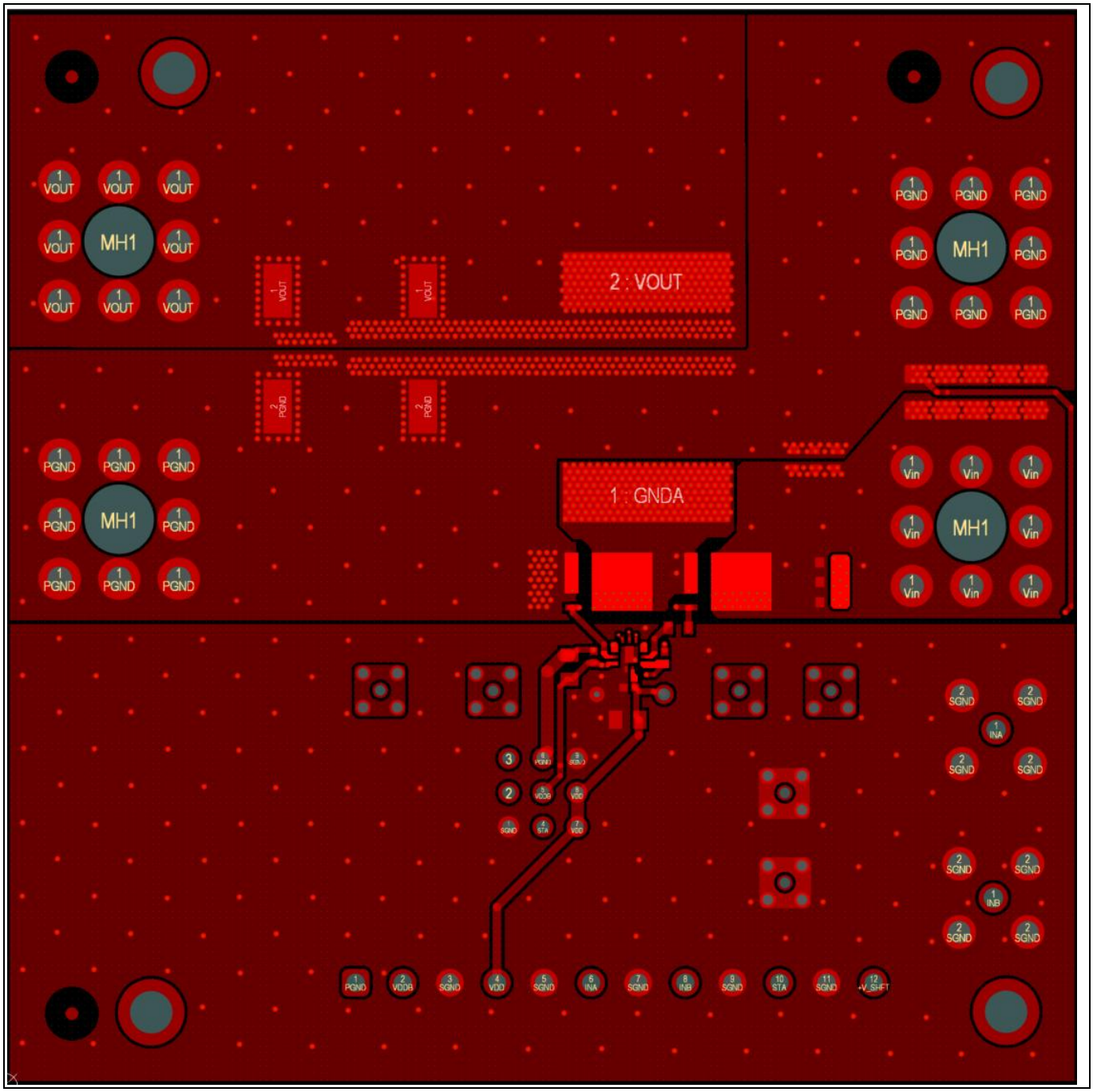

Figure 15 Top layer – Layer 1

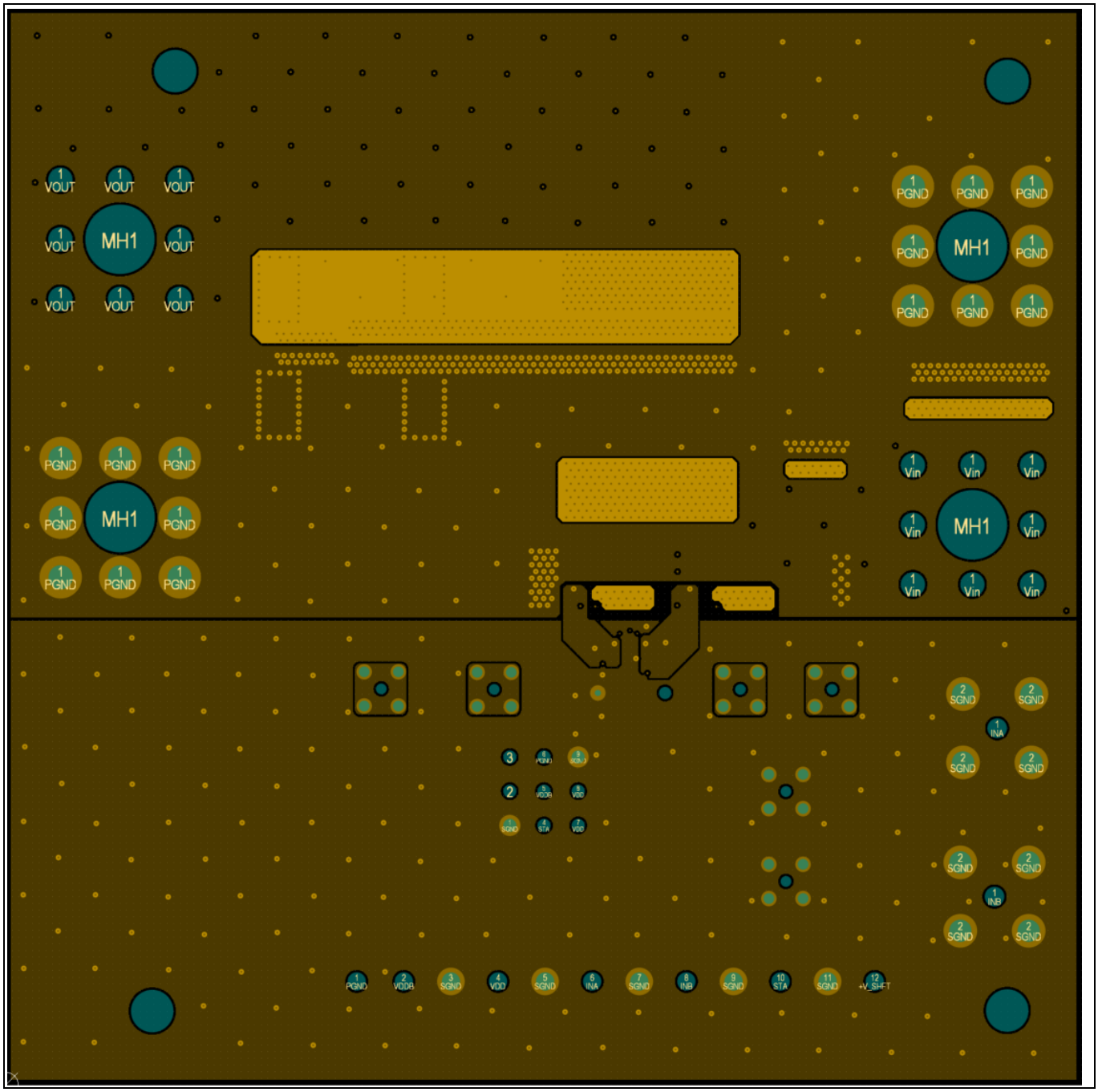

Figure 16 Layer 2

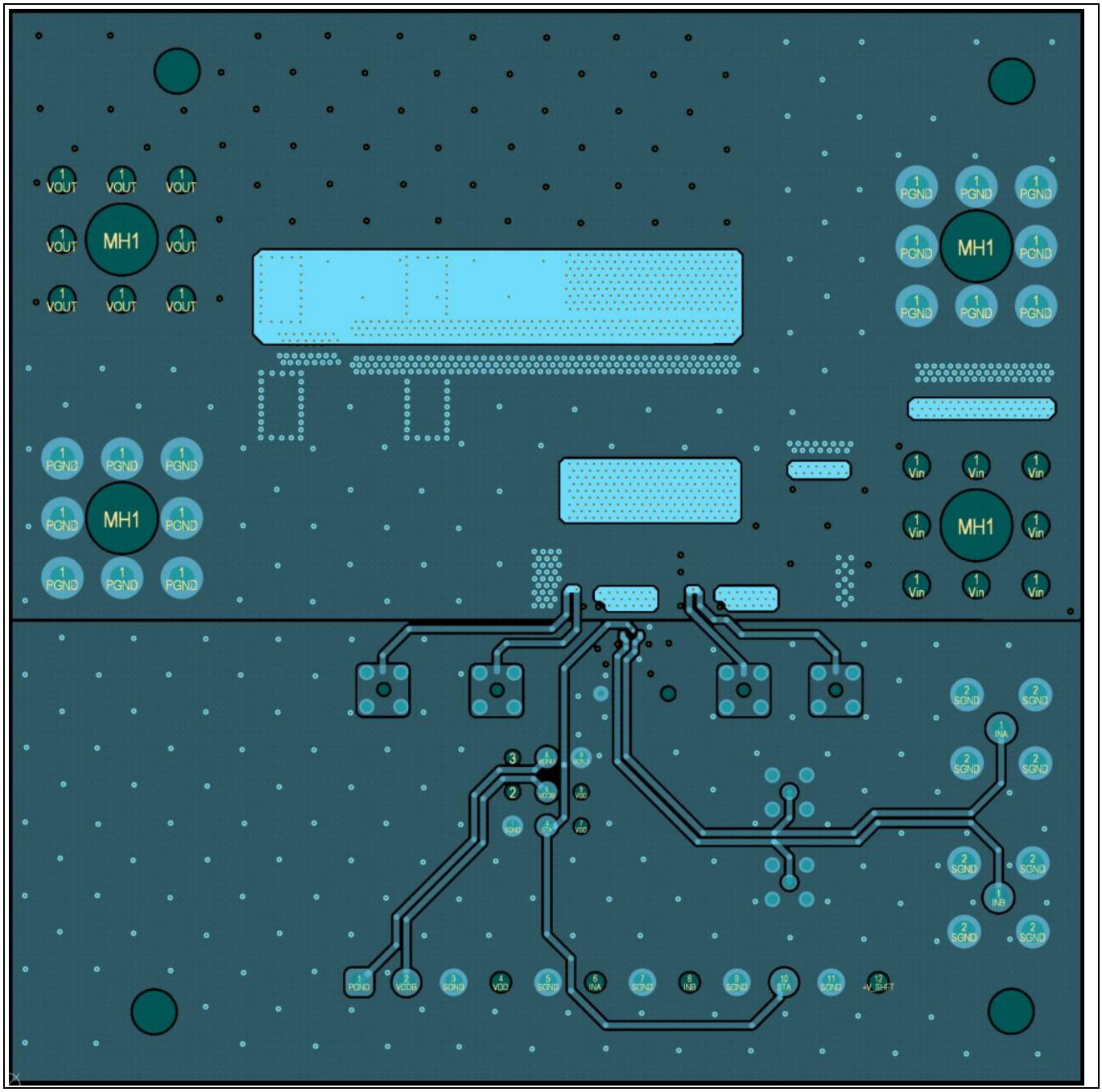

Figure 17 Layer 3

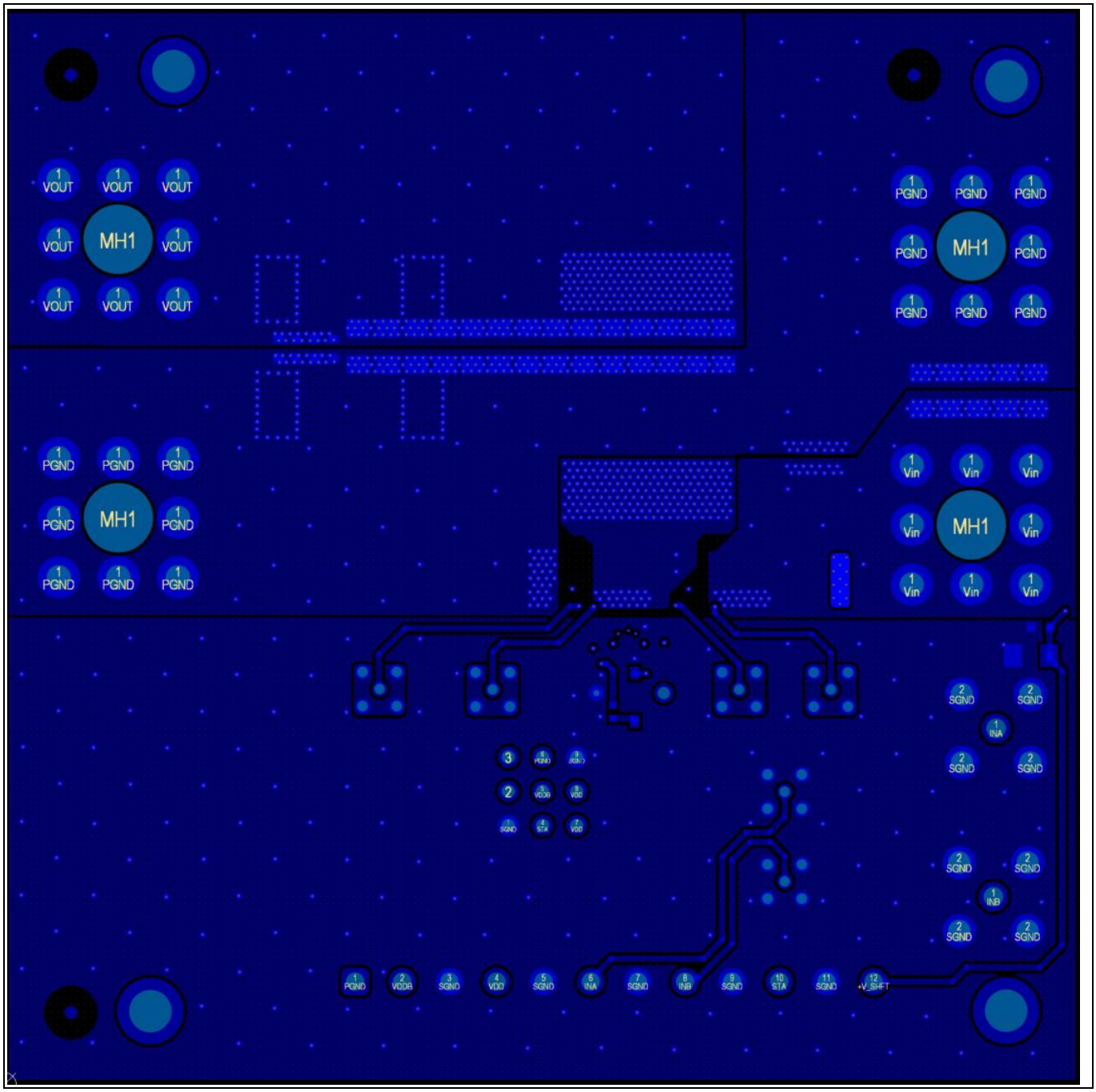

Figure 18 Bottom layer – Layer 4

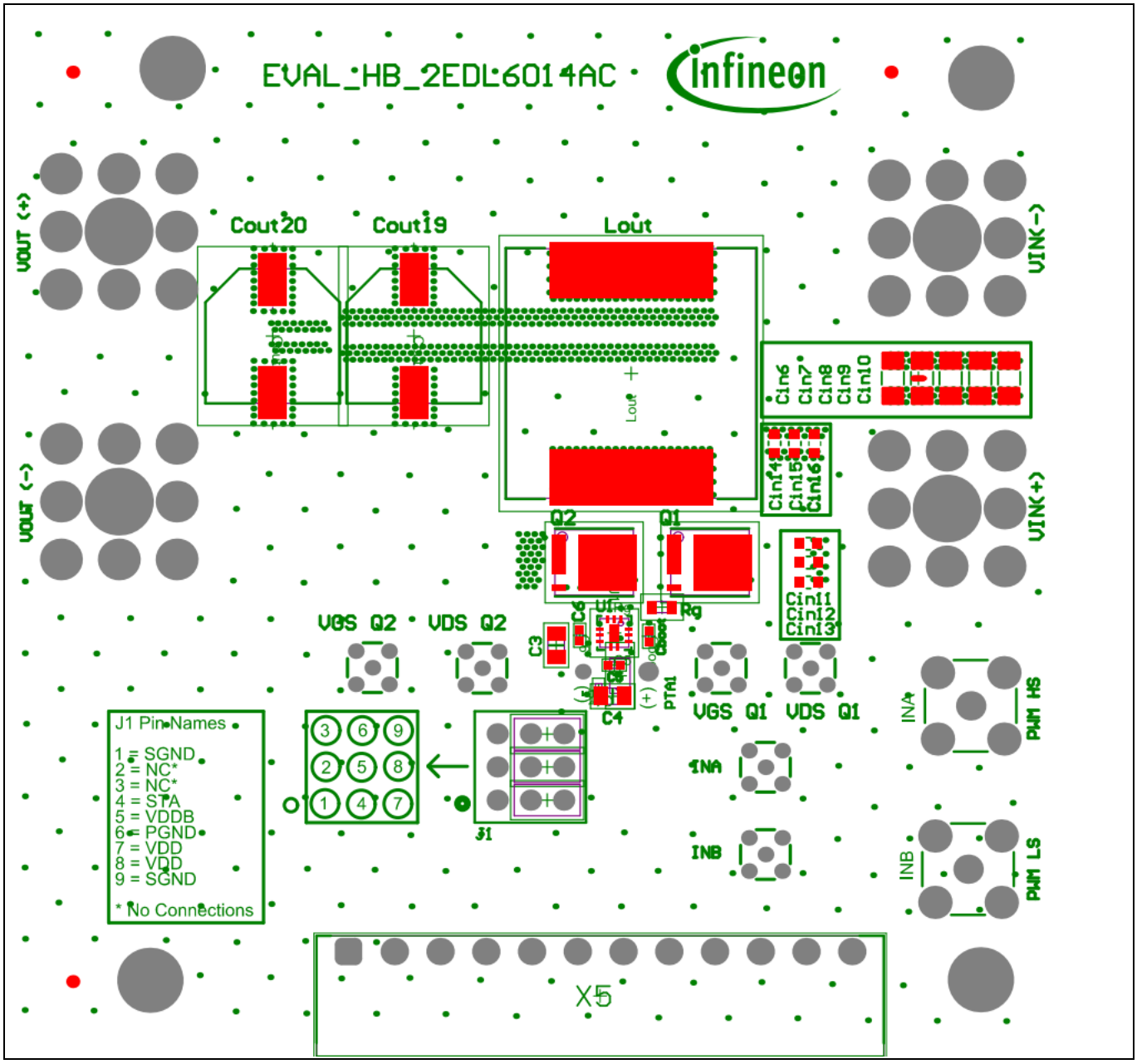

Figure 19 Component assembly – top side

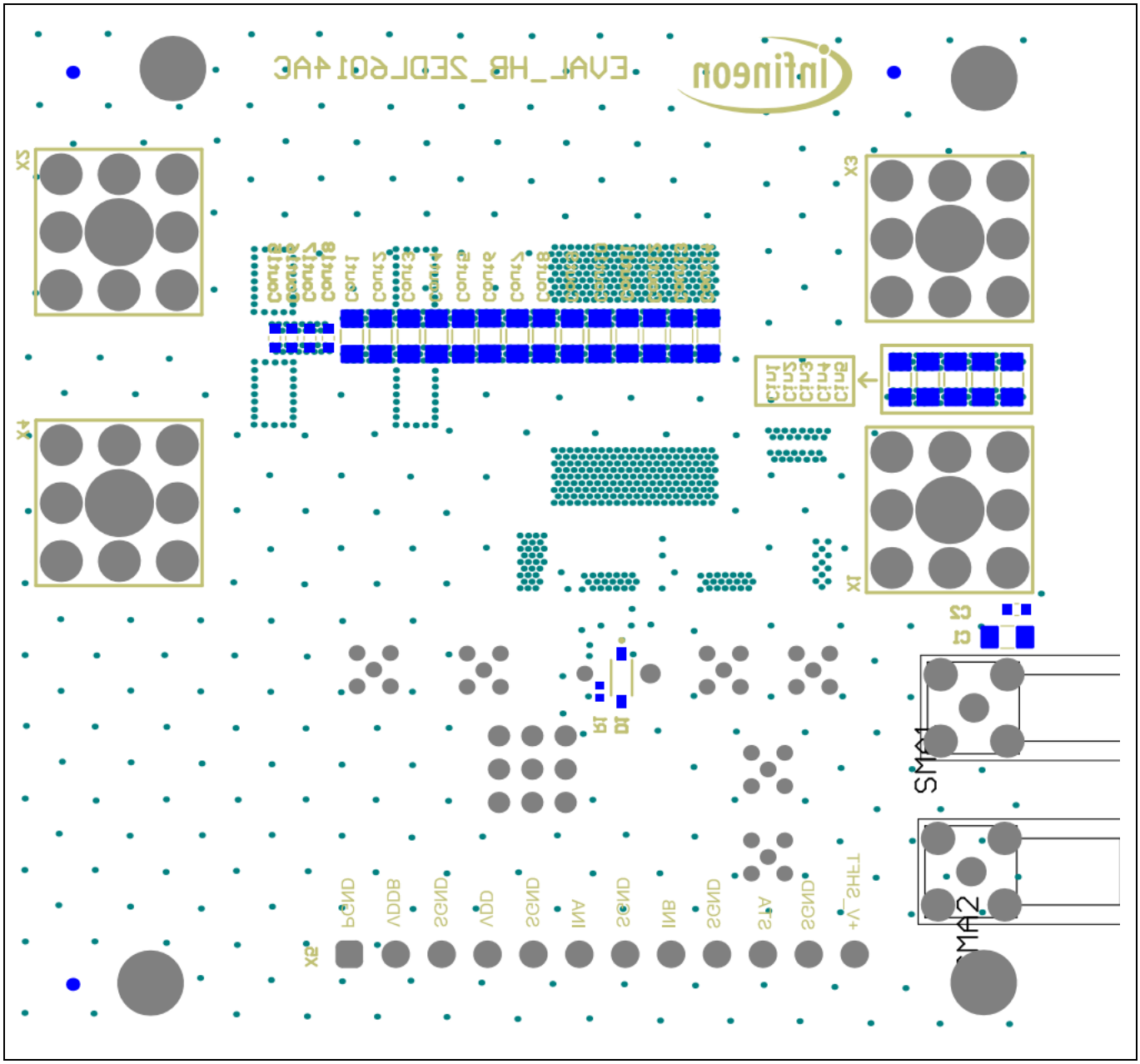

Figure 20 Component assembly – bottom side

5.3 Bill of materials

Table 9 BOM list

Designator	Qty	Value	Manufacturer	Manufacturer part number/ Manufacturer order number
C1, Cin1, Cin2, Cin3, Cin4, Cin5, Cin6, Cin7, Cin8, Cin9, Cin10, Cout1, Cout2, Cout3, Cout4, Cout5, Cout6, Cout7, Cout8, Cout9, Cout10, Cout11, Cout12, Cout13, Cout14	25	4.7 µF	Murata	GRM31CC72A475ME11L
C2, Cin11, Cin12, Cin13, Cin14, Cin15, Cin16, Cout15, Cout16, Cout17, Cout18	11	220 nF	Taiyo Yuden	HMK107C7224KAHTE
C3, C4	2	10 µF	Murata	GRM21BR61E106MA73L
C5, C6, Cboot	3	100 nF	Murata	GRM155R71H104KE14D
Cout19, Cout20	2	68 µF	Nichicon	PCR1K680MCL1GS
D1	1	100 V	STMicroelectronics	BAT41ZFILM
J1	1		Samtec	TSW-103-07-G-T
Lout	1	3.3 µH	Vishay	IHLP7575GZER3R3M5A
MMCX1, MMCX2, MMCX3, MMCX4, MMCX5, MMCX6	6		Würth Elektronik	66012002111503
Q1	1		Infineon Technologies	ISC031N08NM6SC
Q2	1		Infineon Technologies	ISC016N08NM8SC
R1	1	2.1R	Vishay	CRCW04022R10FKED
Rg	1	3.3R	Vishay	CRCW06033R30FKEA
S1, S2, S3, S4	4	M5x6	RS PRO	914-1510
S5, S6, S7, S8	4		Wuerth Elektronik	970150321
S9, S10, S11, S12	4		Wuerth Elektronik	971300321
SMA1, SMA2	2		Würth Elektronik	60311002111526
U1	1		Infineon Technologies	2EDL6014AC-G2D
X1, X2, X3, X4	4		Würth Elektronik	74655095R
X5	1		Würth Elektronik	691322110012
X6, X7, X8, X9, X10, X11	6		Würth Elektronik	691363110002
X12, X13, X14	3		Würth Elektronik	609002115121

6 System performance

6.1 Test conditions

- VIN = 36 V to 60 V
- D = 25%
- Maximum load current = 15 A
- fsw = 200 kHz
- VDD - SGND = 5 V
- VDDB - PGND = 10 V
- No fan and at room ambient temperature
- CONFIGURATION: Non-voltage-level-shifted and voltage-level-shifted

Note: In voltage-level-shifted configuration, +V_SHFT to SGND = +10 V and VDDB – PGND = 12 V.

6.2 Test waveforms

6.2.1 Non-voltage-level-shifted configuration

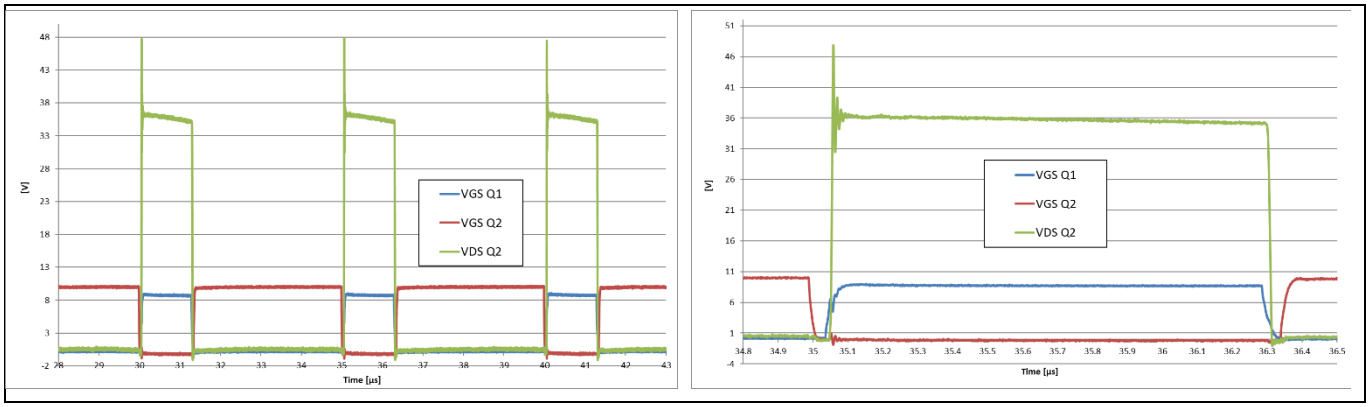

Figure 21 Gate-to-source voltage of Q1, Q2 and drain-to-source voltage of Q2 at Vin = 36 V, 15 A load current

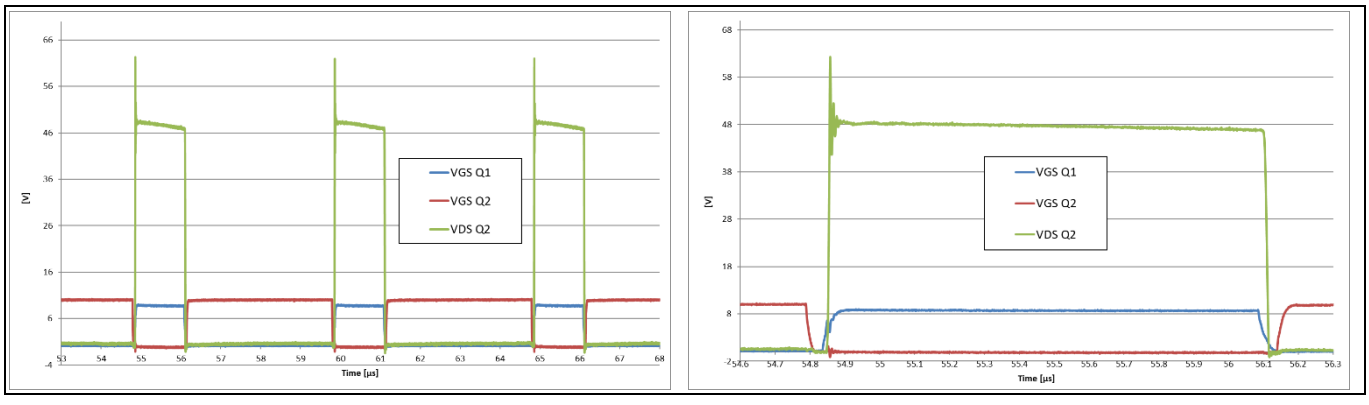

Figure 22 Gate-to-source voltage of Q1, Q2 and drain-to-source voltage of Q2 at Vin = 48 V, 15 A load current

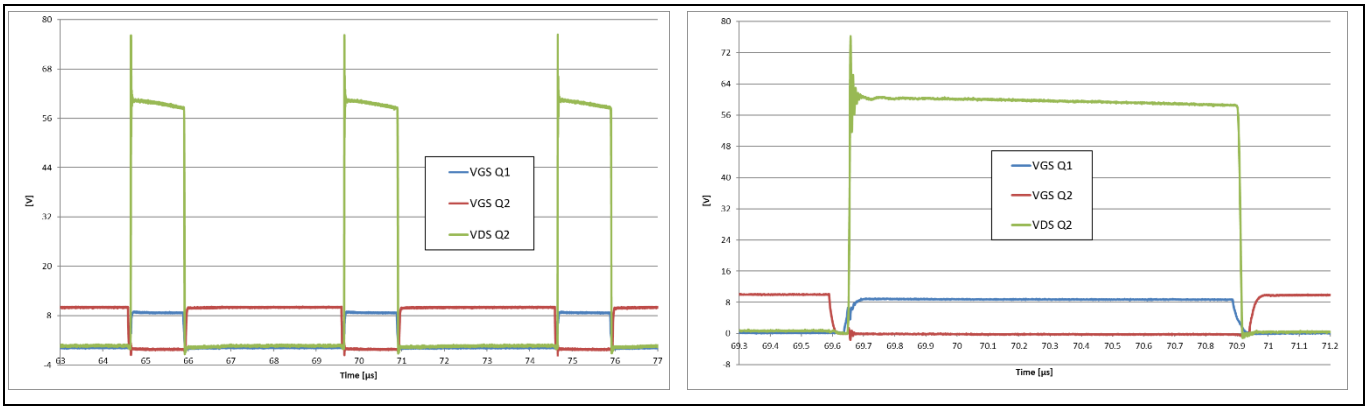

Figure 23 **Gate-to-source voltage of Q1, Q2 and drain-to-source voltage of Q2 at Vin = 60 V, 15 A load current**

6.2.2 Voltage-level-shifted configuration

Note: *In voltage-level-shifted configuration, the VDS Q2 waveform is not included. Waveforms focus on the switching transition of the two output channels.*

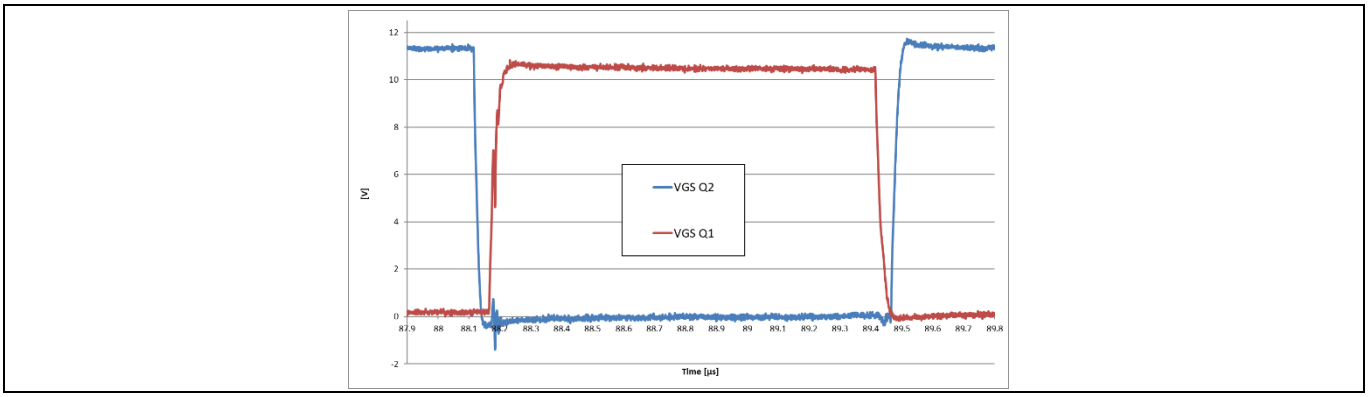

Figure 24 **VGS Q1 and VGS Q2 at Vin = 36 V, 15 A load current**

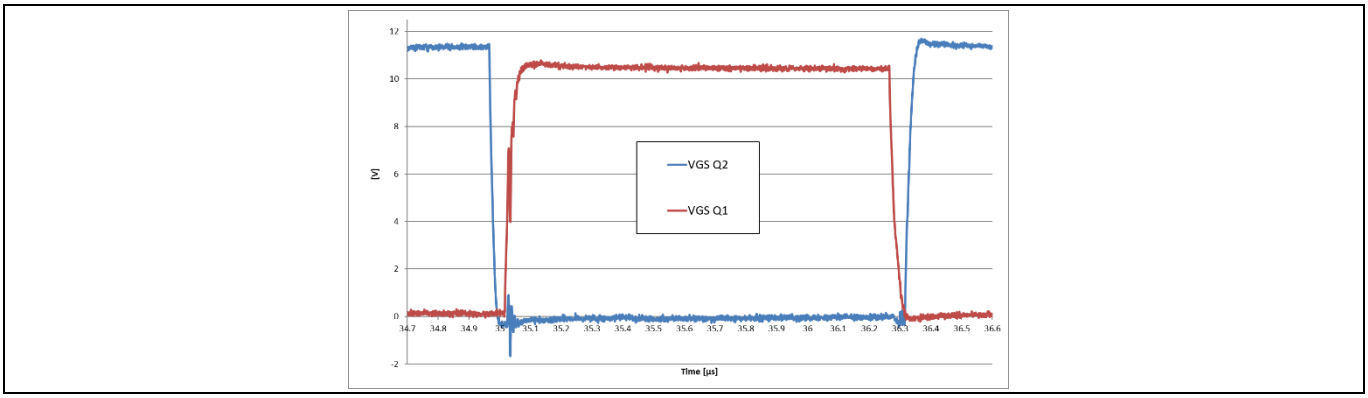

Figure 25 **VGS Q1 and VGS Q2 at Vin = 48 V, 15 A load current**

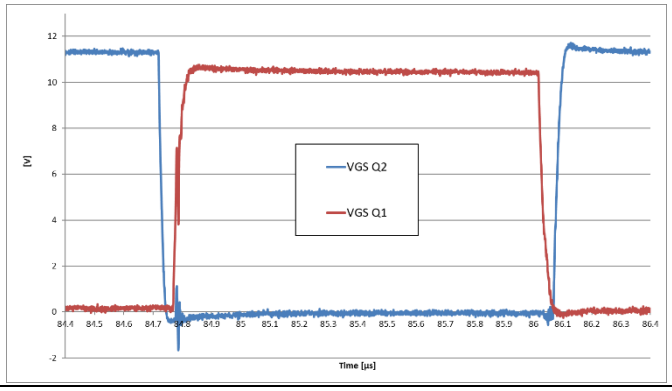

Figure 26 VGS Q1 and VGS Q2 at Vin = 60 V, 15 A load current

6.2.3 STA functions and thermal performances

Note: All waveforms and data in this section were performed in non-voltage-level-shifted configuration.

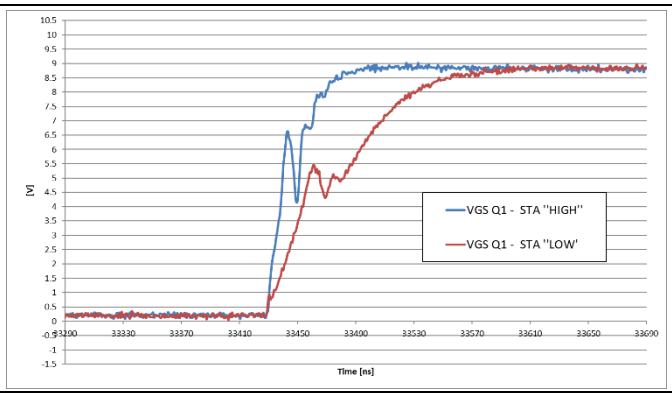

Figure 27 STA Functionality. Waveform at Vin = 48 V, 15 A load current

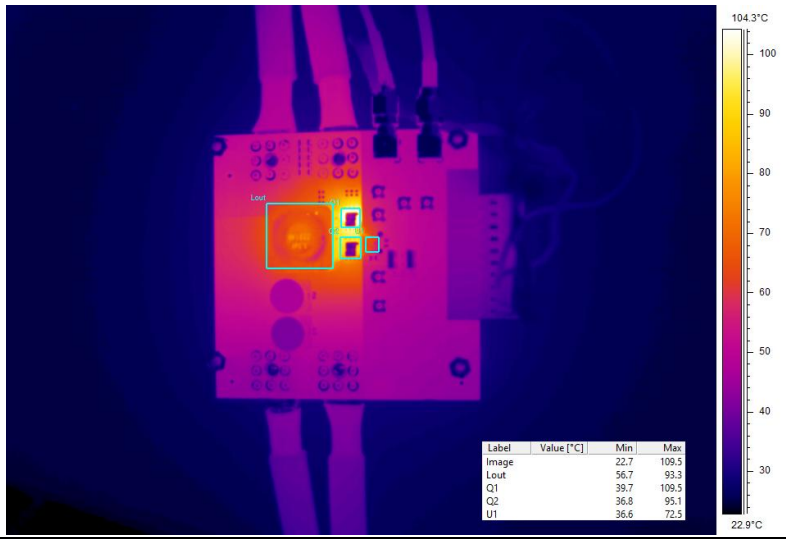

Figure 28 Thermal performances of Lout, Q1, Q2 and U1 at Vin = 60 V, 15 A load current with 300 kHz switching frequency, no fan and at room ambient temperature (worst-case condition)

Related resources

- Gate driver ICs
- Developer Community forum

References

[1] Infineon Technologies AG: *2EDL6014AC-G2D web page*; Available online

Abbreviations or acronyms

Abbreviation	Expanded form
BNC	Bayonet Neill-Concelman connector
DSC	Dual-side cooled package
fsw	Switching frequency
IBC	Intermediate bus converter
INA	Input A
INB	Input B
MMCX	Micro Miniature Coaxial Connector
PGND	Power ground
SGND	Signal ground
SMA	SubMiniature version A connector
STA	Source current trim adjust pin
VDD	Gate driver supply voltage
VDDB	Floating channel supply voltage
VDS	Drain-to-source voltage
VGS	Gate-to-source voltage
VIN	Input Voltage

Revision history

Document revision	Date	Description of changes
V 1.0	2026-05-20	Initial release

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