Using monolithic high-voltage gate drivers

About this document

Scope and purpose

This document highlights the most common subjects driving a half-bridge power stage in motor drive applications (with monolithic IC gate driver) and to suggest appropriate solutions to solve the problems.

Intended audience

The intended audiences for this document are design engineers, technicians, and developers of electronic systems.

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1 Introduction

This document highlights the most common subjects driving a half-bridge power stage in motor drive applications (with monolithic IC gate driver) and to suggest appropriate solutions to solve the issues.

Topics such as the sizing of some fundamental components, as bootstrap circuit and on/off gate resistors; and half-bridge parasitic elements with their effects are discussed. Some possible solutions are proposed and finally, some layout tips are presented.

All the situations and the solutions proposed are, unless otherwise specified, for a typical Infineon monolithic gate driver with floating bootstrap supply.

2 The bootstrap circuit

The bootstrap supply is formed by a diode and a capacitor connected as shown in Figure 1.

This method has the advantage of being simple and low cost, but may force some limitations on duty-cycle and on-time as they are limited by the requirement to refresh the charge in the bootstrap capacitor.

Choosing an appropriate capacitor can drastically reduce these limitations.

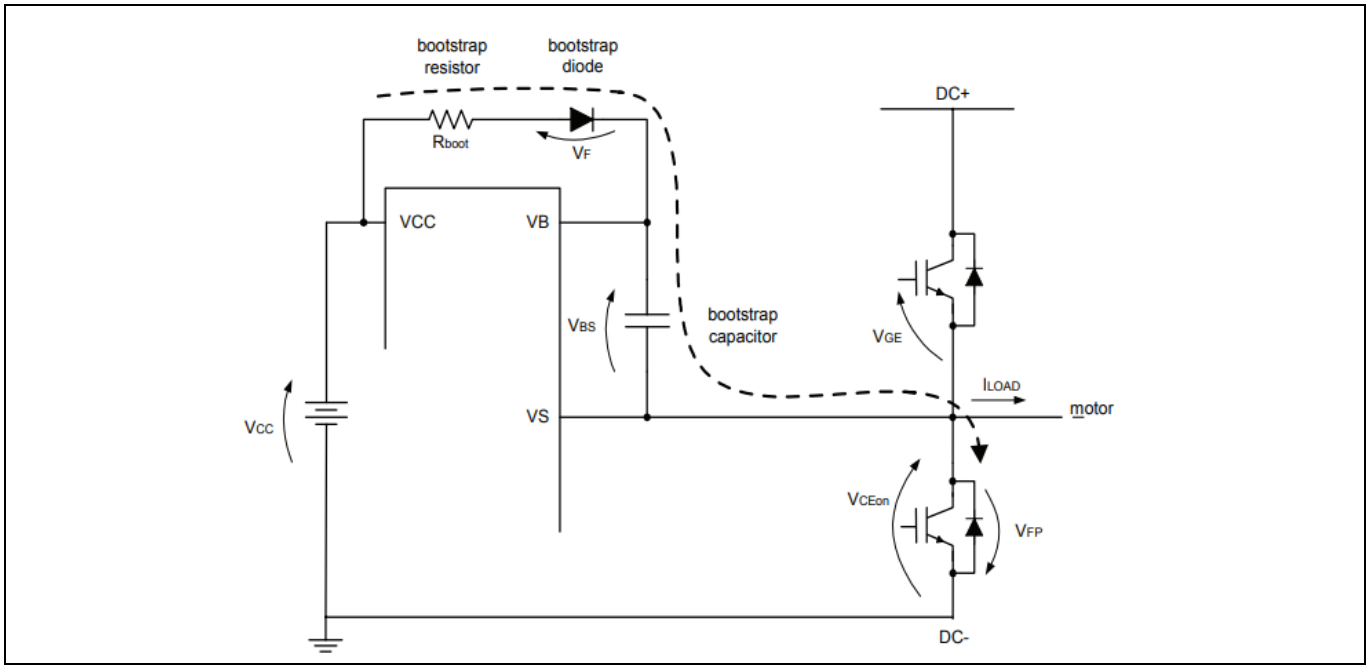


Figure 1 Bootstrap supply schematic

2.1 Bootstrap capacitor sizing

To size the bootstrap capacitor, the first step is to establish the minimum voltage drop (ΔV_{BS}) that is guaranteed when the high-side IGBT is on. If V_{GEmin} is the minimum gate emitter voltage to maintain, the voltage drop must be:

$$\Delta V_{BS} \leq V_{CC} - VF - V_{GEmin} - V_{CEon}$$

Equation 1

under the condition:

$$V_{GEmin} > V_{BSUV-}$$

Equation 2

Here, V_{CC} is the IC voltage supply, V_F is bootstrap diode forward voltage, V_{CEon} is emittercollector voltage of the low-side IGBT, and V_{BSUV-} is the high-side supply undervoltage negative going threshold.

The bootstrap circuit

Now, consider the influencing factors causing the decrease in V_{BS}:

- IGBT turn-on required gate charge (Q_G);
- IGBT gate-source leakage current (I_{LK_GE});
- Floating section quiescent current (I_{QBS});
- Floating section leakage current (I_{LK})
- Bootstrap diode leakage current (I_{LK_DIODE});
- Desat diode bias when on (I_{DS-})
- Charge required by the internal level shifters (Q_{LS});
- Bootstrap capacitor leakage current (I_{LK_CAP});
- High-side ON time (T_{HON}).

I_{LK_CAP} is only relevant when using an electrolytic capacitor and can be ignored if other types of capacitors are used. Using at least one low ESR ceramic capacitor is strongly recommended (paralleling electrolytic and low ESR ceramic may result in an efficient solution).

Then we have:

$$Q_{TOT} = Q_G + Q_{LS} + (I_{LK\_GE} + I_{QBS} + I_{LK} + I_{LK\_DIODE} + I_{LK\_CAP} + I_{DS-}) \times T_{HON}$$

Equation 3

The minimum size of the bootstrap capacitor is:

$$C_{BOOTmin} = \frac{Q_{TOT}}{\Delta V_{BS}}$$

Equation 4

For example:

a) Using a 25 A IGBT (IRGP30B120KD) at 125°C and a high voltage half-bridge gate driver (IR2214SS):

- I_{QBS} = 800 µA (Datasheet IR2214SS);
- I_{LK} = 50 µA (Datasheet IR2214SS);
- Q_{LS} = 20 nC; QG = 160 nC (Datasheet IRGP30B120KD);
- I_{LK_GE} = 100 nA (Datasheet IRGP30B120KD);
- I_{LK_DIODE} = 100 µA (with reverse recovery time <100 ns);
- I_{LK_CAP} = 0 (ignored for ceramic capacitor);
- I_{DS-} = 150 µA (Datasheet IR2214SS);
- T_{HON} = 100 µs.

The bootstrap circuit

And:

- V_{CC} = 15 V
- V_F = 1 V
- $V_{CEonmax}$ = 3.1 V
- V_{GEmin} = 10.5 V

the maximum voltage drop, ΔV_{BS}, becomes:

$$\Delta V_{BS} \leq V_{CC} - V_F - V_{GEmin} - V_{CEon} = 15V - 1V - 10.5V - 3.1V = 0.4V$$

Equation 5

and the bootstrap capacitor is:

$$C_{BOOT} = \frac{290\ nC}{0.4\ V} = 725\ nF$$

Equation 6

Notes:

- Here V_{CC} was chosen to be 15 V. Some IGBTs may require higher supply to work properly with the bootstrap technique. Also V_{CC} variations must be considered in the abovementioned formulas
- This kind of bootstrap sizing approach does NOT take into account either the duty cycle of the PWM or the fundamental frequency of the current. It considers only the amount of charge that is required when the high voltage side of the driver is floating and the IGBT gate has been driven once.

The PWM duty cycle and the type of modulation (6-step, 12-step, sine-wave) must be considered, with their own peculiarities, to achieve the best sizing for the bootstrap circuit.

2.2 Considerations about the bootstrap circuit

2.2.1 Voltage ripple

Three different situations can occur during bootstrap-capacitor charging (see Figure 1):

- $I_{LOAD} < 0$: The load current flows in the low-side IGBT displaying relevant V_{CEon}

$$V_{BS} = V_{CC} - V_F - V_{CEon}$$

Equation 7

In this case, we have the lowest value for V_{BS}. It represents the worst case for bootstrap-capacitor sizing. When the IGBT is turned off the Vs node is pushed up by the load current until the high-side freewheeling diode gets forward biased.

- I_{LOAD} = 0: The IGBT is not loaded while its on and V_{CE} can be neglected

$$V_{BS} = V_{CC} - V_F$$

Equation 8

- I_{LOAD} > 0: The load current flows through the freewheeling diode

$$V_{BS} = V_{CC} - V_F + V_{FP}$$

Equation 9

In this case, we have the highest value for V_{BS}. When the high-side IGBT is turned on, I_{LOAD} flows into it and V_S is pulled up.

To minimize the risk of undervoltage, bootstrap capacitors should be sized according to the I_{LOAD} < 0 case.

2.2.2 Bootstrap resistor

A resistor (R_{boot}) is placed in series with the bootstrap diode (see Figure 1) to limit the current when the bootstrap capacitor is initially charged. The choice of bootstrap resistor is strictly related to V_{BS} time constant. The minimum on-time for charging the bootstrap capacitor or for refreshing its charge must be verified against this time constant.

2.2.3 Bootstrap capacitor

For high T_{HON} designs where an electrolytic tank capacitor is used, its ESR must be considered. This parasitic resistance forms a voltage divider with R_{boot} generating a voltage step on V_{BS} during the first charge of the bootstrap capacitor. The voltage step and the related speed (dV_{BS}/dt) should be limited. As a general rule, ESR should meet the following constraint:

$$\frac{ESR}{ESR + R_{boot}} \cdot V_{CC} \leq 3\ V$$

Equation 10

A parallel combination of small ceramic and a large electrolytic capacitor is normally the best compromise. The the first acts as a fast-charge tank only for the gate charge and limits the dV_{BS}/dt by reducing the equivalent resistance, while the second keeps the V_{BS} voltage drop within the desired ΔV_{BS}.

2.2.4 Bootstrap diode

The diode must have a BV > DC+ and a fast recovery time (t_{rr} < 100 ns) to minimize the amount of charge fed back from the bootstrap capacitor to V_{CC} supply.

3 Gate resistances

The switching speed of the output transistor can be controlled by sizing the resistors controlling the turn-on and turn-off gate current properly. The following section provides some basic rules for sizing the resistors to obtain the desired switching time and speed by introducing the equivalent output resistance of the gate driver (RDRp and RDRn respectively of p and n channels). The examples always use an IGBT power transistor. Figure 2 shows the nomenclature used in the section. In addition, V_{ge}* indicates the plateau voltage, Q_{gc} indicates the gate-to-collector charge, and Q_{ge} indicates the gate-to-emitter charge.

3.1 Sizing the turn-on gate resistor

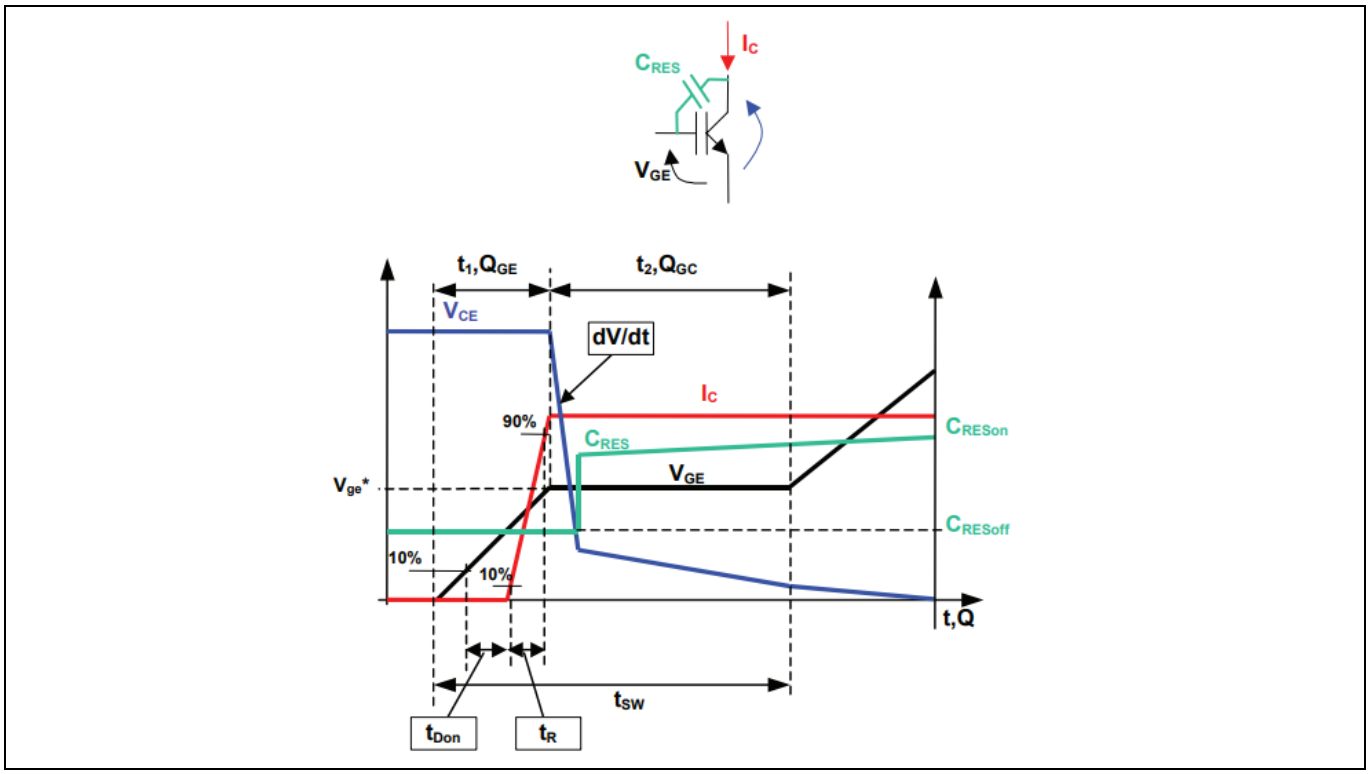


Figure 2 Nomenclature

The gate resitance can be chosen to fix either the switching time or the output voltage slope. Methods for both are presented in the next sections.

3.2 Switching time

In the calculations given in this section, the switching time, t_{sw}, is defined as the time spent to reach the end of the plateau voltage (the total Q_{gc} + Q_{ge} is provided to the IGBT gate). To obtain the desired switching time, the gate resistance can be sized starting from Q_{ge} and Q_{gc}, V_{cc}, V_{ge}* (see Figure 3):

$$I_{avg} = \frac{Q_{gc} + Q_{ge}}{t_{sw}}$$

Equation 11

And

Gate resistances

$$R_{TOT} = \frac{V_{CC} - V_{ge}^*}{I_{avg}}$$

Equation 12

Here, $R_{TOT} = R_{DRp} + R_{Gon}$, R_{Gon} = gate on-resistor and R_{DRp} = driver equivalent on-resistance (from the gate driver datasheet)

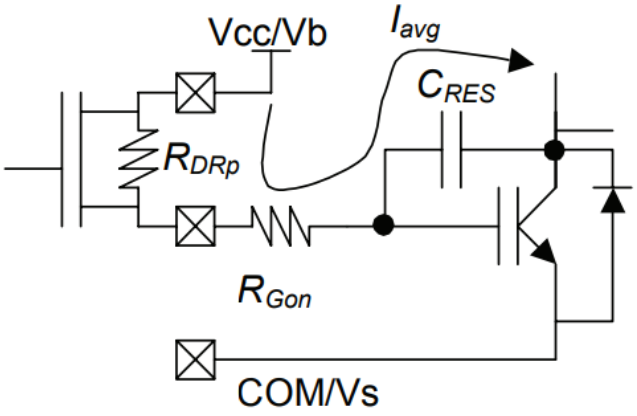


Figure 3 RG_{on} sizing

Table 1 lists the gate resistance size for two commonly used IGBTs (calculated using typical datasheet values and assuming V_{cc} = 15 V).

Table 1 t_{sw} driven R_{Gon} sizing (for RDRp = 7 Ω)

IGBT	Q_{ge}	Q_{gc}	V_{ge}*	t_{sw}	I_{avg}	R_{tot}	RG_{on} → standard commercial value	T_{sw}
IRGP30B120K(D)	19 nC	82 nC	9 V	400 ns	0.25 A	24 Ω	R_{TOT} - R_{DRp} = 17 Ω → 18 Ω	→ 420 ns
IRG4PH30K(D)	10 nC	20 nC	9 V	200 ns	0.15 A	40 Ω	R_{TOT} - R_{DRp} = 33 Ω	→ 200 ns

3.3 Output voltage slope

The turn-on gate resistor R_{Gon} can be sized to control the output slope (dV_{OUT}/dt).

While the output voltage has a non-linear behavior, the maximum output slope can be approximated by:

$$\frac{dV_{out}}{dt} = \frac{I_{avg}}{C_{RESoff}}$$

Equation 13

Inserting the expression yielding I_{avg} and rearranging:

Gate resistances

$$R_{TOT} = \frac{V_{CC} - V_{ge}^{*}}{C_{RESoff} \cdot \frac{dV_{out}}{dt}}$$

Equation 14

For example, Table 2 lists the sizing of gate resistance to get dV_{out}/dt = 5 V/ns when using two popular IGBTs, typical datasheet values, and assuming V_{cc} = 15 V.

Table 2 dV_{OUT}/dt driven R_{Gon} sizing (for R_{DRp} = 7 Ω)

IGBT	Q_{ge}	Q_{gc}	V_{ge}*	C_{RESoff}	R_{tot}	R_{Gon} → std commercial value	dV/dt
IRGP30B120K(D)	19 nC	82 nC	9 V	85 pF	14 Ω	RTOT - RDRp = 17 Ω → 8.2 Ω	→ 5 V/ns
IRG4PH30K(D)	10 nC	20 nC	9 V	14 pF	85 Ω	RTOT - RDRp = 78 Ω → 82 Ω	→ 5 V/ns

3.4 Sizing the turn-off gate resistor

The worst case scenario in sizing the turn-off resistor, R_{Goff}, is when the collector of the IGBT in off-state is forced to commutate by external events.

In this case, dV/dt of the output node induces a parasitic current through C_{RESoff} flowing in R_{Goff} and R_{DRn} (see Figure 4)[1].

If the voltage drop at the gate exceeds the threshold voltage of the IGBT, the device may turn on by itself, causing large oscillation and relevant cross conduction.

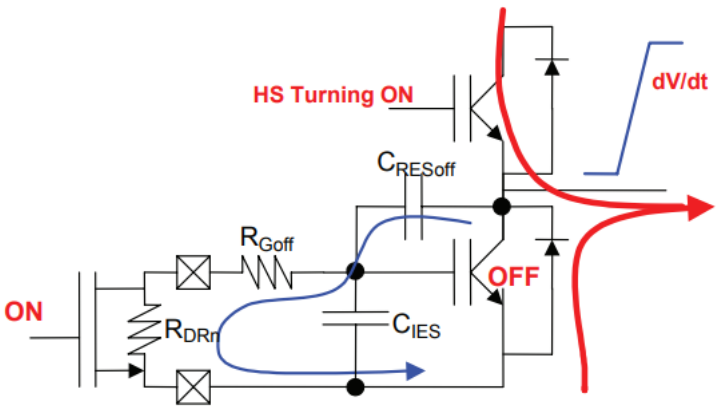


Figure 4 R_{Gon} sizing: Current path when the low side is off and the high side turns on

How to size the turn-off resistor when the output dV/dt is caused by the companion IGBT turning on (as shown in Figure 4) is described below.

Other dV/dt cases may be present and must be taken into account. For example, the dV/dt generated by long motor cable coupling (high frequency spikes).

Thereore, the off-resistance must be properly sized according to the application's worst case scenario.

The following equation relates the IGBT gate threshold voltage to the collector dV/dt:

Gate resistances

$$V_{th} = (R_{Goff} + R_{DRn}) \cdot I = (R_{Goff} + R_{DRn}) \cdot C_{RESoff} \frac{dV_{out}}{dt}$$

Equation 15

Rearranging the equation yields:

$$R_{Goff} \leq \frac{V_{th}}{C_{RESoff} \frac{dV_{out}}{dt}} - R_{DRn}$$

Equation 16

For example, Table 3 lists the R_{Goff} required by two popular IGBTs to withstand $dV_{out}/dt = 5$ V/ns.

Table 3 R_{Gon} sizing

IGBT	$V_{th(min)}$	C_{RESoff}	R_{Goff}
IRGP30B120K(D)	4	85 pF	$R_{Goff} \leq 4\ \Omega$
IRG4PH30K(D)	3	14 pF	$R_{Goff} \leq 35\ \Omega$

Note: The equations given above are an approximate way to size the gate resistances. More accurate sizing may take into account more precise device modeling and parasitic components that are dependent on the PCB and the power section layout and related connections.

Another way to size the gate resistors is by following the power dissipation constraints. This way is not discussed in this application note.

[1]This is true under the assumption that the gate voltage remains fixed during dV/dt. The result is reasonable whenever C_{IES} is at least two order of magnitude greater than C_{RES}.

4 Effects of parasitic elements

Figure 5 shows a single-phase, motor drive power stage and its driver. Some of the characteristics of the driver and the power stage will be analyzed in this chapter. To drive the power stage properly, it is very important to know the effects of inductive parasitic elements. In the normal operation mode, fast voltage variations, induced by a fast current change, may influence the performance of the gate driver.

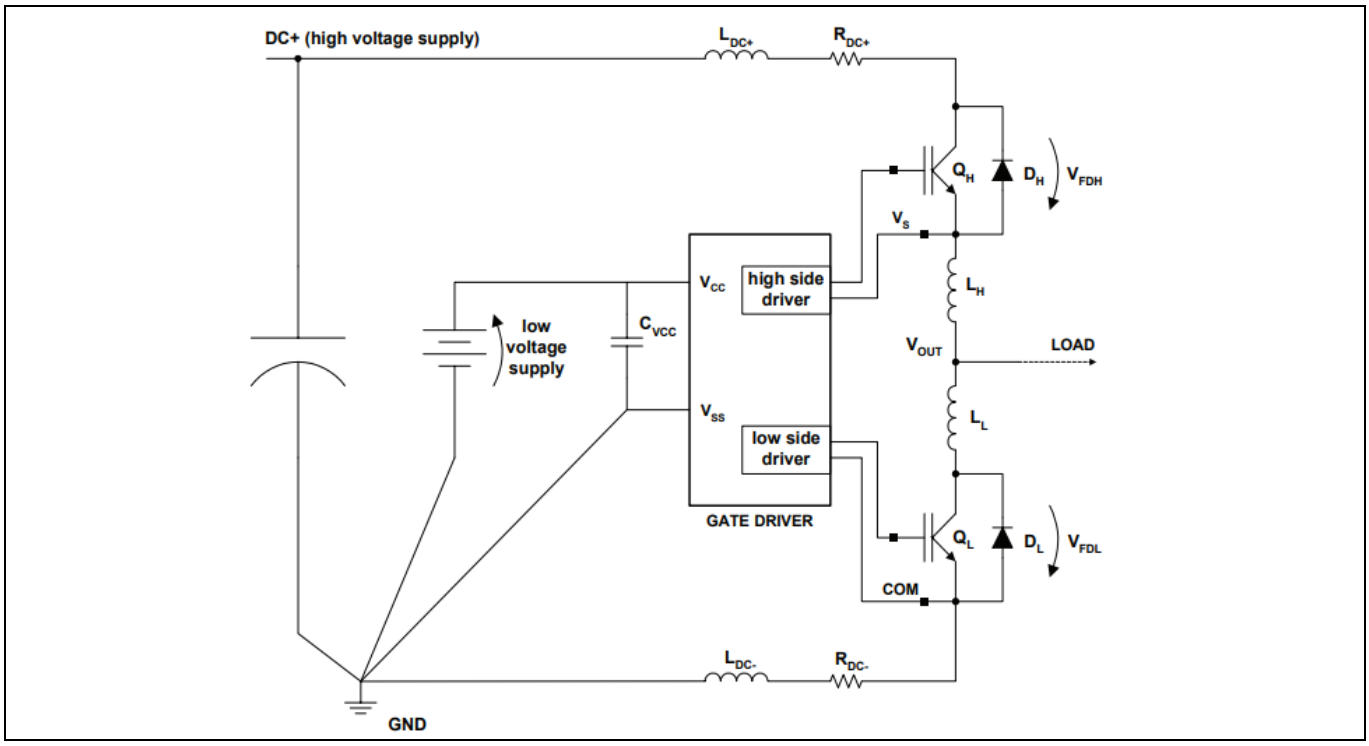


Figure 5 Parasitic elements in the power stage

In the presence of high and low-power signals, both referenced to the same ground, it is important to avoid ground loops on the board or ground planes close to the switching portions of the board. This solution reduces the noise coupled to the local ground of the driver. Moreover, making star connections between the ground pins and the board ground for all gate drivers (see Chapter 5, Layout tips) is suggested.

4.1 COM below ground (V_{ss}-COM)

The low-side IGBT is used for explaining the COM-below-V_{ss} event. Figure 6 shows one of the possible configurations of the parasitic elements in a half-bridge configuration. Here the emitter sense shunt is included for completeness.

Effects of parasitic elements

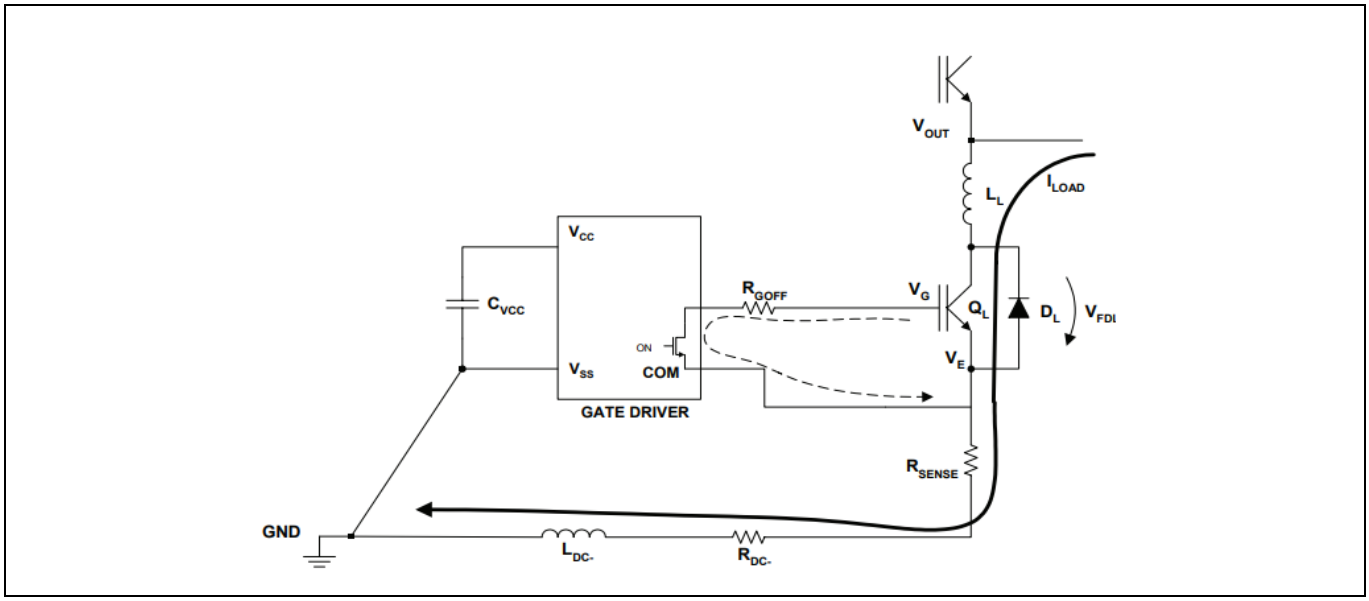


Figure 6 Parasitic elements during low-side turn-off

Consider turning off (dotted arrow) the low-side IGBT when the load current is flowing through it (bold arrow). As the power device turns off, the current flowing in the parasitic inductance (L_{DC-}) changes rapidly and the induced voltage pushes COM below ground.

The amount of voltage flyback is governed by the well-known law:

$$V_{L_{dc-}} = L_{DC-} \cdot \frac{dI_{L_{dc-}}}{dt}$$

Equation 17

This equation relates the COM undershoot (strictly dependent on inductance voltage) to the slope of the load current. Therefore, the first solution is to turn the IGBT off more softly, by increasing the low-side turn-off resistor (respecting the higher limit, see the section “Sizing the turn-off gate resistor”), to limit the dI_L/dt.

However, this solution may not be sufficient in the presence of a phase-DC+ short circuit.

This type of short circuit usually breaks when the low-side IGBT turns off. Short circuit detection may react when the current exceeds the rated current for normal operation by several times, inducing faster current change at turn-off.

In that case, the solution shown in Figure 7 prevents the COM pin from following the IGBT emitter filtering the under-Vss spike.

Effects of parasitic elements

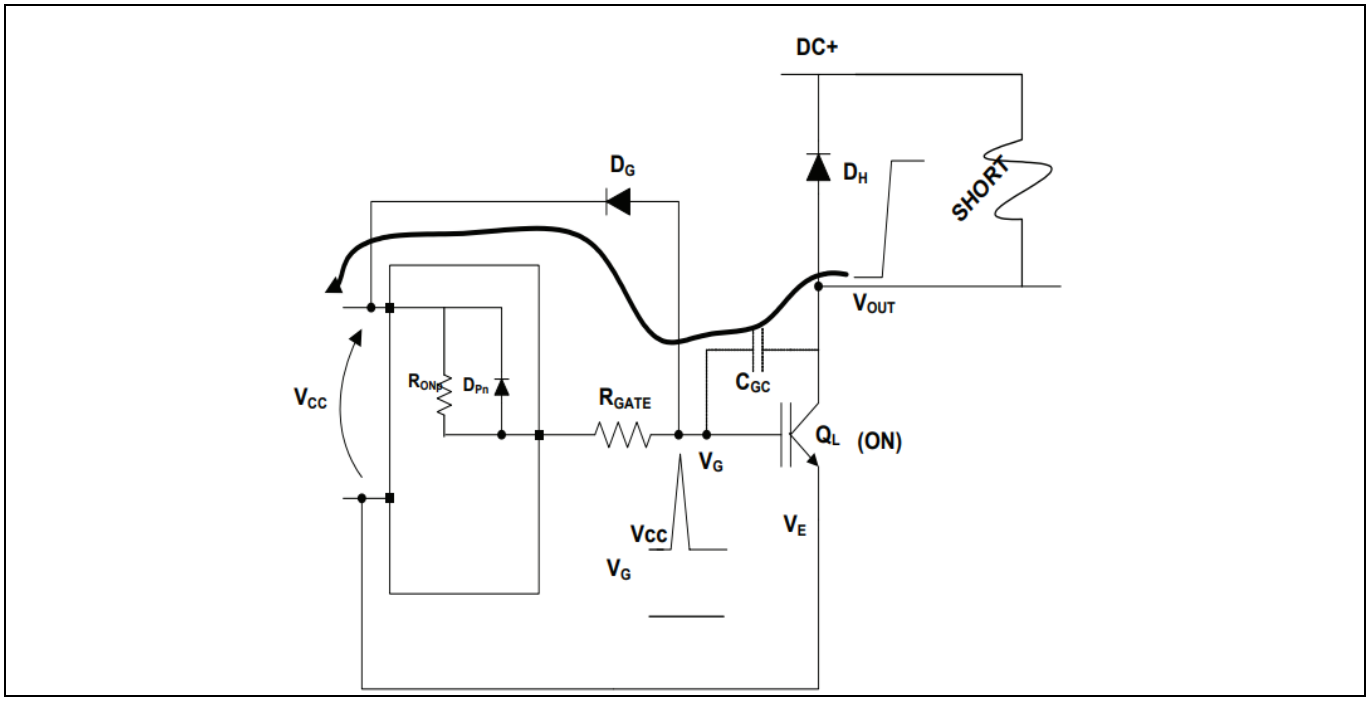


Figure 7 Driver output protection in case of IGBT desaturation

- R_{COM} should be taken into account when sizing the turn-off resistance (that becomes $R_{GOFF} + R_{COM}$)
- R_{COM} and C_{COM} sizing establishes the time constant of the COM pin that can be set to some hundred of nanoseconds
- To avoid noise coupling to V_{CC}, size as per the rule $\frac{C_{COM}}{C_{VCC}} \ll 1$ as required by the application

Note: IGBT short circuit desaturation easily generates high collector dV/dt. IGBT gate is pulled above the local supply by the gate-collector stray capacitance.

In some cases (usually when the turn-on resistor is low), a fast diode is required between the IGBT gate and the local supply to protect the driver output (see Figure 8). As an alternative solution; a Zener clamp can be placed between the IGBT gate and the emitter. It should be sized accordingly to the IGBT gate-emitter absolute maximum ratings.

The advantage of the Zener clamp is that it protects the driver output (by sinking the current generated by the collector dV/dt) and keeps the IGBT gate-emitter voltage under control.

This is particularly important when the IGBT turns off after a short-circuit is detected and the IGBT emitter spikes under VSS due to the DC- stray inductance (L_{DC-}, see Figure 9).

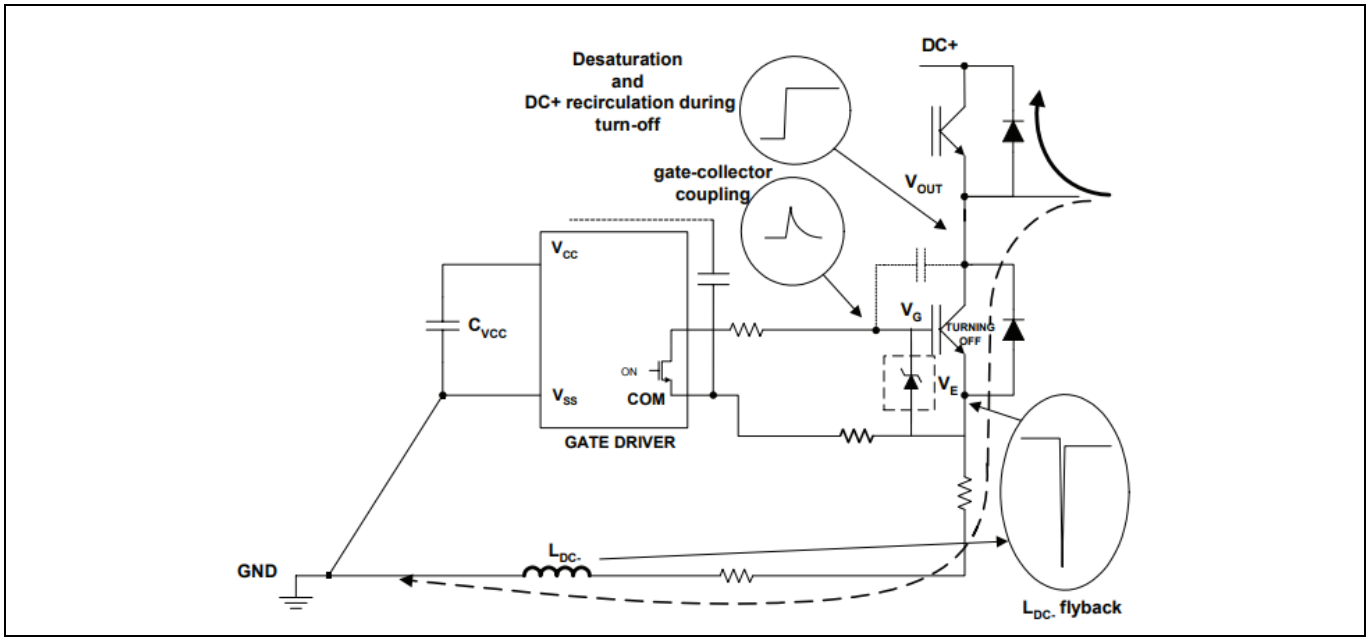


Figure 8 Zener protection for the IGBT gate emitter

4.2 V_S below ground (V_S-COM/V_{SS})

A well-known event that triggers V_S to go below V_{ss} or COM is the forward biasing of the low-side freewheeling diode. This usually happens when current flows out of the half-bridge towards the load.

In the steady state, V_s is clamped below V_{ss} to about:

$$V_S^{steady} - V_{SS} = -V_{FDL} - (R_{SENSE} + R_{DC-}) \cdot I_{LOAD}$$

Equation 18

And below COM:

$$V_S^{steady} - COM = -V_{FDL}$$

Equation 19

Here, I_{LOAD} is positive, flowing towards the load.

The maximum voltage difference between V_s and V_{ss} or COM can be found in the datasheet containing absolute maximum ratings for V_S and recommended operating conditions.

Major issues may appear during commutation, just before the freewheeling diode starts clamping.

In this case, the inductive parasitic elements shown in Figure 10 (L_{dc-}, L_L, and L_H) may act by pushing down V_s below V_{ss}, even lower than the value mentioned earlier for the steady state condition.

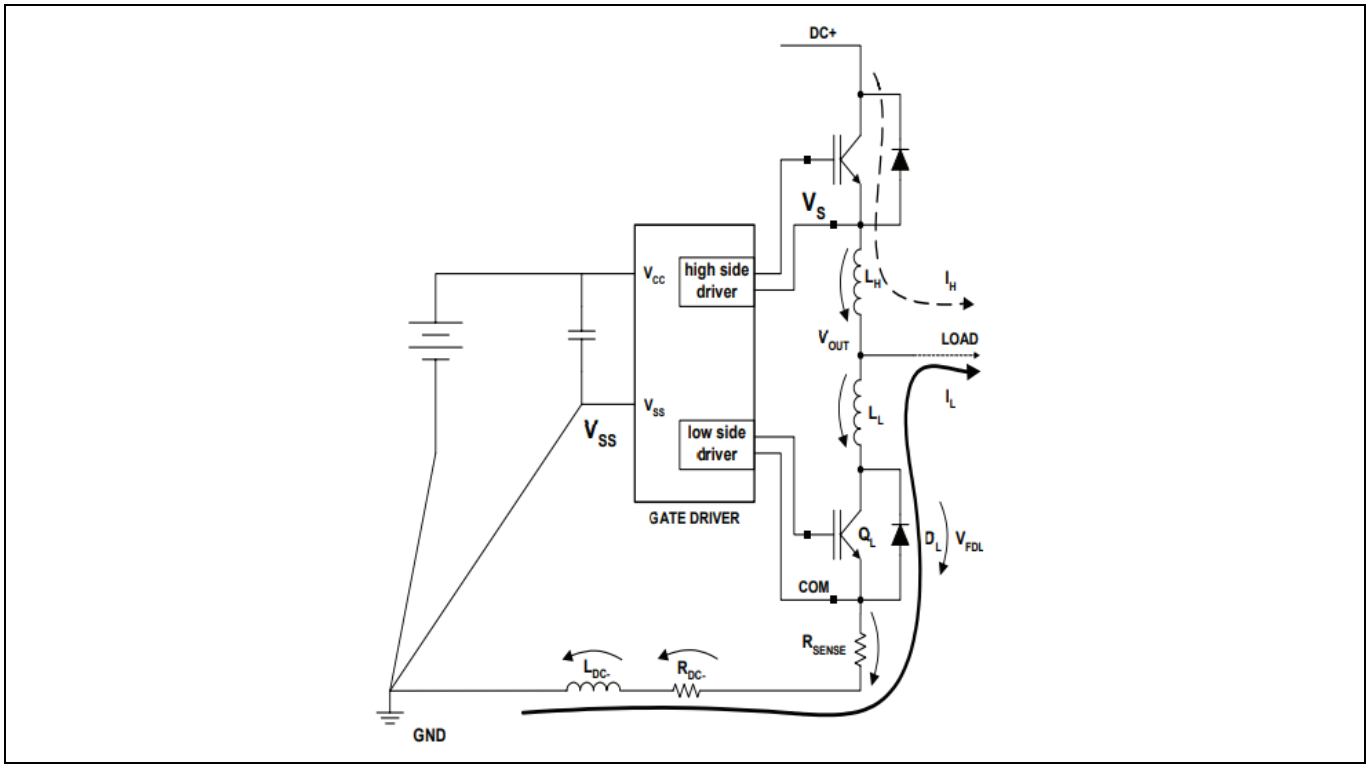


Figure 9 Elements causing V_s to go under V_{ss}

The derivative terms of the following equation may be the highest contributors to negative Vs effect during the commutation transient:

For V_{ss}:

$$V_S^{tran} - V_{SS} = -V_{FDL} - (R_{SENSE} + R_{DC-}) \cdot I_L - (L_{DC-} + L_L) \cdot \frac{dI_L}{dt} - L_H \cdot \frac{dI_H}{dt}$$

Equation 20

For COM:

$$V_S^{tran} - COM = -V_{FDL} - L_L \cdot \frac{dI_L}{dt} - L_H \cdot \frac{dI_H}{dt}$$

Equation 21

To reduce the slope of the current flowing in the parasitic inductances so to minimize the derivative terms, R_{GOFF} can be increased, respecting previously discussed constraints (see the section on R_{GOFF} sizing).

4.3 Resistor between V_s and V_{out}

While the above mentioned solution may work in normal operating conditions, it can be insufficient, for example, when a short circuit occurs between the phase and ground while the high-side IGBT is on. After the high-side IGBT is turned off, the high amount of current that was flowing through it starts flowing through the low-side freewheeling diode.

Effects of parasitic elements

The high $\frac{dI}{dt}$ may even pull VB (the floating stage supply) below ground by means of the bootstrap capacitor. This happens when:

$$V_S^{tran} - V_{SS} < -V_{CC}$$

Equation 22

Note that only high frequency events are being considered here, so that the bootstrap diode may reasonably stay turned off.

The real damage to monolithic ICs is caused by the amount of current stolen from the VB pin (via C_{boot} coupling with VS). To minimize this current a resistor (R_{VS}) can be placed between V_S and V_{out}, as shown in Figure 11.

Suggested values for R_{VS} are in the range of some ohms.

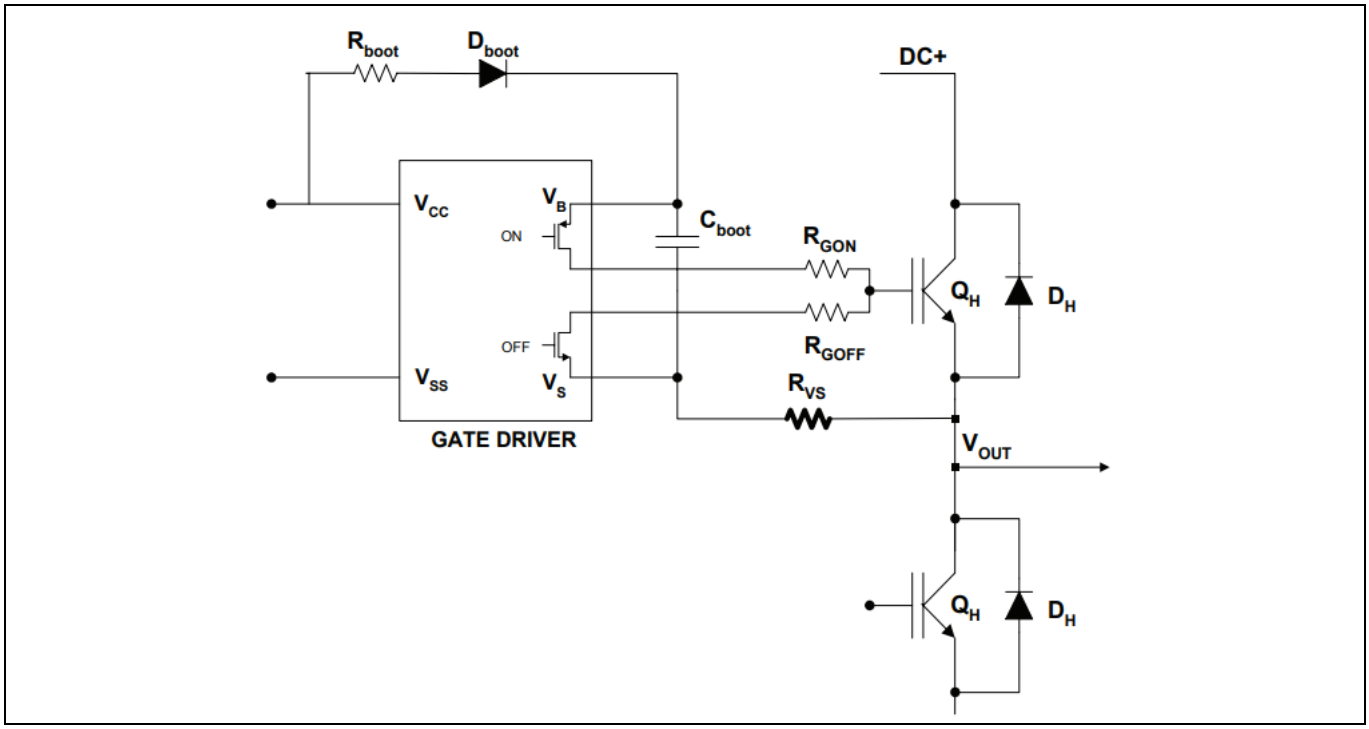


Figure 10 R_{VS} connection

NOTES:

- R_{VS} works in series with the bootstrap resistor and must be considered when sizing the bootstrap resistance (R_{BOOT}*= R_{BOOT} + R_{VS})
- It is also important to notice that the current developed across R_{VS} during initial bootstrap charge may be such that a relevant voltage is developed between the high-side IGBT emitter and the VS pin. This voltage may be brought to the high-side output (HO) through the HO-VS ESD protection diode. In this case, verify that the IGBT gate does not turn on at the bootstrap startup (the gate resistor and gate-emitter capacitance help to filter out this pulse). This may cause a short shoot-through at inverter output
- R_{VS} is also included in turn-on (R_{GON} + R_{VS}) and turn-off resistor sizing (R_{GOFF} + R_{VS}) as shown in Figure 12

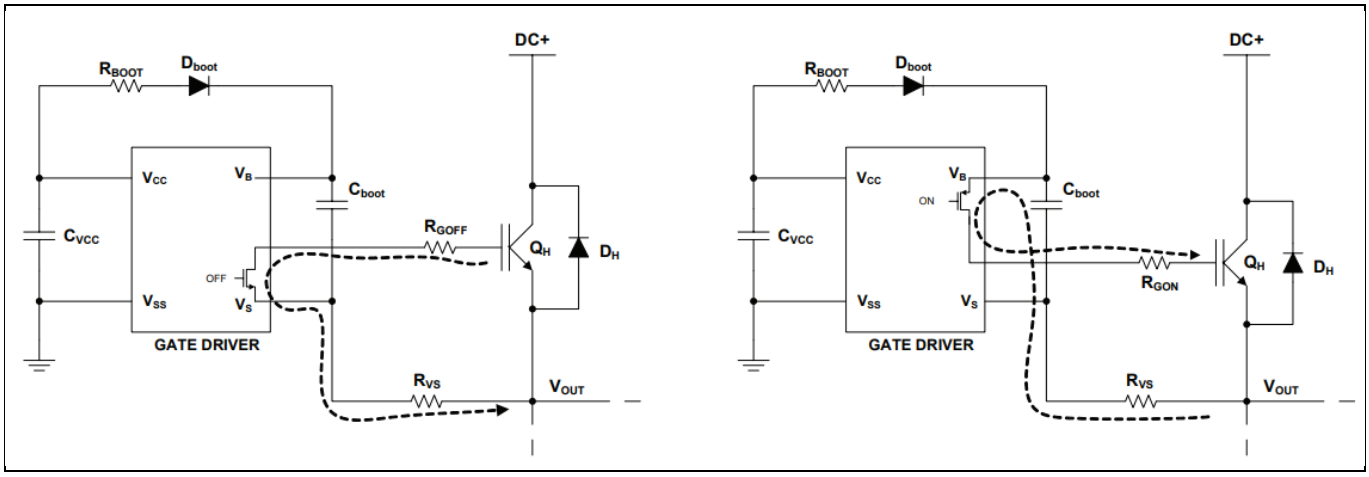


Figure 11 Gate turn-on and turn-off with R_{VS}

4.4 Clamping diode for V_S

In the previous section, it was assumed that D_{BOOT} stays switched off considering the events at high frequency.

Whenever this assumption is not verified, while V_S follows V_{OUT}, V_B can be tied to V_{CC} by the bootstrap diode. In this case, the difference between V_B and V_S should be kept within the absolute maximum specification given in the IC's datasheet:

$$V_B - V_S < -V_{VBS\_abs\ max}$$

Equation 23

To keep within the specifications, a clamp device should be positioned between V_{SS} and V_S, as shown in Figure 13 where a Zener diode and a 600 V diode are placed.

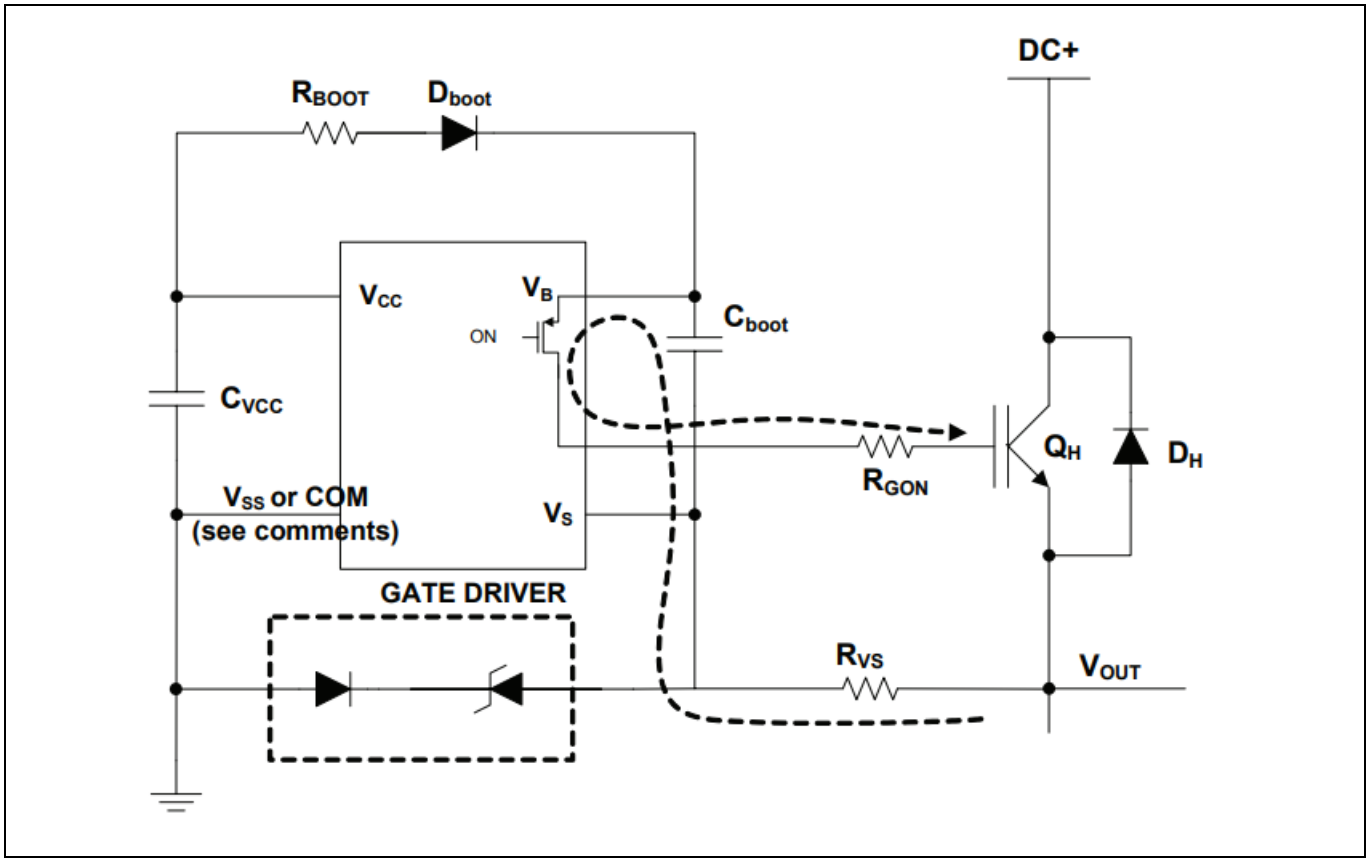


Figure 12 Clamping structure with a Zener diode

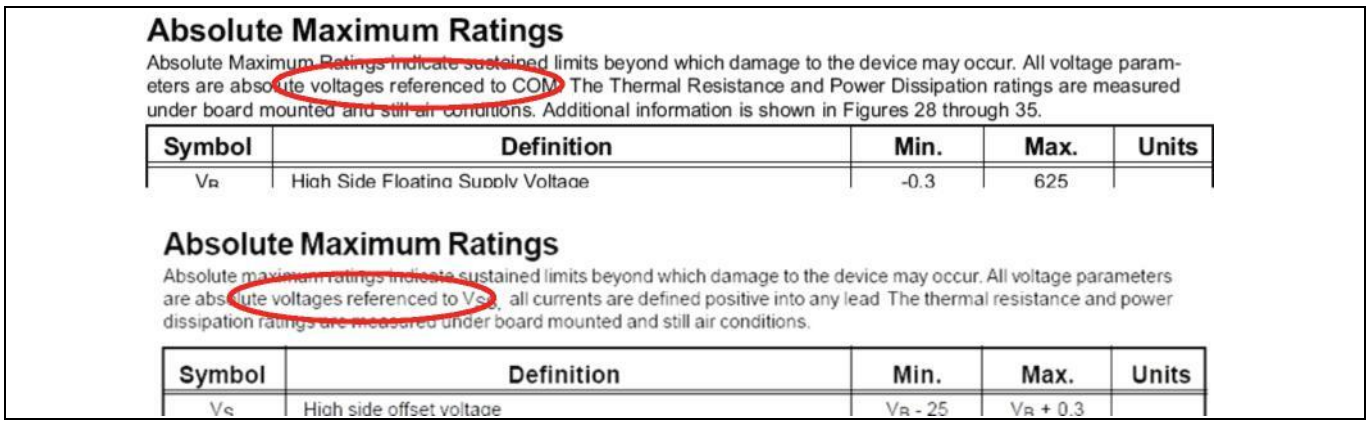
The Zener voltage must be sized as per the following equation:

$$V_Z \leq -V_{VBS\_abs\,max} - V_{CC}$$

Equation 24

In most of the cases, using a Zener diode is not necessary and only an high voltage (HV) diode is used.

The clamp must be connected to the COM pin (and in some cases to the Vss pin) according to the device datasheet. This information is usually available in the section on absolute maximum ratings.



Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions. Additional information is shown in Figures 28 through 35.

Symbol	Definition	Min.	Max.	Units
VB	High Side Floating Supply Voltage	-0.3	625	

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to VSS, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
VS	High side offset voltage	VB - 25	VB + 0.3	

Figure 13

5 Tips for PCB layout

5.1 The distance from high voltage to low voltage

To minimize the noise coupled between the signals referred to the ground and those floating, placing the components tied to the floating voltage on the high- voltage side of the device (V_B, V_S side) is strongly recommended, while the other components are on the opposite side.

5.2 Ground plane

The ground plane must not be placed under or near the high-voltage floating side to minimize noise coupling.

5.3 Supply capacitors

If the output stages are able to turn on the IGBT quickly with a large amount of current, the supply capacitors must be placed as close as possible to the device pins (V_{CC} and V_{SS} for the ground-tied supply, V_B and V_S for the floating supply) to minimize parasitic inductance/resistance.

5.4 Gate drive loops

Current loops behave like an antenna and are able to receive and transmit EM noise. To reduce EM coupling and improve the power switch turn-on/off performances, gate drive loops must be reduced as much as possible. Figure 14 shows the high-side and low-side gate loops.

Moreover, current can be injected inside the gate drive loop via the IGBT collector-to-gate parasitic capacitance. The parasitic auto-inductance of the gate loop contributes in developing a voltage across the gate emitter, increasing the possibility of a self-turn-on effect. Therefore, placing the gate resistances close together is strongly recommended to minimize the loop area (see Figure 14).

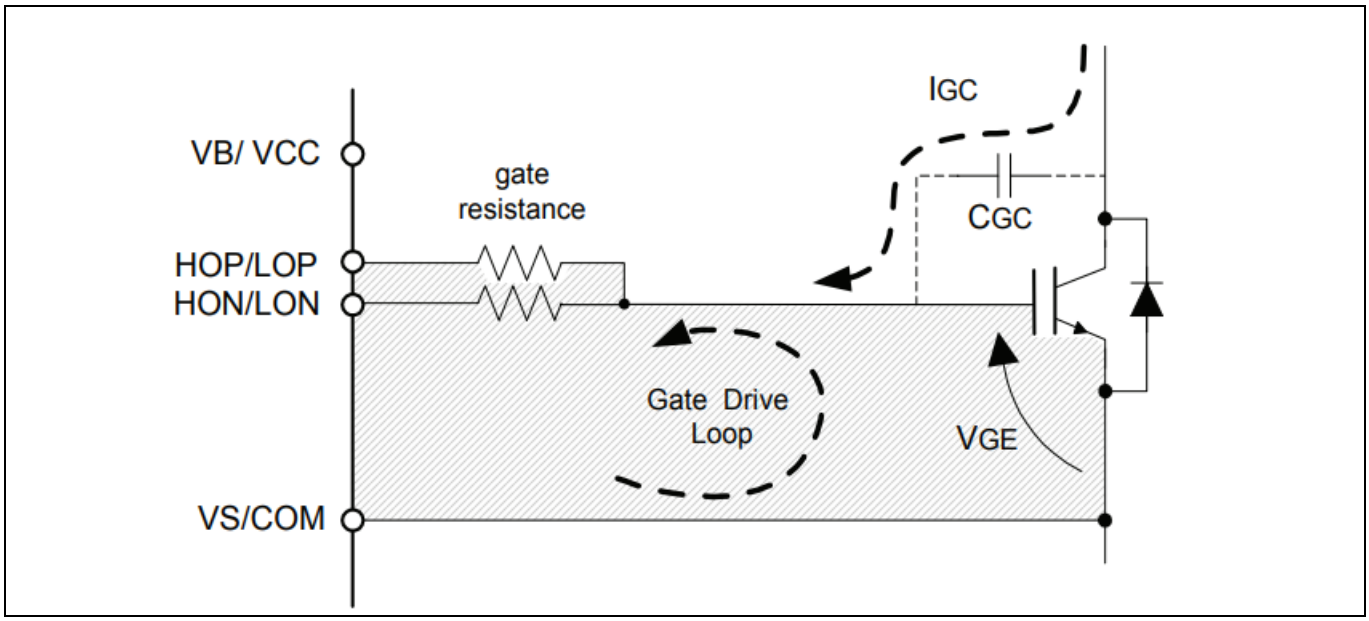


Figure 14 The gate drive loop

5.5 Example of routing and placement

Figure 15 shows the lead assignments for IR2214SS – a high voltage and high output current gate driver.

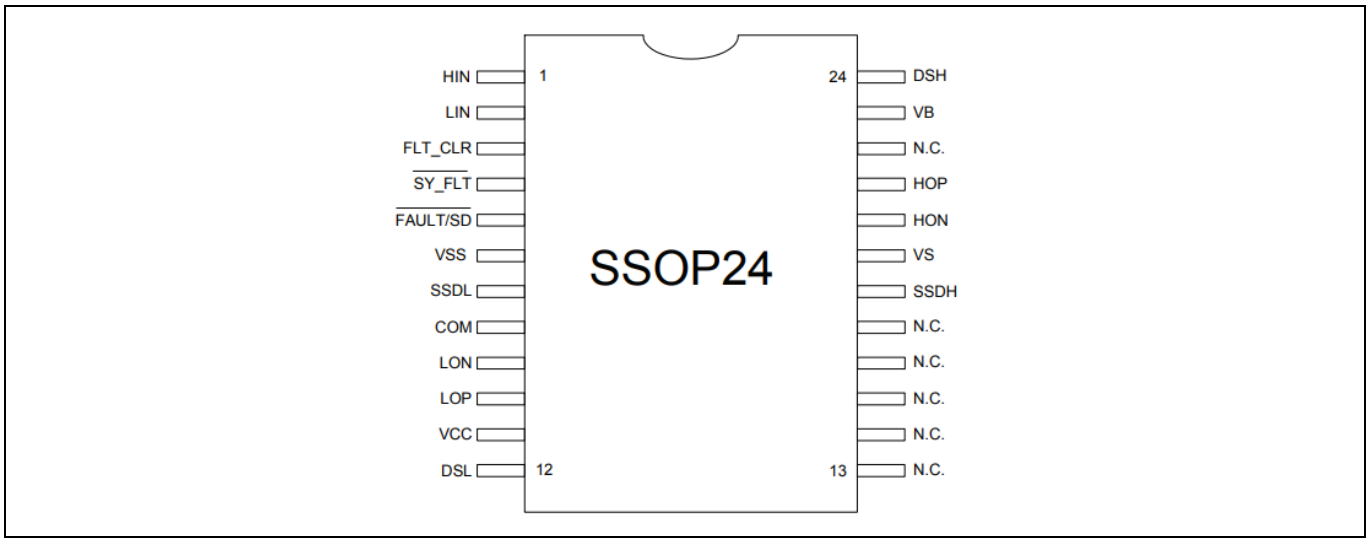
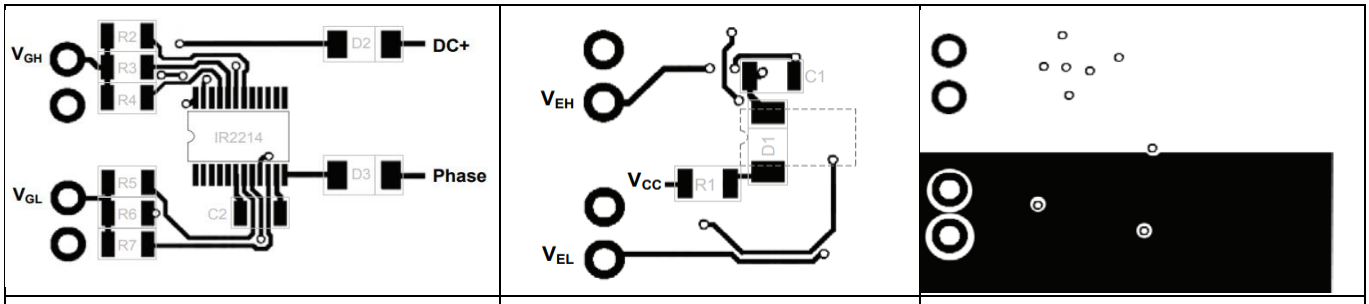


Figure 15 Lead assignments for IR2214SS

Figure 16 shows one of the possible layout solutions using a 3-layer PCB. This example includes all the previous considerations. The placement and routing of supply capacitors and gate resistances in the high and low-voltage sides minimizes the supply path and gate drive loop, respectively. The bootstrap diode is placed under the device to keep the cathode as close as possible to the bootstrap capacitor, and to keep the anode as far as possible from high voltage and close to V_{CC}.



(a) TOP	(b) BOTTOM	(c) Ground plane

Figure 16

Labels in Figure 16:

- Bootstrap section: R1, C1, D1
- High-side gate: R2, R3, R4
- High-side Desat: D2
- Low-side supply: C2
- Low-side gate: R5, R6, R7
- Low-side Desat: D3

References

[1] Datasheeet of IR2214SS: https://www.infineon.com/cms/en/product/power/gate-driver-ics/ir2214ss/

[2] Datasheet of IRGP30B120KD: https://www.infineon.com/dgdl/irgp30b120kd-epbf.pdf?fileId=5546d462533600a401535655acdb2440

[3] Datasheet of IRG4PH30K(D): https://www.infineon.com/dgdl/irg4ph30kpbf.pdf?fileId=5546d462533600a4015356481b11230f

[4] Gate driver reference page: https://www.infineon.com/cms/en/product/power/gate-driver-ics/

Revision history

Document revision	Date	Description of changes
Revision 1.00		Initial version
Revision 1.01	2024-11-20	Document template change and grammar review

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