Using HEXFET III in PWM Inverters for Motor Drives and UPS Systems

(HEXFET is a registered trademark of International Rectifier)

by D. Grant

Introduction

The advantages of MOSFETs for high frequency pulse-width modulated (PWM) inverters and choppers for variable speed motor drives, uninterruptible power supplies (UPS) and similar applications, covering power outputs to tens of kilowatts, include the ability to operate at frequencies above the audible range, low output distortion, high overload capability, fast response, and simple drive circuitry.

It has only been recently, however, that MOSFETs are becoming generally popular in these applications. MOSFETs were not previously always the automatic device of choice, because they had to supplant bipolar transistors which were already well entrenched. Often there was not sufficient incentive to change to MOSFETs, which were still descending the price learning curve. Also the MOSFET's internal body-diode, while superficially offering itself as a needed circuit component, in reality caused circuit difficulties, which often could be solved only by using additional discrete diodes, adding circuit complexity and cost.

In cases where designers did manage to use the MOSFET's internal body diode, they had to establish the allowable limits of operation by painful experience, without any firm guarantee from the manufacturer that the devices were being operated within their capabilities.

The introduction of International Rectifiers HEXFET III generation power MOSFETs eliminates the previous barriers to the use of MOSFETs in PWM motor drives and similar applications. HEXFET America's high volume in-line manufacturing facility now makes HEXFETs decidedly cost-competitive. And HEXFET III incorporates several major design improvements. Its body diode is far more rugged than that of previous power MOSFETs, and can be used without fear of failure.

This means that a three-phase bridge inverter can be constructed using just six HEXFETs, without the need for external diodes or snubbers. The HEXFET III diode rating allows the designer to exploit the presence of the integral diode with confidence, thereby greatly simplifying the design and minimizing overall system cost.

The PWM Inverter

The technique of pulse-width modulation, by which an inverter operating from a fixed-voltage dc supply can generate an ac output voltage of variable frequency and voltage, is well known. Figure 1 shows the basic power circuit for operation from a single-phase ac supply. The load is switched alternately between the positive and negative rails of the dc supply. By appropriate control of the switching instants of the power devices, an output voltage waveform can be produced whose fundamental is of the required frequency and amplitude (Figure 2). The details of PWM waveform generation are discussed in Appendix 1.

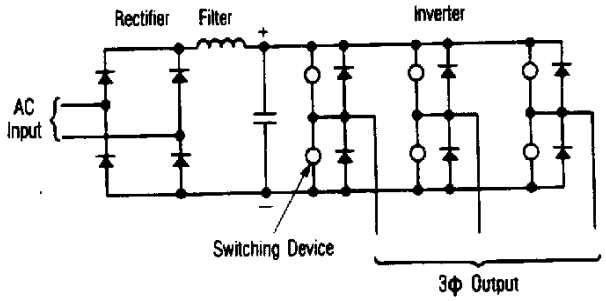


Figure 1. Inverter circuit

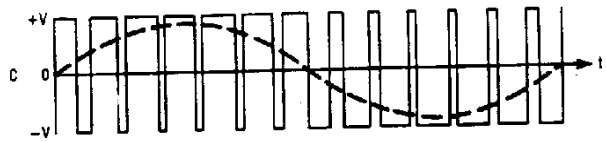


Figure 2. Pulse-width modulated waveform (line to neutral).

Power MOSFET switching speeds permit the use of a switching frequency outside of the audible frequency range. Since in a typical application the switching frequency is a least an order of magnitude higher than the output frequency, output filtering is a practical proposition. This makes variable-frequency ac supplies possible that are virtually free of harmonics and RFI problems. Audible acoustic noise is also eliminated, making such systems acceptable for use in home and office. Applications include variable frequency ac motor drives and uninterruptible power supplies.

The Need For An Inverse Diode

Figure 1 shows a diode connected in inverse parallel across each switching device. These diodes are variously referred to as "feedback," "reactive," "reactive feedback," "freewheeling," "clamp," or even "protection" diodes. Whatever they're called, their presence is fundamentally necessary to the circuit operation.

The load connected to the output of each phase of the inverter will generally be either the filter inductor or an inductive load, such as one phase of the stator winding of a motor. Due to the wide separation of the switching frequency and the output frequency, the load will appear highly inductive relative to the switching frequency and, therefore, the load current will be approximately constant and continuous within each switching cycle. That means that during a switching cycle within each "leg" (or "pole") of the bridge the load current commutates between one of the switching devices and one of the freewheeling diodes.

If the switching devices are HEXFETs, the integral body-drain diode contained within the HEXFET structure may be used as the freewheeling diode. Therefore, only six HEXFETs are required to form a complete three-phase bridge, as Figure 3 shows.

The output current and voltage waveforms for one leg of such an inverter at various points during the output cycle are shown in Figure 4. When load current is flowing out of the center point of the bridge the top HEXFET and bottom diode conduct alternately. When load current is flowing into the center point, the bottom HEXFET and top diode conduct.

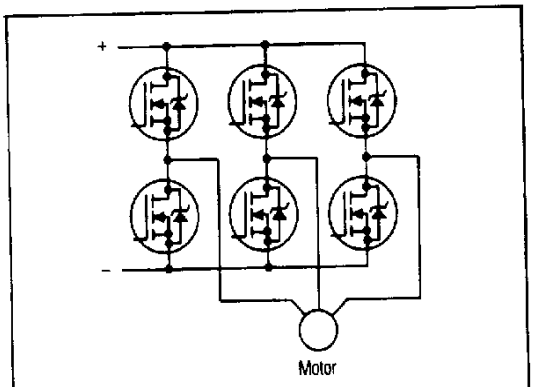


Figure 3. A three-phase inverter using HEXFETS

Problem With Using The Body-Drain Diode

Whichever direction the load current is flowing, each switching cycle sees the commutation of the load current from the body-drain diode of one HEXFET to the channel of the other. This occurs when the previously non-conducting HEXFET turns on and results in a pulse of diode recovery current flowing between the rails of the dc power supply. The magnitude of the "short-circuit" current is limited by parasitic circuit inductance and by the transconductance of the HEXFET. Figure 5 shows the waveforms associated with turn-on of one of the HEXFETs in a bridge inverter.

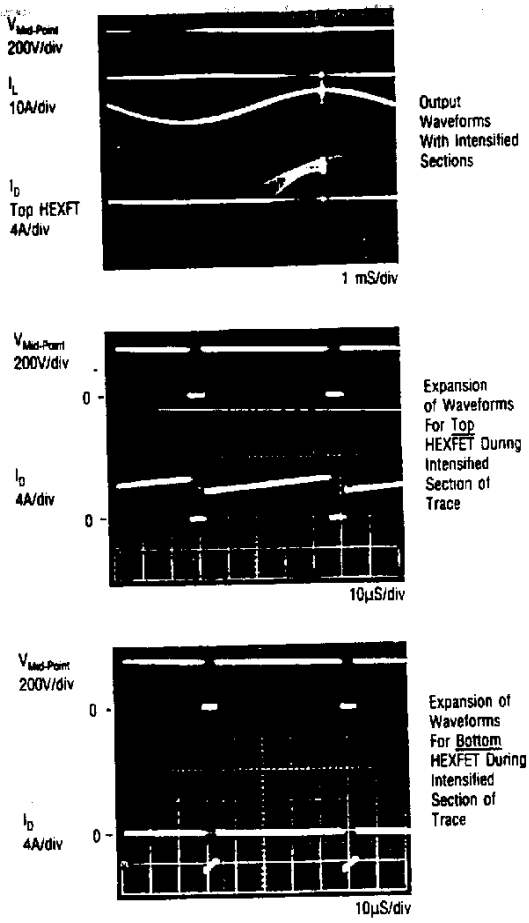


Figure 4a. Current in top and bottom HEXFETS during positive load current

The waveforms shown in Figure 5 were obtained by controlling the gate voltage so that the drain current, composed of the load current plus the diode recovery current, reached the maximum allowable value of drain current I_{DM}, thereby allowing commutation to take place in the shortest possible time. By this means the total commutation losses are minimized. However it is possible to reduce the magnitude of the diode-recovery current to practically any value desired by slowing down the turn-on of the HEXFET. Commutation losses are not reduced until switching is slowed to a point where the delay time and switching time might compromise the quality of the PWM waveform. Although the diode-recovery current pulse appears large in amplitude, it is brief in duration and even with a switching frequency of 20 kHz, the losses produced by the diode-recovery current are acceptable. This is demonstrated later.

The diode recovery current has two main consequences. Firstly, it causes losses in the MOSFETs. More seriously, it tends to initiate conduction of the internal parasitic bipolar transistor contained within the structure of every power MOSFET. The consequence of the parasitic bipolar transistor turning on is that the cell loses its blocking capability, current crowds into that cell and the device is destroyed. It is therefore essential that for inverter applications, power MOSFETs should be used that are immune to this phenomenon.

Diode-Recovery dv/dt

Figure 6 demonstrates the presence of a parasitic bipolar transistor within the double-diffused power MOSFET structure. This parasitic transistor is muted by the shorting of its

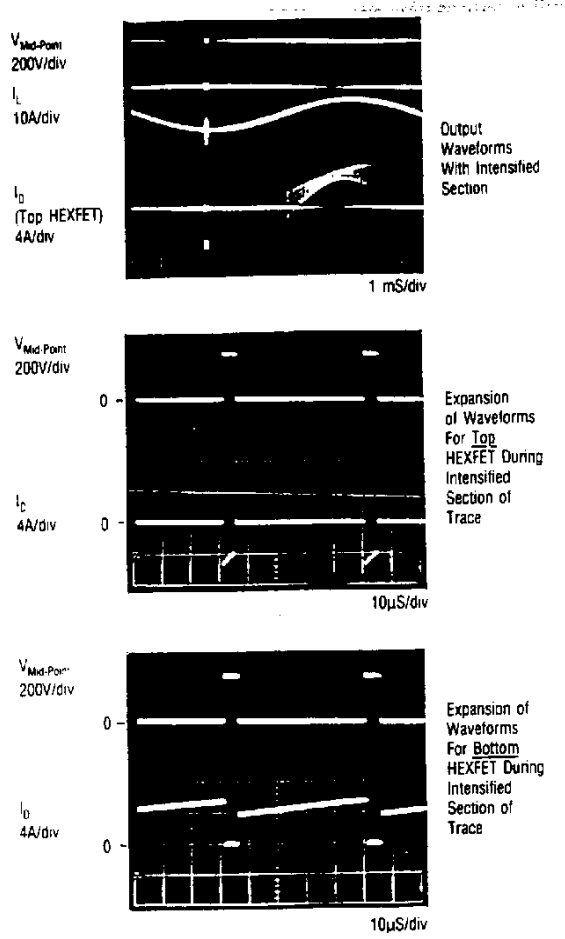


Figure 4b. Current in top and bottom HEXFETs during negative load current

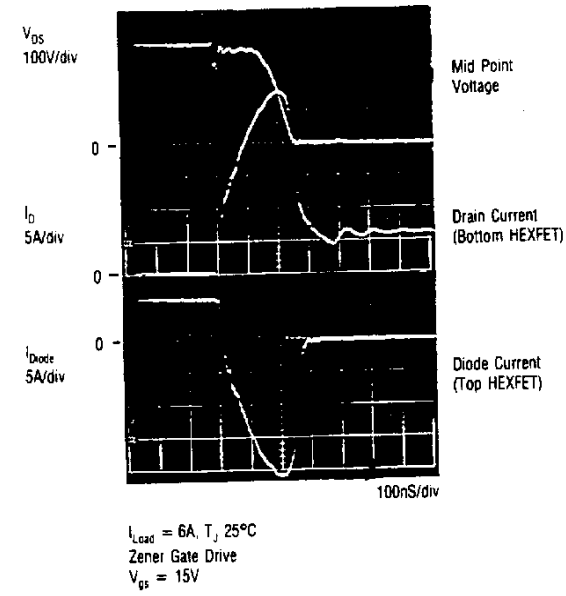


Figure 5. Turn-on current waveforms for inverter consisting of two IRF840 HEXFETS

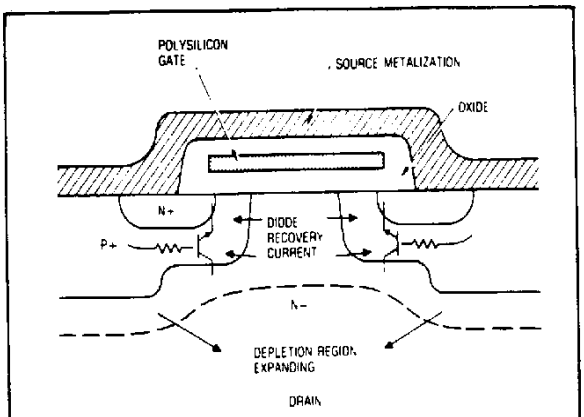


Figure 6. The parasitic bipolar transistor and diode recovery currents in a DMOS power MOSFET

base and emitter regions through the source metalization. However, it is possible for the base emitter junction to become forward biased if a significant amount of current flows laterally through the P-body region. One way of creating this lateral current flow is by avalanche breakdown. The HEXFET III range of devices have been designed to tolerate high levels of avalanche current without activation of the parasitic bipolar transistor [Ref 1].

A second way in which lateral current flow can be generated in the P-body region is by rapid recovery of the body-drain diode after carrying current. Figure 6 illustrates this effect. The drain drift region of the device is saturated with minority carriers as a result of diode conduction. During recovery of the diode a depletion region is formed between the P-body region and the N-type drift region. This sweeps out the remaining carriers as it expands into the drift region. Without proper device design this sweep-out current can be exceptionally large in certain cells of the power MOSFET, thereby causing the parasitic bipolar transistor to conduct with catastrophic consequences.

The critical moment for the device comes as the diode is recovering and the MOSFET (and its internal parasitic bipolar transistor) is called upon to block forward voltage. The more rapid the rise of drain voltage, the more likely is activation of the parasitic bipolar transistor.

The designer of bridge inverters who wishes to make use of the integral diode of a power MOSFET, therefore, needs assurance that the device will not fail under these conditions. The HEXFET III generation of power MOSFETs are rated for dv/dt. The rating is called the diode-recovery dv/dt rating, since it describes the HEXFET's ability to withstand dv/dt during diode recovery. A dv/dt capability of at least 3 V/nS is required in a typical PWM inverter operating from a rectified 220 V ac supply. All HEXFET III devices are rated above this value. A full description of the new ratings can be found in Reference 1.

HEXFET III dv/dt ratings are generally adequate to encompass values of dv/dt found in typical inverter applications. Therefore, when using HEXFET III devices it is unnecessary to slow down switching of the HEXFETs in order to limit dv/dt, although the switching speed may need to be adjusted for other reasons such as maintaining the diode recovery current within the I_{DM} rating and limiting RFI.

Avalanche

As Figure 3 illustrates, the HEXFET symbol employs a zener or avalanche diode symbol to represent the integral body-drain diode. This reflects the enhanced avalanche capabilities of the HEXFET III generation of power MOSFETs, which

are rated for both high-energy non-repetitive avalanche breakdown as well as repetitive avalanching. This avalanche capability adds to the suitability of the HEXFET for inverter applications. As well as being able to tolerate voltage spikes produced by such events as sudden load connection and disconnection and contactor operation, HEXFETs can tolerate overvoltage transients produced during normal operation. For example, if a large amount of parasitic inductance is included in the mid-point of the inverter, as shown in Figure 7, energy will be stored in this inductance during diode recovery. As the waveforms in Figure 8 demonstrate, this energy results in avalanche operation of the HEXFET. The device used in Figure 8 is experiencing first diode-recovery dv/dt (actually well above the rated level) followed immediately by avalanche operation.

An important benefit of the avalanche capability of HEXFET III devices is that since they can tolerate avalanche operation, traditional safety margins which are applied when selecting the voltage rating can be relaxed. This is particularly beneficial in the case of power MOSFETs since their $R_{DS(ON)}$ increases rapidly with voltage rating.

Diode Recovery Losses

At the beginning of every switching cycle the load current is circulating through the body-drain diode of one HEXFET prior to the turn-on of the other HEXFET. Before the diode can sustain a reverse voltage a quantity of charge must be extracted. Further charge is extracted as the voltage of the center point of the bridge swings between power rails with a corresponding rise in the reverse voltage of the diode. The total charge associated with diode recovery flows between the rails of the dc supply without doing useful work. The diode recovery current therefore constitutes a loss of energy which appears as heat in the HEXFETs. (The commutation process is illustrated in Figure 5).

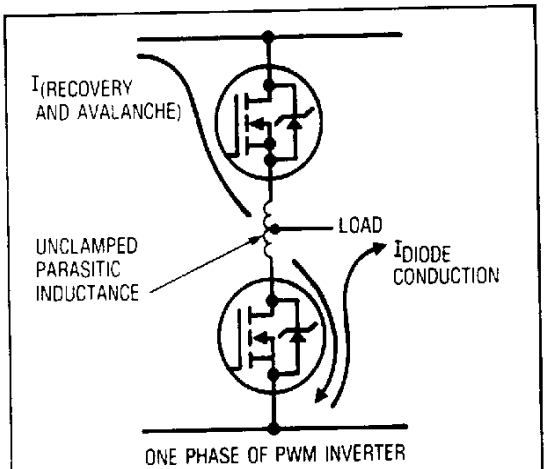


Figure 7. Unclamped parasitic inductance in a bridge circuit

Figure 9 shows the voltage and current waveforms during turn-on of one of the HEXFETs in a bridge composed of a pair of IRF840 HEXFETs, for various values of load current.

Figure 10 illustrates the effect of switching speed on the diode reverse recovery current. The switching speed is determined by the value of the series gate resistor. The diode recovery charge, Q_{RR}, falls as the recovery time is extended due to increased minority carrier recombination.

For very low values of series gate resistance a large dip occurs in the dc supply rail voltage due to the parasitic inductance of the reservoir capacitors and the system wiring. While this may not be too detrimental to waveform quality, it is likely to contribute to the level of RFI generated by the circuit. The gate voltage used in Figure 10 was set by a level which would cause the peak drain current to be limited by transconductance, below the I_{DM} rating of the device.

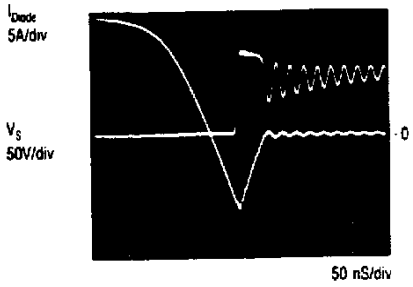
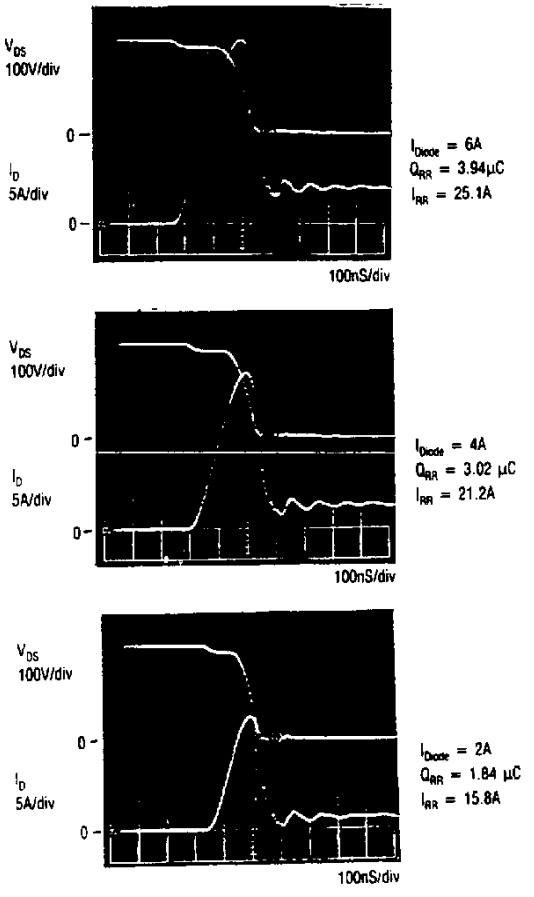


Figure 8. An IRF530 subject to diode recovery dv/dt and avalanche



T_J = 25°C, V_{GS} = 15V, R_G = 220Ω

Figure 9. Variation of recovery current with load current (IRF840)

The diode recovery charge for HEXFETs increases with temperature, but not greatly, as Figure 11 illustrates. This contrasts with other types of power MOSFETs in which minority carrier lifetime killing is employed in order to reduce the recovery time of the diode. As Figure 12 shows, the lifetime killing becomes ineffective as the junction temperature is raised so that at typical maximum junction temperature there is little difference between the speed of the HEXFET and other types of "fast diode" power MOSFETs.

With reference to Figure 13, during turn-on of HEXFET2, the dc rail voltage will be supported by the circuit inductance, the body-drain diode of device 1 and the drain source voltage of device 2. During the period when the body-drain diode of HEXFET 1 is still saturated with carriers and cannot support reverse voltage, the dc rail voltage is approximately distributed across the circuit inductance and the drain-source of HEXFET 2.

The rate of rise of current in HEXFET 2 is controlled by the rate of rise of its gate voltage, since drain current and gate voltage are linked by transconductance. The rate of rise of current determines the voltage drop across the circuit inductance (since $V = L \times di/dt$). The rest of the dc rail voltage appears across HEXFET 2.

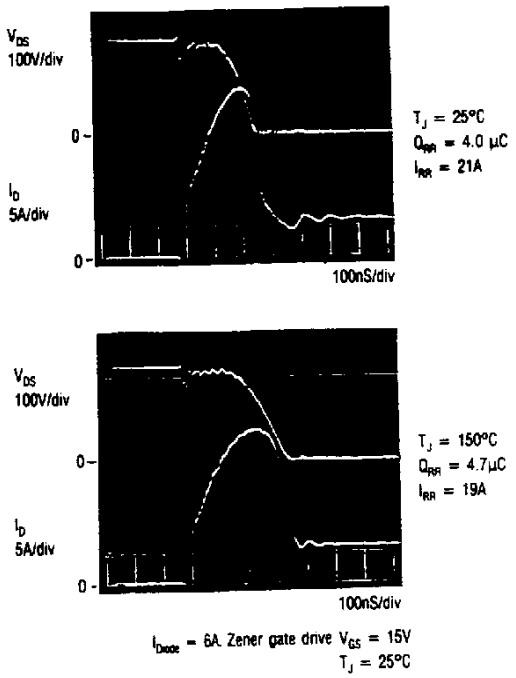


Figure 11. Variation of diode recovery current with junction temperature (IRF840)

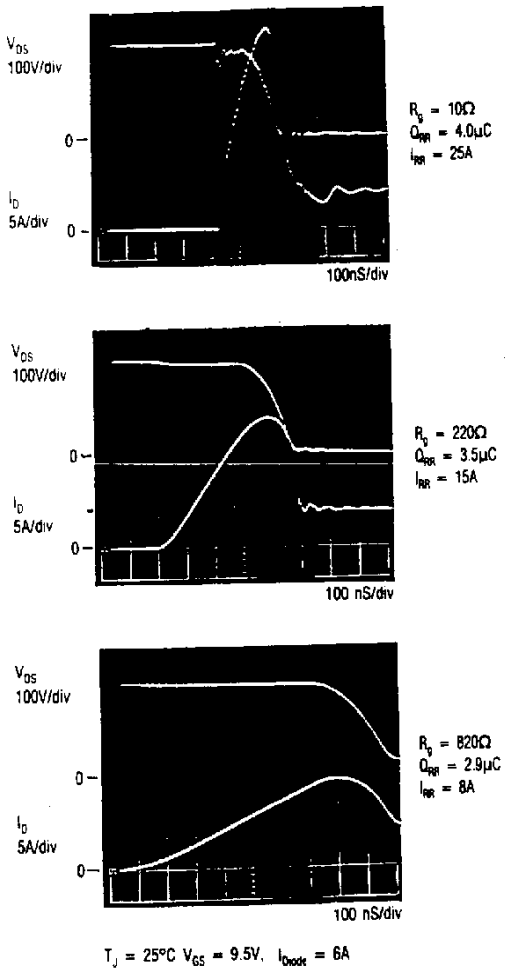


Figure 10. Variation of recovery current with switching speed (IRF840)

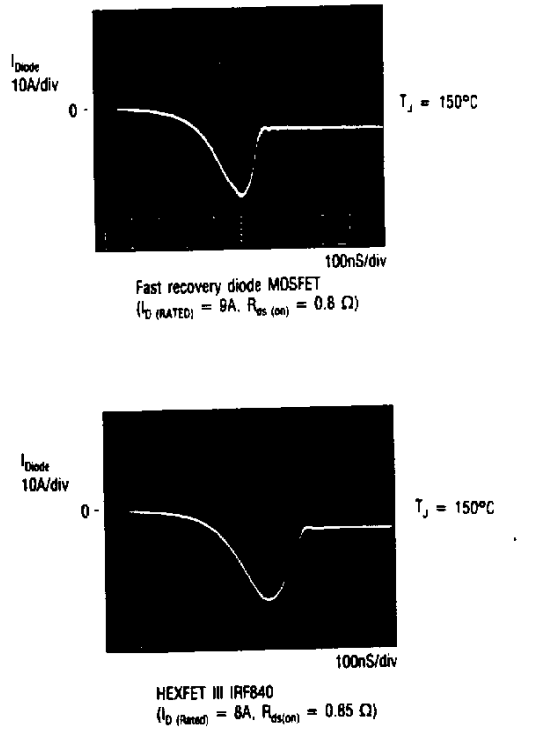


Figure 12. Comparison of recovery time of HEXFET III and MOSFET with minority carrier lifetime killing

The value of parasitic circuit inductance generally will not influence the di/dt during turn-on in an "off line" application. For example, the maximum di/dt in Figure 9 is about 0.15A/nS. This di/dt would develop a voltage of 30V across a typical circuit inductance of 200nH. If the dc bus voltage is 300V, this leaves 270V across HEXFET 2, leaving it still very much in its "linear" region of operation, and fully "in control" of its own di/dt. (The situation can be different for a low voltage high current circuit, or where inductance is purposefully added in the dc bus).

There are a number of ways in which the rate of rise of gate voltage can be controlled, and the reader is referred to IR Application Note AN-937.

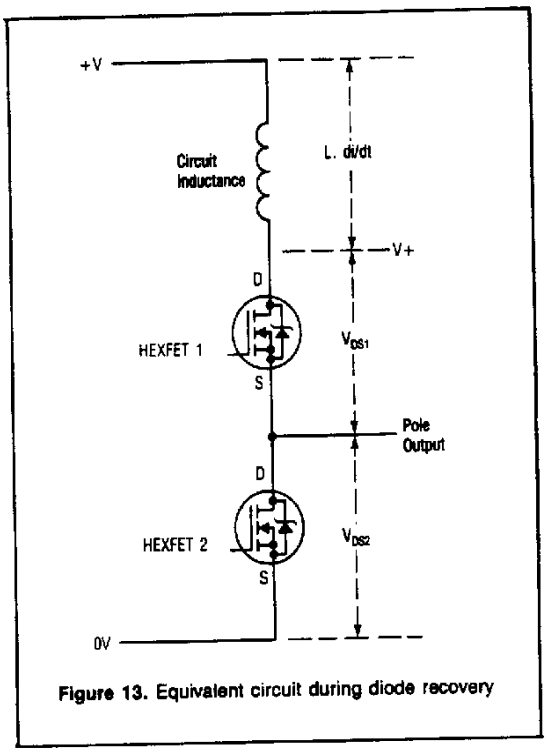


Figure 13. Equivalent circuit during diode recovery

Figure 14 shows an idealized version of the waveforms associated with the turn-on of the lower HEXFET (device 2) in one leg of an inverter. The origin of these waveforms is as follows:

t0 - t1. Delay time. The gate capacitance is charging to the threshold value, which it attains at time t1.

t1 - t2. HEXFET 2 starts to conduct, with a di/dt determined by the rate of rise of the gate voltage. The di/dt causes a voltage drop in the circuit inductance. The rest of the dc rail voltage is supported by the HEXFET. By t2 HEXFET 2 has taken over the load current from the diode of HEXFET 1 and the diode current has fallen to zero.

t2 - t3. Negative diode current in HEXFET 1 (shown as positive drain current) removes charge from the diode of HEXFET 1. At time t3 sufficient charge has been removed to enable HEXFET 1 to block voltage.

t3 - t4. The drain voltage of HEXFET 2 falls as the voltage across HEXFET 1 rises. Miller feedback now influences the switching of HEXFET 2. The diagram shows a constant current during this period. In reality the current is determined both by the Miller feedback and the relationship between rate of change of voltage and diode current during this stage of the recovery.

t4 - t5. The dc rail voltage, aided by the voltage across the circuit inductance produced by the changing current, now appears across HEXFET 1, and the current in its diode decays to zero.

In practice the periods t3 - t4 and t4 - t5 are very short and merge together. The fall in diode current is in fact very rapid at this time and the gate voltage falls to threshold level as the drain current falls to zero. The gate voltage then rises as the gate capacitance is charged through the series gate resistor.

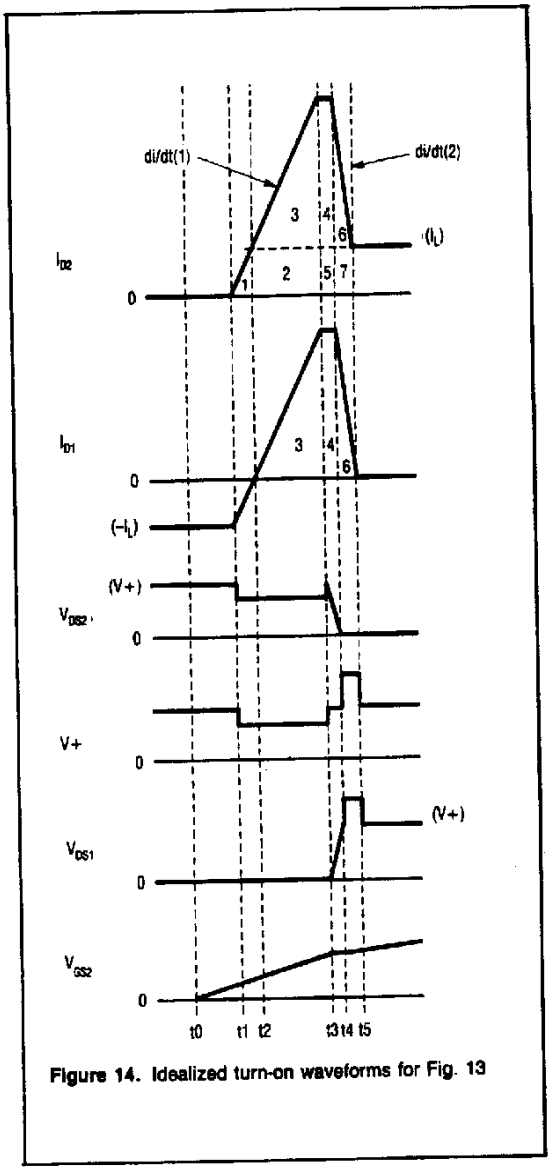


Figure 14. Idealized turn-on waveforms for Fig. 13

Figure 15 shows the waveform photographs corresponding to the theoretical waveforms shown in Figure 14.

Effect of di/dt and Temperature on Q_{RR}

Figure 16 illustrates how Q_{RR} varies with switching speed. The relationship between Q_{RR} and di/dt is shown in Figure 17.

Figure 18 illustrates the effect of increasing temperature on Q_{RR}. The relationship between Q_{RR} and temperature is shown in Figure 19.

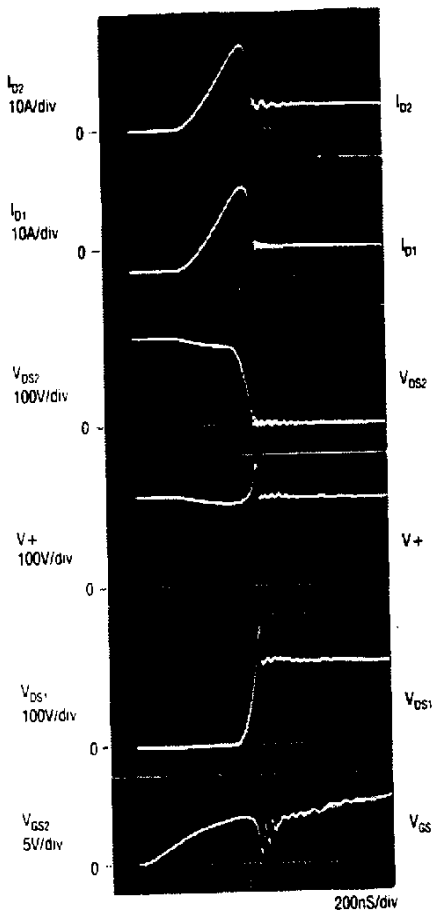


Figure 15. Waveform photographs correspondent to Fig. 14

Calculation of Switching Losses

The losses incurred during commutation may be predicted from Figure 14.

Conduction losses are ignored and only those losses produced when devices are simultaneously carrying current and blocking voltage are considered.

The losses in HEXFET 2 are as follows:

t1 - t2. The drain current builds up to the value of the load current while supporting the available voltage (dc rail voltage minus the drop in the circuit inductance.)

t2 - t3. Both the load current and the rising diode recovery current are carried while blocking the available voltage.

t3 - t4. Some losses incurred during this period but not a significant amount since the drain voltage is falling rapidly.

As the losses in HEXFET 2 decline the losses in HEXFET 1 increase:

t3 - t4. Some losses incurred as the voltage across the diode increases.

t4 - t5. The final phase of the diode recovery current producing losses, since the diode now blocks the available voltage.

The losses in HEXFET 1 and HEXFET 2 have two basic origins: the conduction of the load current by HEXFET 2 during the period t0 - t3 and the passage of diode recovery current through both devices during the period t1 - t5.

Estimation of the total losses is simplified if it is assumed that the effect of the circuit inductance is neutral, in that while it reduces the available voltage during one part of the switching cycle, it increases it during another. (If the breakdown voltage of the HEXFET is exceeded then this energy will be dissipated in avalanche breakdown, which is permitted with HEXFET III devices, provided the repetitive avalanche ratings are respected). Therefore, if it is assumed that all charge transfer takes place between supply rails whose voltage remains constant at the nominal value, the total losses during commutation of the inverter leg may be calculated approximately by multiplying the dc rail voltage by the various transfers of charge that occur. If a series inductor with its own clamping circuit is located in the dc rail, then energy stored in this inductor is not dissipated in the HEXFET but in the clamp circuit.

Thus the losses in HEXFET 2 are given by the rail voltage times the charge represented by areas 1, 2 and 3 in Figure 14. The losses in HEXFET 1 are given by the rail voltage times the charge represented by area 6. Losses associated with areas 4 and 5 are distributed between the two HEXFETs. The total losses are therefore approximately equal to the rail voltage multiplied by the charge represented by areas 1, 2, 3, 4, 5 and 6. Areas 3, 4 and 6 represent the Q_{RR} of the diode. Areas 1, 2 and 5 are a function of the load current and the rate of rise of diode recovery current, di/dt.

Thus the total commutation energy loss may be expressed as:

$$E = V_{dc}\,[(\text{Area 3} + \text{Area 4} + \text{Area 6}) + (\text{Area 2} + \text{Area 5}) + (\text{Area 1})]$$

$$= V_{dc}\left[Q_{RR} + I_L\,(t_4 - t_2) + (t_2 - t_1)^2 \cdot \frac{di/dt}{2}\right]$$

$$= V_{dc}\left(Q_{RR} + I_L\sqrt{\frac{2Q_{RR}}{di/dt}} + \frac{I_L^2}{2di/dt}\right) \qquad (1)$$

Where I_L is the load current at the time of the commutation.

This gives the energy loss for the pulse at one value of drain current. From Figure 20 it can be seen that to a first approximation Q_{RR} is linearly related to drain current and therefore, assuming a sinusoidal load current, can be expressed as:

$$Q_{RR}(t) = K \cdot i(t)$$
$$= K \cdot I_L \sin(\omega t),$$

and:

$$Q_{RR}(\theta) = K \cdot I_L \sin\theta, \text{ where } 0 < \theta < \pi \qquad (2)$$

Substituting into (1) for Q_{RR} gives the energy dissipated when a commutation occurs at a current value of I sin θ.

$$E(\theta) = V_{dc}\left[K \cdot I_L \sin\theta + I_L \sin\theta\sqrt{\frac{2KI_L \sin\theta}{di/dt}} + \frac{I_L^2 \sin^2\theta}{2\,di/dt}\right] \qquad (3)$$

The power loss due to commutation during that switching cycle is given by:

$$P(\theta) = V_{dc} \cdot f_s\left[K \cdot I_L \sin\theta + I_L \sin\theta\sqrt{\frac{2KI_L\sin\theta}{di/dt}} + \frac{I_L^2 \sin^2\theta}{2\,di/dt}\right] \qquad (4)$$

Where f_s is the switching frequency

Since the switching frequency is approximately two orders of magnitude greater than the output frequency, equation (4) can be taken as representing the power loss due to commutation expressed as a continuous function of θ.

The average power loss due to commutation during one half cycle of output current is therefore given by:

$$P_{ave} = \frac{V_{dc} \cdot f_s}{\pi}\left[K \cdot I_L \int_0^{\pi} \sin\theta \, d\theta + I_L \sqrt{\frac{2KI_L}{di/dt}} \int_0^{\pi} \sin^{3/2}\theta \, d\theta + \frac{I_L^2}{2di/dt} \int_0^{\pi} \sin^2\theta \, d\theta\right]$$

$$= \frac{V_{dc} \cdot f_s \cdot I_L}{\pi}\left[2K + 2.47\sqrt{\frac{KI_L}{di/dt}} + 0.785\,\frac{I_L}{di/dt}\right] \quad (5)$$

This represents the sum of the commutation power loss in both HEXFETs in that inverter "leg" (or "pole").

The process for determining the commutation losses is therefore:

(1) Read the typical value for Q_{RR} from the data sheet.

(2) Adjust Q_{RR} for di/dt and temperature, using the graphs shown in Figure 17 and Figure 19.

(3) Using this value of Q_{RR} obtain K from the equation:

$$K = Q_{RR} / I_F$$

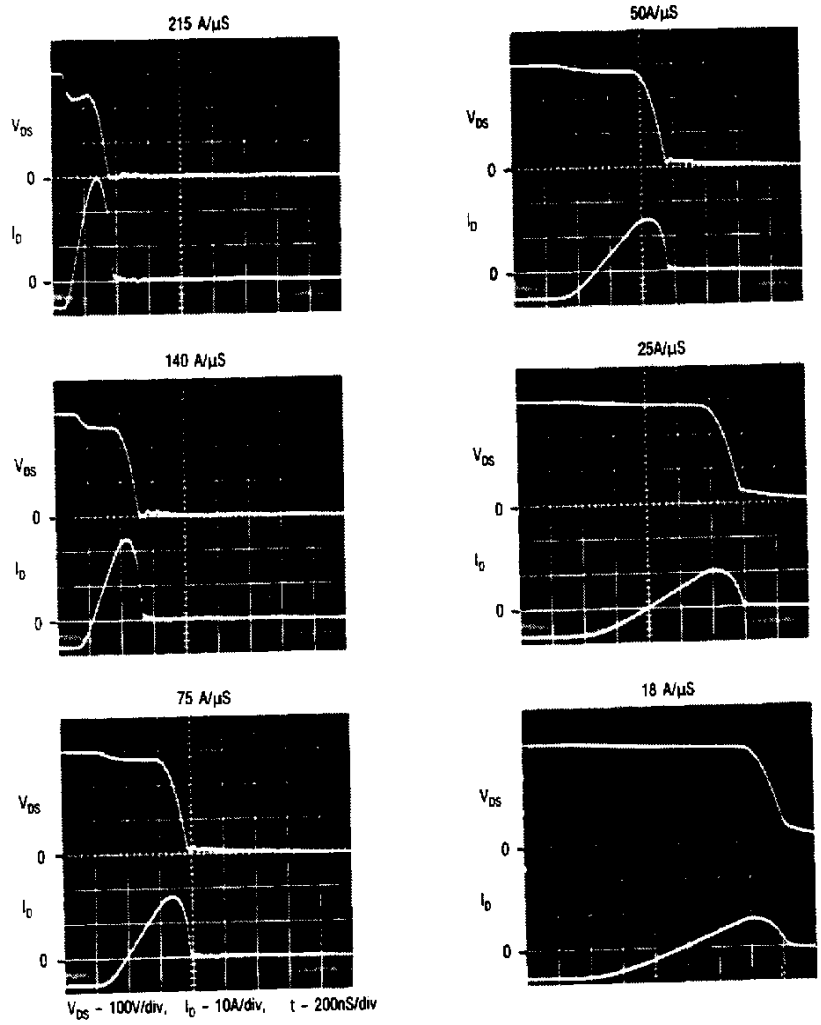


Figure 16. Diode recovery waveforms for a range of di/dt

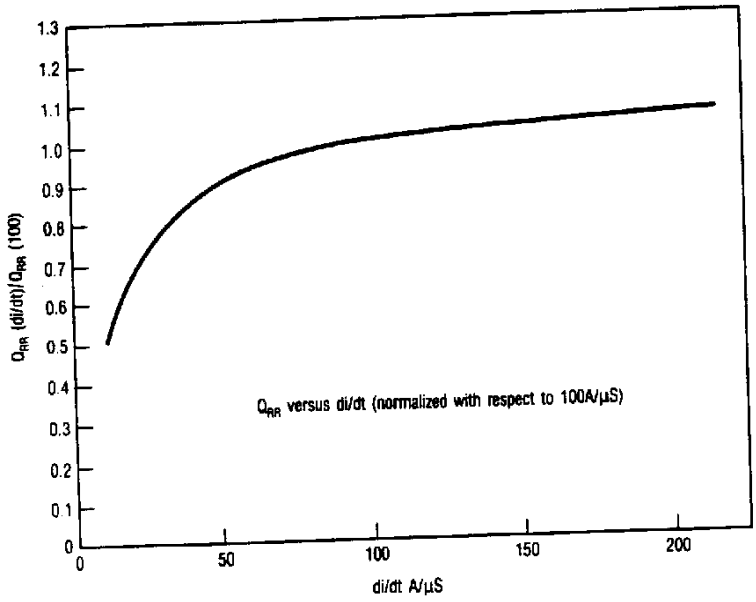


Figure 17. Relationship between Q_{RR} and di/dt

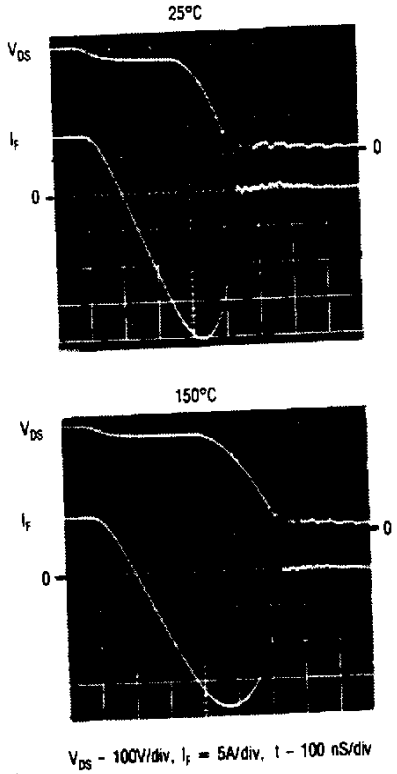


Figure 18. Effect of temperature on Q_{RR}

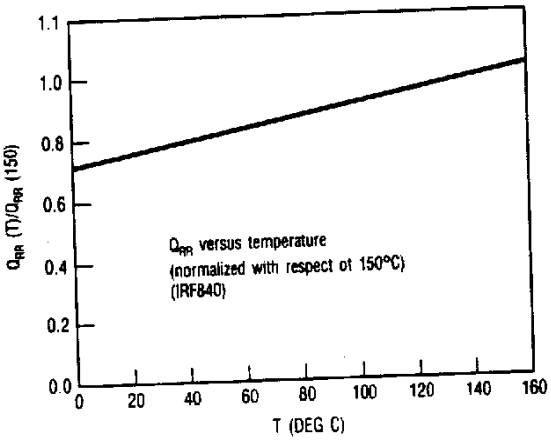


Figure 19. Relationship between Q_{RR} and temperature

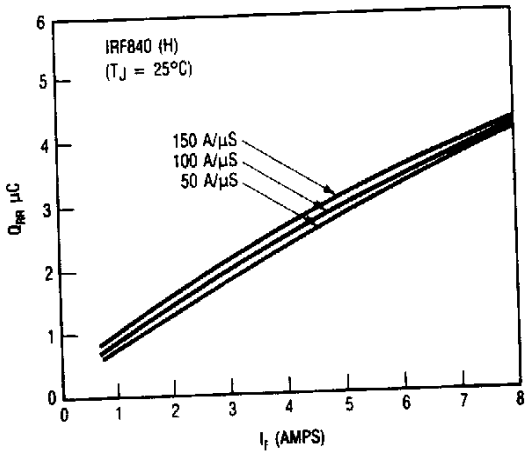


Fig. 20 — Q_{RR} vs. Drain Current

where I_F is the test current specified in the typical Q_{RR} rating in the data sheet.

(4) Substitute K along with di/dt and I_L in equation (5) to obtain the commutation power loss.

Turn-Off Losses

As Figure 21 shows, turn-off losses are small compared with conduction losses and diode recovery losses. Therefore turn-off losses do not significantly affect loss calculations and can be ignored.

Optimum Switching Speed

As long as Q_{RR} remains constant the commutation losses can be minimized by using as high a value of di/dt as possible, as Figure 22 shows. The highest acceptable value of di/dt will be determined by how closely the peak drain current is to be allowed to approach the maximum allowable drain current, I_{DM}.

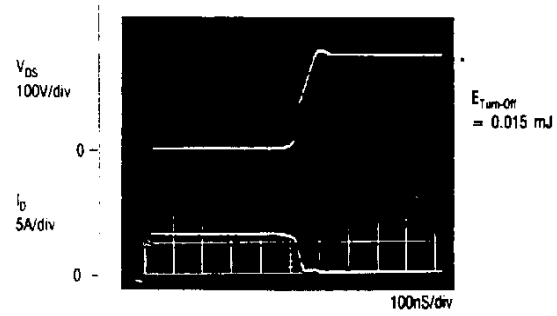


Figure 21. Turn-off (IRF840)

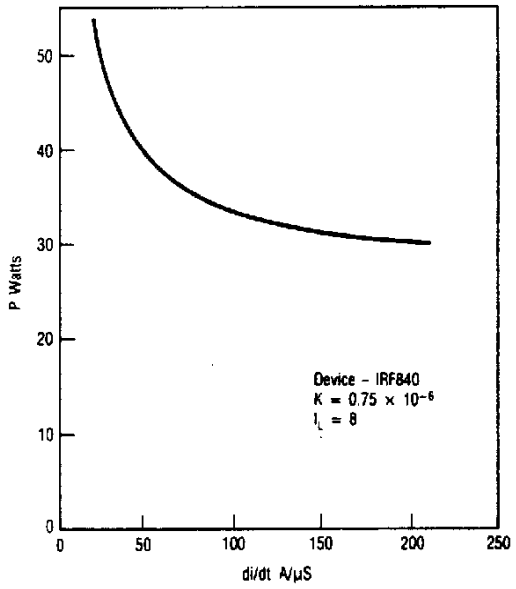


Figure 22. Commutation power loss versus di/dt

Q_{RR} is approximately constant over a wide range of di/dt as Figure 17 shows. Very low values of di/dt do lead to a reduction in Q_{RR}, but this reduction is only achieved by switching at a rate which makes the switching time unacceptably long for most PWM applications.

Conduction Losses

The load current is carried either by the channel of one HEXFET or by the body-drain diode of the other. If carried by the channel of a HEXFET the power dissipation in the HEXFET during that period is given by:

$$P_d = i_d \cdot R_{DS(on)}$$

$R_{DS(on)}$ is a function of the die temperature and, to a lesser extent, of the instantaneous value of the drain current. HEXFET data sheets include graphs of $R_{DS(on)}$ versus temperature and $R_{DS(on)}$ versus drain current.

During the period when the load current is being carried by the body-drain diode of one of the HEXFETs the power dissipation is given by:

$$P_d = i_d \cdot V_{SD}$$

V_{SD}, the forward drop of the body-drain diode, is a function of the load current. HEXFET data sheets incorporate a graph showing V_{SD} versus diode current.

Since the direction of current flow at any time is not predetermined, but rather is determined by load conditions, the upper HEXFET is kept on all the time during positive segments of a switching cycle and the lower HEXFET is kept on during the negative segments of a switching cycle (except for short deadbands when both devices are off to prevent overlapping conduction and shoot-through). When load current is flowing through a body-drain diode, therefore, the channel associated with that diode will be in conducting state. A proportion of the load current will flow through the channel, since current can flow through the channel of a HEXFET in either direction. This lowers the voltage drop across the HEXFET. In high voltage devices with relatively high values of $R_{DS(on)}$ this effect will be negligible but in low voltage inverters conduction losses can be mitigated by this effect. Diode recovery losses, however, are not affected since the channel is turned off prior to commutation, to avoid a shoot-through, and the freewheeling current reverts to flowing in the diode.

As Figure 23 shows, during each switching cycle the proportion of time spent in each mode (channel conduction or diode conduction) depends on the modulation duty cycle, δ, prevailing during that switching cycle. The modulation duty cycle is directly related to the required magnitude of fundamental output voltage at that time. Therefore, for a sinusoidal output waveform, the division of losses between channel conduction and diode conduction varies sinusoidally throughout the output cycle. At the same time the magnitude of the load current varies with a phase relationship to the fundamental voltage output waveform that is determined by the load power factor.

Calculation of Conduction Losses

Heat sinking must be sized for worst-case dissipation, which occurs when the load power factor is unity and the longest MOSFET conduction periods coincide with the peaks of the load current. As will be seen, diode conduction losses are much less than MOSFET forward conduction losses, so that although diode losses increase as the load phase angle moves away from 0°, the total losses are reduced. Similarly total losses are greatest when the modulation depth is unity (assuming sinusoidal modulation).

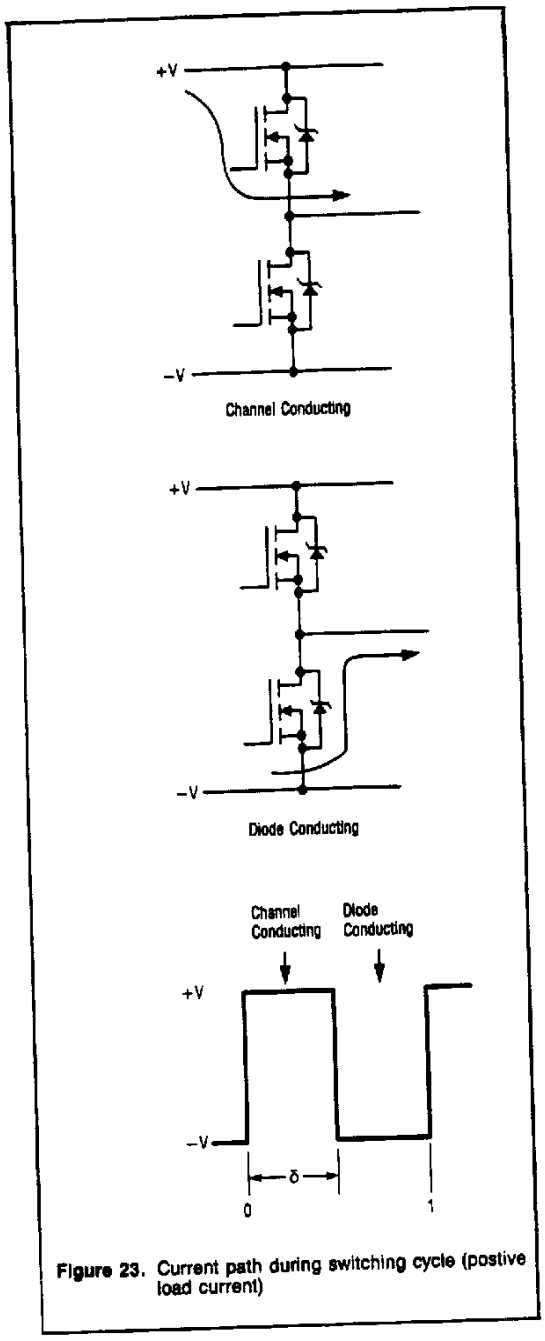


Figure 23. Current path during switching cycle (postive load current)

Under these conditions the MOSFET losses may be calculated as follows. Assume a load current waveform or the form $I_L \cdot \sin\theta$. During a switching cycle occuring approximately at a time corresponding to the angle θ, the MOSFET will conduct in the forward direction for a proportion of the cycle given by:

$$\text{MOSFET pulse width} = 1/2\ (1 + \sin\theta)$$

The proportion of the cycle for which the diode conducts is given by:

$$\text{Diode pulse} = 1/2\ (1 - \sin\theta)$$

Therefore the MOSFET power loss during a pulse occuring at angle θ is:

$$P(\theta) = I_L^2\ R$$
$$= I_L^2 \sin\theta .\ 1/2\ (1 + \sin\theta) \cdot R_{DS(on)}$$
$$= 1/2\ I_L^2\ R_{DS(on)}\ (\sin^2\theta + \sin^3\theta)$$

The average power loss over one half cycle is given by:

$$P_{ave} = \frac{I_L^2\ R_{DS(on)}}{2\pi} \int_0^{\pi} (\sin^2\theta + \sin^3\theta)\, d\theta$$

$$= 0.462\ I_L^2\ R_{DS(on)}$$

Figure 24 shows how losses vary with load power factor.

The diode conduction losses for a switching cycle at angle θ are given by:

$$P(\theta) = I_L \cdot V_{SD}$$
$$= I_L \sin\theta \cdot 1/2\ (1 - \sin\theta) \cdot V_{SD}$$

Where V_{SD} is the forward diode drop. To simplify calculations this is assumed to be constant for all values of current.

The average power loss due to diode conduction over one half cycle is therefore given:

$$P_{ave} = \frac{I_L \cdot V_{SD}}{2\pi} \int_0^{\pi} (\sin\theta - \sin^2\theta)\, d\theta$$

$$= 0.068 \cdot I_L \cdot V_{SD}$$

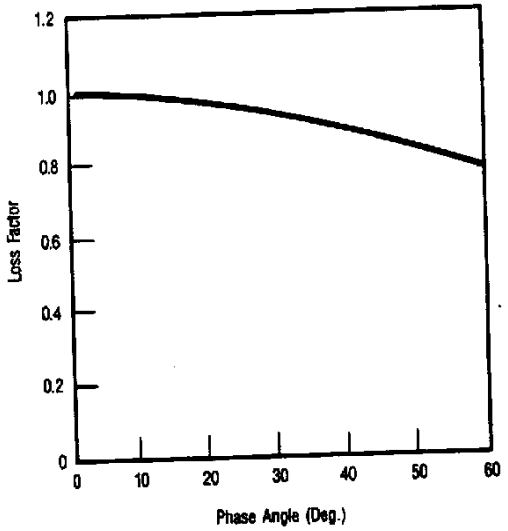


Figure 24. MOSFET conduction losses versus phase angle

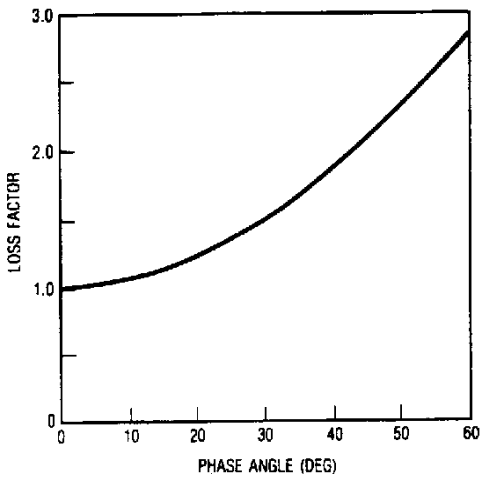


Figure 25. Diode conduction versus phase angle

Figure 25 shows how these losses vary with load power factor.

Example Design - 240V Input 1kVA Inverter

The circuit shown in Figure 26, operating from a dc supply of 305V (rectified 220Vac), using IRF840 HEXFET's, delivered an output power of 1kVA, as detailed by the following test results:

V_{dc} = 305V
Switching Frequency = 20 kHz
Output Frequency = 100 Hz
Modulation Depth = 98%
Power Factor = 0.95
I_{load} = 3.43 amps rms
T_J = 90°C
dc supply input power = 1125 Watts
ac output power = 1005 Watts
Total inverter losses = 1125 − 1005 = 120W
Inverter efficiency = 90%
Inverter rating = 1.05 kVA

The HEXFET losses may be calculated using the following data.

Measured value of I_L = 5.0 Amps (slightly higher than 2 × I_{rms} due to ripple and waveform distortion.)

The data sheet typical value for $R_{DS\ (on)}$ at 25°C is 0.8 Ohms. Using the data sheet graph of $R_{DS\ (on)}$ versus temperature, the typical value of $R_{DS\ (on)}$ at 90°C is 0.8 × 1.6 = 1.28 Ohms.

The diode forward drop is assumed to be 1 Volt for all values of current.

The average power loss per phase due to conduction is therefore given by:

P_{ave} = 0.462 I_L^2 $R_{DS(on)}$ × (phase angle factor from Fig. 24)
+ 0.068 I_L V_{SD} × (phase angle factor from Fig. 25)
= 0.462 × 25 × 1.28 × 0.972) + (0.068 × 5 × 1 × 1.22)
= 14.4 + 0.4
= 14.8 Watts per phase.

Using the data sheet value for Q_{RR} of 6.4 µC (for the conditions I_F = 9 amps at di/dt = 100 A/µs and 150°C) the value of K at 90°C and di/dt = 100 A/µs is given by:

$$K = (6.4 \times 0.9) / 8 = 0.72\ \mu C/Amp$$

$$P_{ave} = \frac{V_{dc} \cdot f_s \cdot I_L}{\pi} \left[2K + 2.47 \sqrt{\frac{KI_L}{di/dt}} + 0.785 \frac{I_L}{di/dt} \right]$$

$$= \frac{305 \times 20 \times 10^3 \times 5}{\pi} \left[2 \times 0.7 + 2.47 \sqrt{\frac{0.72 \times 5}{100}} + \frac{0.785 \times 5}{100} \right]$$

$$= 9.71\ [1.4 + 0.47 + 0.04]$$
$$= 18.5 \text{ watts/phase}$$

The calculated total HEXFET losses are therefore given by:

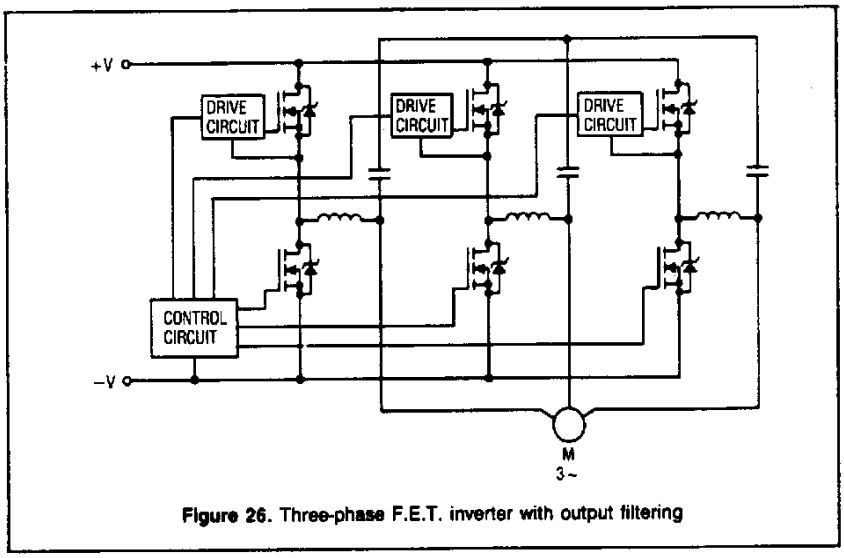


Figure 26. Three-phase F.E.T. inverter with output filtering

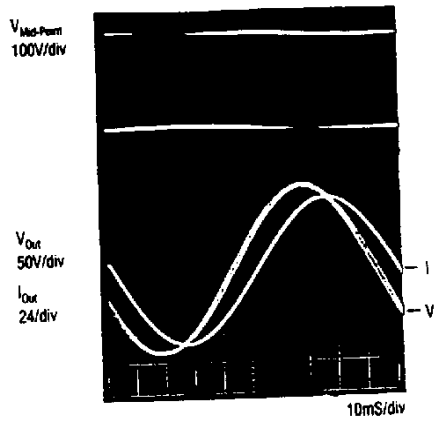


Figure 27. Output waveforms of IKVA inverter using IRF840 HEXFET

$P_{total} = 3 \times (14.8 + 18.5) = 100$ Watts.

The total measured inverter losses were 120W, of which 9W were calculated to be in the filter inductors and wiring. There is thus good agreement between the above calculated HEXFET losses and actual test measurements, with 11W "left over" for capacitor losses and HEXFET turn-off losses (not included in the above because they are relatively small).

Figure 27 shows typical output waveforms of this particular inverter.

Choice of HEXFET for Different Inverter Ratings

The power rating obtainable from a three-phase inverter using a particular HEXFET type depends on two considerations — efficiency and equipment size. The two are linked to some extent. The governing factor for both criteria is the size of the heat sink that the designer considers acceptable. A small heatsink will, for a given power output, give a high junction temperature, high $R_{DS}(on)$ and therefore higher conduction losses. The efficiency will be reduced but the equipment will be small. A larger heatsink, on the other hand, will run cooler with a lower $R_{DS}(on)$ so that although the equipment will be larger the efficiency will be higher.

Conduction losses can be reduced by using HEXFETs with a larger die and a lower $R_{DS}(on)$.

Using the previous example of the IRF840 design, the size of heatsink required can be estimated. The losses for all three phases are 100 Watts (calculated). Allowing a 40°C difference between heatsink and ambient temperatures would require a heatsink with a rating of approximately 0.38°C per Watt for all six devices. Assuming a maximum R_{thJC} of 1°C per Watt and a maximum R_{thCS} of 1° C/W, the junction temperature would be 73° C above ambient temperature. Assuming an ambient temperature of 40°C gives a junction temperature of 113° C. This is an acceptable value given that the maximum allowable junction temperature is 150°C. The calculations were based on a junction temperature of 90°C, so that if a more accurate estimate of maximum junction temperature is required another iteration is required with the new junction temperature.

However, the calculations do show that a heat sink with a thermal resistance of 0.38°C/W is appropriate. The size of such a heatsink would be, for example, 25 cm × 20cm × 4 cm. This size should be acceptable for a general industrial use 1 kVA inverter.

HEXFET Selection Guide

Table 1 is a guide to HEXFET selection for three-phase inverters of various output kVA ratings, for 120V and 240V ac line inputs, for a modulation frequency in the 20kHz range. Higher ratings will be obtainable if forced cooling is used.

Comparison with Bipolar Transistors

Due to the high switching losses associated with bipolar transistors, HEXFETs have clear advantages for dr s switching at 20kHz or higher. However, for PWM driv operating in the 1 - 2 kHz band and for quasi-square-wav drives, HEXFETs must be compared with bipolar transistors on the basis of conduction losses and cost.

The conduction losses in a HEXFET can be reduced to any level desired by using a device with a large enough die (or by parallelling devices.) This means, when using a HEXFET that cost and conduction losses may be exchanged. Therefore, when comparing HEXFETs and bipolar transistors for low switching frequency applications, it is necessary to consider the total cost of each system.

For example, consider an application requiring 400 Volt tran-

Inverter kVA Rating	AC Line Input Voltage	HEXFET Voltage Rating	Die Size	HEXFET GUIDE TO220AB	TO247AC (TO3P)	TO204AA (TO3)	TO240AA (HEXPAK)
0.3	240	500	2	IRF820	—	IRF420	—
0.5	240	500	3	IRF830	—	IRF430	—
1.0	240	500	4	IRF840	IRFP440	IRF440	—
2.0	240	500	5	—	IRFP450	IRF450	—
3.0	240	500	6	—	IRFP460	—	—
3.5	240	500	2 × 5	—	—	—	IRFK2D450
7	240	500	4 × 5	—	—	—	IRFK4H450
0.25	120	250	2	IRF624	—	IRF224	—
0.45	120	250	3	IRF634	—	IRF234	—
0.9	120	250	4	IRF644	IRFP244	IRF244	—
1.8	120	250	5	—	IRFP254	IRF254	—

sistors in which the maximum load current is 5 Amps. The nearest equivalent to a HEXFET, with its high gain and integral freewheeling diode, is a Darlington bipolar transistor with built-in anti-parallel diode. A bipolar transistor rated at 8 Amps would generally have a gain that was just adequate at 5 Amps. Such a device would typically have a guaranteed maximum value of V_{CE} of 2.0 Volts when carrying 5 Amps.

An IRF350 (400V, $R_{DS(on)}$ at 25 C = 0.3 Ohms) has a maximum Rds(on) of 0.5 Ohms at a junction temperature of 100°C. The peak forward drop (at 5 Amps) is therefore 2.5 Volts, so that the average conduction losses would be about the same or slightly lower than for the bipolar transistor; this would be enhanced by the lower switching losses and absence of base drive losses in the HEXFET. Furthermore the bipolar transistor may well require snubbering in order to operate within its SOA during switching. Based on a comparison of device and system losses the correctly chosen HEXFET can have a slight edge.

It has a bigger edge when the base/gate drive requirements, and the ability to withstand arduous operating conditions, are considered. While the bipolar transistor requires both positive and negative current base drives to achieve respectable switching times, the HEXFET may be driven directly from buffered logic. Also, the surge current rating of a HEXFET is approximately four times its average current rating, so that the IRF350 described in the above design could withstand 60 Amps, representing a 1200% overload capability. Furthermore this surge current capability is encompassed within the SOA of the HEXFET.

An important cost factor when a range of drives is planned is that an increase in the power of a HEXFET inverter only requires an increase in the ratings of the HEXFETs, whereas it is necessary to redesign the base drive and snubber circuits when a different type of bipolar transistor is used. Little or no modification is required to the HEXFET gate drive when a HEXFET of different rating is used and no snubber is required with HEXFETs. Expensive design effort is thereby reduced when a product range is designed around HEXFETs.

For operation from a rectified 120V ac supply the 250 Volt range of HEXFETs (for example the IRF244) are suitable. The repetitive avalanche capability of the HEXFET III range ensures that the margin between likely peak values of dc rail voltage and the voltage rating of the HEXFETs is more than adequate. The value of $R_{DS(on)}$ for a die of given size decreases rapidly with decreasing voltage rating. HEXFET conduction losses or HEXFET costs, therefore, reduce rapidly with decreasing voltage.

The following table compares the characteristics and performance of HEXFETs and bipolar transistors:

HEXFET	Bipolar
Integral freewheel diode.	Only some Darlingtons have diode.
No snubber required.	Snubber often required.
Low switching losses.	High switching losses.
Can be driven direct from buffered logic.	Base drive circuits required.
Same design for different power ratings.	New base drive and snubber design required for different power rating.
High overload capability.	Limited overload capability.
Avalanche capability.	Usually no avalanche capability.

References

(1) International Rectifier Application Note An-966. "A New Generation of HEXFETs — HEXFET III."

(2) D.A. Grant, J.A. Houldsworth, K.N. Lower. IEEE IAS Proc. March/April 1983. "A New High-Quality PWM AC Drive."

Appendix 1 PWM Waveform Generation

The traditional method of PWM waveform generation has been to input to a comparator a triangular timing wave and a sinusoidal reference waveform. This method has to a large extent been replaced by digital waveform generation. The digital method has the advantage of freedom from drift, absence of dc components in the output, perfect phase balance, etc. The digital method also facilitates the generation of non-sinusoidal output waveforms where this is advantageous, such as when the output of the inverter is to be increased by the addition of a third harmonic to the phase voltage waveform.

Overmodulation may be used to obtain maximum output from the inverter. While overmodulation increases the amplitude of the fundamental of the output waveform, it also introduces distortion as Figure 28 illustrates. A preferable method of increasing the amplitude of the output is the addition to the reference sine wave a measure of third harmonic as shown in Figure 29 (Ref 2). Since the third harmonic will be eliminated from the line-to-line voltage waveform, by adding a third harmonic of one-sixth amplitude of the fundamental output voltage of the inverter, its kVA rating can be increased by 15% without distortion of the output. □

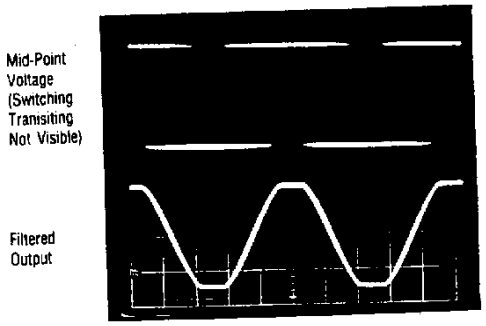


Figure 28. Distortion introduced by overmodulation

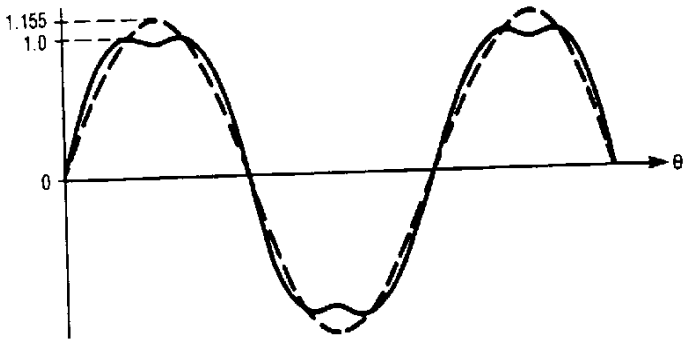


Figure 29. Increasing fundamental output voltage by addition of third harmonic