The new OptiMOS™ 6 80 V family of MOSFETs

Latest Infineon trench MOSFET technology setting the new industry standard for higher power density designs

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About this document

Scope and purpose

This document introduces the OptiMOS™ 6 80 V MOSFET technology, the latest member of Infineon's OptiMOS™ 6 family of MOSFETs already released and available in 40 V, 100 V and 120 V [1], [2], [3].

Based on Infineon's latest trench MOSFET technology, which takes advantage of a revolutionary cell design, the brand new OptiMOS™ 6 80 V combines the benefits of exceptionally low on-state resistance $R_{DS(on)}$ and superior switching performance. Moreover, the new technology comes with an extended safe operating area (SOA), and it is available in a rich portfolio of packages. These features make the OptiMOS™ 6 suited to a variety of applications, supporting the trend toward significantly higher efficiency while enabling design for higher power densities and cost-effectiveness.

Typical applications for OptiMOS™ 6 80 V MOSFETs include switched-mode power supplies (SMPS) and DC-DC converters in data centers and telecom as well as solar and battery management systems.

This application note showcases the new OptiMOS™ 6 80 V, with a focus on fast-switching DC-DC telecom/data center SMPS. First, a brief introduction to the technology highlights its technical benefits. Next, an extensive experimental evaluation is carried out, comparing OptiMOS™ 6 to the previous generation (OptiMOS™ 5) of 80 V MOSFETs.

Intended audience

This application note is targeted at application engineers and designers of DC-DC converters for telecom/data center applications.

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1 Introduction: The new OptiMOS™ 6 80 V

1.1 Features and benefits

OptiMOS™ 6 80 V represents Infineon's latest silicon trench MOSFET technology specifically optimized for high-frequency SMPS. Showing the industry's best figures-of-merit (FOMs), it helps with achieving high efficiency, high power density, and high system reliability.

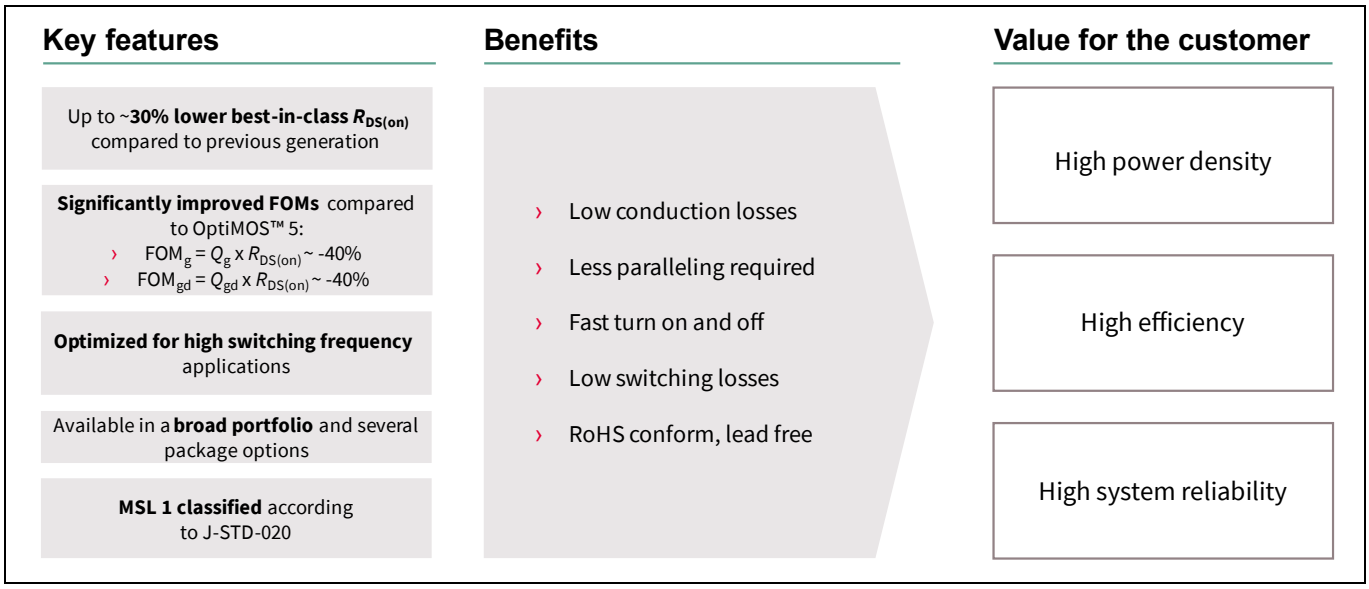


Figure 1 Key features and benefits of the new OptiMOS™ 6 80 V MOSFET technology

Similar to OptiMOS™ 6 in 100 V and the upcoming 200 V, the new 80 V class comes with a novel cell design, exploiting a full tri-dimensional charge compensation principle and enabling remarkable improvements in the specific on-state resistance.

The new cell structure also comes with a completely redesigned gate trench, leading to an outstanding reduction of the gate-to-drain charge Q_{gd} and total gate charge Q_g. The introduction of a metal gate technology brings a number of advantages. Beside the overall reduction of the internal gate resistance, it significantly improves the gate resistance uniformity over the chip, which translates to superior switching performances. It also enhances the robustness against dv/dt-induced parasitic re-turn-on of the MOSFET.

The new OptiMOS™ 6 80 V comes with a broad product portfolio (Section 2: Product portfolio) and is packaged in SuperSO8 (PQFN 5 x 6 mm^2) and PQFN 3.3 x 3.3 mm^2.

1.2 Target applications

The new OptiMOS™ 6 80 V shows very well-balanced improvement across all the FOMs, to the benefit of high-power, high-switching-frequency applications where both low $R_{DS(on)}$ and charges (switching performances) play crucial roles as efficiency drivers.

Indeed, the new technology is specifically optimized for high-frequency SMPS, suitable for both hard- and soft-switching applications.

The best-in-class (BiC) $R_{DS(on)}$, together with an expanded SOA, also addresses applications such as e-fuse, hot-swap and battery-management systems. The list of main applications targeted by the new Infineon OptiMOS™ 6 80 V is shown in Table 1.

Table 1 List of applications targeted by the new Infineon OptiMOS™ 6 80 V

Scope	Application	Topology	Fitting
Primary applications	 48 V systems: telecom/data center brick DC-DC converters	Hard-switched full-bridge/half-bridge (FB/HB)	Primary-side MOSFETs
	 Telecom 5G RFPA PSUs	Various isolated/non-isolated topologies	Control MOSFET
	  Telecom/data center PSUs	FB/FB LLC (400 V to 54 V)	Synchronous rectifier (SR) MOSFETs
	 Microinverter, power optimizer	Hard-switched FB/HB	High-side/low-side (HS/LS) MOSFETs
Secondary applications	 Battery management in BPA	Static charge/discharge switch	Pass transistor

1.3 Technology parameters: comparison between OptiMOS™ 6 and OptiMOS™ 5 in 80 V

In the following sections the latest OptiMOS™ 6 80 V technology will be compared with its predecessor, OptiMOS™ 5. First, the focus will be on BiC devices (i.e., with the minimum $R_{DS(on)}$) in SuperSO8 package (PQFN 5 x 6 mm^2) from the previous and latest families' portfolios. Later, the discussion will be generalized to the respective families by comparing the FOMs of the two technologies.

1.3.1 Datasheet comparison for BiC devices

In Table 2, a datasheet comparison is given for BiC devices with OptiMOS™ 6 80 V and OptiMOS™ 5 80 V. The table focuses on parameters that are most important for high-switching-frequency SMPS.

Table 2 Datasheet comparison between OptiMOS™ 6 (latest) and OptiMOS™ 5 (predecessor) 80 V BiC devices in SuperSO8 package

Specification	Symbol	Unit	Conditions	Infineon OptiMOS™ 6 ISC014N08NM6	Infineon OptiMOS™ 6 ISC018N08NM6	Infineon OptiMOS™ 5 BSC019N08NS5
On-state resistance	$R_{DS(on)}$	mΩ	V_{GS} = 10 V, I_D = 50 A T_J = 25°C (typ./max.)	1.2/1.45	1.5/1.8	1.6/1.9
Gate threshold voltage	$V_{GS(th)}$	V	V_{DS} = V_{GS} (min./typ./max.)	2.4/3.0/3.5	2.4/3.0/3.5	2.2/3.0/3.8
Gate resistance	R_G	Ω	(min./typ./max.)	0.55/0.8/1.0	0.5/0.77/1.0	N.A. /1.9/2.9
Drain current	I_D	A	T_C = 25°C	279	230	237
	$I_{D,\,pulse}$	A	T_A = 25°C	1116	920	948
Typ. charges	Q_{gs} Q_{gd} Q_g	nC	See notes [1]	27 15.8 79	22 12.7 63	29 20 94
Typ. capacitances	C_{iss} C_{oss} C_{rss}	pF	V_{DS} = 40 V, V_{GS} = 0 V, f = 1 MHz	5700 1900 46	4500 1500 37	6600 1100 47
Typ. output charge	Q_{oss}	nC	V_{DS} = 40 V, V_{GS} = 0 V	159	126	110
Typ. reverse recovery charge	Q_{rr}	nC	V_R = 40 V, di_F/dt = 100 A/µs [1]	65	54	80
Thermal resistance, junction to case	R_{thJC}	°C/W	Case bottom (typ./max.)	0.29/0.59	0.35/0.69	0.4/0.7
Max. junction temperature	$T_{J,max}$	°C		175	175	175

[1] Datasheet published value. Value depends on the datasheet-defined operating conditions.

1.3.2 On-state resistance $R_{DS(on)}$

The new OptiMOS™ 6 80 V technology shows significant improvement in terms of specific on-state resistance, compared to the previous generation of OptiMOS™ 5 80 V MOSFETs.

Figure 2 shows the comparison between the maximum $R_{DS(on)}$, specified for a gate-to-source voltage V_{GS} = 10 V, declared in the datasheet of BiC products of the OptiMOS™ families. The BiC device from the OptiMOS™ 6 80 V portfolio – packaged in PQFN 3.3 x 3.3 mm² – records a decrease of roughly 30 percent in $R_{DS(on)}$ compared to its counterpart from the the OptiMOS™ 5 family.

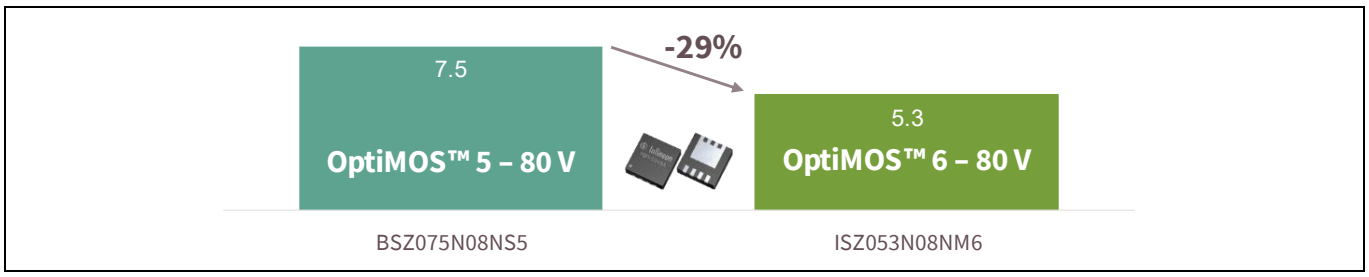


Figure 2 Comparison of the maximum $R_{DS(on)}$ (mΩ) for the BiC 80 V MOSFETs in PQFN 3.3 x 3.3 mm²

The new OptiMOS™ 6 80 V comes with the industry's best specific on-resistance FOM. This brings a series of advantages for the end applications, such as:

1. Reduction of conduction losses, depending on the package, by a factor of up to 30 percent.
2. The improvement in $R_{DS(on)}$ would enable reduction of the number of paralleled MOSFETs, saving both cost and PCB real estate and improving the power density.
3. Depending on the application, it would be possible to choose a smaller package (e.g., PQFN 3.3 x 3.3 mm²) without compromising the $R_{DS(on)}$.
4. For the same $R_{DS(on)}$ – compared to OptiMOS™ 5 – the new OptiMOS™ 6 80 V will bring price/performance benefits with improved efficiency, as will be shown in Section 3.1.

1.3.3 Technology FOM$_g$, and gate-to-drain charge figure-of-merit FOM$_{gd}$

The innovative gate trench design of the new OptiMOS™ 6 80 V leads to an outstanding reduction of both gate-to-source and gate-to-drain capacitances. This is reflected in the gate figures-of-merit FOM$_g$ and FOM$_{gd}$, with an improvement of roughly 40 percent compared to the previous generation, OptiMOS™ 5. (Figure 3).

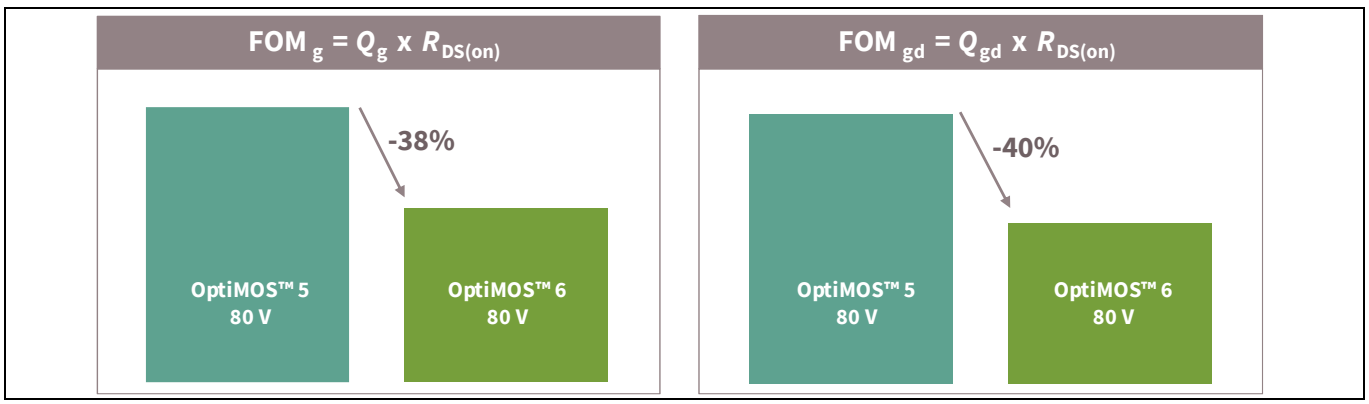


Figure 3 Comparison of FOM$_g$ and FOM$_{gd}$ for OptiMOS™ 5 80 V and OptiMOS™ 6 80 V families

The FOM_g – usually referred to simply as FOM – represents a synthetic performance indicator of a technology, and it is usually expressed in units of mΩ x nC. $R_{DS(on)}$ is a measure of the conduction losses, while Q_g impacts on both the driving losses and part of the switching losses, as it embeds Q_{gd}. In order to minimize the total losses, both $R_{DS(on)}$ and Q_g need to be minimized: the lower the FOM the better, as this minimizes the product of both of these quantities.

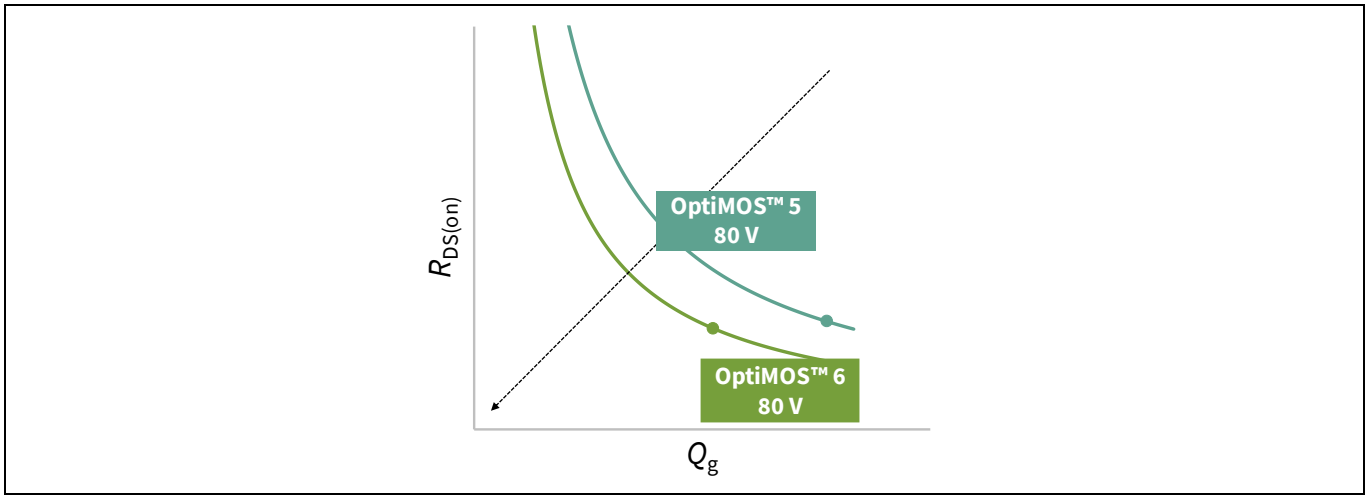


Figure 4 FOM imposes a trade-off between $R_{DS(on)}$ and Q_g for a given technology.

For a given technology, it is not possible to reduce the $R_{DS(on)}$ without impacting the charges, because this requires a bigger chip or parts paralleling. The only way to bring an improvement in both $R_{DS(on)}$ and Q_g is by moving to a new technology, with a better FOM (Figure 4).

In Figure 5 are plotted the gate charge characteristics for two devices – with roughly the same $R_{DS(on),max}$ – from OptiMOS™ 6 (ISC031N08NM6) and OptiMOS™ 5 (BSC030N08NS5) 80 V product portfolios, in SuperSO8 package.

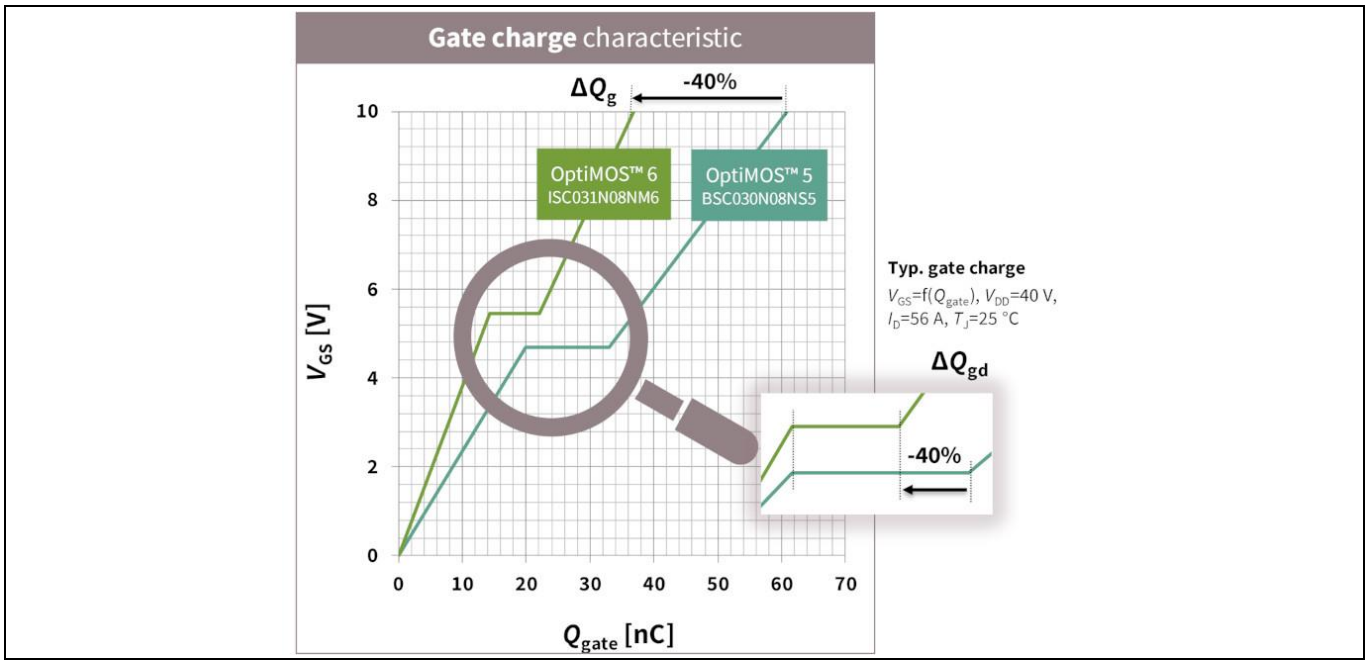


Figure 5 Gate charge curves comparison between devices with the same $R_{DS(on),typ}$ = 2.6 mΩ, from OptiMOS™ 6 (green) and OptiMOS™ 5 80 V (greenish-blue) product families

The new OptiMOS™ 6 80 V ISC031N08NM6 shows an outstanding reduction of 40 percent in both total gate and gate-to-drain charges, compared to its equivalent in the previous generation – OptiMOS™ 5 – of 80 V MOSFETs.

The Q_g reduction translates to better efficiency – especially in light-load conditions – due to reduced driving losses $P_{aux} = Q_g \times U_{GG} \times f_{sw}$. This is of particular importance in high-switching-frequency SMPS and in applications where a number of MOSFETs are paralleled, such as in synchronous rectification or in motor drives. In the latter case, low Q_g also enables relaxation of the requirements in the driver strength.

On the other hand, low Q_{gd} leads to fast-switching transients, lowering switching crossover losses, which are a non-negligible contributor to overall turn-off losses in hard-switching applications.

1.3.4 Output charge figure-of-merit FOM_{oss} and R_{oss}

The MOSFET output capacitance is charged in every switching cycle. In general, in hard-switched topologies, the stored energy cannot be recovered and generates a significant portion of the turn-on losses, because it is in fact dissipated across the channel during turn-on of the MOSFET.

Similarly to the technology FOM_g, the output charge figure-of-merit $FOM_{oss} = R_{DS(on)} \times Q_{oss}$ captures the technology trade-off between $R_{DS(on)}$ and some switching performances.

In hard-switching applications, losses associated with Q_{oss} get larger as the switching voltage increases, and scale linearly with the switching frequency. In general – in order to improve the efficiency in hard-switched, high-switching frequency SMPS – it is desirable to have a low value for the output charge.

When it comes to zero-voltage switching (ZVS) applications, a lower value for the output charge is also beneficial. It allows achieving ZVS with less circulating current, thus reducing the corresponding conduction losses and increasing the light-load efficiency. Lower Q_{oss} also allows reduction of the duration of the dead time, while extending the duration of the powering phase: this reduces the current waveform peak-to-average/RMS values, further decreasing the conduction losses for the same power transferred. Moreover, the new technology helps in significantly reducing the losses associated with the charge transfer when achieving ZVS, e.g., in resonant converters. These losses are sometimes known as hysteresis losses or E-passive losses associated with the MOSFET equivalent output capacitance. In modern silicon trench MOSFETs, the physical source of such losses is associated with the sheet resistance of the fieldplate electrode, which can be lumped into an equivalent resistance, R_{fp}, as shown in Figure 6b [4], [5]. Such resistance goes in series to a portion of the total output equivalent capacitance of the MOSFET, and such a network can be further simplified in a series-equivalent circuit – as if measured by an impedance meter – where an equivalent output resistance R_{oss} goes in series to the output capacitance C_{oss}. In the process of charging and discharging the output capacitance C_{oss}, part of the energy gets dissipated on this equivalent series resistance, resulting in losses which can impact significantly the efficiency of soft-switching power converters.

The value of the equivalent R_{oss} resistance can become significant for established trench MOSFET technologies with a common stripe layout, as the fieldplates are connected to the source at the end of the trench stripes. The new OptiMOS™ 6 80 V MOSFET technology – adopting a completely new concept for the cell design – shows a much lower value for R_{oss}, as each fieldplate is directly connected from the top to the source metal, significantly reducing the associated loss mechanism.

OptiMOS™ 6 80 V FOM_{oss} is unimpaired when compared to the industry's leading output charge figure-of-merit shown by OptiMOS™ 5 (Figure 6a).

Overall, the improvements recorded in the switching figures and other parasitics like R_{oss} make the new OptiMOS™ 6 80 V a switching-optimized technology. This means that the latest Infineon trench MOSFET technology is preferred for targeting both hard and soft fast-switching applications.

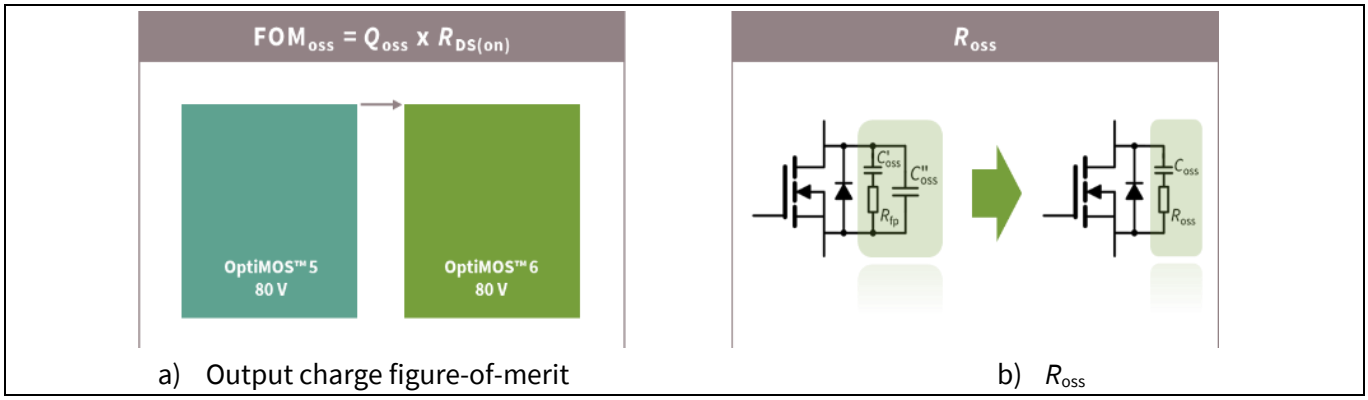


Figure 6 Comparison of output charge FOM_{oss} for the different technologies of 80 V MOSFETs

1.3.5 Transfer characteristic and safe operating area

The novel cell structure of the new OptiMOS™ 6 80 V is also reflected in the transfer characteristics of the MOSFET $I_D = f(V_{GS})$. The transfer characteristic is of particular importance when the MOSFET is driven to work in the linear region; that is, when the MOSFET operates as a voltage-controlled current source.

During the switching transient the MOSFET passes through the linear region of operation, so the transfer characteristics also control the switching characteristics, such as the value of the Miller plateau voltage.

The transfer characteristics for BiC devices from the new OptiMOS™ 6 80 V family of MOSFETs and from the previous-generation OptiMOS™ 5 are compared (Figure 7a). In OptiMOS™ 6, the particular design of the cell is reflected as a more gradual turn-on behavior of the MOSFET (Figure 7b). The lower transconductance recorded at low currents enhances the robustness of the MOSFET against thermal runaway. Indeed, MOSFETs may suffer from thermal instability at low current densities and high drain-source voltages due to a positive feedback effect with temperature, where the transconductance acts as a gain for this phenomenon. Together with an excellent junction-to-case thermal resistance, the new OptiMOS™ 6 shows significant SOA improvement, as is clear from the comparison in Figure 8. This is especially beneficial in applications other than SMPS, where the MOSFET is slowly switched or when the MOSFET is deliberately operated in the linear region, such as in hot-swap applications or in e-fuse protection circuits.

For a better insight into the thermal runaway phenomenon in MOSFETs and its origin, please refer to Infineon application notes [6], [7].

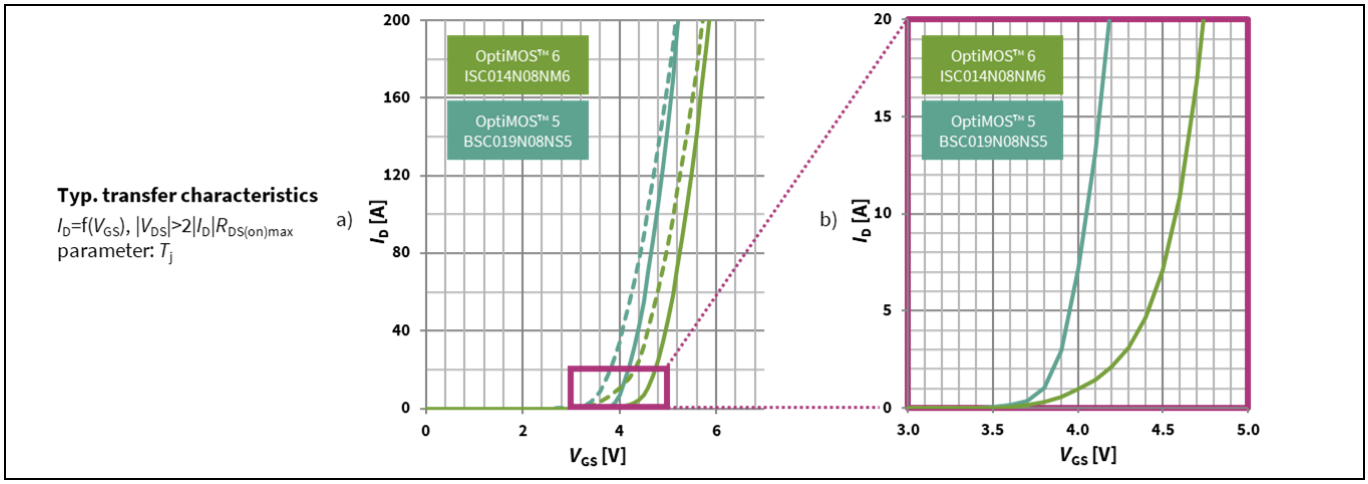


Figure 7 Comparison of typical transfer characteristics of BiC devices from OptiMOS™ 5 and OptiMOS™ 6 families of 80 V MOSFETs

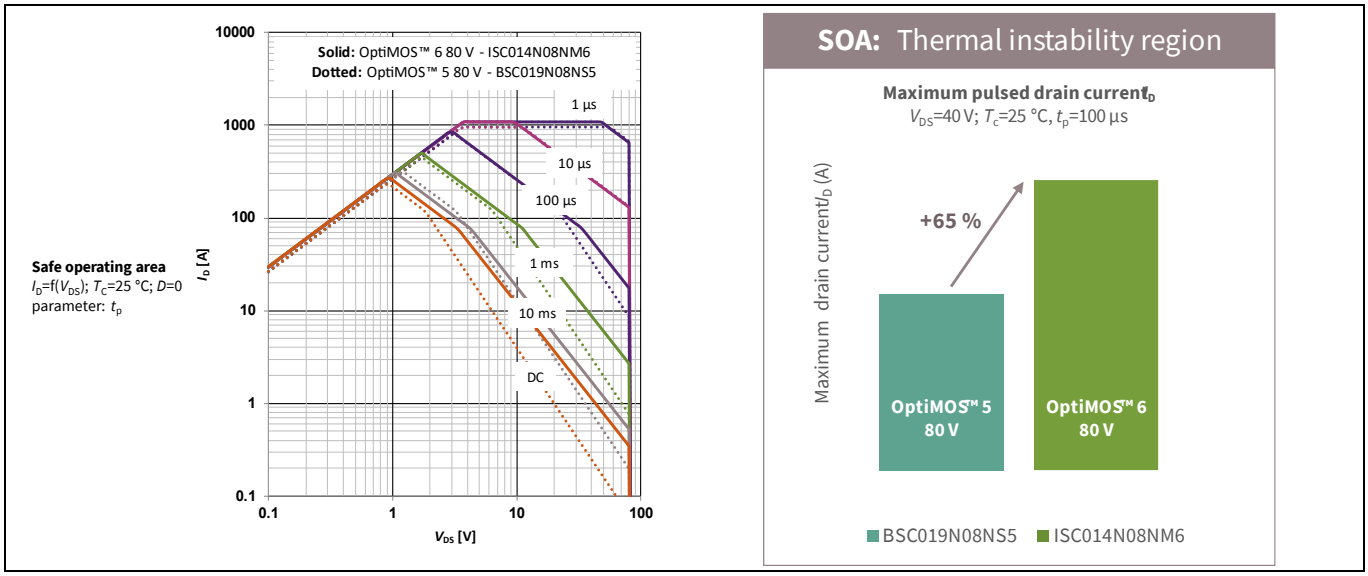


Figure 8 **Left: SOA comparison between BiC devices selected from OptiMOS™ 6 80 V and OptiMOS™ 5 80 V families of MOSFETs. Right: improvement in current capability in linear operation due to SOA improvement.**

Note: *The SOA diagram is provided within the ideal case of package temperature held at T_C = 25°C. When power pulse is applied, junction temperature rises according to the transient thermal impedance Z_{thjC}. In Infineon's OptiMOS™ power transistor datasheets, the $R_{DS(on)}$-limited region is traced, considering the worst-case value for the on-state resistance, i.e., the maximum value expected at T_J = 175°C.*

A narrowing trend in the SOA in modern trench MOSFET technologies is generally observed as a trade-off with the need to reduce the specific on-state resistance and improve figures-of-merit.

Nevertheless, Infineon OptiMOS™ 6 technology addresses this matter by showing a remarkably wider SOA, especially for longer power pulses in the range of hundreds of microseconds to DC, all while also significantly improving the $R_{DS(on)}$.

This would make the new OptiMOS™ 6 80 V, which is a clearly switching-optimized technology, also a feasible candidate for various linear applications, like hot-swap and e-fuse MOSFETs, especially in the smaller PQFN packages.

When the best-in-class performance in linear operation is the primary target, the OptiMOS™ Linear FET portfolio, tailored for linear applications, is recommended [8].

2 Product portfolio

OptiMOS™ 6 80 V comes in a large product portfolio, available in SuperSO8 (PQFN 5 x 6 mm^2) and PQFN 3.3 x 3.3 mm^2 surface-mount packages. Addressing a number of different applications, OptiMOS™ 6 80 V products help elevate power designs to the next level.



Figure 9 Potential application areas for OptiMOS™ 6 80 V

Table 3 OptiMOS™ 6 80 V product portfolio

V_{DS} [V]	Package	Product	$R_{DS(on)}$ at V_{GS} = 10 V [mΩ]	Q_g at V_{GS} = 10 V [nC]	$T_{J,max}$ [°C]	Qualification
80	PQFN 3.3 x 3.3 mm^2	ISZ053N08NM6	5.3	21	175	Industrial
		ISZ157N08NM6	15.7	8		
	SuperSO8 5 x 6 mm^2	ISC014N08NM6	1.45	79		
		ISC018N08NM6	1.8	63		
		ISC031N08NM6	3.1	37		
		ISC056N08NM6	5.6	21		
		ISC088N08NM6	8.8	14		
		ISC151N08NM6	15.1	8.3		

3 Value proposition in primary applications

In the following sections, the value proposition of OptiMOS™ 6 80 V in primary applications (hard- and soft-switching DC-DC converters/SMPS) is proven by experimental evaluations.

Experimental evaluations are carried out for three different SMPS applications:

1. The first application considered is a 1 kW DC-DC intermediate bus converter (IBC) for 48 V data center applications, in a distributed-power open standards alliance (DOSA) quarter-brick form factor. The converter is based on a 4:1 fixed-ratio full-bridge LLC. Zero-voltage switching (ZVS) for primary MOSFETs and zero-voltage/zero-current switching (ZVZCS) for the synchronous rectifiers is achieved for all line/load conditions, hence eliminating the switching losses to a large extent. With an input voltage range spanning from 42 V to 60 V, 80 V MOSFETs are used at the primary bridge. The right fit for this application is a best-in-class device with the lowest possible $R_{DS(on)}$. The new OptiMOS™ 6 80 V ISC014N08NM6, 1.45 mΩ $R_{DS(on),max}$ packaged in SuperSO8 replaces in this application two BSC030N08NS5 from the previous generation, OptiMOS™ 5, of 80 V MOSFETs.

2. The second application presented is a 600 W telecom DC-DC IBC, again in quarter-brick form factor. The fully regulated converter is based on a full-bridge topology with center-tapped (CT) rectification. As the input voltage can be as high as 75 V, and the turns-ratio is 3:1, 80 V MOSFETs are used for the synchronous rectifiers. The right fit for this application is a device combining the lowest possible $R_{DS(on)}$ with the need for low output charge Q_{oss} and reverse recovery charge Q_{rr} to minimize switching losses. The new OptiMOS™ 6 80 V ISZ053N08NM6, 5.3 mΩ $R_{DS(on),max}$ packaged in PQFN 3.3 x 3.3 mm^2 replaces in this application the BSC040N08NS5 in PQFN 5 x 6 mm^2 from the previous-generation OptiMOS™ 5, reducing losses and saving more than 60 percent of PCB real estate allocated for the SRs.

3. The third application presented is a 750 W telecom DC-DC converter for the power supply of modern GaN/LDMOS radio-frequency power amplifiers (RFPAs). The fully regulated converter is based on a full-bridge topology, where both conduction and switching losses impact the overall system efficiency, due to its hard-switching nature. As the input voltage can be as high as 60 V, 80 V MOSFETs are used at the primary bridge. The right fit for this application is a device combining the lowest possible $R_{DS(on)}$ with the need for low charges. The new OptiMOS™ 6 80 V ISC031N08NM6, 3.1 mΩ $R_{DS(on),max}$ packaged in SuperSO8 is compared in this application with the BSC030N08NS5 from the previous OptiMOS™ 5 generation.

3.1 Infineon 1 kW 4:1 DCX intermediate bus converter for 48 V data center

3.1.1 Introduction

In modern data center systems, especially those targeting high-performance computing (HPC) or artificial intelligence (AI) training workloads, extremely high currents (more than 1000 A) must be supplied to sub-1 V digital loads (xPUs/ASICs), from the available 48 V DC power distribution bus. The problem of powering such processors from the 48 V is typically addressed by means of the cascode of two conversion stages. An intermediate bus DC-DC converter (IBC) steps down the 48 V to an intermediate voltage V_{mid}. A voltage regulator module (VRM) later performs the final V_{mid} to V_{core} conversion, while meeting the needs of the digital load.

The efficiency of the two stages can be maximized by choosing the most opportune down-conversion ratio for the IBC and with the burden of regulation being transferred to the multiphase VRM. Indeed, unregulated IBCs in the form of DC transformers (DCX) are employed in these applications, showing typical peak efficiencies that exceed 98 percent, much higher than their regulated counterparts (Figure 10).

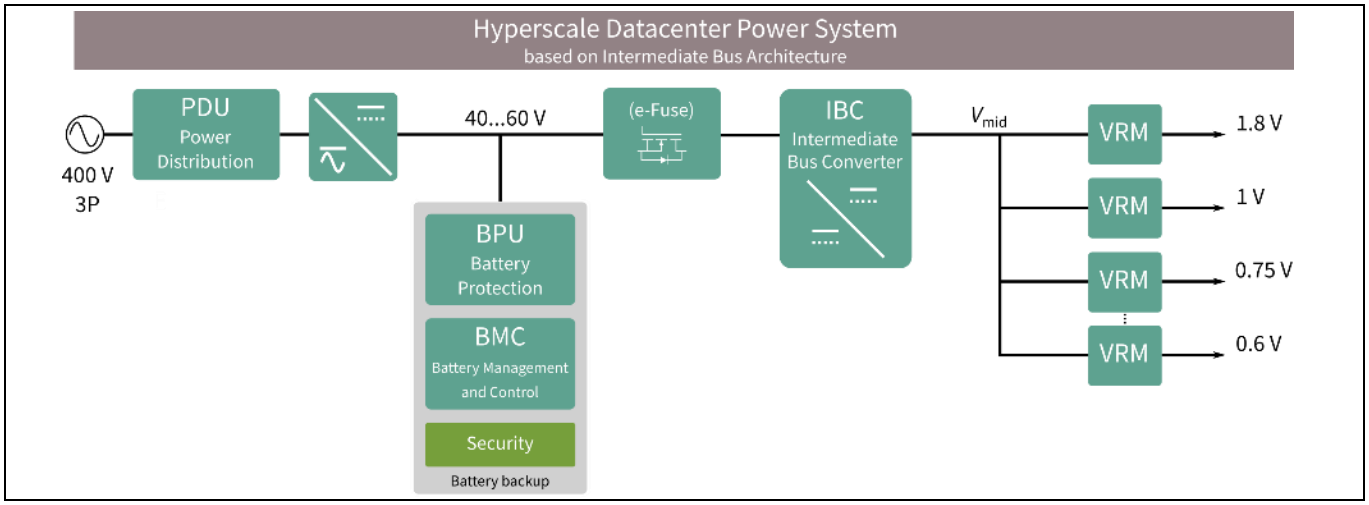


Figure 10 Simplified schematic representation of a typical hyperscale data center power system, based on the intermediate bus architecture (IBA)

IBCs can come either in the form of power modules, or down solutions already laid out on the system motherboard. A wide variety of topologies are nowadays adopted for the IBC, which can rely on transformers (isolated) or autotransformers (non-isolated), switched capacitor dividers or both (hybrid converters). Such IBCs may be fully regulated, partially regulated or unregulated. In the case of fixed-ratio converters (DCX), down-conversion ratios can span from 4:1 down to 12:1.

3.1.2 Test platform description

Infineon has developed a fully functional, 4:1 unregulated IBC reference design, operating from an input voltage range of 42 to 60 V DC. The Infineon reference design REF_1KW_LLC_XDPP1100 is a 1 kW fixed-frequency, 4:1 LLC converter coming in a standard DOSA-compliant quarter-brick footprint and achieving 97.3 percent typical peak efficiency.

The board has been designed as a testing platform, trading power area density for easier access to probe test points, with an option for resonant current measurement, and easy reworking/replacement of components. The module is equipped with an onboard auxiliary housekeeping supply to provide the required bias.

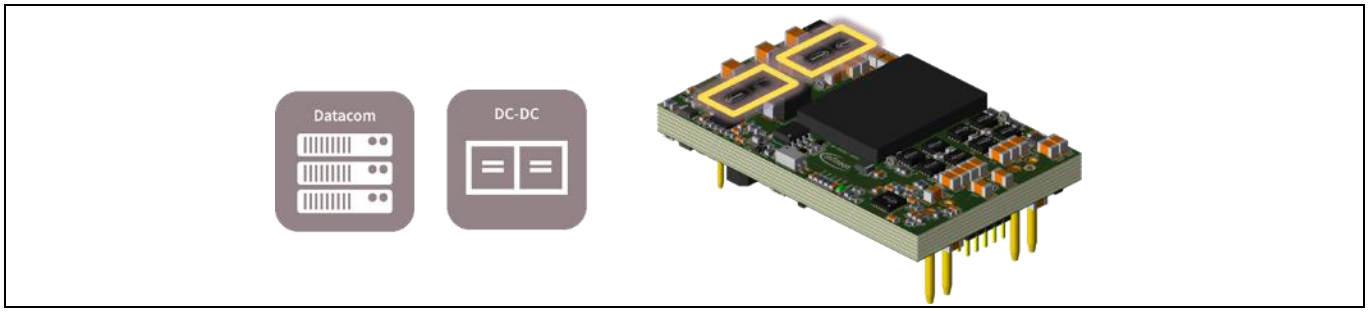


Figure 11 3D view of the Infineon REF_1KW_LLC_XDPP1100 1 kW, 4:1 LLC IBC with the primary-full bridge devices (focus of the test) highlighted

3.1.2.1 Design description and schematics

The schematic diagram for the main power stage of the Infineon 1 kW, 4:1 FB LLC isolated quarter-brick converter REF_1KW_LLC_XDPP1100 is shown in Figure 12.

Main power stage, control and housekeeping

In the design of the converter REF_1KW_LLC_XDPP1100, the following products from Infineon's portfolio were selected:

- OptiMOS™ 6 80 V MOSFETs ISC031N08NM6, 3.1 mΩ $R_{DS(on),max}$ in SuperSO8 package (PQFN 5 x 6 mm^2) are used at the primary side of the FB LLC converter. The board is designed to fit two devices per position, for a total of eight power MOSFETs.
- OptiMOS™ 5 25 V MOSFETs IQE006NE2LM5, 0.65 mΩ $R_{DS(on),max}$ in PQFN 3.3 x 3.3 mm^2 source-down package are used as SRs in the secondary-side FB. Four devices per position are paralleled to handle the output current, for a total of 16 power MOSFETs.
- Primary MOSFETs are driven by EiceDRIVER™ 2EDL8034G4B gate driver, the latest generation of 2EDL8x 120 V HB drivers, with fastest propagation delay.
- EiceDRIVER™ gate driver 2EDL8124G dual-channel junction-isolated gate drivers are used in the secondary-side bridge, offering differential inputs with built-in hysteresis for inherent shoot-through protection.
- Infineon's digital power controller XDP™ XDPP1100-Q024, combining high-performance analog front-end (AFE), state-machine-based digital control loop and a microcontroller in a single chip. The controller is perfectly suited to telecom infrastructure, 48 V server motherboards, data centers and industrial applications.

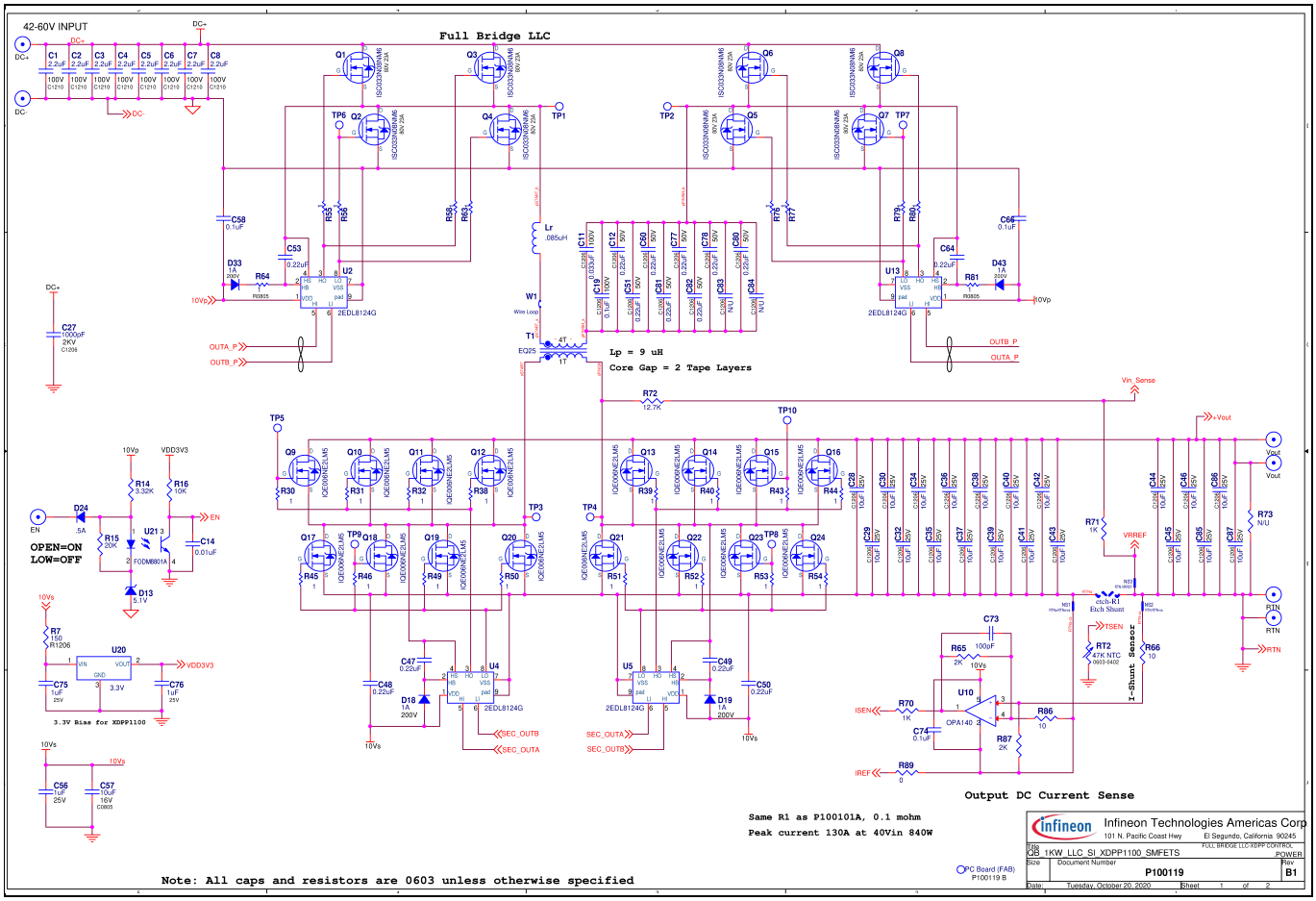


Figure 12 Infineon 1 kW, 4:1 FB LLC isolated quarter-brick converter REF_1KW_LLC_XDPP1100. Schematic page 1: main power stage.

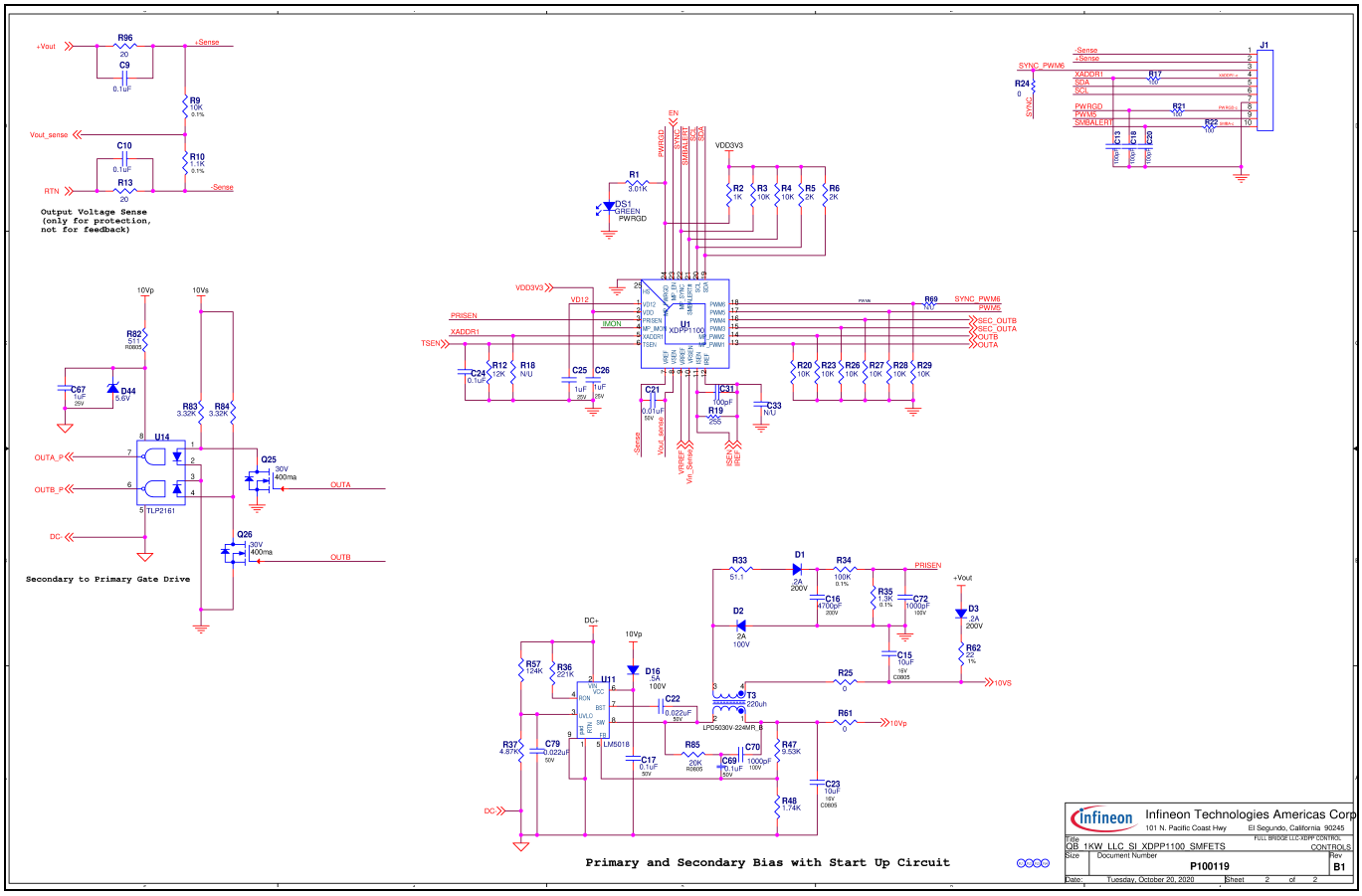


Figure 13 Infineon 1 kW, 4:1 FB LLC isolated quarter-brick converter REF_1KW_LLC_XDPP1100. Schematic page 2: control and housekeeping.

3.1.2.2 PCB description

Figure 14 shows the placement of the different components and measurement test points on the Infineon 1 kW, 4:1 FB LLC isolated quarter-brick converter REF_1KW_LLC_XDPP1100.

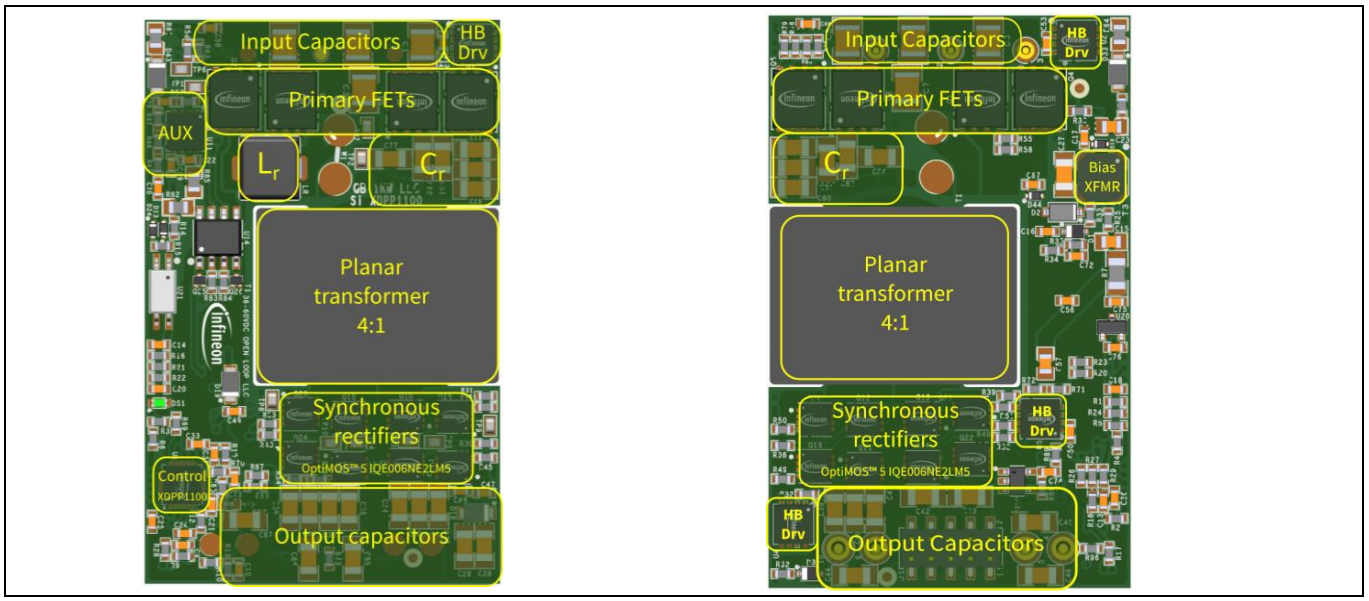


Figure 14 Placement of the most significant components in the Infineon 1 kW, 4:1 FB LLC isolated quarter-brick converter

The outer dimensions of the board, designed without enclosure, are 2.3 in. x 1.45 in. x 0.5 in. (58.42 mm x 36.83 mm x 12.7 mm), which results in a power density in the range of 35 W/cm^3 (560 W/in^3). The PCB stackup is 14 layers deep. The internal layers are all 6 oz. copper thickness with the top and bottom layers at 4 oz. copper thickness. The total board thickness is 186 mils (4.72 mm).

3.1.2.3 Board specifications

The specifications for the Infineon 1 kW, 4:1 FB LLC isolated quarter-brick converter REF_1KW_LLC_XDPP1100 are given in Table 4.

Table 4 Infineon 1 kW, 4:1 FB LLC isolated quarter-brick converter REF_1KW_LLC_XDPP1100

Parameter	Symbol	Values			Unit	Note/test condition
		Min.	Typ.	Max.		
Operating input voltage	V_{in}	42	48	60	V	
Efficiency	η		97.3		%	V_{in} = 54 V, I_{out} = 40 A
Start-up voltage threshold	$V_{in\ (on)}$	34			V	
Minimum operating voltage after start-up	$V_{in\ (off)}$			32	V	
Output power (TDP)	$P_{out,TDP}$	0		1000	W	
Power dissipation	P_{diss}		41		W	V_{in} = 54 V, P_{out} = $P_{out,TDP}$
Output voltage	V_{out}	10		15	V	Output voltage is unregulated
Dynamic load response	$\Delta V_{out(tr,load)}$			680	mVpp	Load step 50-100% of $P_{out,TDP}$, di/dt = 1 A/µs, $C_{out,ext}$ = 1800 µF aluminum electrolytic
Output ripple and noise	$V_{out,ac}$			250	mVpp	V_{in} = 48 V, $C_{out,ext}$ = 1800 µF aluminum electrolytic
Recommended output capacitance	C_{out}	1000			µF	
Switching frequency	f_{sw}		310		kHz	
Airflow velocity	v_{air}		600 3		LFM m/s	

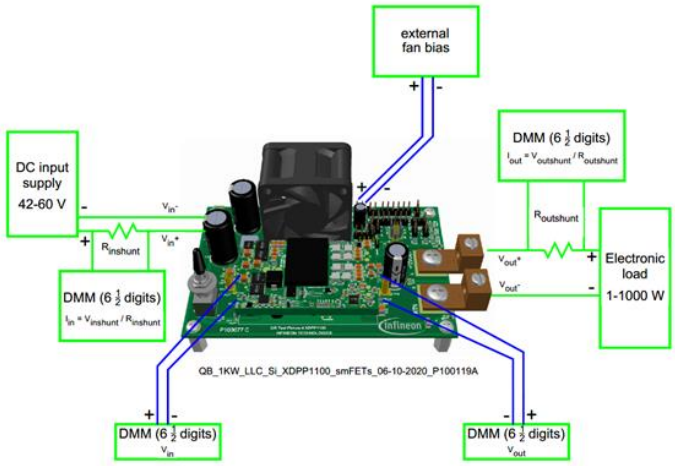
3.1.3 Test setup description

3.1.3.1 Description of the test setup

The test setup is described here in detail. The actual test setup is shown in Figure 16.

Measuring equipment

- 6½ digits data acquisition unit (DAQ) for input, output and shunt voltage measurement
- High-bandwidth (1 GHz) digital oscilloscope (DSO), passive voltage probes, 30 A current probe
- High-resolution thermal camera



DC voltage sources

- DC PSU capable of delivering at least 1100 W, up to 60 V DC
- Auxiliary DC PSU capable of providing 6 to 12 V DC to provide bias to cooling fan

Active load

- Low-voltage, high-current (more than 80 A) DC electronic load

Precision current shunts

- Input and ouput precision current shunt resistor (0.1 %)

Figure 15 Test setup schematic description

Test fixture board

The Infineon 1 kW, 4:1 FB LLC IBC REF_1KW_LLC_XDPP1100, being a brick power module, is a board-mounted power supply. In order to provide reliable and repeatable measurement data, tests were carried out with the help of a proper brick test fixture.

The fixture provides the necessary filter capacitor for the input and output ports, power connection terminals and a cooling fan. The measuring equipment is directly connected to the test fixture, while the brick module can be easily plugged in and out, easing the reworking activities between different tests. The power connections with the host board are made with press-fit connectors.

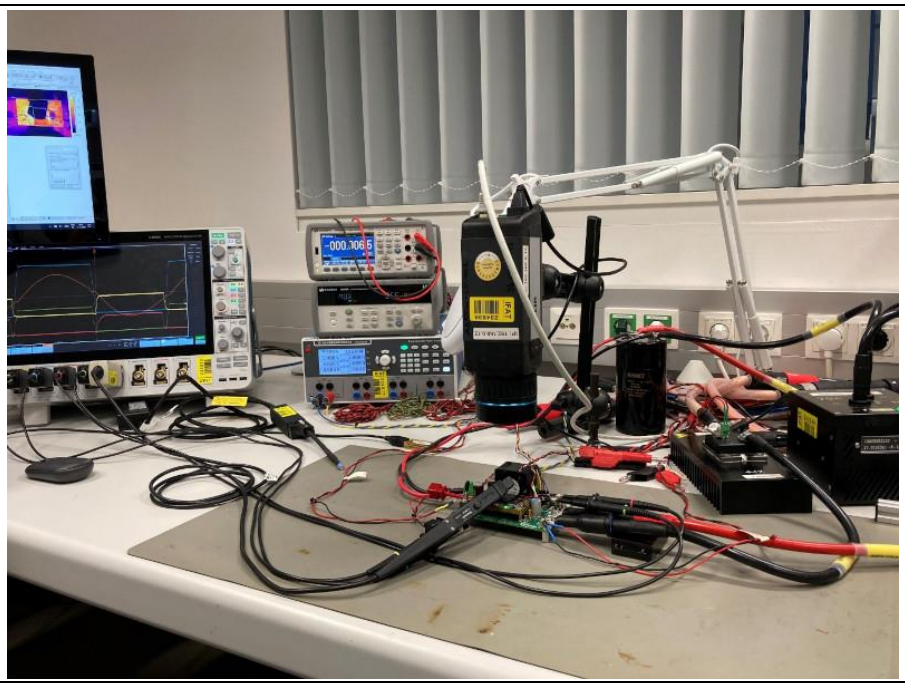


Figure 16 Actual test setup

3.1.4 Efficiency test

3.1.4.1 Introduction

Efficiency tests have been performed for the Infineon 1 kW, 4:1 FB LLC isolated quarter-brick converter [10] using the test setup introduced in section 3.1.3 Test setup description.Efficiencies have been captured for three different configurations of the primary full bridge, featuaring three different devices under test (DUTs). All the DUTs come with the same surface-mount package, commonly known as SuperSO8 (PQFN 5 x 6 mm^2).

Only the primary MOSFETs change among the tests, while everything else is kept unchanged in the brick board and in the whole test setup, except for the fine adjustments in the duty cycle needed for fair comparison of the device performance (in order to achieve the same duration of the effective body diode conduction for all the DUTs).

All the tests have been carried out on the same brick unit.

A summary of the DUTs and their position is given in Table 5.

Table 5 Devices under test – refer to schematic file reported in Figure 12

DUTs	DUT #1	DUT #2	DUT #3
Primary-bridge MOSFETs: Q1…Q8	**Infineon OptiMOS™ 5 80 V, 3 mΩ** BSC030N08NS5	**Infineon OptiMOS™ 6 80 V, 3.1 mΩ** ISC031N08NM6	**Infineon OptiMOS™ 6 80 V, 1.45 mΩ** ISC014N08NM6
DUTs per each full-bridge position	2	2	1

Note: When testing DUT #3, OptiMOS™ 6 80 V ISC014N08NM6, which comes with ~half of the $R_{DS(on)}$ compared to the other DUTs, only one device in each FB position has been used. As paralleling of each device is achieved on opposite sides of the board, devices were soldered only on top, with positions on the bottom left unpopulated.

3.1.4.2 Efficiency comparison at V_{in} = 54 V

Table 6 summarizes the efficiencies acquired at nominal input voltage (V_{in} = 54 V) for the different DUTs. The efficiency is measured at 600 LFM (3 m/s) airflow, T_A = 25°C and captured after thermal steady-state is reached.

Table 6 Measured efficiency (%) at nominal input voltage V_{in} = 54 V

DUT / Output current I_{out}	Infineon OptiMOS™ 5 80 V, 3 mΩ BSC030N08NS5 (2 DUTs/pos)	Infineon OptiMOS™ 6 80 V, 3.1 mΩ ISC031N08NM6 (2 DUTs/pos)	Infineon OptiMOS™ 6 80 V, 1.45 mΩ ISC014N08NM6 (1 DUT/pos)
8 A	92.78	93.66	93.54
20 A	96.43	96.83	96.78
40 A	97.17	97.40	97.36
60 A	96.92	97.09	97.02
80 A	96.29	96.46	96.37

First, the comparison of devices with same typical $R_{DS(on)}$ from the latest (OptiMOS™ 6) and previous-generation (OptiMOS™ 5) is given. The efficiency, and system total power dissipation curves (relative to the reference DUT BSC030N08NS5 from the previous-generation OptiMOS™ 5) are reported in Figure 17.

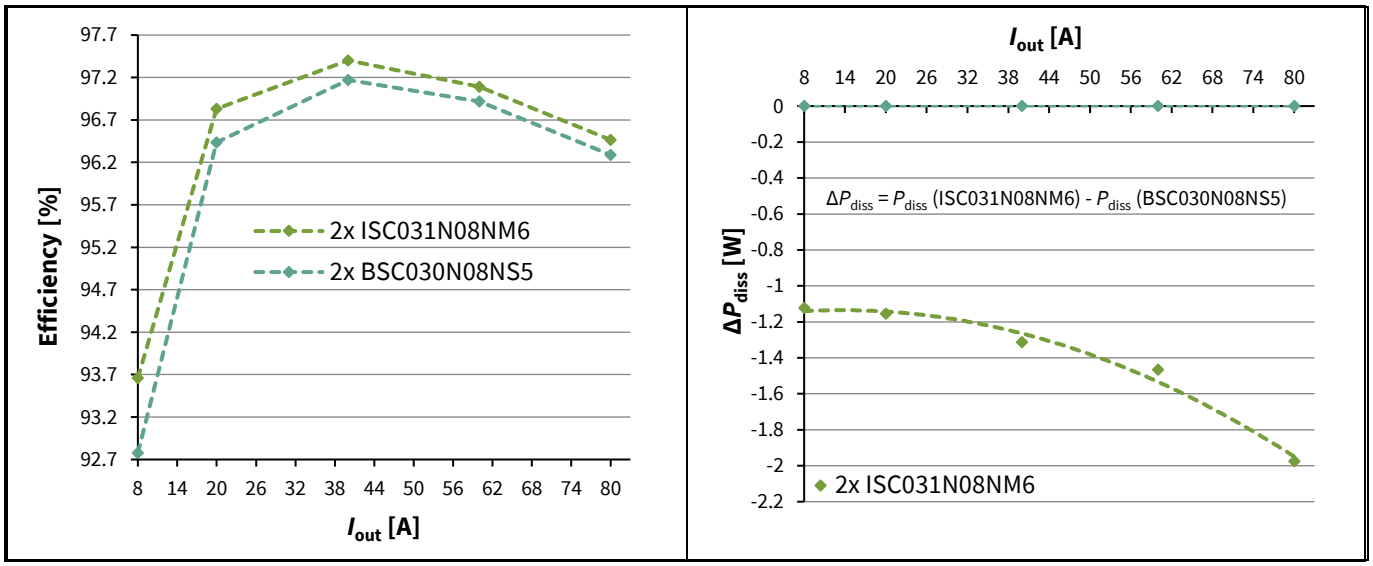


Figure 17 Efficiency and total ΔP_{diss} comparison at V_{in} = 54 V. Reference DUT is Infineon OptiMOS™ 5 80 V BSC030N08NS5. Legend entries report the number of DUTs used in each full-bridge position.

The significant improvement recorded in specific on-state resistance of the new-generation technology allows the replacement of the original two paralleled MOSFETs on the primary side by just one new-generation device with halved $R_{DS(on),max}$ of 1.45 mΩ.

The performance comparison against OptiMOS™ 6 ISC014N08NM6 (one DUT/each position of the FB, for a total of four devices) and OptiMOS™ 5 BSC030N08NS5 (two paralleled DUTs/each position of the FB, for a total of eight devices) is given. The efficiency curves, and power dissipation curves (relative to the reference DUT BSC030N08NS5 from the previous-generation OptiMOS™ 5) are reported in Figure 18.

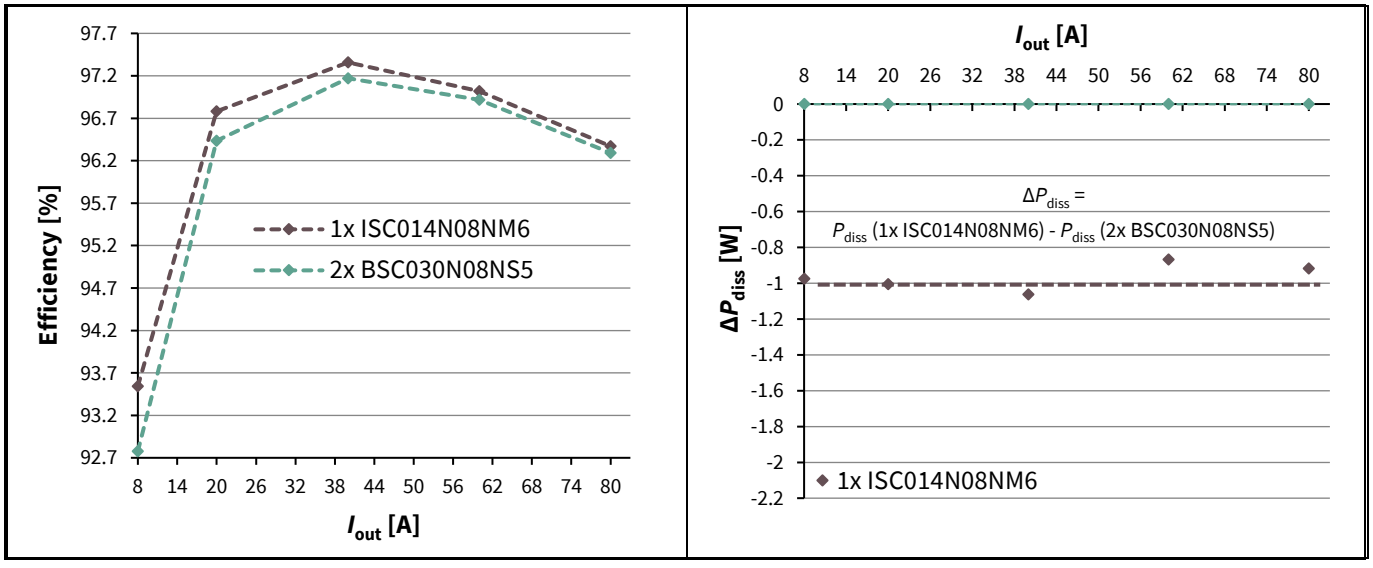


Figure 18 Efficiency and ΔP_{diss} comparison at V_{in} = 54 V. Reference DUT is Infineon OptiMOS™ 5 80 V BSC030N08NS5

The efficiency plots in Figure 17 and Figure 18 demonstrate the gain in performance delivered when OptiMOS™ 6 80 V is used in place of the predecessor technology, in a typical 4:1 LLC DCX IBC.

A gain in efficiency of up to ~1 percent is recorded at light-load conditions, as a direct consequence of the better FOM of the new OptiMOS™ 6 technology. The ~40 percent lower (typ.) Q_g would yield a corresponding reduction in the power consumption from the auxiliary bias supply.

At nominal line voltage, the full-load efficiency gain is up to a remarkable ~0.17 percent, in spite of the slightly higher $R_{DS(on)}$ compared with the OptiMOS™ 5.

ZVS on the primary side occurs thanks to the transformer magnetizing current i_m that forces a transfer of charge, on each full-bridge leg, between the output capacitances of the MOSFETs. Every time C_{oss} is either charged or discharged, a large portion of the magnetizing current i_m passes through R_{oss}, as previously illustrated in Section 1.3.4: Output charge figure-of-merit FOMoss and Ross. As R_{oss} losses happen because of the commutation of the devices, they can be somehow interpreted as an additional switching loss mechanism. OptiMOS™ 6 technology comes with a dramatic reduction in R_{oss} value. In ZVS topologies, such as the LLC, this device property helps to achieve a significant reduction in the switching losses, as turns to be evident from the efficiency plots in Figure 17 and Figure 18. Reduction in switching losses achieved by OptiMOS™ 6 drives better efficiency across all the line and load conditions.

The same (typ.) value for the output charge Q_{oss} = 73 nC characterize both ~3 mΩ DUTs from the previous and latest OptiMOS™ generations. This also means that the magnetic energy required to deplete the output capacitance and achieve ZVS is the same for the two DUTs, i.e., duty-cycle and peak value for the magnetizing current are the same for the two tests. At the same time, R_{oss} losses are greatly reduced for OptiMOS™ 6 by a corresponding reduction in the fieldplate parasitic resistance.

OptiMOS™ 6 allows the replacement of the original two paralleled MOSFETs with a single device, bringing price and performance benefits.

The BiC device in the OptiMOS™ 6 80 V SuperSO8 portfolio, ISC014N08NM6, coming with the industry's lowest $R_{DS(on),max}$ of 1.45 mΩ, has a slightly higher value for the output charge of Q_{oss} = 159 nC compared to two OptiMOS™ 5 BSC030N08NS5 ($Q_{oss,tot}$ = 2 x 73 nC = 146 nC). This requires slightly extending the dead time duration to allow the ZVS to happen. It also shows higher Q_g when compared to 2 x ISC031N08NM6, slightly offsetting the the gain in light load compared to the paralleled OptiMOS™ 6 solution. As the losses are not split between two paralleled devices, a flattening in the ΔP_{diss} is recorded from mid to full load compared to the solution which uses two OptiMOS™ 6 ISC031N08NM6. Nevertheless, it achieves better efficiency across the entire line and load conditions over the OptiMOS™ 5 solution, as well as lower case temperature despite the single device placement.

By replacing two paralled devices with just one, OptiMOS™ 6 enables saving more than 120 mm^2 or 50 percent in PCB real estate allocated for the primary FB, with further margin for performance improvement by design optimization.

To complement the analysis of the value proposition in the application, efficiencies are also given for minimum input voltage V_{in} = 42 V (Figure 19 and Figure 20). Such results are again in agreement with the foregoing statements.

Experimental results highlight how the new Infineon OptiMOS™ 6 80 V family – bringing $R_{DS(on)}$ and FOM improvement, as well as a novel device structure reducing the R_{oss} – shines in resonant applications such as high-frequency DC-DC, where such parameters are of primary importance to achieve best efficiency across the whole load range. OptiMOS™ 6 80 V also drives price/performance improvements by avoiding or reducing paralleling of devices.

3.1.4.3 Efficiency comparison at V_{in} = 42 V

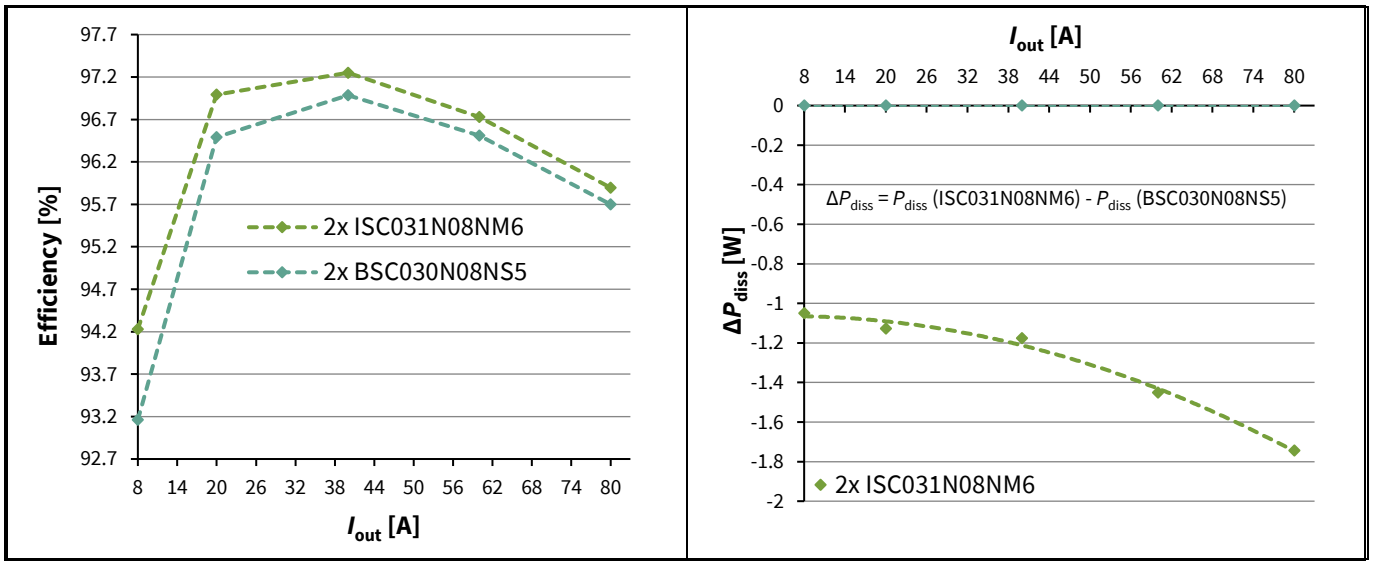


Figure 19 Efficiency and total ΔP_{diss} comparison at V_{in} = 42 V. Reference DUT is Infineon OptiMOS™ 5 80 V BSC030N08NS5. Legend entries report the number of DUTs used in each full-bridge position.

Below is the comparison against OptiMOS™ 6 ISC014N08NM6 (one DUT/each position of the FB, for a total of four devices) and OptiMOS™ 5 BSC030N08NS5 (two paralleled DUTs/each position of the FB, for a total of eight devices).

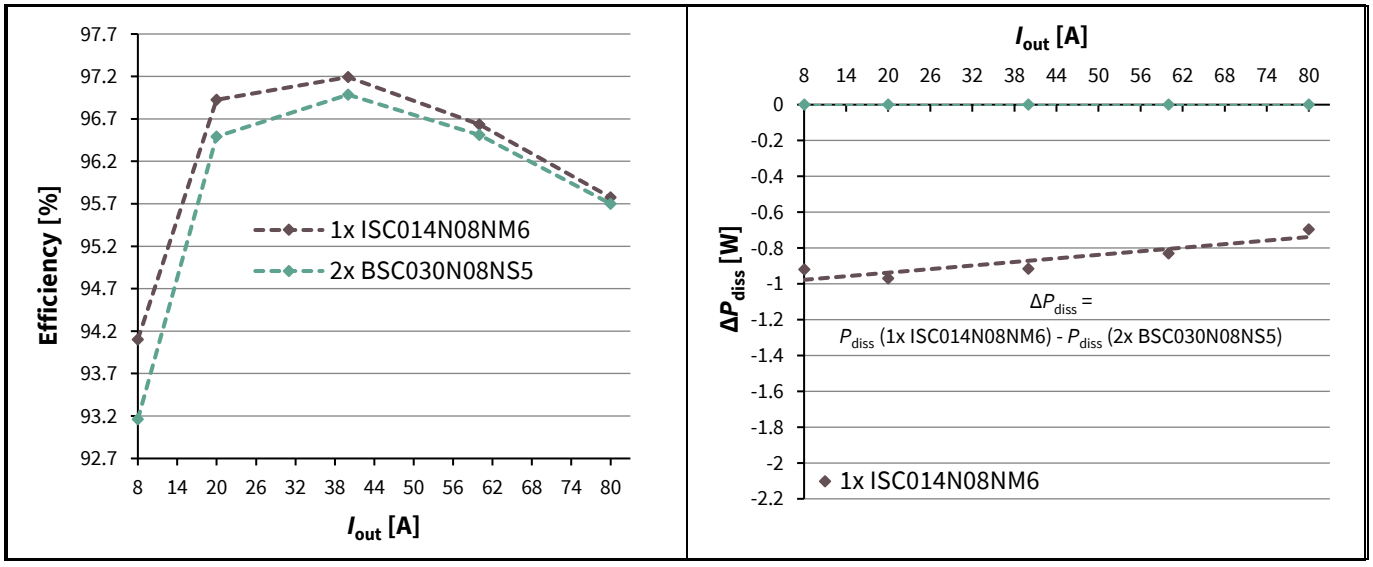


Figure 20 Efficiency and ΔP_{diss} comparison at V_{in} = 42 V. Reference DUT is Infineon OptiMOS™ 5 80 V BSC030N08NS5

3.1.4.1 Thermal pictures at V_{in} = 54 V

Along with efficiency tests, thermal data were also acquired, using the test setup introduced in Section 3.1.3 Test setup description. Temperatures were measured across the entire brick board by using a thermal camera, after thermal steady-state was reached. In Figure 21 and Figure 22 the temperatures recorded on the primary

MOSFETs are compared for the different DUTs. Measurements are provided for 600 LFM (3 m/s) airflow, T_A = 25°C.

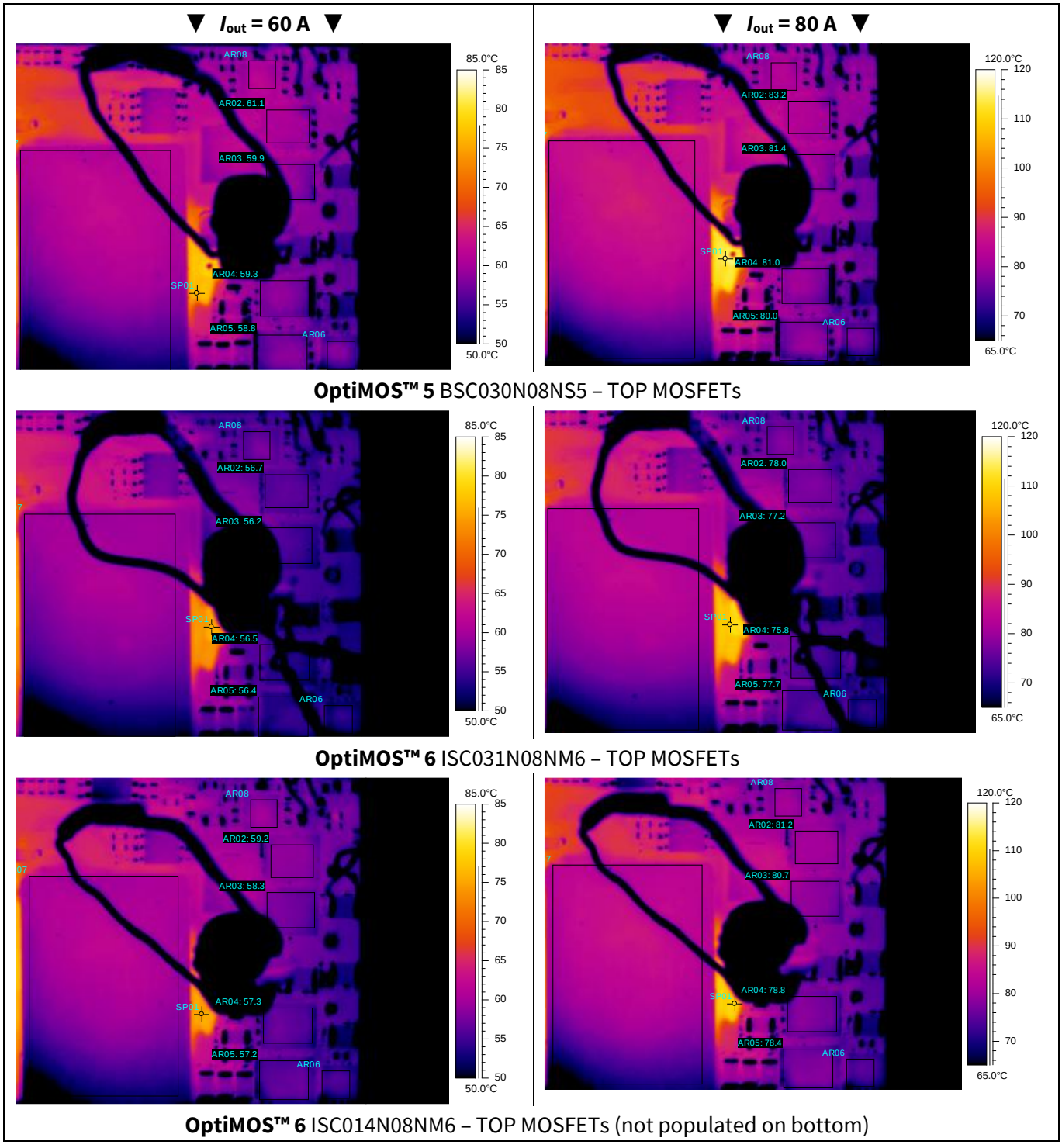


Figure 21 Thermal pictures at V_{in} = 54 V

Thermal measurements reflect the overall efficiency improvement enabled by the OptiMOS™ 6, with up to ~5°C lower case temperature recorded on the primary MOSFETs. Despite the area penalty, the solution with BiC OptiMOS™ 6 ISC014N08NM6, which avoids paralleling, still records a slightly lower-case temperature compared to the paralleled solution using OptiMOS™ 5.

Table 7 Maximum recorded case temperature comparison at V_{in} = 54 V

DUT / Output current I_{out}	Infineon OptiMOS™ 5 80 V, 3 mΩ BSC030N08NS5 (2 DUTs/pos)	Infineon OptiMOS™ 6 80 V, 3.1 mΩ ISC031N08NM6 (2 DUTs/pos)	Infineon OptiMOS™ 6 80 V, 1.45 mΩ ISC014N08NM6 (1 DUT/pos)
60 A	61.1°C	56.7°C	59.2°C
80 A	83.2°C	78.0°C	81.2°C

While the primary MOSFETs show lower temperatures in all the line and load conditions, the advantage is also reflected at system level, with reduced thermal stress across gate drivers and onboard bias regulator.

Achieving lower temperatures is of primary importance for system reliability as the mean time between failures (MTBF) is ultimately dependent on the temperature by an exponential law.

Reducing power losses – the result of optimizations brought at product level such as lower $R_{DS(on)}$, low Q_g and low Q_{oss} – is a fundamental measure to keep the power density increasing, while at the same time meeting the demanding reliability requirements imposed on power DC-DC modules. The new OptiMOS™ 6 80 V family enables the trend toward ultimate-efficiency power conversion, helping power system designers meet the design requirements, and making life easier.

3.1.5 Operation waveforms

To conclude the comparison, waveforms were acquired for the different DUTs in the Infineon 1 kW, 4:1 FB LLC isolated quarter-brick converter REF_1KW_LLC_XDPP1100.
Primary-side steady-state waveforms (gate-source and drain-source voltages) were acquired for Infineon OptiMOS™ 5 BSC030N08NS5 and the new OptiMOS™ 6 ISC031N08NM6 at nominal line voltage (V_{in} = 54 V) and 80 percent of $P_{out,TDP}$ (I_{out} = 60 A). Waveforms are overlaid for easy comparison.

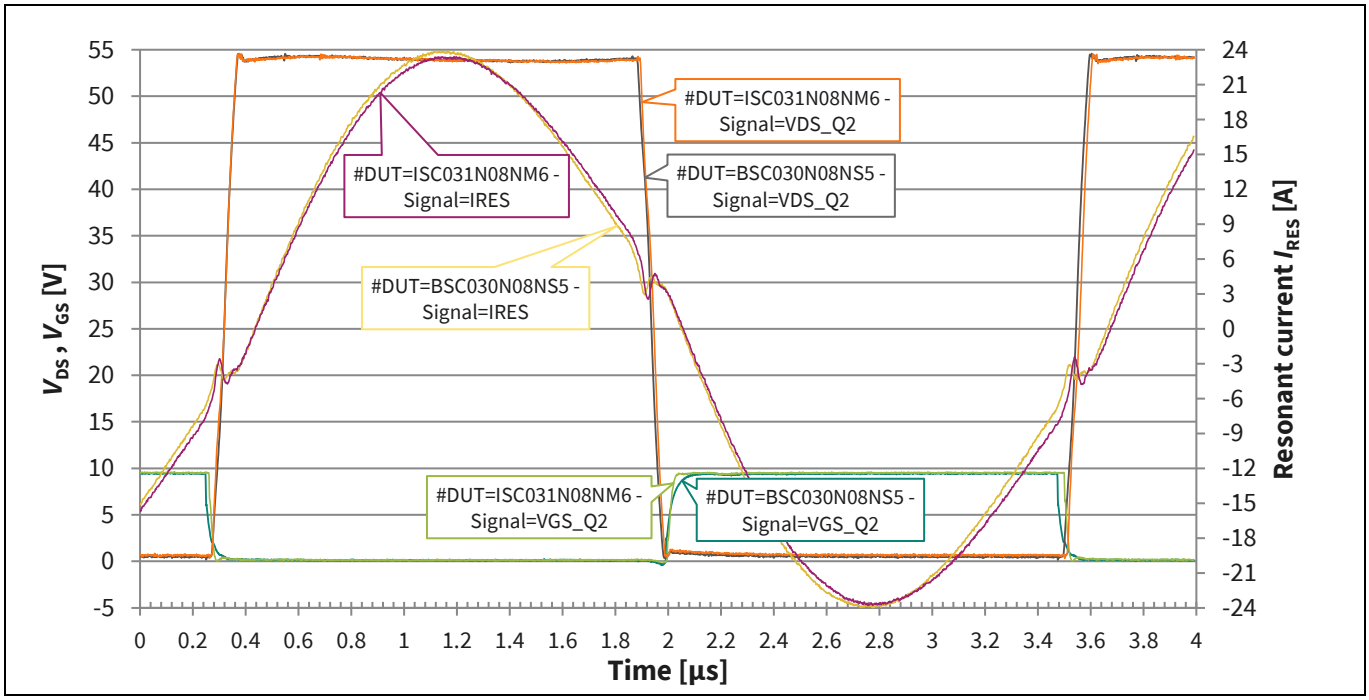


Figure 22 Overview of a switching cycle. V_{in} = 54 V, I_{out} = 60 A

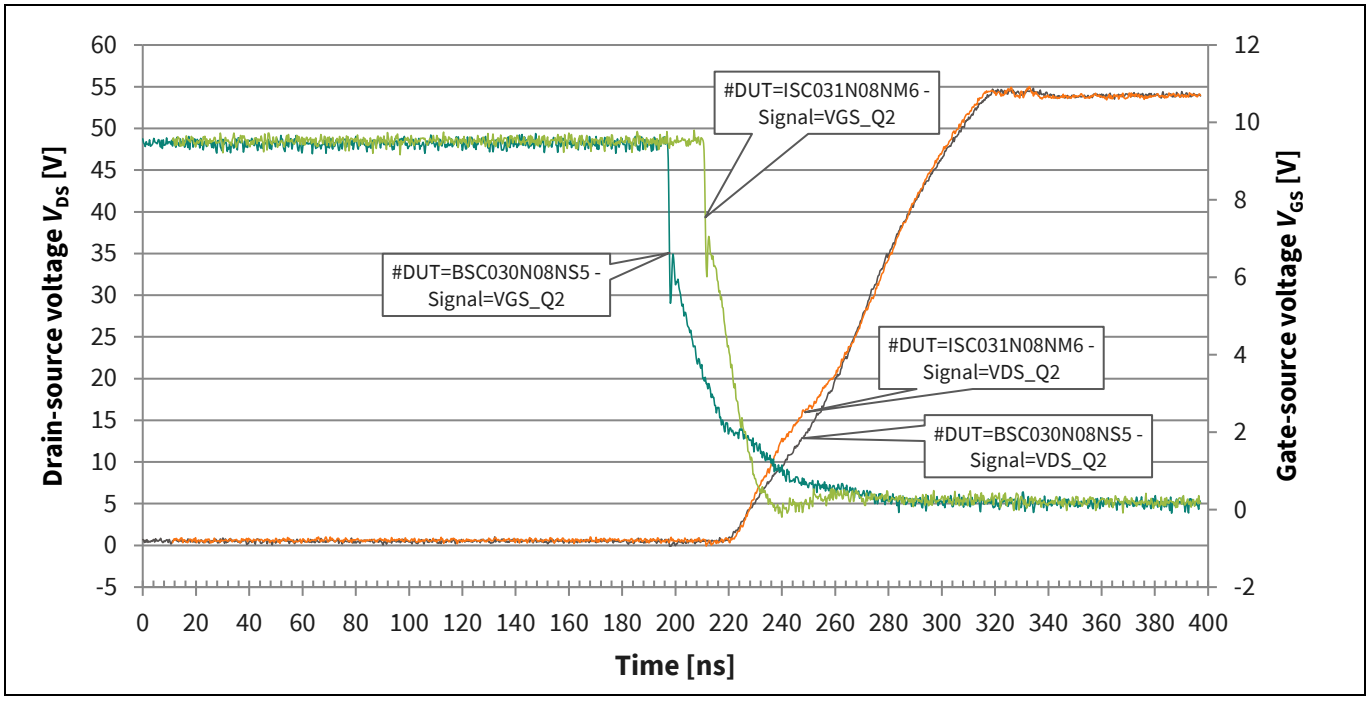


Figure 23 **Turn-off transition. V_{in} = 54 V, I_{out} = 60 A**

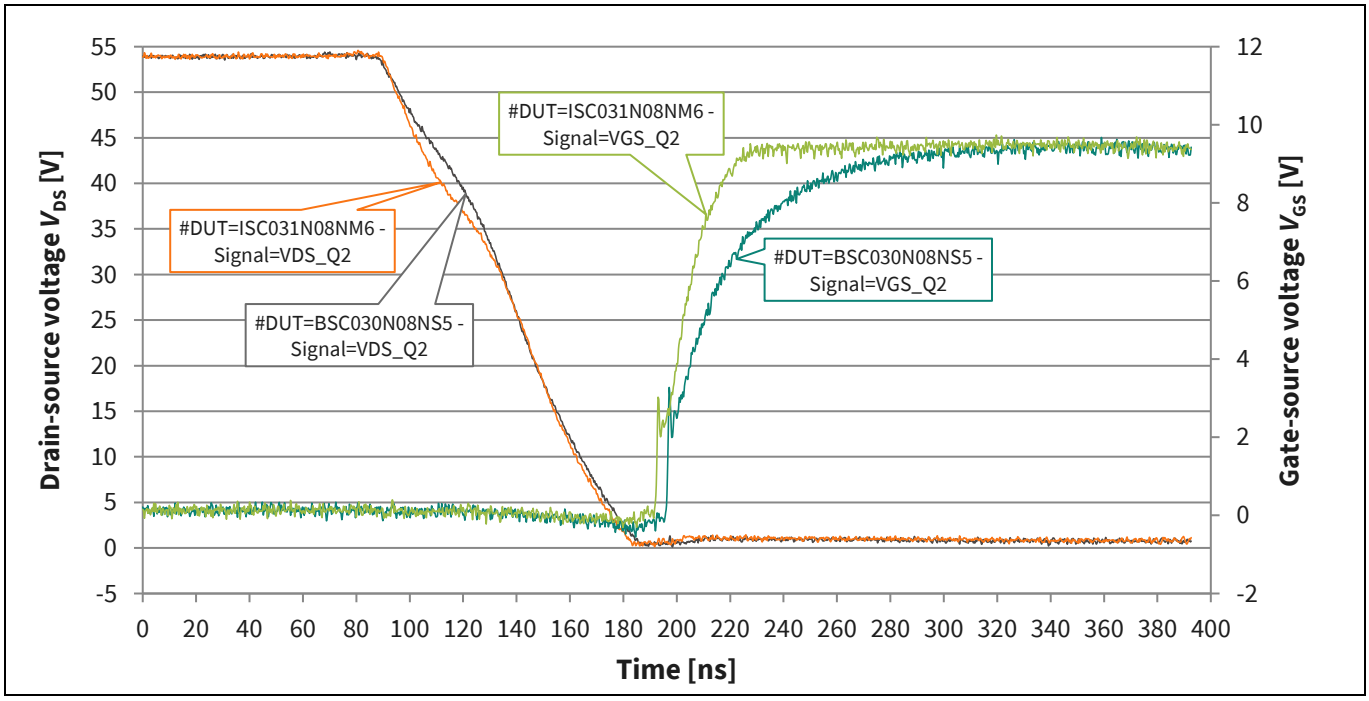


Figure 24 **Turn-on transition. V_{in} = 54 V, I_{out} = 60 A**

Dead times are finely adjusted to achieve the same body diode conduction time for the two DUTs. The drain-source voltage waveforms match closely, as expected. Minor deviations in the voltage transition waveforms are due to the different shape of the output capacitance of the DUTs. From waveforms it is evident how the ~40 percent improvement in the FOM_g, hence in the total gate charge Q_g, results in a much faster transition of the gate-source voltage. The approximately similar reduction in Q_{gd} helps in lowering the turn-off losses associated with the peak magnetizing current.

3.2 Infineon 600 W FB-CT isolated quarter-brick DC-DC IBC converter for telecom

3.2.1 Introduction

In telecom power systems, an isolated DC-DC IBC is typically employed in the conversion chain, to take a nominal -48 V input and generate a 12 V bus for the downstream point-of-load (PoL) converters. The scheme closely resembles the one illustrated earlier for 48 V data centers (Figure 10), which in turn was inspired by the proven conversion system historically adopted in telecoms.

IBCs usually come as power modules, in a family of standardized form factors and footprints. Brick converters are available from several established manufacturers. The standard defines only the set of mechanical outlines and the footprint for the power modules, while no electrical specifications are given. This means that modules can be designed according to different applications (telecoms, datacoms, etc…), the type of system (-48 V, -60 V) or requirements imposed by the downstream PoLs. Specifically, different power-conversion topologies may be implemented, either unregulated or regulated. Regulated topologies, despite being somewhat less efficient, are usually needed to deal with the universal telecom range, extending from -75 V to -36 V.

In recent years, the quarter-brick format has been affirmed as the industry standard. Most typical power-conversion architectures for IBCs embracing this form factor are isolated and buck-derived; namely the half-bridge and the full-bridge forward-type converters. The full-wave synchronous rectification (SR) stage can either take advantage of a center-tapped transformer design or may be configured as a bridge. The continuous improvement in MOSFET technology in recent years has enabled the power density to increase steadily. Presently an IBC in a standard quarter-brick is typically able to continuously deliver power up to 700 W.

Infineon has developed a fully functional quarter-brick IBC evaluation unit, operating from an input voltage range of 36 to 75 V DC that provides up to 600 W output power. The unit will be introduced in the next section and is used as a testbench to showcase the value proposition of the new OptiMOS™ 6 80 V in a real application.

3.2.2 Test platform description

IBCs are required to provide functional and safety isolation. The Infineon 600 W isolated quarter-brick converter was designed as full-bridge (FB) topology with full-wave center-tapped (CT) SR stage. The transformer turns ratio is 3:1 and the design is regulated by means of an analog control loop.

The FB-CT board was designed as a testing platform, with easy access to probe test points, and easy reworking/replacement of components. The module is equipped with an onboard auxiliary supply to provide the required bias. The quarter-brick unit operates in a variety of thermal environments, and sufficient cooling should be provided to ensure reliable operation.

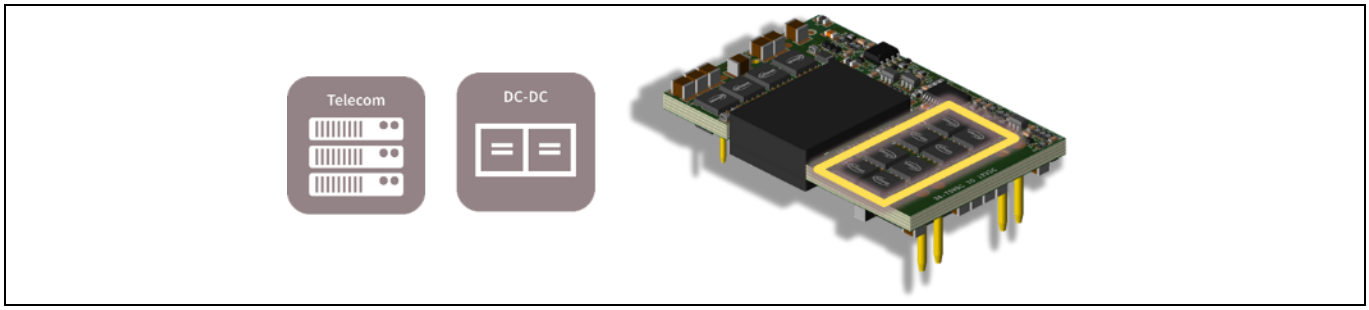


Figure 25 3D view of the Infineon 600 W FB-CT 36 to 75 V to 12 V isolated quarter-brick converter with the SR MOSFETs (DUTs) highlighted

3.2.2.1 Design description and schematics

The schematic diagram for the main power stage of the Infineon 600 W FB-CT 36 to 75 V to 12 V isolated quarter-brick converter is shown in Figure 26.

Main power stage

In the original design of the Infineon 600 W isolated quarter-brick converter, the following products from the Infineon portfolio were selected:

- OptiMOS™ 5 80 V MOSFETs BSC040N08NS5, 4.0 mΩ $R_{DS(on),max}$ in SuperSO8 package (PQFN 5 x 6 mm^2) are used as synchronous rectifiers in the secondary-side center-tap rectifier. The board is designed to fit four devices per position, for a total of eight power MOSFETs. Devices will be replaced and benchmarked with the latest OptiMOS™ 6 80 V power transistors.
- OptiMOS™ 5 100 V MOSFETs BSC050N10NS5, 5.0 mΩ $R_{DS(on),max}$ in SuperSO8 package are used in the primary-side full-bridge, for a total of four power MOSFETs. Also, these devices will be replaced and benchmarked with the latest OptiMOS™ 6 power transistors, in the 100 V voltage class [2].
- EiceDRIVER™ gate driver 2EDL8124G dual-channel junction-isolated gate drivers are used to drive the primary-side bridge, offering differential inputs with built-in hysteresis for inherent shoot-through protection.
- EiceDRIVER™ 2EDN7524G dual-channel, low-side gate drivers are used to drive the synchronous rectifier MOSFETs.

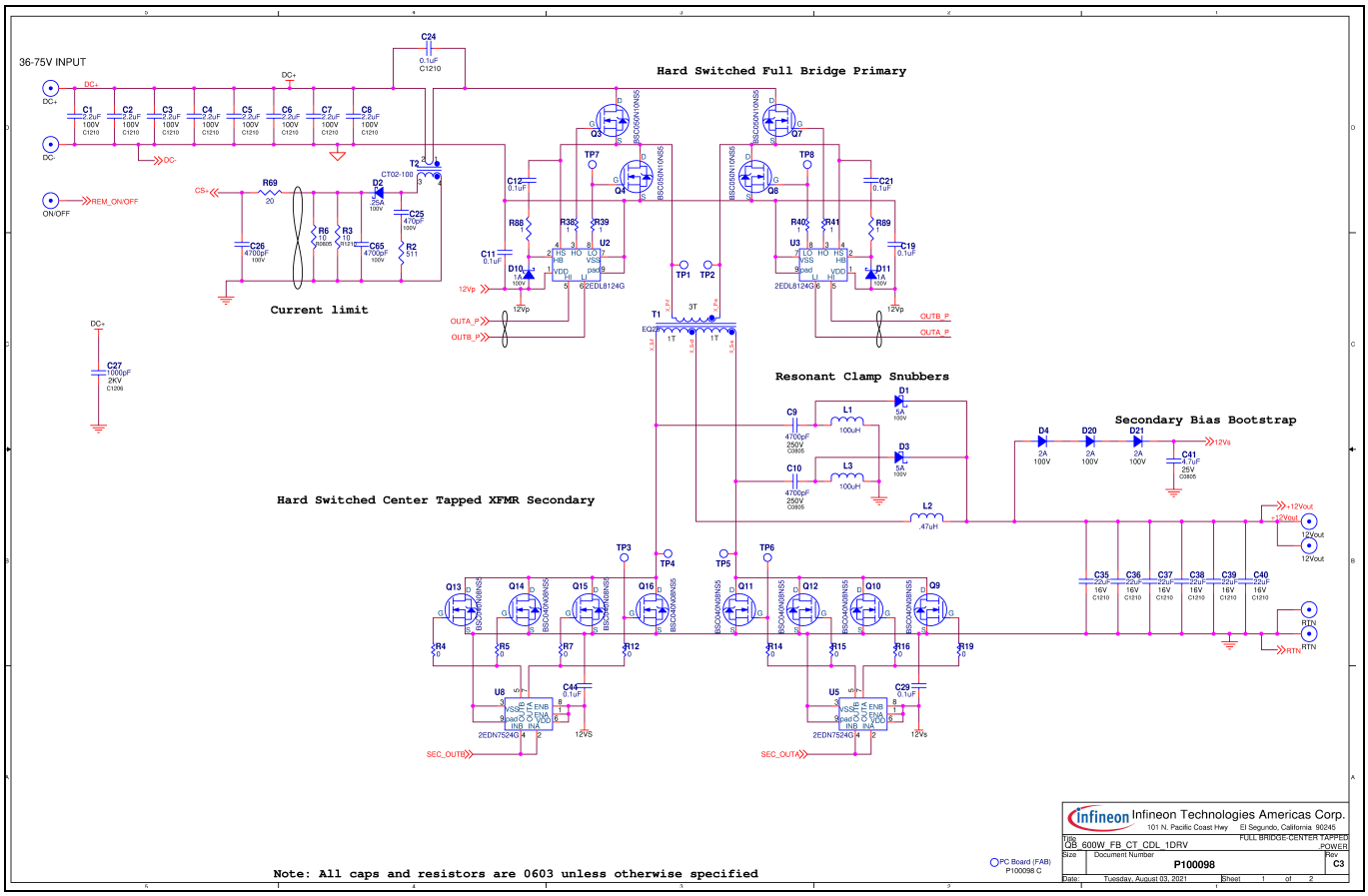


Figure 26 Infineon 600 W FB-CT 36 to 75 V to 12 V isolated quarter-brick converter. Schematic page 1: main power stage.

3.2.2.2 PCB description

Figure 27 shows the placement of the different components and measurement test points on the Infineon FB-CT isolated quarter-brick converter. The outer dimensions of the board are 4.25 in. x 4 in. x 0.87 in. (108 mm x 102 mm x 22 mm). The PCB stackup is 10 layers deep. The internal layers are all 5 oz. copper thickness with the top and bottom layers at 4 oz. copper thickness. The total board thickness is 118 mils (3 mm).

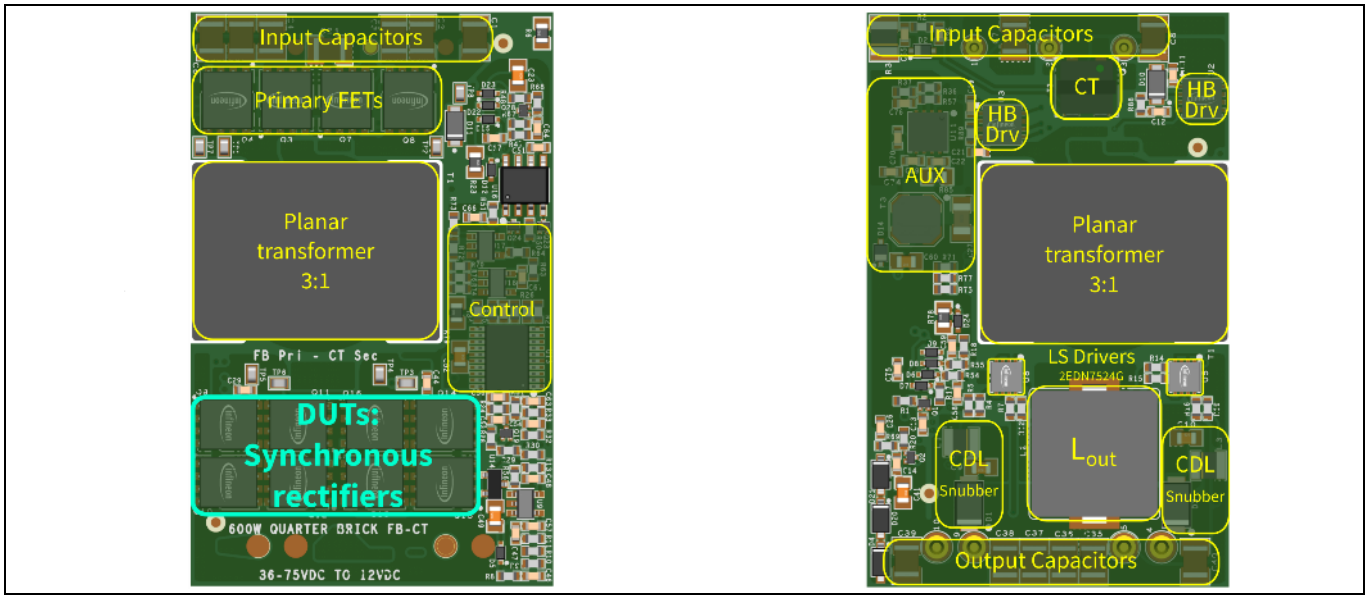


Figure 27 Top and bottom views of the Infineon 600 W FB-CT 36 to 75 V to 12 V isolated quarter-brick converter, where the placement of the most significant components is highlighted.

3.2.2.3 Board specifications

The specifications for the Infineon 600 W FB-CT 36 to 75 V to 12 V isolated quarter-brick converter are shown in Table 8.

Table 8 Specification of the 600 W FB-CT 36 to 75 V to 12 V isolated quarter-brick converter

Parameter	Symbol	Values			Unit	Note/test condition
		Min.	Typ.	Max.		
Operating input voltage	V_{in}	36	48	75	V	
Input current RMS value (V_{out} = 50 V)	$I_{in,RMS}$		16 13 9		A	V_{in} = 36 V, P_{out} = 600 W V_{in} = 48 V, P_{out} = 600 W V_{in} = 75 V, P_{out} = 600 W
Start-up voltage threshold	$V_{in(on)}$	32		36	V	
Minimum operating voltage after start-up	$V_{in(off)}$	29		34	V	
Output voltage set-point	$V_{out,nom}$		12		V	
Output voltage set-point tolerance	$\sigma V_{out,nom}$	-3		+3	%	
Output power (TDP)	$P_{out,TDP}$	0		600	W	v_{air} = 3 m/s
Efficiency	η		95.4		%	V_{in} = 48 V, P_{out} = 75% $P_{out,TDP}$
Power dissipation	P_{diss}		33		W	V_{in} = 48 V, P_{out} = $P_{out,TDP}$
Recommended output capacitance	C_{out}	1000	1800	150000	µF	

Parameter	Symbol	Values			Unit	Note/test condition
		Min.	Typ.	Max.		
Switching frequency	f_{sw}		250		kHz	
Airflow velocity	v_{air}		600 3		LFM m/s	
Functional isolation voltage	V_{iso}		1500		V	

3.2.3 Test setup description

The test setup is described here in detail. The actual test setup is shown in Figure 28.

3.2.3.1 Description of the test setup

The measurement setup precisely follows that already described earlier in Section 3.1.3.1: Description of the test setup, with the difference that the main DC power supply must be able to provide at least 80 V DC. The actual test setup is shown in Figure 28.

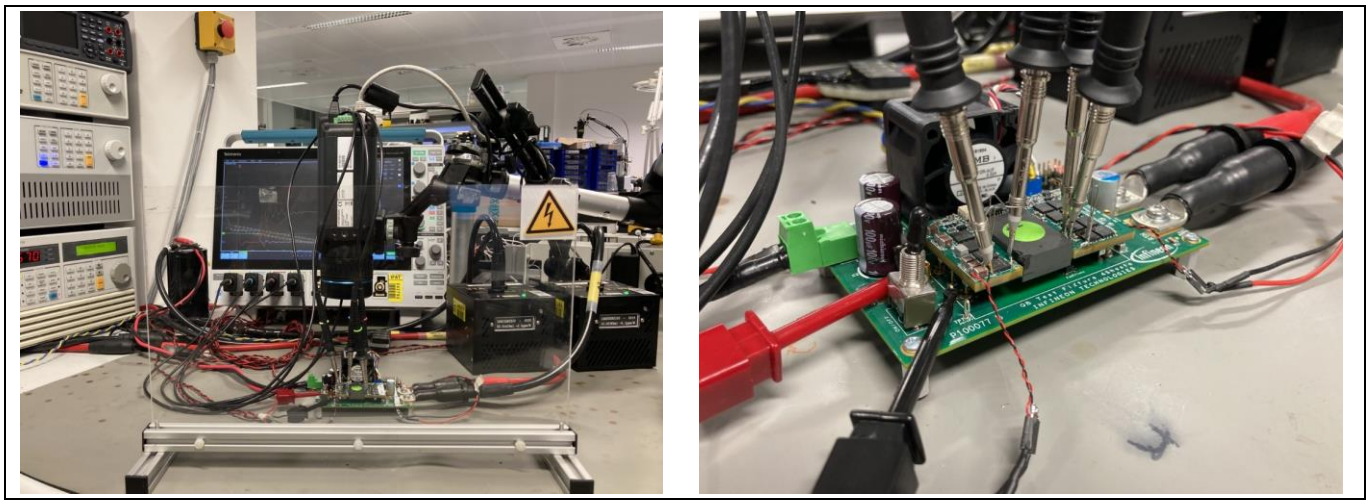


Figure 28 Actual test setup

3.2.4 Efficiency test

3.2.4.1 Introduction

Efficiency tests were performed for the Infineon 600 W FB-CT 36 to 75 V to 12 V isolated quarter-brick converter, using the test setup introduced in section 3.1.3 Test setup description.

Efficiencies were captured for three different configurations of the secondary center-tap full-wave rectifier, featuring three different DUTs. The DUTs came with either a SuperSO8 (PQFN 5 x 6 mm^2) or a Shrinked-SuperSO8 (S3O8 or PQFN 3.3 x 3.3 mm^2) surface-mount package.

Only the synchronous rectifier MOSFETs change across the tests, while everything else was kept unchanged in the brick board and in the whole test setup. All the tests were carried out on the very same brick unit, and timings were adjusted for fair comparison of the DUTs.
A summary of the DUTs and their position is given in Table 9.

Table 9 Devices under test – refer to schematic file reported in Figure 26

DUTs	DUT #1	DUT #2	DUT #3
SR MOSFETs: Q9…Q16	**Infineon OptiMOS™ 5 80 V, 4 mΩ** BSC040N08NS5	**Infineon OptiMOS™ 6 80 V, 5.3 mΩ** ISZ053N08NM6	**Infineon OptiMOS™ 6 80 V, 3.1 mΩ** ISC031N08NM6
Package	PQFN 5 x 6 mm²	PQFN 3.3 x 3.3 mm²	PQFN 5 x 6 mm²
DUTs per each center-tap rectifier position	4	4	3

3.2.4.2 Efficiency comparison at V_{in} = 48 V

Table 10 summarizes the efficiencies acquired at nominal input voltage (V_{in} = 48 V) for the different DUTs. The efficiency is measured at 600 LFM (3 m/s) airflow, T_A = 25°C and captured after thermal steady-state is reached. The efficiency curves and system total power dissipation curves (relative to the reference DUT BSC040N08NS5 from the previous-generation OptiMOS™ 5) are reported in Figure 29.

Table 10 Measured efficiency (%) at nominal input voltage V_{in} = 48 V

DUT / Output current I_{out}	Infineon OptiMOS™ 5 80 V, 4 mΩ BSC040N08NS5 PQFN 5 x 6 mm² (4 DUTs/pos)	Infineon OptiMOS™ 6 80 V, 5.3 mΩ ISZ053N08NM6 PQFN 3.3 x 3.3 mm² (4 DUTs/pos)	Infineon OptiMOS™ 6 80 V, 3.1 mΩ ISC031N08NM6 PQFN 5 x 6 mm² (3 DUTs/pos)
5 A	87.65	88.83	88.35
12.5 A	92.94	93.57	93.31
25 A	95.13	95.50	95.40
37.5 A	95.39	95.65	95.64
50 A	94.88	95.08	95.18

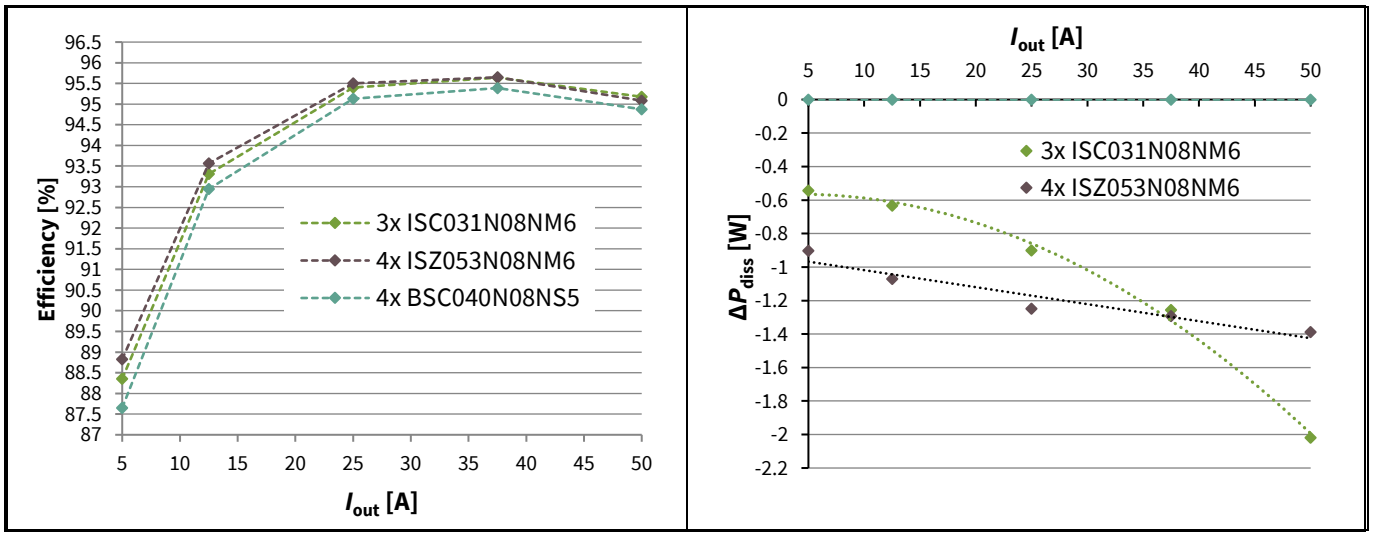


Figure 29 Efficiency and total ΔP_{diss} comparison at V_{in} = 48 V. Reference DUT is Infineon OptiMOS™ 5 80 V BSC040N08NS5. Legend entries report the number of DUTs used in each center-tap leg.

The significant improvement in specific on-state resistance and FOMs recorded by the new OptiMOS™ 6 technology allows the replacement of the original four paralleled OptiMOS™ 5 SR MOSFETs in PQFN 5 x 6 mm² by either:

1. Four OptiMOS™ 6 devices in a smaller package, PQFN 3.3 x 3.3 mm², with the industry's best $R_{DS(on),max}$ of 5.3 mΩ.

   This enables saving more than 150 mm² or 63 percent in PCB real estate allocated for the SRs, with further margin for performance improvement by design optimization. The compact PQFN 3.3 x 3.3 mm² package offers enhanced layout flexibility for a more effective termination of transformer windings. This results in a substantial reduction in conduction losses, which are indeed relevant given the high RMS value of the secondary current.

2. Three OptiMOS™ 6 devices in the same package and lower $R_{DS(on),max}$ of 3.1 mΩ.

   In this case, OptiMOS™ 6 enables moving to lower $R_{DS(on)}$, without impacting the light-load efficiency thanks to the ~40 percent improved FOMs. At the same time, it is possible to save cost and 25 percent of PCB real estate.

In both cases, the efficiency plots in Figure 29 demonstrate that the new Infineon OptiMOS™ 6 80 V delivers a valuable gain in performance when used in a typical telecom DC-DC quarter-brick intermediate bus converter. A gain in efficiency of up to ~1.2 percent is recorded at light-load conditions, and up to 0.3 percent at full-load at the nominal line voltage of 48 V.

In a loss breakdown, the main contributions at light load are the losses associated with the energy stored in the output capacitance of the SR MOSFETs. For every switching cycle, MOSFET output capacitance has to be charged, storing energy in the amount of E_{oss}. Part of this energy is recovered and delivered to the load prior the next freewheeling phase, while energy in the amount of $E_{diss} = Q_{oss}V_s - E_{oss}$ is lost in the process. The power dissipated in the process is then proportional to Q_{oss}, the switching voltage and the switching frequency f_{sw}. MOSFETs with a low value of the output charge Q_{oss} are then preferred in the application. OptiMOS™ 6 ISZ053N08NM6 shines in the application, with ~20 percent less Q_{oss} than the previous-generation device.

With OptiMOS™ 6 ISZ053N08NM6, a ~50 percent lower (typ.) Q_g with respect to the previous-generation device yields a corresponding reduction in power consumption from the auxiliary bias supply.

At high output currents, conduction losses gain most of the share, and MOSFET $R_{DS(on)}$ is the parameter that impacts most on the conversion efficiency. In addition, there are losses associated with the reverse recovery of the MOSFET body diode, as the value for the reverse recovery charge Q_{rr} is load dependent. Despite the ~30 percent higher $R_{DS(on)}$ compared to the previous-generation DUT, OptiMOS™ 6 ISZ053N08NM6 delivers higher efficiency in the whole load range (with +0.2 percent gain at full load), thanks to an overproportionate reduction in the switching losses, possible with the improvement recorded in FOMs.

The solution which uses four OptiMOS™ 6 ISZ053N08NM6 in place of the previous-generation devices is clearly optimal for this 600 W converter. The solution with three OptiMOS™ 6 ISC031N08NM6 achieves an extra +0.1 percent gain in efficiency at full load, but at the expense of slightly higher switching losses, which affect the light-load efficiency. Nevertheless, it achieves better efficiency across entire line and load conditions over the OptiMOS™ 5 solution, as well as lower case temperature. This second solution is to be preferred when targeting higher-power designs.

To complement the analysis of the value proposition in the application, efficiencies are also given for V_{in} = 36 V and 60 V. Such results are again in agreement with the foregoing statements.

3.2.4.3 Efficiency comparison at V_{in} = 36 V and V_{in} = 60 V

Table 11, Table 12, and Figure 30 summarize the efficiencies acquired at low-/high-line (-48 V system) for the different DUTs. Efficiency is measured at 600 LFM (3 m/s) airflow, T_A = 25°C at thermal steady-state.

Table 11 Measured efficiency (%) at nominal input voltage V_{in} = 36 V

DUT / Output current I_{out}	Infineon OptiMOS™ 5 80 V, 4 mΩ BSC040N08NS5 PQFN 5 x 6 mm² (4 DUTs/pos)	Infineon OptiMOS™ 6 80 V, 5.3 mΩ ISZ053N08NM6 PQFN 3.3 x 3.3 mm² (4 DUTs/pos)	Infineon OptiMOS™ 6 80 V, 3.1 mΩ ISC031N08NM6 PQFN 5 x 6 mm² (3 DUTs/pos)
5 A	89.28	90.34	89.89
12.5 A	94.34	94.84	94.67
25 A	95.72	95.99	95.95
37.5 A	95.63	95.80	95.85
50 A	94.96	95.03	95.19

Table 12 Measured efficiency (%) at nominal input voltage V_{in} = 60 V

DUT / Output current I_{out}	Infineon OptiMOS™ 5 80 V, 4 mΩ BSC040N08NS5 PQFN 5 x 6 mm² (4 DUTs/pos)	Infineon OptiMOS™ 6 80 V, 5.3 mΩ ISZ053N08NM6 PQFN 3.3 x 3.3 mm² (4 DUTs/pos)	Infineon OptiMOS™ 6 80 V, 3.1 mΩ ISC031N08NM6 PQFN 5 x 6 mm² (3 DUTs/pos)
5 A	85.26	85.93	85.87
12.5 A	91.14	91.88	91.55
25 A	94.02	94.46	94.32
37.5 A	94.50	94.86	94.80
50 A	94.00	94.32	94.38

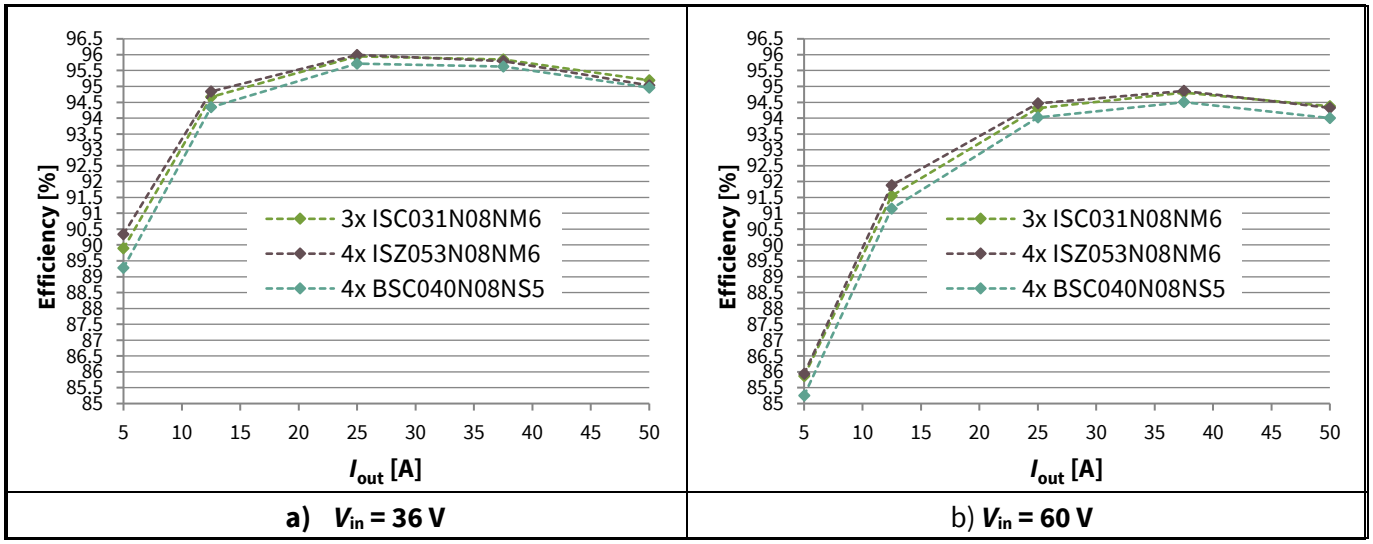


Figure 30 Efficiency comparison at V_{in} = 36 V (a) and 60 V (b). Legend entries report the number of DUTs used in each center-tap leg.

3.2.4.1 Complete OptiMOS™ 6 (80 V + 100 V) system solution

To prove the value proposition of the new OptiMOS™ 6 technolgy, also already available in 100 V [2], the latest-generation MOSFETs were used on both sides of the converter. On the primary side full-bridge, 100 V MOSFETs are used, whereas MOSFETs from the 80 V family portfolio are used as synchronous rectifiers.

The efficiency comparison against the original system solution, using the established OptiMOS™ 5 technology, is here reported. In the original design of the Infineon 600 W FB-CT quarter-brick converter, OptiMOS™ 5 100 V BSC050N10NS5, with $R_{DS(on),max}$ = 5 mΩ, was selected to be used on the primary full-bridge. As a hard-switched topology, $R_{DS(on)}$ has to be traded for low charges, in order to achieve the best efficiency across line and load.

As is evident from thermal pictures acquired at full load (Figure 32**Error! Reference source not found.**), the hotspot in the converter is localized at the primary MOSFETs, which then limit, for a given thermal budget, the power rating of the converter. It is thus necessary to choose devices with lower $R_{DS(on)}$ to extend the power density or the full-load efficiency. For a given technology, this means increasing the switching losses, at the expense of lower light- to mid-load efficiency. Instead, by moving to the new OptiMOS™ 6 technology, it is possible to relax this trade-off thanks to the better figures-of-merit.

Efficiencies are measured for OptiMOS™ 5 and OptiMOS™ 6 devices in the same test platform, according to Table 13.

Table 13 DUTs chosen from OptiMOS™ 5 and OptiMOS™ 6 80 V and 100 V technologies

Position \ Solution	Original OptiMOS™ 5 solution	Full system solution with latest OptiMOS™ 6 technology
Primary full-bridge (100 V MOSFETs)	**OptiMOS™ 5** BSC050N10NS5 $R_{DS(on),max}$ = 5 mΩ PQFN 5 x 6 mm² (1 DUT/pos)	**OptiMOS™ 6 ISC030N10NM6** $R_{DS(on),max}$ = 3 mΩ PQFN 5 x 6 mm² (1 DUT/pos)
Secondary SRs (80 V MOSFETs)	**OptiMOS™ 5** BSC040N08NS5 $R_{DS(on),max}$ = 4 mΩ PQFN 5 x 6 mm² (4 DUTs/pos)	**OptiMOS™ 5 ISZ053N08NM6** $R_{DS(on),max}$ = 5.3 mΩ PQFN 3.3 x 3.3 mm² (4 DUTs/pos)

Efficiencies were acquired at nominal input voltage (V_{in} = 48 V), with 3 m/s (600 LFM) airflow, T_A = 25°C and at thermal steady-state (Table 14). Efficiencies were captured in the very same brick unit.

Table 14 Efficiencies (V_{in} = 48 V) for full OptiMOS™ 5 and OptiMOS™ 6 80 V + 100 V system solutions

Output current I_{out} \ Efficiency	Original OptiMOS™ 5 solution	Full system solution with latest OptiMOS™ 6 technology
5 A	87.65	88.41 (+0.76%)
12.5 A	92.94	93.32 (+0.36%)
25 A	95.13	95.48 (+0.36%)
37.5 A	95.39	95.74 (+0.35%)
50 A	94.88	95.29 (+0.41%)

The incorporation of the latest OptiMOS™ 6 technologies at 80 V and 100 V drive a noteworthy improvement in the system efficiency across the entire load range. The devices selected from the OptiMOS™ 6 80 V and 100 V product portfolios lead to the best optimization for this 600 W FB-CT quarter brick converter. By system design

optimization, the performance gains achieved through a straightforward drop-in replacement of the previous-generation devices can be further enhanced.

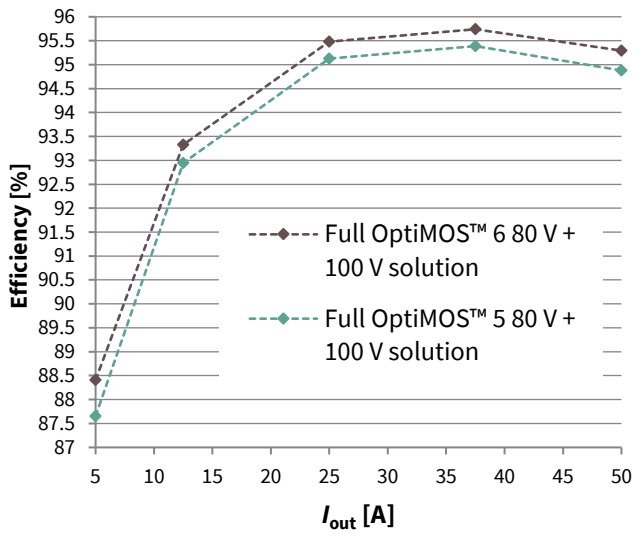
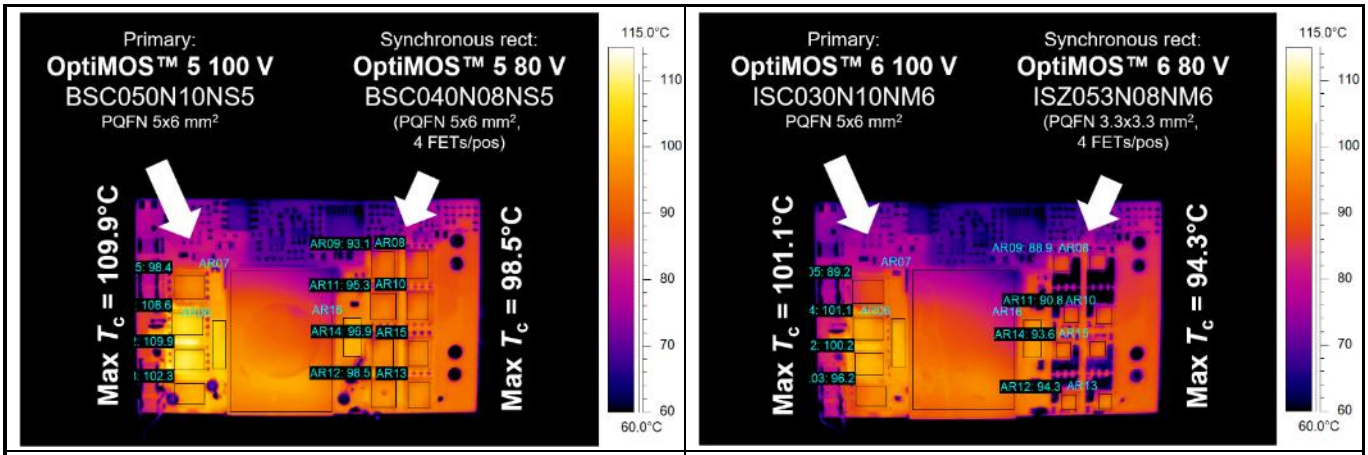




Figure 31 Efficiencies (V_{in} = 48 V) for full OptiMOS™ 5 and OptiMOS™ 6 80 V + 100 V system solutions. Detail of the smaller PQFN 3.3 x 3.3 mm² SRs soldered onto the original PQFN 5x6 footprint.

Advantages also reflect reduced hotspot temperature by ~9°C (on the primary MOSFETs), as well on the SRs, with ~4°C lower temperature. This is despite having moved to the smaller PQFN 3.3 x 3.3 mm² package and to the suboptimal solder joints with the PCB, as the footprint is only partially compatible with the bigger PQFN 5 x 6 mm².



a) Original OptiMOS™ 5 solution | b) Full OptiMOS™ 6 80 V + 100 V solution

Figure 32 Thermal pictures (V_{in} = 48 V) for full OptiMOS™ 5 and OptiMOS™ 6 80 V + 100 V system solutions.

3.2.5 Operation waveforms

To conclude the comparison, waveforms were acquired for the different DUTs in the Infineon 600 W FB-CT isolated quarter-brick converter. Steady-state waveforms (gate-source and drain-source voltages) were acquired for the DUTs at nominal line voltage (V_{in} = 48 V) and 50 percent of $P_{out,TDP}$ (I_{out} = 25 A). Primary-side waveforms are provided for reference. Waveforms are overlaid for the simplest comparison. Transformer-based

DC-DC brick designs commonly employ snubbers or active clamps for the SRs, to absorb the high leakage energy that otherwise will cause large voltage overshoots and – eventually – avalanche. This Infineon FB-CT design uses a resonant (LC+D) regenerative snubber, which is kept unchanged among the tests with different DUTs.

The analog-controlled design relies on a conservative, long dead time of ~85 ns (at this load condition). Effective dead time duration is the same for the two DUTs. OptiMOS™ 6 ISZ053N08NM6 is definitively faster with ~50 percent less $Q_{g(sync)}$ compared to the previous-generation device, as is evident from the faster gate-source voltage transition. Despite the considerably lower value for the output capacitance, OptiMOS™ 6 ISZ053N08NM6 shows a peak drain-source voltage overshoot only ~1.7 V higher than the OptiMOS™ 5 DUT. This can be easily addressed with a minor adjustment in the snubber.

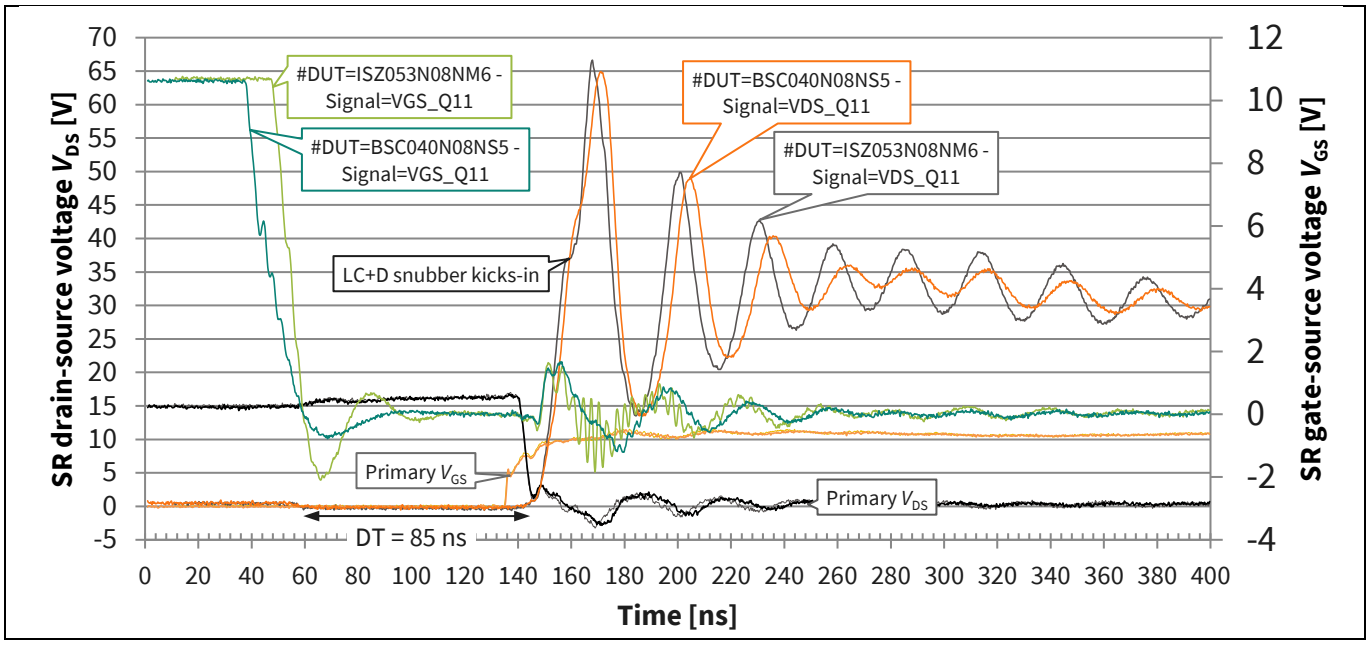


Figure 33 Turn-off transient. V_{in} = 48 V, I_{out} = 25 A

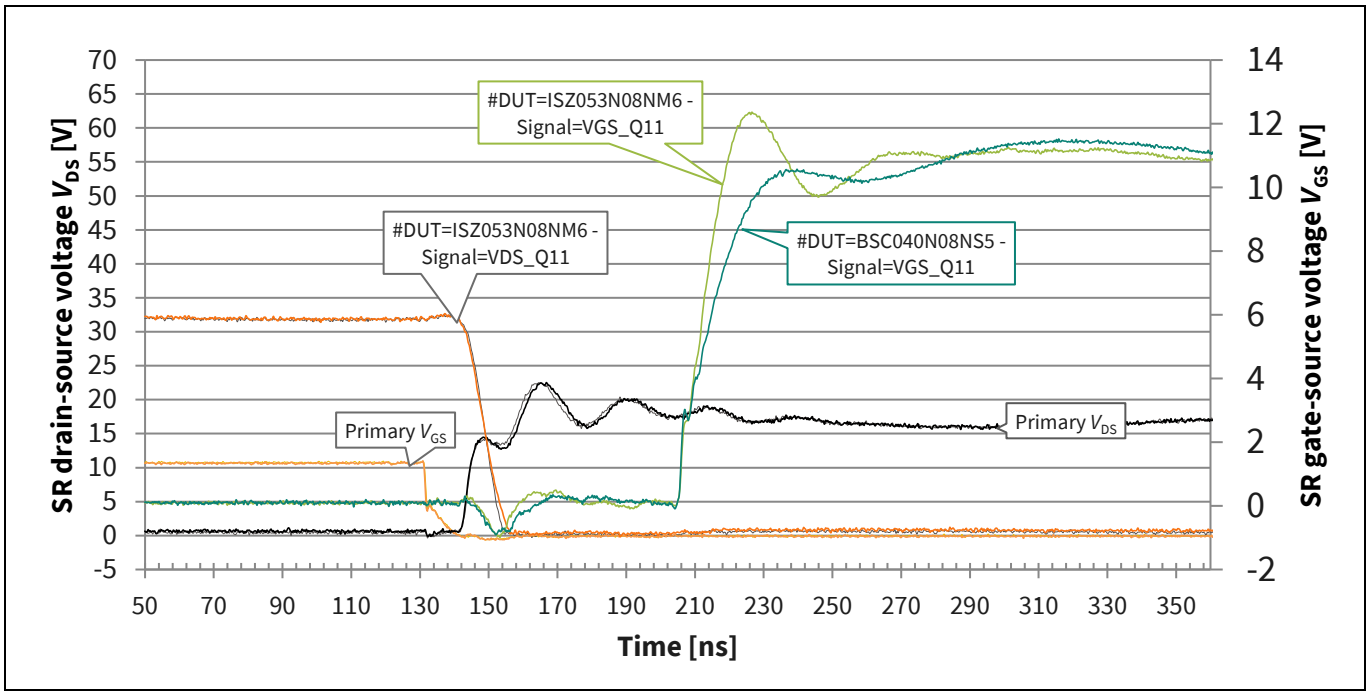


Figure 34 Turn-on transient. V_{in} = 48 V, I_{out} = 25 A

3.3 Infineon 750 W FB-FB quarter-brick DC-DC converter for RFPA application

3.3.1 Introduction

The next stage in mobile network development is 5G, offering higher data capacity and faster response times, enabling new applications in a connected society. To support this, traditional architectures of mobile networks have changed dramatically, in both core networks and radio access networks (RANs).

In the first phase of the rollout, the majority of the cellular base stations (BTSs) will be operated at sub-6 GHz frequencies. Massive MIMO arrays at sub-6 GHz dictate the demand for small form-factor, highly efficient power amplifiers (RFPAs) to be used. GaN HEMT-based RFPAs are preferred for 5G base stations due to their high-power density and efficiency.

Supplying GaN RFPAs poses several challenges for the DC-DC converter. GaN RFPAs typically require a 50 V supply that needs to be regulated starting from the usual telecom -48 V bus. Different conversion approaches and topologies have been proposed to meet the requirements. Often DC-DC converters aiming at RFPA come in the form of standard brick power modules, from half- to eighth-brick form factors. The Infineon evaluation board REF_750W_FBFB_50V_QB aims to address the application requirements by means of a single-stage, isolated topology, in quarter-brick form factor. The digitally controlled power supply includes advanced protections for the most reliable operation of the power module.

The unit will be introduced in the next section and is used as a testbench to showcase the value proposition of the new OptiMOS™ 6 80 V in hard-switching in a real application.

3.3.2 Test platform description

The Infineon evaluation board REF_750W_FBFB_50V_QB operates from an input voltage range of -60 to -36 V DC. The nominal output voltage is +50 V, with a maximum output current of 15 A, corresponding to a maximum output power of 750 W. The board is non-baseplated, and is intended to be operated under forced airflow of approximately 3 m/s. The output is galvanically isolated from the input, allowing versatile grounding configurations.

The 750 W isolated DC-DC converter consists of full-bridge topology with full-wave synchronous rectification, switching at 140 kHz. The isolation transformer of the main power stage provides a 3:5 step-up ratio to regulate the +50 V output rail during low-line conditions of -36 V.

The FB-FB board was designed as a testing platform, with easy access to probe test points, and easy reworking/replacement of components. The module is equipped with an onboard auxiliary supply to provide the required bias. The quarter-brick unit operates in a variety of thermal environments, and sufficient cooling should be provided to ensure reliable operation.

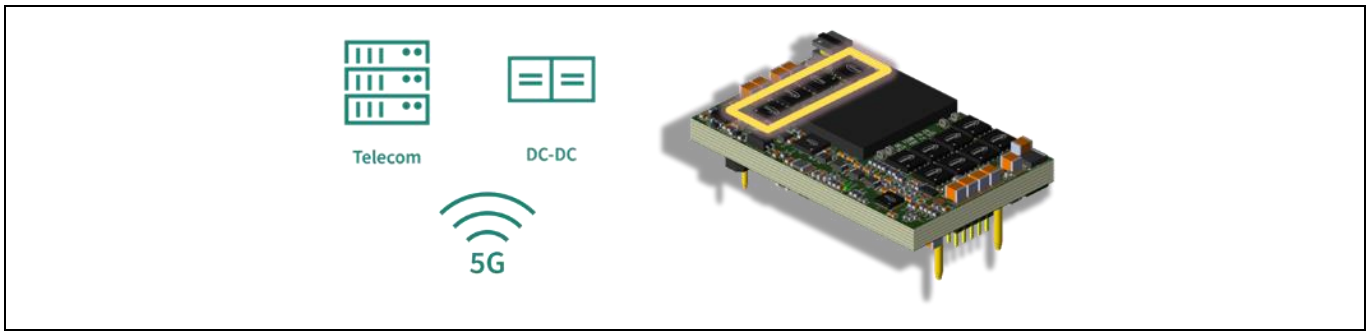


Figure 35 3D view of the Infineon 750 W FB-FB quarter-brick converter REF_750W_FBFB_50V_QB with the primary full-bridge MOSFETs (DUTs) highlighted.

3.3.2.1 Design description and schematics

The schematic diagram for the main power stage of the Infineon 750 W FB-FB isolated quarter-brick converter REF_750W_FBFB_50V_QB is shown in Figure 36.

Main power stage

In the original design of the Infineon reference design, the following products from the Infineon portfolio were selected:

- OptiMOS™ 6 80 V MOSFETs ISC031N08NM6, 3.1 mΩ $R_{DS(on),max}$ in SuperSO8 package (PQFN 5 x 6 mm²) are used in the primary-side full-bridge. The board is designed to fit two devices per position, for a total of four power MOSFETs. These devices will be replaced and benchmarked with the previous OptiMOS™ 5 80 V power transistors.
- OptiMOS™ 5 150 V MOSFETs BSC110N15NS5, 11 mΩ $R_{DS(on),max}$ in SuperSO8 package are used as synchronous rectifiers in the secondary-side full-bridge rectifier, for a total of four power MOSFETs.
- The functionally isolated (coreless transformer technology) gate driver EiceDRIVER™ 2EDF7275K is used on both the primary and secondary side of the converter.
- The Infineon XDP™ XDPP1100-Q024 is responsible for the control of the power stage. The device is specifically optimized for the control of isolated and non-isolated DC-DC converters. It features high-resolution pulse-width modulation (PWM), state-machine-based digital control loop and high-performance AFE. It comes with GUI-based system configuration for ease of use, accurate telemetry and PMBus support.

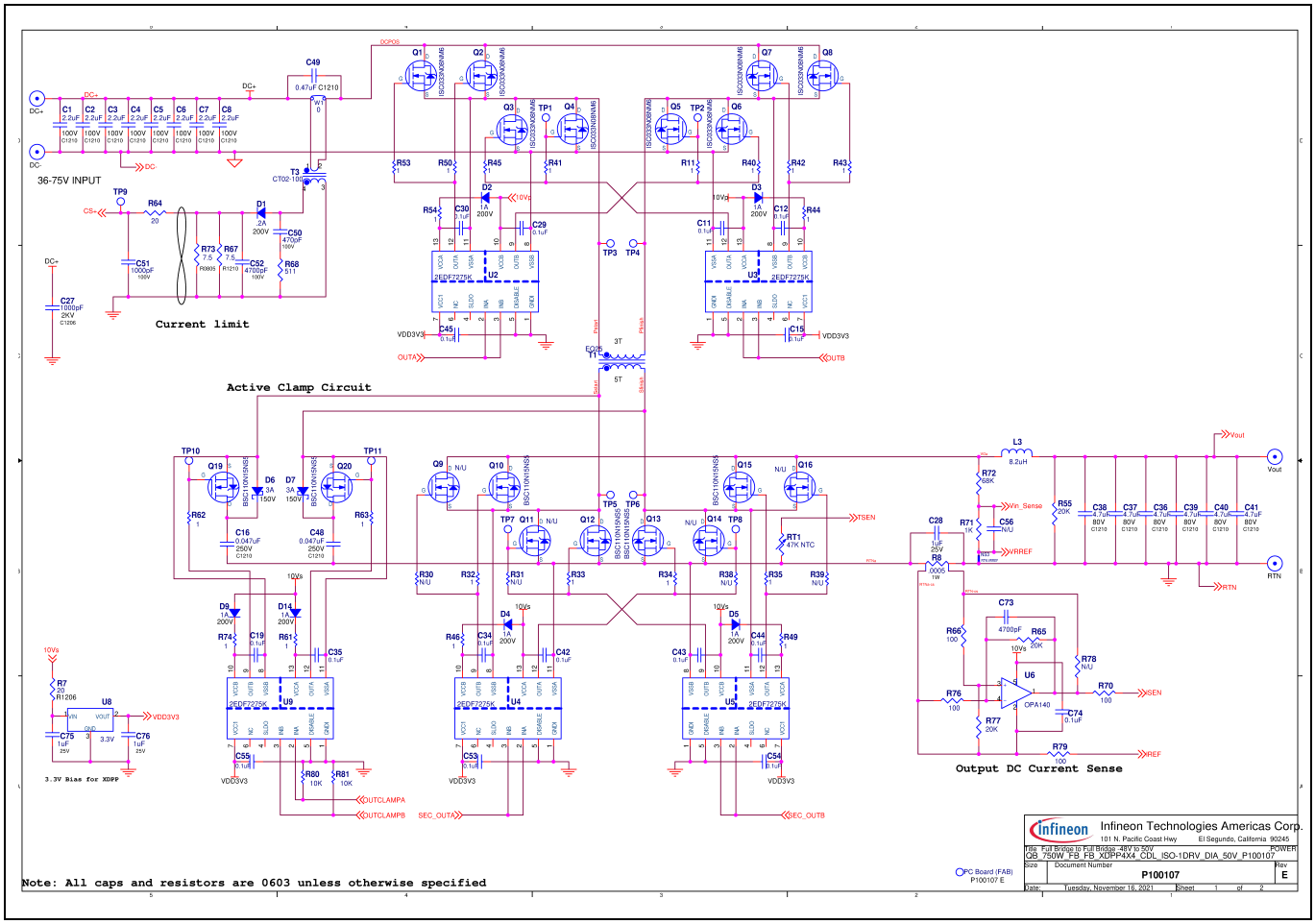


Figure 36 Infineon 750 W FB-FB isolated quarter-brick converter REF_750W_FBFB_50V_QB. Schematic page 1: main power stage

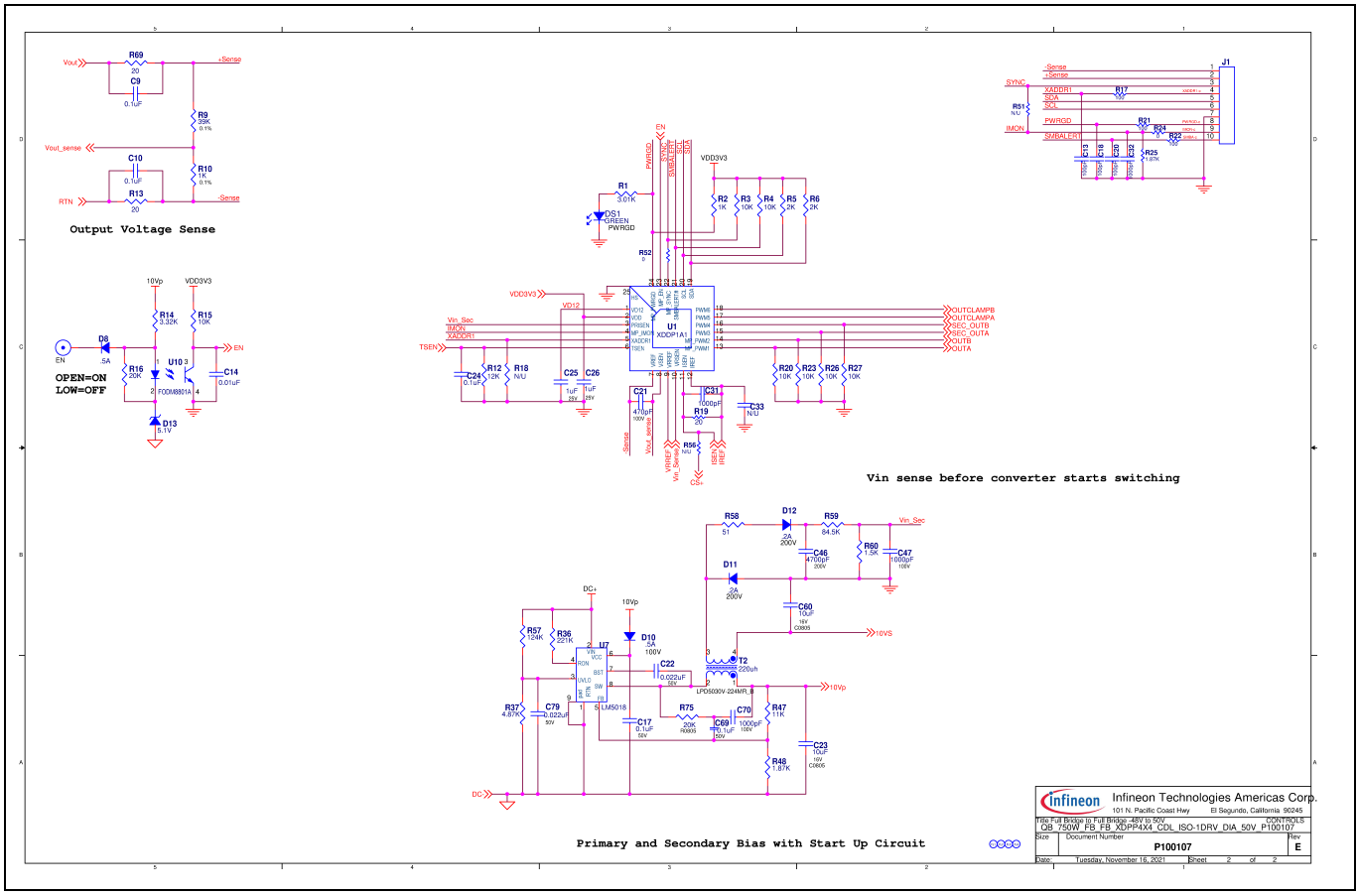


Figure 37 **Infineon 750 W FB-FB isolated quarter-brick converter REF_750W_FBFB_50V_QB. Schematic page 2: control and housekeeping.**

3.3.2.2 PCB description

Figure 38 shows the placement of the different components and measurement test points on the Infineon FB-FB isolated quarter-brick converter REF_750W_FBFB_50V_QB.

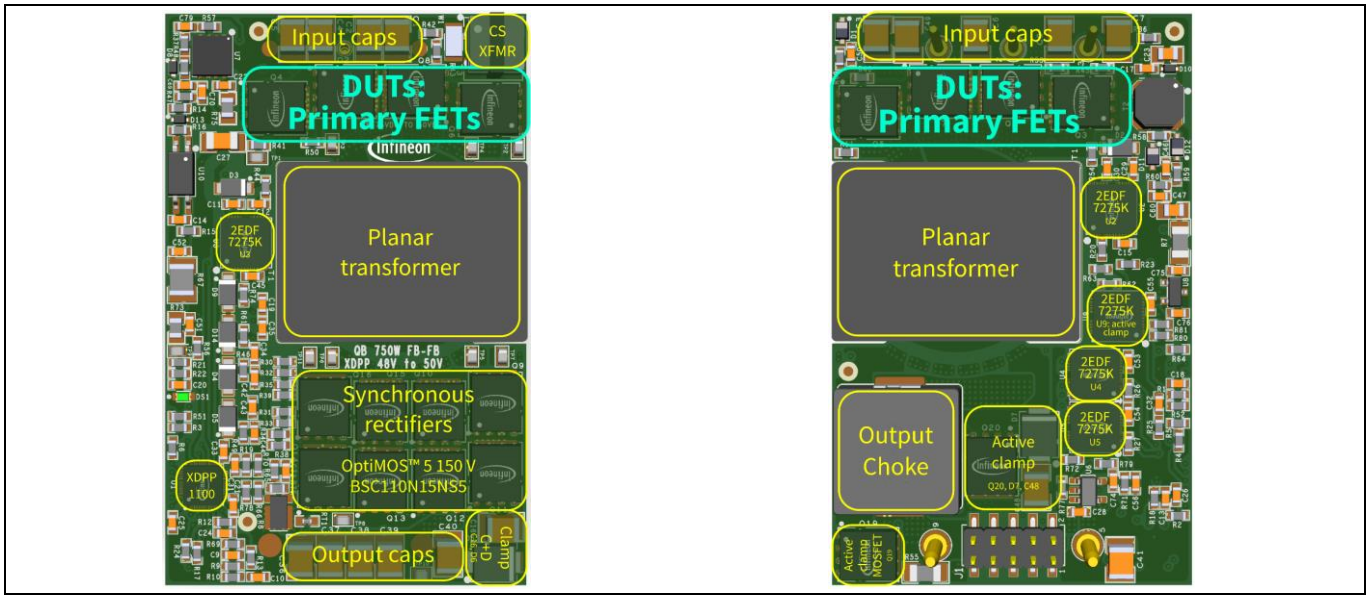


Figure 38 **Top and bottom views of the Infineon 750 W FB-FB isolated quarter-brick converter REF_750W_FBFB_50V_QB. The most significant components are highlighted.**

The outer dimensions of the board are 4.25 in. x 4 in. x 0.87 in. (108 mm x 102 mm x 22 mm). The PCB stackup is 14 layers deep. The internal layers are all 6 oz. copper thickness with the top and bottom layers at 4 oz. copper thickness. The total board thickness is 4.72 mm (186 mils).

3.3.2.3 Board specifications

The specifications for the Infineon REF_750W_FBFB_50V_QB isolated quarter-brick DC-DC converter are given in Table 15.

Specifications are given for T_A = 25°C unless otherwise specified.

Table 15 Specifications of the Infineon REF_750W_FBFB_50V_QB evaluation board

Parameter	Symbol	Values			Unit	Note/test condition
		Min.	Typ.	Max.		
Operating input voltage	V_{in}	-36	-48	-60	V	
Input current RMS value (V_{out} = 50 V)	$I_{in,RMS}$		16.5 22		A	V_{in} = -48 V, P_{out} = 750 W V_{in} = -36 V, P_{out} = 750 W
Start-up voltage threshold	$V_{in(on)}$	-43			V	
Minimum operating voltage after start-up	$V_{in(off)}$			-34	V	
Output voltage set-point	$V_{out,nom}$	25	50	55	V	Adjustable setpoint
Output current	I_{out}			15	A	
Output power	P_{out}			750	W	V_{out} = 50 V, v_{air} = 3 m/s
Efficiency (V_{out} = 50 V)	η		95.3		%	V_{in} = -48 V, P_{out} = 750 W
Power dissipation (V_{out} = 50 V)	P_{diss}			37	W	V_{in} = -48 V, P_{out} = 750 W
Output voltage ripple	$V_{out,ac}$			200	mV	Peak-to-peak, V_{out} = 50 V, $C_{out,ext}$ = 4x56 µF
Output voltage set-point tolerance	σ$V_{out,nom}$	-1		+1	%	
Output voltage regulation (load)	Δ$V_{out(load)}$			100	mV	V_{in} = -48 V, 0-100% of $I_{out,max}$
Output voltage regulation (line)	Δ$V_{out(line)}$			100	mV	V_{in} = -60…-36 V, I_{out} = 15 A
Recommended output capacitance	C_{out}	220		1000	µF	
Dynamic load response -Output voltage deviation -Settling time	Δ$V_{out(tr,load)}$ $t_{tr(load)}$			 ±500 40	 mV µs	V_{in} = -48 V, V_{out} = 50 V, 25% to 75% of $I_{out,max}$ at 2 A/µs, C_{out} = 4x56 µF
Switching frequency	f_{sw}		140		kHz	
Airflow velocity	v_{air}		600 3		LFM m/s	
Operating temperature (ambient)	T_a	-40		50	°C	
Functional isolation voltage	V_{iso}		1500		V	

3.3.3 Test setup description

The test setup is described here in detail. The actual test setup is shown in Figure 39.

3.3.3.1 Description of the test setup

The measurement setup precisely follows that already described earlier in Section 3.1.3.1: Description of the test setup.

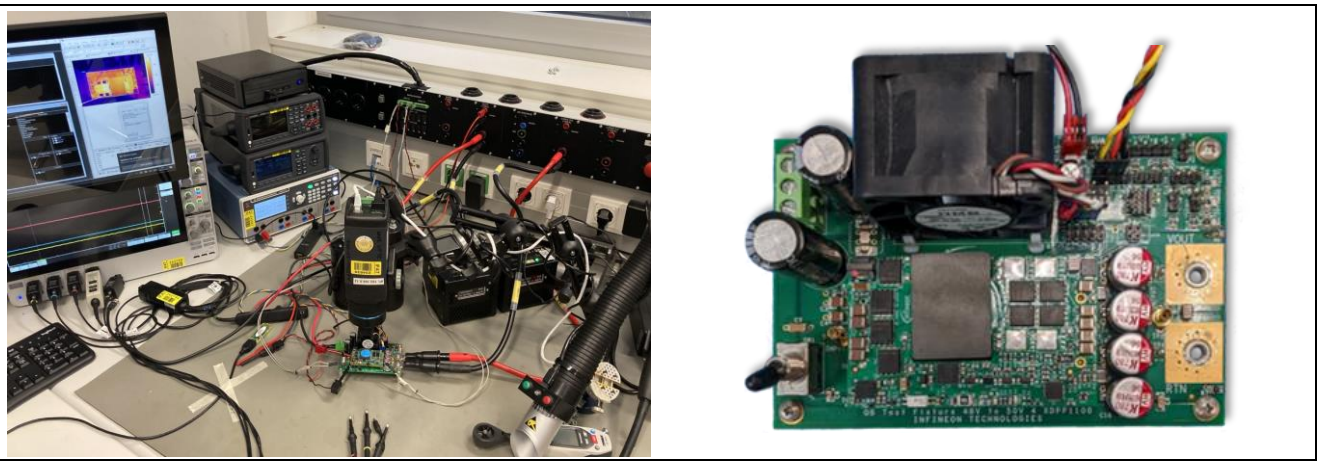


Figure 39 Actual test setup and detail of the quarter-brick converter on the fixture board

3.3.4 Efficiency test

3.3.4.1 Introduction

Efficiency tests were performed for the Infineon REF_750W_FBFB_50V_QB isolated quarter-brick DC-DC converter, using the test setup introduced in Section 3.3.3 Test setup description.

Efficiencies were captured for two different configurations of the primary full bridge, featuring two different devices under test (DUTs). DUTs come with a SuperSO8 (PQFN 5 x 6 mm^2) surface-mount package.

Only the primary bridge MOSFETs changed across the tests, while everything else was kept unchanged in the brick board and in the whole test setup. All the tests were carried out on the same brick unit.

The external gate resistors for the primary bridge MOSFETs were shorted out to benchmark the switching performance of the DUTs.

A summary of the DUTs and their position is given in Table 16.

Table 16 Devices under test – refer to schematic file reported in Figure 36

DUTs	DUT #1	DUT #2
Primary full bridge MOSFETs: Q1…Q8	**Infineon OptiMOS™ 5 80 V, 3 mΩ** BSC030N08NS5	**Infineon OptiMOS™ 6 80 V, 3.1 mΩ** ISC031N08NM6
Package	PQFN 5 x 6 mm^2	PQFN 5 x 6 mm^2
DUTs per each full-bridge position	2	2

3.3.4.2 Efficiency comparison at V_{in} = 48 V

Table 17 summarizes the efficiencies acquired at nominal input voltage (V_{in} = 48 V) for the different DUTs. The efficiency is measured at 600 LFM (3 m/s) airflow, T_A = 25°C and captured after thermal steady-state is reached. The efficiency curves, and system total power dissipation curves (relative to the reference DUT BSC040N08NS5 from the previous-generation OptiMOS™ 5) are reported in Figure 40.

Table 17 Measured efficiency (%) at nominal input voltage V_{in} = 48 V

Output current I_{out} \ DUT	Infineon OptiMOS™ 5 80 V, 3 mΩ BSC030N08NS5 PQFN 5 x 6 mm² (2 DUTs/pos)	Infineon OptiMOS™ 6 80 V, 3.1 mΩ ISC031N08NM6 PQFN 5 x 6 mm² (2 DUTs/pos)
1 A	82.79	83.23 (+0.44%)
3 A	92.25	92.41 (+0.17%)
7 A	94.75	94.84 (+0.09%)
11 A	95.32	95.44 (+0.12%)
15 A	95.05	95.14 (+0.10%)

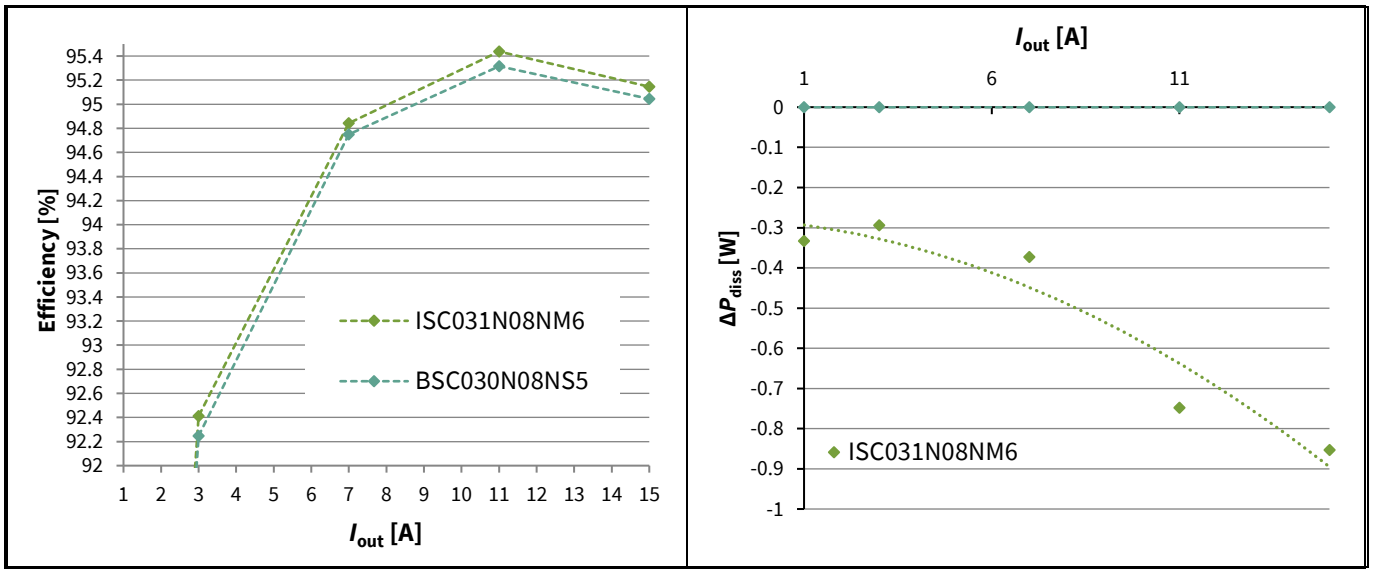


Figure 40 Efficiency and total ΔP_{diss} comparison at V_{in} = 48 V. Reference DUT is Infineon OptiMOS™ 5 80 V BSC030N08NS5

The efficiency plots in Figure 40 demonstrate the gain in performance delivered when OptiMOS™ 6 80 V is used in place of the predecessor technology, in a state-of-the-art 750 W DC-DC converter for RFPA applications.

A gain in efficiency of up to ~0.44 percent is recorded at light-load conditions, as a direct consequence of the better FOM of the new OptiMOS™ 6 technology. The ~40 percent lower (typ.) Q_g would yield a corresponding reduction of power consumption from the auxiliary bias supply.

At nominal line voltage, the full-load efficiency gain is up to a remarkable ~0.1 percent, in spite of the slightly higher $R_{DS(on)}$ compared with the OptiMOS™ 5. This is made possible by the faster switching of the new OptiMOS™ 6 technology. Coming with ~40 percent gate-to-drain charge Q_{gd} and a typical gate resistance of

0.65 Ω as opposed to the 1.6 Ω of the OptiMOS™ 5, the turn-off switching losses are proportionally reduced. Please note that in this converter, the primary current is larger than the secondary current in RMS value, because of the transformer 3:5 ratio.

To complement the analysis of the value proposition in the application, efficiencies are also given for maximum input voltage V_{in} = 60 V, which represents the most challenging condition for the DC-DC converter in terms of switching losses. Such results are again in agreement with the foregoing statements, with the system efficiency gaining further advantage from the better FOMs of the OptiMOS™ 6 technology.

3.3.4.3 Efficiency comparison at V_{in} = 60 V

Table 18 summarizes the efficiencies acquired at nominal input voltage (V_{in} = 60 V) for the different DUTs.

Table 18 Measured efficiency (%) at nominal input voltage V_{in} = 60 V

DUT / Output current I_{out}	Infineon OptiMOS™ 5 80 V, 3 mΩ BSC030N08NS5 PQFN 5 x 6 mm² (2 DUTs/pos)	Infineon OptiMOS™ 6 80 V, 3.1 mΩ ISC031N08NM6 PQFN 5 x 6 mm² (2 DUTs/pos)
1 A	77.91	78.51 (0.60%)
3 A	90.18	90.47 (0.29%)
7 A	93.48	93.63 (0.15%)
11 A	94.39	94.59 (0.20%)
15 A	94.29	94.55 (0.27%)

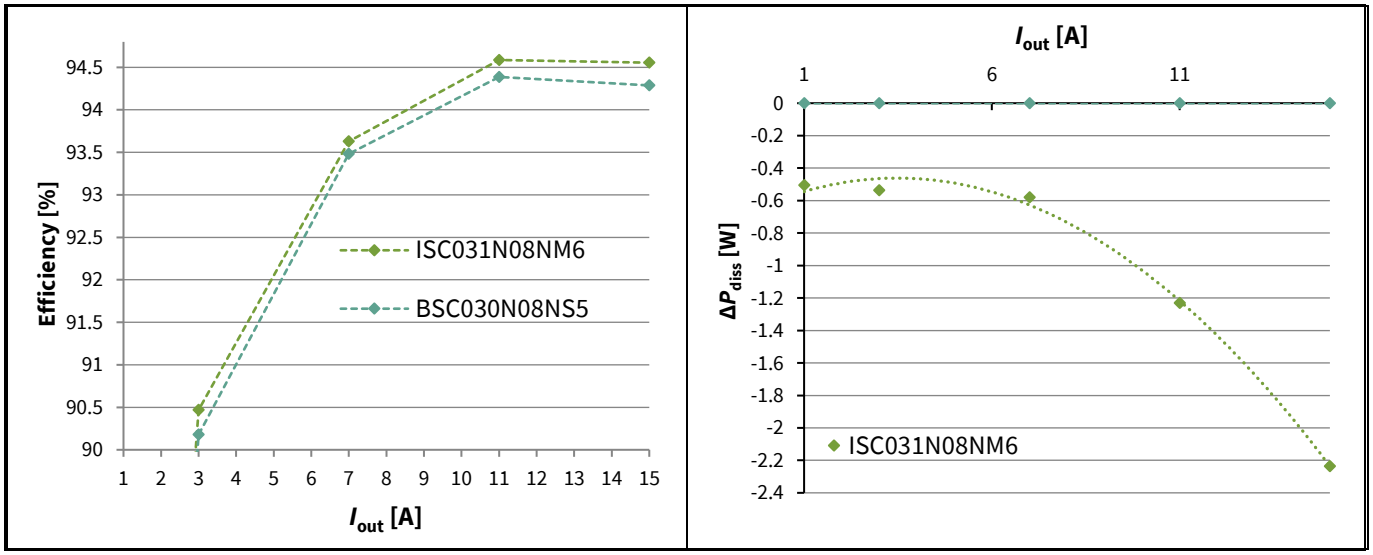


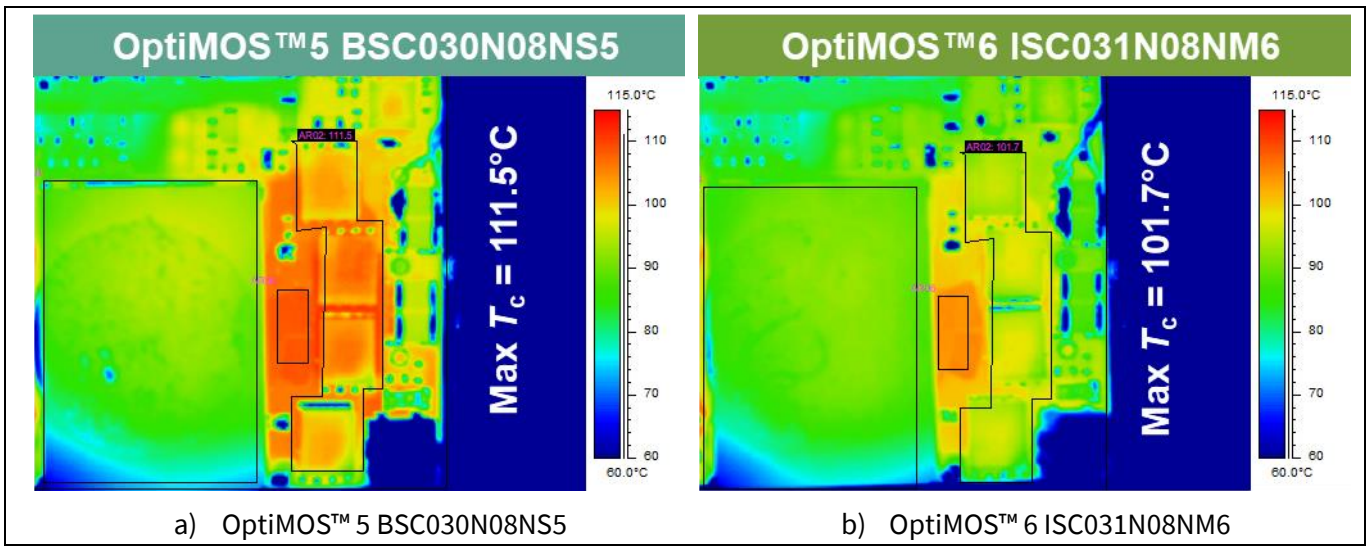
Figure 41 Efficiency and total ΔP_{diss} comparison at V_{in} = 60 V. Reference DUT is Infineon OptiMOS™ 5 80 V BSC030N08NS5

Experimental results highlight how the new Infineon OptiMOS™ 6 80 V family – bringing FOMs improvement – shines in hard-switching applications, where technology parameters are of primary importance to achieve best efficiency across the whole load range.

3.3.4.4 Thermal pictures at V_{in} = 60 V

Along with efficiency tests, thermal data were also acquired, using the test setup introduced in Section 3.1.3 Test setup description.

Temperatures were measured across the entire brick board by using a thermal camera, after thermal steady-state was reached. In Figure 42 the temperatures recorded on the primary MOSFETs are compared for the different DUTs. Measurements are provided for 3 m/s airflow, T_A = 25°C.



a) OptiMOS™ 5 BSC030N08NS5 b) OptiMOS™ 6 ISC031N08NM6

Figure 42 Thermal pictures at V_{in} = 60 V and P_{out} = $P_{out,TDP}$ show the worst case condition for this hard-switching converter

Thermal measurements reflect the overall efficiency improvement enabled by the OptiMOS™ 6, with up to ~10°C lower case temperature recorded on the primary MOSFETs – an outstanding achievement, of particular importance for this application.

Original equipment manufacturers (OEMs) are imposing strict miniaturization requirements for radio equipment, in turn enforcing challenging requirements on the PSU subsystem, usually sharing the same heatsink with the RF power amplifier itself. Lowering power losses and temperatures is therefore essential to deal with reduced thermal budget.

On top of that, achieving lower temperatures is of primary importance for system reliability and to meet the mission profile requirements of the application.

4 Summary

Infineon has expanded the latest OptiMOS™ 6 technology family with the introduction of 80 V MOSFETs to the product portfolio. This family raises the bar with benchmark performance combined with highly efficient packages. The portfolio includes PQFN 3.3 x 3.3 mm^2 with $R_{DS(on),max}$ ranges from 5.3 mΩ to 15.7 mΩ, and PQFN 5 x 6 mm^2 (SuperSO8) with $R_{DS(on),max}$ ranges from 1.45 mΩ to 15.1 mΩ.

The latest Infineon thin wafer technology, the result of 20+ years of experience in advanced trench MOSFET design, comes with a totally redesigned cell, showing the industry's best FOMs.

All the most relevant FOMs of the latest OptiMOS™ technology show improvements, resulting in a device specifically optimized for high-switching-frequency SMPS applications. Compared to the previous OptiMOS™ 5 technology, Infineon's leading thin wafer technology enables significant performance improvements with up to ~30 percent reduction in $R_{DS(on)}$ and ~ 40 percent improved FOMs.

These improvements make the latest OptiMOS™ 6 technology specifically optimized for high-switching-frequency SMPS applications. Nevertheless, the new OptiMOS™ 6 80 V also comes with wider SOA, ultimately enabling the latest trench MOSFET technology to address some linear applications which require small PQFN packages together with the lowest $R_{DS(on)}$.

As demonstrated in this document, OptiMOS™ 6 80 V technology helps to elevate power designs to the next level, bringing performance, ease of use, reliability and price benefits.

References

[1] Infineon Technologies AG: *OptiMOS™ 6 40 V family page*; Available online

[2] Infineon Technologies AG: *OptiMOS™ 6 100 V family page*; Available online

[3] Infineon Technologies AG: *OptiMOS™ 6 120 V family page*; Available online

[4] Chen, J.: *Design optimal built-in snubber in trench field plate power MOSFET for superior EMI and efficiency performance*; 2015 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD); Washington DC, USA; 2015; pp. 459–462; doi: 10.1109/SISPAD.2015.7292361

[5] Perera, N./Kampitsis G./van Erp R. et al: *Analysis of Large-Signal Output Capacitance of Transistors Using Sawyer–Tower Circuit*; IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 9, no. 3, pp. 3647–3656; June 2021; doi: 10.1109/JESTPE.2020.2992946

[6] Infineon Technologies AG: *Linear Mode Operation and Safe Operating Diagram of Power-MOSFETs*; Available online

[7] Infineon Technologies AG: *Linear FET combines advantages of planar and trench MOSFETs*; Available online

[8] Infineon Technologies AG: *OptiMOS™ Linear FET family page*; Available online

[9] Infineon Technologies AG: *The XDPP1100 digital power supply controller*; Available online

[10] Infineon Technologies AG: *Reference design XDPP1100 fixed-frequency LLC 1 kW quarter brick converter with hybrid soft-start;* Available online

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