Solid-state battery disconnect unit with Infineon CoolSiC™ JFET technology

Design considerations for a dedicated power stage

About this document

Scope and purpose

This application note explains the motivation and need for a solid-state battery disconnect unit in an electric commercial, construction, and agricultural vehicle (eCAV). It outlines design considerations for a dedicated power stage using the Infineon CoolSiC™ JFET technology as used in the solid-state battery disconnect demonstrator REF-SSBD800VDCJCQJ1.

Intended audience

This document is intended for design engineers, technicians, and electronic system developers who want to learn about the solid-state battery disconnect application in eCAVs.

Key points

- Introducing the application
- Infineon's CoolSiC™ JFET technology
- Thermal design
- Power switch overvoltage protection
- Fast overcurrent detection

About this product family

Product family

The Infineon CoolSiC™ JFET family delivers high-voltage power tr neieansistors with ultra-low $R_{DS(on)}$ that are optimized for solid-state switching applications. The silicon carbide trench JFET technology is engineered for robustness and long-term reliability under harsh operating conditions. Quick overcurrent protection is achieved using Infineon's XENSIV™ high-bandwidth tunnel magnentoresistive (TMR) effect open-loop current sensors.

Target applications

Battery disconnect switch, DC solid-state circuit breaker, DC solid-state relay

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1 eBDU introduction

This application note discusses design considerations for a CoolSiC™ JFET solid-state battery disconnect unit with discretes. To provide context for the intended application, section 1.1 outlines the motivation and the requirements of an eBDU application. This section provides a brief overview with some examples and is not a complete guide for this type of application. The main design focus of this application note is the battery disconnect function in an eCAV. The same concepts can also be used in applications where a fast disconnect function of the DC current is required (e.g., energy storage).

1.1 General application information

The electrification of CAVs is comparable to a passenger vehicle drive-train system as shown in Figure 1. However, CAVs need significantly higher power for driving and therefore higher storage capacity to achieve a useful driving range. This higher storage capacity is achieved by using several battery packs in parallel. With the paralleling of several battery packs, the effective impedance of the battery system becomes as low as ~2 mΩ and ~1.5 µH. With this low impedance, the prospective short-circuit currents in the system can easily reach 200 – 400 kA.

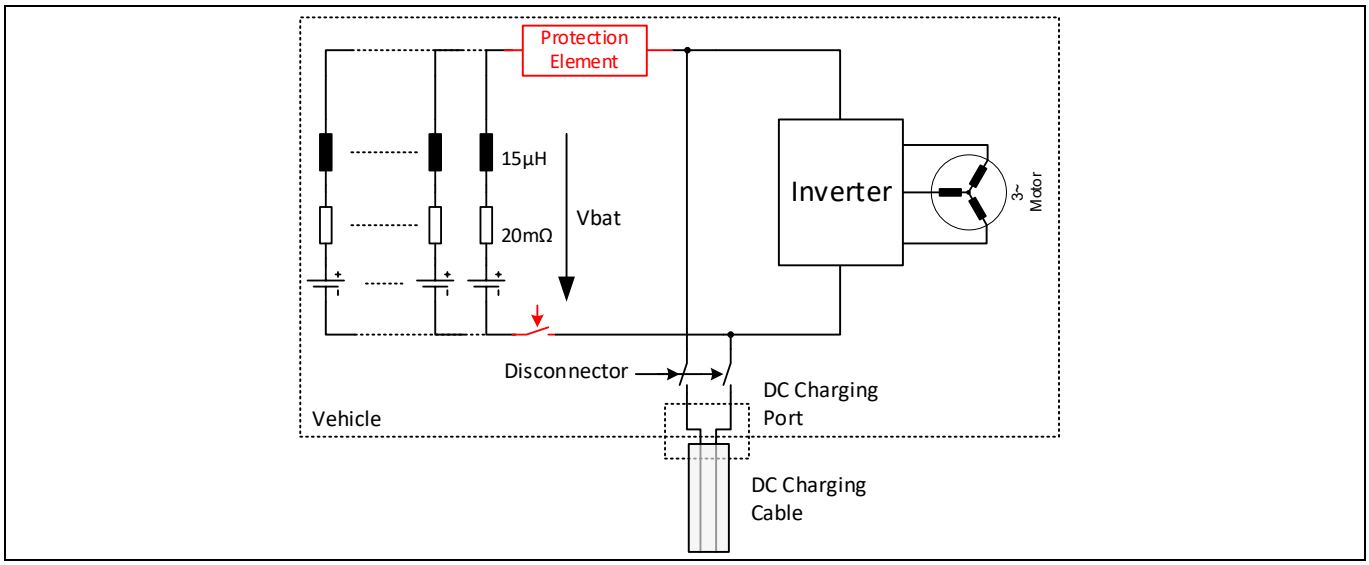


Figure 1 Simplified overview of a typical eCAV drive train

A protection element is required to protect the vehicle and the surroundings from the high energy stored in the batteries in case of a failure event, such as a short circuit. The DC charging ports of such vehicles should enable a low-impedance connection to the battery for fast charging, thus enabling a low-impedance connection to the outside. As the probability of malfunctioning, especially of the charging cable, is high, the charging standards define the maximum short-circuit current and short-circuit energy at the charging port in case of such a failure. According to the combined charging system (CCS) standard ISO 5474-3, the maximum short-circuit current at the vehicle inlet shall not exceed 30 kA [1] and according to the megawatt charging system (MCS) whitepaper, the vehicle shall limit the short-circuit current at the MCS connector to a maximum of 70 kA [2]. These limits necessitate a protective element in the vehicle that can safely and reliably disconnect the battery system from the charging port.

1.2 Protection technologies

Different electro-mechanical implementations are currently in use as protection elements, e.g., melting-, pyrofuse, or a mechanical switch system with fast overcurrent detection. Such protection elements can however switch off a short-circuit event only once (and have to be replaced after each such event) or just a few times during their lifetime. Solid-state solutions such as the hybrid circuit breaker or full solid-state circuit breakers like the eBDU demonstrator REF-SSBD800VDCJCQJ1 address these limitations and also trip faster than legacy solutions. Table 1 provides a comparative overview of typical tripping times and the expected lifetime for short-circuit tripping across different solutions.

Furthermore, the robustness of semiconductor solutions exceeds that of mechanical switches throughout their lifetime. Mechanical switches face limitations due to mechanical wear, which restricts the number of switching cycles they can support. Similarly, melting fuses can experience fuse fatigue, resulting in reduced current-carrying capabilities over time.

Figure 2 shows a simulation of the short-circuit current with the cut-off current overshoot of the protection elements in a sample eCAV battery system with several battery packs in parallel. In such low-impedance systems, the short-circuit current can rise rapidly, making it crucial to detect and swiftly disconnect the current in the event of a short circuit.

To maintain short-circuit currents within specified limits at the charging port for advanced battery technologies, a full solid-state circuit breaker (SSCB) implementation is required to switch off the short circuit fast enough. With fast overcurrent detection and switch-off time, any current overshoot exceeding the threshold level can be kept at a minimum.

Table 1 Reaction time of protection elements

Protection element	Typical tripping time	No. of short-circuit trips in a lifetime
Melting fuse	10 ms	1
Mechanical switch	4 ms	< 10
Pyrofuse	1 ms	1
Hybrid circuit breaker (HCB)	500 µs	> 1000
Solid-state circuit breaker - eBDU	< 2 µs	> 1000

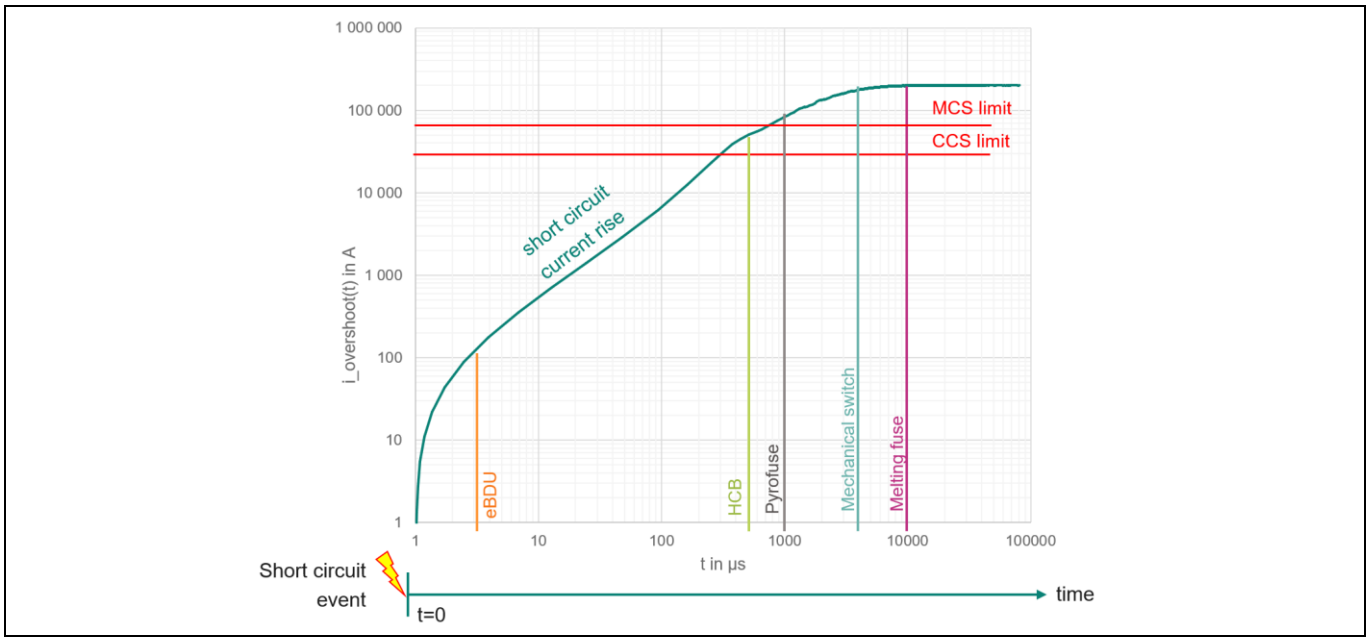


Figure 2 Short-circuit current and shutdown current overshoot versus tripping time in a typical eCAV system

1.3 Integration of solid-state protection

In a typical eTruck power system, there are multiple potential locations where a solid-state battery disconnect can be integrated, as illustrated in Figure 3. These locations include an electronic battery disconnect unit (eBDU) within the battery pack, a centralized eBDU in the power distribution unit (PDU), and solid-state relays (SSRs) in the DC charging sockets. Additionally, solid-state fuses (eFuses) can be implemented within the PDU to protect auxiliary systems.

Given the diverse requirements of the different sockets and system configurations, a scalable solution is essential to address the power classes and integration needs of the system. The eBDU demonstrator REF-SSBD800VDCJCQJ1 focuses on a battery pack disconnect unit built using discrete components. The discrete approach offers both flexibility and scalability, allowing for customization in applications requiring lower currents. This includes solutions like eFuses for auxiliary sockets, which can be adapted to meet specific requirements effectively.

For high-current applications, such as the megawatt charging system (MCS) port or a centralized battery disconnect unit, utilizing the power modules may offer advantages in terms of system integration. Power modules are specifically designed to manage the high-current demands of these applications while also offering integrated isolation and direct water cooling capabilities, which simplifies the overall system integration process.

Design considerations for a dedicated power stage

eBDU introduction

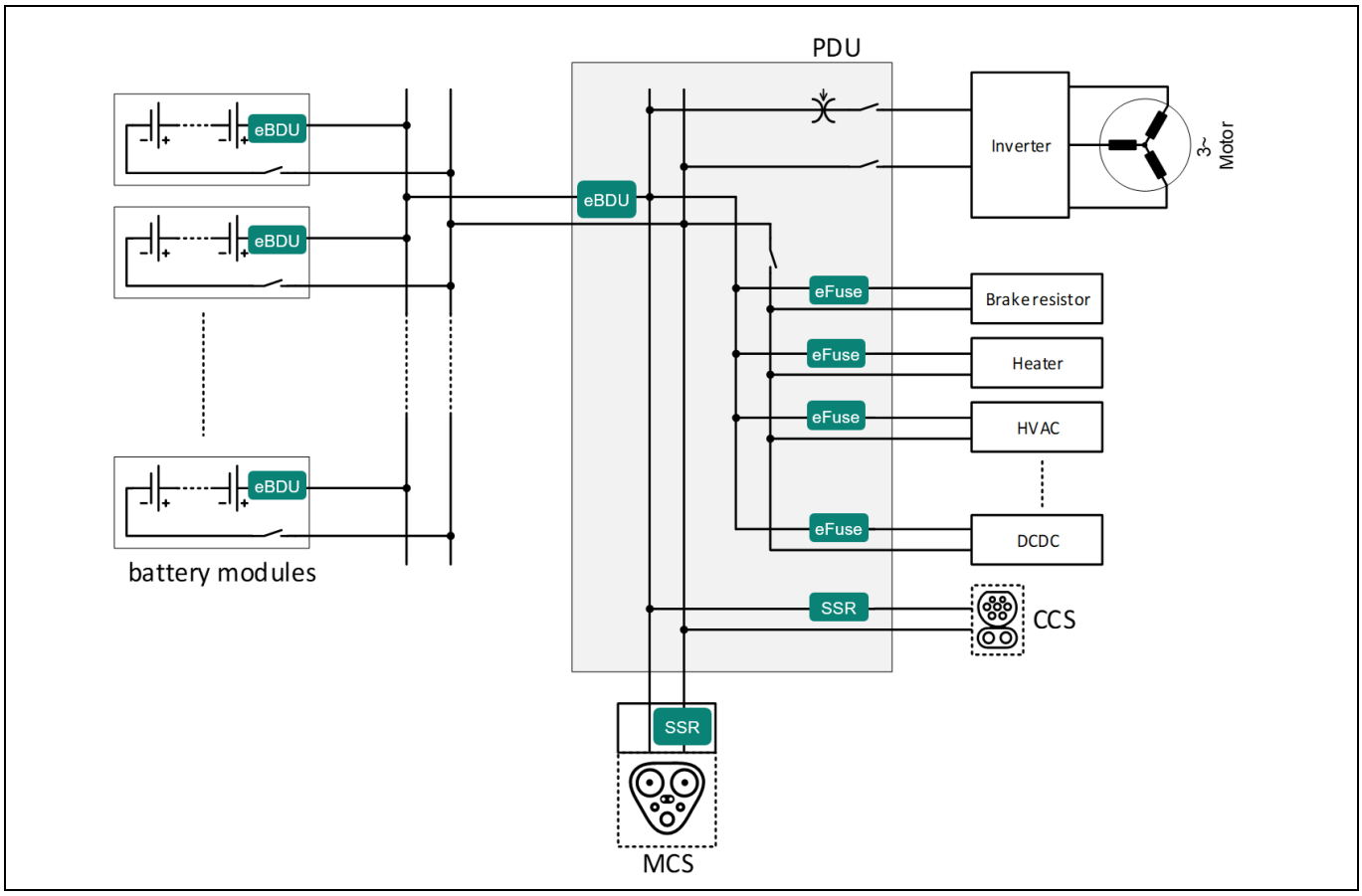


Figure 3 eBDU application sockets in a typical eCAV system

2 Infineon CoolSiC™ JFET technology

2.1 System concept

As discussed in section 1.1, the eBDU acts as a solid-state protection element in a typical eCAV drive train. A typical battery pack application with an eBDU is shown in Figure 4. In this case, the eBDU is protecting one pole and a mechanical contactor is used for separation on the second pole of the battery. An additional mechanical contactor in series with the eBDU is optional depending on the overall system topology.

In a semiconductor solution, all load switching, overcurrent, or short-circuit switch-off events are handled by the eBDU. The mechanical contactor only provides galvanic isolation with a physical air gap and does not perform any load switching. As a result, the high-current relay used in this application can be simplified (for example, by removing the arc-extinguishing chamber) and optimized for minimal conduction losses.

A mechanical contactor that provides galvanic isolation in the OFF state enables the use of Infineon's CoolSiC™ JFET technology in a barebone configuration. The JFET device is intrinsically conductive when no gate-source voltage is present. Therefore, during power-down of the battery junction box supply, the mechanical contactor is opened to ensure isolation of the battery. If a normally OFF eBDU system is needed, a cascode configuration with an LV MOSFET enables an intrinsic normally OFF behavior. For a cascode configuration, refer to Infineon CoolSiC™ JFET cascode evaluation board for solid-state circuit breaker applications [6].

In addition, the application socket in the battery junction box is required to block the flow of current in one direction. Other sockets may demand bidirectional blocking. To block current flow in both polarities, an anti-serial (back-to-back or common-source) connection between two power devices is required.

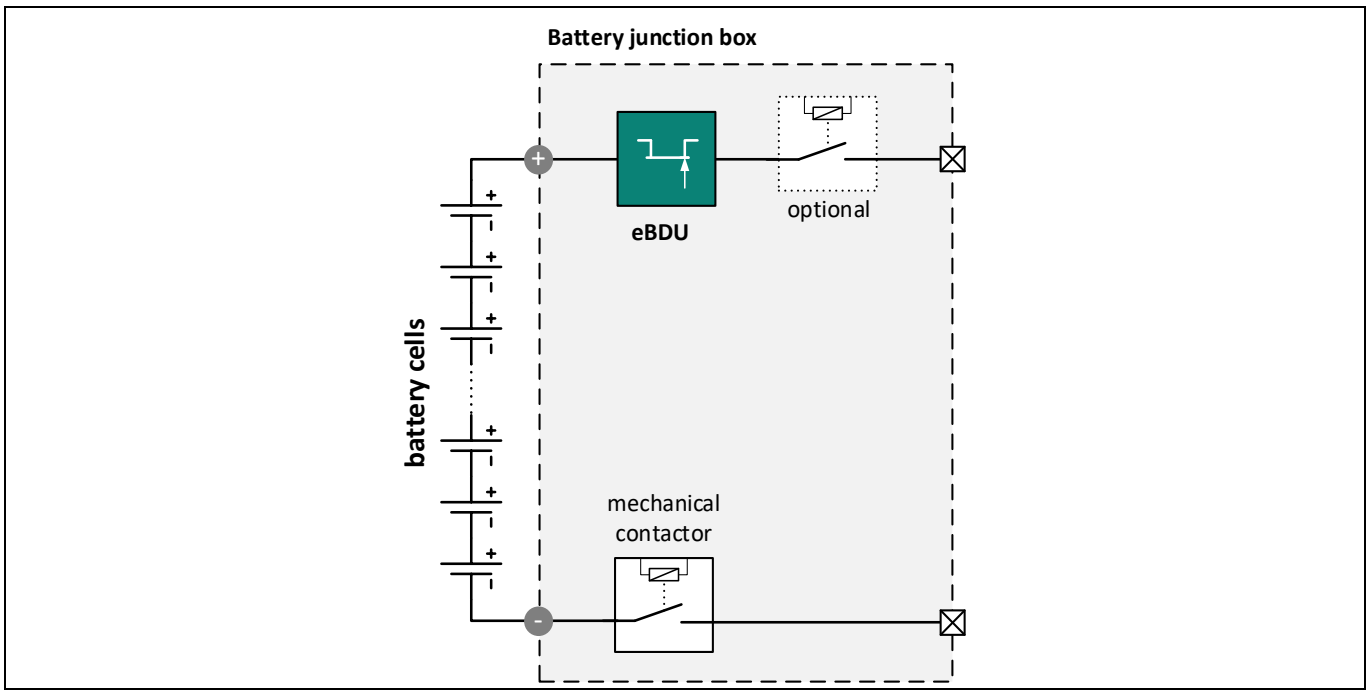


Figure 4 eBDU application in a battery junction box

2.2 CoolSiC™ JFET technology

The Infineon CoolSiC™ JFET technology complements Infineon's technology portfolio for power distribution applications. Legacy semiconductor solutions are usually optimized for switching applications, but the JFET technology is dedicated to solid-state applications. It is optimized for conduction losses ($R_{DS(on)}$*A figure of merit) and robustness.

The very good thermal stability of the JFET technology under wide operating conditions prevents hot-spotting during overload conditions and supports high-current avalanche events. This enables the simplification of the clamping design and the elimination of the V_{DSS} voltage margin that is needed in other technologies.

For more detailed information, please refer to the JFET application note [7].

2.3 Concept of paralleling CoolSiC™ JFETs

As battery technology advances, the charging power in eCAV applications continues to rise, increasing the current requirements for the battery disconnect unit. To meet these requirements, while staying within the power dissipation limits, even with the CoolSiC™ JFET that provides the lowest $R_{DS(on)}$ per device, the discrete devices must be paralleled. Leveraging the benefits described in section 2.2, the CoolSiC™ JFET technology simplifies device parallelization. To prevent parasitic turn-on of the power stage caused by fast transient voltage swings at the terminals, a local low ohmic clamp MOSFET can be placed for each JFET device. A simplified concept is shown in Figure 5. For more information and sample implementation, refer to the eBDU demonstrator user guide [8].

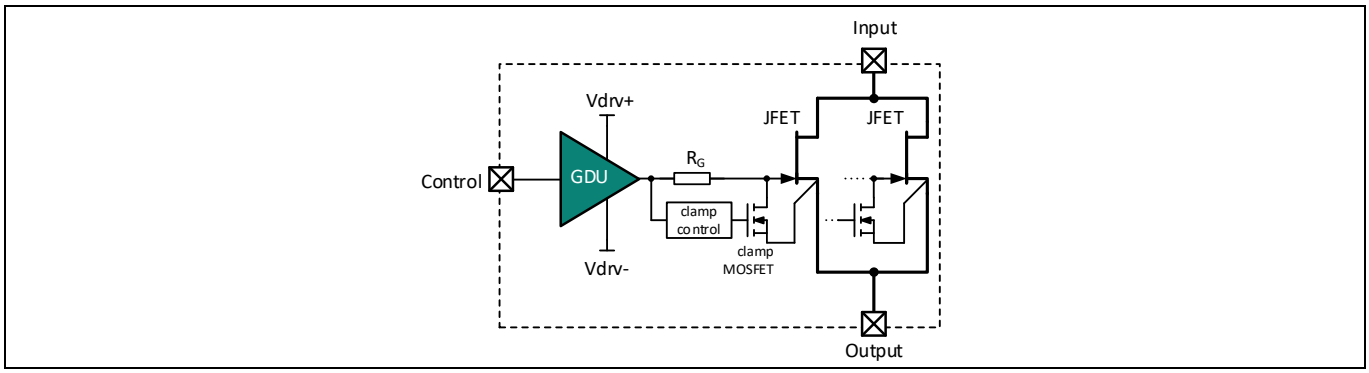


Figure 5 Simplified JFET paralleling concept

3 Thermal design

The Infineon JFET IJCQ120RM25J1 power device used in this type of application is based on the Q-DPAK package with a top-side cooling (TSC) configuration. The main advantage of using the TSC package is that the heat generated in the semiconductor is extracted through an exposed pad on the package's topside to an attached heat sink. The thermal path is decoupled from the electrical connections of the power device [3].

In this application, the active cooling system (water or air) is located externally to the ECU. Therefore, it is essential to ensure electrical isolation from the exposed-pad potential of the package that corresponds to the drain pin of the power device. Electrical isolation is typically the limiting factor for the thermal resistance in the entire cooling stack. It creates a bottleneck when attempting to increase the local thermal mass for enhancing the thermal capacitance. During short-term overloads (e.g., pulse durations in the range of 100 ms), this local thermal capacitance plays a crucial role in buffering the energy generated by the device's power loss.

An economically optimized thermal management solution can be achieved by increasing the interface area between the component and the heat sink, reducing thermal resistance. A sample implementation would be using copper heat spreaders directly soldered on to the exposed pad of the Q-DPAK package, doubling the interface area. This approach can eliminate the need for advanced isolation materials, providing a cost-effective alternative while maintaining thermal performance.

A cross-section of the cooling stack is shown in Figure 6. For galvanic isolation of the exposed pad to the heat sink, a direct bonded copper (DBC) material is used. The DBC isolation is coated with copper and directly soldered to the heat spreader. To compensate for mechanical tolerances of the cooling stacks, a thermal interface material (TIM) is used to fill the gap between the heat sink and the DBC. The parts and assembly of the cooling stack are shown in Figure 7.

Tables 2 and 3 demonstrate the benefits of using a heat spreader. Table 2 lists the simplified thermal stack calculations for a sample cooling stack without heat spreader, and Table 3 lists the calculations for a cooling stack as implemented in the eBDU demonstrator REF-SSBD800VDCJCQJ1. In both calculated cases, the heat sink is not considered in the comparison. The heat spreader can reduce the R_{th} of the cooling stack towards the heat sink by more than 30%.

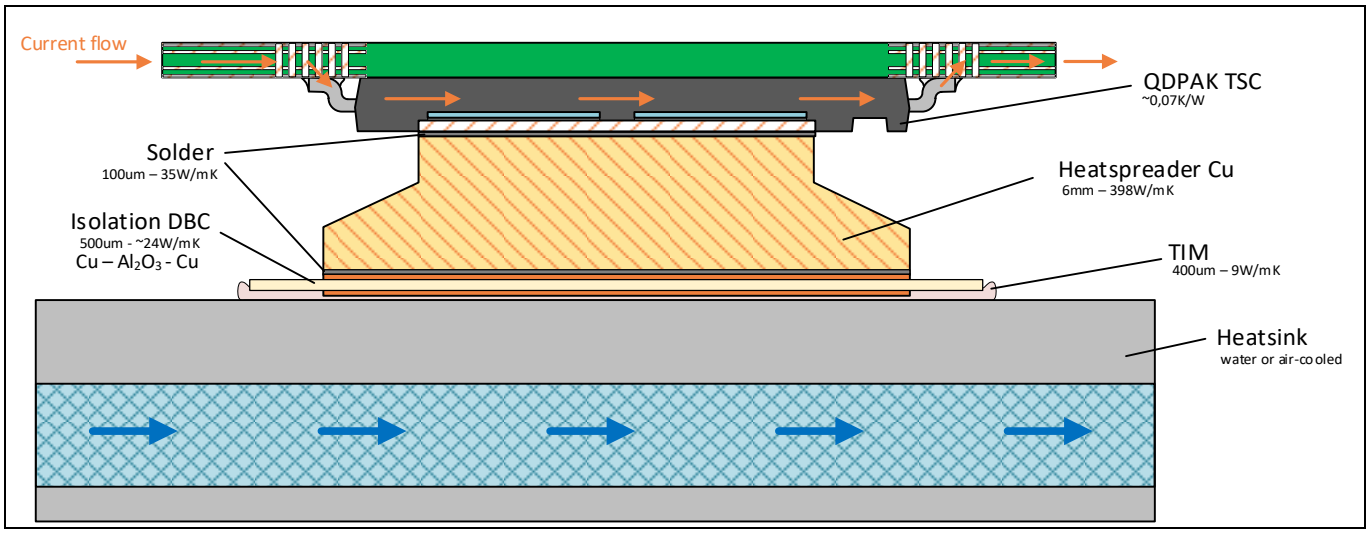


Figure 6 Cross-section of a thermal TSC cooling stack

Table 2 **Example stackup for TSC without a heat spreader (without a heat sink)**

	thickness [µm]	conductivity [W/mK]	area [mm²]	R_{th} [K/W]
Package	-	-	122.76	0.06
Exposed pad solder	100	34.8	122.76	0.023
DBC Cu	300	398	122.76	0.006
DBC (Al_2O^3)	380	24	122.76	0.129
DBC Cu	300	398	122.76	0.006
TIM (conductive grease)	400	9	122.76	0.362
Total				**0.587**

Table 3 **Example stackup for TSC with heat spreader (without a heat sink)**

	thickness [µm]	conductivity [W/mK]	area [mm²]	R_{th} [K/W]
Package	-	-	122.76	0.06
Exposed pad solder	100	34.8	122.76	0.023
Heat spreader	6000	398	322.76	0.047
Solder	100	34.8	400	0.007
DBC Cu	300	398	400	0.002
DBC (Al_2O_3)	380	24	400	0.040
DBC Cu	300	398	400	0.002
TIM (conductive grease)	400	9	400	0.111
Total				**0.292**

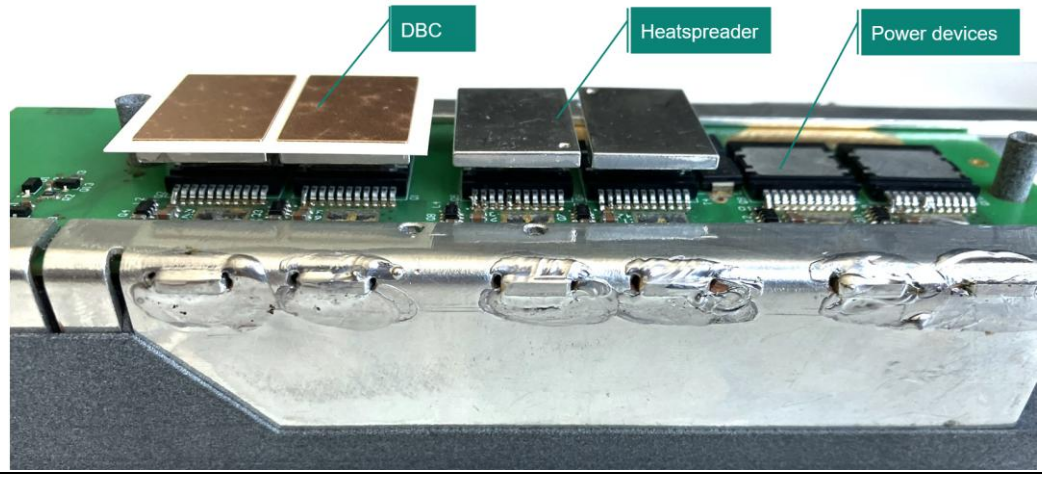


Figure 7 TSC cooling stack assembly

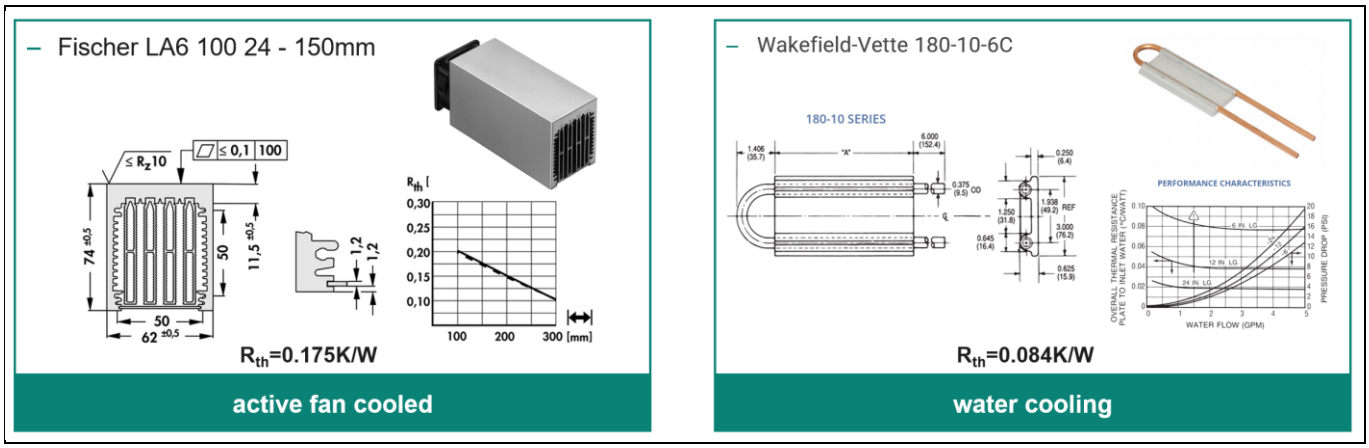


Figure 8 Heat sink options for demonstrator – active air-cooled and water-cooled

For easier usage of the eBDU demonstrator REF-SSBD800VDCJCQJ1, an active air-cooled heat exchanger is used. To increase the current capabilities of the demonstrator, this heat exchanger can be replaced by a water cooler. Figure 8 shows the active air cooling and water cooling options with the respective R_{th} values from the datasheet.

To calculate the overall R_{th} of the complete system, a simplified model as shown in Figure 9 is used. The individual cooling stacks are modeled with a parallel connection between the package's $R_{th,jc}$ and the cooling stack's $R_{th,cs}$. The value of $R_{th,total}$ can be calculated as:

$$R_{th,total} = \left(R_{th,jc1} + R_{th,cs1}\right) \parallel \left(R_{th,jc2} + R_{th,cs2}\right) \parallel \cdots \parallel \left(R_{th,jcn} + R_{th,csn}\right) + R_{th,cooler}$$

$$R_{th,total} = \frac{1}{\frac{1}{\left(R_{th,jc1} + R_{th,cs1}\right)} + \frac{1}{\left(R_{th,jc2} + R_{th,cs2}\right)} + \cdots + \frac{1}{\left(R_{th,jcn} + R_{th,csn}\right)}} + R_{th,cooler}$$

If all blocks are considered to have the same cooling stack, the calculation can be simplified as:

$$R_{th,total} = \frac{\left(R_{th,jc} + R_{th,cs}\right)}{n} + R_{th,cooler}$$

Using ($R_{th,jc}$+$R_{th,cs}$) from Table 3 and paralleling n = 6 stacks will give:

$$R_{th,total,water} = 0.078\ K/W; \qquad R_{th,total,air} = 0.224\ K/W$$

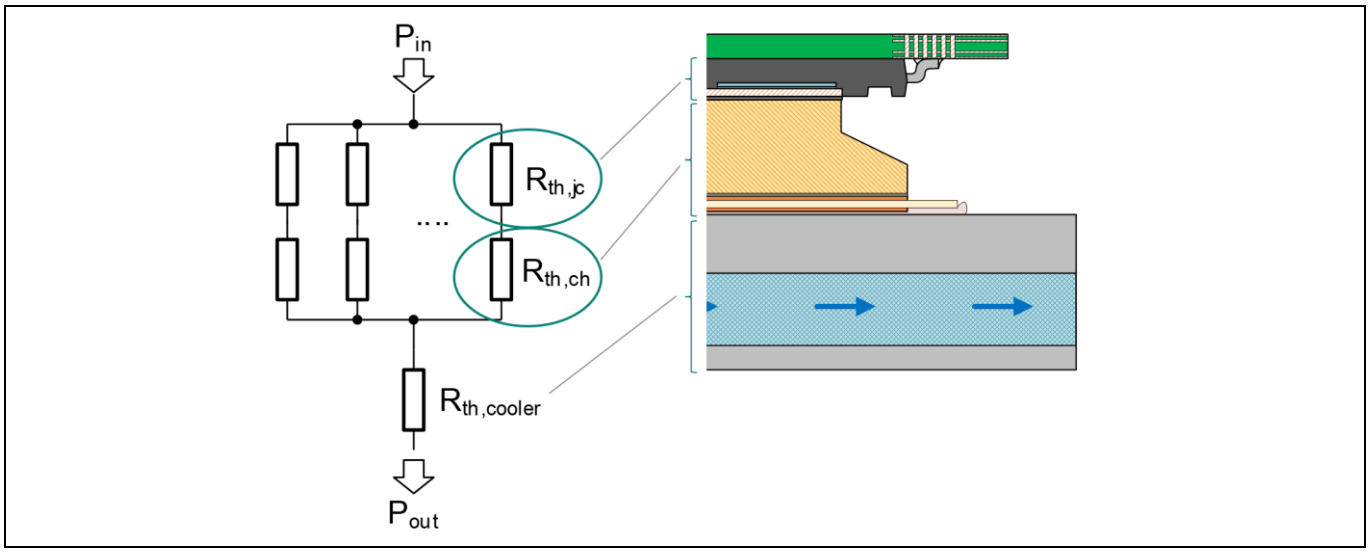


Figure 9 R_{th} calculations model

To calculate the number of devices needed for a certain current capability, the maximum allowable junction temperature swing of the power device needs to be considered. The maximum coolant temperature (water cooling) or ambient temperature (air cooling) is considered to be 65°C. The maximum continuous operating junction temperature T_{vj} of the power device IJCQ120RM25J1 is 175°C with a time-limited overload capability of 200°C. [4]

Figure 10 shows the maximum junction temperature swing ΔT_j when considering the worst-case mechanical tolerances and $R_{DS(on)}$ mismatch as well as a temperature sensor error and safety margin. In this example, a maximum junction temperature swing of 80 K is used for further calculations.

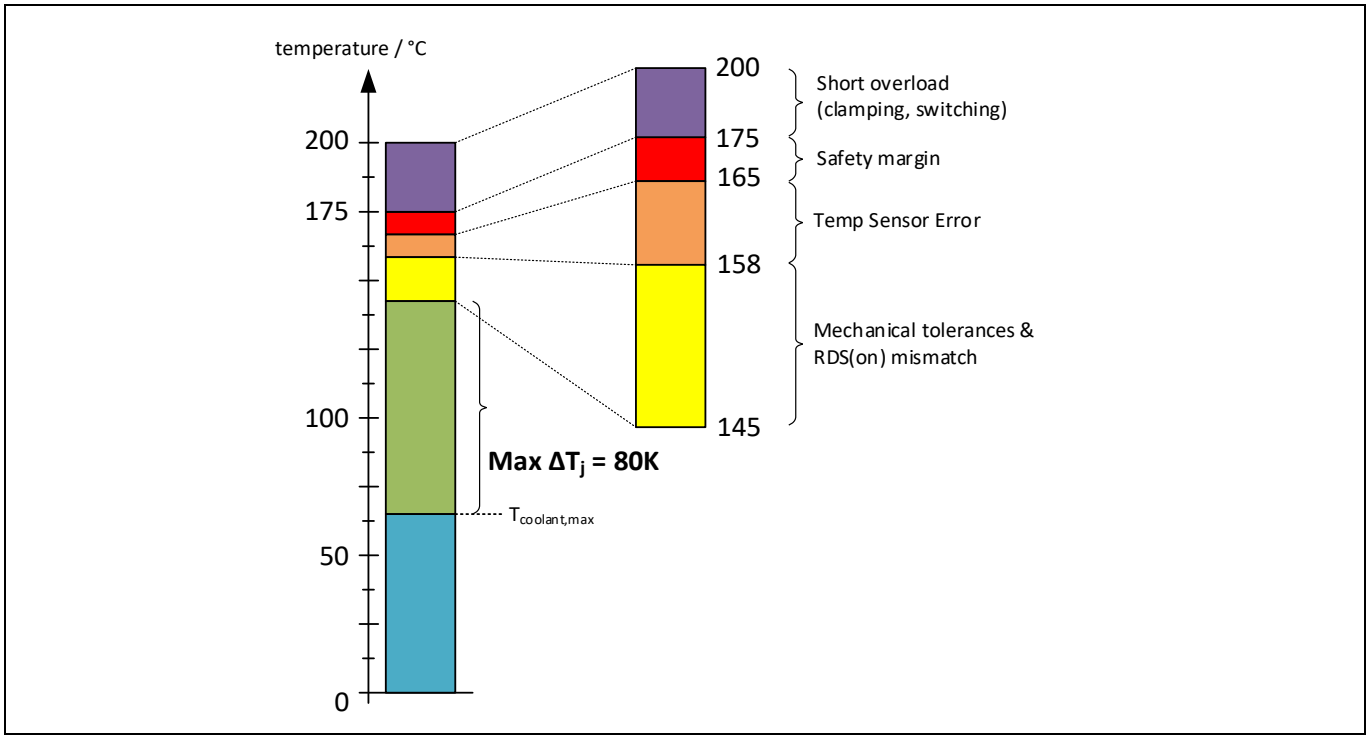


Figure 10 Thermal budget power device

With this temperature swing, the maximum power loss of a particular cooling stack for six devices can be calculated as:

$$P_{air,max} = \frac{\Delta T_j}{R_{th,total,air}} = \frac{80}{0.241} = 357.68\,W \ldots for\ n = 6$$

$$P_{water,max} = \frac{\Delta T_j}{R_{th,total,water}} = \frac{80}{0.096} = 1016.95\,W \ldots for\ n = 6$$

With the maximum power dissipation rating per stack, the current capabilities can be calculated. To calculate the loss of the power device, the $R_{ds(on)}$ value from the datasheet at T_{vj} = 125°C is used. Additionally, a wiring adder of 564 µΩ (at 125°C) is used. It is added to the power losses of the power device for simplification:

$$I_{max} = \sqrt{\frac{P_{max}}{\frac{R_{DS(on),125C}}{n} + R_{wiring,125C}}}$$

Figure 11 shows the calculation of the maximum current capability for air-cooled and water-cooled options with respect to the number of paralleled devices.

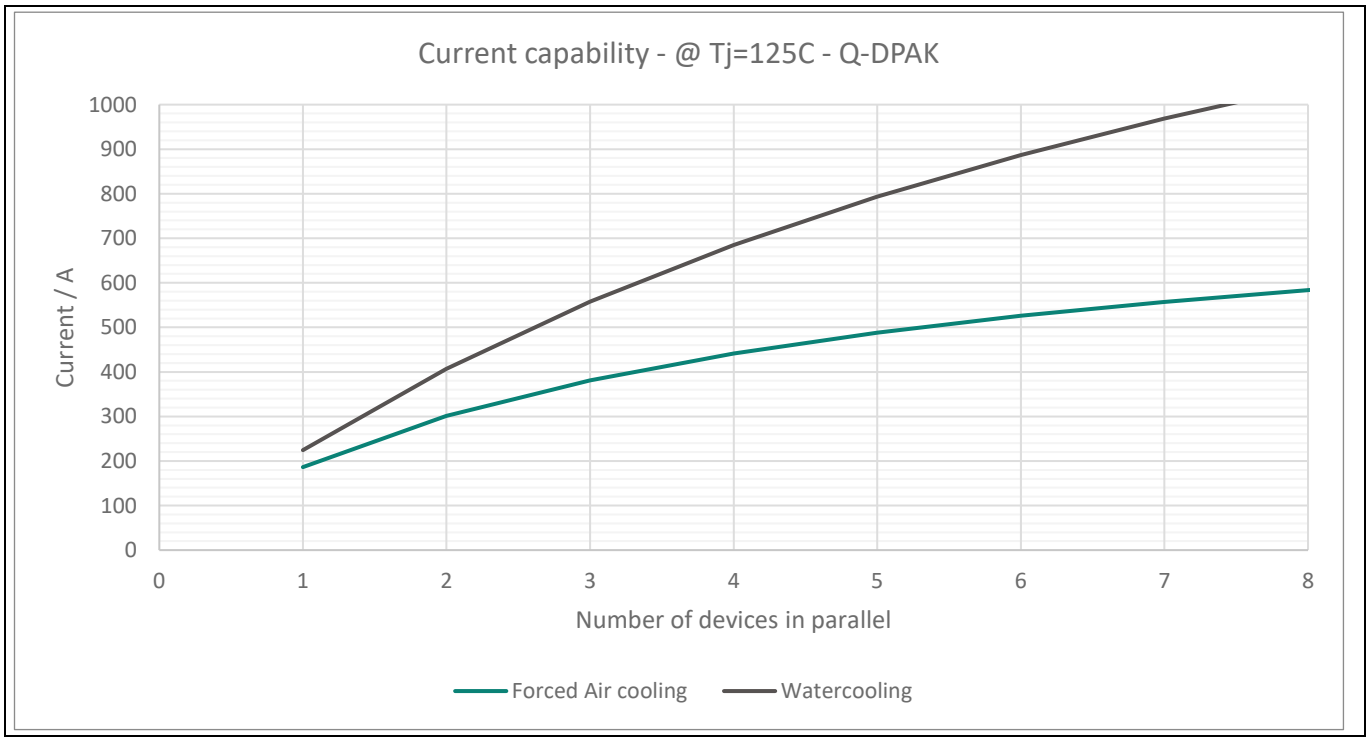


Figure 11 R_{th} calculations model

By selecting six power devices (IJCQ120RM25J1) in parallel, a current capability of 500 A with air cooling and 800 A with water cooling can be achieved.

4 Power switch overvoltage protection

When a power switch is used to switch an inductive load (e.g., wiring harness), the inherent behavior of this load generates a high-voltage spike during turn-off, commonly referred to as inductive kickback. If this induced voltage exceeds the power semiconductor's maximum drain-source voltage ($V_{DSS,max}$), it can lead to overvoltage stress, causing immediate breakdown or long-term degradation of the semiconductor. To prevent such damage and to ensure the reliable operation of the power semiconductor, a proper protection strategy must be implemented. Typically, this includes the use of freewheeling diodes, RC snubbers, metal oxide varistors (MOV), or transient voltage suppressors (TVS) to clamp the voltage spike caused by the inductive kickback effectively.

As the use of freewheeling diodes is not feasible in all application cases, a clamping network combination is used in the eBDU demonstrator REF-SSBD800VDCJCQJ1. The clamping network needs to be adapted to the requirements in the application. Several parameters such as switch-off current, power device breakdown voltage, or operating voltage range need to be considered. This chapter describes some of the clamping possibilities.

A typical clamping measurement when switching off an inductive load is shown in Figure 12. To emulate a low-impedance power source like a battery stack, the DC voltage supply was buffered with a 3.3 mF capacitor and a 5 µH inductor was used as the inductive load. The V_{gs} voltage controlling the power device, the V_{ds} voltage across the power device, and the current through the power device and the clamping network are shown in the graph. The measurement setup that was used is shown in Figure 13.

As discussed in section 2.2, the JFET technology simplifies the clamping circuitry by enabling the device to go into avalanche until the current is commutated to the clamping device, minimizing the need for a dedicated snubber circuit.

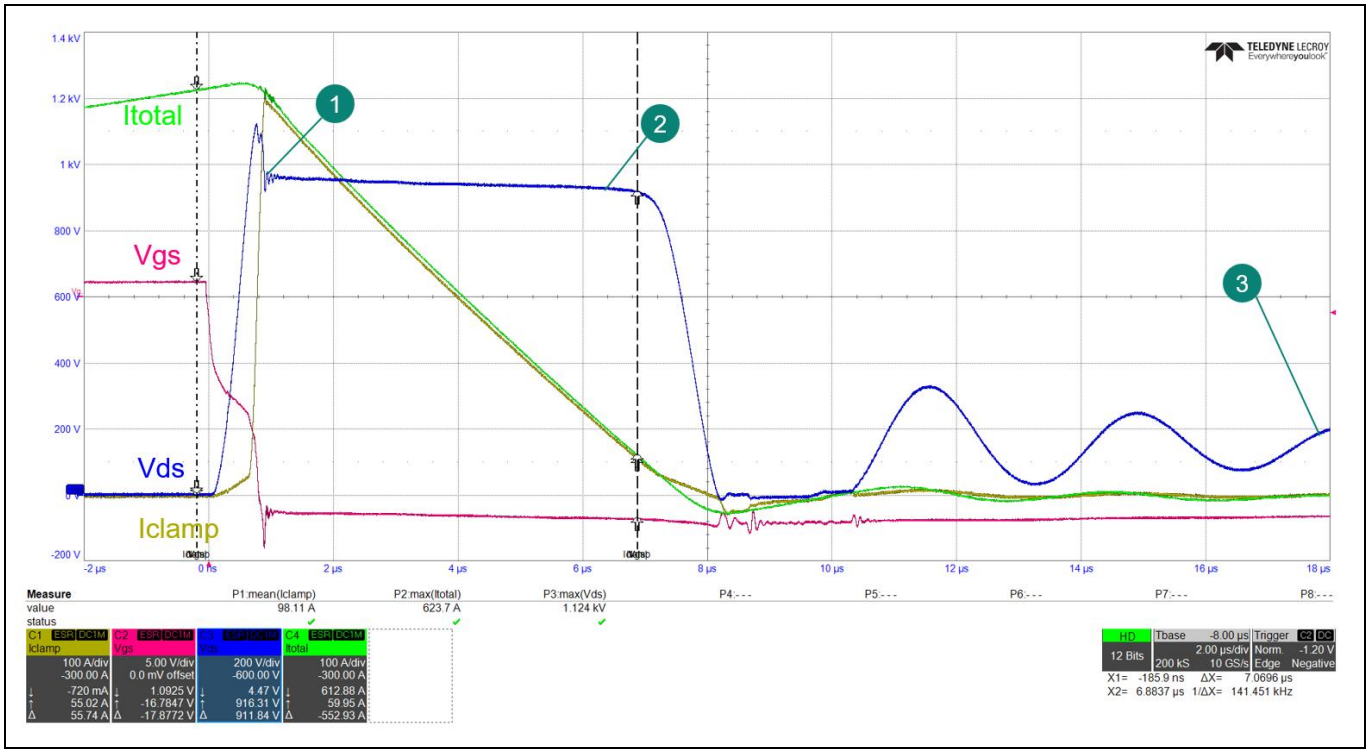


Figure 12 Measurement of a typical clamping event

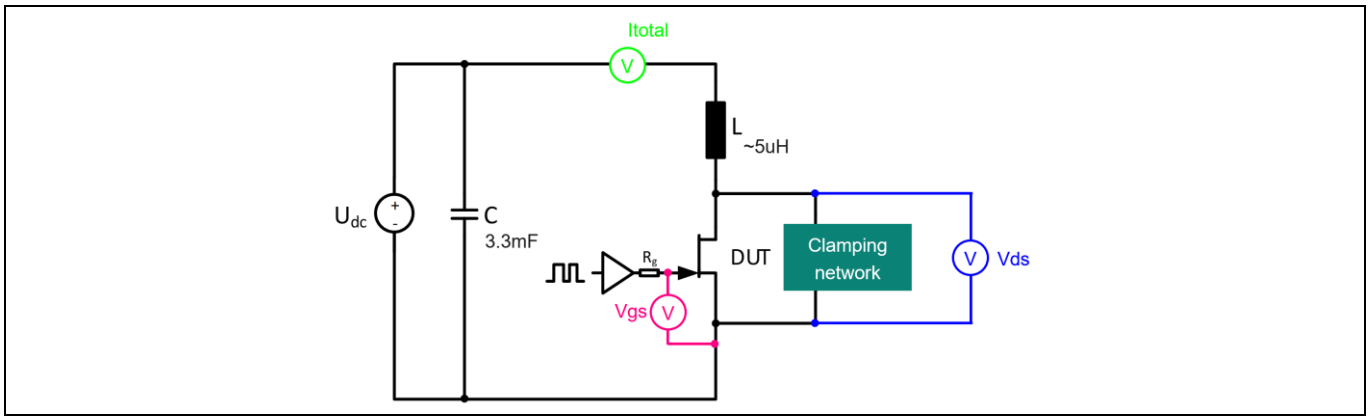


Figure 13 Clamping test measurement setup

The three operating points highlighted in Figure 12 are critical when designing a clamping network:

1. **Start of clamping**: After the initial short spike where the power device is in avalanche, the clamping network begins to conduct, and the current commutates from the power device (DUT) path to the clamping network. This avalanche occurs primarily due to the stray inductance between the DUT path and the clamping path, and it is achievable with Infineon CoolSiC™ JFET technology. JFET actively controls the avalanche effect and distribute the energy across the entire chip area, leading to a greater capability for managing critical energy compared to other power technologies (For more information refer to [7]).
2. **Clamping plateau**: In this phase, the clamping network is actively limiting the voltage and the current will decay based on the energy discharge in the inductance of the load.
3. **End of clamping**: The inductance is completely discharged and the current decayed. The clamping network will now be inactive and the voltage across the device (V_{ds}) will settle to the battery voltage (V_{dc}).

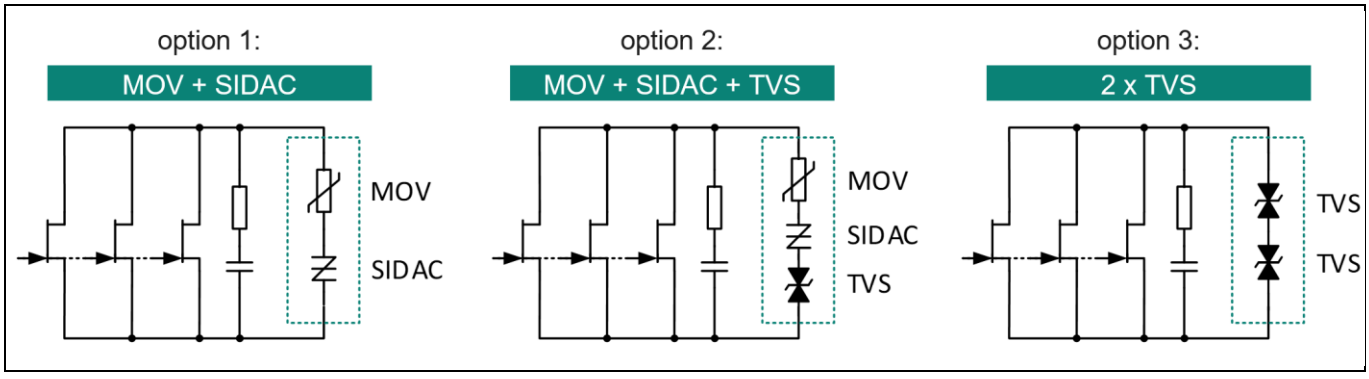


Figure 14 Clamping circuit options

Figure 14 shows different clamping circuit options, which are detailed in the upcoming sections. To reduce the leakage current when using an MOV as the clamping element, a silicon diode for alternating current (SIDAC) is used. The SIDAC starts conducting when the voltage reaches the switch-on voltage V_s and returns to the blocking mode when the current decays below the holding current I_H. For the calculations in this document, a SIDAC with a switching voltage of 400 V was selected (Littelfuse® P3500S3NLRP) [9]. Its electrical parameters are shown in Figure 15.

Electrical Characteristics

Part Number	Marking	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	I_H	I_S	I_T	V_T @I_T=2.2A	Capacitance @1MHz, 2V bias	
		V min	V max	mA min	mA max	A max	V max	pF min	pF max
P3100S3NLRP	P31N	275	350	50	800	2.2	4	150	450
P3500S3NLRP	P35N	320	400	50	800	2.2	4	150	450
P3800S3NLRP	P38N	350	430	50	800	2.2	4	150	450



Figure 15 SIDAC electrical parameters [9]

To select an MOV, the three clamping operating points should be considered. For comparison, the parameters were extracted from the datasheet of the TDK SIOV SuperioR S25 series. Figure 16 shows the MOV v/i characteristics graph. The first operating point is the MOV voltage at 1 mA – when the MOV starts getting conductive. The second point is the maximum clamp voltage at the switch-off current, which was chosen to be 1 kA in this example. The third operating point is the voltage when the current reaches the holding voltage of the SIDAC (50 mA) after the clamping event, so the SIDAC returns to the blocking state. Table 4 shows the values taken from the graph that were used for further calculations.

As a boundary for the calculations, the maximum operating battery voltage was defined as:

$V_{bat,max} = 850\ V$

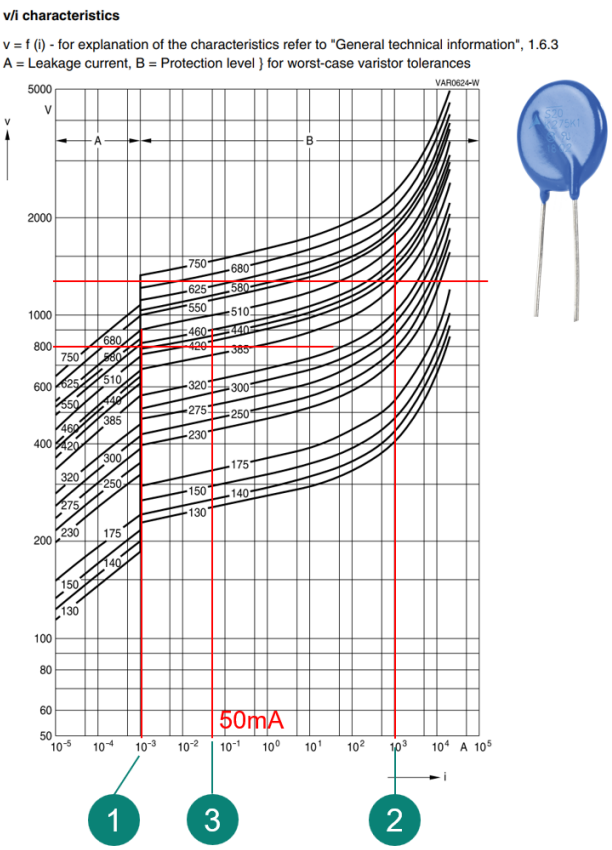


Figure 16 MOV v/i characteristics curve [10]

Table 4 **MOV v/i characteristics curve point of interests [10]**

	V_{mov} at 1 mA/V	V_{mov} at 50 mA/V	V_{mov} at 1 kA/V
MOV 320V - S25K320E4R12	510	568	932
MOV 385V - S25K385E4R12	620	689	1120
MOV 420V - S25K420E4R12	680	755	1230
MOV 460V - S25K460E4R12	750	833	1355

4.1 Clamping option 1: MOV + SIDAC

A SIDAC in series with a MOV can address the issue of leakage current in area A of the V/I characteristics shown in Figure 16. Figure 17 shows the results of the calculations for each clamping application case.

In the calculation, it can be observed that the clamping network starts to get conductive (case 1) below the minimum breakdown voltage of the power device. However in case 2, when MOVs rated 420 V or 460 V were used, the voltage plateau rose above the breakdown voltage of the power device. This means that these MOVs cannot effectively protect the power device for the given current range. On the other hand, using MOVs with lower voltage rating, e.g., 385 V or 320 V, imposes limitations on the maximum allowable battery voltage. Specifically, when the voltage across the MOV exceeds the breakdown voltage of the SIDAC, the SIDAC no longer enters its blocking mode, causing a constant current of more than 50 mA to flow through the clamping circuit.

In the calculated case, the maximum battery voltage would be restricted to 689 V for the 385 V MOV and 568 V for the 320 V MOV. Such limitations make these configurations unsuitable for systems with the chosen maximum operating voltage range.

Figure **18** shows a typical clamping event measurement using a 420 V MOV in series with the selected SIDAC. In this example, the battery voltage was set to 750 V, and after the clamping event concluded, the voltage dropped below the defined maximum of 850 V.

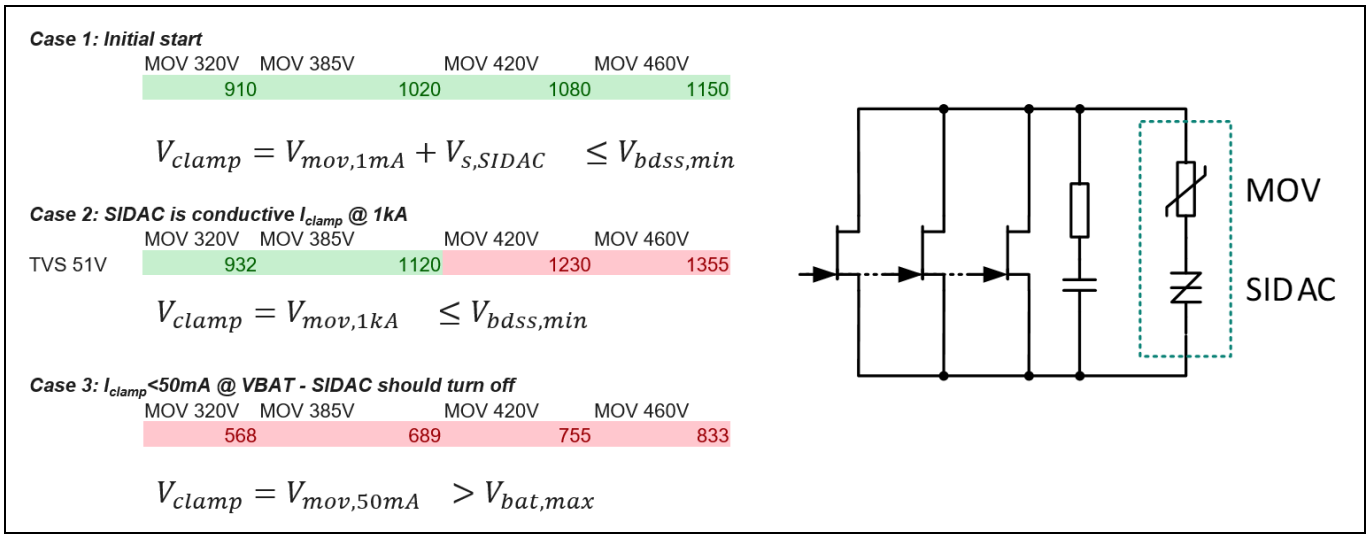


Figure 17 Clamping option 1: MOV + SIDAC calculation results

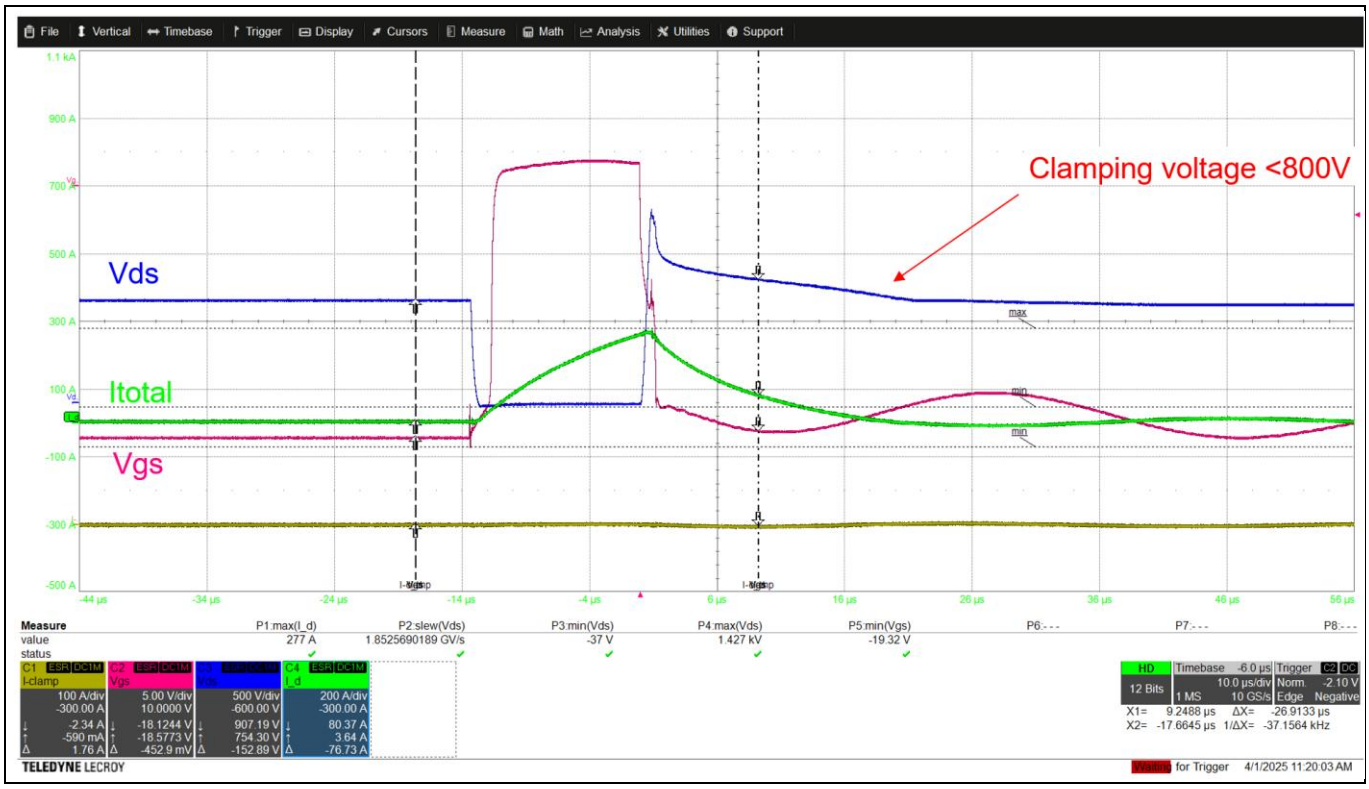


Figure 18 **Clamping option 1: Clamping measurement at V_{bat} = 750 V**

4.2 Clamping option 2: MOV + SIDAC + TVS

To increase the usable battery voltage when using an MOV as the clamping element, a TVS diode can be placed in series with the MOV. The primary role of the TVS diode in this configuration is to increase the voltage handling capability of the MOV in case 3 (maximum V_{bat}). For this purpose, TVS diodes with voltage ratings of up to 110 V were selected. Table 5 summarizes the key parameters of the chosen TVS diodes, as given in their respective datasheet. It is important to note that achieving the required current rating may necessitate the use of multiple TVS diodes connected in parallel.

Table 5 **LV TVS diodes parameters [11][12]**

	$V_{br,min}$/V	$V_{br,max}$/V	$V_{c,max}$/V	$I_{c,max}$ (8/20)/A
TVS 51V - 8.0SMDJ51CA	56.7	62.7	106.5	631
TVS 75V - 8.0SMDJ75CA	83.3	92.1	156.3	430.5
TVS 78V - 8.0SMDJ78CA	86.7	95.8	162.8	412.8
TVS 85V - 8.0SMDJ85CA	94.4	104	177	379.6
TVS 90V - 8.0SMDJ90CA	100	111	188.6	357.5
TVS 100V - 8.0SMDJ100CA	111	123	209.3	321.1
TVS 110V - 8.0SMDJ110CA	122	135	228.7	293.8
LTKAK10-076C	85	95	140	10000
LTKAK10-086C	95	105	157	10000

Design considerations for a dedicated power stage

Power switch overvoltage protection

This calculation results for clamping option 2 are shown in Figure 19. For 850 V battery voltage systems, the option with a 420V MOV would be the best fit. With this combination, the maximum clamping voltage in case 2 at 1 kA would exceed the maximum allowable drain-source voltage of the power device. To address this issue, several MOVs need to be connected in parallel to reduce the current flowing through each individual MOV, which in turn would lower the clamping voltage. Alternatively, a power device with a higher breakdown voltage $V_{DSS,max}$ can be used.

With a 320 V MOV, the breakdown voltage will stay below the $V_{DSS,max}$, but the maximum V_{bat} voltage is limited to 690 V. Figure 20 shows typical measurements with a 420 V MOV, a SIDAC, and a 90 V TVS diode.

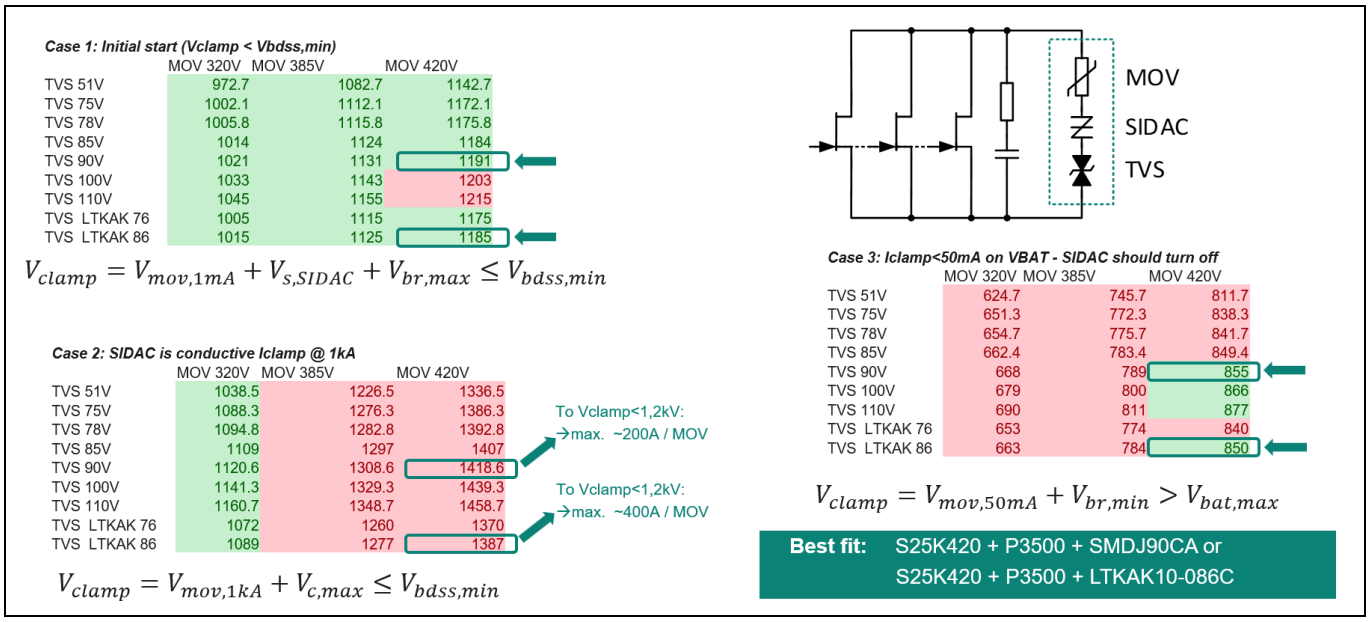


Figure 19 Clamping option 2: Calculation results for an MOV + SIDAC + TVS

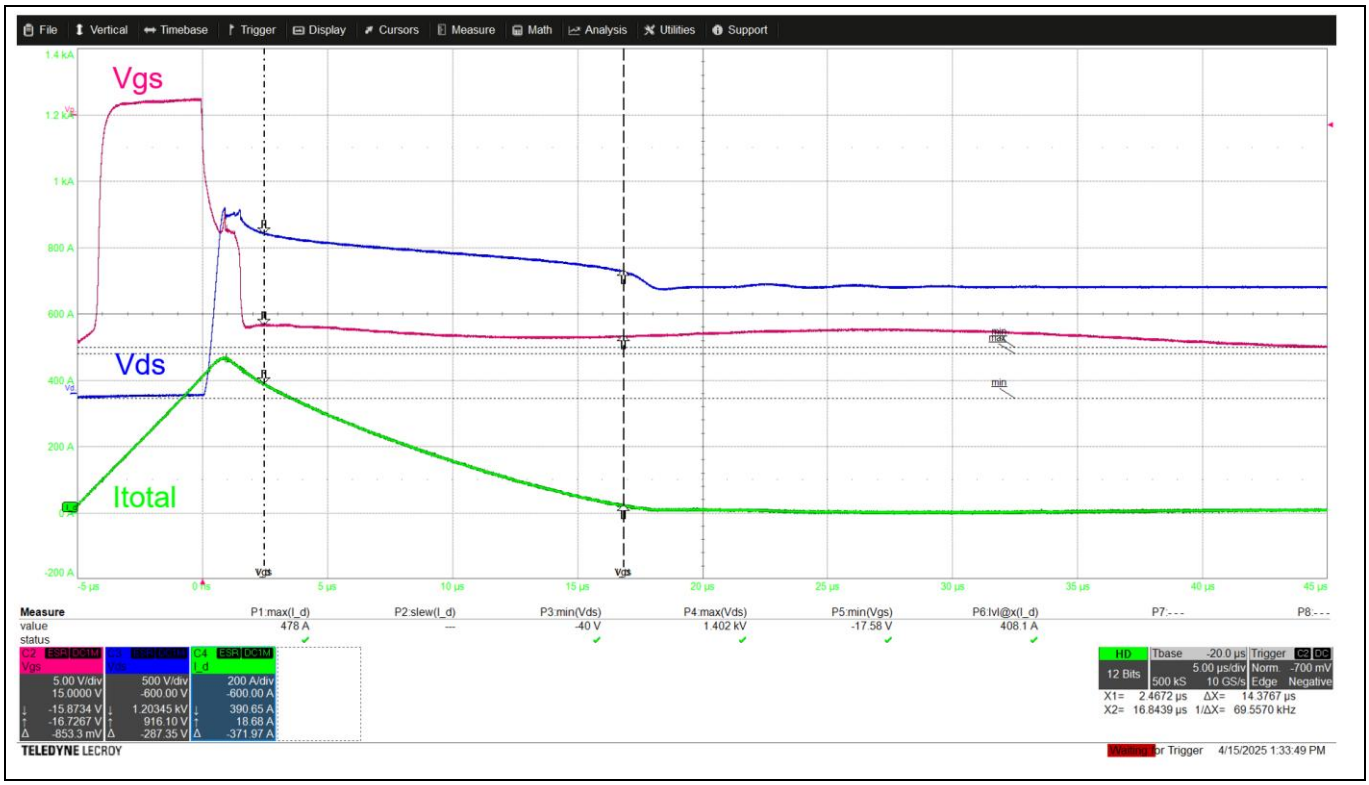


Figure 20 Clamping option 2: Clamping measurement at V_{bat} = 800 V, 480 A (420 V MOV, 90 V TVS)

4.3 Clamping option 3: High-power TVS diodes

Another option to limit the maximum voltage during an inductive kickback is to use transient voltage suppressor (TVS) diodes. Characteristically, a TVS diode does not exhibit such a high voltage/current dependency, resulting in a more precise clamping voltage. High-power TVS diodes used in these calculations were the AKx series from Littelfuse® and the PTVS series from Bourns®. Table 6 lists the datasheet values for the chosen diodes. For the maximum clamp voltage $V_{c,max}$, a simulated value at 3 kA was used for the 10 kA diodes. [12][14][15]

Table 6 **High-power TVS diode parameters [12][14][15][16]**

	$V_{br,min}$/V	$V_{br,max}$/V	$V_{c,max}$/V	$I_{c,max}$ (8/20)/A
Littelfuse® AK3-430C	440	490	625	3000
Littelfuse® AK10-430C	440	490	625 (~550 V at 3 kA)	10000
Bourns® PTVS10-470C	470	530	630(~610 V at 3 kA)	10000
Littelfuse® AK10-530C	560	619	750(~650 V at 3 kA)	10000
Yageo HFA-430L	440	500	625	3000

The selected TVS diodes are typically used for surge protection applications, where a snapback characteristic can be advantageous for the protection voltage level of the diodes. The snapback characteristic allows the diodes to reduce their clamping voltage during a surge (conductive) event and then gradually recover to their original breakdown voltage after the event has subsided. Figure 21 shows the behavior of the snapback characteristic in the respective datasheets.

With this behavior, it is important that the snapback voltage level remains above the battery voltage in this application use case. However, for protecting the power devices from inductive kickback, a TVS diode without snapback characteristics (e.g., HFx-430L) would be more suitable.

As the snapback voltage is not specified in the datasheets of the selected components listed in Table 6, the compatibility of the possible TVS diode combinations must be validated through measurements to ensure proper functionality in a given use case. A typical measurement with a snapback behavior is shown in Figure 22. In this measurement, the voltage dropped to ~750 V during the surge event, which makes this diode combination only suitable for battery voltages up to 750 V.

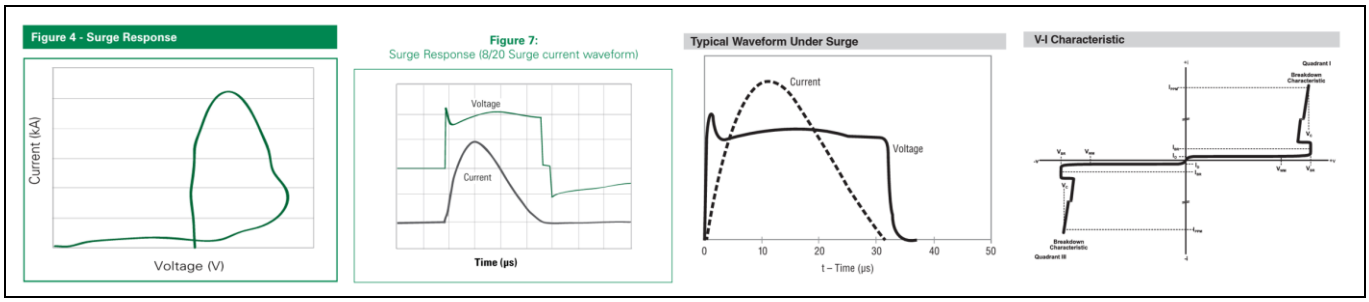


Figure 21 Snapback characteristics of different TVS diodes [14][15]

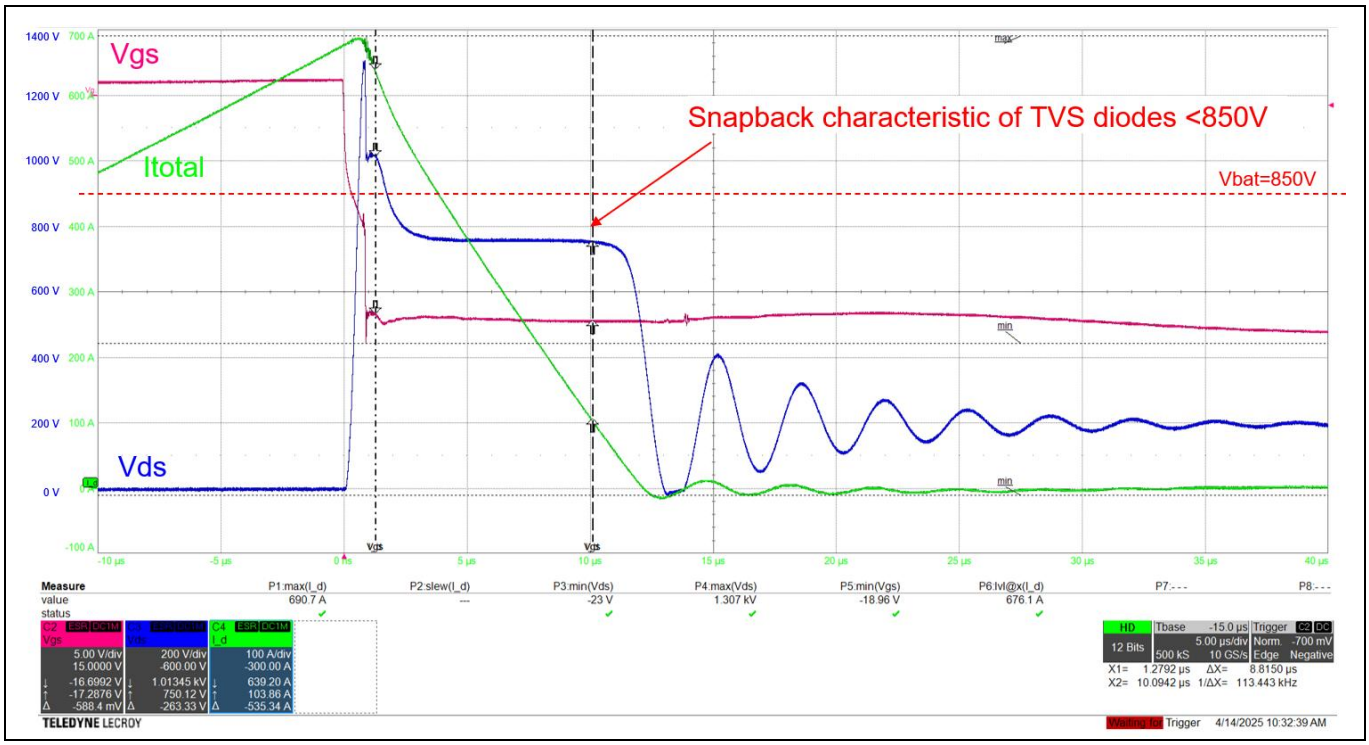


Figure 22 Measurement of the snapback characteristics of two PTVS10-430C in series

The calculation results for various TVS diode combinations are presented in Figure 23. These calculations considered the maximum clamping voltage at a current level of 3 kA. Among the evaluated combinations, the pairing of AK10-430C and AK10-530C proved to be the most suitable, as it met all the specified requirements.

With the combination of two PTVS10-470 or two HFA-430L devices, the maximum clamp voltage would be exceeded at 3 kA. However, given that the switch-off current in the application is not expected to reach this level, this combination can also be considered a viable solution for the intended use case. If higher switch-off

current is required, the HFx-L-430L is available with higher current ratings as well. Typical clamping measurements using these combinations are shown in Figure 24 and Figure 25.

Series connection of different TVS diodes; Vc,max @3kA

Case 1: Initial start (Vclamp < Vbdss,min)

	Vclamp,1
TVS 2xAK3-430	980
TVS 2xPTVS10-470	1060
TVS 2xAK10-530	1238
TVS AK10-530+430	1109
TVS HFA-430L	1000

$$V_{clamp} = 2 \cdot V_{br,max} \leq V_{bdss,min}$$

Case 2: Max clamp voltage Iclamp @ 3kA

	Vclamp,2
TVS 2xAK3-430	1250
TVS 2xPTVS10-470	1220
TVS 2xAK10-530	1300
TSV AK10-530+430	1200
TVS HFA-430L	1250

$$V_{clamp} = 2 \cdot V_{c,max} \leq V_{bdss,min}$$

Case 3: Min clamping voltage > Vbat,max

	Vclamp,3
TVS 2xAK3-430	880
TVS 2xPTVS10-470	940
TVS 2xAK10-530	1120
TSV AK10-530+430	1000
TVS HFA-430L	880

$$V_{clamp} = 2 \cdot V_{br,min} > V_{bat,max}$$

Best fit: AK10-430C + AK10-530C
or 2 x PTVS10-470
or 2 x HFA-430L

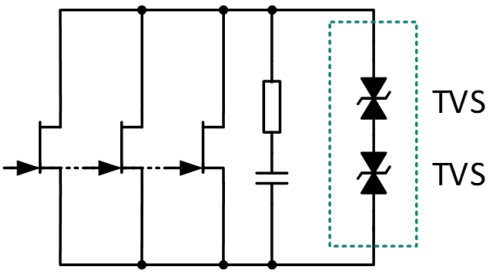


Figure 23 Clamping option 3: 2 x TVS calculation results

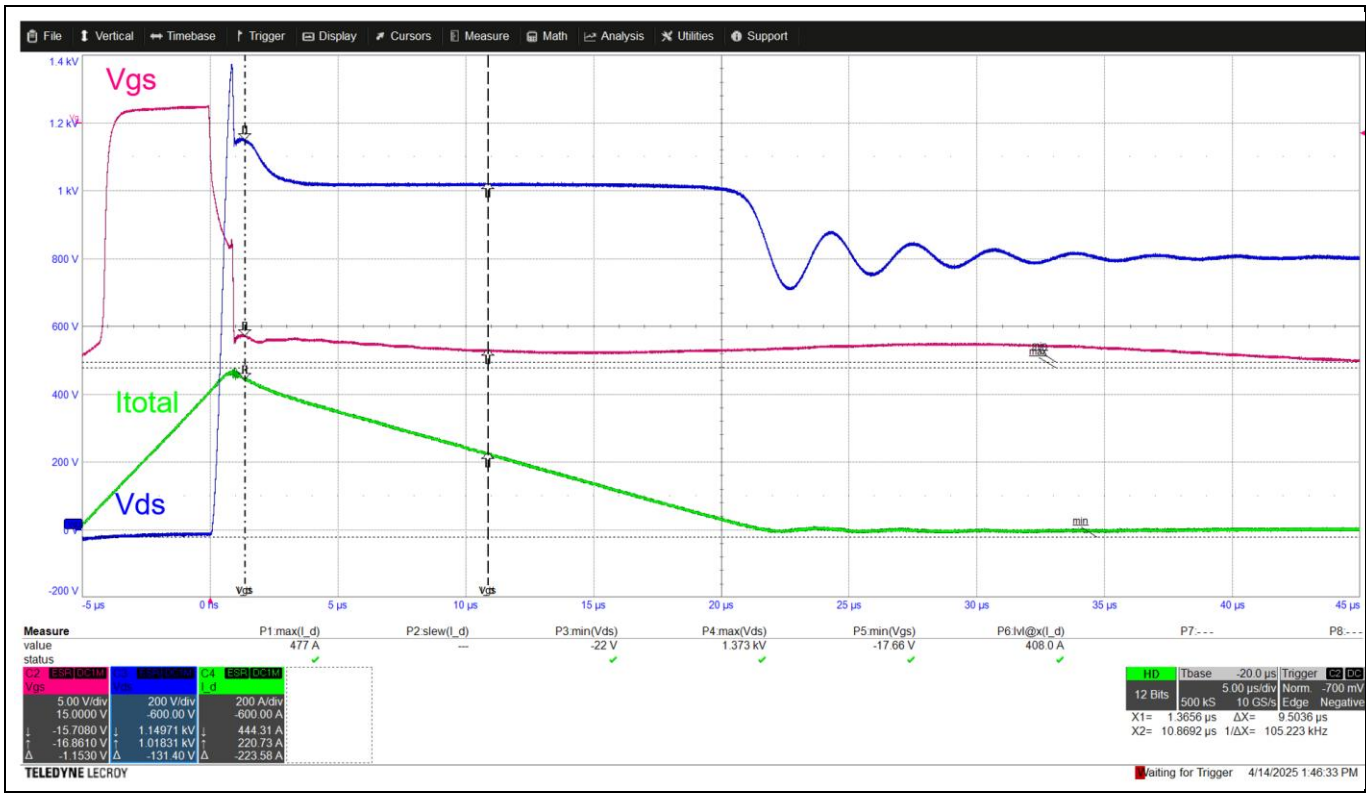


Figure 24 Clamping option 3: Clamping measurement at V_{bat} = 800 V, 480 A (AK10-530C + AK10-430C)

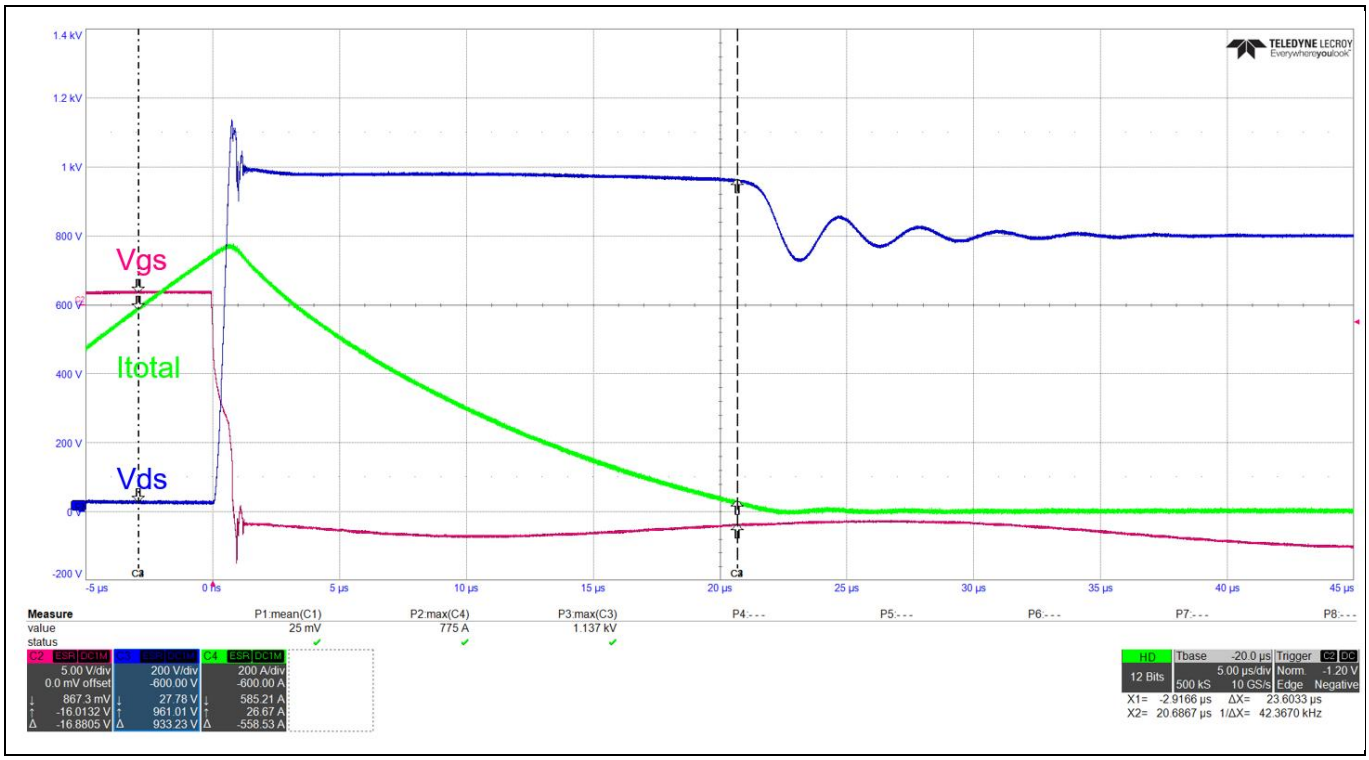


Figure 25 Clamping option 3 – Clamping measurement at V_{bat} = 800 V, 780 A (2 x HFA-430L)

4.4 Maximum clamping energy

As the use case for this clamping circuit is to protect the power device from the high voltage caused by the inductive kickback, the maximum energy handling capability of the circuit is one of the key aspects. In contrast to MOVs that are typically used in this application, the main application of the TVS diodes is of surge protection. In this case, TVS diodes usually do not specify the maximum energy handling capability but instead the maximum current capability or power for a given surge test pulse.

To find the energy handling limits of the aforementioned clamping circuits, their energy handling capability needs to be calculated. For this, the specification for the 8/20 µs surge pulse is used from the datasheets.

The 8/20 µs surge pulse defined by the IEC standard 61000-4-5 is shown in Figure 26.

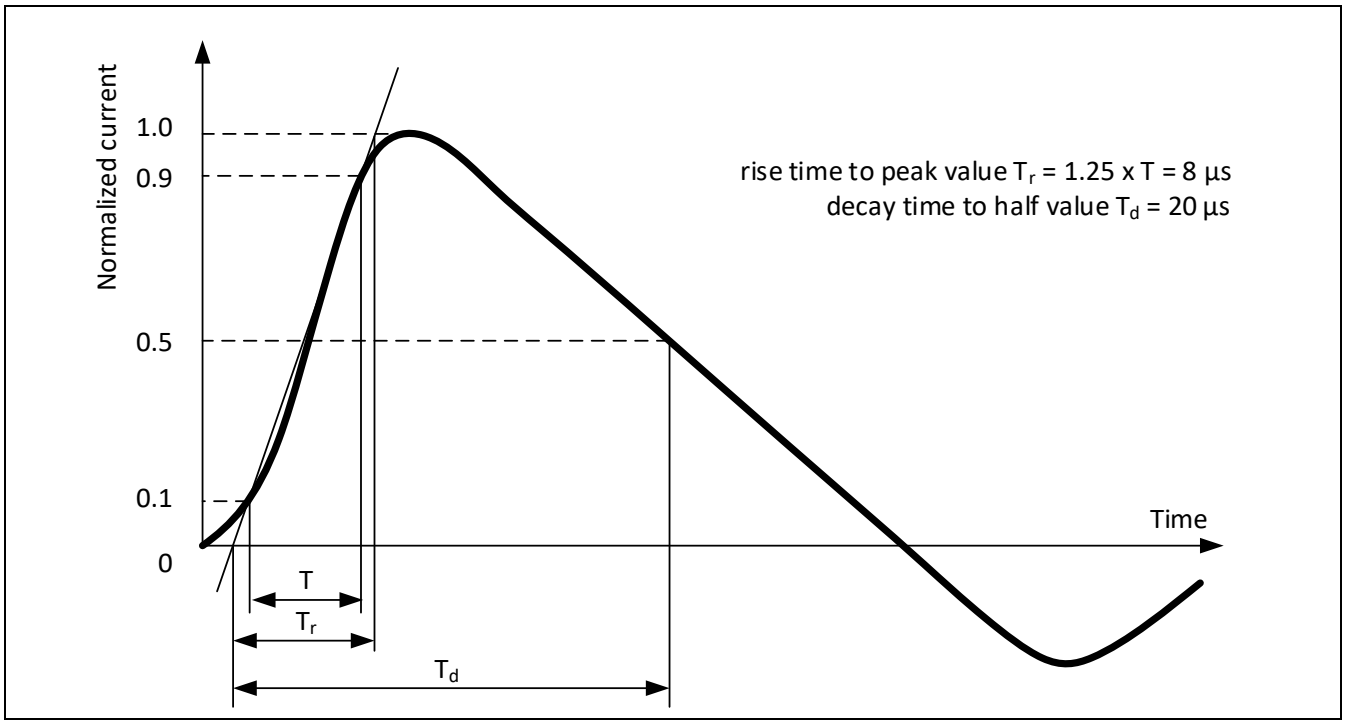


Figure 26 Definition of the 8/20 µs surge pulse according to IEC 61000-4-5 [17]

The energy contained in the surge pulse can be calculated using the charge and discharge curve of a capacitor. By separating the charging and discharging path, the energy can be calculated for each charge and discharge segment accordingly:

$$E \approx \int_0^{5\tau} u(t) \cdot i(t)\, dt = u_0 \cdot i_0 \int_0^{5\tau} \left(1 - e^{-\frac{t}{\tau}}\right) \cdot e^{-\frac{t}{\tau}}\, dt$$

$$E \approx \frac{1}{2} u_0 \cdot i_0 \cdot \tau$$

The rise time is given until the peak current has been reached. The value of τ_{rise} can then be calculated as:

$$i_{rise}(t) = I_0 \left(1 - e^{-\frac{t}{\tau_{rise}}}\right) \quad \rightarrow \quad t = -\ln\left(1 - \frac{i(t)}{I_0}\right) \cdot \tau_{rise}$$

$$t_{10\%} = -\ln(1 - 0.1) \cdot \tau_{rise} = -\ln(0.9) \cdot \tau_{rise} = 0.105 \cdot \tau_{rise}$$

$$t_{90\%} = -\ln(1 - 0.9) \cdot \tau_{rise} = -\ln(0.1) \cdot \tau_{rise} = 2.303 \cdot \tau_{rise}$$

With the definition of T_r = 1.25 x T = 8 µs:

$$T = \frac{T_R}{1.25} = t_{90\%} - t_{10\%} = \tau_{rise} \cdot (2.303 - 0.105)$$

$$\tau_{rise} = \frac{T_R}{1.25 \cdot (2.303 - 0.105)} = \frac{T_R}{2.747} = \frac{8\ \mu s}{2.747}$$

For the decay, the time until 50% of the peak value is defined. With this, τ_{fall} can be calculated as:

$$i_{fall}(t) = I_0 \left(e^{-\frac{t}{\tau_{fall}}}\right) \quad \rightarrow \quad t = -\ln\left(\frac{i(t)}{I_0}\right) \cdot \tau_{fall}$$

$$t_{50\%} = -\ln(0.5) \cdot \tau_{fall} = 0.693 \cdot \tau_{fall}$$

With $t_{50\%} = T_d - T_r = 12\ \mu s$:

$$\tau_{fall} = \frac{t_{50\%}}{0.693} = \frac{12\ \mu s}{0.693}$$

With these calculations the energy of the 8/20 pulse can be calculated and thus, the energy capability of the TVS diode for a clamping element can be estimated. As an inductive kickback event has different time constants than a surge pulse, this calculation only gives an indication. Table 7 lists the results of energy calculation for each diode individually.

Table 7 **High-power TVS diodes energy calculations**

	$V_{c,max}$/V	$I_{c,max}$ (8/20)/A	E_rise/J	E_fall/J	E_total/J
TVS 90V - 8.0SMDJ90CA	188.6	357.5	0.1	0.58	0.682
TVS 100V - 8.0SMDJ100CA	209.3	321.1	0.1	0.58	0.680
LTKAK10-076C	140	10000	2.04	12.12	14.2
LTKAK10-086C	157	10000	2.29	13.59	15.9
AK3-430C or HFA-430L	625	3000	2.73	16.23	19.0
AK10-430C or HFC-430L	625	10000	9.10	54.10	63.2
Bourns® PTVS10-470C	630	10000	9.18	54.53	63.7
Littelfuse® AK10-530C	750	10000	10.92	64.92	75.8
Yageo HFB-430L	625	6000	5.46	32.46	37.9

The energy capability of different possible clamping implementations is shown in Figure 27.

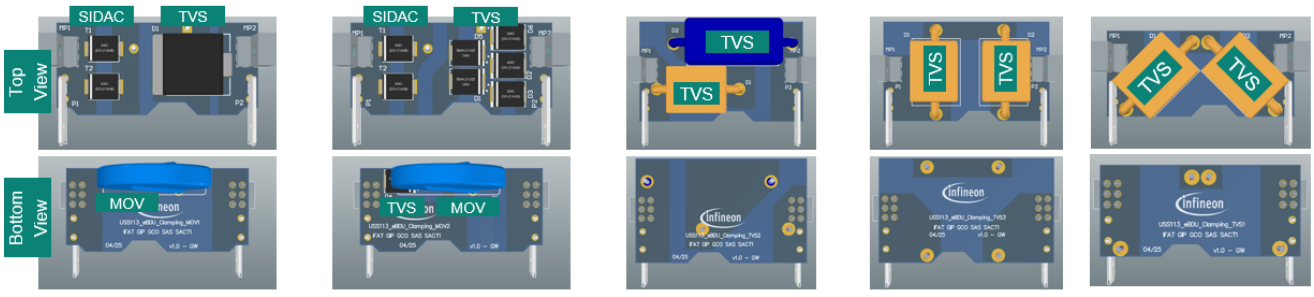


Figure 27 Energy capability of different clamping options

The required clamping energy depending on the switch-off current and the inductance of the switching path can be calculated using:

$$E_{clamp} = \frac{L \cdot I_{switch,off}^2}{2}$$

Figure 28 shows the different clamping energy requirements at different switch-off inductance and current levels with an overcurrent shutdown commit time of 2 µs.

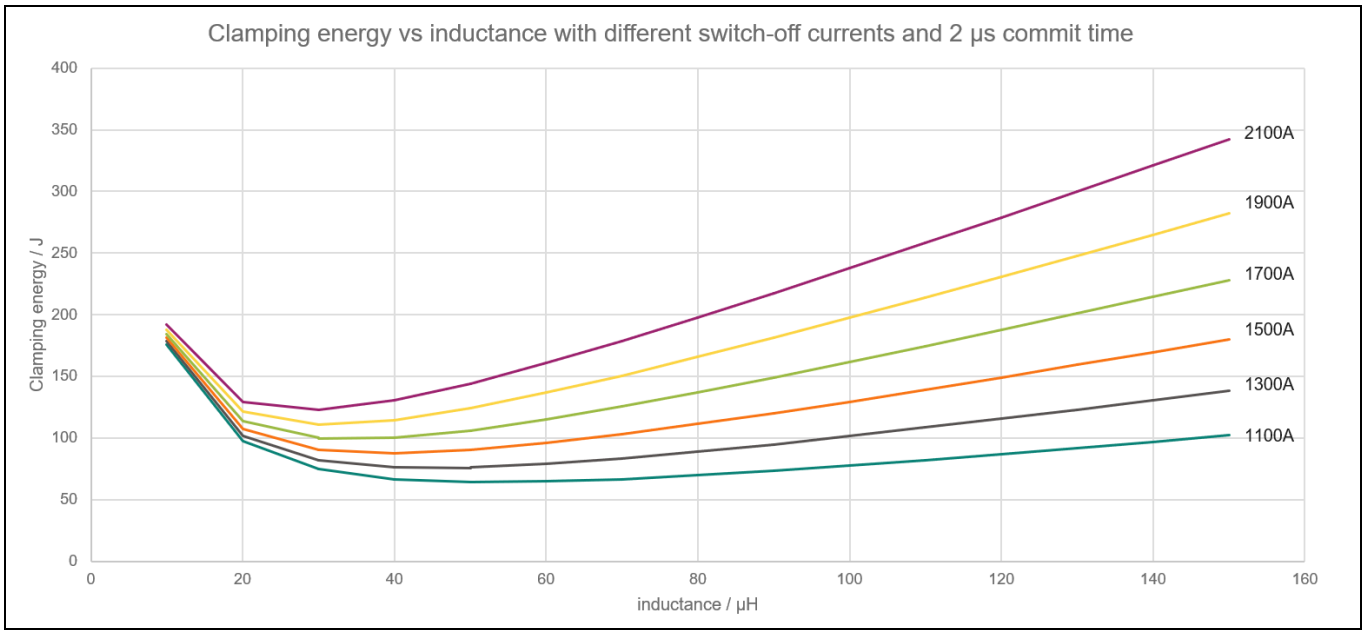


Figure 28 Energy requirements at different switch-off inductance and current levels with a commit time of 2 µs

With a maximum switch-off current of 1500 A, the maximum inductance for the selected clamping circuit is shown in Figure 29.

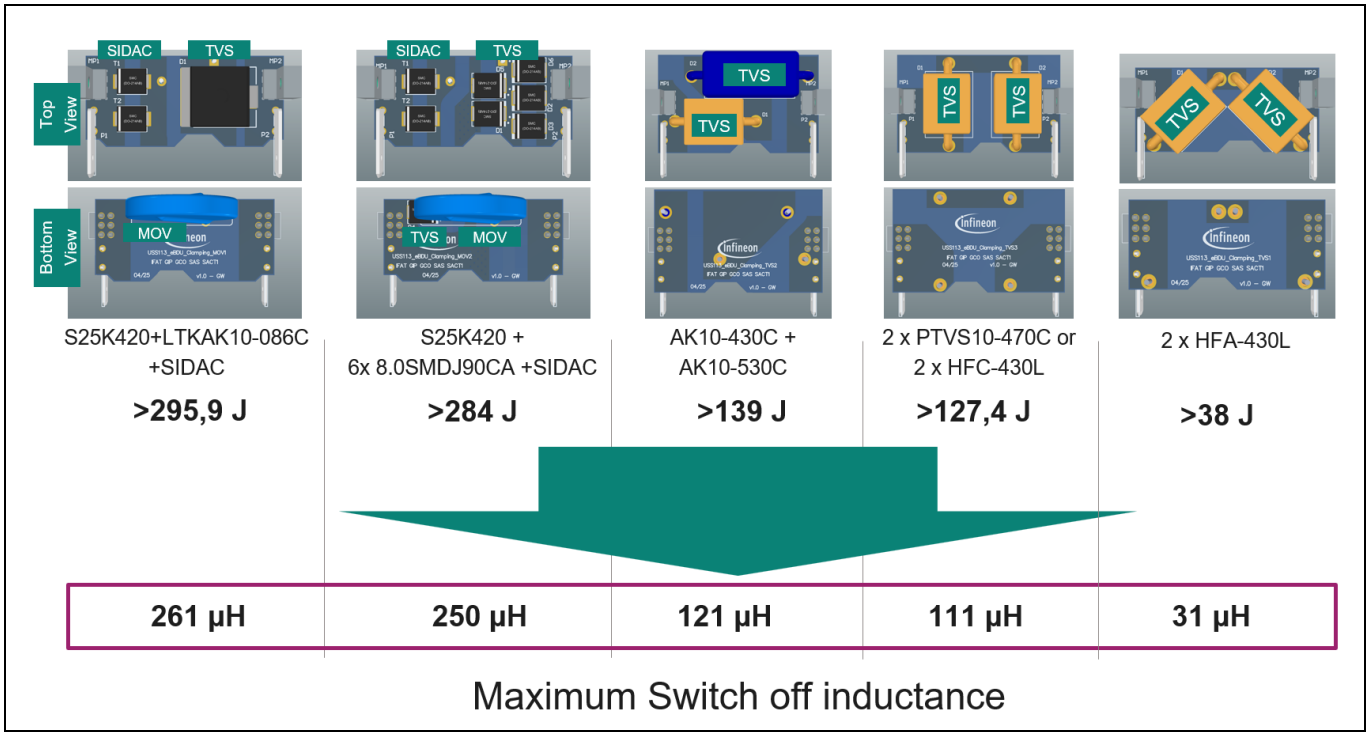


Figure 29 Energy requirements for different switch-off inductances and current levels

The energy requirements calculated previously represent a simplified worst-case scenario in which the clamping device is assumed to absorb all energy stored in the wiring harness. In practice, a portion of this energy is dissipated as resistive (ohmic) losses in the harness conductors.

Consequently, the energy that the clamping device absorbs for a given inductive load is lower than the worst-case estimate. Figure 30 shows a simplified simulation of a short-circuit event with a harness modeled as L = 100 µH and series R = 50 mΩ.

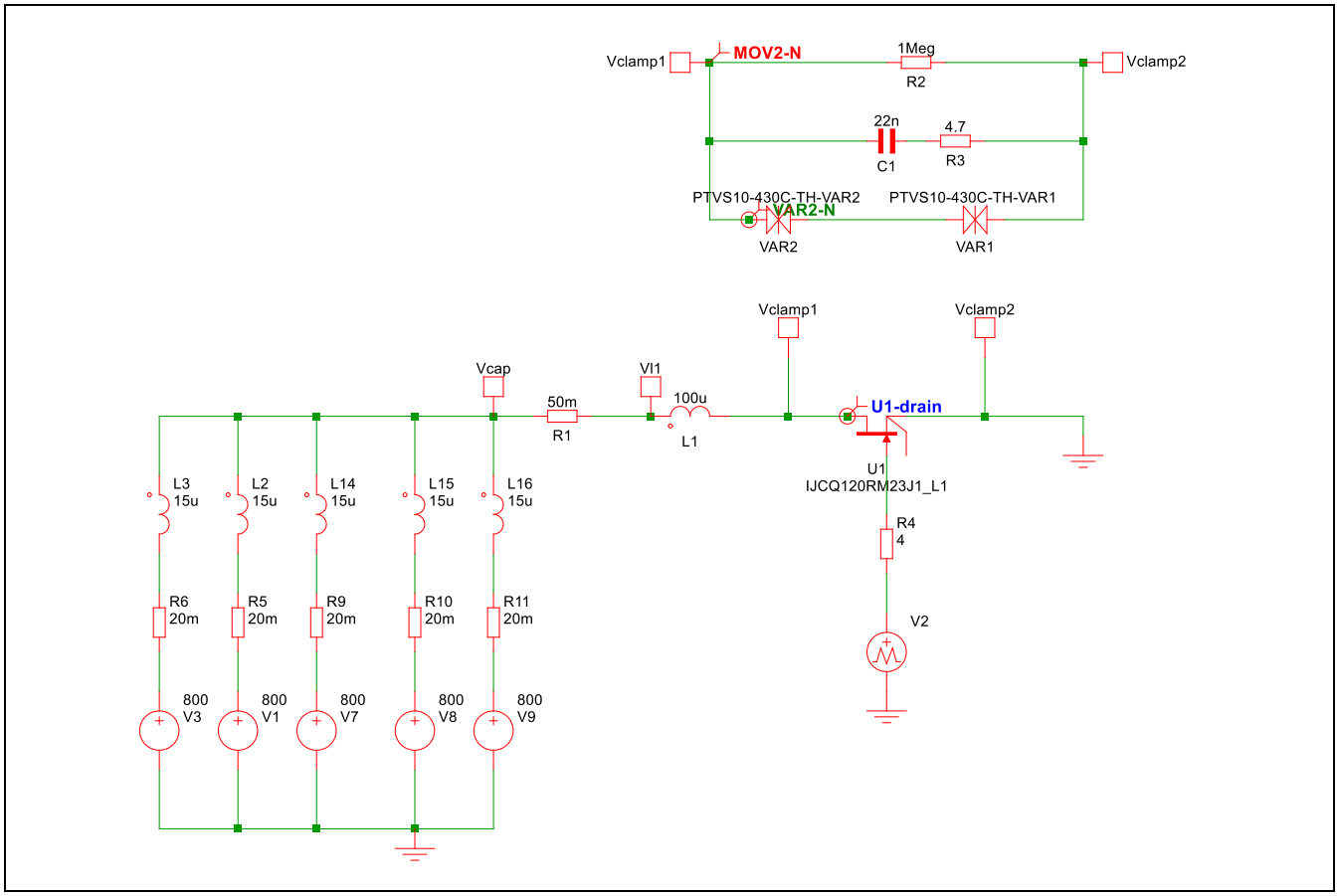


Figure 30 Short-circuit energy simulation model

Figure 31 shows the simulation of a 1.5 kA short-circuit turn-off event. At t = 200 µs, the power device turns off and the fault current commutates into the clamping network. At this instant, the energy stored in the wiring inductance L1 is ~108 J. After the current decays to zero, the clamping elements dissipate about 91 J, while the remaining ~16 J is dissipated in the wiring harness resistance modeled by R1.

This way, the required energy rating of the clamping device can be lower than the worst-case estimate and should be sized considering the wiring harness's ohmic losses.

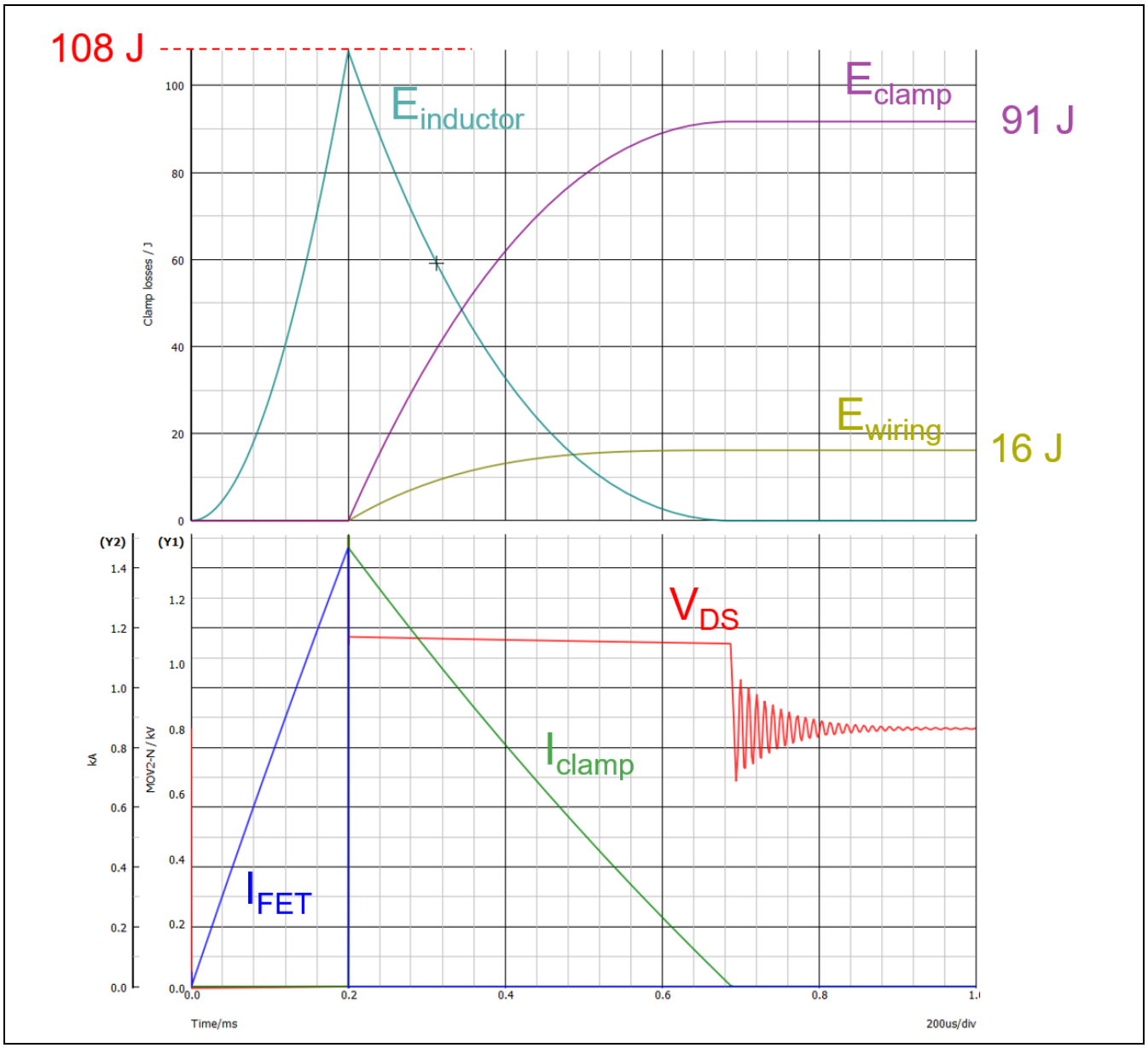


Figure 31 Results of a short-circuit energy simulation

4.5 The RC snubber

Another common solution for protecting the power devices from overvoltage caused by the inductive kickback is using an RC snubber circuit. Considering that the full clamping energy (e.g., 127.4 J) needs to be stored in a capacitor with a maximum voltage $V_{bdss,min}$, the required capacitance value can be calculated as:

$$C_{clamp} = \frac{2 \cdot E_{clamp}}{V_{bdss,min}} = \frac{2 \cdot 127.4}{1200} = 176.9\ \mu F$$

Capacitors with such capacitance and voltage ratings are large and therefore not considered as a viable option for clamping the full energy of the system in this application. For applications with lower switch-off current or clamping energy requirement like an auxiliary fuse, this solution can still be considered and needs to be assessed for the specific requirements.

However, a smaller RC snubber can still be beneficial in reducing the voltage slew rate and improve the switching behavior of the power stage. In the eBDU demonstrator REF-SSBD800VDCJCQJ1, a 4.7 Ω resistor and 22 nF capacitor are used to improve the commutation between the power switches and clamping circuit. Figure 32 shows the behavior of a switch-off with and without a snubber circuitry.

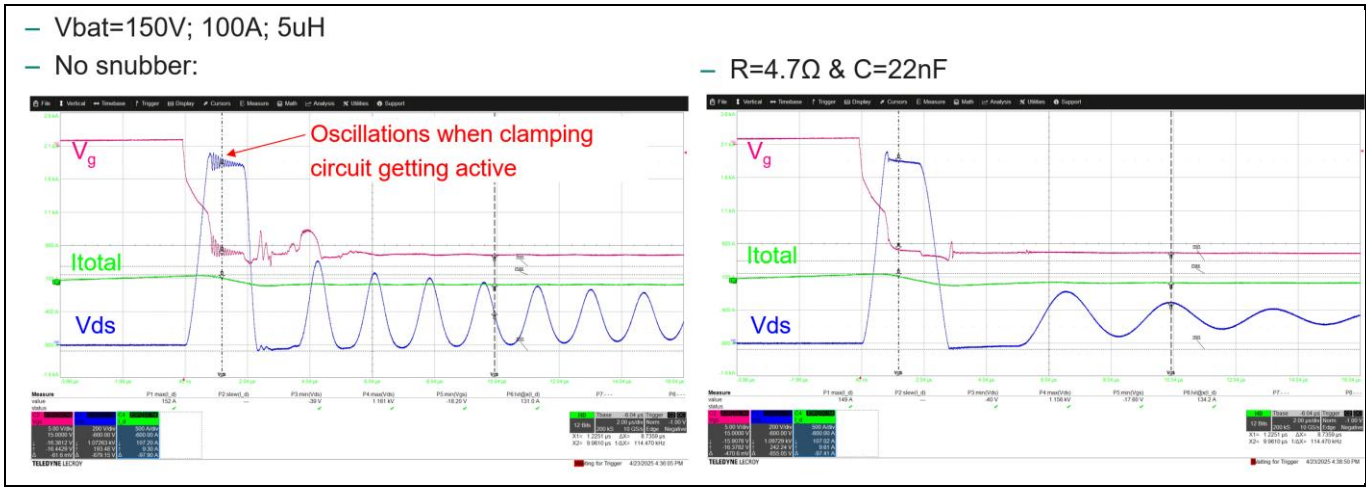


Figure 32 Measurement of a switch-off using an RC snubber

4.6 Freewheeling diode

To minimize the energy dissipated in the clamping circuit during short-circuit turn-offs, a freewheeling diode can be used. The freewheeling diode can only redirect a portion of the energy back to the battery.

Figure 33 shows an example with a freewheeling diode when a semiconductor switch is used in the negative pole of the battery pack. In this configuration, the inductive kickback energy generated by the wiring harness outside the battery can be rerouted through the freewheeling diode and fed back into the battery. However, it is important to note that the energy stored in the inductance of the battery pack itself will still dissipate within the clamping network of the power switch.

The effectiveness and practicality of incorporating a freewheeling diode depends largely on the system's architecture and specific implementation options. For example, in systems with a centralized battery main switch or in a DC-charging port, the advantages of a freewheeling diode may be lesser. Additionally, because the operation of a freewheeling diode requires access to the second pole of the battery, it may not always be feasible to implement this approach. Considering these constraints, the freewheeling diode has not been implemented in the design of the eBDU demonstrator REF-SSBD800VDCJCQJ1.

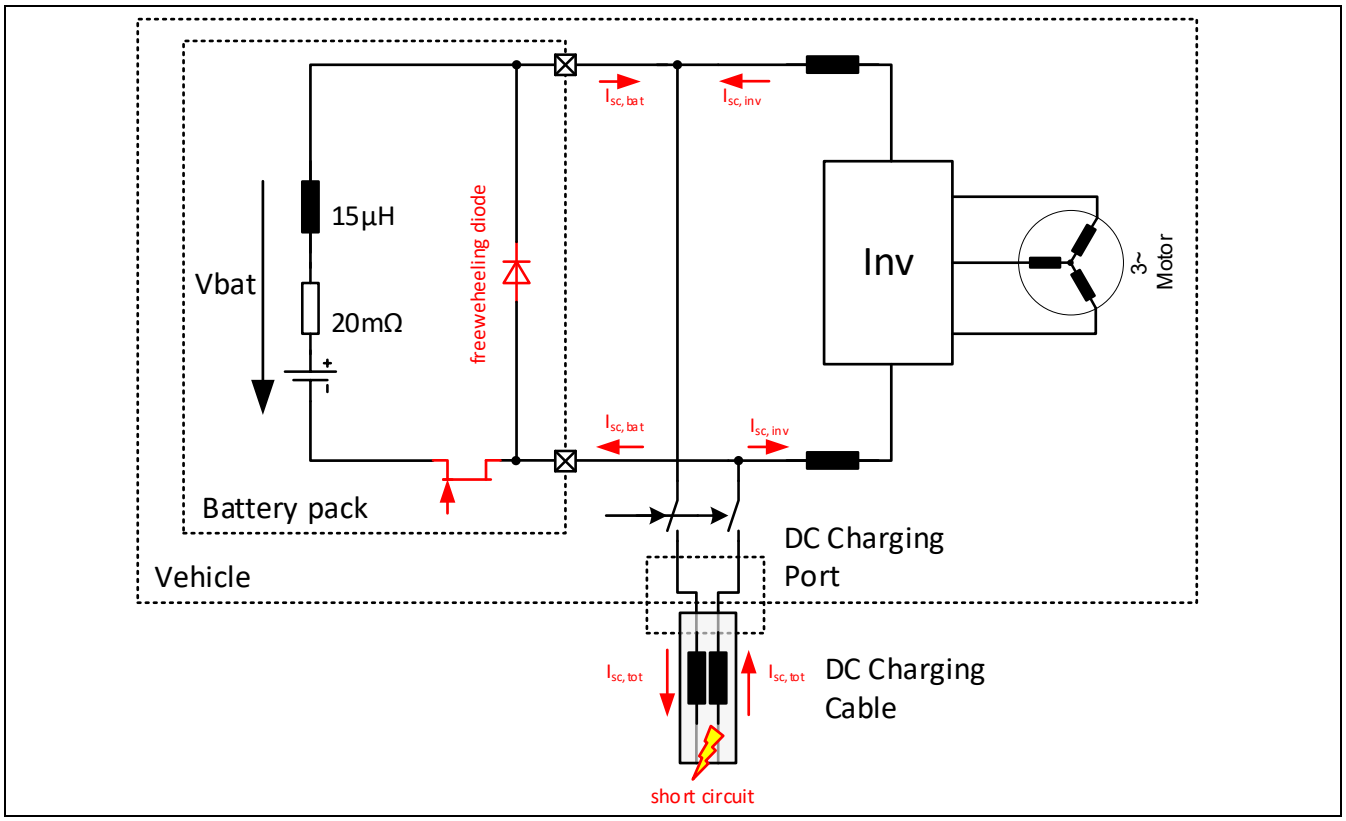


Figure 33 Short-circuit currents with a freewheeling diode

5 Fast overcurrent detection

As discussed in section 1.1, one of the key advantages of an electronic battery disconnect unit is its ability to perform a fast switch-off in an overcurrent or a short-circuit event. Achieving this functionality relies heavily on the rapid and accurate detection of overcurrent events, which necessitates the use of a high-performance current sensor. The speed and precision of the current sensor are critical to ensure that the system can respond promptly, protecting the battery and connected circuitry from potential damage.

For this case, Infineon coreless magnetic current sensor TLE5571 is used. With its tunnel magneto resistance (TMR) technology, the sensor achieves a maximum bandwidth of 2.5 MHz and a maximum overcurrent detection delay of 150 ns [18]. By using an external current sensing structure, additional (insertion) resistance can be minimized. This can significantly lower the power loss in the system compared to sensors with integrated current rail or shunt resistors. It is important to note that the sensing structure contributes significantly to the overall system response time and must be considered when designing the system.

Unlike a busbar without sensing structure, the current sensing structure designed for this application provides a sensitivity of ~2.97 µT/A and adds a resistance of ~0.6 µΩ. Figure 34 illustrates the integration of the TLE5571 sensor into the busbar within the eBDU demonstrator REF-SSBD800VDCJCQJ1. This integration highlights a compact and efficient design in which the sensor is positioned such that it accurately measures the magnetic field generated by the current flowing through the busbar.

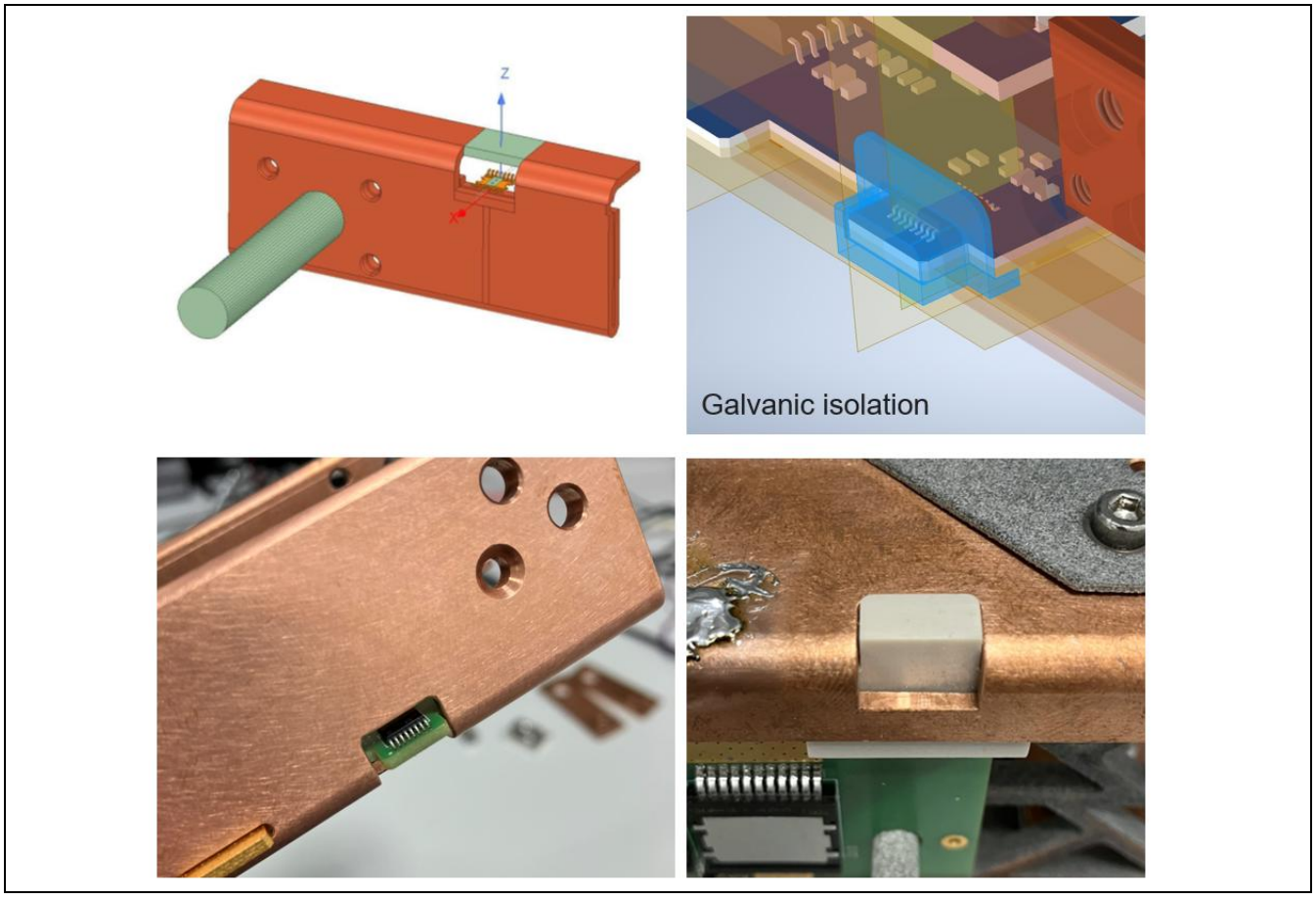


Figure 34 Coreless, magnetic, current-sensing structure

Design considerations for a dedicated power stage

Fast overcurrent detection

With the given sensing structure and the TLE5571 sensor's accuracy, the worst-case switch-off current for a nominal shutdown current of 900 A is approximately 1500 A, as shown in Figure 35.

The eBDU demonstrator REF-SSBD800VDCJCQJ1 is designed as a battery pack disconnect. Therefore, the minimum inductance estimated with a safety margin is ~7 µH for a short-circuit event. This ensures that the maximum di/dt during a short-circuit event is limited compared to other sockets where the switch needs to protect more paralleled battery packs.

The highest likelihood of short-circuit failures is when the charging is done outside the vehicle. In such cases, the wiring harness leading to the charging port must also be considered. For an eCAV system, this wiring harness, along with the short circuit and total battery inductance, is typically around 7 µH. The resulting maximum di/dt during a short-circuit event can be calculated as:

$$\frac{di}{dt_{max}} = \frac{V_{bat,max}}{L_{short,min}} = \frac{850\ V}{\sim 7\ \mu H} = \sim 120\ A/\mu s$$

Here a maximum short-circuit di/dt of 120 A/µs has been considered for the OCD overshoot with a commit time of 2 µs.

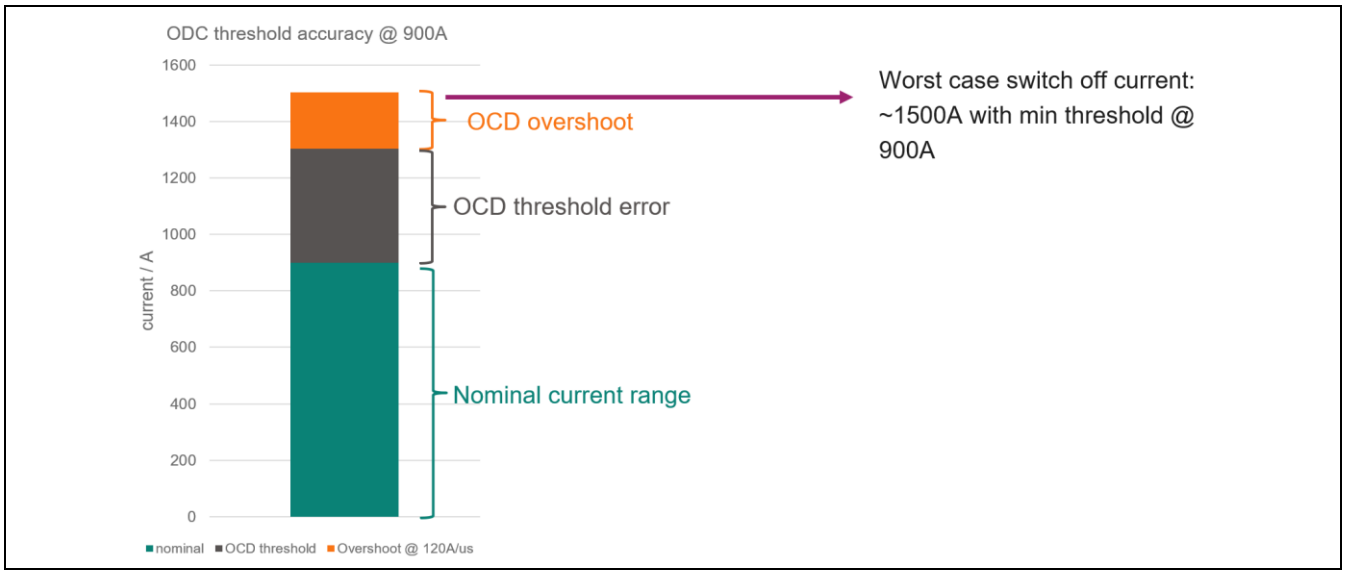


Figure 35 Worst-case switch-off current

6 Related resources

- Infineon CoolSiC™ JFET
- IJCQ120RM25J1
- eBDU Demonstrator REF-SSBD800VDCJCQJ1
- User guide UG2025-14: Solid-state battery disconnect unit demonstrator user guide
- Application note AN-2025-04: JFET Application note

References

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[2] CharIN Megawatt Charging System (Whitepaper), Berlin, CharIN e.V., 2022, https://www.charinev.org

[3] Application Note AN_2101_PL52_2103_112902: Innovative top-side cooled package solution for high-voltage applications, Infineon Technologies AG, 2024; [Link]

[4] Datasheet IJCQ120RM25J1: CoolSiC™ 1200 V SiC JFET: Q-DPAK top-side cooling; Infineon Technologies AG, 2025

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[6] Application Note AN-2025-06: CoolSiC™ JFET - Cascode Evaluation Board for Solid-State Circuit Breaker Applications, Infineon Technologies AG, 2025

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[8] User Guide UG-2025-14: Solid-state battery disconnect unit demonstrator user guide, Infineon Technologies AG, 2025

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Glossary

CAN
Controller area network

CCS
Combined charging standard

CRC
Cyclic redundancy check

DBC
Direct bonded copper

DBC
Direct bonded copper

DUT
Device under test

eBDU
electronic battery disconnect unit

eCAV
electric commercial, construction, and agricultural vehicle

ECU
Electronic control unit

EOF
End of frame

GUI
Graphic user interface

HV
High voltage

IC
Integrated circuit

IEC
International Electrotechnical Commission

IR
Infrared

JFET
Junction field effect transistor

LDO
Low dropout regulator

LV
Low voltage

Glossary

MCS
Megawatt charging standard

MCU
Microcontroller unit

MOSFET
Metal oxide field effect transistor

MOV
Metal oxide varistor

NTC
Negative temperature coefficient

OCD
Overcurrent detection

OVL
Overload protection

OVP
Overvoltage protection

OVT
Overtemperature protection

PC
Personal computer

PCB
Printed circuit board

PDU
Power distribution unit

RX
Receive

SIDAC
Silicon diode for alternating current

SOF
Start of frame

SSR
Solid-state relay

SWD
Single wire debug

TIM
Thermal interface material

TJ
Junction temperature

TMR
Tunnel Magnetoresistance

TSC
Top-side cooling

TVS
Transient voltage suppressor

TX
Transmit

USB
Universal serial bus

UVP
Undervoltage protection

Revision history

Document revision	Date	Description of changes
1.0	2025.10.21	Initial version

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