International
IOR Rectifier

APPLICATION NOTE

Application Note AN-985

Six-Output 600V MGDs Simplify 3-Phase Motor Drives

Table of Contents

	Page
Gate Drive Requirements	2
IR213x Block Diagram	2
Input Control Logic	3
Protection Circuits and Fault Reporting	4
Output Drivers	6
Application Guidelines	7
Layout Guidelines	8
Specific Applications	8
Appendix 1 Component Switches	10

Traditionally the functions described above have required discrete circuits of some complexity but International Rectifier's IR213X series six-channel gate drivers perform all the requirements for interfacing logic level control circuits to high power MOS-gated devices in high-side/ low-side switch configurations using up to six devices.

International
IOR Rectifier

APPLICATION NOTE AN-985

International Rectifier • 233 Kansas Street, El Segundo, CA 90245 USA

Six-Output 600V MGDs Simplify 3-Phase Motor Drives

1. Gate Drive Requirements

MOS-gated transistors commonly used in motor drives, UPS and converters operating at dc bus voltages up to 600VDC require voltage drive in order to achieve a saturated "ON" state condition. The drive signal must have the following characteristics:

1) An amplitude of 10V to 15V.
2) A low source resistance for rapid charge and discharge of the gate capacitance.
3) A floating output so that high side switches can be driven.

In addition to the above requirements the actual driver should be capable of driving combinations of devices in both low-side and high-side switch configurations. With this in mind the driver should also provide the following:

1) Low internal power loss at high switching frequency and maximum offset voltage.
2) Accept ground referenced logic level input signals.
3) Protect the power switch from damage by clamping the gate signal to the low state in the event of gate undervoltage or overvoltage or if the load current exceeds a predetermined peak value.
4) Protect the power switch by clamping the signal to the low state if the signal inputs are disconnected.

Traditionally the functions described above have required discrete circuits of some complexity but International Rectifier's IR213X series six-channel gate drivers perform all the requirements for interfacing logic level control circuits to high power MOS-gated devices in high-side/ low-side switch configurations using up to six devices.

2. IR213x Block Diagram

As shown in Figure 1 the I.C. consists of six output drivers which receive their inputs from the three input signal generator blocks each providing two outputs. The three low-side output drivers are driven directly from the signal generators L1, L2 and L3 but the high-side drive signals H1, H2 and H3 must be level shifted before being applied to the high-side output drivers.

An undervoltage detector circuit monitoring the VCC level provides an input to inhibit the six outputs of the signal generator circuits. In addition, there are individual undervoltage lockout circuits for the high-side outputs should any of the floating bias supplies fall below a predetermined level.

The ITRIP signal which can be derived from a current sensor in the main power circuit of the equipment (current transformer, viewing resistor, etc.) is compared with a 0.5volt reference and is then "OR-ed" with the UV signal to inhibit the six signal generator outputs.

HEXFET® is the registered trademark for International Rectifier Power MOSFETs

A fault logic circuit set by the UV or ITRIP inputs provides an open drain TTL output for system indication or diagnostics. There is also an internal current amplifier in the IR2130 and IR2132 that provides an analog signal proportional to the voltage difference between V_{SS} and V_{S0}. Thus, a viewing resistor in the main power circuit can provide a positive voltage at V_{S0} and by suitable feedback resistors the current amplifier can be scaled to generate 0-5Vdc as a function of actual load current (see 2.2.4). The IR2131 does not have the internal current amplifier.

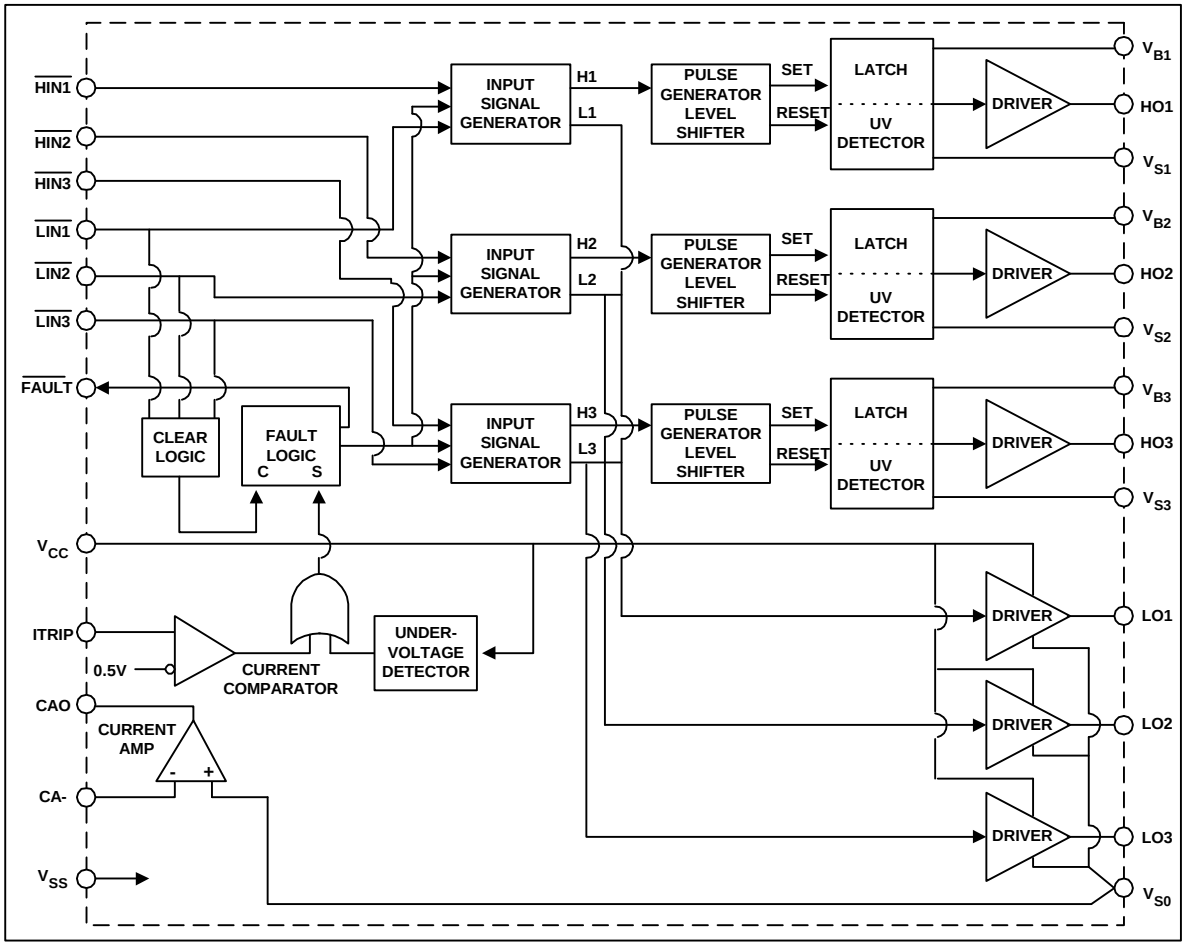


Figure 1. Functional block diagram of the IR2130/2132 drivers.

2.1. Input Control Logic

A logic low at any of the six inputs causes its corresponding output to go high, as shown in the truth tables (Tables 1 and 2).

Internal 50k pull-up resistors to V_{CC} ensure that all outputs are low if the inputs are open-circuited. Inputs are TTL and CMOS compatible with V_{IH} set at 2.2V and V_{IL} at 0.8V. A 500 nsec input filter prevents spurious triggering from fast noise pulses. The input logic circuitry also provides deadtime to avoid overlap when nearly coincident transitions take place at the LIN and HIN input pins in the same channel. This is illustrated in Figure 2.

A further protection against shoot-through currents in the power devices is provided by shutting down both high and low outputs if both are simultaneously commanded "ON" for the IR2130 and IR2132.

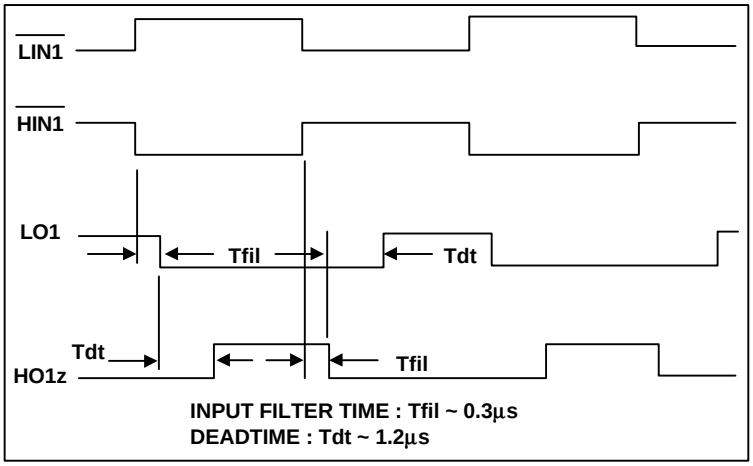


Figure 2. Input to output timing diagram for IR2130/2132 only

For some applications such as variable reluctance drives it is necessary to enable the high side and low side outputs simultaneously. The logic circuitry of the IR2131 allows this (see table 2) and permits any output condition determined only by the 6 input logic levels.

HIN	LIN	HO	LO
1	1	0	0
1	0	0	1
0	1	1	0
0	0	0	0

Table 1. IR2130, IR2132 Truth table for each input/output pair

HIN	LIN	HO	LO
1	1	0	0
1	0	0	1
0	1	1	0
0	0	1	1

Table 2. IR2131 Truth table for each input/output pair

2.2 Protection Circuits and Fault Reporting

2.2.1 UV Protection

An undervoltage condition on the V_{CC} level, defined as less than 8.9V (as V_{CC} is reduced) and less than 9.3V nominal (as V_{CC} is increased) causes all outputs to shutdown (see Section 2.2.3).

With V_{CC} at around 9 volts the drivers provide marginally adequate drive voltages to ensure full enhancement of the power switches for most applications. Separate UV lockout circuits are provided on the three high-side outputs. They also have a 0.4V hysteresis band with levels of 8.3 volts for a falling bias voltage and 8.7 volts for a rising voltage. Unlike the V_{CC} UV circuit they inhibit only their particular high-side output and do not affect the operation of any other output.

2.2.2 Current Trip

In the event of a shoot-through current or an output overload it is desirable to terminate all the output signals from the driver. This is accomplished through a current comparator circuit which monitors the voltage drop across a low side viewing resistor and compares it with a 0.5 volt reference level. The current comparator output is "OR-ed" with the V_{CC} UV circuit output (2.2.1) so that a fault condition of either type causes the fault logic circuit to actuate.

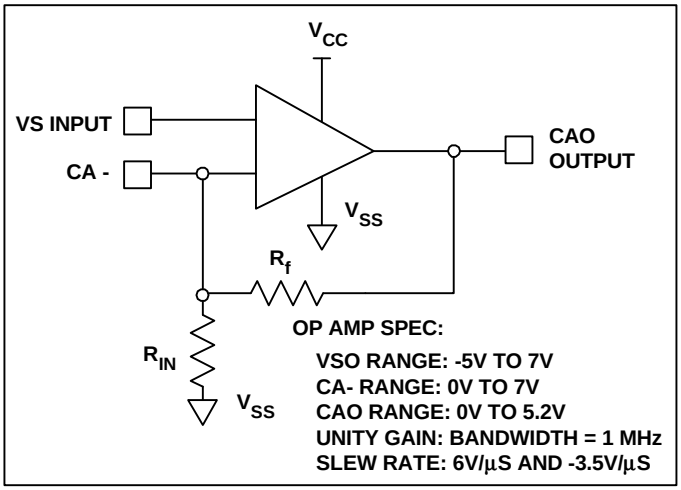


Figure 3. Current Amplifier Operation with Triangular Waveform Input

2.2.3 Fault Logic

This circuit consists of a latch which is set by the conditions described in 2.2.2 and is reset by holding all three low-side inputs high for more than 10 microseconds or by recycling the V_{CC} bias supply. When the fault latch is set it produces two output signals. One is used to inhibit all three input signal generator circuits thus inhibiting all six outputs. The other output signal appears as a fault indicator which goes low in the presence of a fault condition as defined in 2.2.2. The active low condition can drive an LED fault indicator or external logic circuit.

2.2.4 Current Sensing in IR2130, IR2132

Using the same current viewing resistor described in 2.2.2 the current sense voltage of 0-0.5V is amplified in the current amplifier to generate a 0-5V analog function for processing in an external control circuit.

In actual operation the voltage difference between the V_{S0} and V_{SS} pins forms the input voltage for the noninverting amplifier although only the positive current (V_{S0} positive WRT V_{SS}) is measured. Two resistors R_f and R_{IN} set the gain of the amplifier as shown in Figure 3.

Actual voltage gain is given by the relationship

$$A = \frac{R_f + R_{IN}}{R_{IN}}$$

for a gain of 10 with R_{IN} = 1k:

$$10 = \frac{R_f + 1K}{1K}$$

$R_f + 1K = 10K$

$R_f = 9K$

Power for the current amplifier is supplied from V_{CC}.

The shape of the current seen in the DC link will depend on the switching topology used for the three phase bridge. Two such topologies are the "Six Step Inverter" and the "Pulse Width Modulated Inverter". Suffice to say that for reasonable load levels at moderate to high power factors the DC link current will always be a positive value. Any negative current passed back through the free wheeling diodes in the bridge due to the lagging current will be absorbed in the bridge and not appear in the DC link.

At light or low power factor loads the negative current levels will begin to exceed the positive demands in the bridge and a net negative current will flow in the DC link. The same will occur if the load is caused to regenerate back into the system.

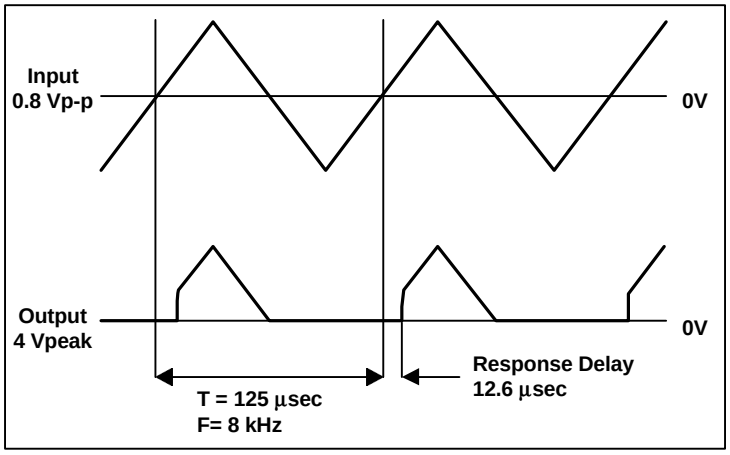


Figure 4. Current Amplifier Operation with Triangular Waveform Input

The output of the amplifier will not provide a negative voltage. This means that any negative current excursions in the DC link through the current sensing resistor will not appear at the output of the amplifier. This loss of information is further compounded by a characteristic of the amplifier that is not obvious from the data sheet. A recovery delay exists in the current sense amplifier operation as the input signal changes from a negative to a positive value.

The loss of negative input signals and the recovery delay of the amplifier is illustrated in Figure 4 where a triangular input was used as an example. The length of the delay is related to the dv/dt at the zero crossover of the input signal. As described earlier, negative inputs to the current sense amplifier are possible at light and low power factor loads. These negative excursions of current will be lost by the current amplifier.

The recovery delay of the amplifier is due to the V_{s0} input pin to the amplifier saturating when a negative voltage is applied. The charge accumulated requires time to be removed or dissipated before the amplifier will begin to function correctly. The only method to stop this recovery delay time is to inhibit the V_{s0} input voltage from going negative.

The input voltage will generally be of a small magnitude (less than 1 volt) since it is desirable to minimize the losses across the current sensing resistor and not introduce excessive voltages that will upset the drive circuitry. Such a small voltage signal is unsuitable for diode clipping.

Figure 5 shows one way of preventing the non-inverting input to the amplifier from going negative. If a differential amplifier is used with a voltage reference to shift the effective zero current reference input signal, the output will appear as an amplified version of the input signal, offset by some positive voltage.

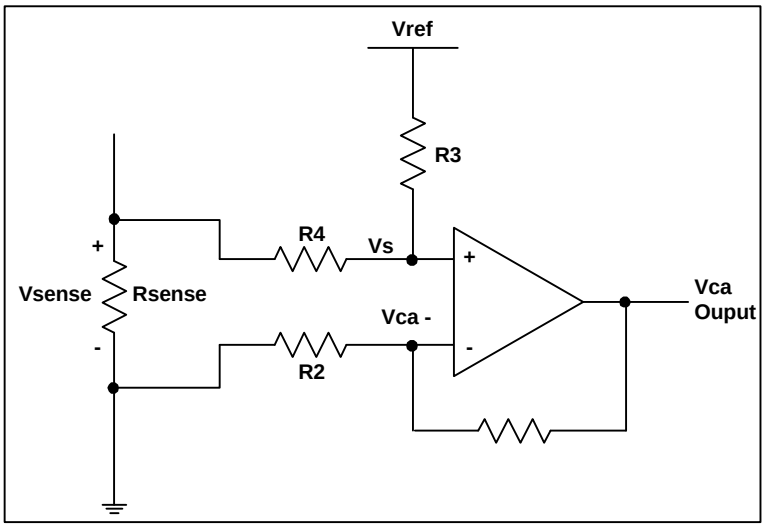


Figure 5. Different Amplifier with Voltage Offset

The relevant calculations for the selection of components for the given circuit are given in Appendix 1. It can be seen that the choice of components is limited by the total amount of resistance allowed in the gate loop, and the maximum current that can be sourced by the internal amplifier.

For those motor drives that do not use co-pak IGBTs, it is a relatively simple operation to prevent the negative component of dc link current from flowing into the current sensing resistor. The circuit in Figure 6 shows an implementation of this technique in a bridge that utilizes IGBTs. When MOSFETS are used as the switching devices an additional diode is required in series with each MOSFET to negate the internal body-drain diode.

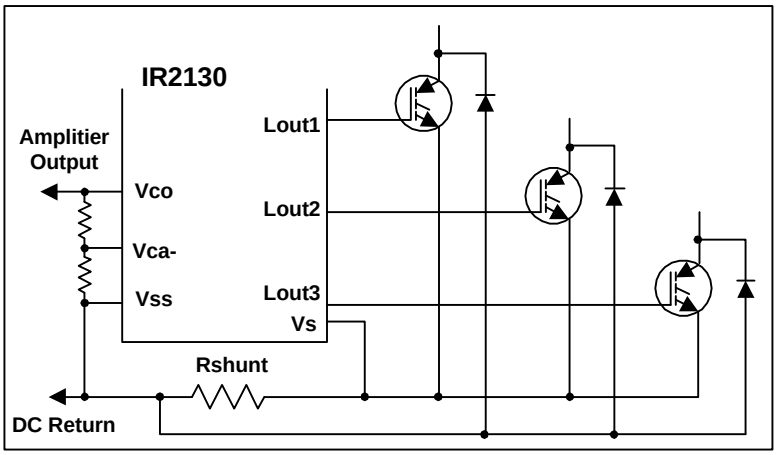


Figure 6. Measurement of Positive Current Components in the DC Link

Another possibility, suitable for lower power applications is shown in Figure 7.

Negative current components are blocked by the shunt resistor diode and forced through a second rated parallel diode. Schottky diodes are suitable for this application.

Note: The IR2131 does not have an analog current amplifier.

2.3 Output Drivers

The International Rectifier 213X family has six output drivers, three referenced to V_{S0} and three floating drivers capable of operating with offset voltages up to 600V positive to V_{S0}. All outputs have inverted logic, i.e., they go positive when the corresponding LIN or HIN goes low unless there is an over-riding fault condition (see 2.2.3). The output current is typically 0.25A on the positive edge and 0.5A on the negative edge of the output pulse, and when driving a typical MOS gate of 1000pF results in a maximum risetime of 100 nsec and falltime of 50 nsec.

Figure 2 shows the time relationship between input and output waveforms for the IR2130, IR2132. The input filter delay is typically 300 nsec and the deadtimes are 1.5 msec minimum and 2.0 msec maximum for the IR2130 and 700 ns for the IR2131.

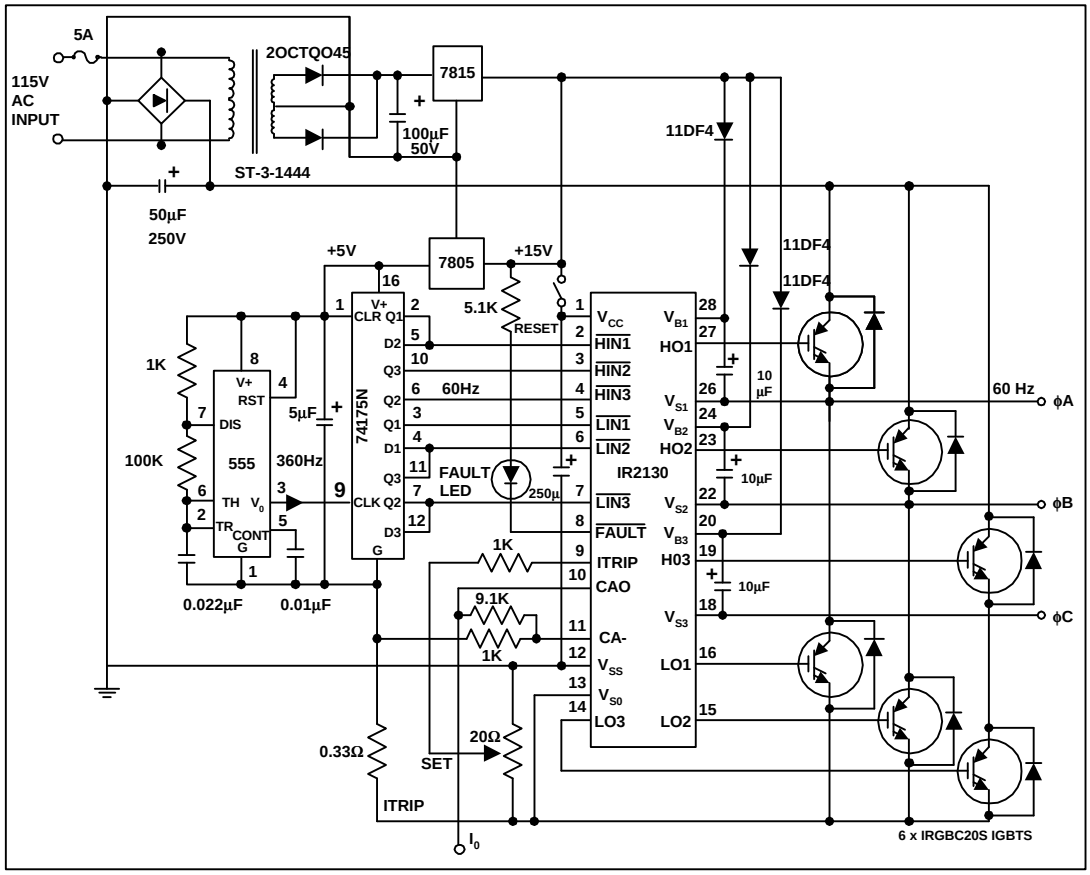


Figure 7. Three-phase six-step motor drive and 6 x HFA04TB60® HEXFRED diodes

2.3.1 Low Side Output Drivers

Because of the current amplifier requirements and to increase noise immunity between the power ground and the ground reference of the logic circuits, the V_{S0} to V_{SS} offset voltage capability is bi-directional at ±5V.

2.3.2 High-Side Output Drivers

When driving inductive loads the V_{S1}, V_{S2} and V_{S3} terminals are driven negative with respect to V_{S0} as inductive energy is commutated by the diodes across each low side power switch. For this reason the total offset capability is specified as -5V to +600V. The -5V spec is needed to accommodate instantaneous diode drops due to forward recovery as well as inductive effects of high current wiring, etc.

As previously mentioned in Section 2.2.1, undervoltage lockout is provided for each high side driver to prevent marginal operation if the bootstrap capacitors become discharged. This problem occurs more frequently in six-step brushless dc drives at extremely low speed or stall conditions and could result in high dissipation operation of the upper power switches if the UV lockout circuits were absent.

During long pulses, with the bootstrap capacitors supplying all the energy for the floating drivers, the capacitors gradually discharge until at 8.3 volts nominal the UV detector shuts down the output and prevents the power switch from overdissipating.

If long pulses have to be delivered to the outputs the shutdown condition can be avoided by:

1) Using larger bootstrap capacitors.
2) Refreshing bootstrap charge by momentarily turning off and reapplying input command pulse.
3) Providing continuous bias from floating dc power supplies.

3.0 APPLICATION GUIDELINES

3.1 Bootstrap and Decoupling Capacitors

Three bootstrap capacitors are required to supply power for the floating outputs of the driver, the values of which are a function of the gate charge requirements of the power switch and the maximum power switch "ON" times.

The internal floating driver current also must be supplied from the bootstrap capacitors. After all these energy requirements have been met there must still be enough charge remaining on C_{BOOT} to avoid UV shutdown (8.3V nominal).

Example:

What is the maximum t_{ON} under the following conditions?

If V_{CC} = 15V and the charging of the bootstrap capacitor occurs when V_{S0} = -1.0V and V_F of the bootstrap diode is 1.0V we have a net voltage on C_{BOOT} of 15Vdc. Let us also assume that we are using a #5 size power switch such as an IRF450 or IRGPC50U either of which require a total gate charge of around 0.12 mC and that we want to maintain a C_{BOOT} of 0.1pF at a minimum voltage of 10Vdc:

during discharge $\Delta v = 5V$

$Q_{AVAIL} = CV = 0.1 \text{ X } 10^{-6} \text{ X } 5 \text{ Volts} = 0.5 \text{ mC}$

Q_{REQD} = 0.12 mC (See data sheet IRF450 or IRGPC50U)

Hence, having supplied the gate charge, the gate voltage is 13.8 V (0.38 mC). From the point on, a constant leakage current I_{QBS} = 15 µA discharges the bootstrap capacitor. The time it takes for the bootstrap capacitor to discharge to 10 V can be calculated as follow:

$\Delta t = C \text{ x } \Delta v / I = 0.1 \text{ µF x } 3.8 \text{ V } / 15 \text{ µA} = 25 \text{ ms.}$

The above calculation neglects the leakage current in the bootstrap diode, which must be a fast recovery type to avoid discharging C_{BOOT} as the diode starts to block voltage.

In practice, as indicated in INT-978 Section 5, it is not advisable to use a bootstrap capacitor smaller than 0.47 µF

In terms of decoupling requirements, a capacitor at least 10X the value of C_{BOOT} is required from V_{CC} to V_{SS} to provide adequate charging current for C_{BOOT} and also to minimize voltage transients on the V_{CC} supply resulting from these currents.

3.2 Power Dissipation

The drivers have a "fault" output on pin 8 which is really an open drain MOSFET with its source connected to V_{SS} (pin 12) . The intrinsic diode of this MOSFET has a negative temperature coefficient of V_f almost exactly equal to -0.002V/°C. Thus we have a "built-in" thermometer to monitor die temperature using a -1mA constant current supply to pin 8.

Actual die temperatures are dependent on frequency of operation, the offset voltage (HVDC bus voltage) and the capacitance of the MOS-gated power switches being driven. The value of the series gate resistors also determines overall switch loss but has little effect on the driver temperature. A detailed analysis of losses in MGDs can be found in INT-978 Section 4.

Curves of junction temperature using various 500-volt MOSFETs and gate resistors versus switching frequency are to be found in the individual date sheets for the IR213X series of MOS gate drivers.

4.0 LAYOUT GUIDELINES

The driver forms the interface between the low level logic circuitry and the high power switching devices. It follows then that signal grounds and high power returns should not be mixed together indiscriminately but should follow carefully formulated rules so that crosstalk problems can be avoided. Some detailed rules are contained in Sections 5 and 6 of INT-978.as follows:

1) The gate drive returns from the three low side devices should be run to the V_{S0} pin with separate and independent tracks to avaid crosstalk between the different legs of the inverter

2) Common mode currents arising from wiring layouts that allow load currents to flow in signal return circuits must be avoided.

3) Load current loop size must be small to minimize circuit inductance.

4) High current buses must be adequately decoupled at the switching point to minimize inductive spiking.

5) Adequate shielding between high voltage, high dv/dt points and low level signal circuits must be provided.

6) Transformer designs must minimize voltage gradients between adjacent windings and to the core to prevent capacitively coupled currents from flowing in sensitive signal circuits.

7) Power switch dv/dt values should be kept as low as possible consistent with overall system efficiency so that induced bus voltage spikes are minimized.

Contrary to generally accepted theory that faster switching is better, there are several conflicting requirements in the interface between the driver and the driven power device:

1) If the distance between driver and power stage is more than a couple of inches, the drive signal should be run in a twisted pair routed directly to the gate and source (or emitter) of the power device.

2) Drivers such as the IR2130 have low impedance outputs and consequently cause very fast switching of power MOSFETs. Severe ringing occurs at the switching transistors resulting in unwanted RFI generation and possible dv/dt failure of the power MOSFETs. A quarter-watt non-inductive series gate resistor of about 10 to 33 Ohms usually provides sufficient roll-off with C_{ISS} to damp out the ringing. With small HEXFETs (die sizes 1 to 3) the resistor value should be increased from about 30 to 50 Ohms.

3) In motor drive circuits where the load inductance is high, the motor current is commutated by diodes across the power switches when the switches are "OFF." As the opposite switch in a particular bridge leg is turned "ON" it must pull the conducting commutation diode out of conduction through its reverse recovery condition. A spike of current occurs at this time which causes ringing and RFI generation. The magnitude of the current spike can be reduced by the use of the series gate resistor described in (2) above.

5. SPECIFIC APPLICATIONS

5.1 Six-Step 3-Phase Motor Drive

Figure 4 shows a typical 3-phase non-regulated motor drive in which the IR2130 supplies all the gate drive signals for the high-side and low-side IGBTs. The IR2130 is operated from a 15-volt dc supply from a 3-terminal regulator and the inputs are derived from a six-step ring counter with its input signal supplied by a 555 astable multi-vibrator operating at 360 Hertz. The dc bus for the six-step inverter is supplied off-line by rectifying the 115-volt ac input and filtering it with a 50 microfarad 250-volt capacitor.

Motor current is sensed by a series viewing resistor in the negative bus with a 20-Ohm pot across the resistor so that a voltage proportional to load current is delivered to the ITRIP pin 9 of the IR2130. Also, a dc voltage proportional to motor current is available at pin 10. This uses a 9KΩ feedback resistor and a 1KΩ input resistor on pin 11, the inverting input to the current amplifier.

5.2 A 3-Phase Variable Reluctance Drive Using IR2131

Figure 6 shows a variable reluctance motor drive using IGBT's and the IR2131 MOS Gate Driver. High side and low side outputs are simultaneously provided to drive each set of motor phase coils.

The inputs can be simple logic levels spaced 120 electrical degrees apart or can be pulse width modulated to control motor torque.

The values of the bootstrap capacitors are selected to prevent undervoltage lockout at the minimum frequency of operation.

Typically when the minimum frequency is around 30Hz, 10mF electrolytic capacitors are used. They must be selected for low ESR/ESL particularly when large power switches are used as the peak demand currents can be fairly high.

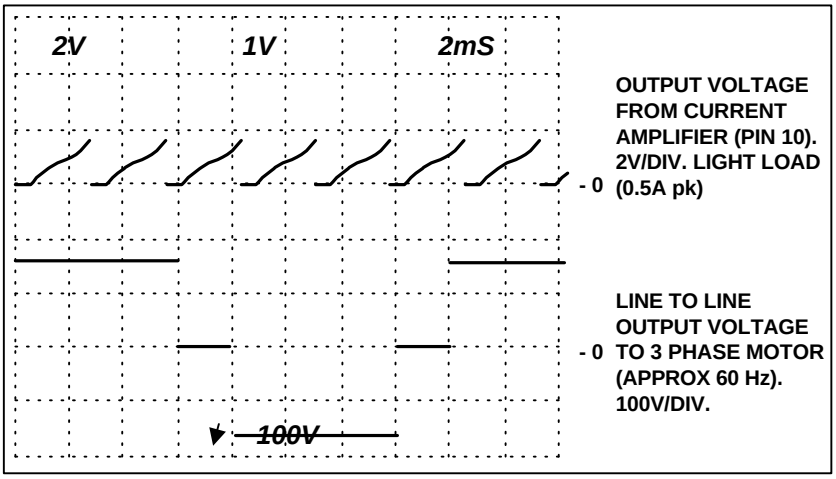


Figure 8. Six-step motor drive waveforms

When starting with the bootstrap capacitors discharged, the first input commands are used to charge them and subsequent commands provide rotational power for the motor. To avoid this problem, the bootstrap capacitors can be pre-charged by connecting high value resistors across the 3 low side power switches. With the bootstrap pre-charged, all input logic signals provide rotational inputs to the motor.

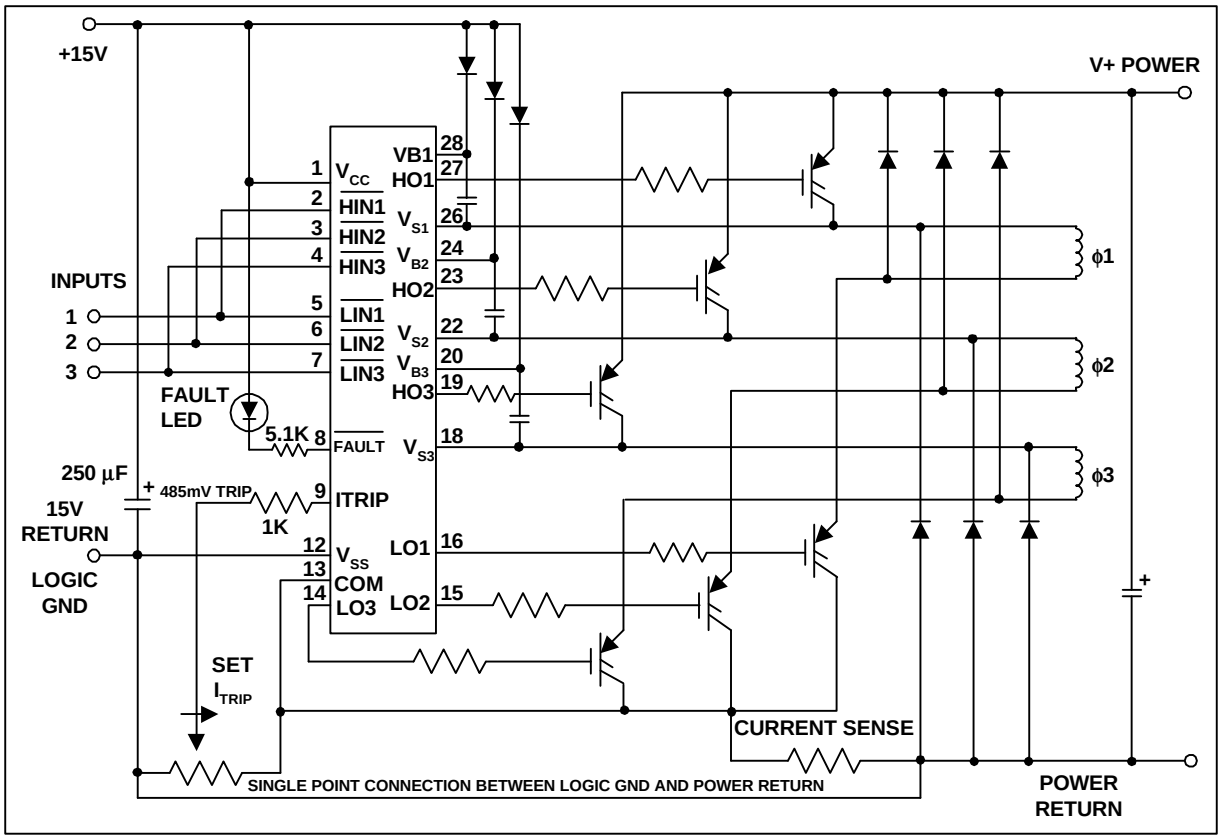


Figure 9. Three-phase variable reluctance motor drive

5.3 General Considerations Using MOS Gate Drivers

Although the IR213X family of drivers can considerably simplify 3-phase motor drives there are some pitfalls to be avoided.

1) The V_{S1}, V_{S2} and V_{S3} pins have a maximum specified rating of only -5Vdc. In high current drives it is quite common for inductive spike voltages to exceed -5V because of stray inductances, diode forward recovery problems etc. We recommend techniques as described in AN-978 Sec. 6 to address this problem.

2) High current motor drives can also generate ground bus currents which are sometimes severe enough to disrupt logic circuits and cause mis-commutation of the power switches. This usually results in catastrophic failure of the entire drive. To combat this we recommend the use of high speed optical couplers as shown in Figure 7. Using this technique, the power return and logic grounds are completely isolated from one another (see Figure 7).

Appendix 1 Component Selection

When selecting components to use with the internal current amplifier the following design guidelines should be followed.

1) The maximum value of resistor that can be inserted in the gate return path is 47 Ohms. Larger values than this may affect the switching performance of the device.

2) The maximum output current of the amplifier is 2mA under worst case conditions.

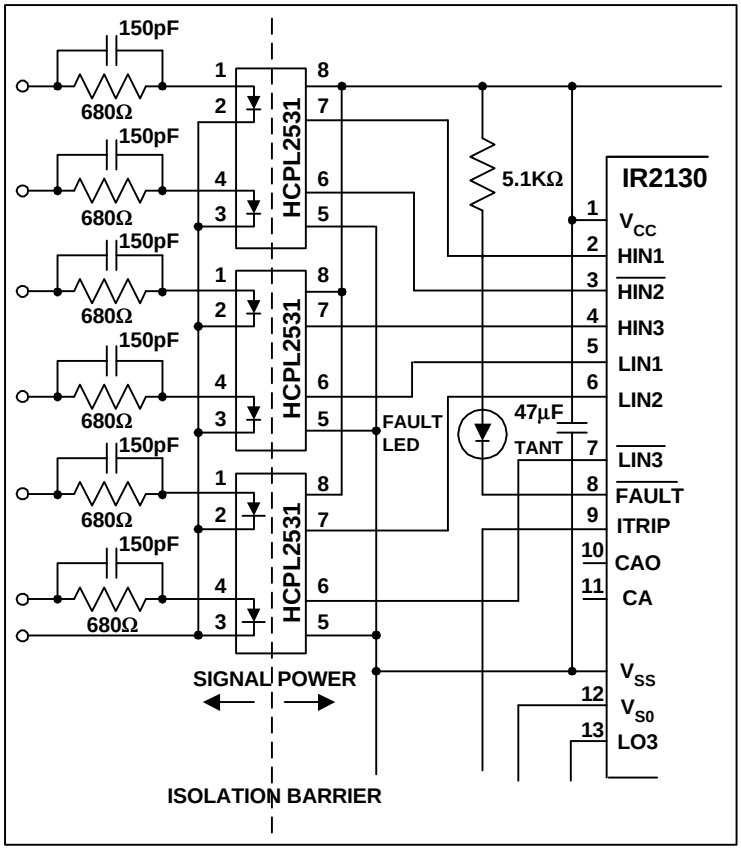


Figure 10. Recommended opto-isolated input circuit to the IR2130

Consider the circuit configuration shown in Figure 2. The gain of the non-inverting amplifier stage is:

$$V_{cao} / V_{s0} = 1 + R1/R2 \qquad (1)$$

The signal at the V_{S0} pin may be defined by the equation:

$$V_{s0} = V_{sense} + (V_{ref} - V_{sense}) * R4 / (R3 + R4) \qquad (2)$$

Combining equations (1) and (2) gives:

$$V_{cao} = V_{sense} (l + R1/R2) + [(V_{ref} - V_{sense}) * R4 / (R3 + R4)] * (1 + R1/R2)$$

If the conditions R1 = R3 and R2 = R4 are true, then the last equation collapses to:

$$V_{out} = V_{ref} + V_{sense} * R1/R2$$

Using the design guidelines sets the range of resistor values that may be chosen. The 2mA current limit sets a minimum for the resistance sum R1 + R2. -This limit is defined by:

$I_{limit} = V_{cao(max)} / (Rl + R2)$; I_{limit} = 2mA, $V_{cao(max)}$ = 5V.

This means that R1 + R2 > 2.5 kOhm. R2 is limited to 47 Ohms and R1 > 2.45 kOhm. This gives a gain in the circuit of R1/R2 = 52. If the output of the amplifier is in the range [0;+5V], then the offset could be 2.5V, giving an allowable output voltage variation of +/-2.5V. The maximum variation of the input voltage is thus +/-50mV.

This small signal level is possible with commercially available shunts that are low inductance to reduce noise from power device switching. It does mean however that the internal current trip function of the IR2130 cannot be used, as it has an internal 0.5V trip point. Care should be taken when using small input signal levels as the data sheet specification for the amplifier offset voltage is 10mV. An offset adjustment may need to be included in the circuit.

FIGURE CAPTIONS FOR INT-985

Figure No.	Title
1	Functional block diagram of the IR2130/2132 drivers
2	Input to output timing diagram for IR2130/2132 only
3	Current feedback amplifier connection
4	Current Amplifier Operation with Triangular Waveform Input
5	Differential Amplifier with Voltage Offset
6	Measurement of Positie Current Components in the DC Link
7	Three-phase six-step motor drive and 6 x HFA04TB60 HEXFRED diodes
8	Six-step motor drive waveforms
9	Three-phase variable reluctance motor drive
10	Recommended opto-isolated input circuit to the IR2130