Short-circuit robustness of CoolGaN™ and OptiMOS™ 6 100 V transistors

About this document

Scope and purpose

The document shows the behavior of low-voltage CoolGaN™ and OptiMOS™ transistors under various short-circuit tests, the methodologies used, and the hardware used to conduct the tests.

Intended audience

The document is intended for electronic engineers and technicians who design with these transistors and want to understand the reaction time of the protection in short-circuit conditions, as well as the behavior of the device in such scenarios.

Key points

The short circuit reported in the documents emulates the following conditions:

- Output short circuit (also referred to as load short circuit)
- DC or half-bridge short circuit, also known as SCWT (Short Circuit Withstand Time)

About this product family

Product family

The tests use 100 V CoolGaN™ (IGD015S10S1 [4]) in an RQFN package and 100 V OptiMOS™ 6 (ISC022N10NM6 [5]) in a SuperSO8 package mounted on a general-purpose evaluation board with TDI EiceDRIVER™ 1EDN7116G [6] (EVAL_7116G_100V_SSO8 [7]).

Target applications

The main applications are those that implement the transistors in a half-bridge configuration, such as inverters and low-voltage power supplies.

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1 Introduction

The tests reported in this application note compare similar MOSFETs and GaN HEMTs in terms of package, typical $R_{DS(on)}$, and voltage rating. The two types of short-circuit conditions are the most sensitive in different applications (e.g., motor drive and DC-DC converter), where the protection needs to react within a certain amount of time to avoid destruction of the devices and maintain a safe operating area for the final system.

MOSFET and GaN HEMT technologies have intrinsically different structures, which correspond to different parameters reported in the datasheet (SOA, output characteristics, and transfer characteristics). In this regard, the comparison aims to highlight the different behaviors in a limited situation, even outside the declared SOA of the two transistors, as reported in similar tests in [2].

The short-circuit tests are divided into two parts. The first one is the output short circuit, which can emulate the condition of a short between two half-bridges through a small inductance or wire [1]. The second one is called half-bridge short circuit with stand time, where the device under test (DUT) needs to handle a critical condition where the current is limited only by a small resistor.

Both tests characterize the behavior of the device under an ambient temperature of 25°C and for how long the condition can be maintained before destruction of the devices. The tests are handled with CoolGaN™ IGD015S10S1 (GaN HEMT) [4] and CoolMOS™ ISC022N10NM6 MOSFET [5], both mounted on the evaluation board EVAL_7116G_100V_SSO8 [7], which implements an optimal layout to minimize parasitics, as reported in [3].

2 Measurements setup

2.1 Environmental laboratory conditions

The laboratory during the tests reports an ambient temperature of 25°C and humidity below 35%. Each component was managed against any possible ESD issue.

2.2 Instruments

The following instruments (including the board) were used to simulate the short-circuit event:

- Function generator: Tektronix AFG3102C (1 GS/s, 100 MHz)
- Oscilloscope: Tektronix MSO58 (6.5 GS/s, 1 GHz)
- Evaluation board: EVAL_7116G_100V_SSO8 [7]
- Power supply: EA-PSI 9200-210 (200 V, 210 A, 15 kW)
- Isolated probe (IsoVu): Tektronix TIVP1 (1 GHz, diff. voltage ±2500 V, common mode 60 kV)
- Rogowski coil: CWT ultra mini CWTUM/3/B (600 A, 10 mV/A, 30 MHz)
- Additional electrolytic capacitor off-board to decouple the power supply: 10 mF ±10%

The setup of the measurements is reported in Figure 1.

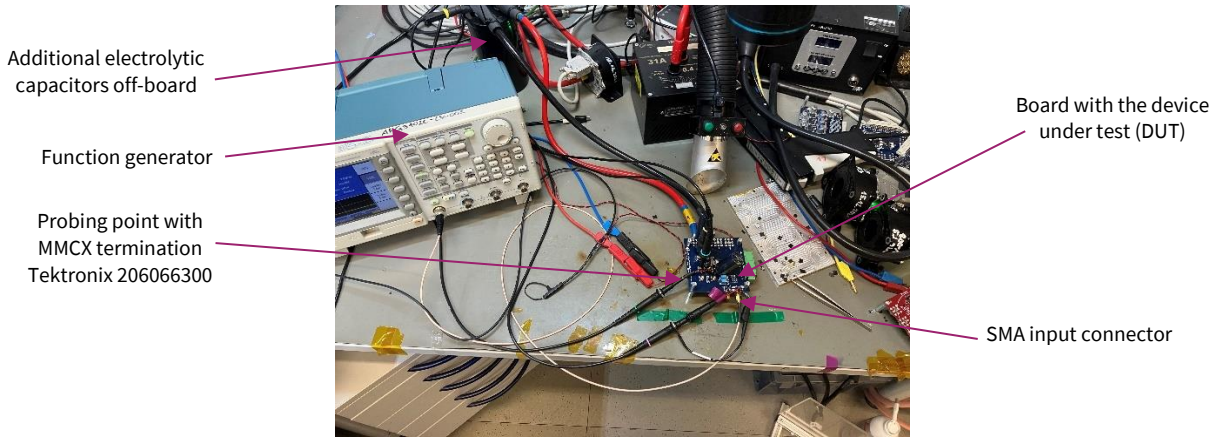

Figure 1 Setup of the measurements

Note: Figure 1 does not show all instruments due to the bench configuration.

2.3 Hardware configuration

The used evaluation board [7] necessitates some modifications to manage the tests for both transistors. The following tables (Table 1 and Table 2) summarize the main changes in the original board and the used components to perform the measurements, as well as the driving voltage of the gate and loads used.

Measurements setup

Table 1 Hardware change on the output short circuit test

Output short circuit - IGD015S10S1			
Rg (R_{g1}, R_{g2})	Rg off (R_{bst1}, R_{bst2})	Gate driving voltage	Inductive load (L1 - Figure 4)
2 Ω	Not mounted	5 V with 1EDN7116G (charge pump disabled)	35 nH at 1 kHz with ESR of 2 mΩ in air core (Figure 5)
Output short circuit - ISC022N10NM6			
Rg (R_{g1}, R_{g2})	Rg off (R_{bst1}, R_{bst2})	Gate driving voltage	Inductive load (L1 - Figure 4)
2 Ω	Not mounted	10 V with 1EDN7116G (charge pump disabled)	35 nH at 1 kHz with ESR of 2 mΩ in air core (Figure 5)

Table 2 Hardware change on the half-bridge short circuit withstand time

Output short circuit - IGD015S10S1			
Rg (R_{g1}, R_{g2})	Rg off (R_{bst1}, R_{bst2})	Gate driving voltage	Resistive load (R_{shunt} - Figure 13)
10 Ω	Not mounted	5 V with 1EDN7116G (charge pump disabled)	20 mΩ (x2 TLRH3APTTE10L0F)
Output short circuit - ISC022N10NM6			
Rg (R_{g1}, R_{g2})	Rg off (R_{bst1}, R_{bst2})	Gate driving voltage	Resistive load (R_{shunt} - Figure 13)
10 Ω	Not mounted	10 V with 1EDN7116G (charge pump disabled)	10 mΩ (x1 TLRH3APTTE10L0F)

To withstand the high request of current in a short amount of time, the board requires additional capacitance with low ESR and ESL, as shown in Figure 2, across the input voltage (V_{in}). The added capacitance with respect to the original hardware [7] is around 3 mF with the electrolytic capacitance (EEU-FC2A681).

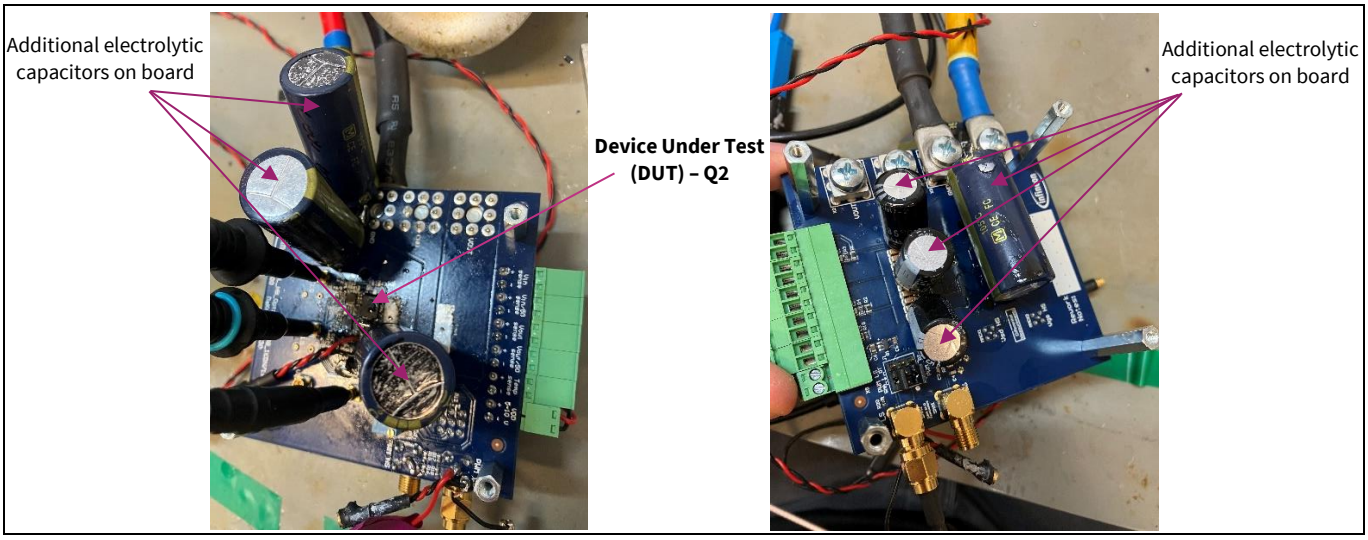

Figure 2 Added electrolytic capacitor in the evaluation board for short-circuit tests

3 Output short circuit

The output short circuit, also called load short circuit, can be associated with a short circuit between two phases of an inverter or a full bridge configuration, where the two phases are associated with a high-side short circuit between V_{in} and the SW node, as reported in Figure 3.

In the setup taken into consideration, the device Q3 is considered as a short circuit, which implements a more demanding test that does not limit the current in the high side. Q1 is always used as an off-device for a freewheeling path.

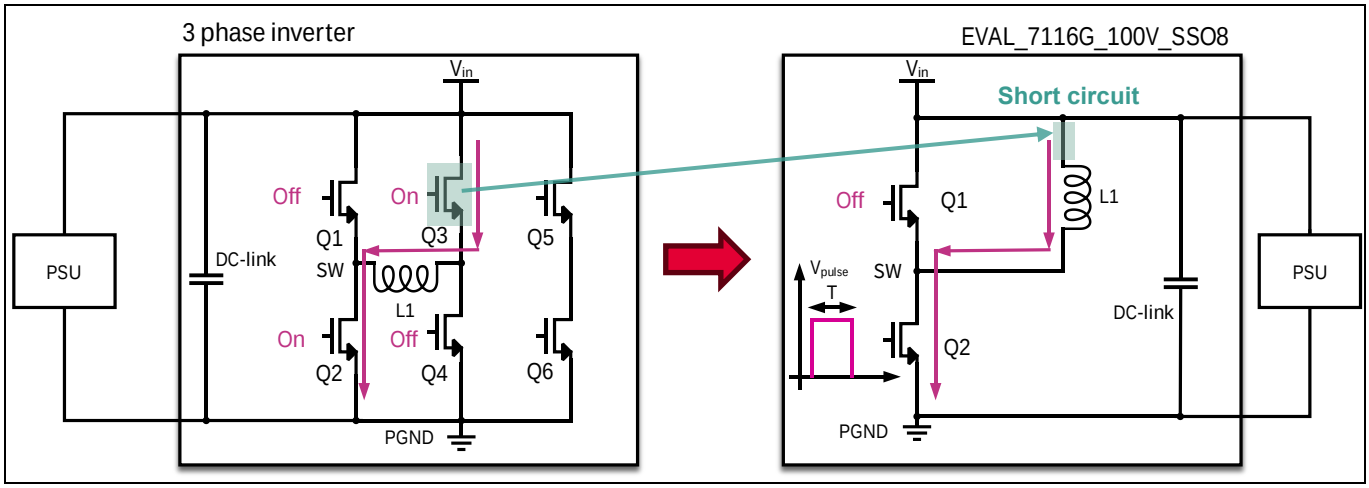

Figure 3 Phase-to-phase short circuit and test implementation on the evaluation board [7]

3.1 Schematic block and setup

The values of the setup in Figure 4 are reported in Table 1.

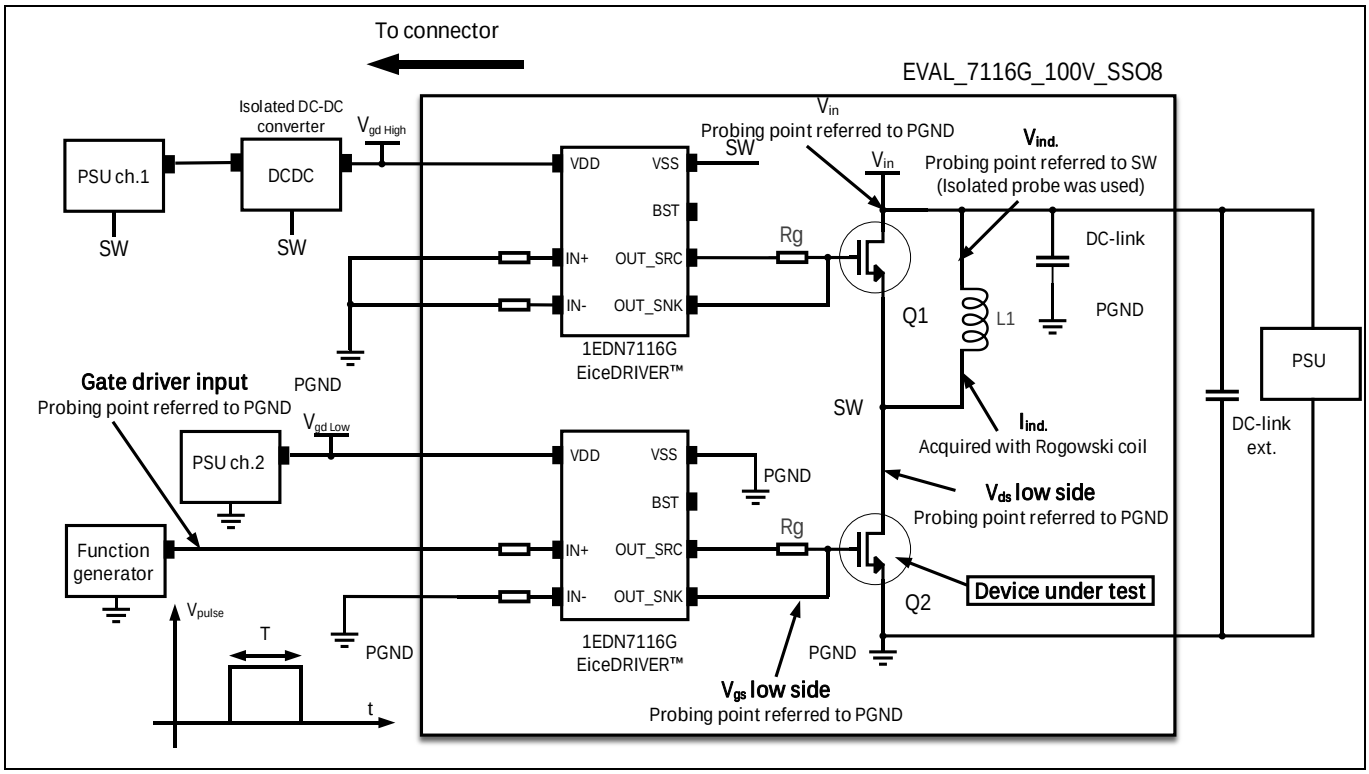

Figure 4 Schematic block of the output short circuit

Output short circuit

The test is performed with a handmade inductor (L1 in Figure 4 and Figure 5) based on an air-core structure, which will maintain the linearity and avoid saturation even at high current. To reduce the resistance, the coil was built with multiple wires wrapped together, using three wires.

The setup of the measurements, in Figure 5, shows the different probing points and the acquisition of the current through a Rogowski coil. Due to the low limit, it is necessary to capture only one of the wires of the coil, and consequently, the value is multiplied by 3 in the scope to obtain the correct amount of current.

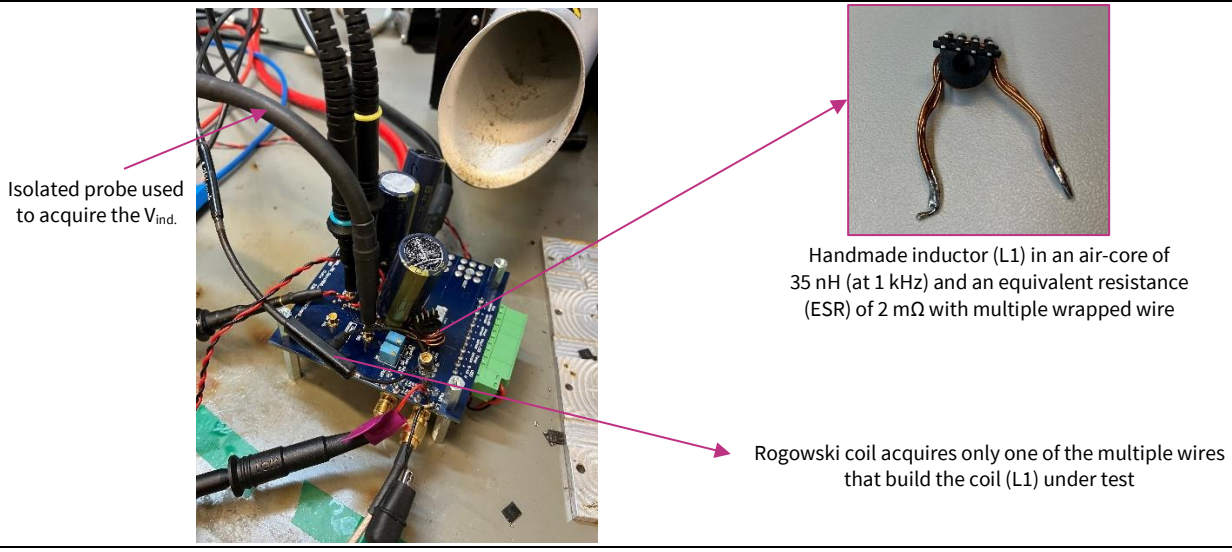

Figure 5 Setup of the output short-circuit

The inductor (L1) value is chosen to have a max. current >>2000 A so that it will let the device under test enter the linear region (reported in Figure 10) and emulate the phase-to-phase short in a one-time event. Equation 1 and Equation 2 report the limit of current and the time constants of the value reported in Table 1 for what concerns the inductive load in an ideal setup (no parasitics).

$$I_{max} = \frac{V_{in}}{ESR} = \frac{48\ V}{2\ m\Omega} \approx 24\ kA \qquad I_{1^{st}\tau} = 0.63 \cdot I_{max} \approx 15\ kA$$

Equation 1 Maximum current achievable with the inductive load in an ideal setup in Figure 4

$$\tau = \frac{L}{ESR} = \frac{35\ nH}{2\ m\Omega} \approx 17.5\ \mu s$$

Equation 2 Time constant of the inductance in an ideal condition load with an ideal setup in Figure 4

Attention: Important notice of the chosen inductive load and real setup

The previous equations represent the ideal behavior of the circuit without taking into account the resistance (R_{on}) of the two transistors, [4] and [5], that are dependent on temperature. Moreover, the voltage drop during the transition is not considered due to the difficulty in modeling the stray inductance between all the capacitance added in the setup shown in Figure 2.

3.2 Test of 100 V OptiMOS™ 6

Figure 6 shows the waveforms of current and voltage during the switching event. The device is damaged after turning off due to the high temperature that reaches more than 400°C. At this temperature, the MOSFET transistor is in an intrinsic condition that continues to sink current even in the off state [9], and therefore causes a high dissipation and consequently a high thermal stress till its destruction. The temperature of the device is reported in detail in Section 3.4 with SPICE simulation.

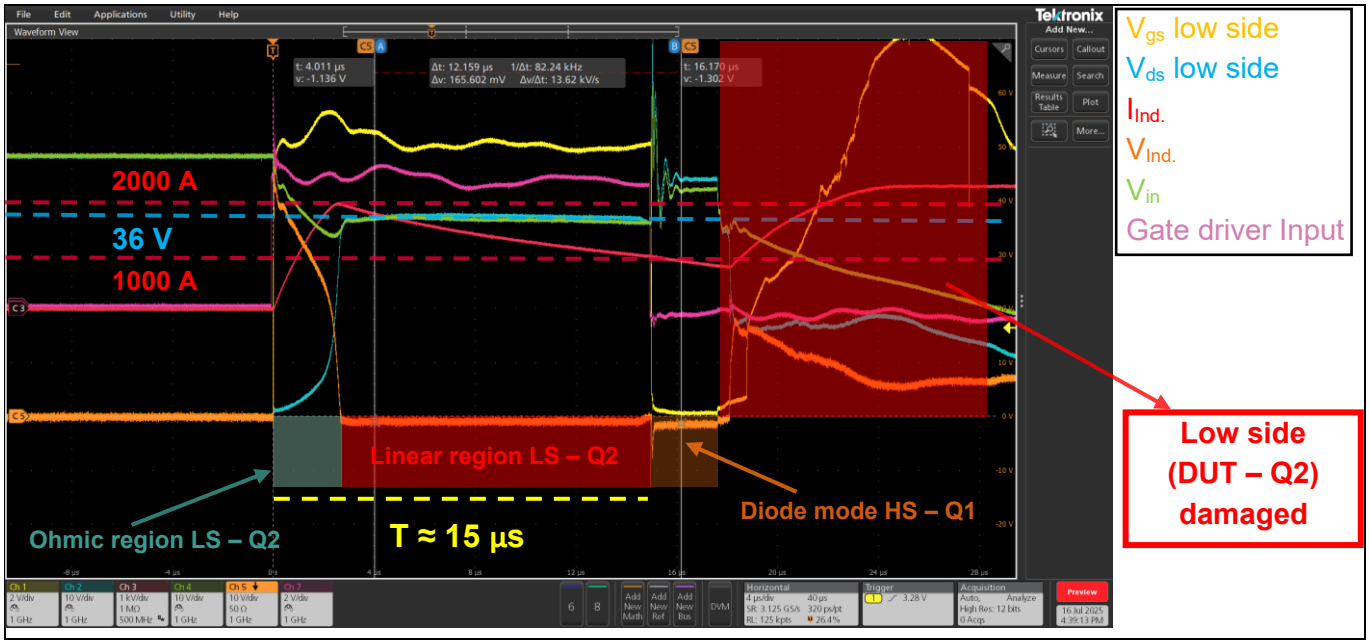

Figure 6 Measurements of the output short circuit with OptiMOS™ 6 – screen 1

Figure 7 reports the first few microseconds of the transition, where the MOSFET passes from the ohmic region to the linear region and remains there for the entire duration of the pulse, which is more than 10 µs as reported in Figure 6.

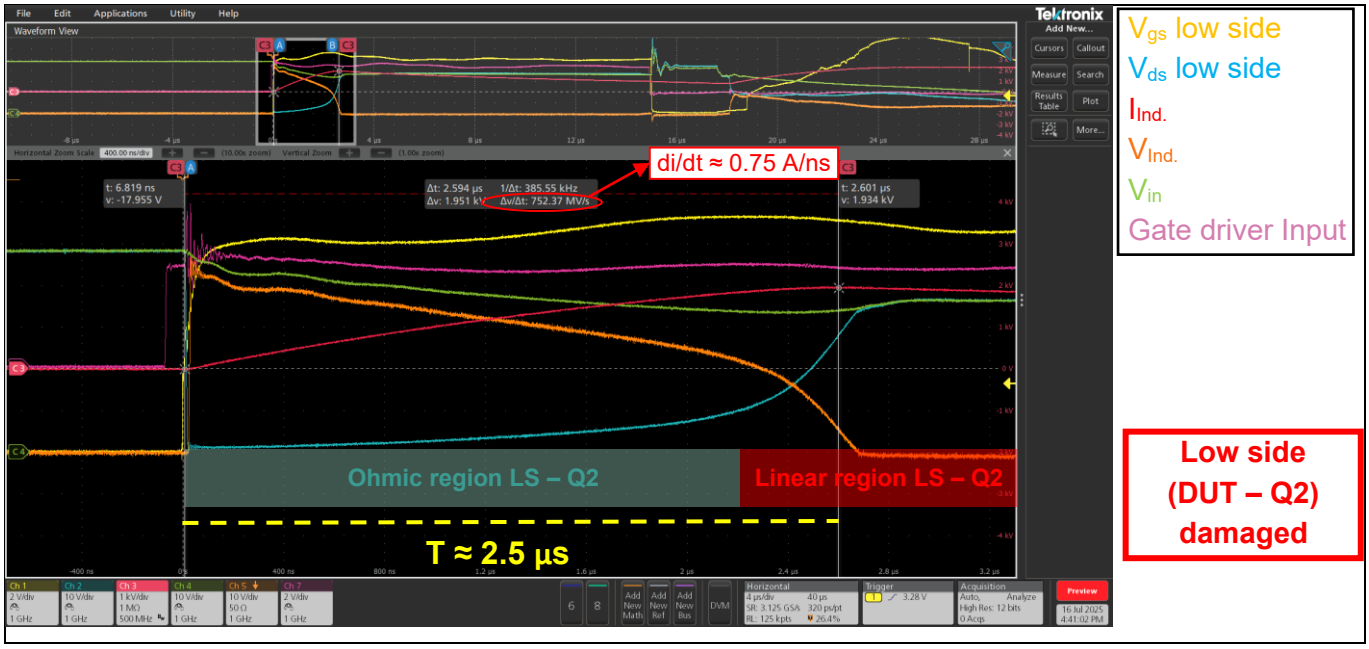

Figure 7 Measurements of the output short circuit with OptiMOS™ 6 – screen 2

3.3 Test of 100 V CoolGaN™

The transition of the GaN HEMT in the configuration reported in Figure 4 differs based on the fact that the transistor Q1 is letting the current flow in the body diode as detailed in [8] and as seen in Figure 8, and a higher time is maintained without the destruction of the device. Q2 enters the linear region after 1.7 µs as seen in Figure 9. The high voltage drop of the Q2 transistor will let the current recirculate in Q1 and avoid the destruction of the GaN HEMT. This condition maintains for a time period greater the that of the on-state without destruction with respect to the MOSFET, as shown in Figure 6. Due to this event the GaN HEMT enters the linear region with a lower current of 200 A as seen in Figure 8, and it will survive for a time period 3 times higher than that of the MOSFET described in Section 3.2.

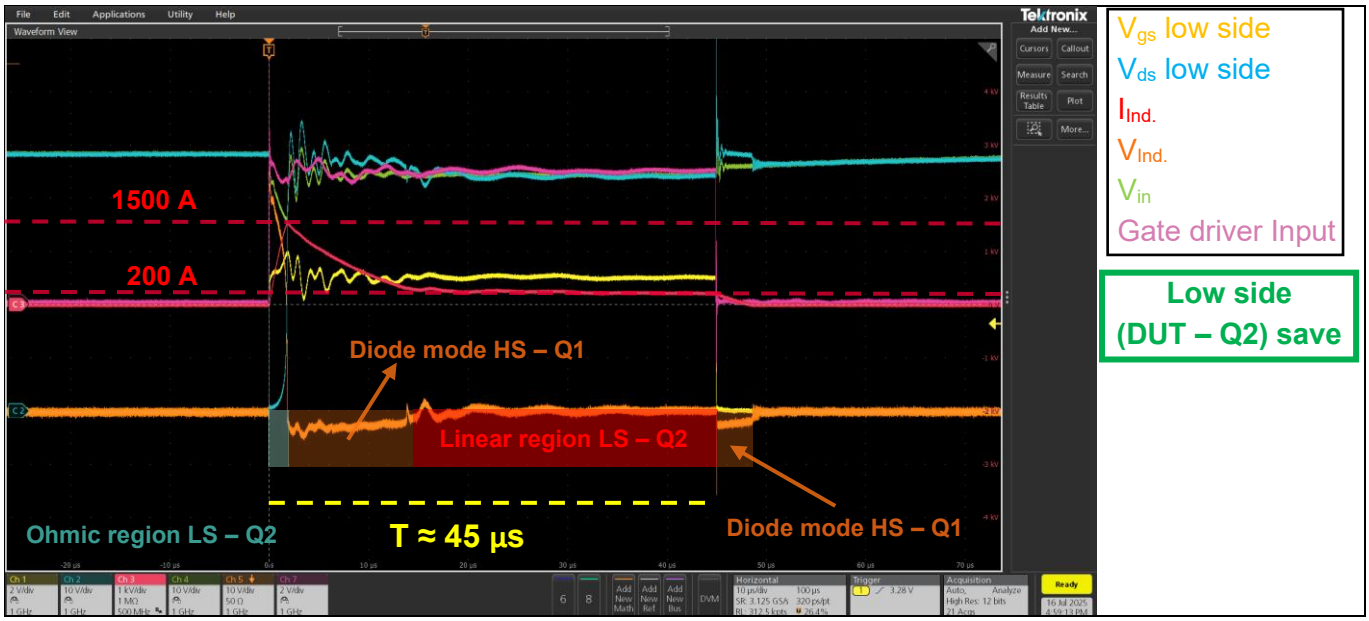

Figure 8 Measurements of the output short circuit with 100 V CoolGaN™ – screen 1

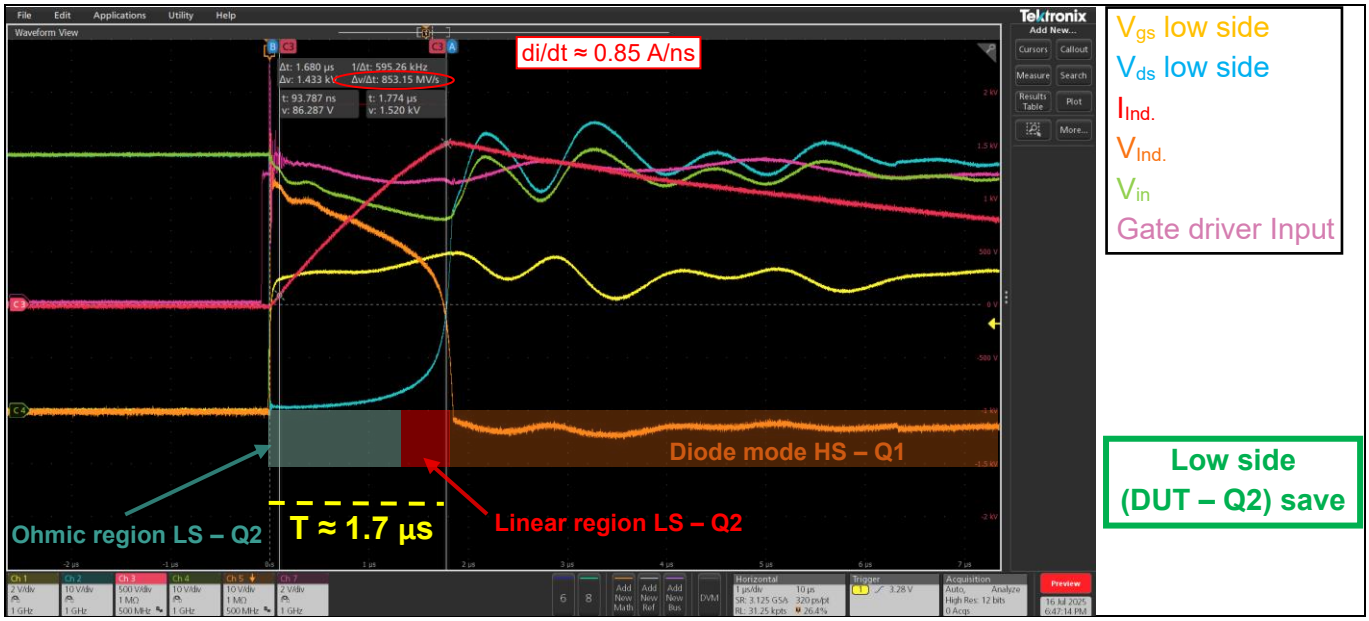

Figure 9 Measurements of the output short circuit with 100 V CoolGaN™ – screen 2

3.4 Comparison of the results

The results shown in Section 3.2 and Section 3.3 of the two transistors during an output short circuit report the entering of the devices in the linear region in both cases with the increase of I_d. This behavior is described in the output characteristics seen in Figure 10, where a fixed gate voltage (V_{gs}) of 5 V is applied for the GaN HEMT and 10 V for the silicon MOSFET.

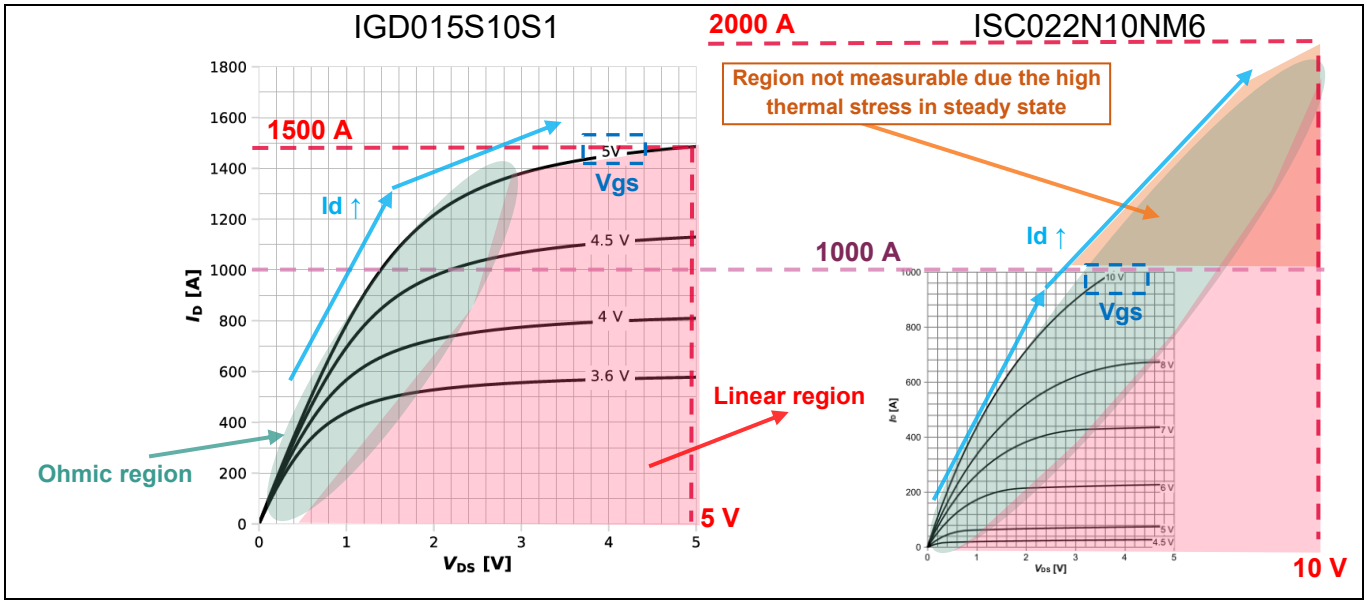

Figure 10 Output characteristics of the GaN HEMT [4] and MOSFET [5]

The temperature is not directly measurable due to the fast impulse and the thermal inertia of the devices. To extract temperature data, running a SPICE simulation with the device's equivalent thermal circuit is necessary. Figure 11 shows there is a high temperature increase during the ohmic to the linear region transition. This temperature increase can destroy the silicon device, which has more thermal inertia due to the molded package compared to the GaN device, consequently resulting in a different slope in the temperature rise.

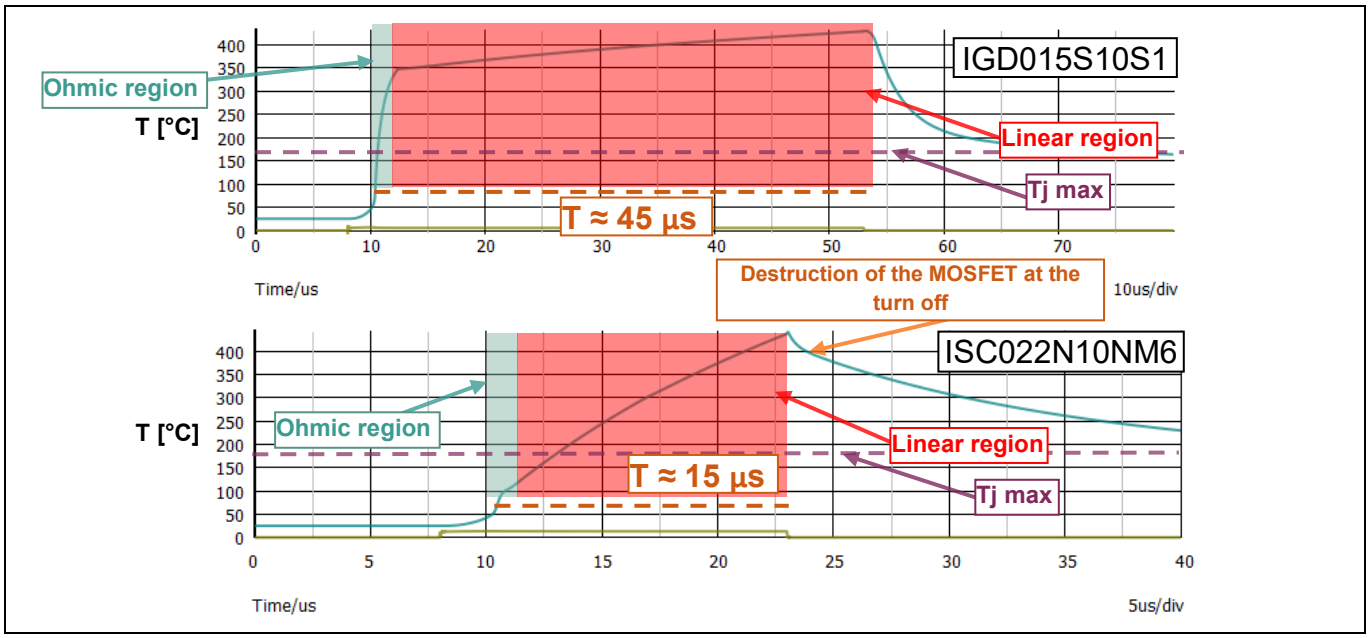

Figure 11 Temperature of the GaN HEMT [4] and MOSFET [5] in SPICE simulation for the setup in Figure 4

4 Half-bridge short-circuit withstand time (SCWT)

The half-bridge short-circuit withstand time (SCWT), frequently called leg short-circuit, represents the condition of failure on one side of the half-bridge, when one of the devices is broken (shorted), or in some cases when the V_{in} and SW (switching node of the phases of the inverter) are connected together.

In Figure 12, the implementation of the setup is represented, where the broken device is substituted with a shunt resistor of different values (listed in Table 2), and the current is measured through an IsoVu probe as mentioned in Section 2.2.

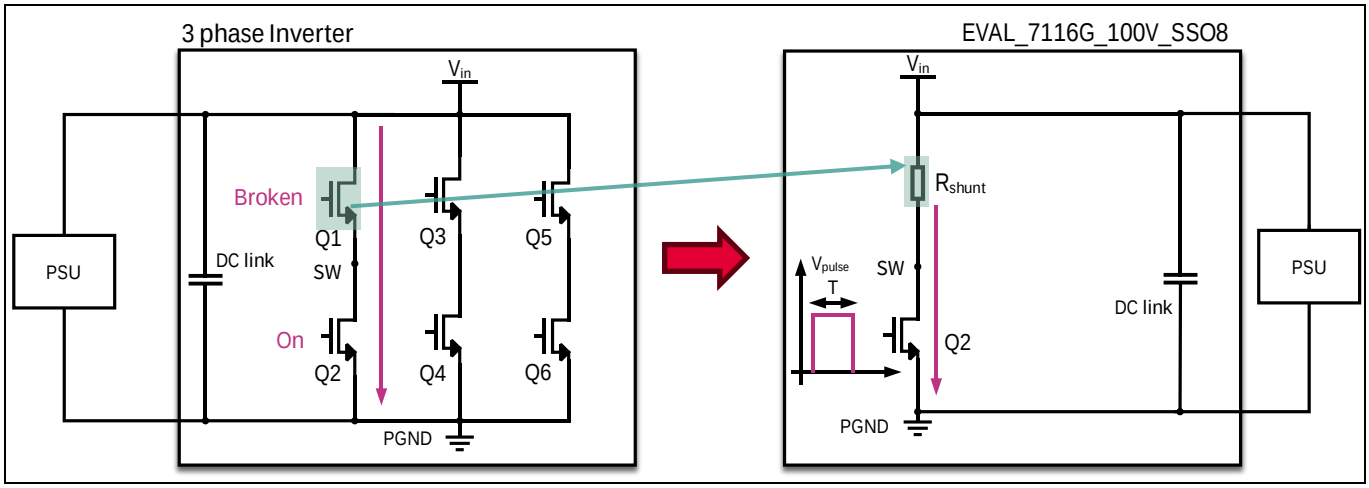

Figure 12 Phase short-circuit and test implementation on the evaluation board [7]

4.1 Schematic block and setup

The values of the setup in Figure 13 are reported in Table 2.

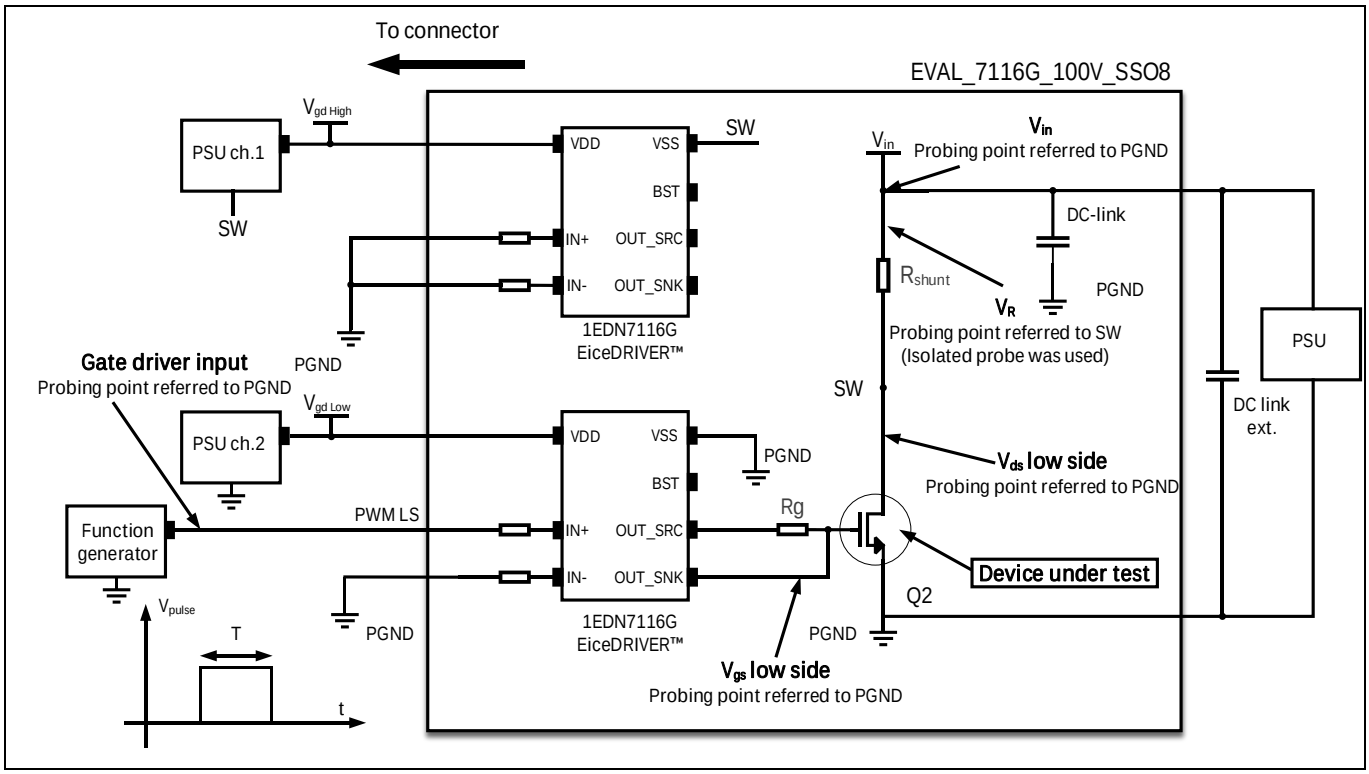

Figure 13 Schematic block of the half-bridge short circuit withstand time

In Figure 14, the shunt resistor used for the test is emphasized, where an optimal power loop is maintained by using a vertical layout implementation [7], which was made possible by utilizing the footprint of Q1 (Figure 4) device and keeping the resistor close to it to achieve magnetic cancellation during the switching event [3]. The low stray inductance of the layout corresponds to a ringless transition as well as a small amount of energy stored in the inductance, which can destroy the device during the turn-off of the device under test, which is the device Q2 (Figure 13).

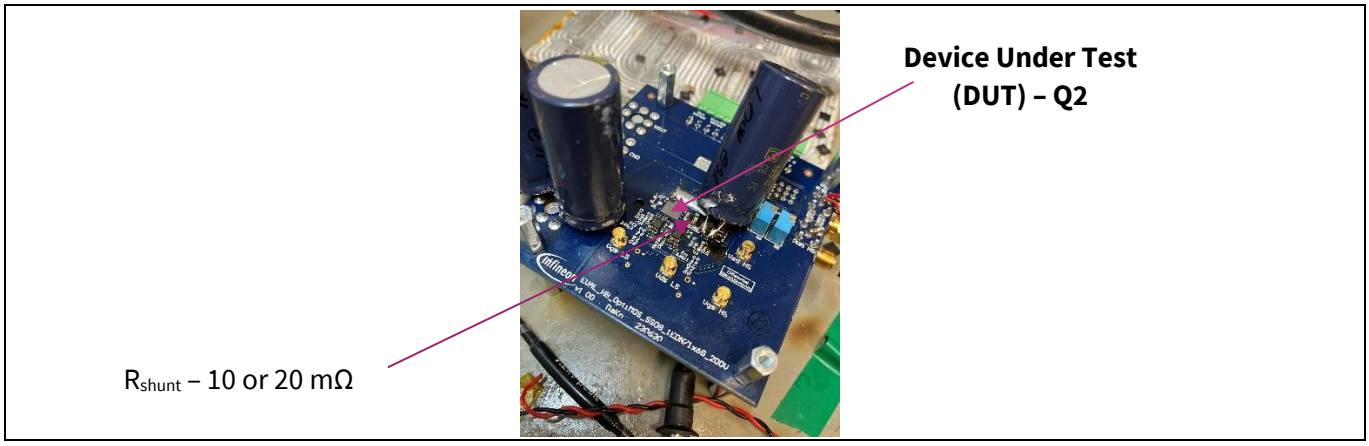

Figure 14 Setup of the half-bridge short circuit withstand time

The resistor (R_{shunt}) value is chosen to have a max. current >2000 A that will let the device under test enter the linear region (reported in Figure 10) and emulate a leg short.

Half-bridge short-circuit withstand time (SCWT)

Equation 3 and Equation 4 can be used to calculate the limit of the current of the value reported in Table 2 for what concerns the resistive load in an ideal setup (no parasitics).

$$I_{max} = \frac{V_{in}}{R_{Shunt}} = \frac{48\ V}{20\ m\Omega} \approx 2.4\ kA$$

Equation 3 Maximum current achievable with only the resistive load in Figure 13 for the GaN HEMT

$$I_{max} = \frac{V_{in}}{R_{Shunt}} = \frac{48\ V}{10\ m\Omega} \approx 4.8\ kA$$

Equation 4 Maximum current achievable with only the resistive load in Figure 13 for the MOSFET

Attention: Important notice of the chosen resistive load and real setup

The previous equations represent the ideal behavior of the circuit without taking into account the resistance (R_{on}) of the two transistors, [4] and [5], that are dependent on temperature.

Moreover, the drop of voltage during the transition is not considered, due to the difficulty in modeling of the stray inductance between all the capacitances added in the setup shown in Figure 2.

4.2 Test of 100 V OptiMOS™ 6

The results of the half bridge short circuit withstand time for OptiMOS™ ISC022N10NM6 [5] is in Figure 15. The waveform reports that the silicon device does not enter the thermal runaway region [10]. That is emphasized due to the current response being always below the saturation point of 2000 A at V_{gs} = 10 V, reported in Figure 6 and Figure 10. Moreover, the driver voltage (V_{gs} = 10 V) is above the zero temperature coefficient [11] and [12].

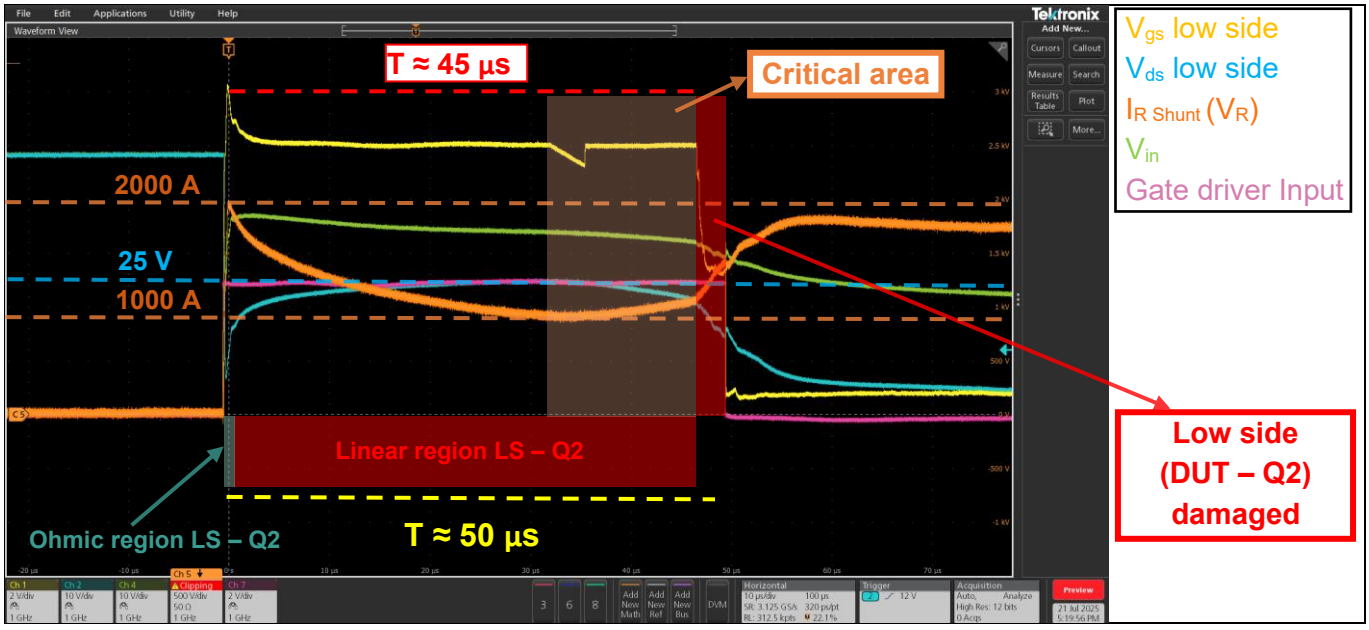

Figure 15 Measurements of the half-bridge short circuit withstand time with OptiMOS™ 6

In the overview of the waveform in Figure 15, the critical area is reported where the device exhibits a continuous increase in current even after crossing the linear region. This event is a consequence of high temperatures (>400°C) that transform the transistor to an intrinsic device that is no longer controllable and

behaves as a fixed current sink at this point [9], till the thermal stress destruction. More considerations of the temperature and the thermal stress are reported in Section 4.4.

4.3 Test of 100 V CoolGaN™

The result of the test of 100 V CoolGaN™ [4], as shown in Figure 16, has a time of several hundreds of microseconds with respect to the MOSFET as seen in Section 4.2, which is already reported in [13] and [14]. Figure 16 shows that the current enters the linear region after a few microseconds and then collapses to a fixed point of 150 A. This effect allows the device to maintain a short-circuit condition for a significantly longer time than the MOSFET, which is approximately 6 times lower, as seen in Figure 15.

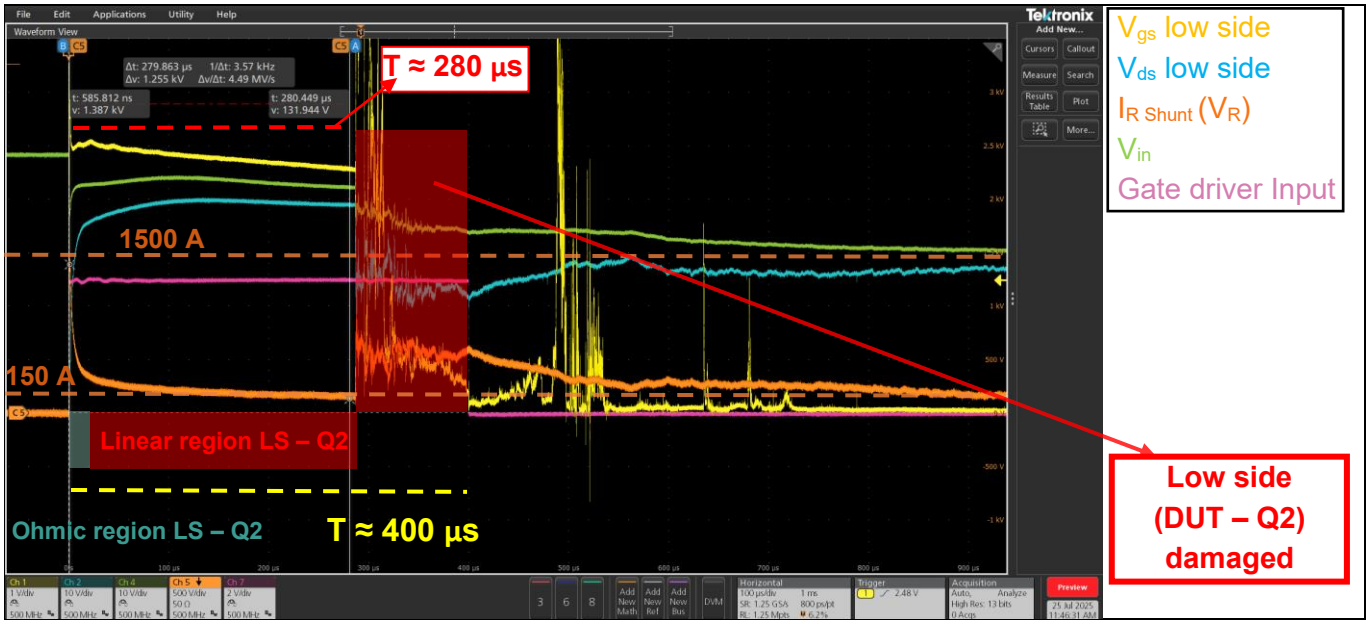

Figure 16 Measurements of the half-bridge short circuit withstand time with 100 V CoolGaN™

The damage to the transistors is always attributed to high thermal stress of the device, as previously discussed for the MOSFET in Section 4.2. The failure reported occurs in the middle of the pulse after 280 µs, whereas the MOSFET fails after 45 µs, as seen in Figure 15. The limitation of the current to only 150 A, compared to the MOSFET, is reported in Section 4.4, where temperature simulations are also presented.

4.4 Comparison of the results

The energy and power computed based on the tests in Section 4.2 and Section 4.3 are reported in Figure 17, where the values are calculated till the destruction of the device. It is evident that the high power of the silicon devices with respect to the GaN devices emphasize the possible high thermal stress reached from the part before the damage, ~45 µs before the failure. The GaN HEMT is able to run a short-circuit operation for a longer period of time due to the low power achieved from the transistor, which is around 280 µs.

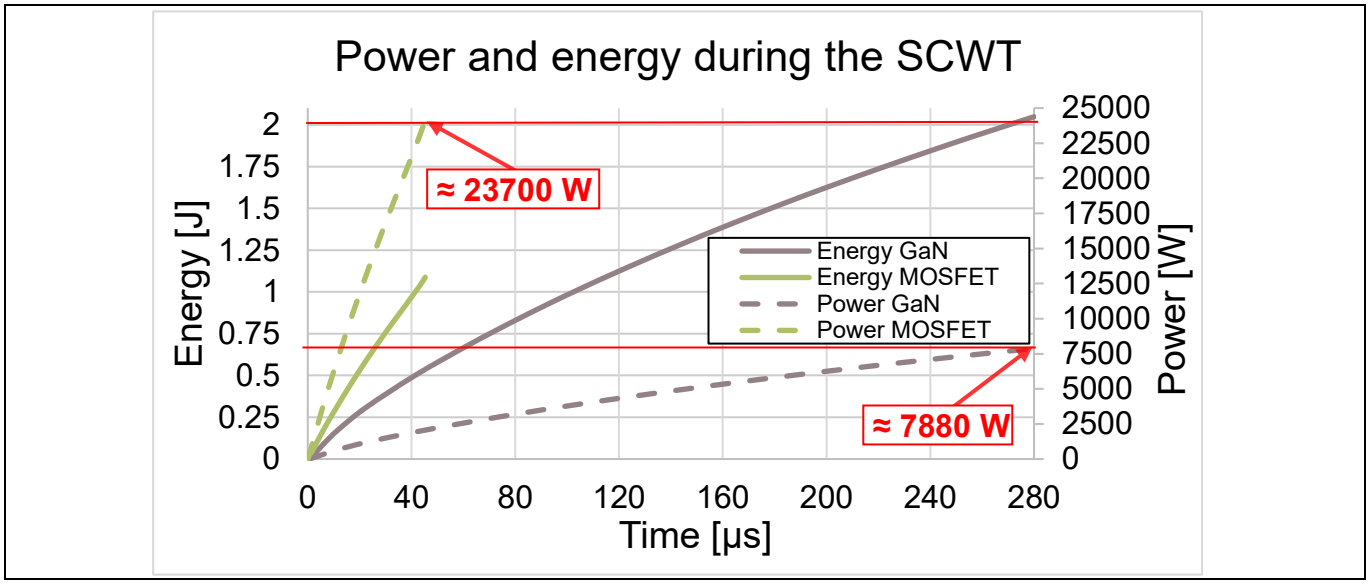

Figure 17 **Power and energy during the event of short circuit withstand time (SCWT)**

The evaluation of the power shown in Figure 17 for both technologies supports the analysis of the rise of temperature for a single pulse condition. In Figure 18 the thermal impedance expected for the single pulse of the SCWT is reported; the evaluation is done with the pulse time before destruction in both cases.

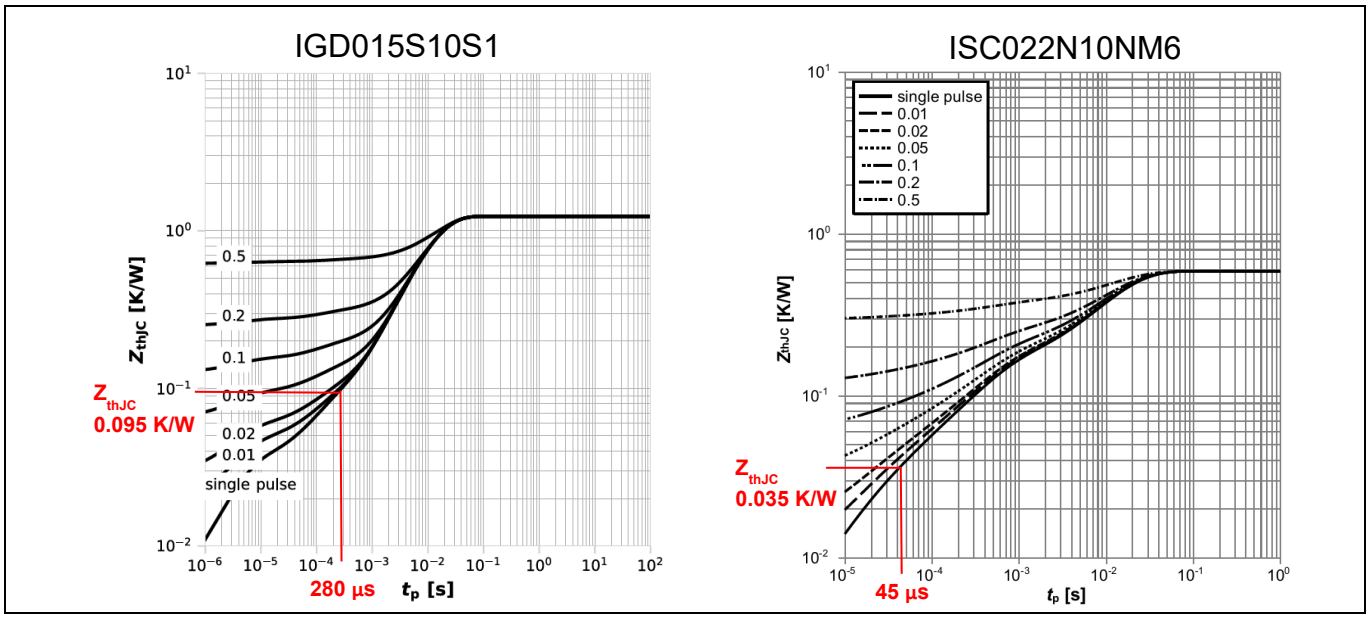

Figure 18 **Maximum transient thermal impedance for the GaN HEMT [4] and MOSFET [5] with relative short circuit pulses**

Equation 5 and Equation 6 report the rise of temperature related to the peak power achieved before the destruction event. In both cases the temperature achieved is higher than that of the maximum junction temperature and the devices enter the critical region (>400°C) where all the materials used in the MOSFET's construction can become fragile, as reported in [2] and [18].

$$\Delta T = Z_{th-JC} \cdot P_{peak} = 0.095 \frac{K}{W} \cdot 7880\,W \approx 750°C \quad \rightarrow \quad \Delta T = T_j + T_{amb.} = 750°C + 25°C = 775°C$$

Equation 5 **Maximum rise of junction temperature with a single pulse for the GaN HEMT [4]**

$$\Delta T = Z_{th-JC} \cdot P_{peak} = 0.035 \frac{K}{W} \cdot 23700\,W \approx 840°C \quad \rightarrow \quad \Delta T = T_j + T_{amb.} = 840°C + 25°C = 865°C$$

Equation 6 **Maximum rise of junction temperature with a single pulse for the MOSFET [5]**

The temperature of the device cannot be measured with instruments due to the fast response in a short amount of time. The overview is seen in Figure 19, generated with SPICE simulation.

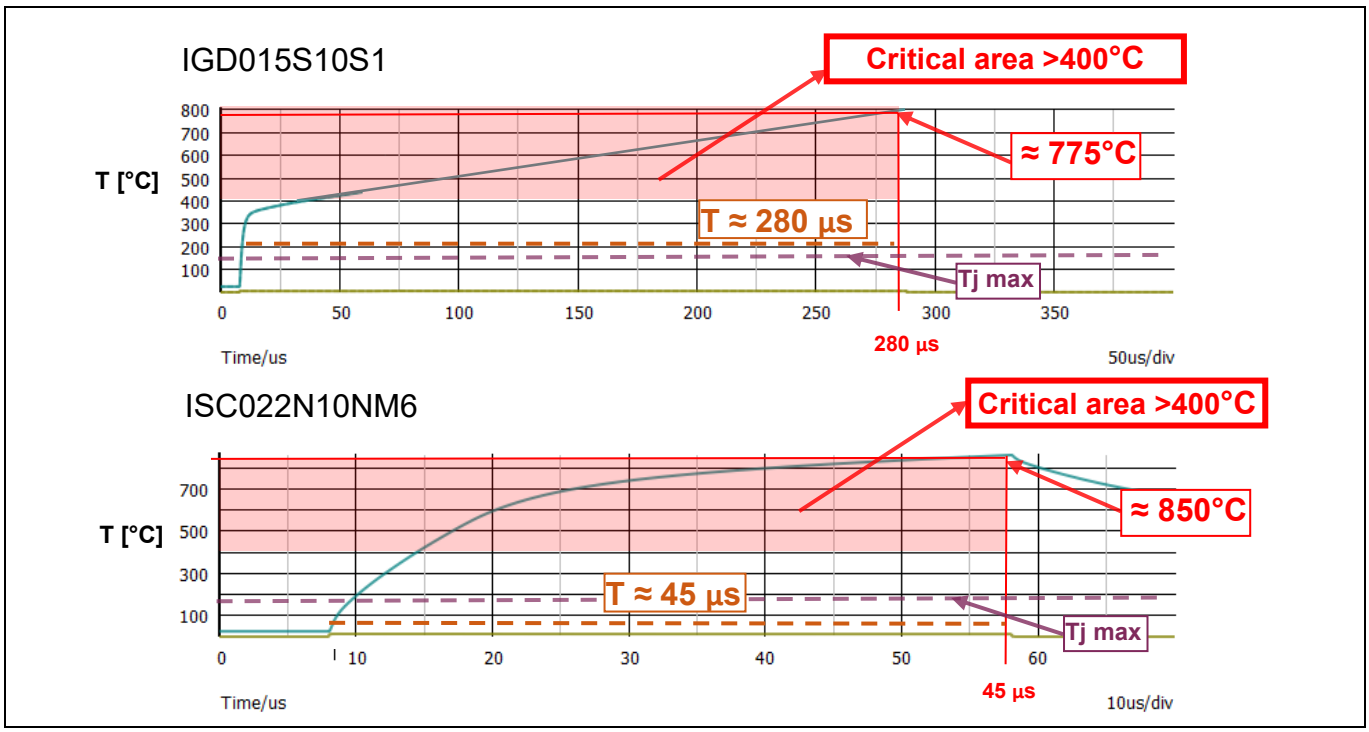

Figure 19 **Temperature of the GaN HEMT [4] and MOSFET [5] in SPICE simulation for the setup shown in Figure 13**

The temperature rises up to the same level before the failure of the transistors to the point that is sensitive to the degradation due to high thermal stress and the consequent hotspot ([15], [16], and [17]) that unbalances the current sharing over all the tranches or cells of the transistor.

The main reason behind the high amount of time during the short circuit condition for the GaN HEMT is related to the current limit reducing down to 150 A when the device is entering the linear region as shown in Figure 16. In contrast, the MOSFET maintains a high current in the linear region, with a reported value of 1000 A as seen in Figure 15. The derating of the current in the GaN HEMT is due to the high temperature achieved, as reported in Figure 19, which highlights the degradation of the current versus temperature in the transfer characteristics comparison with the MOSFET in Figure 20. The characteristics already report the difference between the two technologies, where the plot for different temperatures for the GaN HEMT always has a negative temperature coefficient with respect to the MOSFET. Below the Zero Temperature Coefficient (ZTC) point, the temperature has the impact of amplifying the current and creating a positive effect that ensures thermal runaway, as discussed in [19] and [20]. This phenomenon is magnified due to the less sensitive change of V_{th} over

temperature for the GaN HEMT compared to the MOSFET, with more details provided in a previous study [21]. The plot in Figure 20, from datasheets [4] and [5], reports the sensitivity of the temperature of the transconductance related to the working points of the short circuit withstand time (SCWT) of the tests. The GaN HEMT has a lower transconductance over temperature [15] compared to the MOSFET, guaranteeing a limit on power and consequently reducing thermal stress for the same amount of time, as seen in Figure 17.

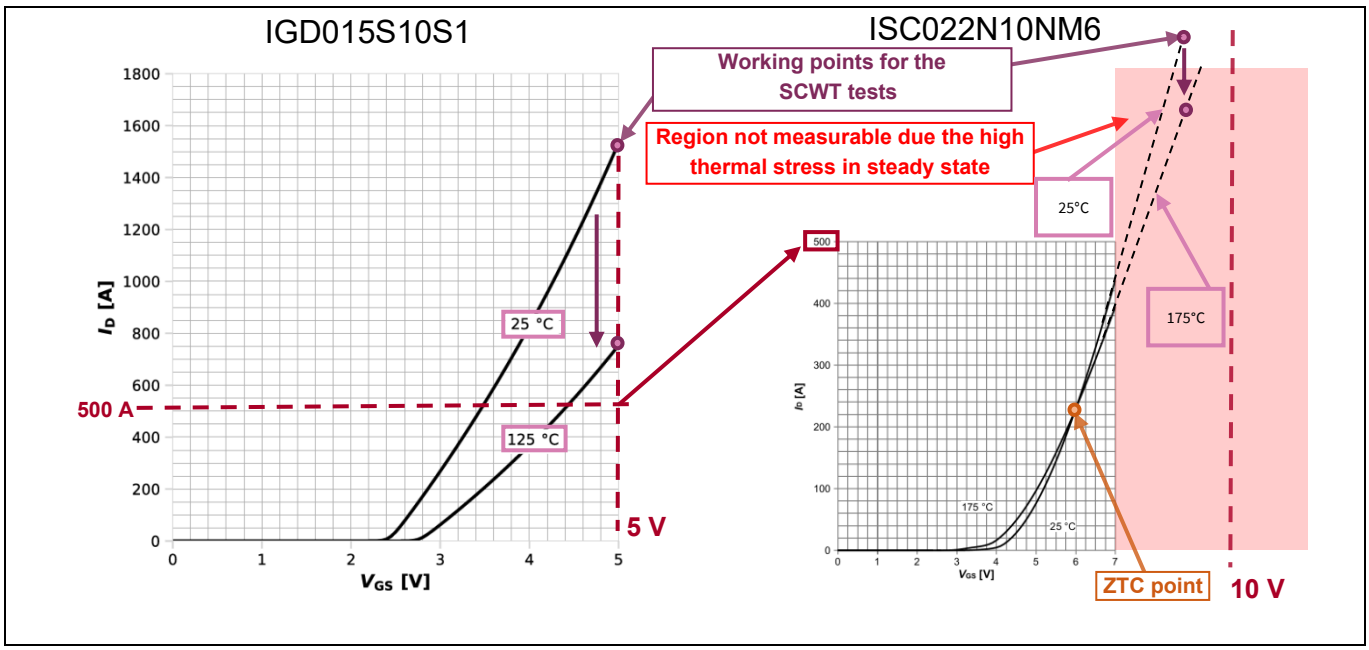

Figure 20 Transfer characteristics of the GaN HEMT [4] and MOSFET [5]

5 Conclusion

The application note presents the comparisons of short circuit tests for 100 V CoolGaN™ G3 (IGD015S10S1 [4]) and 100 V OptiMOS™ 6 (ISC022N10NM6 [5]), both available in a PQFN 5 mm × 6 mm package, in a drain-down configuration. The 59% larger die size for CoolGaN™ G3 results in a 63% lower $R_{DS(on)}$, when compared with OptiMOS™ 6.

The two types of short circuits have to handle a significant amount of current in a very short time period, and this tends to move the devices to exit from their SOA. In both short-circuit types, as seen in Section 3 and Section 4, the GaN HEMT reports a longer short-circuit time with respect to the MOSFET. This is because transconductance is lower for GaN over temperature compared to the MOSFET as detailed in Section 4.4 and also in [15]. This will limit the current naturally and maintain it for a longer time with a lower amount of current after the device enters the linear region of operation. The results present the possibility to have more flexible protection in terms of reaction times in such conditions.

6 Related resources

- Datasheets
  - Infineon Technologies AG: *Datasheet for IGD015S10S1 100 V G3 RQFN CoolGaN™ Transistor (2025)*; Available online
  - Infineon Technologies AG: *Datasheet for ISC022N10NM6 100 V OptiMOS™ Transistor (2023)*; Available online
  - Infineon Technologies AG: *User guide half bridge evaluation board for SSO8 package together with TDI EiceDRIVER™ 1EDN7116G (2024)*; Available online
- User guides
  - Infineon Technologies AG: *User guide half bridge evaluation board for SSO8 package together with TDI EiceDRIVER™ 1EDN7116G (2024)*; Available online
  - Infineon Technologies AG: *Designing an optimized half-bridge DC-DC converter with medium-voltage CoolGaN™ transistors (2025)*; Available online
- Application notes
  - Schoiswohl, J., Infineon Technologies AG: “Linear mode operation and safe operating diagram of power-MOSFETs”; (2017)

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[3] Infineon Technologies AG: *Designing an optimized half-bridge DC-DC converter with medium-voltage CoolGaN™ transistors (2025)*; Available online

[4] Infineon Technologies AG: *Datasheet for IGD015S10S1 100 V G3 RQFN CoolGaN™ Transistor (2025)*; Available online

[5] Infineon Technologies AG: *Datasheet for ISC022N10NM6 100 V OptiMOS™ Transistor (2023)*; Available online

[6] Infineon Technologies AG: *Datasheet for EiceDRIVER™ 1EDN71x6G, 200 V high-side TDI gate driver IC for GaN transistors and MOSFETs*; Available online

[7] Infineon Technologies AG: *User guide half bridge evaluation board for SSO8 package together with TDI EiceDRIVER™ 1EDN7116G (2024)*; Available online

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