Application Note AN-1200

RIC7113 Vdd/Vcc Power Sequencing

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1. Introduction

Since the mid 1990's, The RIC7113/IR2113 family of HVIC's have served many thousands of applications ranging from DC to DC converters to motor drives to ultrasonic and induction heaters. Application spaces include consumer/industrial applications as well as military applications that require Rad Hard IC's. The architecture of the IC is tried and true.

The IC has two different power supply inputs. The input referred to as Vdd is the front end of the IC. This supplies the input circuitry. For a 5V TTL input, this supply would be tied to a 5V source. It can be tied to a supply as low as 3.3V to accept 3.3V TTL signals directly on the inputs.

There are several different power sequencing scenarios that may be applied to the RIC7113 IC and its sister device on the commercial side. These different scenarios are:

- Vcc comes up before Vdd
- Vdd comes up before Vcc
- Vdd and Vcc are tied together

This work will explore these power up scenarios and one particular anomaly that was found.

2. Test Schematic

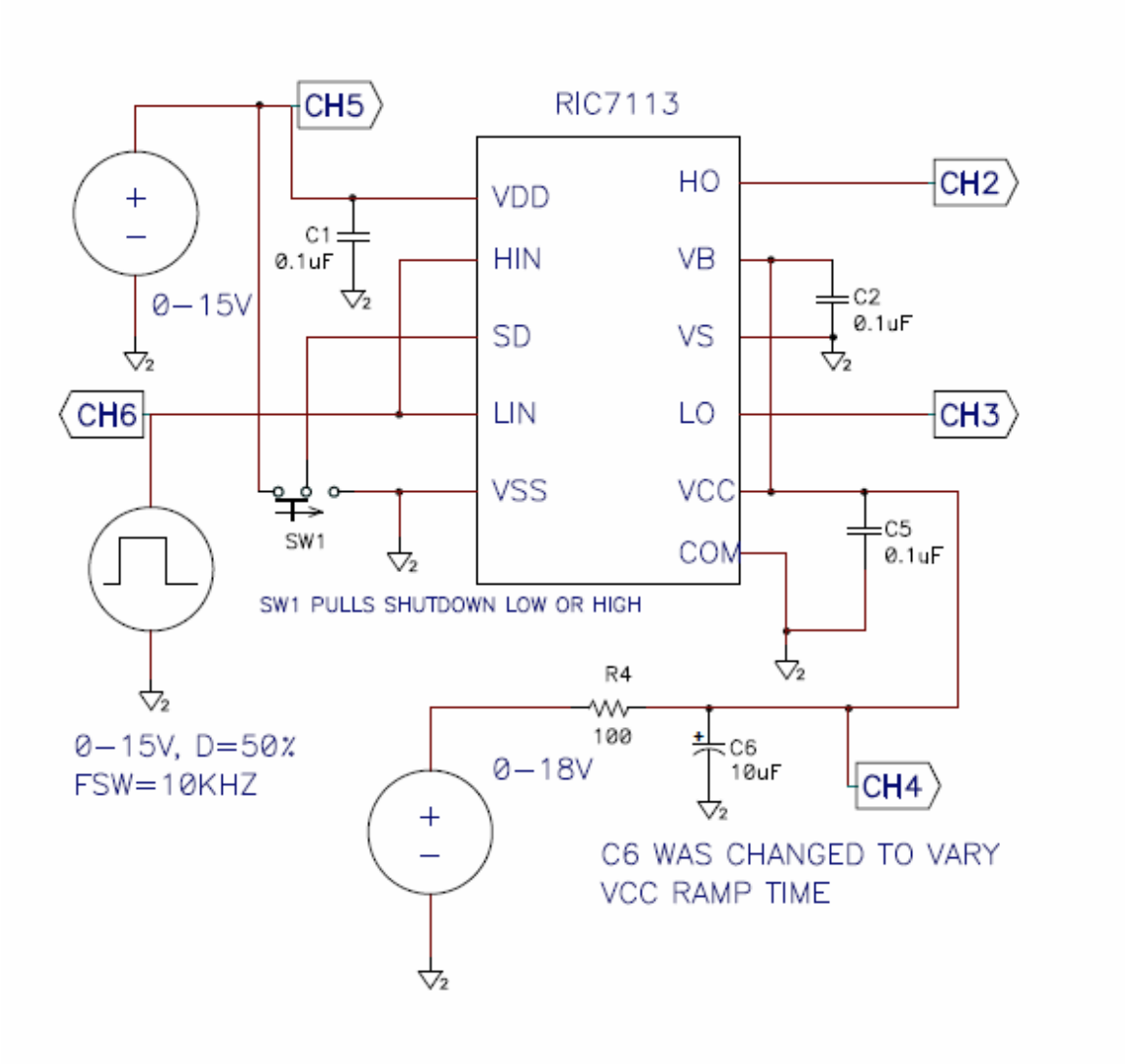


Figure 1: Schematic of Test Circuit

3. Test Results

3.1 Vcc and Vdd tied together; Lin pulses applied through startup event

The inputs to the RIC7113 have ESD clamping diodes to Vdd and Vss. It is important to understand this for sequencing reasons. If Vcc is brought up first, followed by the application of input pulses to Lin and or Hin pins, the input will forward bias the high side ESD protection diodes and pump Vdd up to approximately 0.6V below the voltage compliance of the input pulses on Hin and or Lin. This is enough to turn on the input circuitry and start the operation of the IC. If Vdd and Vcc are tied together, both rails are pumped up. The waveforms are identical for these two startup modes.

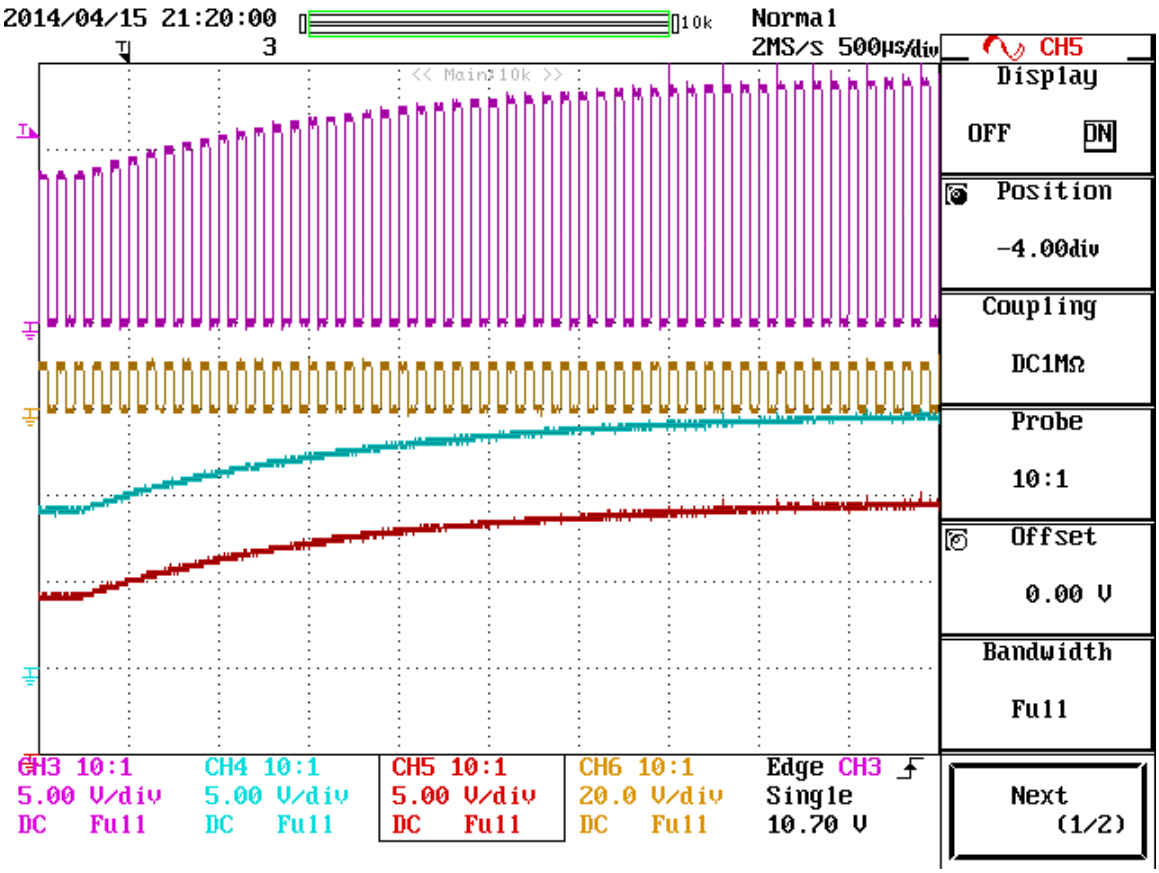


Figure 2: ESD clamp diodes on inputs rectify gate pulses to the peak voltage of the applied pulse less the forward drop of the ESD clamp diode. Vdd capacitor charges up to this value. When voltage is applied to Vdd and Vcc terminals, there is a slight rise in voltage. Nothing anomalous observed.

3.2 Vcc is on before Vdd; Lin pulses applied through startup event

See above section. Waveforms are identical. No anomaly observed

3.3 Vdd is on before Vcc; Lin pulses applied through startup event

This power up sequence is not adviseable. If Vcc is asserted after Vdd has settled to its nominal value, there may be a slight anomaly on the output of the IC.

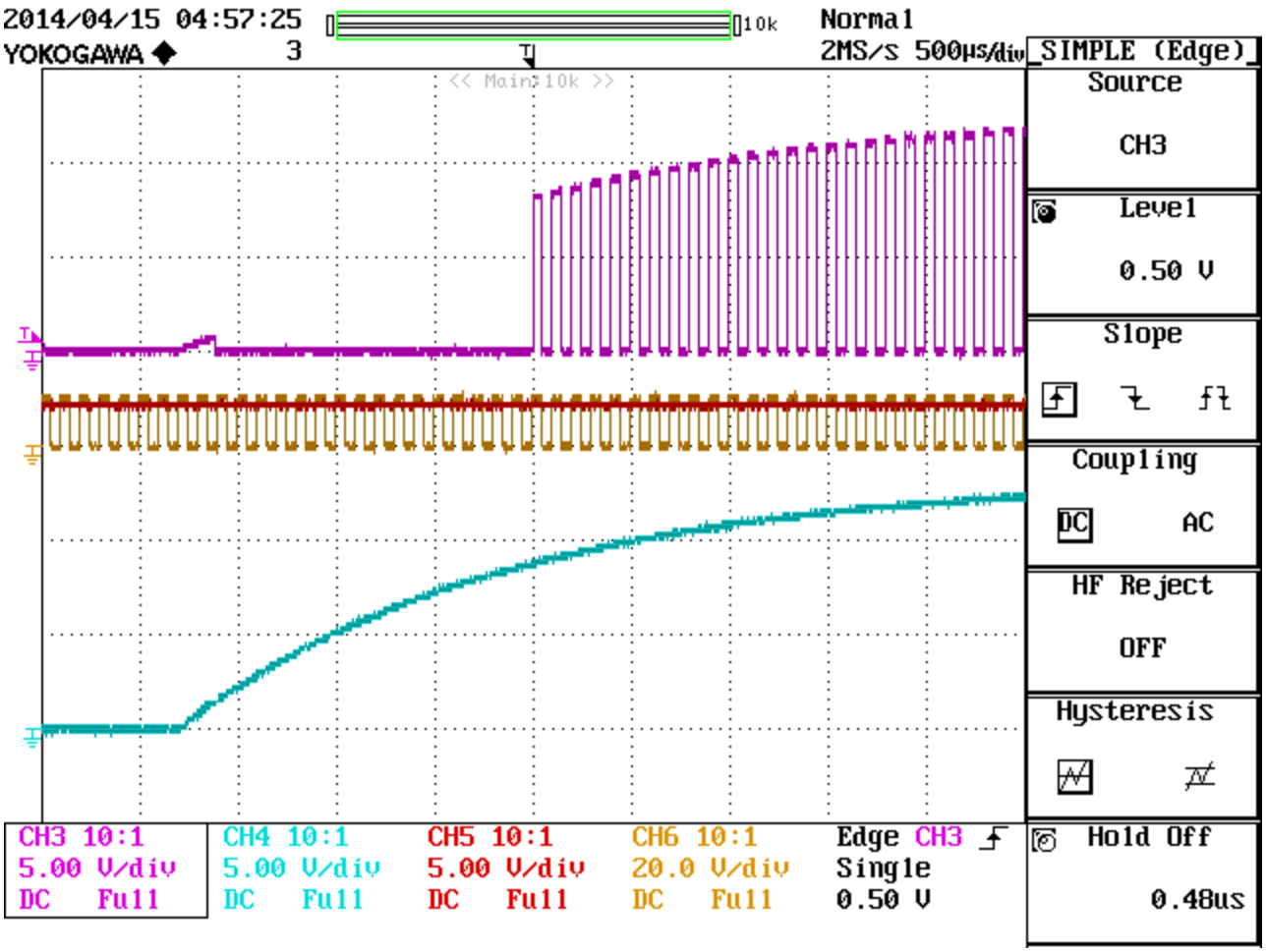


Figure 3: Industrial part: IR2113, Hi side input grounded, high side output open circuited. Anomaly output pulse shows about 1V peak as Vcc passes through about 2V.

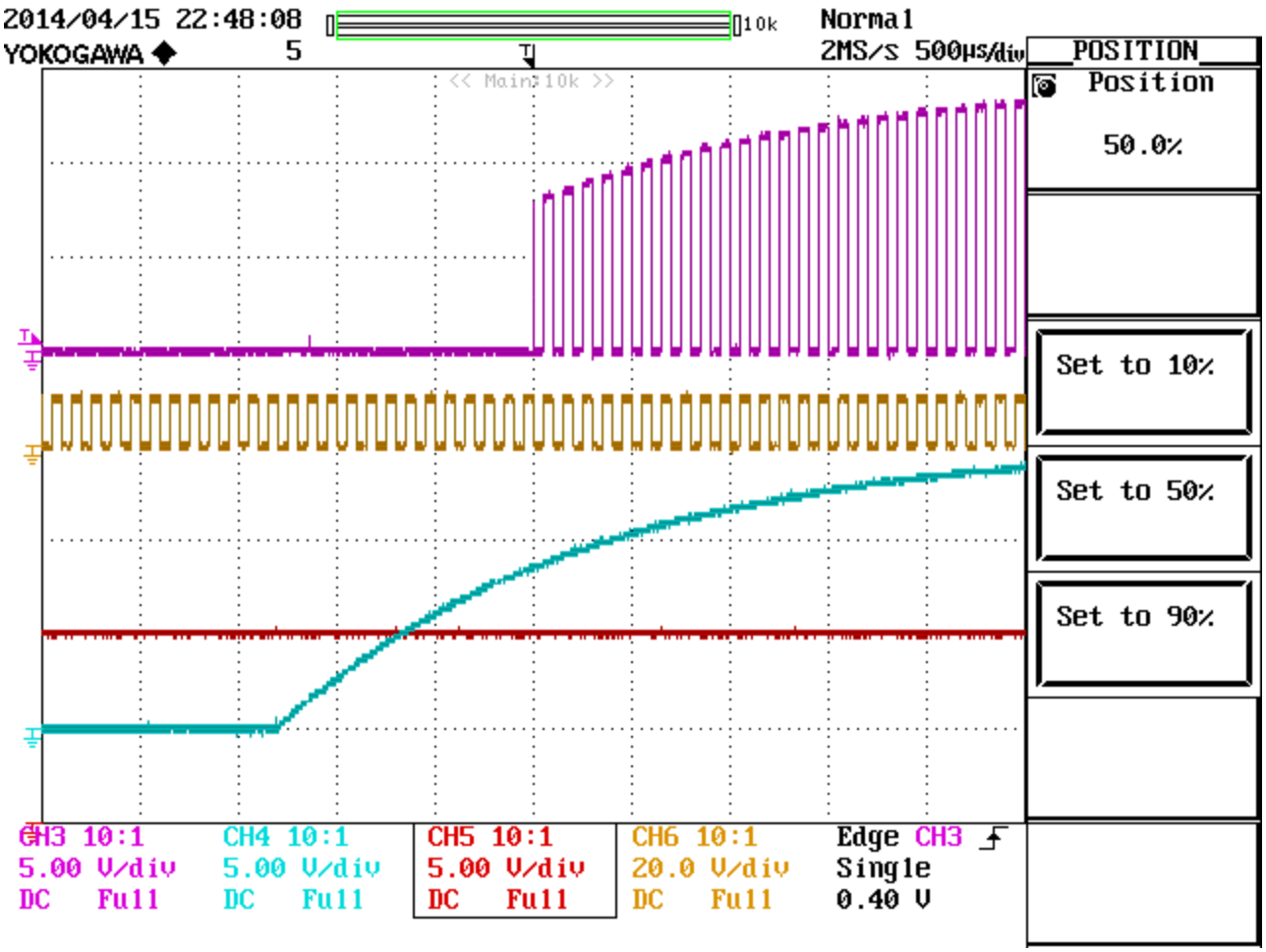


Figure 4: same setup as Figure 2 only with RIC7113 serial number 7-34. Very narrow anomaly output pulse.

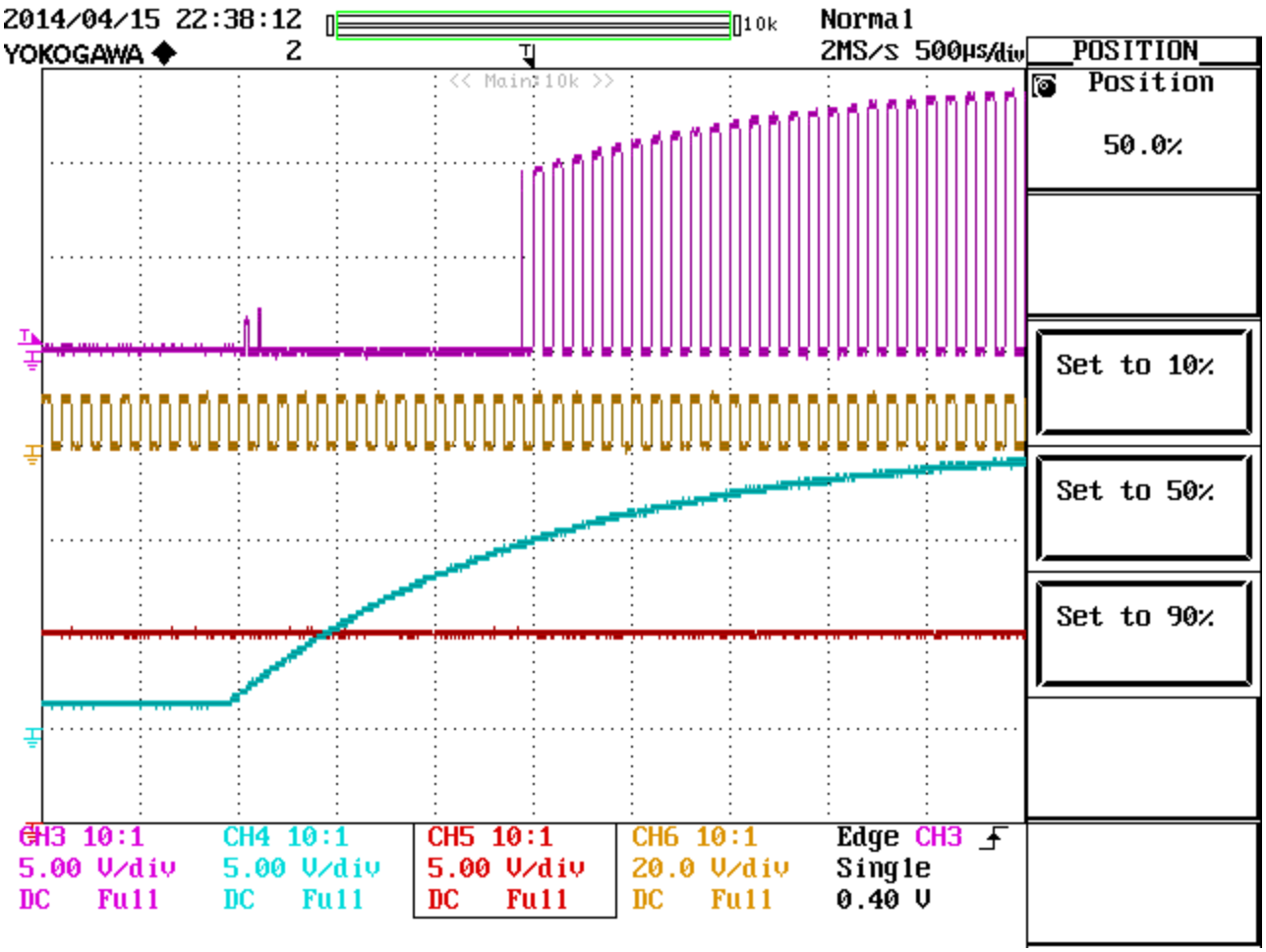


Figure 5: Same setup as figure 2. RIC7113 Serial Number 118-37 shows longer, repetitive anomaly output pulses.

3.4 Vdd is on before Vcc; Hin and Lin pulses held low through startup event
Nothing anomalous observed. Outputs remain at zero.

3.5 Vcc is on before Vdd; Hin and Lin pulses held low through startup event
Nothing anomalous observed. Outputs remain at zero.

3.6 Vcc and Vdd tied together; Hin and Lin pulses held low through startup event
Nothing anomalous observed. Outputs remain at zero.

3.7 Impact on high side driver
For these tests the high side driver connections are rudimentary. Vboot is tied to Vcc (ramped supply), Vs is tied to power ground, H_out is then ground referenced. There were a couple of slight anomalies observed, however the voltage amplitude of the nuisance output pulse is much lower.

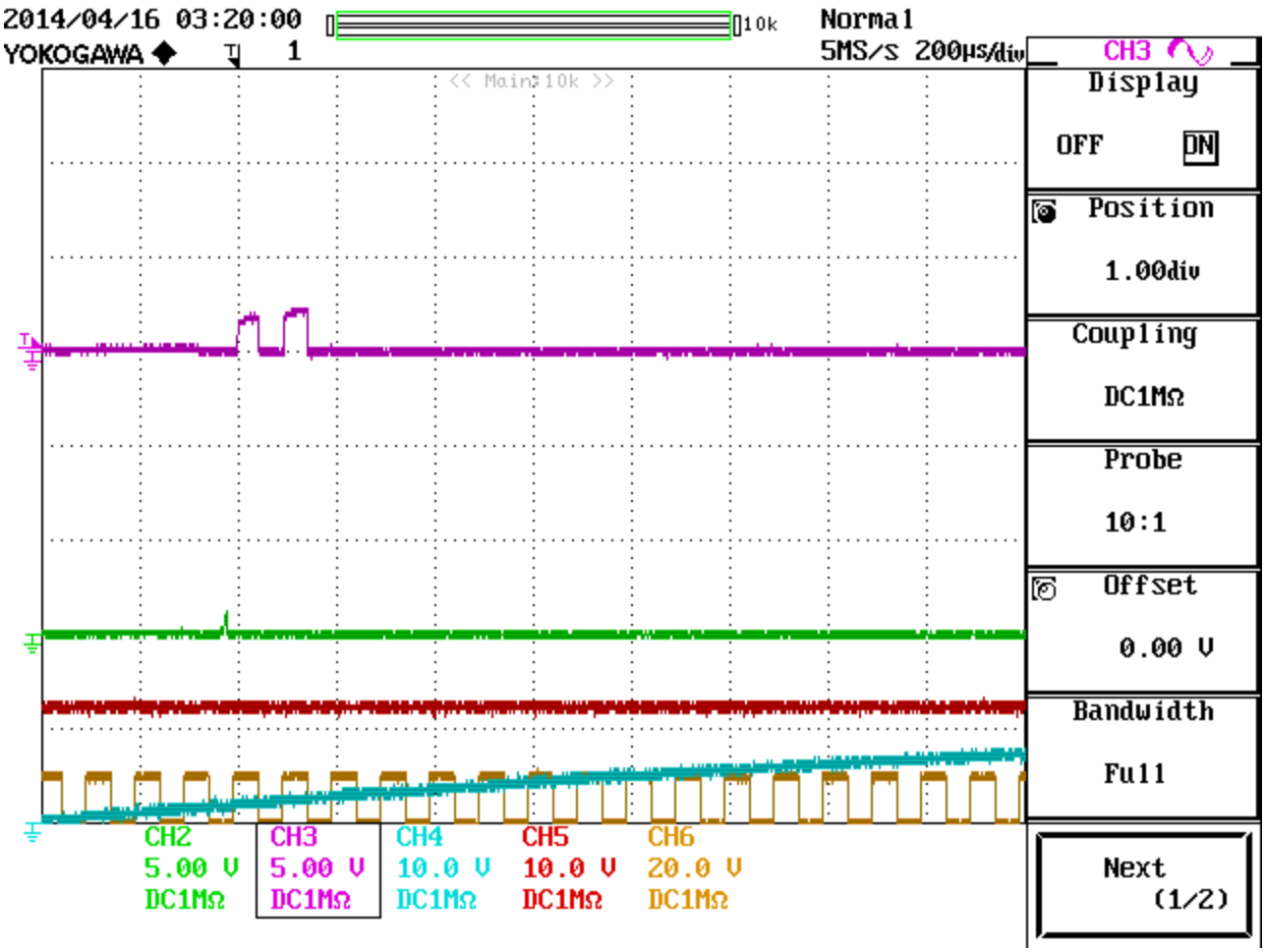


Figure 6: The impact on the high side driver is less, but it is still apparent (green trace).

3.8 Frequency of anomaly

The frequency of the anomaly is quite small. On the bench,10 to 20 startup events had to be forced to catch one anomalous turn on event.

3.9 Radiation dependency

Of some 20 parts tested, some parts had been exposed to full datasheet irradiation, some had been exposed to a partial dose, some had been exposed to a full dose and some had never seen any radiation at all (including the commercial/industrial parts). The results indicate that the anomaly is not impacted by radiation dosage.

3.10 Notes on speed of power up waveforms:

Power up ramps were set up as long as 1 second, as fast as 500us, all exhibited problems at about the same frequency.

3.11 Switching Frequency dependency:

There was no switching frequency dependency observed.

3.12 Pulse width dependency:

There was no pulse width dependency observed.

3.13 SD Assertion

There was no anomaly observed with Shutdown tied to Vdd during any power up sequence

4.0 Explanation of why this occurs

If we interpret the data, we have an anomaly that occurs when there are gate pulses present AND the Logic Supply (Vdd) is at nominal value with rising Vcc. If we take a look at the internal workings of the IC, there is an undervoltage lockout circuit (UVLO) on both the logic supply (Vdd) and the power driver section (Vcc). We have seen that with active input pulses and no Vdd applied, the ESD clamp diodes simply conduct and pump the applied input pulses into the Vdd capacitance. With active inputs, the UVLO section of the Vdd section isn't really seen. Further, without active inputs, the UVLO section on the Vdd side operates as it should, as does the UVLO circuit on the Vcc side.

Both the Vcc and Vdd UVLO circuits are comprised of a zener reference, a current source to feed it, a comparator and a voltage divider referenced to Vcc or Vdd respectively.

At very low voltages, when the input voltage in the Vcc UVLO circuit is well below the zener voltage, the comparator sees a relatively high voltage at the negative terminal. This is due to the current source being in saturation and the zener looking like a high impedance (Vin<Vzener). In this state, the voltage divider holds the positive terminal of the comparator at a fairly low voltage, thereby making the output deterministic: The IC is in UVLO state, no outputs passed.

As the Vcc supply comes up and the zener approaches its knee voltage the current source comes out of saturation and the zener impedance drops to its relatively stable clamping voltage. During this transition period from high to low impedance with rising Vcc, the reference leg of the comparator is not as deterministic. The noise burst associated with the zener coming into bias can be passed by the comparator causing an active state on the high or low outputs. This usually occurs between Vcc of 1.8 and 2.5V. Under these conditions, the erratic operation captured above is plausible.

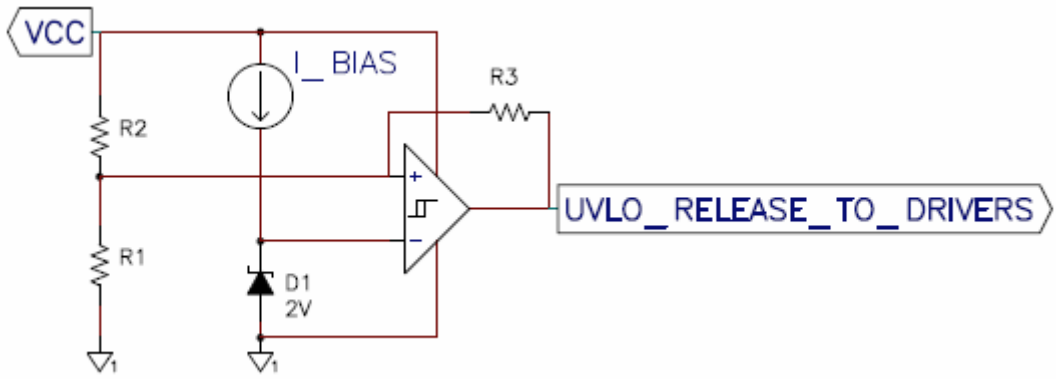


Figure 7: block diagram of internal UVLO circuit

5.0 Conclusions

From an applications standpoint, the net impact of this anomaly is quite small. These are the applications that use separate input supplies (Vdd) and drive section supplies (Vcc). Of this group, the anomaly will only be seen in those circuits where Vcc comes up after

Vdd. Further, this will only be a problem at hot temperatures where the threshold voltage of the mosfet being driven drops into the range of the anomaly voltage.

The anomaly output pulse is most always below 2V, in most cases observed it was below 1V. Based on existing information, the best design practice for this part may be to:

1. Use good layout techniques and MLCC bypassing as near Vcc, Vdd and Vboot/Vs as possible. This is not at all related to the anomaly described here in, however it is in line with good design practice.
2. Assert Shutdown pin high through power up event.
3. Bring up Vcc and Vdd together (monotonically) or Vcc first
4. Release shutdown and Apply input pulses to Hin, Lin after Vdd and Vcc is at nominal value
5. If possible, apply a few low side pulses first to allow the lowside power switch to turn on and provide a path to charge the bootstrap capacitor on the high side driver. This will make both high and low side operation maximally deterministic.
6. Keep the minimum pulse width above 100ns for both the high and low side inputs.