RIC70849 Design Tool

Application Note

About this document

Scope and purpose

This document describes the use of RIC70849 Design Tool and details the theory and calculations to configure RIC70849 for point of load (PoL) applications.

Intended audience

The intended audience for this document is Power Electronics Design Engineers, Technicians, and Developers of electronic systems.

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1 Introduction

The RIC70849 is a rad-hard buck controller and gate driver IC intended for use in PoL converter applications such as space-grade FPGA and ASIC power rail conversion and satellite system power distribution. The RIC70849 is optimized to drive the gates of Gallium Nitride (GaN) HEMT FETs with a tightly regulated 4.8V gate driving voltage, enabling higher switching frequencies, smaller magnetics, and higher efficiency operation across a wide input and output voltage range. However, the RIC70849 is also compatible with logic-level (LL) Si MOSFETS and can drive both GaN and LL Si FETS, ensuring reliable and flexible power conversion applications for a variety of space missions.

This Design Tool will assist with configuring the RIC70849 through the automation of passive component value calculations, efficiency estimates, and control loop frequency response analysis.

The RIC70849EVAL1 evaluation board utilizes IR HiRel IG1NT052N10R GaN FETs for high and low-side switches, and this Design Tool's prepopulated selected FET values have been chosen to match these GaN FETs. To view all the available rad-hard GaN HEMT product options, visit the IR HiRel rad-hard GaN webpage.

2 Calculation Example

RIC70849 Design Tool is a comprehensive tool used to recommend components and model system behavior of the RIC70849 in a PoL buck controller application. Figure 1 shows the front page of the Design Tool. Using user-provided, known target system parameters in Section 1, the tool calculates nominal component values shown in Section 2. The Design Tool plots total converter efficiency and AC frequency response (control to output) of the system. If desired, the user can input standard values to further model and optimize converter performance. When first opened, the tool is pre-filled with a RIC70849 design example, and this design example will be covered throughout this application note.

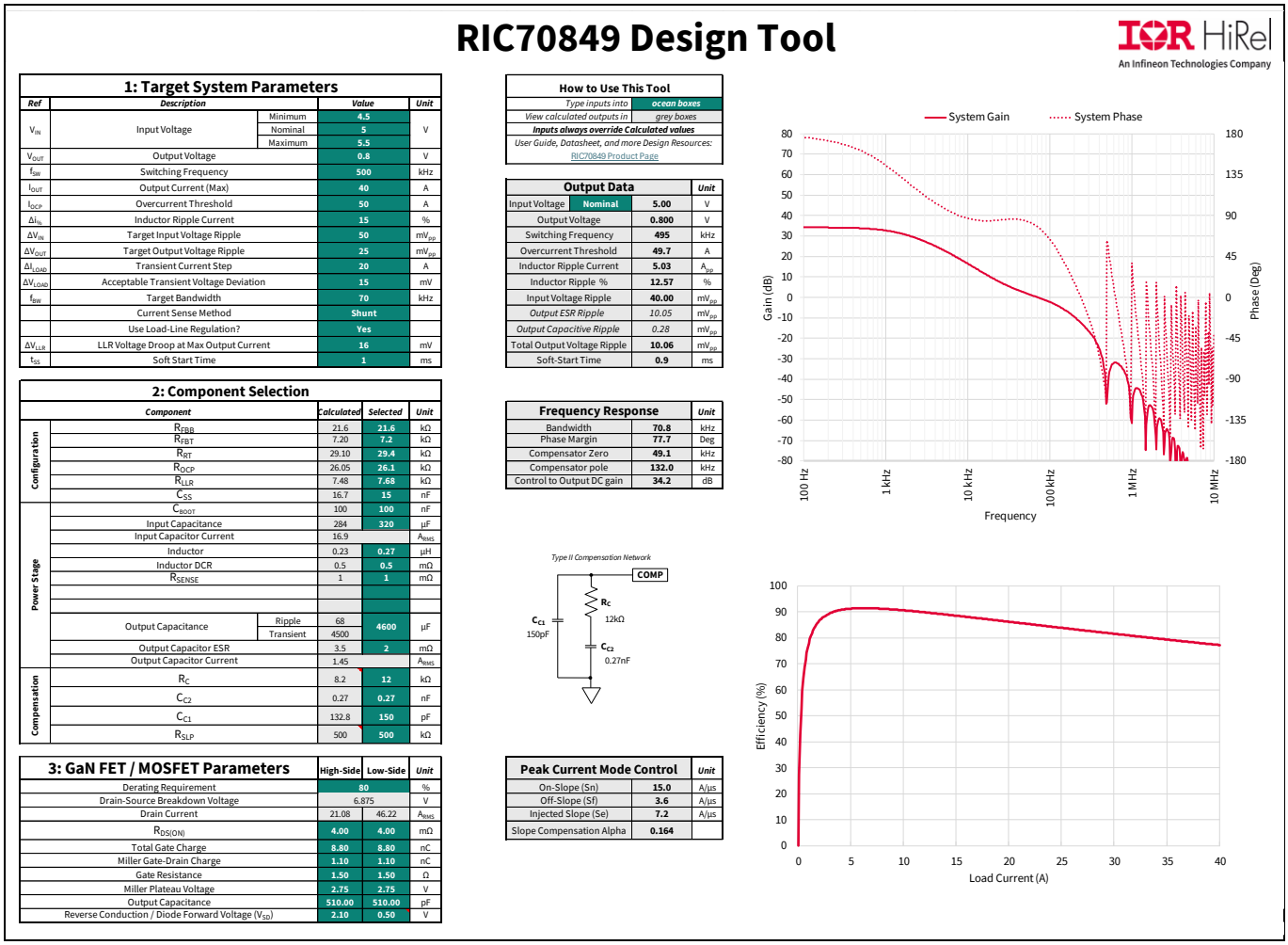


Figure 1 RIC70849 Design Tool Front Page

2.1 Tool Operation

The Calculator page provides the input cells and a summary of the system performance given the conditions and components. All grey-colored cells are calculated outputs, while ocean-colored cells are user-provided inputs. To start, system parameters must be input into Section 1. These are high-level parameters that dictate the remainder of component choices. The choices for this design example are detailed in Table 1 and pictured in the Design Tool in Figure 2.

Table 1 Design Example Parameters

Reference	Term	Description	Value	Unit
V_{IN}	Input Voltage (min/nom/max)	Minimum, nominal, and maximum input voltage	4.5/5/5.5	V
V_{OUT}	Output Voltage	Regulated output voltage	0.8	V
f_{SW}	Switching Frequency	Switching frequency of the converter	500	kHz
I_{OUT}	Output Current	Maximum DC output current	40	A
I_{OCP}	Overcurrent Threshold	Overcurrent trip threshold for Overcurrent Protection	50	A
$\Delta i_{\%}$	Inductor Ripple Current	Inductor ripple current target as a percent of maximum DC output current	15	%
ΔV_{IN}	Target Input Voltage Ripple	Maximum peak-to-peak input voltage ripple requirement	50	mV_{PP}
ΔV_{OUT}	Target Output Voltage Ripple	Maximum peak-to-peak output voltage ripple requirement	25	mV_{PP}

Reference	Term	Description	Value	Unit
ΔI_{LOAD}	Transient Current Step	Change in current under maximum load transient conditions	20	A
ΔV_{LOAD}	Acceptable Transient Voltage Deviation	Maximum change in converter output voltage during transient load	15	mV
f_{BW}	Target Bandwidth	Compensated AC response target bandwidth	70	kHz
	Current Sense Method	Method to sense inductor current for peak current mode control. DCR uses the DCR of the inductor, while Shunt uses a shunt resistor between the inductor and output capacitors. See Section 3.3.3 for more details.	Shunt	
	Load-Line Regulation	LLR is a feature to improve transient performance of the converter by intentionally decreasing output voltage under heavy loads. See Section 3.3.4 for more details.	Yes	
ΔV_{LLR}	LLR Voltage Droop	LLR decreases the output voltage proportionally to load current. The voltage droop sets the change in output voltage from the setpoint at maximum DC load. (Section 3.3.4)	16	mV
t_{SS}	Soft Start Time	Sets the soft-start time of output voltage during converter startup.	1	ms

1: Target System Parameters				
Ref	***Description***		***Value***	***Unit***
V_{IN}	Input Voltage	Minimum	**4.5**	V
		Nominal	**5**	
		Maximum	**5.5**	
V_{OUT}	Output Voltage		**0.8**	V
f_{SW}	Switching Frequency		**500**	kHz
I_{OUT}	Output Current (Max)		**40**	A
I_{OCP}	Overcurrent Threshold		**50**	A
$\Delta i_{\%}$	Inductor Ripple Current		**15**	%
ΔV_{IN}	Target Input Voltage Ripple		**50**	mV_{pp}
ΔV_{OUT}	Target Output Voltage Ripple		**25**	mV_{pp}
ΔI_{LOAD}	Transient Current Step		**20**	A
ΔV_{LOAD}	Acceptable Transient Voltage Deviation		**15**	mV
f_{BW}	Target Bandwidth		**70**	kHz
	Current Sense Method		**Shunt**	
	Use Load-Line Regulation?		**Yes**	
ΔV_{LLR}	LLR Voltage Droop at Max Output Current		**16**	mV
t_{SS}	Soft Start Time		**1**	ms

Figure 2 System Parameters Input

After the system parameters are entered into the Design Tool, the remaining sections will update with results. Section 2 displays Calculated component values, each of which can be overridden with user-chosen standard values (Figure 3). The plots and Output Data of the Tool use **Selected** values for computation if provided, otherwise **Calculated** values are used.

2: Component Selection					
	Component		***Calculated***	***Selected***	***Unit***
Configuration	R_{FBB}		21.6	**21.6**	kΩ
	R_{FBT}		7.20	**7.2**	kΩ
	R_{RT}		29.10	**29.4**	kΩ
	R_{OCP}		26.05	**26.1**	kΩ
	R_{LLR}		7.48	**7.68**	kΩ
	C_{SS}		16.7	**15**	nF
Power Stage	C_{BOOT}		100	**100**	nF
	Input Capacitance		284	**320**	µF
	Input Capacitor Current		16.9		A_{RMS}
	Inductor		0.23	**0.27**	µH
	Inductor DCR		0.5	**0.5**	mΩ
	R_{SENSE}		1	**1**	mΩ
	Output Capacitance	Ripple	68	**4600**	µF
		Transient	4500		
	Output Capacitor ESR		3.5	**2**	mΩ
	Output Capacitor Current		1.45		A_{RMS}
Compensation	R_C		8.2	**12**	kΩ
	C_{C2}		0.27	**0.27**	nF
	C_{C1}		132.8	**150**	pF
	R_{SLP}		500	**500**	kΩ

Figure 3 Component Selection

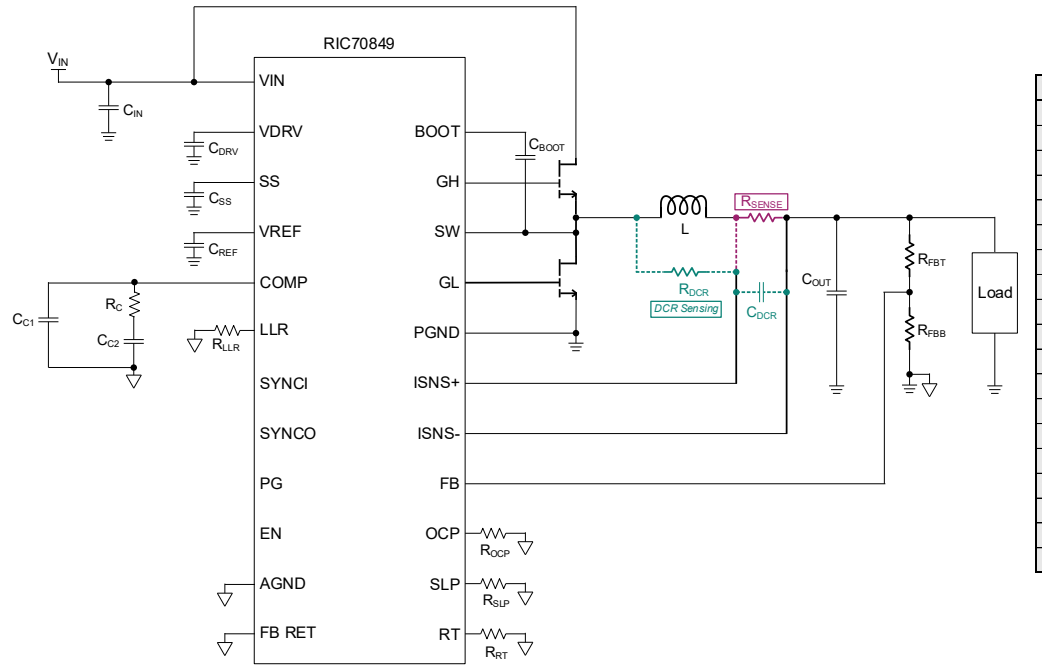
GaN FET or MOSFET parameters can be entered into Section 3 (Figure 4). These fields are populated with RIC70849EVAL1 IG1NT052N10R GaN FET parameters by default [5]. However, if different FETs are used, this section must be manually updated for accurate efficiency calculations. The Derating Requirement can be used to apply a required safety margin for the calculated Drain Current and Drain-Source Breakdown Voltage. Once all parameters are entered, the output values, Bode plot, and efficiency curve will populate with updated calculated results based on the input component choices and system definition.

3: GaN FET / MOSFET Parameters	High-Side	Low-Side	*Unit*
Derating Requirement	80		%
Drain-Source Breakdown Voltage	6.875		V
Drain Current	21.08	46.22	A_{RMS}
$R_{DS(ON)}$	4.00	4.00	mΩ
Total Gate Charge	8.80	8.80	nC
Miller Gate-Drain Charge	1.10	1.10	nC
Gate Resistance	1.50	1.50	Ω
Miller Plateau Voltage	2.75	2.75	V
Output Capacitance	510.00	510.00	pF
Reverse Conduction / Diode Forward Voltage (V_{SD})	2.10	0.50	V

Figure 4 FET Parameters

2.2 Schematic

The schematic shows component values listed in the BOM, cross-referenced to the PoL application schematic of the device. If selected values are not input on the Overview page, this will populate using calculated values based on system inputs. For accurate frequency response, efficiency, and calculated values, user-provided Selected components should be input on the Calculator page. Figure 5 depicts the schematic for the design example.



Designator	Value	Unit
R_{OCP}	26.1	kΩ
R_{SLP}	500	kΩ
R_{RT}	29.4	kΩ
R_{LLR}	7.68	kΩ
R_C	12	kΩ
C_{C2}	0.27	nF
C_{C1}	150	pF
C_{DRV}	1	µF
C_{SS}	15	nF
C_{REF}	1	nF
C_{BOOT}	100	nF
C_{IN}	320	µF
L	0.27	µH
C_{OUT}	4600	µF
R_{FBT}	7.2	kΩ
R_{FBB}	21.6	kΩ
R_{SENSE}	1	mΩ
R_{DCR}	DNP / Open	kΩ
C_{DCR}	DNP / Open	µF

Figure 5 Schematic Page

2.3 Frequency Detail

The frequency detail page allows plotting combinations of the converter's plant (combined current-control loop and output power stage), control (compensator and voltage feedback loop), and entire control-to-output AC response. Being able to view individual blocks can be helpful when tuning compensator values to optimize the AC response. Individual plots can be shown or hidden using the drop-down menu located in the Frequency Plot Selection field. Figure 6 shows this page with all plots in view, Figure 7 shows a configuration plotting only the Control response.

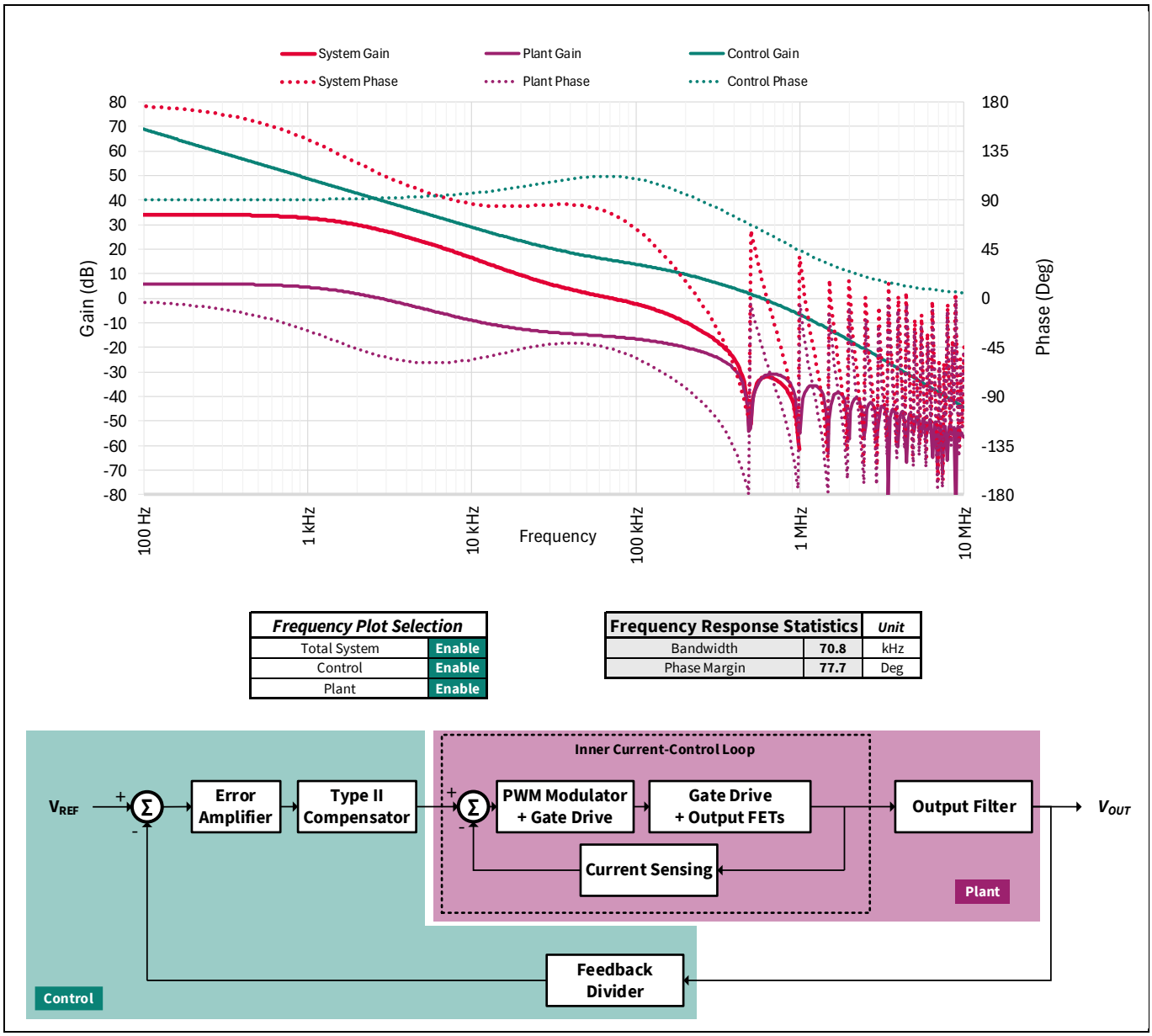


Figure 6 Frequency Detail Page, All Plots Enabled

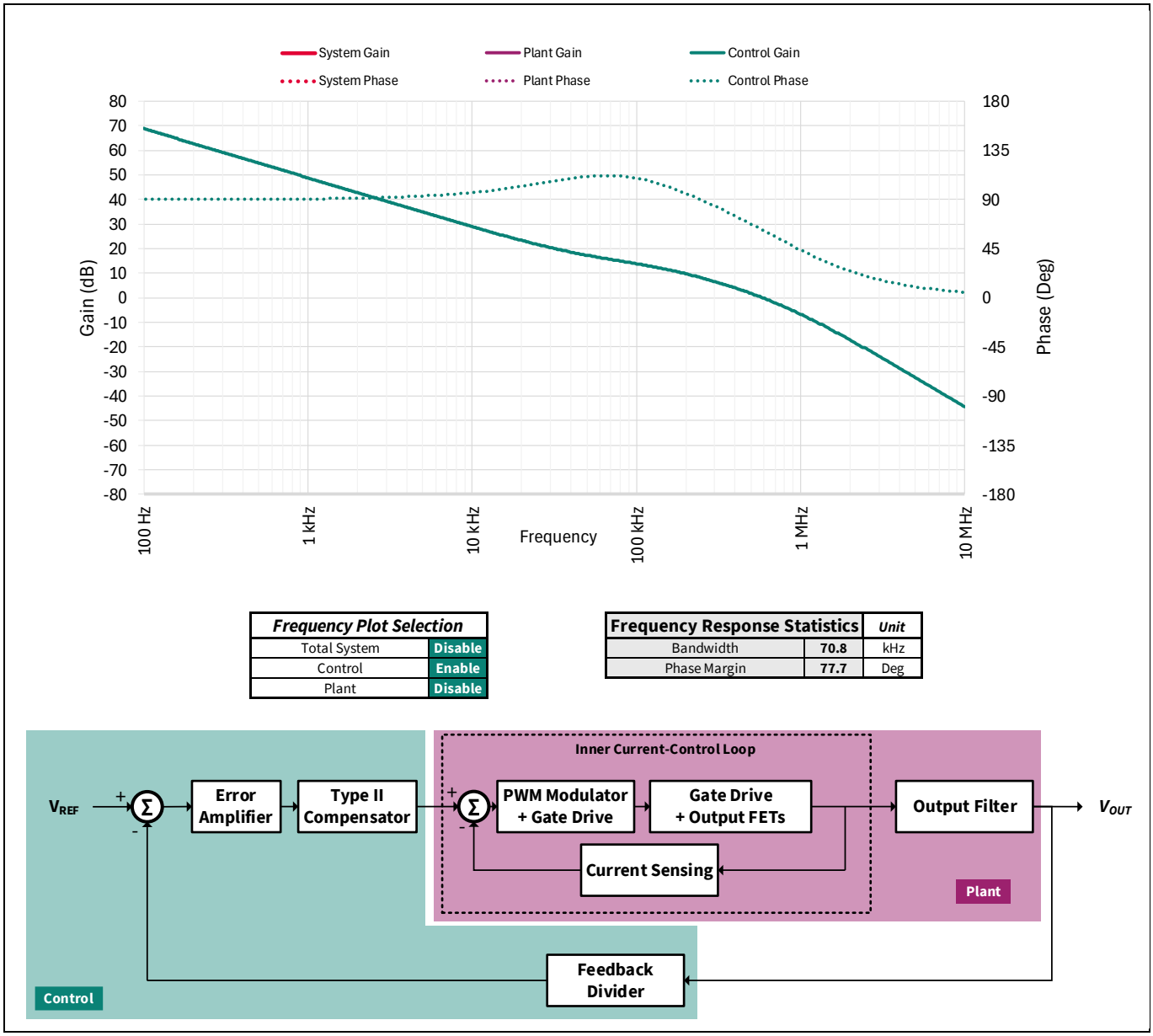


Figure 7 Frequency Detail Page, Only Control Plot Enabled

2.4 Efficiency Detail

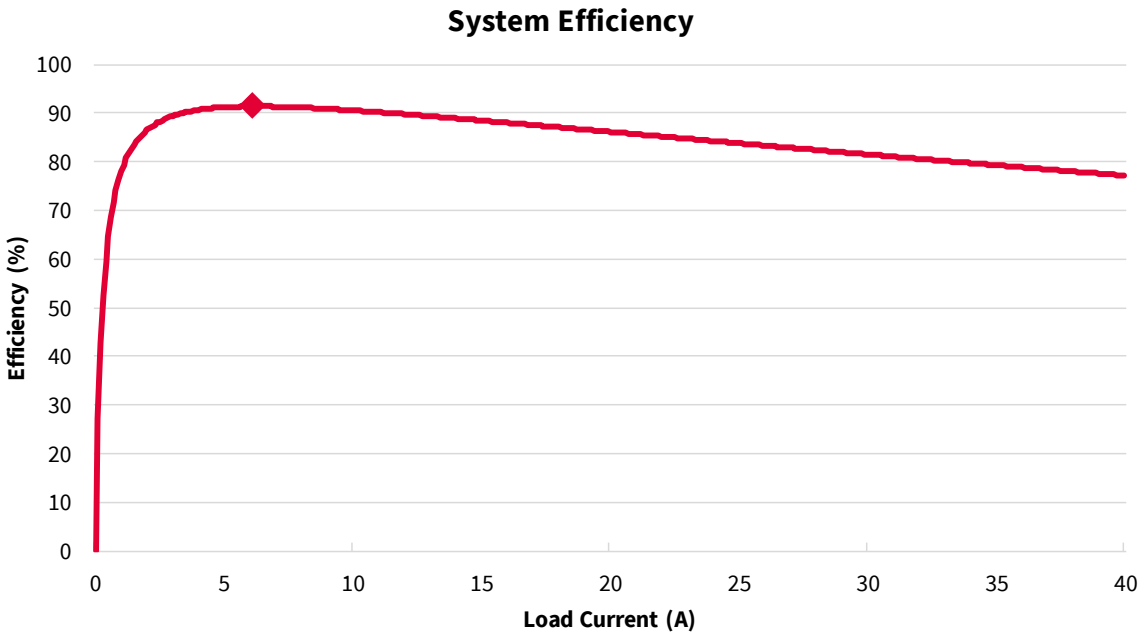
The efficiency detail page shows the efficiency of the configured system swept over the output current range. The losses are broken down into the primary contributions:

- Conduction losses from each FET $R_{DS(ON)}$
- Shunt resistor for current sensing, if populated
- Switching losses from rise / fall time
- Switch-node snubber charge / discharge
- FET output capacitance loss
- IC bias / internal power dissipation
- Gate-drive power consumption
- Inductor DCR losses
- Low-side reverse / diode conduction losses
- Output capacitor ESR losses
- Dummy load resistance present on RIC70849EVAL1 [5]

The minimum load resistance can be removed from the calculation if not populated or unused. The loss breakdown can be shown averaged across load currents, at the peak-efficiency point, or under maximum load. Units can be a normalized percentage of total loss or watts. Figure 8 demonstrates the design example's primary loss contributions under maximum load; the shunt resistance loss is included because DCR sensing is not currently being used.

Dummy Load	Include
Calculate Loss Contributions at	Max Load
Loss Contribution Units	Watts

Peak efficiency (◆)
91.4 %
6.2 A



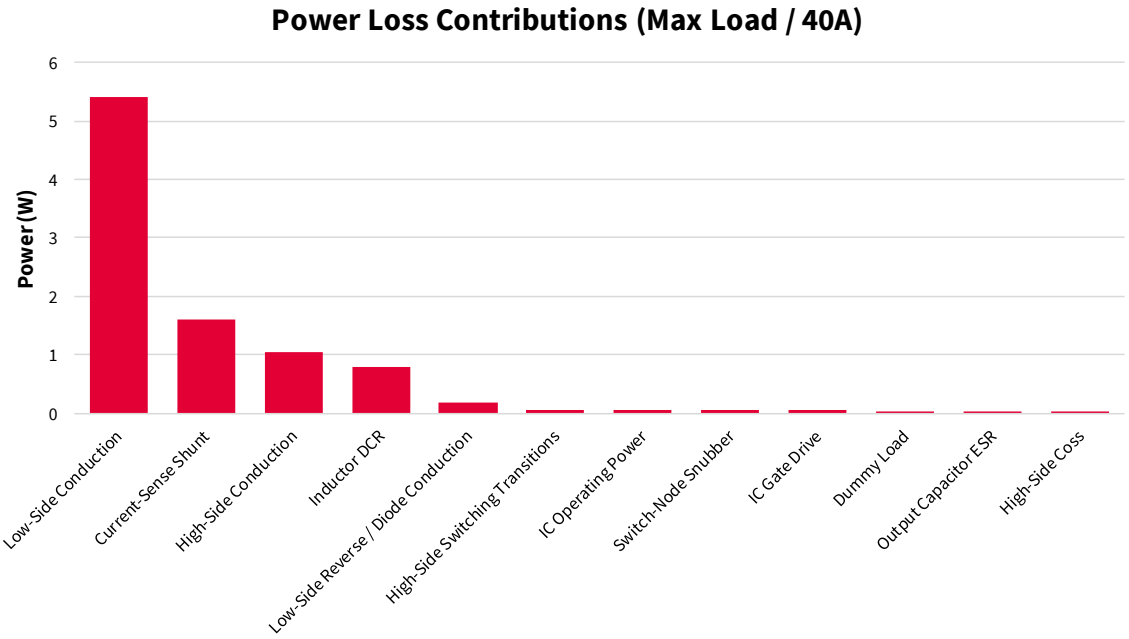


Figure 8 Efficiency Detail Page

3 Major Component Selection

3.1 Inductor Selection

Given an input voltage V_{IN} and output voltage V_{OUT} (V), switching frequency f_{SW} (Hz), and maximum DC output current I_{OUT} (A), with target inductor ripple current Δi (A_{PP}), the minimum required inductance L_{MIN} (H) can be calculated using Equation 1.

$$L_{MIN} = \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{\Delta i \cdot f_{SW} \cdot V_{IN}}$$

Equation 1 Inductor Size Calculation

RIC70849 Design Tool uses inductor ripple current percentage as a provided input to calculate Δi and the required inductance. Typical values for ripple current percentage $\Delta i_{\%}$ are in the range of 20-30%. The inductor ripple current percentage $\Delta i_{\%}$ is related to Δi (A_{PP}) and I_{OUT} (A) by Equation 2.

$$\Delta i_{\%} = \frac{\Delta i}{I_{OUT}} \cdot 100$$

Equation 2 Inductor Ripple Current Percentage

3.2 Capacitor Selection

3.2.1 Output Capacitor

The primary requirements for sizing the output capacitors are output voltage ripple, transient performance, and capacitor RMS current rating.

There are two main contributions to the total peak-to-peak output voltage ripple:

- Steady-state capacitive ripple, due to the charge and discharge of output capacitors
- ESR ripple, due to the inductor's ripple current and ESR of the output capacitance

The total peak-to-peak output voltage ripple ΔV_{OUT} (V_{PP}) can be approximated with a root-sum-square of these contributions, using Equation 3.

$$\Delta V_{OUT} = \sqrt{\Delta V_{CAP}^2 + \Delta V_{ESR}^2}$$

Equation 3 Total Ripple

Given the required capacitive steady-state ripple ΔV_{CAP} (V_{pp}), switching frequency f_{SW} (Hz), and inductor ripple current Δi (A_{PP}), required output capacitance C_{out} (F) can be found using Equation 4.

$$C_{OUT} = \frac{\Delta i}{8 \cdot f_{SW} \cdot \Delta V_{CAP}}$$

Equation 4 Capacitive Ripple Contribution

ESR ripple can be calculated using inductor ripple current (A_{pp}) and output capacitor ESR (Ω) in Equation 5. After selecting output capacitors and determining ESR ripple, it may be necessary to re-evaluate the output capacitor requirement to achieve target ΔV_{OUT} (Equation 3).

$$\Delta V_{ESR} = \Delta i \cdot R_{ESR}$$

Equation 5 ESR Ripple Contribution

Finally, transient capacitance requirement can be found. There are multiple factors that impact the transient performance of the converter:

- Output capacitance, which determines the immediate output voltage change during a transient load, before the control loop has reacted
- Bandwidth (f_{BW}), which determines how quickly the control loop can react to a transient event
- Power stage / inductor, which determines the absolute maximum current slew rates physically possible for the converter to provide

In most PoL applications, bandwidth is the primary limiting factor to the transient performance of the converter. Using the bandwidth of the converter f_{BW} (Hz), allowable voltage deviation ΔV_{LOAD} (V), and transient load current step requirement ΔI_{LOAD} (A), the transient capacitance requirement for a bandwidth-limited system can be found using Equation 6. Further information on bandwidth and AC response can be found in Section 4. Typically, the bandwidth f_{BW} should be set to approximately 1/10 of the switching frequency, f_{SW}.

$$C_{TRAN} = \frac{\Delta I_{LOAD}}{2 \cdot \pi \cdot f_{BW} \cdot \Delta V_{LOAD}}$$

Equation 6 Transient Capacitance Requirement, Bandwidth Limitation

If the power stage is the limiting factor, the inductor is unable to provide a current slew rate to accommodate the transient demand. In this case, the transient capacitance requirement can be found using Equation 7, with the allowable voltage deviation ΔV_{LOAD} (V), transient load current step requirement ΔI_{LOAD} (A), inductor value L (H), and output voltage V_{OUT} (V).

$$C_{TRAN} = \frac{\Delta I_{LOAD}^2 \cdot L}{2 \cdot \Delta V_{LOAD} \cdot V_{OUT}}$$

Equation 7 Transient Capacitance Requirement, Power Stage Limitation

The greater result of Equation 6 and Equation 7 should be used as the final transient capacitance calculation.

Total output capacitance should be selected from the higher of the ripple or transient requirements. In most cases, transient requirements will far exceed ripple capacitance requirements. Capacitors should be sized to support the total RMS current, which can be calculated using Equation 8 and the inductor ripple current Δi (A_{PP}).

$$i_{C_{OUT},RMS} = \frac{\Delta i}{\sqrt{12}}$$

Equation 8 Output Capacitor RMS Current

3.2.2 Input Capacitor

The input capacitance requirement can be found using Equation 9 with the target input voltage ripple Δ V_{IN} (V), maximum DC output current I_{OUT} (A), approximate duty cycle using input and output voltages V_{IN}, V_{OUT} (V), and the switching frequency of the converter f_{SW} (Hz).

$$C_{IN} = \frac{\frac{V_{OUT}}{V_{IN}} \cdot I_{OUT}}{\Delta V_{IN} \cdot f_{SW}}$$

Equation 9 Input Capacitance Requirement

The RMS current for the input capacitance can be found using Equation 10 using the duty cycle of the converter found using input and output voltages V_{IN}, V_{OUT} (V), and maximum DC output current I_{OUT} (A).

$$i_{C_{IN},RMS} = I_{OUT} \cdot \sqrt{\frac{V_{OUT}}{V_{IN}}}$$

Equation 10 Input Capacitor RMS Current

3.3 Configuration Options

3.3.1 Switching Frequency

RIC70849 has an internal oscillator with configurable frequency from 100kHz to 2MHz. Equation 11 solves for the R_{RT} configuration resistor (Ω) given the desired switching frequency f_{SW} (Hz). [6]

$$R_{RT} = \frac{\frac{1}{f_{SW}} - 76 \cdot 10^{-9} s}{66.12 \cdot 10^{-12} \frac{s}{\Omega}}$$

Equation 11 Frequency Configuration

3.3.2 Feedback Resistors

The feedback divider consists of two resistors in series (Figure 9), and resistance is selected based on the output voltage relative to the internal 600mV reference. Equation 12 shows the resistor divider calculation, using V_{OUT}(V), and top / bottom feedback resistance R_{FB} (Ω).

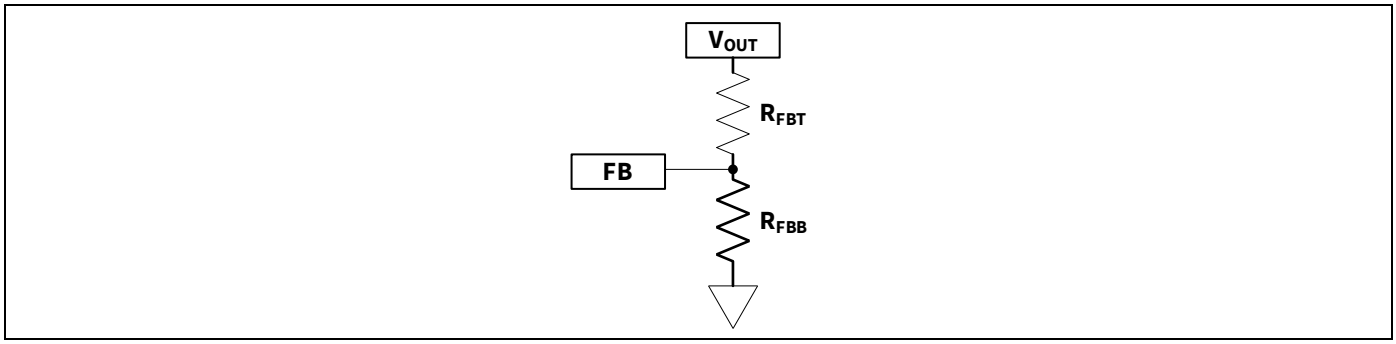


Figure 9 Feedback Divider Schematic

$$0.6V = V_{OUT} \cdot \frac{R_{FBB}}{R_{FBB} + R_{FBT}}$$

Equation 12 Feedback Divider Equation

The lower feedback resistor is set first and should be set to a value less than 25kΩ if LLR is being used. LLR works to adjust output voltage through an injected current from the feedback pin. This feature will not work properly if resistance is outside of this range and could cause instability. See RIC70849 Datasheet [6] and Section 3.3.4 for more information on LLR.

For all design cases, lower resistances should be used in the feedback divider when possible. Since the feedback trace to RIC70849 from the feedback divider in addition to the FB pin on RIC70849 both contain non-trivial parasitic capacitance, this creates an RC circuit with a time constant. In turn, a pole is added to the frequency response of the converter, where the total feedback resistance is inversely related to the pole's frequency. Using high resistances shifts this pole's frequency lower, which can influence gain and phase response near the crossover frequency. See Section 6.2.2 for details on feedback-node parasitics.

3.3.3 Current Sensing

RIC70849 can be used with two different sensing methods. A shunt resistor can be used to directly measure current through the inductor, or DCR sensing can be used to measure the current through the inductor's DC resistance. If DCR sensing is used, the shunt resistor R_{SENSE} is removed (the inductor's output is connected directly to the output capacitor bank) and an RC network is added across the inductor. Figure 10 depicts the current sensing implementation options.

A series sense resistor R_{SENSE} reduces the converter's efficiency slightly but can provide more consistent sensing performance over a temperature range compared to DCR. DCR removes the series resistance and therefore has reduced power loss, but the inductor's DCR can vary significantly with temperature and influence the sensed waveform. RIC70849EVAL1 is designed to allow evaluation of both sensing methods [5].

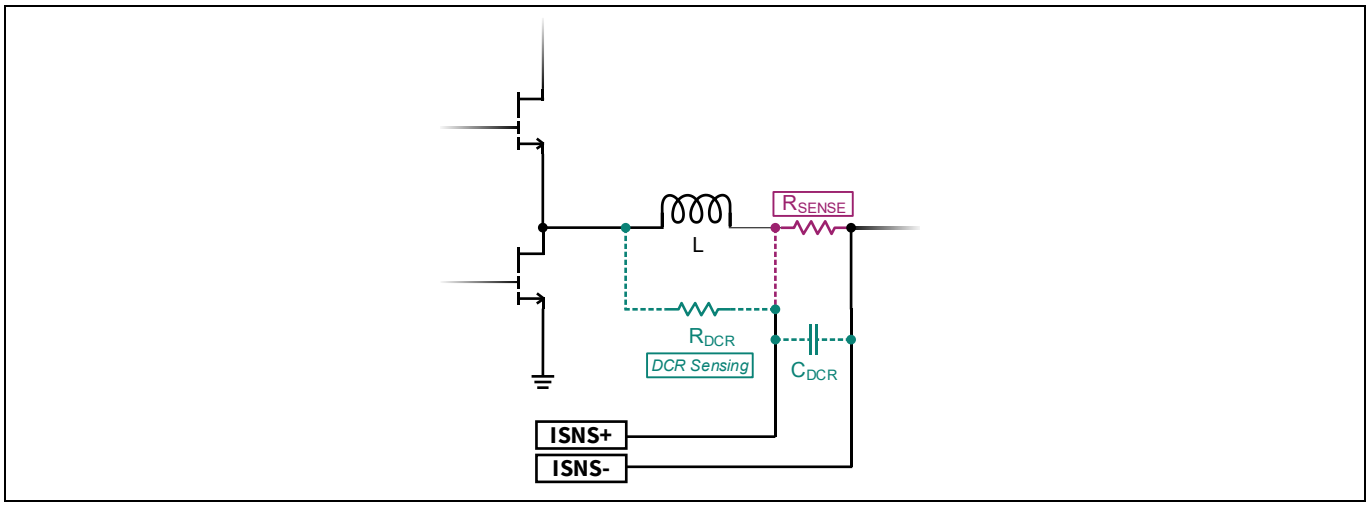


Figure 10 ISNS Configurations

If DCR sensing is used, the RC network will create a voltage across the ISNS pins proportional to the current through the inductor. To calculate the DCR sensing network resistor, the time constant of resistor R_{DCR} (Ω) and capacitor C_{DCR} (F) must be equal to the time constant of the inductor L (H) with DC resistance DCR (Ω). See Equation 13. R_{DCR} should be set between 1kΩ-10kΩ.

$$R_{DCR} \cdot C_{DCR} = \frac{L}{DCR}$$

Equation 13 DCR Network Calculation

The ramp voltage present at the ISNS pins from the current sense method directly influences the inner current-control loop's response. Greater voltage magnitude (from a larger shunt resistance or DCR) will increase the current-control loop's gain. The sense resistor R_{SENSE} can be calculated using the desired differential ISNS voltage magnitude Equation 14. When DCR sensing is used, the voltage present on the ISNS pins can be calculated with Equation 15. Current sensing should be implemented such that ISNS pins do not exceed the maximum datasheet voltages. A current-sense shunt resistance or inductor DCR around 0.5mΩ is suggested, RIC70849EVAL1 is configured with 1mΩ shunt resistor sensing by default [5] [6].

$$R_{SENSE} = \frac{V_{ISNS}}{i_L}$$

Equation 14 ISNS Voltage, Sense Resistor

$$V_{ISNS} = i_L \cdot DCR$$

Equation 15 ISNS Voltage, DCR Sensing

3.3.4 Bootstrap Circuit

RIC70849 incorporates an integrated bootstrap diode for biasing the high-side FET driver to the switch node of the converter. For proper operation, the bootstrap circuit requires a capacitor C_{BOOT} of at least 100nF between the BOOT and SW pins, which is used to charge the gate of the high-side FET during on-time. 100nF is considered the absolute minimum C_{BOOT}. If the FET used has a large gate charge Q_G, a larger capacitor should be used instead which can be estimated as 10 times the gate capacitance. C_{BOOT} (F) can be found using the gate charge of the high-side FET Q_G (C) divided by drive voltage (5V) in Equation 16.

$$C_{BOOT} = 10 \cdot \frac{Q_G}{5V}$$

Equation 16 Bootstrap Capacitor Requirement

3.3.5 LLR Configuration

If LLR is desired to reduce overshoot / undershoot in transient events, the load line configuration resistor R_{LLR} can be set using Equation 17. Given the chosen current-sense resistor R_{SENSE} (Ω), the injected current into the upper feedback resistor R_{FBT} (Ω) is set to produce the output voltage setpoint droop ΔV_{LLR} (V) at maximum load current I_{OUT} (A). If DCR sensing is implemented instead of a shunt resistor, R_{SENSE} should be replaced with the inductor DCR value (Ω). More information about LLR can be found in RIC70849 Datasheet [6].

$$R_{LLR} = \frac{6.65 \cdot R_{SENSE} \cdot I_{OUT} \cdot R_{FBT}}{16 \cdot \Delta V_{LLR}}$$

Equation 17 LLR Configuration

3.4 Soft-Start Time

To set the soft-start time, the soft-start capacitor C_{SS} (F) is calculated using the desired soft-start time (s), and the IC's current source / voltage reference at the SS pin in Equation 18. The numbers provided reflect the 10 µA current source and 600mV reference in RIC70849 [6].

$$C_{SS} = \frac{t_{SS} \cdot 10 \cdot 10^{-6}\ A}{0.6\ V}$$

Equation 18 Soft-Start Calculation

3.5 Overcurrent Protection

The OCP resistor R_{OCP} (Ω) is configured using the nominal internal OCP threshold voltage $V_{OCP} = 1.215V$, internal current sense amplifier gain (333µS) with 30µA offset, and desired overcurrent threshold I_{OCP} (A). Equation 19 calculates the value of R_{OCP} for the desired threshold. [6]

$$R_{OCP} = \frac{1.215\ V}{333 \cdot 10^{-6}\ S \cdot I_{OCP} \cdot R_{SENSE} + 30 \cdot 10^{-6}\ A}$$

Equation 19 OCP Configuration

3.6 Slope Compensation

Slope compensation on the RIC70849 is used to reject sensed noise on the current sense pins (I_{SNS+} and I_{SNS-}) and to prevent subharmonic oscillations observed on the inductor current waveform at duty cycles approaching 50%.

In peak current mode control theory [1], slope compensation is only required with duty cycles of 50% and higher. However, in real-world designs, subharmonic oscillations on the inductor current waveform will begin to be observed as the converter's duty cycle reaches a value that is slightly under, slightly over, or equal to 50%, and increased slope compensation may be required to stabilize these oscillations.

Additionally, in real PCB applications, a common challenge faced is noise coupling into the current sense signal. As such, it can be beneficial to add slope compensation even when the duty cycle does not approach 50%. This slope compensation helps reject the sensed current noise with the injection of a clean ramp signal into the current sense signal path.

The Design Tool recommends a minimum amount of slope compensation equal to two times the magnitude of the sensed inductor off-slope S_F regardless of the duty cycle. In cases where the off-slope S_F is small enough to cause the recommended R_{SLP} to exceed 500kΩ, the R_{SLP} recommended value will be capped at 500kΩ to ensure a minimum amount of slope compensation for current sense noise reduction.

The recommended slope compensation resistor R_{SLP} is determined using the current sense resistor R_{SENSE} and inductor off-slope S_F. Equation 20 calculates the recommended value of R_{SLP}.

$$R_{SLP} = \frac{3.6 \cdot 10^{9}}{2 \cdot S_F \cdot R_{SENSE}}$$

Equation 20 R_{SLP} Calculation

4 Frequency Response

4.1 Overview

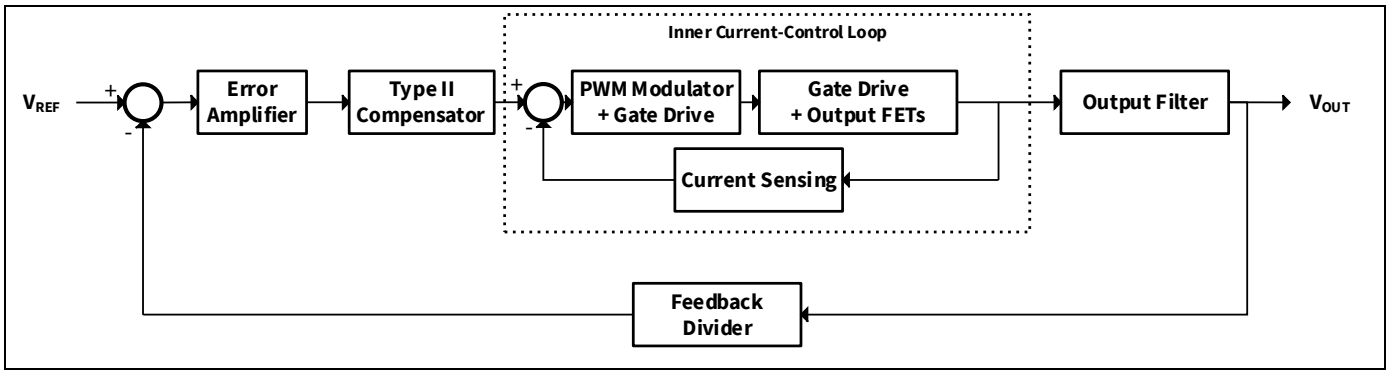


Figure 11 Simplified Block Diagram

RIC70849 uses a peak-current-mode-control method. This section will describe how to compensate this control scheme in a PoL buck converter with RIC70849. More details on AC response and the complete derivation of the numerical model used in RIC70849 Design Tool can be found in the Appendix, Section 6. Further information about peak-current-mode-control can be found in references [1] and [2].

4.2 Loop Compensation

The main points of interest of a buck converter's AC-response performance are crossover frequency (f_C) and phase margin. These parameters dictate the responsiveness to transient loads and overall system stability. Typically, the crossover frequency should be set at approximately 1/10 the switching frequency, f_{SW}.

To set crossover frequency and adjust phase response, RIC70849 uses a Type II compensation network applied to the Operational Transconductance Amplifier (OTA) output on the COMP pin, drawn in Figure 12. This network produces a pole at the origin, high-frequency pole and a lower-frequency zero. This creates a phase boost between the zero and pole location that is used to improve phase margin of the converter. A bode plot of a typical Type 2 compensator is depicted in Figure 13 with annotated high-frequency pole (f_P) and zero frequency (f_z).

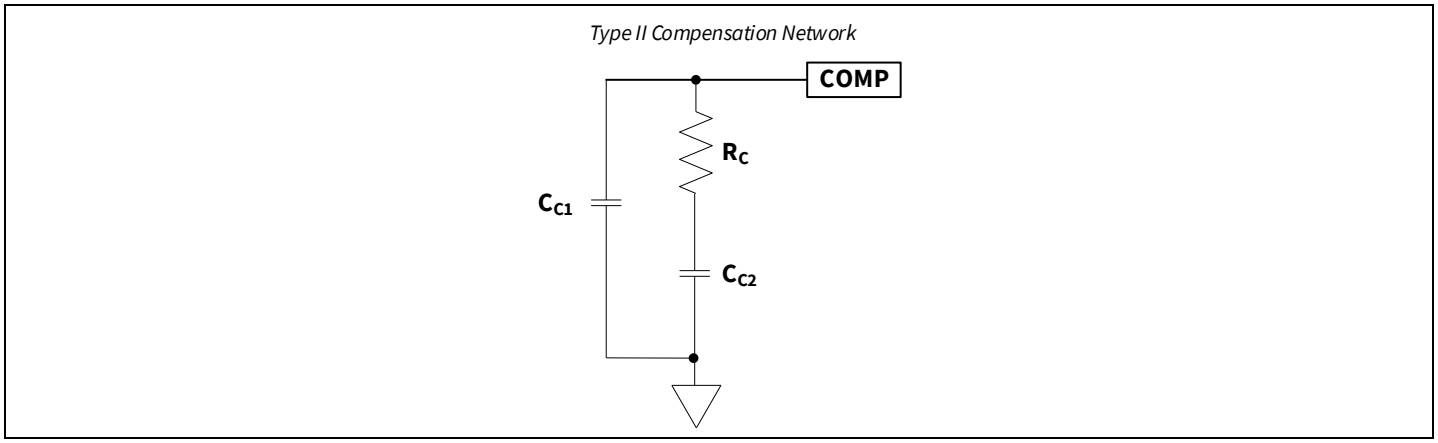


Figure 12 Type II Compensator Schematic

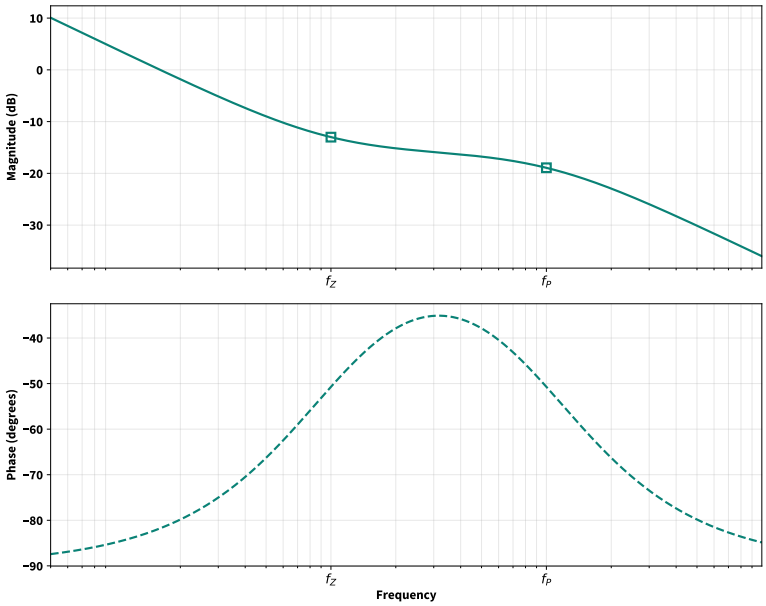


Figure 13 Standard Type II Compensator Bode Plot

The frequency of the pole f_P and zero f_Z (Hz) can be found using Equation 21 and Equation 22 respectively, given R_C (Ω), C_{C1} (F), and C_{C2} (F).

$$f_P = \frac{C_{C1} + C_{C2}}{2 \cdot \pi \cdot R_C \cdot C_{C1} \cdot C_{C2}}$$

Equation 21 Compensator Pole Frequency

$$f_Z = \frac{1}{2 \cdot \pi \cdot R_C \cdot C_{C2}}$$

Equation 22 Compensator Zero Frequency

In most implementations, f_P should be placed above f_C to increase high-frequency attenuation, and f_Z should be placed below f_C to increase phase near crossover (contributing to positive phase margin). Further loop compensation methodology can be found in reference [3] and more numerical background can be found in the Appendix, Section 6.

5 Efficiency Calculations

5.1 High-Side FET Losses

Conduction losses encompass the power dissipated within the transistor's internal resistance during the respective on-time. Using RMS current through the FET, this can be calculated given a simplified duty cycle with V_{OUT} and V_{IN} (V), on-resistance of the FET $R_{DS,ON}$ (Ω), DC load current I_{OUT} (A), and inductor ripple current Δi (A_{PP}). (Equation 23)

$$P_{C(HS)} = \left(\frac{\Delta i^2}{12} + I_{OUT}^2\right) \cdot R_{DS,ON(HS)} \cdot \frac{V_{OUT}}{V_{IN}}$$

Equation 23 Conduction Power Calculation, High-Side FET

Switching losses occur during the Miller plateau region, when there is non-trivial V_{DS} and I_{DS} overlap. The rise and fall times (s) during which these losses occur can be found using the high-side FET Miller gate-drain charge Q_{GD} (C), gate-source plateau voltage V_{MILLER} (V), gate resistance R_G (Ω), SRC / SNK pin resistors R_{SRC}, R_{SNK} (Ω), and drive voltage V_{DRV} (V). (Equation 24)

$$\tau_R = \frac{Q_{GD}}{V_{DRV} - V_{MILLER}} \cdot (R_G + R_{SRC}) \qquad \tau_F = \frac{Q_{GD}}{V_{MILLER}} \cdot (R_G + R_{SNK})$$

Equation 24 Rise and Fall Time

Power loss (W) from switching can be found using Equation 25 with switching frequency f_{SW} (Hz), DC output current I_{OUT} (A), and inductor ripple current Δi (A_{PP}). These switching losses occur primarily on the high-side FET due to high V_{DS} during turn-on and turn-off.

$$P_{SW(HS)} = \frac{V_{IN}}{2} \cdot f_{SW} \cdot \left(\tau_R \cdot \left(I_{OUT} - \frac{\Delta i}{2}\right) + \tau_F \cdot \left(I_{OUT} + \frac{\Delta i}{2}\right)\right)$$

Equation 25 Switching Loss Power Calculation

The output capacitance of the high-side FET also incurs loss in the system. As the switch node cycles high and low, the output capacitance is charged to V_{IN} - V_{OUT}. Using the switch output capacitance C_{OSS} (F), input and output voltages V_{IN}, V_{OUT} (V), and switching frequency f_{SW} (Hz) the power loss (W) due to this charge / discharge cycle can be calculated in Equation 26.

$$P_{C_{OSS}(HS)} = C_{OSS} \cdot (V_{IN} - V_{OUT})^2 \cdot f_{SW}$$

Equation 26 Output Capacitance Power Calculation

5.2 Low-Side FET Losses

Like the conduction losses in the high-side FET, the conduction loss in the low-side FET can be calculated using RMS current through the FET, a simplified duty cycle for the FET using V_{OUT} and V_{IN} (V), on-resistance of the FET $R_{DS,ON}$ (Ω), DC load current I_{OUT} (A), and inductor ripple current Δi (A_{PP}). (Equation 27)

$$P_{C(LS)} = \left(\frac{\Delta i^2}{12} + I_{OUT}^2\right) \cdot R_{DS,ON(LS)} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Equation 27 Conduction Power Calculation, Low-Side FET

In the deadtime period when neither the high or low-side switches are on, there are losses incurred due to low-side GaN FET reverse conduction (third quadrant operation) or MOSFET body diode conduction where the inductor current flows back through the low-side FET. Given the reverse conduction or body diode forward voltage drop of the FET V_{SD} (V), deadtime for each transition τ_{BD} (s), output current I_{OUT} (A), and switching frequency f_{SW} (Hz), the power loss (W) can be calculated using Equation 28.

$$P_{RC(LS)} = 2 \cdot V_{SD} \cdot I_{OUT} \cdot f_{SW} \cdot \tau_{BD}$$

Equation 28 Reverse / Diode Conduction Power Calculation

On RIC70849EVAL1, there is a discrete Schottky diode from PGND to the switch node that has a lower forward voltage intended to conduct the freewheeling current more efficiently [5]. In this case, V_{SD} should be substituted with the Schottky diode's forward voltage for the most accurate results. RIC70849 has built-in deadtime of approximately 8ns on both rising and falling edges.

5.3 Gate Drive Loss

As RIC70849 turns on and off the FETs in the power stage, charging and discharging the gates adds further power loss to the system. This power loss (W) can be found using the gate charge of each FET Q_G (C), drive voltage V_{DRV} (V), and switching frequency f_{SW} (Hz) in Equation 29.

$$P_{GD} = \left(Q_{G(HS)} + Q_{G(LS)}\right) \cdot V_{DRV} \cdot f_{SW}$$

Equation 29 Gate Drive Power Calculation

5.4 Shunt Resistance Loss

If a shunt resistor is used for current sense measurement, the resistor will incur losses and influence the efficiency of the converter. This resistor is exposed to the total RMS current through the inductor, which includes the DC output current I_{OUT} (A) and the inductor ripple current Δi (A_{PP}). Using Equation 30, the power loss (W) can be found given the sense resistance R_{SENSE} (Ω).

$$P_{R_{SENSE}} = \left(I_{OUT}^2 + \frac{\Delta i^2}{12}\right) \cdot R_{SENSE}$$

Equation 30 Shunt Power Calculation

5.5 Inductor DCR Loss

The output current through the DC resistance of the inductor causes power loss, similarly to the series shunt resistance. Since the DCR is in series with the inductor, the inductor's DCR power loss (W) can be calculated using the same technique as for a shunt resistor. (Equation 31)

$$P_{DCR} = \left(I_{OUT}^2 + \frac{\Delta i^2}{12}\right) \cdot DCR$$

Equation 31 Inductor DCR Power Calculation

In the typical RIC70849 POL buck converter application, DCR loss comprises most of the inductor's total loss and allows an accurate starting estimate of the converter's efficiency.

5.6 ESR Loss

The ESR of output capacitors causes power loss due to the inductor's ripple current. Equation 32 can be used to estimate this power loss (W) given the inductor ripple current Δi (A_{PP}) and the equivalent series resistance R_{ESR} (Ω).

$$P_{ESR} = \frac{(\Delta i)^2}{12} \cdot R_{ESR}$$

Equation 32 ESR Power Calculation

5.7 IC Losses

Under non-switching bias conditions, RIC70849 consumes approximately I_{IC} = 5mA. Thus, there will be a fixed power loss (W) due to the IC's internal circuitry, which can be calculated given the IC input voltage V_{IN} (V). (Equation 33)

$$P_{IC} = I_{IC} \cdot V_{IN}$$

Equation 33 IC Power Calculation

5.8 Snubber Losses

The R-C switch-node snubber circuit on RIC70849EVAL1 [5] dissipates power in the resistor during switching transitions as the capacitance charges and discharges. This loss can be calculated using Equation 34, given the input voltage V_{IN} (V), switching frequency f_{sw} (Hz), and snubber capacitance C_{SNUB} (F).

$$P_{SNUB} = f_{SW} \cdot V_{IN}^2 \cdot C_{SNUB}$$

Equation 34 Snubber Power Calculation

6 Appendix – Frequency Response Detail

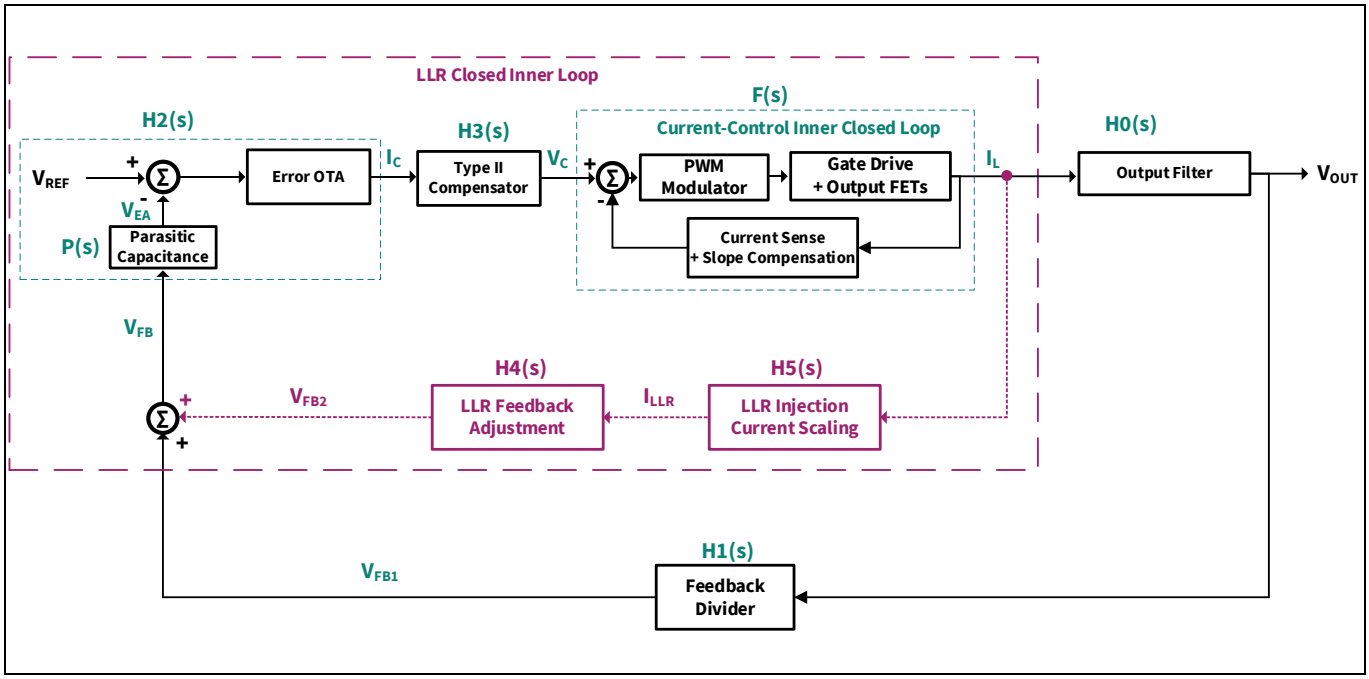


Figure 14 Frequency Response Block Diagram

6.1 System Breakdown

To analyze RIC70849's frequency response numerically, it is broken into transfer functions according to the functional blocks of the converter depicted in Figure 14. These functions are summarized in Table 2.

Table 2 System Transfer Functions

Abbreviation	$\frac{\text{Output}}{\text{Input}}$	Description	Section
H1(s)	$\frac{V_{FB1}}{V_{OUT}}$	Feedback voltage divider	6.2.1
P(s)	$\frac{V_{EA}}{V_{FB}}$	Parasitic input impedance on feedback	6.2.2
H2(s)	$\frac{I_C}{V_{EA}}$	Error OTA	6.2.2
H3(s)	$\frac{V_C}{I_C}$	Type 2 Compensator	6.2.3
F(s)	$\frac{I_L}{V_C}$	Inner current-control loop	6.2.4
H0(s)	$\frac{V_{OUT}}{V_C}$	Power stage filter (inductor / output capacitor)	6.2.5
H5(s)	$\frac{I_{LLR}}{I_L}$	Load-line current injection scaling	6.2.6
H4(s)	$\frac{V_{FB2}}{I_{LLR}}$	Feedback voltage contribution from LLR	6.2.7

6.2 Transfer Functions

6.2.1 H1(s)

H1 represents the simple voltage divider from V_{OUT} to V_{FB1} and is summarized in Equation 35. Notation “FB1” is used because the input to the OTA has multiple contributions, coming from this feedback divider as well as LLR injection if LLR is enabled. See H4(s), section 6.2.7. There are no frequency-dependent contributions from H1(s), it is only a fixed gain factor. R_{FBB} represents the bottom feedback resistor and R_{FBT} represents the top feedback resistor (Ω).

$$H1(s) = \frac{R_{FBB}}{R_{FBB} + R_{FBT}}$$

Equation 35 H1(s)

6.2.2 H2(s)

H2(s) represents the OTA error amplifier within RIC70849. The feedback voltage from the feedback divider H1(s) (V_{FB1}), with a summed contribution from LLR if enabled (V_{FB2}), is fed to the inverting input of the error amplifier. The reference voltage, V_{REF}, is at the non-inverting input. In the small-signal response, the reference voltage can be ignored

Notably, the input to the feedback divider has parasitic frequency response that can influence crossover frequency and phase margin. This is modeled as a separate transfer function P(s), representing the parasitic capacitances within RIC70849 and the feedback trace, creating an RC circuit with the feedback resistors. On RIC70849EVAL1, this was experimentally estimated to be 10pF for the device input capacitance with 22pF of trace capacitance. C_P (F) represents the total parasitic capacitance (32pF) affecting the feedback node. P(s) is defined in Equation 36 using C_P and the top and bottom feedback resistors R_{FB} (Ω).

$$P(s) = \frac{1}{1 + s \cdot \frac{C_P \cdot R_{FBT} \cdot R_{FBB}}{R_{FBT} + R_{FBB}}}$$

Equation 36 Parasitics from Feedback Node

The error OTA has an additional estimated 10pF parasitic capacitance present at the output (COMP pin), but this was included in H3(s) for simplicity as it is parallel to the high-frequency capacitor C_{C1}. The OTA’s GBW is also modelled using the output resistance in H3. Having separately considered the input and output parasitics, the remainder of the OTA can be represented as a fixed gain factor of -g_M, the transconductance of the amplifier (found in the RIC70849 Datasheet [6]). Therefore, the total transfer function H2(s) is the product of P(s) and -g_M (S). (Equation 37)

$$H2(s) = \frac{-g_M}{1 + s\frac{C_P \cdot R_{FBT} \cdot R_{FBB}}{R_{FBB} + R_{FBT}}}$$

Equation 37 H2(s)

6.2.3 H3(s)

H3(s) models the Type 2 compensator, and OTA output non-idealities (GBW, parasitic capacitance). The compensation network is composed of a series resistor-capacitor (defined as R_C and C_{C2}) in parallel with a high-frequency capacitor C_{C1} depicted in Figure 12.

Since this transfer function represents the relationship between OTA output current and control voltage, it is simply the total impedance of the compensator and associated parasitics. Notably, this function incorporates the output parasitic capacitance of the OTA C_{OTA} (F) in parallel with C_{C1} (F), the high-frequency capacitor. Additionally, the output resistance R_{OUT} (Ω) of the error amplifier is included in parallel with the entire compensation network. R_C is represented in the transfer function in Ω. (Equation 38)

$$H3(s) = R_{OUT} \cdot \frac{1 + sR_CC_{C2}}{1 + s(R_CC_{C2} + R_{OUT}(C_{C1} + C_{OTA}) + R_{OUT}C_{C2}) + s^2R_{OUT}(C_{C1} + C_{OTA})R_CC_{C2}}$$

Equation 38 H3(s)

6.2.4 F(s)

F(s) encompasses the entire inner current-control loop in RIC70849. This is calculated using the full exponential model for peak-current-mode control topologies. For more information about the derivation of this numerical model, see reference [1]. This model uses the inductor ramp slopes S_N (Equation 39) and S_F (Equation 40), with injected slope S_E to model the inner loop behavior. To improve slope accuracy, FET voltage drops at load current are included in the ramp slopes. R_{DS} represents the on resistance of the High and Low side switches (Ω) and ramps are calculated given the DC output current I_{OUT} (A) and inductance L (H). All slopes are measured in A/s.

$$S_N = \frac{V_{IN} - (R_{DSH} \cdot I_O) - V_{OUT}}{L}$$

Equation 39 On-Slope

$$S_F = \frac{V_{OUT} + (R_{DSL} \cdot I_O)}{L}$$

Equation 40 Off-slope

On RIC70849, the injected slope S_E (Equation 41) is set using the sense resistor R_{SENSE} (or the inductor DCR, if DCR sensing is used) (Ω) and slope compensation configuration resistor R_{SLP} (Ω).

$$S_E = \frac{3.6 \cdot 10^9}{R_{SENSE} \cdot R_{SLP}}$$

Equation 41 Injected Slope Compensation

Alpha (α) is used as a metric of inner-loop stability. Alpha values greater than 1 represent unstable systems that could encounter subharmonic oscillations and require adjusted slope compensation. This quantity can be calculated using ramp slopes S (A/s) and does not have units. (Equation 42)

$$\alpha = \frac{S_F - S_E}{S_N + S_E}$$

Equation 42 Alpha Calculation

Given the current sense resistor R_{SENSE} (or the inductor DCR, if DCR sensing is used) (Ω), the current sense amplifier gain A_{ISNS} (V/V), switching frequency f_{SW} (Hz), and α calculated previously, F(s) can be modeled. This is calculated using the full exponential sample-and-hold model derived in [1] (Equation 43).

$$F(s) = \frac{1}{R_{SENSE} \cdot A_{ISNS}} \cdot \frac{(1+\alpha) \cdot f_{SW}}{s} \cdot \frac{e^{\frac{s}{f_{SW}}} - 1}{e^{\frac{s}{f_{SW}}} + \alpha}$$

Equation 43 F(s)

6.2.5 H0(s)

H0(s) represents the L-C filter formed by the inductor and capacitor at the output of the switch-node. Since peak-current-mode control schemes mask the second-order behaviors of the typical LC filter, the output voltage given inductor current is simply the impedance of the output capacitors and load. Given an inductor impedance Z_1 and capacitor/load parallel impedance Z_2, it can be derived that the transfer function from inductor current to output voltage is simply Z_2. (Equation 44)

$$V_{IN} = I_L \cdot (Z_1 + Z_2) \quad V_{OUT} = \frac{Z_2}{Z_1 + Z_2} \cdot V_{IN} \quad Z_2 = \frac{V_{OUT}}{I_L}$$

Equation 44 Impedance Derivation

The equivalent load resistance R_{LOAD} (Ω) can be found using output voltage V_{OUT} (V) and maximum DC current I_{OUT} (A) in Equation 45.

$$R_{LOAD} = \frac{V_{OUT}}{I_{OUT}}$$

Equation 45 Equivalent Load Resistance

Given R_{LOAD}, output capacitance C (F), and output capacitor ESR R_{ESR} (Ω), the total impedance can be found using Equation 46.

$$H0(s) = R_{LOAD} \cdot \frac{1 + sCR_{ESR}}{1 + sC(R_{LOAD} + R_{ESR})}$$

Equation 46 H0(s)

6.2.6 H5(s)

H5(s) is the scaling factor from the inductor current I_L to the injected current at the feedback pin I_{LLR} when LLR is enabled. R_{SENSE} and R_{LLR} (Ω) are used to calculate this scaling internally in RIC70849. This equation can also be found in the RIC70849 Datasheet [6] (Equation 47).

$$H5(s) = \frac{6.65 \cdot R_{SENSE}}{16 \cdot R_{LLR}}$$

Equation 47 H5(s)

6.2.7 H4(s)

H4(s) represents the shift in small-signal feedback voltage given the injected LLR current at the feedback pin. The injected current flows through the parallel combination of R_{FBB} and R_{FBT} (Ω). (Equation 48)

$$H4(s) = \frac{R_{FBB}R_{FBT}}{R_{FBB} + R_{FBT}}$$

Equation 48 H4(s)

6.3 System

The overall system (control to output) response can be found by considering two possible operation modes, with and without LLR active. Without LLR, the system is a sequential series of transfer functions, where the output of one transfer function is the input to the next. The LLR functions are ignored, because the injected LLR current is zero. G(s) is defined in Equation 49.

$$G(s) = H1 \cdot H2 \cdot H3 \cdot F \cdot H0$$

Equation 49 System Transfer Function without LLR

With LLR, the functions H4 and H5 create a second, internal closed loop (see Figure 14). There are then two nested loops inside of the outer voltage control loop (being, the duty-cycle modulator in F(s), and inductor current to feedback adjustment through H4 and H5 to the input of H2). This second closed path is represented as H(s) in Equation 50.

$$H(s) = H2 \cdot H3 \cdot F \cdot H5 \cdot H4$$

Equation 50 LLR Closed Loop Path

Using the forward path G(s) and closed loop path H(s), the control-to-output transfer function is represented in Equation 51.

$$\frac{G(s)}{1+H(s)} = \frac{H1 \cdot H2 \cdot H3 \cdot F \cdot H0}{1+H2 \cdot H3 \cdot F \cdot H5 \cdot H4}$$

Equation 51 System Transfer Function with LLR

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[4] Infineon Technologies: “MOSFET fast switching: motivation, implementation, and precautions”; October 20 2023

[5] RIC70849EVAL1 Product Page

[6] RIC70849 Datasheet

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Document revision	Date	Description of changes
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