Infineon Technologies Bipolar

AN2026-10 Prime Switch Press Pack IGBT

Explanation of Technical Information

About this document

Scope and purpose

This guide offers additional explanations and information to the conditions and values fixed in the datasheet for Infineon Prime Switch Press Pack IGBT.

Intended audience

This document is intended for any expert using Infineon Prime Switch Press Pack IGBTs

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Abstract

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1 Abstract

The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device. This Application Note is intended to provide an explanation of the parameters and diagrams given in the datasheet of Press Pack IGBT devices. With the Application Note, the designer of power electronic systems, requiring a Press Pack IGBT, is able to use the datasheet in a proper way and will be provided with background information.

2 Introduction

The parameters listed in the datasheet are values that describe the characteristics of the Press Pack IGBT as detailed as possible.

With this information, the designer should be able to compare devices from different suppliers to each other. Furthermore, the information should be sufficient to figure out the limits of the device.

This document explains the interaction between the parameters and the influence of conditions like temperature. Datasheet values that refer to dynamical characterization tests, e.g. switching losses, are related to a specific test setup with its individual characteristics. Therefore, these values can deviate from a user's application.

The attached diagrams, tables and explanations for Press Pack IGBT refer to the datasheet of a P3000ZL45X168 rev.3.0 from 2021-08-31 as an example. The values and characteristics shown are not necessarily feasible to be used for design-in activities. For the latest version of datasheets please refer to our website.

Infineon's datasheets of Press Pack IGBTs are structured as listed below:

- Summarized device description on the front page as shown in Figure 1
- Maximum rated electrical values of IGBT-chips
- Recommended electrical operating conditions of IGBT-chips
- Maximum rated electrical values of diode-chips, if applicable
- Recommended electrical operating conditions of diode-chips, if applicable
- Parameters concerning the overall device
- Operating characteristics
- Circuit diagram
- Package outline
- Terms and conditions of usage

Introduction

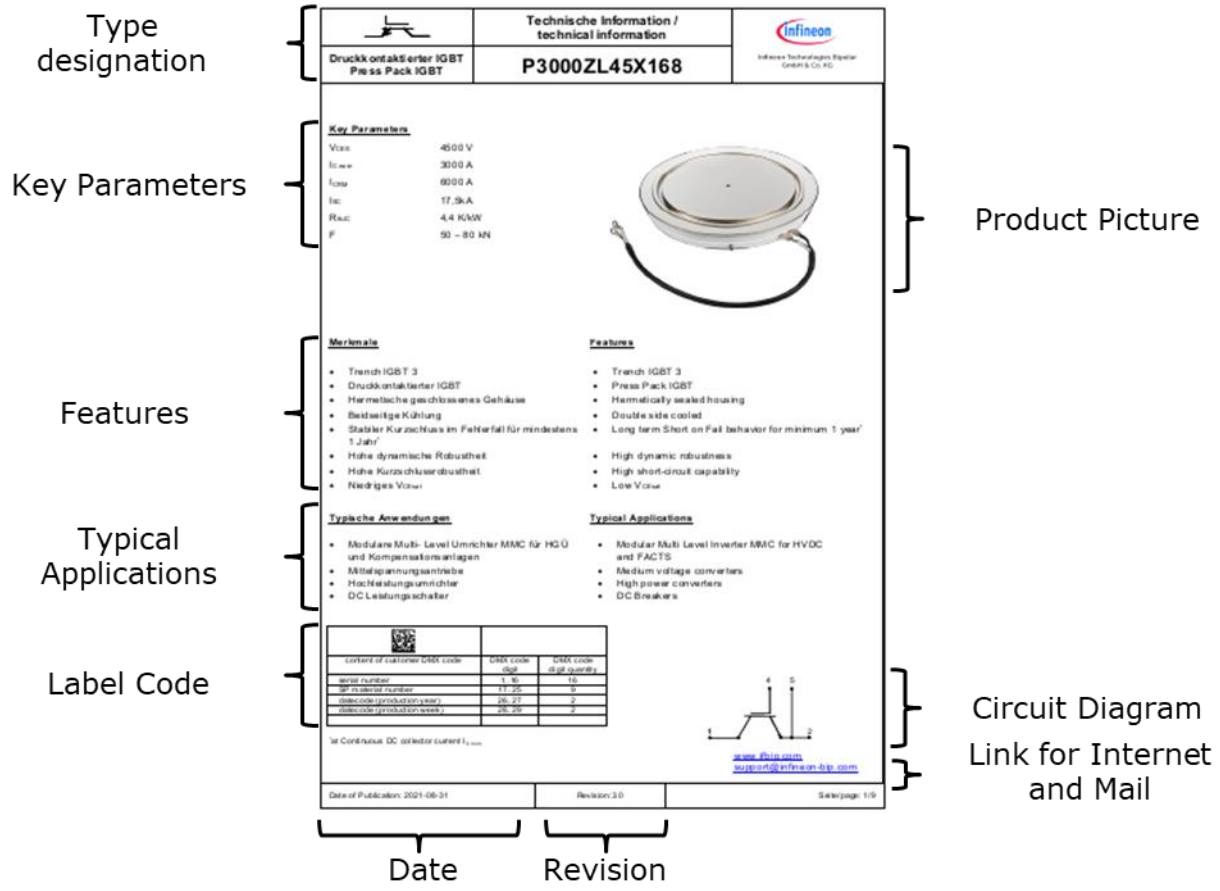


Figure 1: Front page of the datasheet

2.1 Status of datasheets

Depending on the status of the product development, the relating technical information contains:

- **Target data**

The numbers in these datasheets are target values, which are expected to be achieved. Values from these target datasheets are useful for the initial calculations and approximations. The information and values of a target datasheet cannot be guaranteed for the final product. The dimensioning of an inverter should only be done with values based on a preliminary or final datasheet.

During the development phase, the devices are labeled with their type designation and carry the suffix ENG. Modules with the ENG designation are supplied with a Sample Release Document. Important information can be taken from this additional Sample Release Document, e.g. which values of the device are already fixed and which values can still change during the development phase. ENG device samples are used for preliminary and functional tests during the early stages of a product development phase. Samples marked as ENG are not liable to Product Change Notification (PCN).

- **Preliminary data**

The difference between a preliminary and a final datasheet is, that certain values are still missing, for example the maximum values. These missing values in the preliminary datasheet are marked to be defined (t.b.d.).

Devices without ENG on the label reached series production status. All quality requirements are completely fulfilled. If any major change to a device with series production status is necessary, customers must be informed by means of a PCN containing information about the type and extent as well as the time of the changes.

This also applies to devices that have preliminary datasheets.

- **Final data**

The final datasheet is completed with the values which were missing in the preliminary datasheet. Major changes of device characteristics or changes in datasheet values in the series status are accompanied by a PCN.

2.2 Type designation

The first section of the datasheet begins with the type designation of the device as shown in Figure 2.

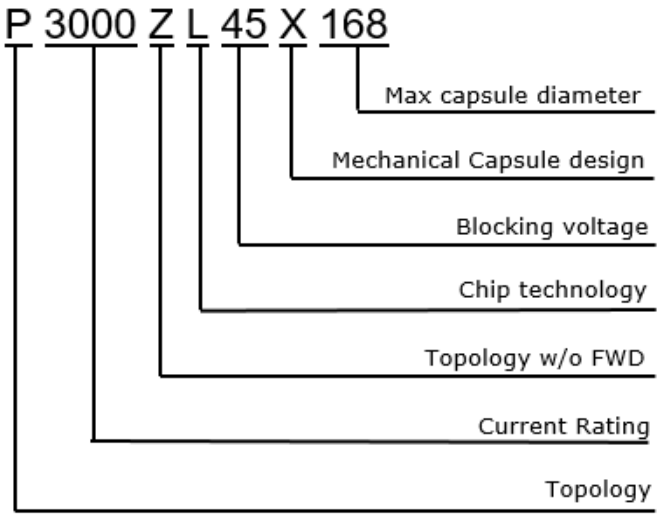


Figure 2: Structure of the type designation

The following table give a detailed insight to the type designation of Infineon's Press Pack IGBTs.

P	3000	Z	L	45	X	168	Explanation
P							Press Pack IGBT
	3000						Max DC current in A
		Z					No freewheeling diode included
		D					Freewheeling diode included
			L				Trench IGBT with low VCE sat
			E				Fast trench IGBT with low VCE sat
				45			Collector-emitter-voltage in 100 V
					X		Mechanical enhanced housing
						168	Outer flange diameter in mm 168mm for 125mm diameter contact area

Table 1: Overview for PPI type designation

2.3 PPI Label Code

To facilitate the handling of the Press Pack IGBT from logistic's and traceability point of view, all Infineon IGBT PPIs are considered as unique and labeled as represented in Figure 3. Each module can be identified with its material number, serial number and datecode. All Press Pack IGBT follow similar rules for labeling and identification. DMX codes are given on the devices for automated identification. Test data are stored for eleven years.



content of customer DMX code	DMX code digit	DMX code digit quantity
serial number	1..16	16
SP material number	17..25	9
datecode (production year)	26..27	2
datecode (production week)	28..29	2

Figure 3: Example of Device Label Code

3 Datasheet electrical parameters Press Pack IGBT

This section explains the electrical properties of the IGBT chips inside the given Press Pack IGBT.

If one of these maximum ratings presented in the datasheet is exceeded, it may result in a breakdown of the semiconductor, even if the other ratings are not stressed to their limits. Unless specified to the contrary, the values apply at a temperature of 25°C.

3.1 Collector – emitter voltage V_{CES}

The permissible peak collector - emitter voltage is specified at different junction temperatures as seen in Figure 4. This value decreases for lower temperatures <-40°C with a factor of approximately $B_{V_{CES}} \approx 0.1 \frac{\%}{K}$.

Kollektor-Emitter-Sperrspannung Collector-emitter voltage	$T_{vj\,max}$ = -40°C $T_{vj\,max}$ = 25°C $T_{vj\,max}$ = 150°C	V_{CES}	4500 4500 4500	V V V

Figure 4: Collector - emitter voltage of the IGBT

3.2 Total power dissipation $P_{tot\,h}$

This parameter describes the maximum feasible power dissipation through the thermal resistance junction to case R_{thJC}.

The total power dissipation can be calculated in general to be:

$$P_{tot} = \frac{\Delta T}{R_{th}} \tag{1}$$

The considered device is a Press Pack IGBT with double side cooling. The power dissipation is related to ΔT between junction and case and the thermal resistance R_{thJC} between junction and case as hinted out in equation.

$$P_{tot} = \frac{T_{vj} - T_C}{R_{thJC}} \tag{2}$$

For example at a case temperature of 25°C the power dissipation, of P3000Z45X168, is specified as a maximum value of:

$$P_{tot} = \frac{(150 - 25)K}{4{,}4\frac{K}{kW}} = 28{,}4kW \tag{3}$$

The power dissipation of the diode chips, where applicable, can be calculated the same way as for the IGBTs, in accordance to equation (2).

3.3 DC Collector Current I_C

Based on the total power dissipation, the maximum permissible collector current rating of a Press Pack IGBT can be calculated with equation (4). Thus, in order to give a current rating of a device, the corresponding

junction and case temperature has to be specified, as shown for example in Figure 6. Please note that current ratings without defined temperature conditions have no technical meaning at all.

$$I_C = \frac{T_{vj} - T_C}{R_{thjc} \cdot V_{CEsat}(I_C, T_{vj})} \quad (4)$$

Since I_C is not known in equation (4), V_{CEsat} @ I_C is also not known, but can be found within a few iterations. The ratings of continuous DC-collector current are calculated using maximum values for V_{CEsat} to ensure the specified current rating, taking component tolerances into account.

Kollektor-Dauergleichstrom Continuous DC collector current	T_C = 105°C, $T_{vj\,max}$ = 150°C	$I_{C\,nom}$	3000	A

Figure 5: DC collector current

3.4 Repetitive peak collector current I_{CRM}

The nominal current rating can be exceeded in an application for a short time. This is defined as repetitive peak collector current in the datasheet as can be seen in Figure 7 for the specified pulse duration. In theory, this value can be derived from the feasible power dissipation and the transient thermal impedance Z_{th}, if the duration of the over current condition is defined. However, this theoretical value is not taking any limitations of bus-bars or power connectors into account.

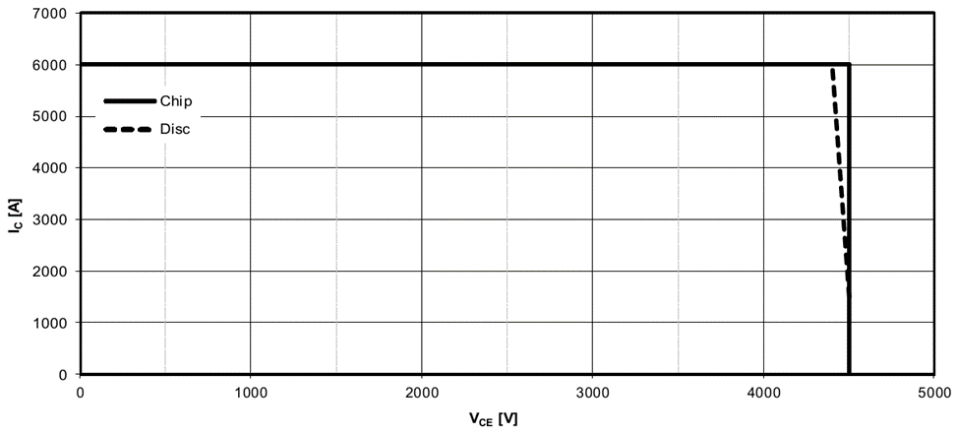
Therefore, the datasheet value is quite low compared to a calculated value based on theory, but it specifies a safe operation considering all practical limitations of the Press Pack IGBT.

Periodischer Kollektor-Spitzenstrom Repetitive peak collector current	t_P = 1 ms	I_{CRM}	6000	A

Figure 6: Repetitive peak collector current

3.5 Reverse bias safe operating area RBSOA

This parameter describes safe operating conditions at turn-off for the IGBT. The Press Pack IGBT can be driven within its specified blocking voltage up to twice its nominal current rating, if the maximum temperature under switching conditions is not exceeded as shown in Figure 8. With increasing currents, the allowed DC-Link voltage is decreased. Furthermore, this derating strongly depends on system related parameters, like stray inductance of the DC-Link and the current commutation slope during the switching transitions. The DC-Link capacitor is assumed to be ideal for this operating area. The current commutation slope is defined via a specified gate resistance and gate driving voltage. In no event the voltage spike must not exceed the specified voltage of the device at the terminals or at chip level to keep the RBSOA limits.



Sicherer Rückwärts-Arbeitsbereich IGBT, Wechselrichter (RBSOA)
Reverse bias safe operating area IGBT,Inverter (RBSOA)

$I_C=f(V_{CE})$
$V_{GE}=\pm15V$, $R_{Goff}= 8\Omega$, $T_{vj}=150°C$

Figure 7: Reverse bias safe operating area

3.6 Typical output and transfer characteristics

This data can be used to calculate conduction losses of the IGBT. In order to contribute to a much better understanding of these parameters, the IGBT device structure as well as it's difference in output characteristic compared to a power MOSFET is discussed briefly. After this, the datasheet parameters of the Press Pack IGBTs are explained.

Figure 8a shows in detail the structure of a trench-field-stop IGBT with a simplified two-transistor equivalent circuit. The emitter-sided pn-junction of the pnp-transistor resembles the IGBT's collector side. Like a diode it leads to a characteristic voltage drop when the IGBT is conducting current. The intrinsic bipolar transistor of the IGBT is driven by a MOSFET. Therefore, the gate driving characteristic is quite similar to a power MOSFET. The output characteristic is different, which is illustrated in Figure 8b schematically. It shows the characteristic of turned-on devices at two different junction temperatures.

The MOSFET as shown in Figure 8b is reverse conducting for negative drain-source voltages due to its intrinsic body diode. The IGBT has no body diode and thus an anti-parallel diode has to be used, when this operating mode is required. The advantage is, that the external diode can be optimized independently to suit the IGBT's switching characteristics.

In contrast to the MOSFET, that has an on resistance as a dominant parameter, the IGBT has a forward voltage drop. As a result, at very low load, indicated with 1 in Figure 8b, the MOSFET always has lower conduction losses than an IGBT.

Both output characteristics depend on the junction temperature. The $R_{ds(on)}$ of a MOSFET typically increases by a factor of about two, when the junction temperature increases from 25°C to 150°C. The temperature coefficient of an IGBT's forward voltage is much lower. At low load, the conduction losses even decrease with increasing temperature, due to the lower voltage drop at the pn-junction as represented in Figure 8b. At higher currents, the increase of the ohmic resistance is dominant. Due to this, a parallel connection of several IGBTs is possible and is commonly required for high current IGBT power modules.

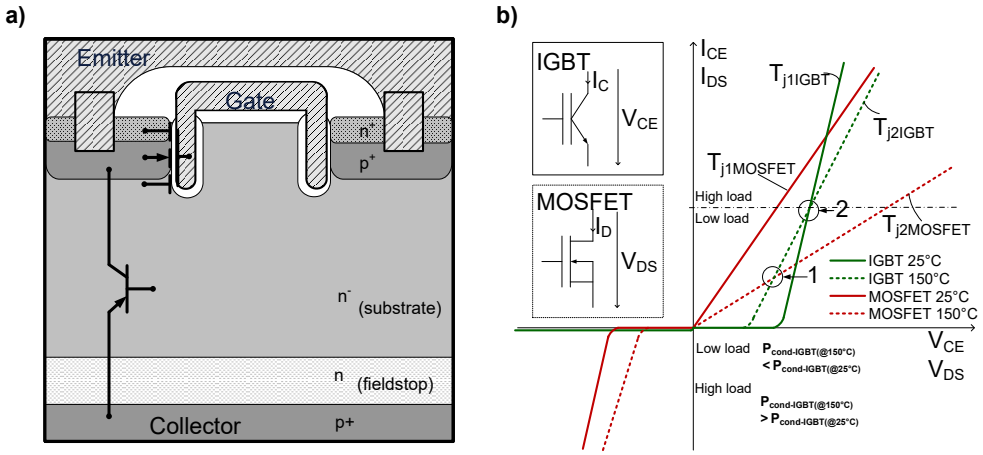


Figure 8: Structure of a Trench-Field-Stop IGBT and two-transistor equivalent circuit (a). Comparison of the output characteristics of power MOSFET and IGBT (b)

The transfer characteristic shows, that the turn-on threshold voltage decreases with increasing junction temperature as seen in Figure 9.

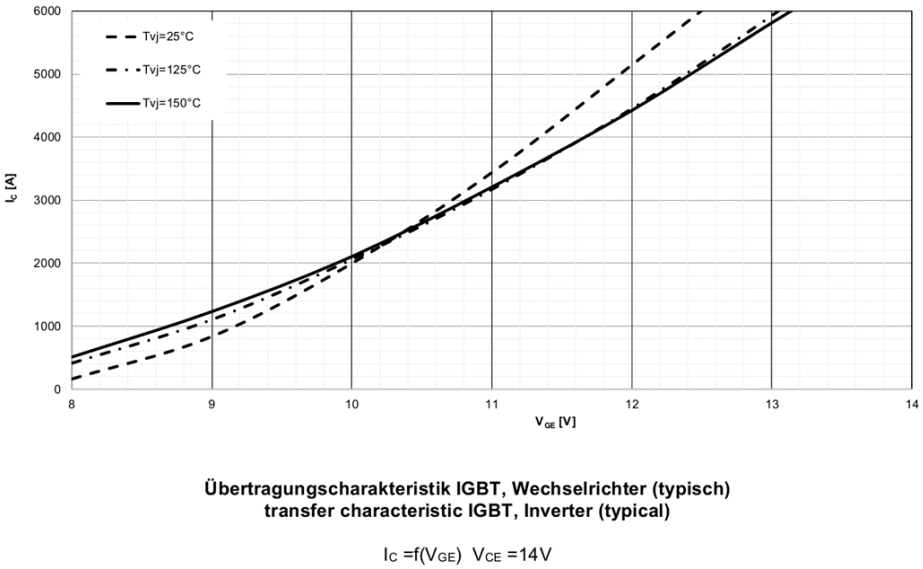


Figure 9: Typical transfer characteristic

As discussed in chapter 3.6, the output characteristic of the IGBT depends on the temperature of the junction. Figure 10a shows the collector current in conducting state as a function of the collector-emitter voltage at different junction temperatures. For currents lower than about 400A, the conduction losses decrease with increasing temperature. For higher currents, the conduction losses increase slightly. In the case considered, an increase in conduction losses of about 25% at nominal current 3000A and a temperature increase from 25°C to 150°C can be observed.

a) b)

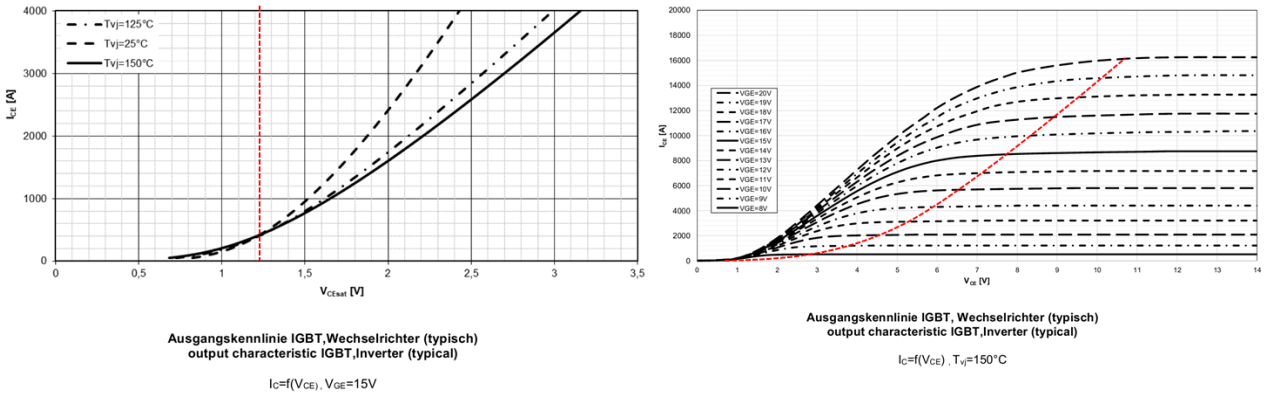


Figure 10: Typical output characteristic as a function of the temperature (a) and gate-emitter voltage variation (b)

Figure 10b shows the typical output characteristic for different gate-emitter voltages. The IGBT should not be operated in linear mode, as this causes excessive conduction losses. If the power dissipation is not limited in magnitude and time, the device might be destroyed. Using 15V as typical gate drive voltage, this linear mode only occurs for short periods at the switching transitions, which is a normal operating condition for the IGBT.

3.7 Parasitic Capacitances

The dynamic characteristics of an IGBT are influenced by several parasitic capacitances. These are inherent parts of the die's internal structure as represented in Figure 11a. A simplified schematic is shown in Figure 11b. The input capacitance C_{ies} and the reverse transfer capacitance C_{res} are the basis for an adequate dimensioning of the gate driver circuit. The output capacitance C_{oss} limits the dV/dt at switching transitions. Losses related to C_{oss} can usually be neglected.

The major parasitic capacitances inside the IGBT die are:

- Input capacitance $C_{ies} = C_{GE} + C_{res}$. C_{GE} includes C_1, C_3, C_4 and C_6
- Reverse transfer capacitance C_{res} including C_2 and C_5. $C_{res} = C_{CG}$
- Output capacitance C_{ce} represented by C_7. $C_{oss} = C_{CE} + C_{res}$

a) b)



Figure 11: Parasitic capacitances of an IGBT, internal structure a), schematic b)

The values of the parasitic capacitances strongly depend on the operating point of the IGBT. To measure these capacitances with gate- or collector-emitter voltages applied, dedicated measurement circuits according to IEC60747-8 have to be utilized.

Input capacitance C_{ies}

This parameter is determined using the setup in Figure 12. C_{ies} is measured across the gate and emitter connections with collector-emitter connection shorted for AC voltage. The values of the DC voltage across the gate-emitter and collector-emitter connections are specified with the test frequency. Capacitors C_1 and C_2 must form an adequate bypass at the test frequency. The inductor L decouples the DC supply.

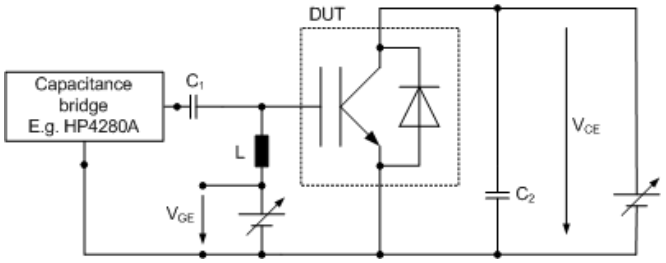


Figure 12: Basic circuit diagram for measuring the input capacitance C_{ies}

Output capacitance C_{oss}

C_{oss} is measured according to the setup in Figure 13. This value is measured across the collector and emitter connections with gate-emitter connections shorted for AC voltage. The values of the DC voltage across the gate-emitter and collector-emitter connections are specified with the test frequency. The capacitors C_1, C_2 and C_3 must form an adequate bypass at the test frequency. The inductor L decouples the DC supply.

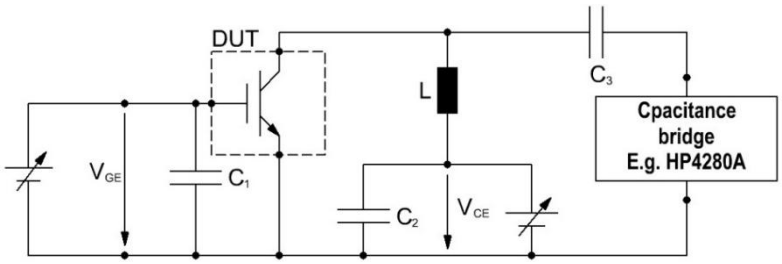


Figure 13: Basic circuit diagram for measuring the output capacitance C_{oss}

Reverse transfer capacitance C_{res}

Figure 14 gives details about the measurement setup for the reverse transfer capacitance. C_{res} is measured across the collector and gate connections, the emitter connection being connected to the protective screen of the bridge. The values of the DC voltage across the gate-emitter connection are specified with the test frequency. Capacitors C_1 and C_2 must form an adequate bypass at the test frequency. The inductors L_1 and L_2 decouple the DC supply.

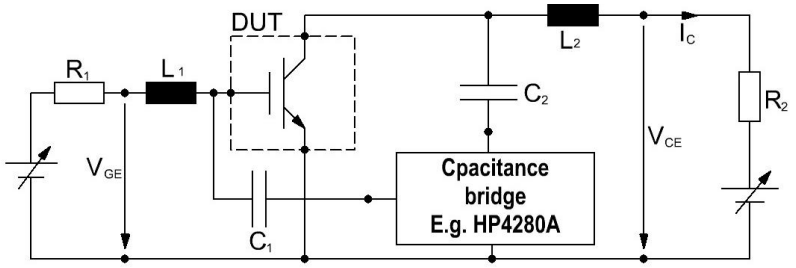


Figure 14: Basic circuit diagram for measuring the reverse transfer capacitance C_{res}

The capacitance meter used for the measurements of C_{ies}, C_{oss} and C_{res} has to be a high resolution capacitance bridge with a sufficient measurement range.

3.8 Gate charge Q_G, gate current, internal and external gate resistor

The value of the gate charge can be used to optimize the design of the gate driver circuit. The average output power that the gate driving circuit has to deliver can be calculated with data of the gate charge, gate driver voltages and switching frequency as given in equation 50.

$$P_{Gdr} = Q_G \cdot \left(V_{GE(on)} - V_{GE(off)}\right) \cdot f_{sw} \qquad (5)$$

Within this formula (5), Q_G refers to the part of the gate charge that is truly active in the given design. What part is used is depending on the gate driver output voltage; an accurate approximation can be done using the gate charge curve.

Typical values used in industrial applications include designs with a turn-off voltage V_{GE}=0V as well as designs featuring negative supply like V_{GE}=-8V

$Q'_G = 0.62 \bullet Q_G$ for 0V/15V

$Q'_G = 0.75 \bullet Q_G$ for -8V/15V

At a switching frequency of f_{sw}=250 Hz and a driver output voltage of +15/ -8V, the required output power of the gate driving circuit P_{Gdr} can be calculated using the adapted gate charge from equation (6) and the gate charge as seen in the datasheet Figure 15.

$$P_{Gdr} = 60\mu C \cdot 0{,}75 \cdot (15V + 8V) \cdot 250Hz = 259mW \qquad (6)$$

Gateladung Gate charge	V_{GE} = -15 / 15 V	Q_G		60		µC
Interner Gatewiderstand Internal gate resistor	T_{vj} = 25°C, v_D = 12 V	r_G		0,07		Ohm

Figure 15: Gate charge and internal gate resistor

The theoretical gate drive peak current can be calculated according to equation (7), knowing the gate drive voltages and gate resistances. The gate resistor is the sum of external and internal gate drive resistance Figure 15 shows the value for the internal resistance to be considered.

$$I_{Gdr,peak} = \frac{V_{GE(on)} - V_{GE(off)}}{R_{Gext} + \mathrm{R}_{Gint}} \quad (7)$$

In practice, this peak current will not be reached, because it is limited by stray inductances and non-ideal switching transitions of a real gate driving circuit.

The datasheet value given for the internal gate resistor has to be understood as a single resistance and may result from paralleled resistors inside the Press Pack IGBT. These internal resistors lead to improved internal current sharing.

The internal resistance should be considered as one part of total gate resistor to calculate the peak current capability of a driver.

The designer can use the external gate resistor to influence the switching performance of the IGBT. Minimum R_{Gon} is limited by turn-on di/dt, minimum R_{Goff} is limited by turn-off dV/dt. Too small gate resistors can cause oscillations and may lead to damage the IGBT or diode. The minimum recommended external gate resistor R_{Gext} is given in the switching losses test conditions as mentioned in

Figure 16. The allowed external gate resistor values are shown in the switching loss diagram Figure 21.

Einschaltverlustenergie pro Puls Turn-on energy loss per pulse	I_C = 3000 A, V_{CE} = 2800 V, Lσ = 150 nH V_{GE} = -15 / 15 V, R_{Gon} = 0,5 Ω Diode D4600U45	Tvj=25°C Tvj=125°C Tvj=150°C	E_{on}		8,5 10 11		J J J
Abschaltverlustenergie pro Puls Turn-off energy loss per pulse	I_C = 3000 A, V_{CE} = 2800 V, Lσ = 150 nH V_{GE} = -15 / 15 V, R_{Goff} = 4,8 Ω dv / dt ≤ 1100 V / µs	Tvj=25°C Tvj=125°C Tvj=150°C	E_{off}		18 23 26		J J J

Figure 16: External gate resistors

3.9 Parasitic turn-on

With the parasitic capacitances of the IGBT, noted in the datasheet as stated in Figure 17, dV/dt induced parasitic turn-on phenomena can occur. The cause of a possible parasitic turn-on is based on the intrinsic capacitive voltage divider between collector-gate and gate-emitter.

In consideration of high voltage transients across collector-emitter, this intrinsic capacitive voltage divider is much faster than an external gate driving circuit that is limited by parasitic inductances. Therefore, even if the gate driver turns off the IGBT with zero gate-emitter voltage, transients of collector-emitter voltage lead to an increase of the gate-emitter voltage. If the gate emitter voltage exceeds the gate threshold voltage V_{GEth}, the IGBT will turn on. Neglecting the influence of the gate driving circuit, the gate-emitter voltage can be calculated by

$$V_{GE} = \frac{C_{GC}}{C_{GC} + C_{GE}} \cdot \Delta V_{CE} = \frac{C_{res}}{C_{ies}} \cdot \Delta V_{CE} \quad (8)$$

The quotient C_{res}/C_{ies} should be as low as possible. To avoid a parasitic dV/dt induced turn-on, the quotient C_{ies}/C_{res} for the P3000ZL45X168 is about 34.2. Furthermore, the input capacitance should be as low as possible to avoid gate driving losses; therefore the use of additional gate-emitter capacitance C_{GE} has to be evaluated carefully.

Eingangskapazität Input capacitance	f = 1 MHz, T_{vj} = 25°C, V_{CE} = 25 V, V_{GE} = 0 V	C_{ies}	-	620	-	nF
Rückwirkungskapazität Reverse transfer capacitance	f = 1 MHz, T_{vj} = 25°C, V_{CE} = 25 V, V_{GE} = 0 V	C_{ires}	-	10,8	-	nF

Figure 17: Parasitic capacitances of the IGBT

The parasitic capacitances are determined under the conditions given in Figure 17. The gate-emitter capacitance C_{GE} as shown in Figure 18 can be approximated to be constant over the collector-emitter voltage as shown in equation (9).

$$C_{GE} \approx C_{ies}(25V) - C_{res}(25V) \tag{9}$$

The reverse transfer capacitance C_{res} strongly depends on the collector-emitter voltage and can be estimated according to equation (10).

$$C_{res}(V_{CE}) \approx \frac{C_{res}(25V) \cdot \sqrt{25V}}{\sqrt{V_{CE}}} \tag{10}$$

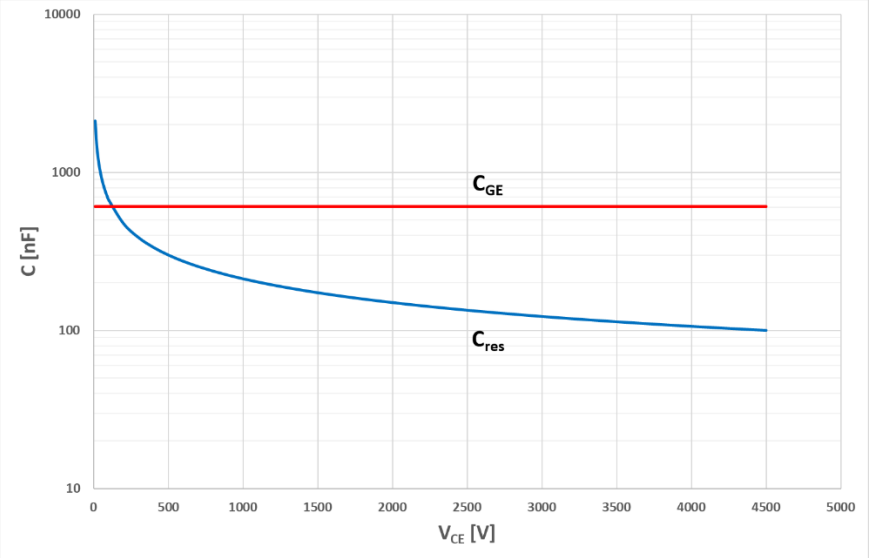


Figure 18: Approximation of C_{GE} and C_{CE} as function of the collector-emitter voltage according to equations (9) and (10)

Consequently, the robustness against dV/dt induced parasitic turn-on increases with the collector-emitter voltage as seen in equation (8).

3.10 Dynamic behavior

The switching characteristic described in the datasheet provides useful information to determine an appropriate dead time between turn-on and turn-off of the complementary devices in a half bridge configuration. For further information about dead time calculation please refer to AN2007-04[1] available at Infineon's website.

[1] Application note 2007-04: How to calculate and minimize the dead time requirement for IGBTs properly.

- Turn-on delay time $t_{d\,on}$:

Time it takes from getting the gate-emitter voltage to 10% of the rated value to the moment the collector current reaches 10% of its nominal size

- Rise time t_r:

Time which the collector current takes to rise from 10% to 90% of its nominal value

- Turn-off delay time $t_{d\,off}$:

Time necessary from getting the gate-emitter voltage to 90% of the rated value to the moment the collector current reaches 90% of its nominal size

- Fall time t_f:

Time which the collector current takes to fall from 90% to 10% of its nominal value

The times in the datasheet are defined as detailed in Figure 19:

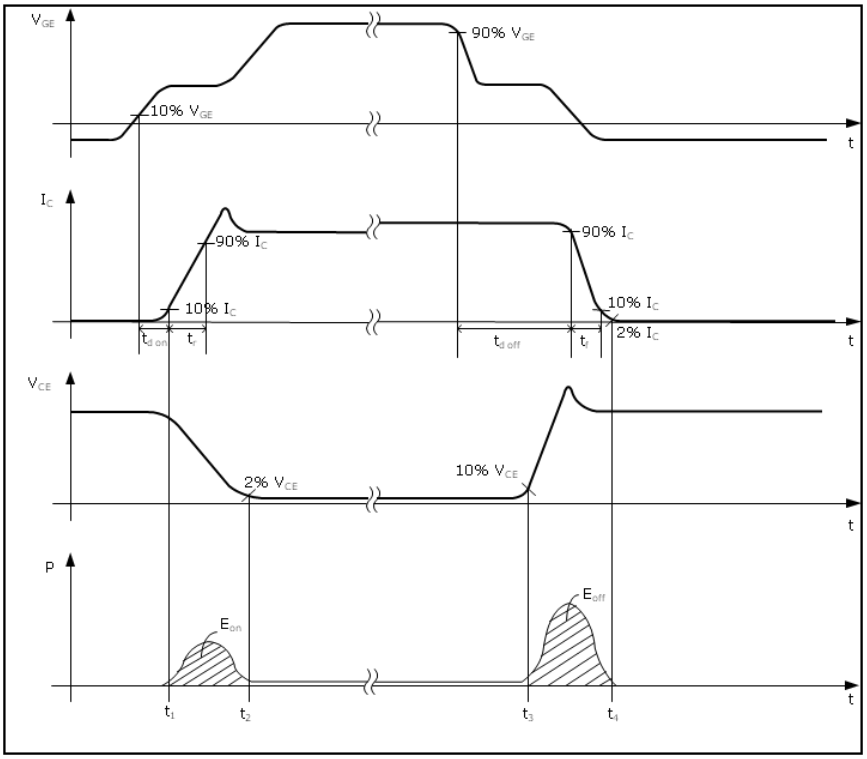


Figure 19: Specification of rise and fall times and conditions to calculate switching losses

These times alone will not give reliable information about switching losses, because voltage rise and fall times as well as current tail shape are not specified. Therefore, switching losses per pulse are given separately.

The switching losses per pulse are defined using the integrals:

$$E_{on} = \int_{t_1}^{t_2} U_{CE} \cdot I_C \cdot dt \qquad E_{off} = \int_{t_3}^{t_4} U_{CE} \cdot I_C \cdot dt \qquad (11)$$

The integration limits for the switching losses are given in Figure 19:

- E_{on} as turn-on energy per pulse from t_1 to t_2
- E_{off} as turn-off energy per pulse from t_3 to t_4

Dynamic behavior and thus energy per pulse strongly depend on a variety of application specific operating conditions like gate driving circuit, layout, gate resistance, magnitude of voltages and currents to be switched as well as the junction temperature. Therefore, datasheet values can only give an indication for the switching performance of the power module. For more accurate values, detailed simulations taking application specific parameters into account or experimental investigations are necessary.

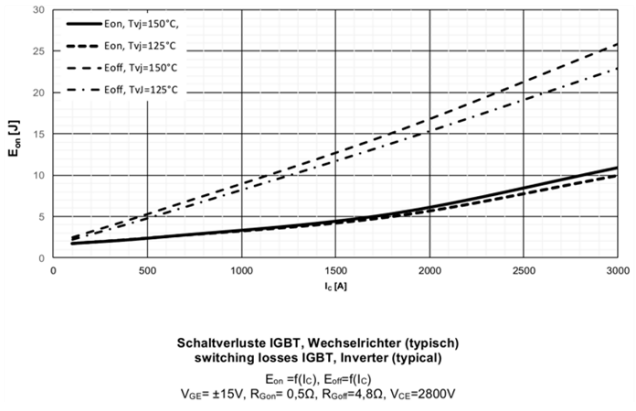
Typically, switching transition duration and energy per pulse are characterized at nominal operating conditions for different temperatures as noted in Figure 20.

Einschaltverzögerungszeit, induktive Last Turn-on delay time, inductive load	I_C = 3000 A, V_{CE} = 2800 V V_{GE} = -15 / 15 V, R_{Gon} = 0,5 Ω Diode D4600U45	Tvj=25°C Tvj=125°C Tvj=150°C	$t_{d\,on}$		0,39 0,41 0,42		µs µs µs
Anstiegszeit, induktive Last Rise time, inductive load	I_C = 3000 A, V_{CE} = 2800 V V_{GE} = -15 / 15 V, R_{Gon} = 0,5 Ω Diode D4600U45	Tvj=25°C Tvj=125°C Tvj=150°C	t_r		0,30 0,32 0,32		µs µs µs
Abschaltverzögerungszeit, induktive Last Turn-off delay time, inductive load	I_C = 3000 A, V_{CE} = 2800 V V_{GE} = -15 / 15 V, R_{Goff} = 4,8 Ω dv / dt ≤ 1100 V / µs	Tvj=25°C Tvj=125°C Tvj=150°C	$t_{d\,off}$		9,8 10,4 11,0		µs µs µs
Fallzeit, induktive Last Fall time, inductive load	I_C = 3000 A, V_{CE} = 2800 V V_{GE} = -15 / 15 V, R_{Goff} = 4,8 Ω dv / dt ≤ 1100 V / µs	Tvj=25°C Tvj=125°C Tvj=150°C	t_f		1,7 3,7 4,2		µs µs µs
Einschaltverlustenergie pro Puls Turn-on energy loss per pulse	I_C = 3000 A, V_{CE} = 2800 V, Lσ = 150 nH V_{GE} = -15 / 15 V, R_{Gon} = 0,5 Ω Diode D4600U45	Tvj=25°C Tvj=125°C Tvj=150°C	E_{on}		8,5 10 11		J J J
Abschaltverlustenergie pro Puls Turn-off energy loss per pulse	I_C = 3000 A, V_{CE} = 2800 V, Lσ = 150 nH V_{GE} = -15 / 15 V, R_{Goff} = 4,8 Ω dv / dt ≤ 1100 V / µs	Tvj=25°C Tvj=125°C Tvj=150°C	E_{off}		18 23 26		J J J

Figure 20: Switching times and energies

A first estimation of dynamical losses can be done utilizing Figure 21. The diagram hints out typical losses depending on R_G, I_C and junction temperature T_{vj}. The switching loss diagram Figure 21a and b shows also the allowed external gate resistor values. The left end of the curves in Figure 21b specifies the minimum allowed external gate resistor value. The gate resistors must not be lower because this may lead to a destruction of the device.

a)



b)

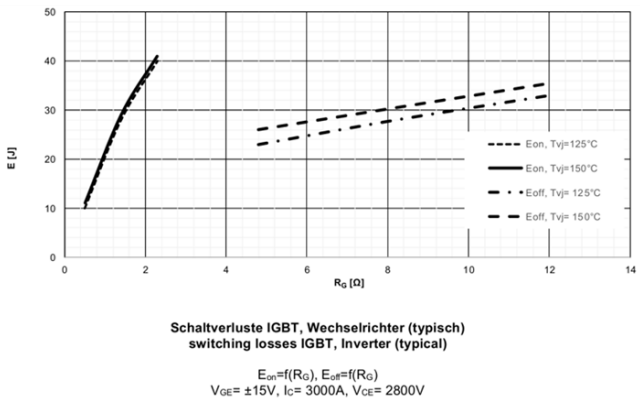


Figure 21: Switching losses per pulse as a function of the collector current and the gate resistance

3.11 Short circuit

The short circuit characteristic strongly depends on application specific parameters like temperature, stray inductances, gate driving circuits and the resistance of the short circuit path. For device characterization, a test setup as drawn in Figure 22a is used. The IGBT is driven with a single pulse. The corresponding typical voltage and current waveforms are illustrated in Figure 22b. The current in the conducting IGBT increases rapidly with a current slope that is depending on parasitic inductances and the DC-Link voltage. Due to desaturation of the IGBT, the current is limited to about 5 times the nominal current in case of IGBT3 and the collector-emitter voltage remains on the high level. The chip temperature increases during this short circuit due to high currents and thus high losses. Because of the increasing chip temperature the current decreases slightly while operating in short circuit condition. Within a defined short-circuit-withstand time t_{sc} the IGBT has to be switched off to avoid a device failure.

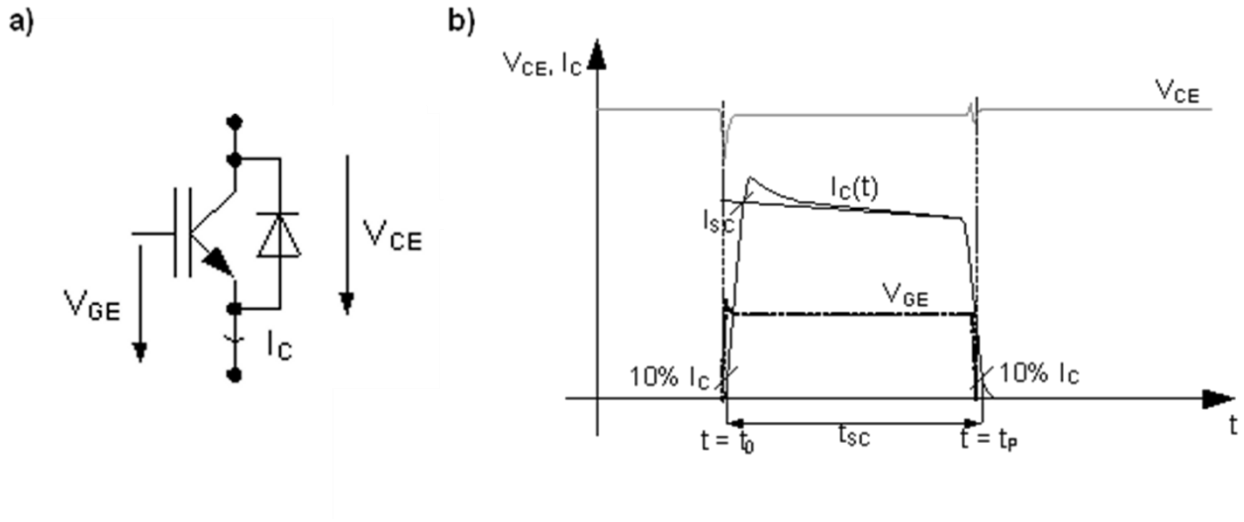


Figure 22: Short circuit test setup (a) and typical ideal voltage/current waveforms during short circuit test (b)

The data of the measured short circuit and the applied parameters are noted in the datasheet as depicted in Figure 23. All of Infineon's Press Pack IGBTs are designed to achieve a short circuit-withstand-time of up to 10µs.

Kurzschlußverhalten SC data	$V_{GE} \leq 15$ V, $V_{CC} = 2800$ V $V_{CEmax} = V_{CES} - L_{sCE} \cdot di/dt$ $T_{vj} = 125°C$	I_{SC}		17,5		kA

Figure 23: Short circuit data

3.12 Leakage currents I_{CES} and I_{GES}

Two major types of leakage currents as given in Figure 24 have to be considered:

- The maximum collector-emitter cut-off current describes the leakage current between the collector and emitter, when the IGBT is in blocking mode
- The gate-emitter leakage current gives a hint about the maximum leakage current between gate and emitter, with collector-emitter short circuited and maximum gate-emitter voltage applied.

Kollektor-Emitter-Reststrom Collector-emitter cut-off current	V_{CE} = 4500 V, V_{GE} = 0 V, T_{vj} = 25°C	I_{CES}		150	200	µA
Gate-Emitter-Reststrom Gate-emitter leakage current	V_{CE} = 0 V, V_{GE} = 20 V, T_{vj} = 25°C	I_{GES}		0,35	1,2	µA

Figure 24: Leakage currents

3.13 Thermal characteristics

The values of power dissipation and current ratings as discussed in chapters 3.2 and 3.3 have no meaning without specification of temperatures as well as thermal resistances. Therefore, in order to compare different devices, it is also necessary to compare thermal characteristics.

When Press Pack IGBT devices are characterized, junction-, case-, and heat sink temperatures are observed. The thermal resistances of junction to case and case to heat sink are specified in the datasheet as given in Figure 25. The datasheet value of the R_{thCH} is a typical value under the specified conditions without use of thermal interface material.

Innerer Wärmewiderstand thermal resistance, junction to case	Kühlfläche / cooling surface beidseitig / two-sided, DC	R_{thJC}	max.	4,4	K/kW
Übergangs-Wärmewiderstand thermal resistance, case to heatsink	Kühlfläche / cooling surface beidseitig / two-sided	R_{thCH}	typ.	1,0	kW

Figure 25: Thermal resistance IGBT, junction to case and case to heat sink

The thermal resistance characterizes the thermal behavior of the Press Pack IGBT at steady state, this value has a strong behavior to the clamping force. Figure 26 shows the typical behavior of the thermal resitance vs clamping force.

All the thermal data in the datasheet are defined at minimum clamping force, e.g. for P3000ZL45X168 this is 50kN.

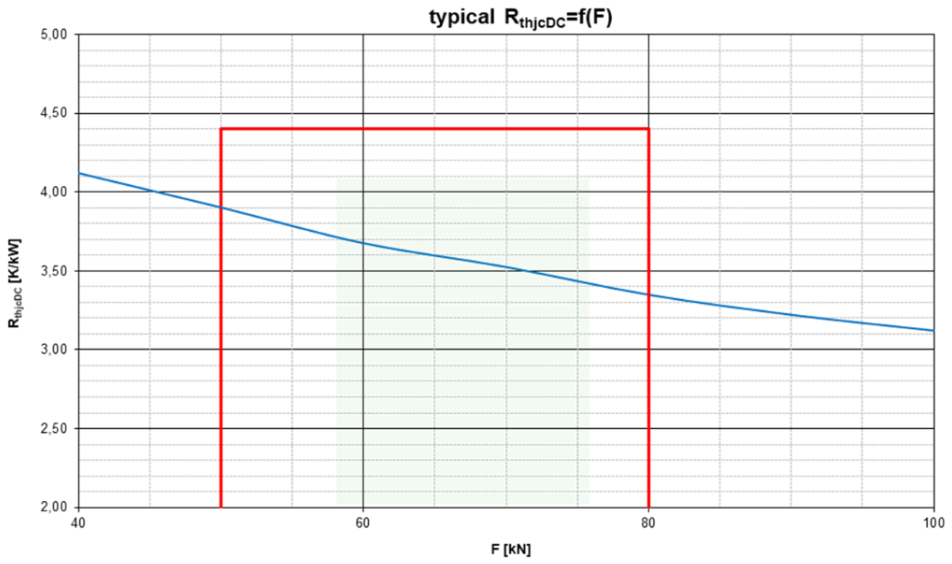
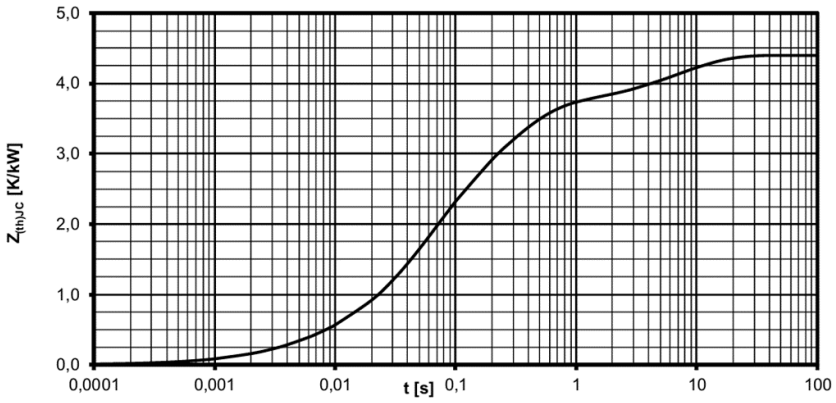


Figure 26: Typical Thermal Resistance as function of the clamping force for P3000ZL45X168

The thermal impedance characterizes the thermal behavior of the device at transient conditions like short current pulses. Figure 27a shows the transient thermal impedance Z_{thJC} as a function of the time.

a)



Transienter innerer Wärmewiderstand für DC
transient thermal impedance Z_{thJC} = f(t) for DC

Beidseitige Kühlung / two-sided cooling

Analytische Elemente des transienten Wärmewiderstandes Z_{thJC} /
analytical elements of transient thermal impedance Z_{thJC}

	Pos. n	1	2	3	4	5	6	7
beidseitig two-sided	R_{thn} [K/kW]	0,7328	1,6488	1,832	0,1832			
	τ_n [s]	7,0	0,25	0,05	0,004			

Analytische Funktion / analytical function: $Z_{thJC} = \sum_{n=1}^{n_{max}} R_{thn}\left(1 - e^{-\frac{t}{\tau_n}}\right)$

b)

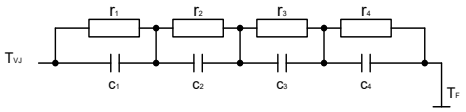


Figure 27: a) Transient thermal impedance junction to case and b) transient thermal model

The main power losses of the Press Pack IGBT are dissipated from the silicon die to the heat sink through different materials. Each material within the dissipation path has its own thermal characteristics. As a result, the thermal impedance behavior can be modeled with the appropriate coefficients of the Press Pack IGBT and is given as diagram $Z_{thJC}(t)$ as shown in Figure 27a. The separate RC-elements from Figure 27b have no physical meaning. Their values are extracted from the measured heating-up curve of the device by a corresponding analysis tool. The datasheet includes the partial fraction coefficients in tabular form as shown in Figure 27a. The values of the capacitances can be calculated by:

$$c_i = \frac{\tau_i}{r_i} \tag{12}$$

4 Datasheet electrical parameters Diode

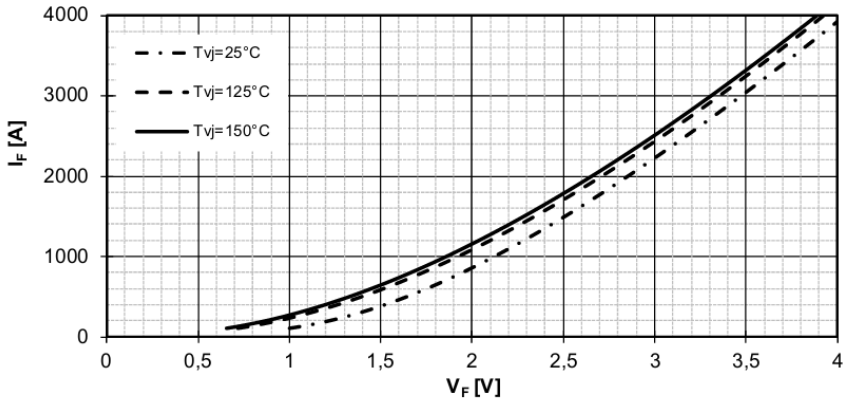
This section explains the electrical properties of the diode chips inside the given Press Pack IGBT when built in. The attached diagrams, tables and explanations for IGBT are referring to the datasheet of a P2000DL45X168 rev.3.1 from 2022-02-17 as an example. The values and characteristics shown are not necessarily feasible to be used for design-in activities. For the latest version of datasheets please refer to our website.

4.1 Diode forward characteristic

The maximum permissible diode forward current rating can be calculated with equation 130. To give a current rating of a module, the corresponding junction and case temperature have to be specified, for example in Figure 28. Please note that current ratings without defined temperature conditions have no technical meaning at all. Since I_F is not known in equation 0, V_F @ I_F is also not known, but can be found within a few iterations. The ratings of continuous collector current are calculated with maximum values for V_F to ensure the specified current rating, taking component tolerances into account.

$$I_F = \frac{(\mathrm{T_{vj}} - \mathrm{T_C})}{R_{thJC} \cdot \mathrm{V_F}(\mathrm{I_F}, \mathrm{T_{vj}})} \tag{13}$$

Figure 28 depicts the typical forward characteristic of the implemented diode at different junction temperatures. A negative temperature coefficient of the diode's forward voltage drop can be observed, which is typical for minority-carrier devices. Therefore, the conduction losses of the diode decrease with increasing temperatures. The negative temperature coefficient does not harm the paralleling of the chips or even of devices as the difference of voltage drop is getting smaller at higher currents. And at very high currents it changes also to a positive temperature coefficient.



Durchlasskennlinie der Diode, Wechselrichter (typisch)
Forward characteristic of Diode, Inverter (typical)
$I_F=f(V_F)$

Figure 28: Forward characteristic of diode datasheet

4.2 Repetitive peak forward current

The nominal diode current rating can be exceeded in an application for a short time. This is defined as repetitive peak forward current in the datasheet for the specified pulse duration, for example 1ms as noted in Figure 29. In theory, this value can be derived from the feasible power dissipation and the transient thermal

impedance Z_{th}, if the duration of the over current condition is defined. However, this theoretical value is not taking any limitations of bus-bars or power connectors into account.

Periodischer Spitzenstrom Repetitive peak forward current	t_P = 1 ms	I_{FRM}	4000	A

Figure 29: Repetitive peak forward current

4.3 Surge current and I²t value

This value defines the surge current capability of the diode. The surge current or I^2t value applied should be lower than the specified values and t_p should not exceed 10ms as mentioned in Figure 30.

Stoßstrom Surge current	V_R = 0V, t_p = 10ms, T_{vj} = 125°C	I_{FSM}	17000	A
Grenzlastintegral I2t - value	V_R = 0V, t_p = 10ms, T_{vj} = 125°C	I^2t	1445	kA^2s

Figure 30: Values of the surge current capability

4.4 Reverse recovery

To investigate the transient behavior of a diode, the surrounding circuitry has to be taken into account. To simplify the circuitry, the output current of the half bridge, shown in Figure 31 a, can be assumed to be constant during commutation. The remaining stray inductances formed by the current loop can now be replaced by just one stray inductance between high-side and low-side switch/freewheeling diode.

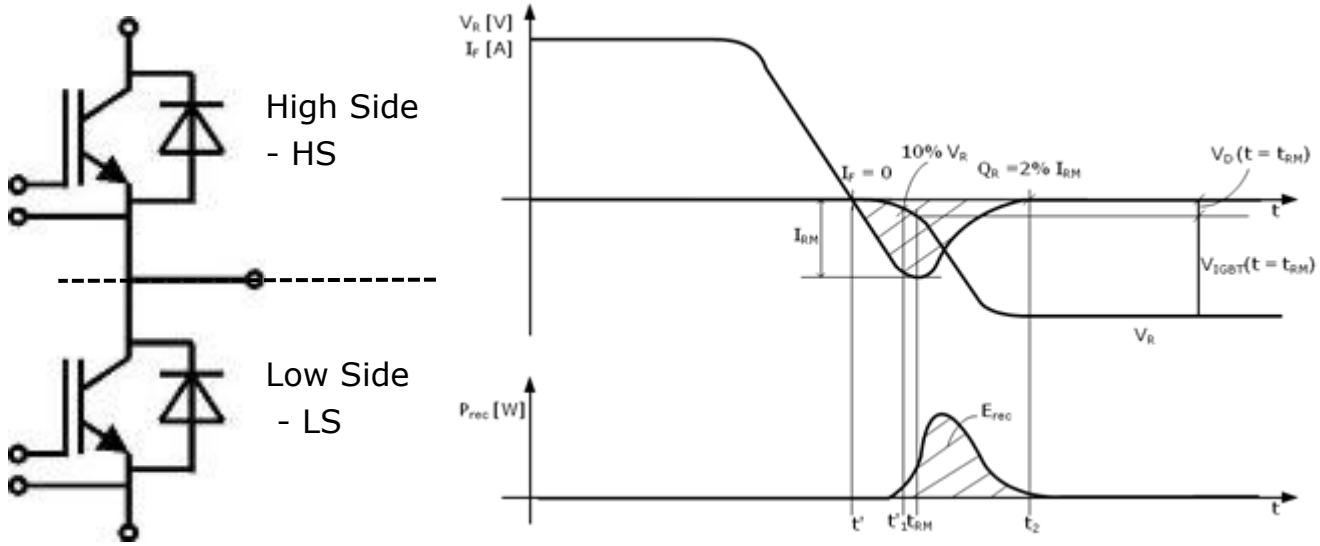


Figure 31: a) Half bridge circuit, b) Schematic voltage and current waveform of a soft-recovery diode during turn-off transition

The commutation is triggered by turning-on the LS-IGBT which will not reduce the blocking voltage to roughly zero immediately. It will keep a portion of blocking voltage during the commutation. Due to the fact that the HS-diode is still on, the difference $V_L = V_R - V_{IGBT}$ will drop across the stray inductance causing a linear change of current. The diode current will reduce in the same way as the IGBT current increases. As soon as the diode current at t = t' crosses zero, a space charge region within the diode can be formed. Hence the voltage drop across the diode increases as can be seen Figure 31 b.

The voltage drop across the stray inductance will be zero if the sum of diode and IGBT voltage is equal to the blocking voltage V_R

$$V_R = V_{IGBT} - V_D \cdot I_F \cdot \frac{di}{dt} \quad (14)$$

As a result, the peak reverse recovery current I_{RM} is reached. The current commutation is finished and the reverse recovery current has to be reduced to zero. Any kind of oscillation has to be avoided.

After $t > t_{RM}$, the LS-IGBT which is still not fully turned on will reduce its voltage further and the blocking voltage of the HS-diode will increase to the final V_R. During this last step, the current change from I_{RM} to zero will result in an overvoltage across the diode; however in this case it will be masked by the increasing blocking voltage.

The reverse recovery of the diode will lead to additional turn-off losses as well as additional turn-on losses in the complementary switch. A current and voltage waveform of a soft-recovery emitter controlled diode during turn-off transition can be seen in Figure 31 b.

The characterized peak reverse recovery current I_{RM} given in the datasheet section on Figure 32, is defined as the difference between the maximum negative current peak and zero current. The recovered charge results from:

$$Q_r = \int_{t'_1}^{t'_2} I_F \cdot dt \quad (15)$$

The integration limits are defined as $t = t'_1$ @ $I_F = 0$ and $t = t'_2$ @ $|I_F| \leq 0.02 \cdot I_{RM}$ as marked in Figure 31 b.

The losses due to reverse recovery can be calculated with the recovered energy per pulse. The energy is determined as defined in equation (16).

$$E_{rec} = \int_{t'_1}^{t_2} V_R \cdot I_F \cdot dt \quad (16)$$

The integration limits are chosen for the time t'_1 corresponding to 10% of the diode reverse voltage V_R and the time t_2 when the reverse recovery current I_{RM} peak attains 2%.

The recovered charge and thus switching losses caused by the reverse recovery of the diode strongly depend on junction temperature as well as current slope.

Rückstromspitze Peak reverse recovery current	I_F = 2000 A, V_R = 2800 V, R_{gon} = 1,2Ω , V_{GE} = +15V ; L_S=150nH	T_{vj}=25°C T_{vj}=125°C T_{vj}=150°C	I_{RM}		1900 2460 2580		A A A
Sperrverzögerungsladung Recovered charge	I_F = 2000 A, V_R = 2800 V, R_{gon} = 1,2Ω , V_{GE} = +15V ; L_S=150nH	T_{vj}=25°C T_{vj}=125°C T_{vj}=150°C	Q_{rr}		1500 3350 3900		µAs µAs µAs
Abschaltenergie Reverse recovery energy	I_F = 2000 A, V_R = 2800 V, R_{gon} = 1,2Ω , V_{GE} = +15V ; L_S=150nH	T_{vj}=25°C T_{vj}=125°C T_{vj}=150°C	E_{rec}		2,2 5,7 6,8		J J J

Figure 32: Reverse recovery current, charge and reverse recovery energy

To give an indication of application specific switching losses, the losses per diode turn-off pulse as noted in the datasheet are a function of diode forward current and gate resistance of the switching IGBT as represented in Figure 33. The variation in gate resistance is an equivalent to a variation in commutation current slopes.

a) b)

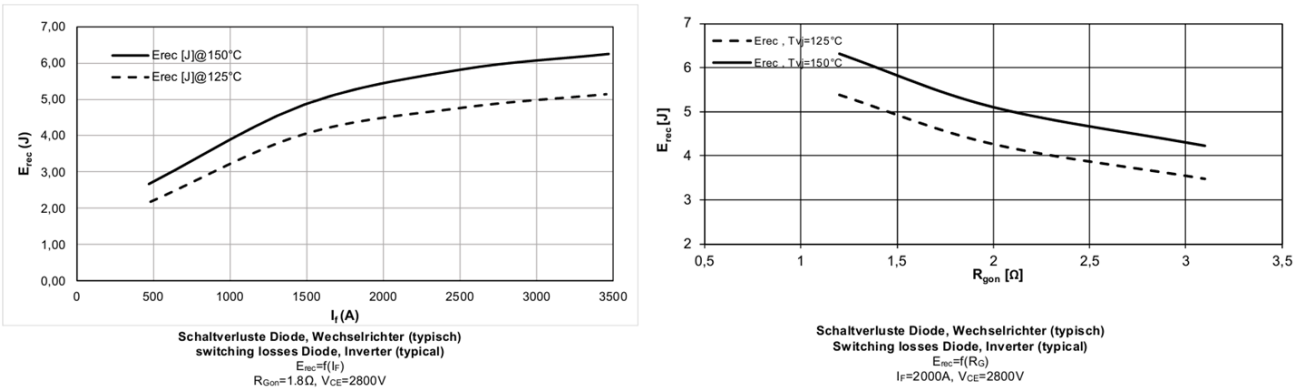


Figure 33: Reverse recovery energy per pulse as a function of

a) Diode conducting current and b) gate resistance

4.5 External Freewheeling Diodes

For external Freewheeling Diodes (FWDs) different diameters of devices are available. In Figure 34 a list of suggestions for different FWDs to be used with Press Pack IGBTs for different applications

Application	Topology	P2000DL45X168	P3000ZL45X168	P5000ZL45X202
HVDC / FACTS	Half Bridge FWD	Internal	D2700U / D3900U	D5000U
	Full Bridge FWD	Internal	D2700U	D2700U
MV Drive	3L-FWD	Internal	D1600U / D2700U	D2700U
	3L-NPC-Diode	D1031SH	D1031SH	D1031SH

Figure 34 Suggestion of different FWDs for PPIs

For further information refer to the datasheet of the FWD on www.infineon.com

5 Datasheet mechanical parameters Press Pack IGBT

This part covers electrical topics related to the mechanical construction of the Press Pack IGBT.

5.1 Clamping Force F

The force for the mechanical mounting of the Press Pack IGBT is specified in the datasheet as noted in Figure 35 These values are important to ensure the proper thermal resistance of the device to the heat sinks.

The clamping force given in the data sheet is necessary for perfect electrical and thermal contact of devices. It must be largely homogeneous across the contact surfaces.

The limits of the clamping force for devices in disc housings are given in the data sheet. These have to be precisely observed. Deviations may alter the data and require special agreement.

Anpresskraft clamping force		F	50…80	kN

Figure 35: Clamping Force requirements

The clamping force selected should be in the top third of the specified force range. This should ensure that even in the case of minimum expansion and compression processes with the materials employed, the level of force does not fall below the minimum requirement.

The clamping force leads to a pressure to the contact area with counter bearing. The pressure must be almost the same to avoid the chips in the multi chip set working with different operating parameters (e.g. differences in conduction resistance and temperature). The pressure calculation needs to be done for 0.8 of the contact area. That is the contact area with counter bearing by the chips. The maximum allowed deviation in pressure between chips is 2 MPa. That value derives mainly from the allowed change in R_{thJC} between the Chips. The minimum required pressure for one chip position is 4 MPa. The maximum allowed pressure for one chip position should not be more than 10 MPa.

That value derives from the height tolerance of the chips and the concept to compensate that tolerance in the multi chip set up.

The PPI is in general from perfect flatness due to conditioning during production process. The PPI flatness can not be measured in the unclamped state.

The flatness of other components in the system (heatsinks, conduction bars, FWD's) bothers the proper pressure distribution. The flatness requirements to those parts needs to be fulfilled (flatness under the pressure used in the application). The flatness of the free-wheeling diode is a special case. The cold welding process for the diode housing results in housing tension. In the unclamped state, the flatness deviation can be up to 40 µm. This is corrected again under pressure.

Please see also chapter 5.5

5.2 Weight

The typical weight of the product, without packaging materials, are given in the datasheet.

Gewicht weight		G	typ. 3000	g

Figure 36: Weight

5.3 Creepage and Clearance Distance

The creepage distance between collecor and emitter or collector and gate is defined according to DIN VDE 0110

Kriechstrecke creepage distance			typ.	35	mm
Luftstrecke Clearance distance			typ.	12	mm

Figure 37: Creepage and Clearance Distance

5.4 Vibration resistance

The values given follow DIN IEC 60068, part 2-6.

Schwingfestigkeit vibration resistance	f = 50 Hz		50	m/s²

Figure 38: Vibration resistance

5.5 Interface definitions

To ensure the best thermal behavior of the Press Pack IGBT we recommend to define the interface materials attached to the emitter and collector as follows:

5.5.1 Surface Finish, Roughness, Average Roughness, Rz

According to DIN EN ISO 1302 Rz 6,3

5.5.2 Flatness

According to ISO 1102, ASME Y 14.5 0.01 mm (10µm)

5.5.3 Thermal interface material

We propose cleaning the interface areas with Kontakt 60

http://www.kontaktchemie.com/KOC/KOCproductdetail.csp?product=KONTAKT%2060

5.6 Outline

The outline given in the datasheet presents the latest mechanical parameters. All data are given in mm, the height of the device is fixed for minimum force defined in the datasheet.

5.6.1 Gate Leads

For the gate leads a coaxial cable type RG58 is used. As the gate leads are fixed to the PPI already, they should be handled with care. The radius for bending must be >=25mm and the maximum pulling force given to the gate leads must be <= 10N at max angle of 45° in each direction. The temperature range for the gate leads is -30°C-70°C.

At the outer end connectors for M4 screws are prepared, for easy connection to the trigger board.

6 Symbols and Terms

Symbols and terms used in this document are part of the standards specification as listed below:

Symbols	Terms
A	Anode
C	Capacitance, collector
$C_{o(er)}$	Effective output capacitance, energy related
$C_{o(tr)}$	Effective output capacitance, time related
C_{ies}	Input capacitance
C_{oes}	Output capacitance
C_{res}	Reverse transfer capacitance
C_{th}	Thermal capacitance
C_{DS}	Drain-Source capacitance
C_{GD}	Gate-Drain capacitance
C_{GS}	Gate-Source capacitance
C_{Mi}	Miller capacitance
C_{σ}	Stray capacity
D	Pulse duty factor/duty cycle D = tp/T
di_F/dt	Rate of diode current rise
di/dt	Rate of current rise general
di_{rr}/dt	Peak rate fall of reverse recovery current
dv/dt	Rate of diode voltage rise
E	Energy
E_A	Avalanche energy

E_{AR}	Avalanche energy, repetitive
E_{AS}	Avalanche energy, single pulse
E_{off}	Turn-off loss energy
E_{on}	Turn-on loss energy
F	Freqeuncy
F	Force
G	Gate
G_{fs}	Transconductance
I	Current
i	Current, instantaneous value
I_{AR}	Avalanche current, repetitive
I_D	DC drain current
I_{Dpuls}	DC drain current, pulsed
I_{DSS}	Drain cutoff current
I_{DSV}	Drain cutoff current with gate voltage applied
I_C	Collector current
I_{CM}	Peak collector current
I_{CES}	Collector cut-off current, gate-emitter short-circuited
I_{CRM}	Repetitive peak collector current
I_{Cpuls}	Collector current, pulsed
I_G	Gate current

Symbols	Terms
I_F	General diode forward current
I_{FSM}	Diode current surge crest value 50 Hz sinusoidal
$I_{c\ nom}$, I_c	Continuous DC collector current
I_{GSS}	Gate-Source leakage current
I_{RM}	Diode peak reverse recovery current
I_{SM}	Inverse diode direct current, pulsed
I_{GES}	Gate leakage current, collector-emitter short-circuited
I_L	Current through inductance
I_{RRM}	Maximum reverse recovery current
K	Cathode
L	Inductance
L_L	Load inductance
L_p	Parasitic inductance (e.g. lines)
L_σ	Leakage inductance
P_{AV}	Avalanche power losses
P_{sw}	Switching power losses
P_{tot}	Total power dissipation
P_{con}	Conducting state power dissipation
Q_G	Gate charge
Q_{GS}	Charge of Gate-Source capacitance

Q_{GD}	Charge of Gate-Drain capacitance
Q_{Gtot}	Total Gate charge
Q_{rr}	Reverse recovery charge
$R_{DS(on)}$	Drain-Source on state resistance
R_G	Gate resistance
R_{Gint}, r_g	Internal gate resistance
R_{GE}	Gate-emitter resistance
R_{Gon}	Gate-turn on resistance
R_{Goff}	Gate-turn off resistance
R_{GS}	Gate-Source resistance
R_i	Internal resistance (pulse generator)
R_L	Load resistance
R_{thCH}	Thermal resistance, case to heat sink
R_{thHA}	Thermal resistance, heat sink to ambient
R_{thJA}	Thermal resistance, junction to ambient
R_{thJC}	Thermal resistance, junction to case
R_{thJS}	Thermal resistance, junction to soldering point
S	Source
T	Cycle time; temperature
T_A	Ambient temperature
T_C	Case temperature

Symbols	Terms
t	Time, general
t_1	Instant time
$t_{d\ off}$	Turn-off delay time
$t_{d\ on}$	Turn-on delay time
t_f	Fall time
T_j	Chip or operating temperature
t_p	Pulse duration time
$T_{vj\ max}$	Maximum junction temperature
$T_{vj\ op}$	Temperature under switching condition
t_{off}	Turn-off time
t_{on}	Turn-on time
t_r	Rise time
t_{rr}	Reverse recovery time
T_{stg}	Storage temperature
T_{sold}	Soldering temperature
V	Voltage, instantaneous value
V_{IN}	Drive voltage
$V_{(BR)CES}$	Collector-emitter breakdown voltage
$V_{(BR)DSS}$	Drain-Source Avalanche breakdown voltage
V_{CC}	Supply voltage

V_{CE}	Collector-emitter voltage
V_{CES}	Collector-emitter voltage, gate-emitter short-circuited
V_{CEsat}	Collector-emitter saturation voltage
V_{CGR}	Collector-Gate voltage
V_{DD}	Supply voltage
V_{DGR}	Drain-Gate voltage
V_{DS}	Drain-Source voltage
V_F	Diode forward voltage
V_{GE}	Gate-emitter voltage
V_{GES}	Gate-emitter voltage, collector-emitter short-circuited
$V_{GE(th)}$	Gate-emitter threshold voltage (IGBT)
V_{GS}	Gate-Source voltage
V_{GSth}	Gate threshold voltage
V_{SD}	Inverse diode forward voltage
$V_{plateau}$	Gate plateau voltage
Z_{thJA}	Transient thermal resistance, chip to ambient
Z_{thJS}	Transient thermal resistance, chip to solder point
Z_{thJC}	Transient thermal resistance, chip to case

7 References

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