Application Note AN-1121

Practical layout for Current Sensing Circuit of IRMCF300 Series IC

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Table of Contents

Page

1. Overview 2
2. Space Vector PWM and Single Shunt Current Reconstruction 3
3. Current Feedback Circuit with IRMCF300 9
4. Test Results 11
5. Summary 14

This application note provides practical tips on printed circuit board layout and how to set configuration registers when using the IRMCF300 series of sensorless motor control IC's. The control IC reconstructs the motor winding currents by sampling the current flowing in the inverter DC link. The IRMCF300 series IC's include the amplifiers, A/D and timing circuits required for motor current reconstruction. Careful design of the current feedback circuit layout will minimize noise and provide a high quality current measurement. Configuration registers in the IRMCF300 series IC's allow fine tuning of the sampling instants to maximize the fidelity of the measurement. The application note describes operating principles, practical implementation and test results.

1. Overview

IRMCF300[1] series digital control IC's are part of iMOTION integrated design platforms for appliance motor control. This digital IC can control motors without motor position sensors. IR's embedded Motion Control Engines enables customers to achieve reliable sensorless field oriented motor control without significant software development effort. The motion control peripherals include a space vector modulator to control the three phase voltages applied to the motor. The IC also employs a single shunt current reconstruction circuit to minimize external analog and digital circuitry. The integrated design platform includes an integrated power module that combines six IGBT power transistors with the high voltage integrated circuit (HVIC) to drive the IGBT gates. The HVIC also implements inverter over-current protection using the same shunt used for motor current measurement.

In order to implement sensorless field oriented control, it is crucial to measure the motor winding currents precisely. The single shunt current reconstruction method derives all necessary current feedback by sampling the currents in the DC link shunt resistor thus eliminating the need for isolation circuits or magnetic current sensors. The space vector modulator generates sample timing signals based on the power inverter state. The IC integrates the A/D converter and amplifier to sample the voltage across the shunt resistor. This is a very cost effective solution but under certain operating conditions the DC link current pulses may become too narrow to guarantee reliable extraction of winding current data. This application note describes the IC features to help overcome these difficulties along with circuit layout techniques needed to maximize signal to noise.

[1] Throughout this document, the IRMCF300 will refer to any one of the five digital control IC's in the IRMCF300 family. This includes the IRMCF312, IRMCF311, IRMCF343, IRMCF341 and IRMCF371.

2. Space Vector PWM and Single Shunt Current Reconstruction

Space vector modulation is a technique to generate the power inverter switching signals based on the desired three phase voltage output. Each leg of the power inverter can connect the load to either the positive or negative DC bus. In one active inverter state, the switches connect one winding to the positive rail and the other two windings to the negative rail. In this instance, 2/3 of the bus voltage is across one winding and 1/3 of the voltage is across the other phase windings. In another active state, the switches connect two windings to the positive rail and the other winding to the negative rail. In the zero vector states, the switches connect all three windings to either the positive or the negative rail. Figure 1 shows the six active vectors and two zero vectors available using three inverter switches. It also shows that switching between two active inverter states can produce any specified inverter voltage. For example, to produce voltage V* in the sector 1, the inverter is in state V1 for time T_a and in state V2 for time T_b. The inverter is in a zero vector state for the time remaining in the switching period. Typically half of this time (T_0) is in the V0 state at the beginning of the cycle and the other half of the time is in the V7 state at the end of the cycle. Figure 2 shows the resultant inverter switching signals where voltage vectors V0, V1, V2 and V7 are applied for time periods T_0, T_a, T_b and T_0. Applying these voltage vectors in the inverse sequence in the second half of the PWM cycle generates symmetrical PWM signals. Since V* is closer to V1 which is aligned with U phase, V1 is applied longer time than V2 (Ta>Tb).

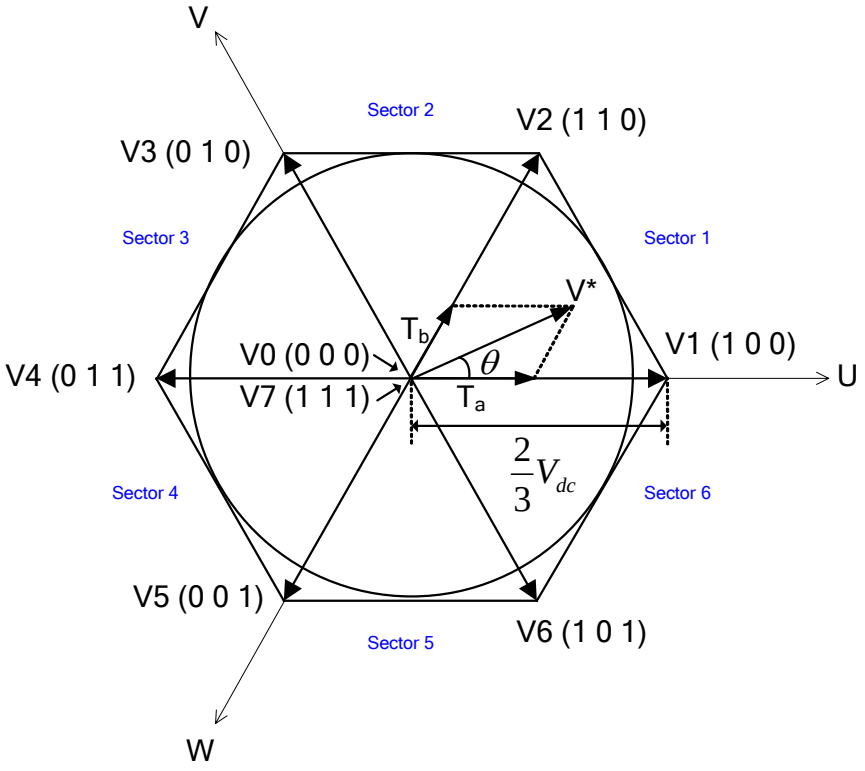


Figure 1. Inverter Output Voltage Space Vectors

The real inverter uses a combination of IGBT or MOSFET transistors and anti-parallel diodes as the power inverter switches. A high voltage integrated circuit provides level shifting between the logic level signal from the digital control IC and the transistors, which switch between the positive and negative DC bus. The polarity of the 'on' signal

may be active high or active low depending on the design of the gate drive HVIC. There must be a delay, so called dead time, between the high side turn-off signal and the low side turn-on signal. This allows the high side power transistor to turn off completely before the low side transistor turns on or vice versa and avoids a shoot through condition that can damage the power devices. The actual gate drive signals include the dead time between all inverter state transitions and so there are six inverter switching signals: PWMUH through to PWMWL in Figure 2. In this case, the gate drive circuit is the IR21363, which accepts active low logic inputs. The modulation circuit typically inserts the dead time but the gate drive circuit can also provide this function. Active high/low gate logic selection is available through a control register, *pwmcfg* on the IRMCF300.

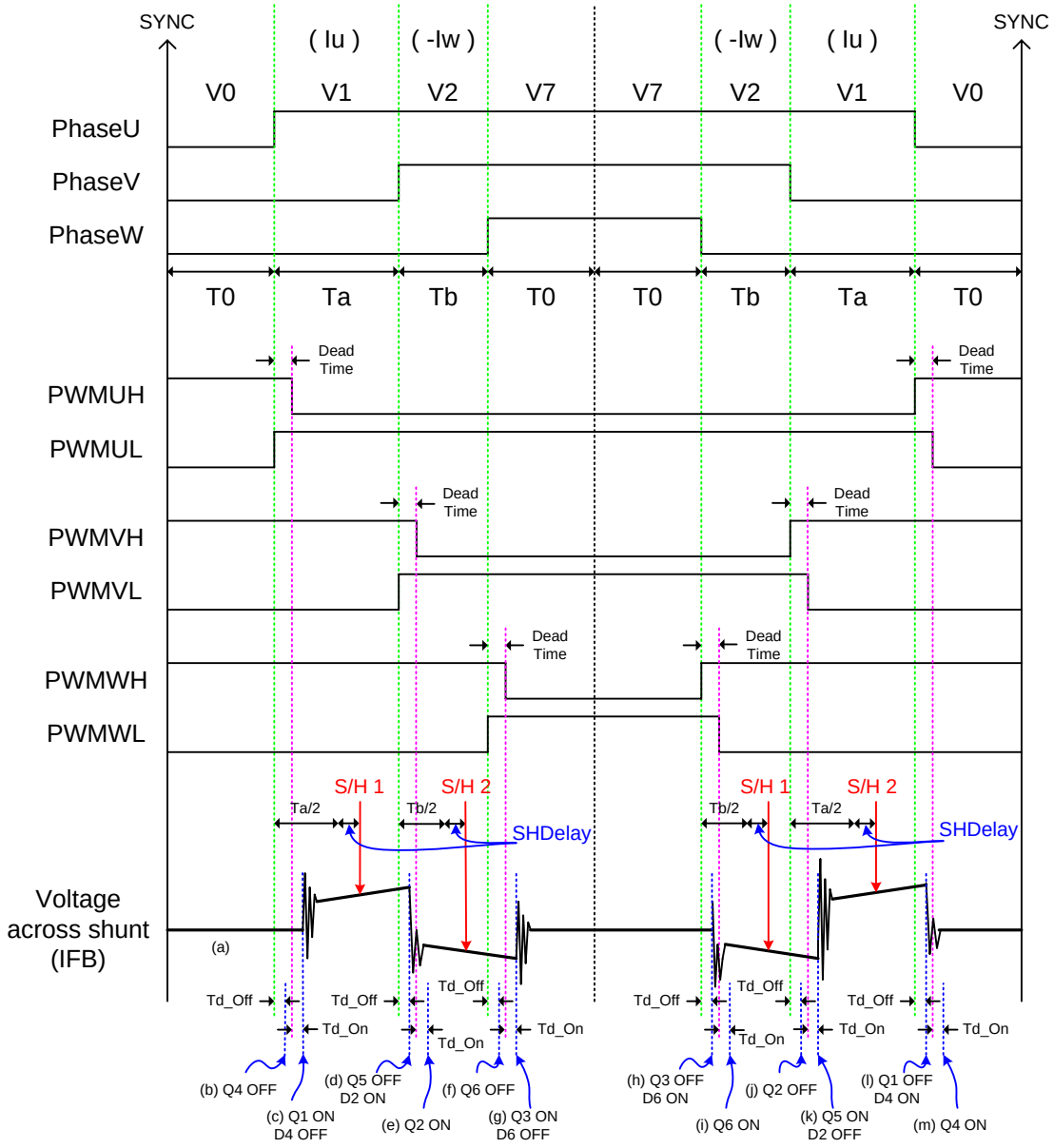
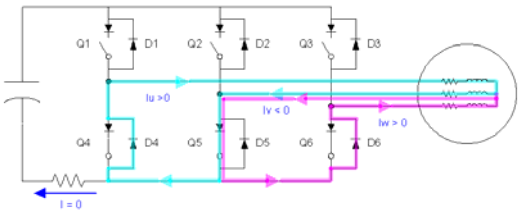


Figure 2. PWM Gate Signals in Sector1

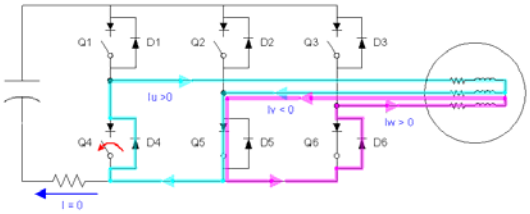
The motor current reconstruction circuit measures the DC link current during the active vectors of the PWM cycle. When the voltage vector V1 is applied, current flows from the positive rails into phase U winding and returns to the negative rail through the V and W phase windings. In this instance, the DC link current flowing from the positive rail equals the U phase current. When the voltage vector V2 is applied, the DC link current returning to the negative rail equals the W phase current. Therefore, in each sector, two phase current measurements are available. The calculation of the third phase current value is possible because the three winding currents sum zero.

The current sampling instant should be at the mid point of the active vector state to sample the average current. This sample instant for the first current sample is at time $T_a/2$ after the start of the first active vector V1. The space vector modulator calculates this timing when it calculates the timing for the gate drive signals. In a symmetrical PWM scheme, there are also two active vectors in the second half of the cycle and so two sets of current measurements are available. Averaging of the two sets of measurement improves the reliability of the current feedback.

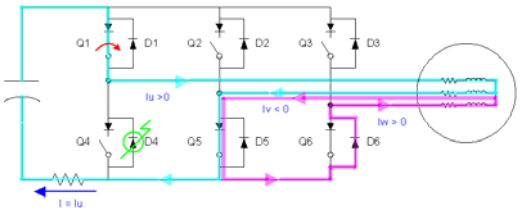
Successful implementation of motor current reconstruction requires detailed knowledge of power inverter operation to account for circuit delays that can result in incorrect current sampling. The error introduced by sampling delays depends on the magnitude of the motor current ripple, which depends on the bus voltage, switching frequency winding inductance and motor back emf. The IRMCF300 includes a sampling delay register, *SHDelay* that allows the system designer to compensate circuit delays to ensure accurate current measurement. The voltage across DC link shunt resistor, IFB, in Figure 2 illustrates how to calculate the sampling delay compensation. Figure 3 illustrates current flow associated with the dead time and each switching instances to display the change of current path and reverse recovery current from the diode. In this example, Iu > Iw > 0 > Iv and the IGBT is modeled as a switch with a diode. Depending on the current direction, sometimes turning on or off the switch doesn't do anything. A thunder mark on a diode indicates the reverse recovery action of the diode.



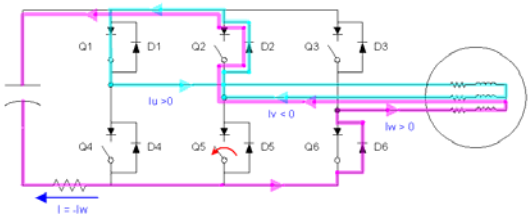
(a) Zero Vector V0



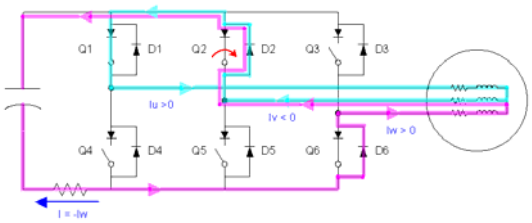
(b) Q4 OFF



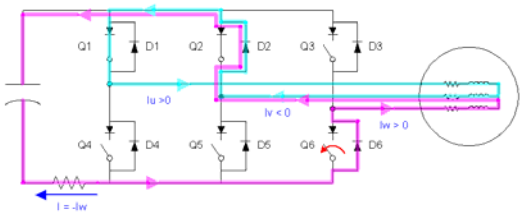
(c) Q1 ON, D4 OFF



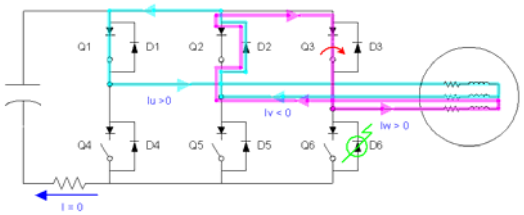
(d) Q5 OFF, D2 ON



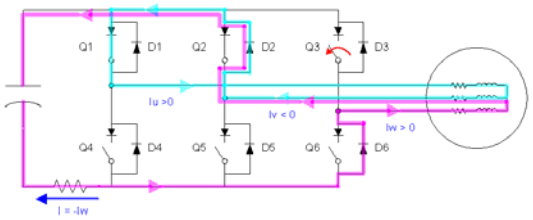
(e) Q2 ON



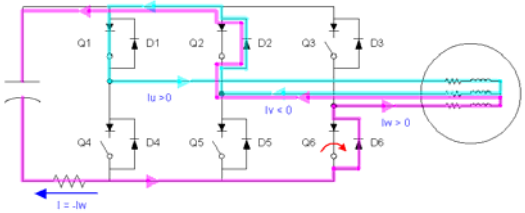
(f) Q6 OFF



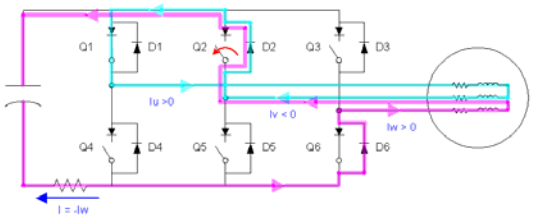
(g) Q3 ON, D6 OFF



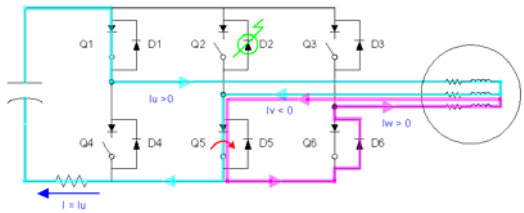
(h) Q3 OFF, D6 ON



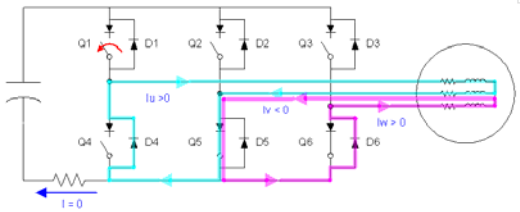
(i) Q6 ON



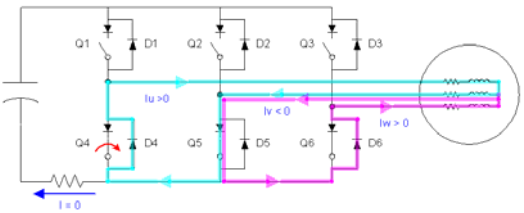
(j) Q2 OFF



(k) Q5 ON, D2 OFF



(l) Q1 OFF, D4 ON



(m) Q4 ON

Figure 3. Current Flow Example in Sector 1

There's a delay between gate driver IC input and output, which is typically 400 ns for IR21363. There's another delay from gate driver output to real switching instance of the device such as IGBT. This is a function of gate charge and gate impedance. It's typically 190 ns on time and 300 ns off time in case of IRAMS10UP60B. Td_On and Td_Off in Figure 2 are the sum of these two delays respectively.

Td_On = gate driver delay + transistor turn on delay = 400 ns + 190 ns = 590 ns
Td_Off = gate driver delay + transistor turn off delay = 400 ns + 300 ns = 700 ns

There is a limitation that one active vector must exist for a minimum time to ensure a reliable sampling of the DC link current. This minimum time is set by the MCE registers TcntMin3Phs for three-phase modulation and TcntMin2Phs for two-phase modulation. This lower bound on the minimum time results in a limitation when modulation index is small or the voltage vector passes an active vector. The areas where problems exist are illustrated in Figure 4.

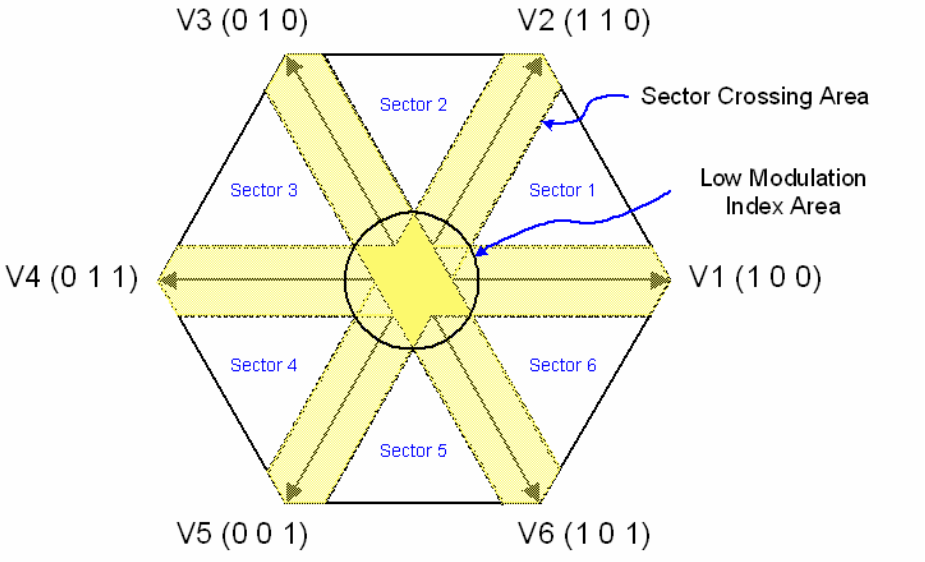


Figure 4. Areas Where Reliable Sampling is Difficult

The minimum time required for reliable current sampling adds undesired voltage distortion, which may cause audible noise especially in low speed operation. In order to minimize this time, it is important to understand when sampling occurs. Ideally, the current sample should occur at the center of the active vector, which results in average value of the current regardless of the slope related to motor inductance. However, as discussed previously, actual switching happens after certain period of time from the edges of PhaseU, PhaseV, and PhaseW. This delay can be as short as Td_Off and as long as dead time plus Td_On. Sampling timings can be adjusted by *SHDelay* register in the way that sampling occurs one half of the active vector time plus *SHDelay* after the edges of PhaseU, PhaseV, and PhaseW. For example, in Figure 2, first sampling instance is Ta/2 plus *SHDelay* after the rising edge of PhaseU. In case of IRAMS10UP60B, Td_On is 590 ns and Td_Off is 700 ns, and dead time can be 400 ns. Real switching instance happens either Td_Off or Td_On plus dead time after the edge of PhaseX. Thus, *SHDelay* can be set to cover worse case as follows.

SHDelay = Td_On + dead time **(1)**

Since sampling should be done after the ringing settles down even in the case of minimum pulse, one condition for sampling delay from the edge can be driven as below.

minimum pulse /2 + SHDelay > dead time + Td_On + ringing time **(2)**

The left hand side is sampling delay in case of active vector with minimum pulse and the right hand side is actual delay time required to sample without noise.
From (1) and (2), minimum pulse can be driven as

minimum pulse > 2 * ringing time **(3)**

Remember that (1) to (3) are mid point sampling case. If the slope of current is not steep, delaying the sample instance further to the end of the active vector can reduce the minimum pulse. Because the switching of the next "PhaseX" edge also has at least Td_Off (or sometimes even dead time plus Td_On) to have a real switching instance, minimum pulse can be as small as following equation.

minimum pulse = dead time + Td_On + ringing time - Td_Off **(4)**

This can be put into (2) to get the proper *SHDelay*.

(dead time + Td_On + ringing time - Td_Off) / 2 + SHDelay
> dead time + Td_On + ringing time **(5)**

SHDelay = (dead time + Td_On + ringing time + Td_Off) / 2 **(6)**

If motor inductance is small and sampling should be done at the center, Equation (3) and (1) need to be used to get the minimum pulse and SHDelay. If application requires shorter minimum pulse and slope of the shunt voltage is not steep due to relatively high inductance of the motor or small DC bus voltage, equation (4) and (6) can be used. Keep in mind that Td_On and Td_Off can vary depending on the operating condition. Actually it's possible to reduce minimum pulse by adjusting sampling point to be in the middle of ringing measured by scope because timing of ringing is consistent if the operating conditions are the same. But it's not recommended because this timing varies as operating conditions change.

3. Current Feedback Circuit with IRMCF300

IRMCF300 series IC has necessary circuit to implement single shunt current feedback including built-in operational amplifiers, sample/holds, and multiplexers. Sampling timing is determined by PWM logic automatically. Only thing user needs to do is to add some resistors and capacitors in order to configure the internal operational amplifier as a differential amplifier and adjust minimum pulse width and sampling instances to optimal ones by setting parameters such as TcntMin3Phs and SHDelay

Figure 5 shows the example of this differential amplifier circuit. Rsh is the shunt resistor in the negative DC link and the voltage across this shunt resistor (displayed as IFB in Figure 2) is used as input to the amplifier. Amplifier gain R5 / (R1 + R3) should be set appropriately to cover operating range with best resolution. C5 is to stabilize Cmext, which is un-buffered 0.6V, and C4 is for Aref, which is buffered 0.6V reference voltage. C2 and C3 may be required to stabilize the operational amplifier output, IFBO. C3 is 10 pF and C2 is not used for IRMCF341 reference design kit, IRMCS3041. Feedback resistor R5 (=R6) needs to be in the range from 5K to 20K Ohm. AVDD and AVSS are power pins for analog circuit and need decoupling capacitors 0.1 µF and 0.01 µF in parallel.

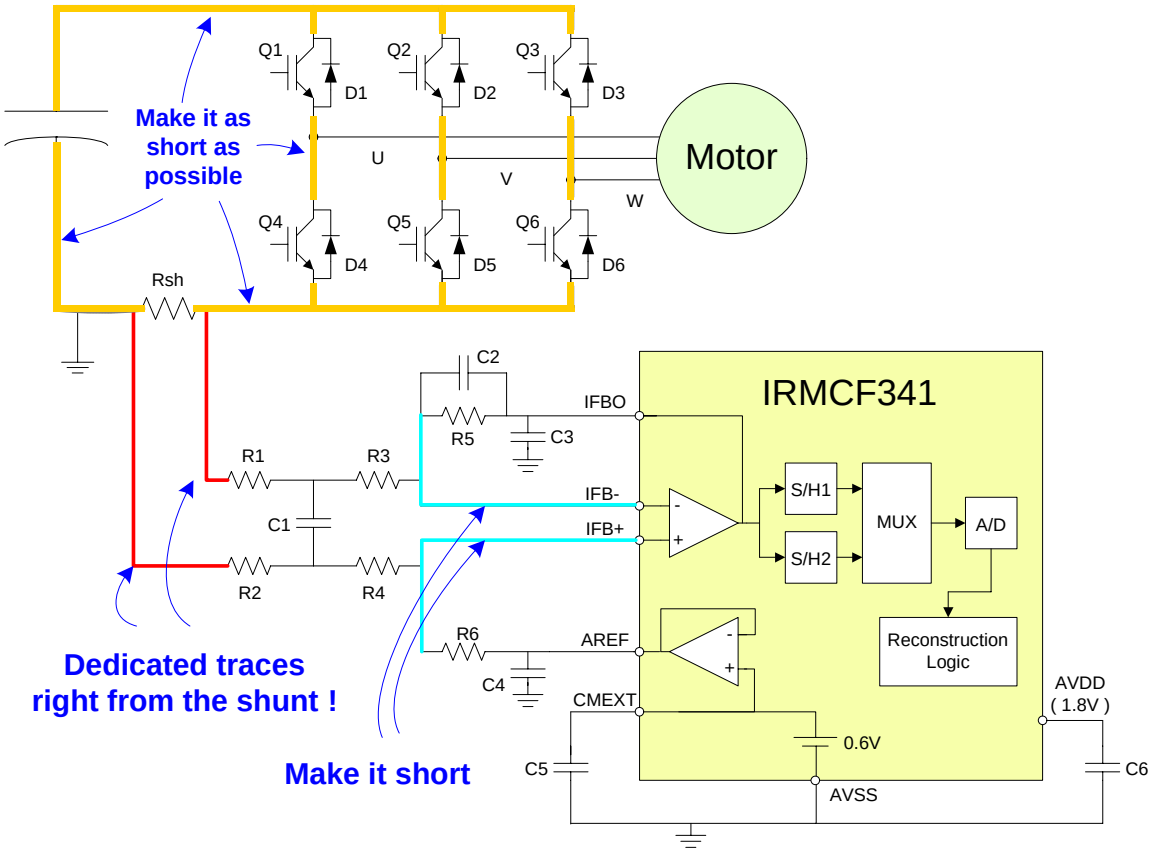
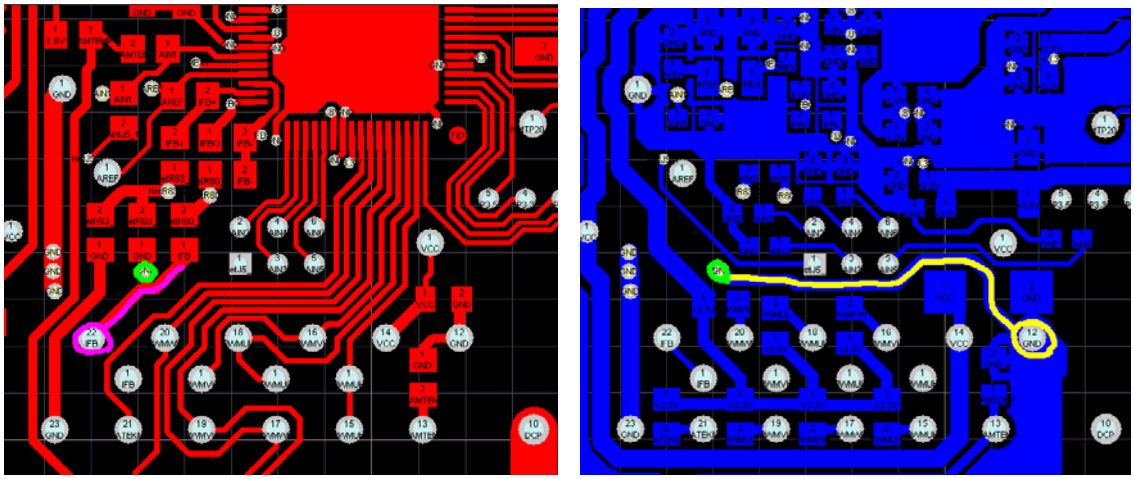


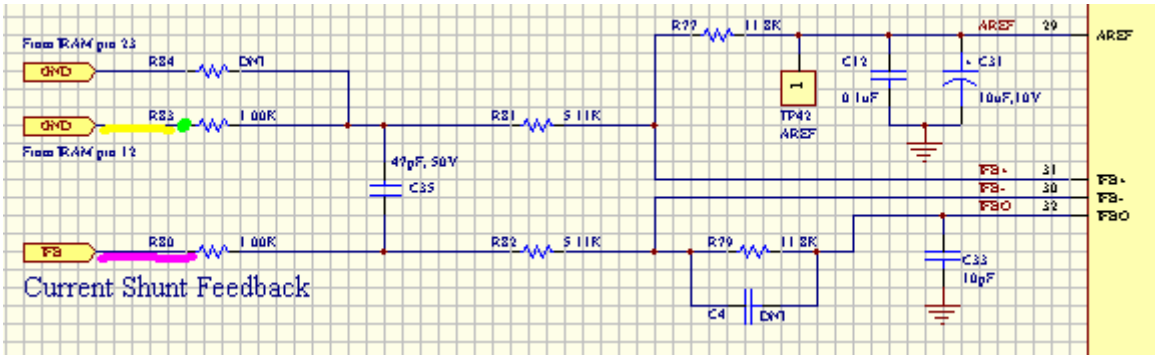
Figure 5. Current Feedback Circuit for IRMCF341

Layout for the single shunt current feedback should be done very carefully. Most important thing is to use dedicated traces right from the shunt resistor to the resistors of amplifier. Traces must not be shared with ground planes. Another important thing is to

make the traces among IGBTs and DC bus capacitors as short as possible. The stray inductances on these traces increase the amount of spike voltage at the switching instances. Figure 6 is a layout example from IRMCS3041. On the bottom layer, a trace starts right from the pin 12 of IRAMS10UP60B without sharing with ground, negative DC bus.



(a) Top Layer (b) Bottom Layer



(c) Schematic

Figure 6. IRMCF341 Reference Board Layout

Another very important fact is that noise from switching power supply may significantly influence the current feedback. It is recommended to separate IRMCF300 ground not only from the main power ground but also from the power supply primary side ground.

Internal operational amplifiers are specifically designed for this application. It has high gain, bandwidth, and slew rate to respond to the rapid rise of current through shunt resistor. Sample/hold actually tracks the signal and then holds to reduce the sampling time. For more information regarding characteristics of operational amplifiers, sample/hold and A/D converter, please refer to the datasheet of IRMCF300 IC.

4. Test Results

Figure 7 shows the real waveforms for V* in sector 1 of Figure 1. Channel 1 is voltage across the shunt resistor and others are low side gate signals. U phase current (Iu) is positive during vector V1 and negate of W phase current (-Iw) is negative, which means W phase current is positive.

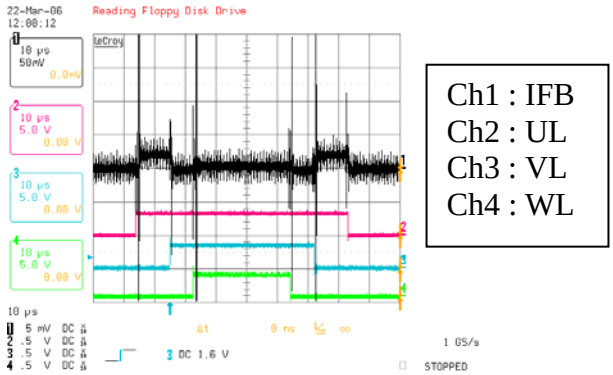
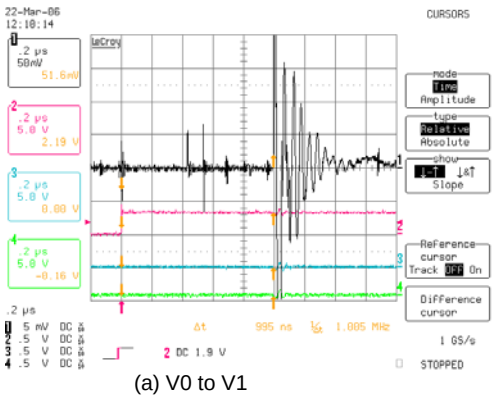
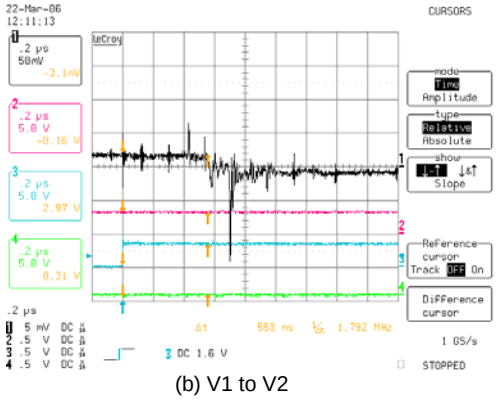


Figure 7. Waveforms in Sector 1

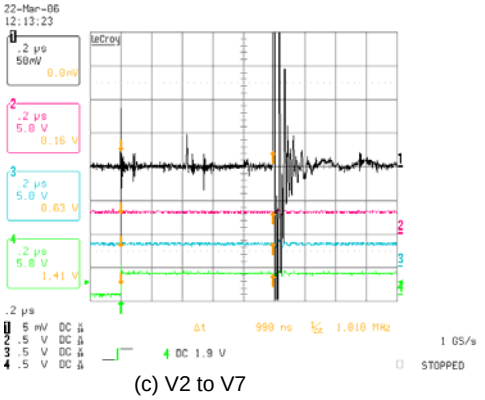
Figure 8 is a collection of waveforms when active vector changes. It will be better to understand together with Figure 2 and Figure 3. It can be observed that ringing is most severe at the transition from V2 to V1 in which case the biggest amount of current is flowing through D2 and therefore reverse recovery is also most significant.



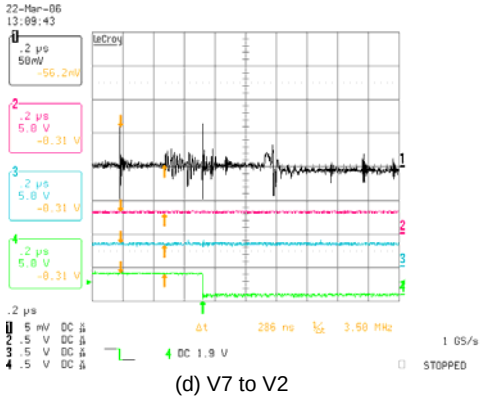
(a) V0 to V1



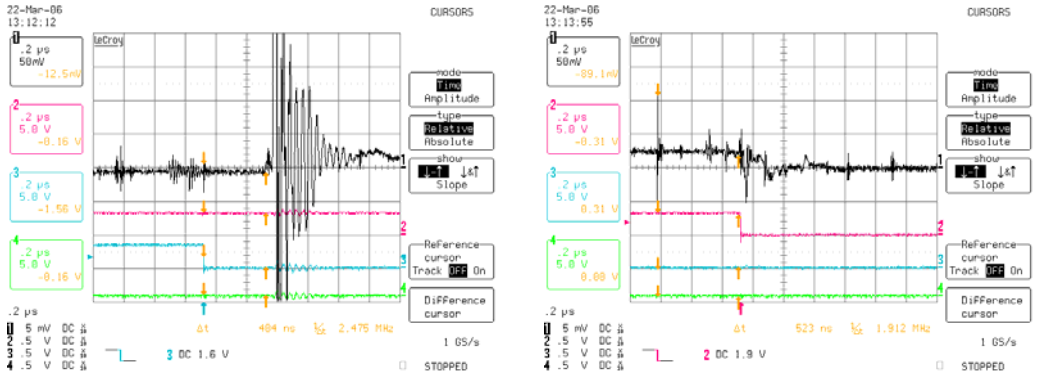
(b) V1 to V2



(c) V2 to V7



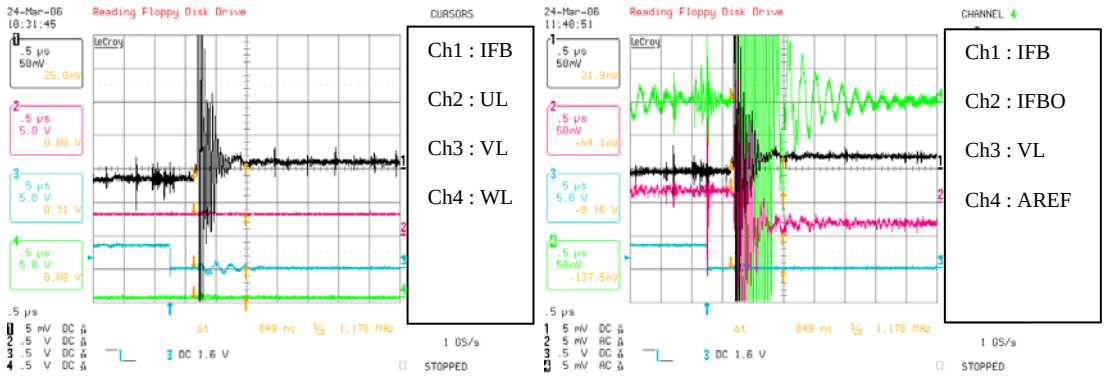
(d) V7 to V2



(e) V2 to V1 (f) V1 to V0

Figure 8. Vector Transition Waveforms in Sector 1

Figure 9(a) is to measure the longest ringing time at the transition from V2 to V1. High frequency noise stops within 0.6 µsec, but there's also slow component ends in 0.85 µsec. However, operational amplifier output (IFBO) is the one needs attention here because this is the input to the sample/hold. Figure 9(b) shows IFBO and AREF together with IFB. Some slow component noise in AREF is reflected into IFBO. This ripple ends in 1.25 µsec.



(a) IFB at V2 to V1 (b) IFBO and AREF

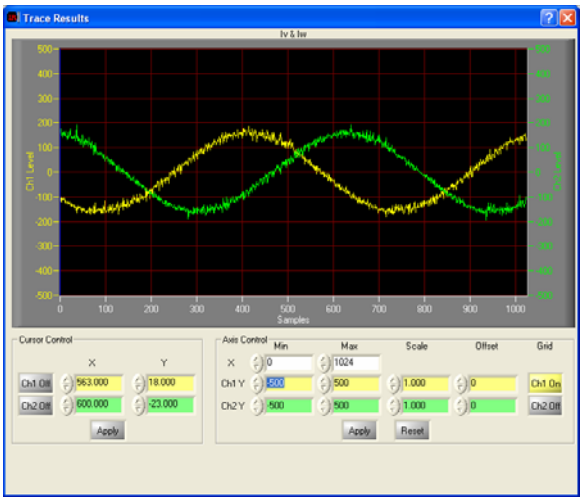
Figure 9. Ringing at Transition from V2 to V1

When dead time is set to 500 ns, equation (1) and (3) give

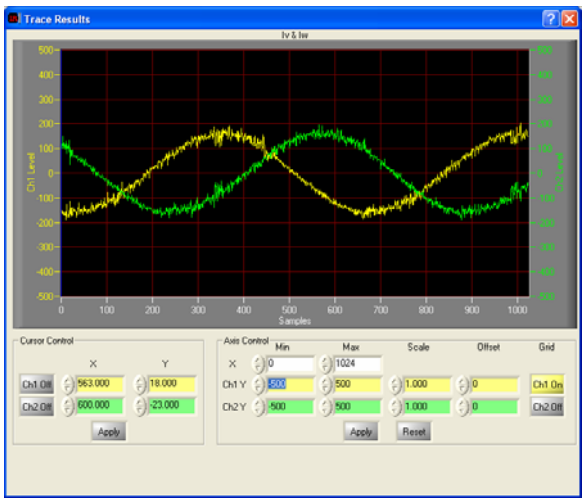
SHDelay = Td_On + dead time = 590 ns + 500 ns = 1.1 µsec

minimum pulse = 2 * ringing time = 2 * 1.25 µs = 2.5 µsec

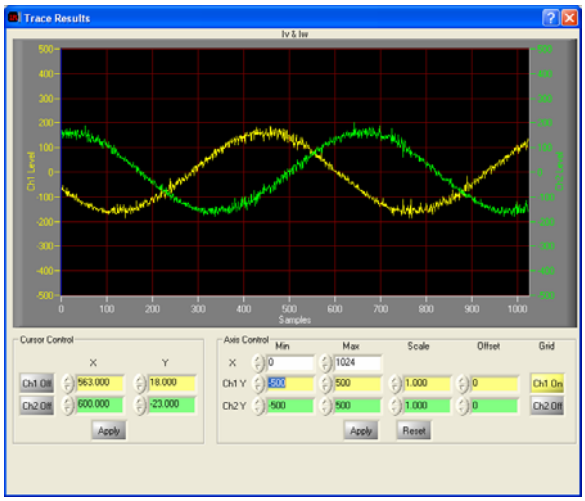
Figure 10(a) is a trace buffer plot from MCE Designer for this case. Figure 10(b) is a plot when *SHDelay* is 1.1 µsec and minimum pulse is 1.5 µsec. Some glitches exist due to slow ripple component.



(a) SHDelay 1.1µs and MinPulse 2.5 µsec



(b) SHDelay 1.1 µs and MinPulse 1.5 µsec



(c) SHDelay 1.5 µs and MinPulse 1.7 µsec

Figure 10. Phase Current Plot from Trace Buffer

From equation (4) and (6),

minimum pulse = dead time + Td_On + ringing time - Td_Off
= 0.5 + 0.59 + 1.25 - 0.7
= 1.64 µsec

SHDelay = (dead time + Td_On + ringing time + Td_Off) / 2
= (0.5 + 0.59 + 1.25 + 0.7) / 2
= 1.52 µsec

Figure 10(c) is a plot for this case and seems as good as 10(a). These plots in Figure 10 verify equations (1) to (6).

5. Summary

Some guidelines for PCB layout associated with IRMCF300 series ICs to extract reliable phase current data from single shunt resistor in the negative DC bus are suggested with practical examples. Also how to set up MCE parameters related to current feedback is explained with equations and proved by trace plots.

In this application note, cable length is not considered because it's rare to have long cables in most case of appliance application. If motor cables become too long, quality of current feedback will deteriorate due to wave reflection.