Powering AD and ADAS applications with smarter, safer and more efficient Infineon OPTIREG™ power stage

OPTIREG™ multiphase DrMOS power stage

About this document

Scope and purpose

Infineon OPTIREG™ TLF12505A Automotive 60 A multiphase DrMOS power stage empowers next-generation vehicles with reliable and efficient power delivery needed for AI-driven Autonomous Driving (AD) and Advanced Driver Assistance Systems (ADAS) by enabling seamless real-time data processing, smart decision making, and energy-efficient performance. They help automotive manufacturers design scalable, sustainable, and future-ready mobility solutions with reduced energy consumption.

Intended audience

The intended audiences for this document are design engineers, technicians, and developers of electronic systems. This application note assumes familiarity with buck converter fundamentals and multiphase topologies, and provides practical implementation guidance for experienced hardware designers working on automotive power delivery networks.

Automotive system engineers who create AI-driven AD and ADAS systems need efficient, reliable power stage solutions. Infineon's power stages [1] empower them to develop smarter, scalable, and energy-efficient systems, accelerating the shift toward a more connected, sustainable, and intelligent future of mobility.

Keypoints

- Demonstrates systematic design methodology for multiphase voltage regulators using integrated DrMOS power stages in automotive applications
- Explains component selection criteria and PCB layout techniques for high-current, low-voltage power delivery optimization
- Describes implementation of integrated current sensing for phase current monitoring and control loop optimization
- Provides thermal management strategies and efficiency optimization using diode emulation mode for light-load conditions

About this product family

Product family

Infineon's OPTIREG™ automotive DrMOS power stages integrate high-performance MOSFETs with optimized gate drivers in a compact package for multiphase voltage regulator applications. This family offers superior power density, integrated current sensing, and comprehensive protection features with AEC-Q100 qualification. The OPTIREG™ power stages support switching frequencies from 100 kHz to 2000 kHz, enabling efficient power delivery for advanced driver assistance systems and autonomous driving platforms.

Target applications

- Automotive AD (Autonomous Driving) compute platforms
- ADAS (Advanced Driver Assistance Systems) modules
- High-performance automotive ECUs
- Infotainment and cockpit domain controllers
- Zonal and central compute architecture

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1 Introduction

Autonomous Driving (AD) and Advanced Driver Assistance Systems (ADAS) leverage AI to process complex sensor data and enable features like adaptive cruise control, lane keeping, object detection, and accident avoidance. AI-powered AD and ADAS applications use high-performance CPUs, GPUs, FPGAs, and increasingly, AI-specific neural processing units (NPUs). These components create substantial power demands due to massive real-time data processing.

This shift presents significant power management challenges. A robust and efficient power delivery network (PDN) is crucial for reliability, safety, and performance of these systems.

This application note provides an overview of the key power stage design considerations for powering modern automotive AD and ADAS.

1.1 The power challenge in the automotive environment

Automotive electronic control units (ECUs) must operate reliably in a harsh electrical environment. The car's 12 V battery is not a stable power source. It is subject to a wide range of transient events as defined by standards like ISO 16750-2. These include:

- **Cold crank:** The battery voltage can drop significantly (as low as 3 V to 6 V) for short periods during engine startup
- **Load dump**: This occurs when the battery is disconnected while the alternator is charging, causing a high-energy voltage spike that can reach 35 V
- **Voltage fluctuations**: Normal operating voltage can vary from 9 V to 18 V depending on the vehicle's electrical load and alternator state

ADAS and PDN must be designed to withstand these events without interruption or damage to sensitive components like the main system on chip (SoC).

The escalating compute load

Cars, these days, are effectively very powerful computers on wheels. The rapid increase in computational performance necessitates high power demands. To manage the resulting thermal density and prevent silicon breakdown, efficient power delivery networks (PDNs) are required, and operating core voltages must mandatorily be below 1 V.

Modern automotive superchips have seen huge leaps in performance expectations, and now routinely target up to 2,000 Tera Operations Per Second (TOPS) of AI compute. Such performance requires specialized chips, and to protect these advanced 7 nm to 3 nm SoCs, scaling to sub-1 V core voltages is imperative to prevent issues such as dielectric breakdown and quantum tunneling as gate oxides reach atomic scales. Because power consumption scales quadratically with voltage ($P \propto V^2$), reducing the supply rail, for example, from 1 V to 0.7 V cuts dynamic power by approximately 50%. This reduction is the primary mechanism for optimizing efficiency and preventing thermal runaway in high-density automotive processors.

In a similar manner, high-end ADAS platforms, which previously drew minimal power, now require between 10 W and >400 W depending on the level of autonomy and integration. But for an electric vehicles, this extreme power demand resulting from the increased compute load is no longer negligible. Level 4 autonomous systems drawing 400–600 W can reduce a vehicle's driving range by as much as 7% to 10%, necessitating aggressive power management and high-efficiency delivery.

OPTIREG™ multiphase DrMOS power stage

Introduction

Here is an illustration of why such high comupting power is needed: To ensure safety during critical manoeuvres such as autonomous emergency braking (AEB) or emergency lane keeping (ELK), ADAS platforms must handle dynamic computational load and real-time execution required for safety-critical functions. These scenarios require nanosecond transient agility to manage massive current surges (~400 A) without compromising GPU stability. Utilizing advanced multiphase regulators is essential to mitigate voltage droop and prevent logic errors during high-speed sensor fusion and optimization algorithms in AD and ADAS.

Automotive power delivery network (PDN) challenges can be mitigated with Infineon's OPTIREG™ TLF12505A Automotive 60 A power stage, an integrated smart power stage that optimizes thermal density, reduces electrical noise, and maximizes efficiency for compact, high-current ADAS processors.

2 The multistage power architecture

In AD and ADAS applications, multistage power architecture is a critical design choice used to ensure high efficiency, reliability, transient response, and thermal management.

2.1 Multistage power delivery network architecture

To address the power challenges in the automotive environment, multistage power architecture is employed as shown in Figure 1. This approach provides cascading levels of protection and voltage regulation.

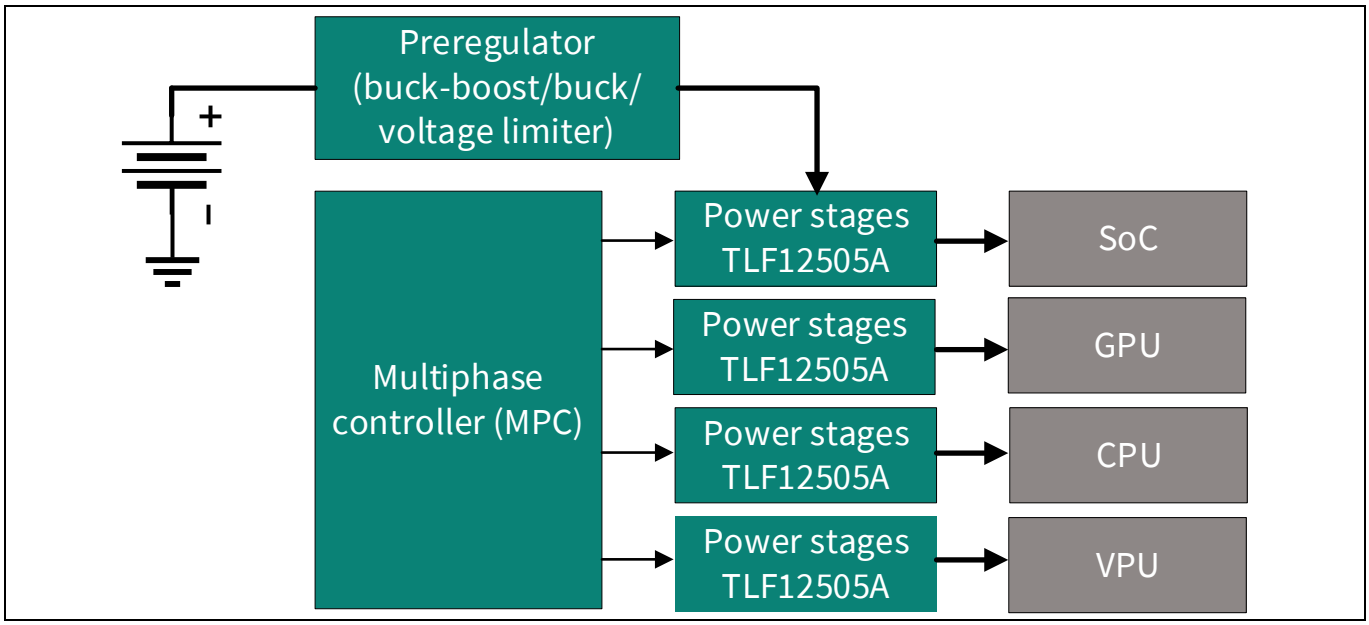


Figure 1 Multistage power delivery network architecture

2.1.1 Stage 1: Preregulator

This is the front end of the PDN. Its primary role is to isolate the ADAS internal circuitry from the car battery's harsh transients. A buck or buck-boost converter is the ideal topology for this stage based on the design specifications. It can efficiently step the voltage up (boost) during cold crank events and step it down (buck) during normal operation and overvoltage conditions. This produces a stable intermediate bus voltage (e.g., 5 V, 9 V , 12 V to 16 V, or 20 V limited) for the subsequent stages. This intermediate bus acts as a buffer, ensuring a continuous and regulated supply despite fluctuations at the battery.

2.1.2 Stage 2: Power stages

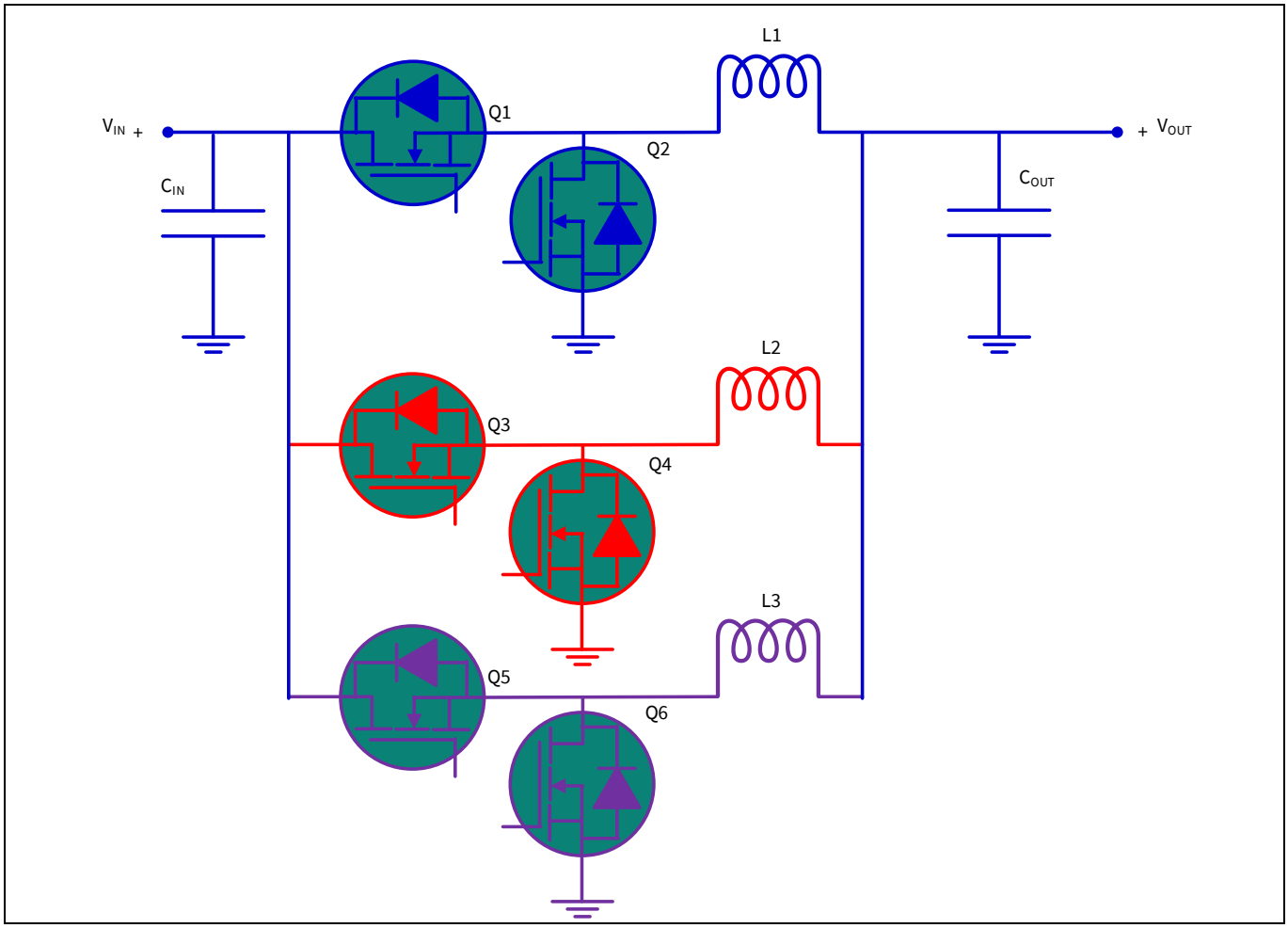
Power stages are intelligent MOSFET half-bridges that embed a driver, diagnosis and protection, and a synchronous buck stage which steps down the vehicle battery voltage to the specific voltage levels required by different ADAS components like GPU, CPU, SoC, VPU, memory, displays, and sensors. A typical power stage integrates low $R_{DS(on)}$ MOSFETs, drive control, current sensing, fault protection, and reporting. This reduces board space, complexity, and bill of materials.

Power stages offer several key advantages:

- **High efficiency:** High-frequency switching power stages are significantly more efficient than linear regulators, reducing heat generation
- **Precise voltage:** Power stages provide a stable, low-noise supply tailored to each component's needs
- **Scalability:** The modular nature of power stages simplifies design and allows for easy adaptation to different system configurations

2.1.3 Interleaved multiphase DC-DC buck converters

Power stages are interleaved to handle high-current and high-power AD and ADAS applications. The main advantages of interleaved operation are the capability of handling high-load transients by artificially increasing the switching frequency and enabling a reduction of output capacitance in high-current and high-power AD and ADAS applications. Figure 2 shows three interleaved buck converters with 120° (360°/number of buck converters) phase offset PWM drive signals.



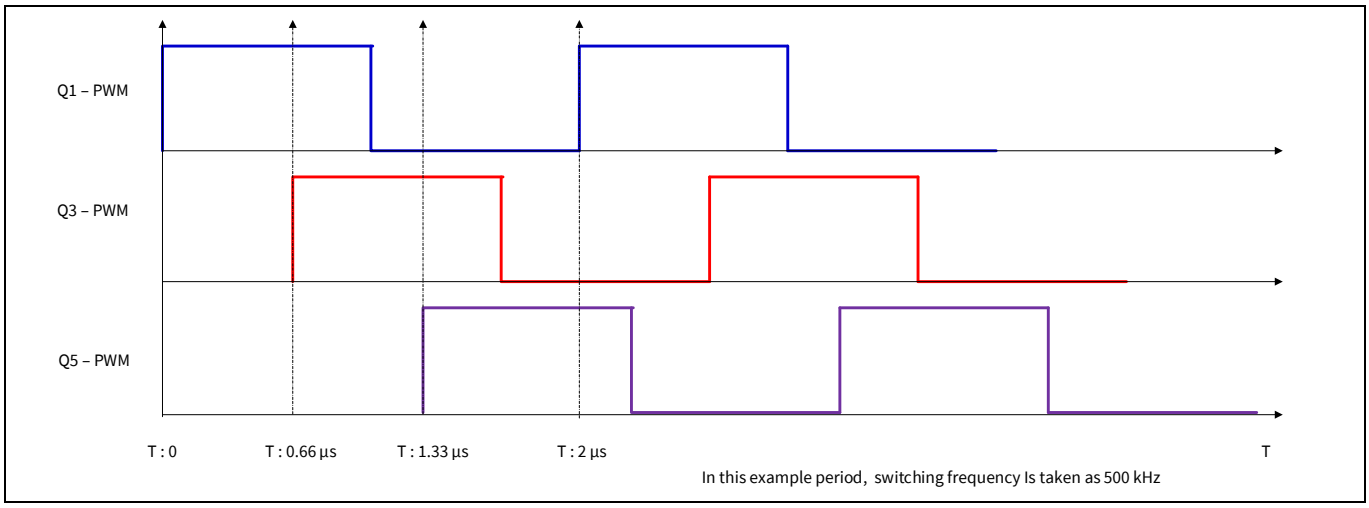


Figure 2 Interleaved multiphase DC-DC buck converters

Interleaved multiphase DC-DC buck converters have several advantages in automotive power stage applications, and here are a few.

Higher efficiency and stability

Multiphase buck converters use multiple interleaved power stages to improve efficiency and reduce ripple. This design distributes the current and making it ideal for high power ADAS applications. For low power conditions, phase-shedding techniques prevent efficiency loss by selectively deactivating phases.

Better thermal performance

Power and heat dissipation are distributed across multiple phases of interleaved buck converter, this decreases thermal stress on individual power stage components by reducing hot spots on components and printed circuit boards, enhancing system reliability and lifespan, essential for automotive operating conditions.

Improved transient response and voltage regulation

Multiphase power stages respond quickly and smoothly to sudden load changes in AD and ADAS, maintaining steady voltage levels for sensitive electronics.

They also provide superior transient response by effectively paralleling inductors during load steps, which reduces equivalent inductance and impedance. This allows for a faster supply of current to the load, minimizing voltage undershoot and overshoot during rapid load changes. Interleaved multiphase converters require fewer capacitors and offer tighter voltage regulation due to phase interleaving and dynamic phase activation.

Reduced EMI

Phase-interleaving lowers current ripple and EMI, which is important to avoid interference with other sensitive automotive systems.

Scalability for complex systems

Interleaved multiphase converters support higher power loads and can scale to meet future growth and added functionalities in evolving ADAS designs.

Power stage redundancy and reliability

The multiphase topology provides inherent redundancy, ensuring uninterrupted power delivery even if a phase is faulty.

Reduced output current ripple

Time-staggered PWM triggering in multiphase buck converters partially cancels ripple components, which reduces output voltage ripple and provides cleaner power rails for sensitive ADAS loads.

Reduced filtering requirements

By reducing ripple and effectively increasing switching frequency, multiphase converters allow the use of smaller inductors and capacitors, saving space and weight, both critical for automotive design.

Higher efficiency

Multiphase designs mitigate the efficiency tradeoffs typically faced when increasing switching frequency in single phase converters by reducing switching and conduction losses.

These benefits make interleaved multiphase buck converters a strong choice for modern automotive ADAS power delivery applications , where high efficiency, power quality, transient performance, and reliability are critical.

A comparison of single-phase and interleaved multiphase power stages is shown in Table 1.

Table 1 Comparison of single phase and multiphase interleaved power stages

Feature	Single-phase power stage	Interleaved multiphase power stage
Efficiency	Lower at higher loads	Higher efficiency at higher loads
Thermal management	Less optimal, higher thermal stress	Better due to even heat distribution across phases
Transient response	Slower dynamic response	Faster, more stable transient performance
EMI control	Higher ripple and EMI	Lower ripple and EMI
Scalability	Limited for high-power requirements	Easily scalable
Complexity	Lower component count and simpler design	More complex, multiple phases
Load handling	Moderate, can face thermal limits	Superior current sharing, reduced thermal burden

3 The new OPTIREG™ TLF12505A

OPTIREG™ TLF12505A DrMOS Automotive 60 A power stage is a highly integrated, 60 A smart power stage designed for automotive DC-DC synchronous buck converter applications. It is optimized for high-frequency operation and is AEC-Q100 Grade 1 qualified for use in harsh automotive environments.

3.1 Introduction

TLF12505A integrates a low-quiescent-current synchronous buck gate driver with control and synchronous MOSFETs. This combination of an optimized package with matched components ensures higher efficiency at the low output voltages required by high-performance CPUs, VPUs, GPUs, and DDR memory. Careful adherence to layout guidelines further enhances heat transfer and minimizes switch node ringing.

TLF12505A features a very accurate current mirror architecture on both high-side and low-side MOSFETs, thus reporting the real-time current information. The current information is reported using the IMON pin. The reported current is in the form of current output with a gain of 5 µA/A from the IMON pin. To convert the current into a voltage, a 1 kΩ, 0.1% resistor must be placed between the IMON and IMONREF pins. This resistor must be positioned close to the multiphase controller (MPC). The resulting differential voltage from this resistor provides the reported current information to the MPC.

Protection includes power stage temperature reporting and overtemperature protection features (OTP with thermal shutdown), cycle-by-cycle overcurrent protection (OCP), negative overcurrent protection, control MOSFET short detection (HSS – high-side short detection), VDRV and bootstrap undervoltage protection. TLF12505A also features a “refreshing” of the bootstrap capacitor to prevent it from over discharging.

Operation from 100 kHz to 2 MHz switching frequency enables high-performance transient response, allowing miniaturization of output inductors, as well as input and output capacitors while maintaining industry-leading efficiency in an optimized form factor.

3.2 TLF12505A-based typical single-phase application diagram

TLF12505A is an integrated smart power stage intended for use in automotive AD and ADAS systems. A typical single-phase application is illustrated in Figure 3.

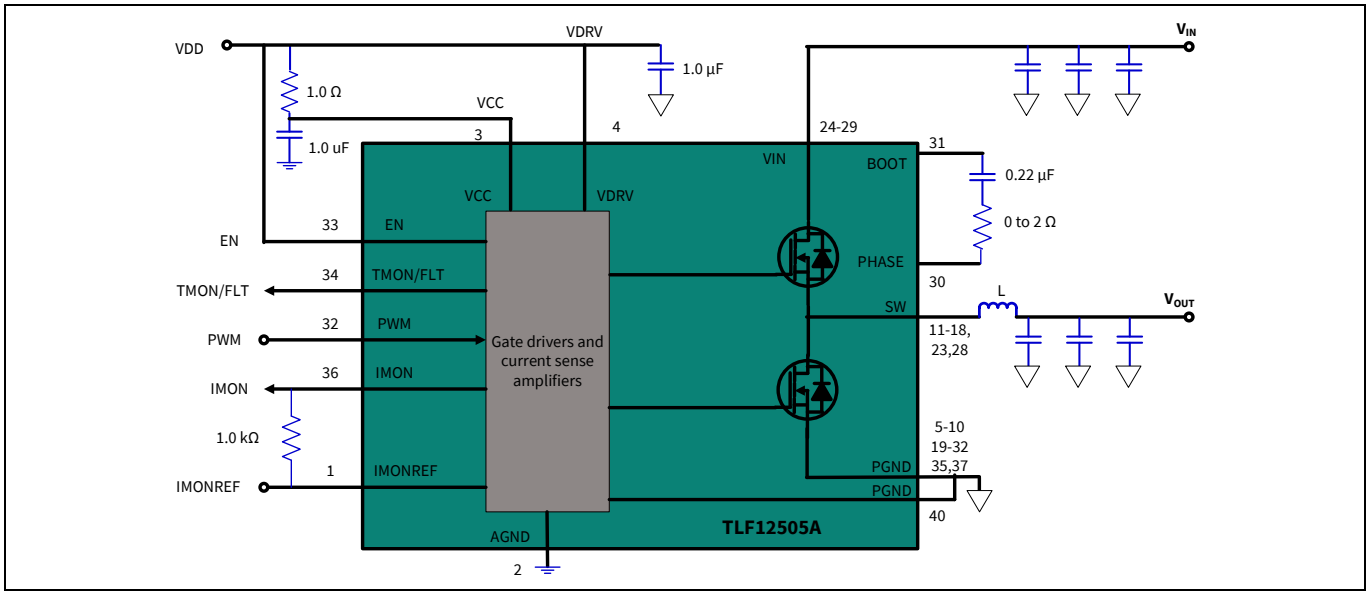


Figure 3 TLF12505A-based typical single-phase application diagram

3.3 TLF12505A simplified block diagram

TLF12505A contains a high-speed MOSFET driver, optimized to drive a pair of co-packaged high-side and low-side OptiMOS™ MOSFETs at frequencies up to 2 MHz.

TLF12505A features advanced current mirror sensing for superior accuracy. By mirroring current from both MOSFETs to an integrated sense element, it provides inherent temperature compensation and enables instantaneous responses to load steps or overcurrent faults without additional circuitry.

TLF12505A also integrates temperature sensing capabilities for protection and monitoring, all within a compact, optimized package. A simplified block diagram of TLF12505A is shown in Figure 4.

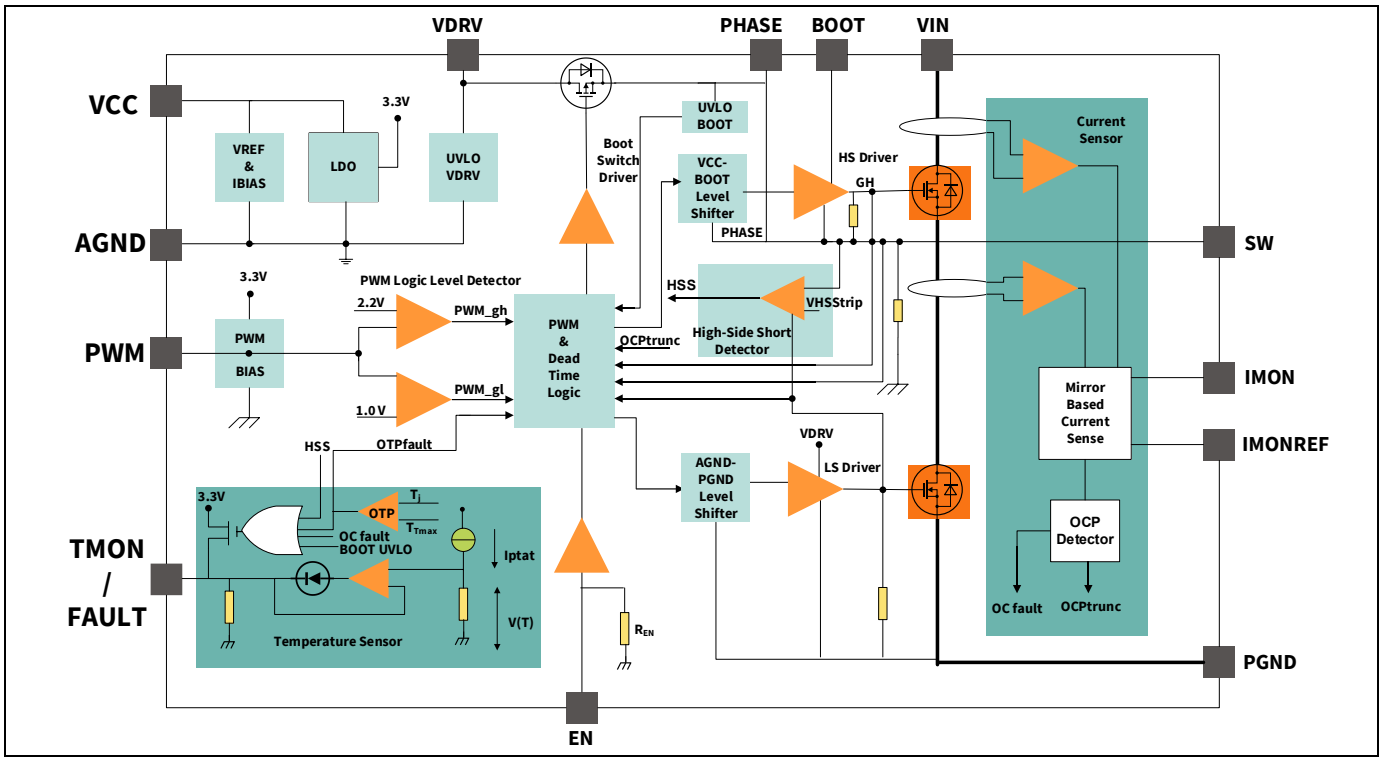


Figure 4 TLF12505A simplified block diagram

3.4 Key features and advantages

Table 2 Benefits of using TLF12505A in improving system design

Characteristic	Features	Benefits
Integrated current sensing	• On-chip MOSFET current mirror architecture for HS/LS sensing • IMON pin with proportional 5 µA/A gain output • Cycle-by-cycle OCP via PWM pulse truncation • Elimination of external sense resistors	• Superior accuracy via inherent temperature compensation • Real-time fault protection for safety and reliability • Simplified board design and reduced BOM costs • Enhanced diagnostics and improved noise immunity
Thermal protection and reporting	• Continuous internal junction temperature monitoring • Analog TMON/FAULT output (8 mV/°C linear reading) • Overtemperature Protection (OTP) shutdown at 155°C • Multifunction fault indicator (High/Low logic)	• Enhanced reliability by preventing thermal runaway • Improved thermal balancing in multiphase systems • Increased longevity (qualified 50% beyond AEC-Q100 Grade 1) • Simplified diagnostics and troubleshooting

Characteristic	Features	Benefits
Integrated gate driver	• Co-packaged MOSFETs (Q1/Q2) and gate driver • High switching frequency (up to 2 MHz) • Diode emulation mode via PWM tri-state • Automatic bootstrap capacitor replenishment	• Reduced component count and board space • Compact solution ideal for space-constrained ADAS modules • Improved light-load efficiency and transient response • Optimized gate timing and MOSFET matching
Enable/Sleep Mode	• Deep Sleep mode via digital EN pin • Low quiescent current (~32 µA) in sleep • Active mode activation with 17 µs delay	• Simplified power sequencing and inrush current control • Significantly improved efficiency during idle/standby • Critical for battery-powered automotive applications
Body Braking (Protection)	• **Rapid response:** Quickly disables both high-side (Q1) and low-side (Q2) MOSFETs upon receiving a tri-state signal • **High impedance output:** Provides a safe state during fault conditions or abrupt load changes	• **Enhanced transient response:** Prevents unwanted current flow during braking or sudden load shifts, improving overall system stability • **Increased reliability:** Reduces heat generation and thermal stress on MOSFETs, ensuring longevity in harsh automotive environments • **Fault protection:** Protects the system against negative current flow during critical fault conditions
Diode emulation mode (also see Section 3.5)	• **Automatic Q2 control:** Disables the low-side MOSFET as inductor current approaches zero • **PWM tri-state driven:** Controlled directly via the standard tri-state input from the PWM controller • **Integrated logic:** Functionality is fully built-in, requiring no external components or complex circuitry	• **Improved light-load efficiency:** Prevents negative inductor current, eliminating unnecessary conduction and switching losses to conserve battery energy • **Optimized power management:** Supports fine-grained control over power consumption, ideal for automotive platforms like ADAS • **Simplified design:** Reduces PCB size and design complexity by

Characteristic	Features	Benefits
		removing external sensing/logic components

3.5 Diode emulation mode

Diode emulation mode is a feature in TLF12505A that improves efficiency during light load conditions by preventing the negative inductor current. When enabled through PWM tri-state signals from the multiphase controller (MPC), the power stage disables the low-side MOSFET (Q2) as shown in Figure 5 at the point when the inductor current is about to become negative. This makes the low-side MOSFET act like a diode, hence the name “diode emulation”.

In a buck converter's diode emulation mode (DEM), the MOSFET gate driver (MGD) for the low-side MOSFET controls the synchronous MOSFET (Q2) to act like a freewheeling diode. This means it only conducts current in one direction, preventing reverse current flow and significantly improving efficiency at light loads.

TLF12505A uses tri-state PWM from a multiphase controller (MPC) to enable diode emulation, which improves transient performance and reduces low-power dissipation.

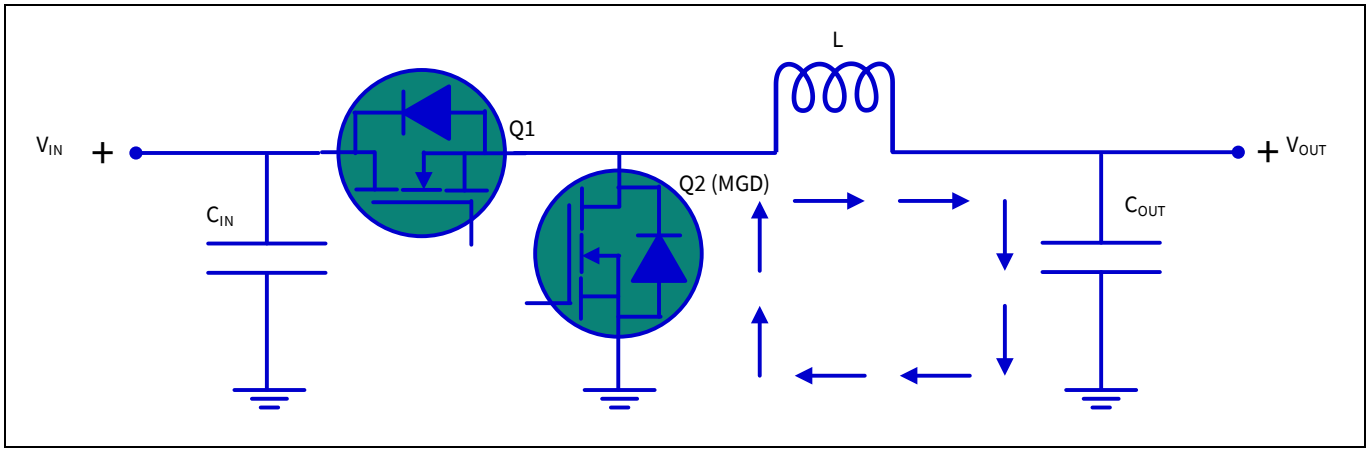


Figure 5 Diode emulation mode

The diode emulation mode in TLF12505A improves light-load efficiency, with the following key features and advantages.

3.5.1 Key features

Improved light-load efficiency: The power stage uses the PWM tri-state input to activate diode emulation. This prevents the negative inductor current by turning off the low-side MOSFET (Q2) when the inductor current approaches zero, preventing conduction losses and boosting efficiency.

Built-in protection (body braking mode): The system quickly disables both MOSFETs (Q1 and Q2) in response to the tri-state signal. This provides a high-impedance output and protects against negative current flow during fault conditions.

Integrated, space-saving solution: The diode emulation function is fully integrated into the power stage, eliminating the need for external components and reducing design complexity.

Simplified control: The function is controlled directly by the standard tri-state PWM input, simplifying system-level integration with the PWM controller.

3.5.2 Advantages

Improved light-load efficiency: By preventing negative inductor current, TLF12505A avoids conduction and switching losses and significantly improves efficiency during light load and standby conditions, which conserves battery energy.

Enhanced transient response and stability: The body braking function, which rapidly disables switching devices, helps prevent unwanted current flow during braking or abrupt load changes. This improves the overall stability and transient response of the system.

Increased system reliability: Reducing switching and conduction losses during light-load conditions decreases heat generation and stress on the power MOSFETs. This leads to greater system reliability and longevity in the challenging thermal environment of automotive applications.

Optimized power management: This feature supports advanced power management strategies by providing fine-grained control over power consumption, which is especially beneficial for modern automotive systems like ADAS.

Simplified design: Because the diode emulation function is integrated, it eliminates the need for additional external circuitry. This reduces the complexity and size of the PCB design.

In summary, diode emulation mode in TLF12505A

- Prevents negative inductor current by disabling the low-side MOSFET during tri-state PWM signals
- Converts the low-side MOSFET to behave like a diode to improve light-load efficiency
- Is controlled via PWM tri-state input from the external multiphase PWM controller
- Helps to reduce conduction losses and improve overall power stage efficiency under light-load conditions

These features and advantages make the diode emulation mode in TLF12505A valuable for efficient, reliable power management in automotive applications such as AD and ADAS modules.

4 Typical ADAS application circuit

Autonomous Driving (AD) and Advanced Driver Assistance Systems (ADAS) constitute interrelated domains within vehicular automation aimed at augmenting safety, operational efficiency, and driving autonomy. ADAS functions as a semi-automated support framework, providing real-time driver assistance through features such as adaptive cruise control, lane keeping, and collision avoidance. In contrast, AD represents the progression toward fully autonomous vehicle operation, characterized by minimal to no human intervention.

Both systems leverage multi-sensor fusion, machine learning algorithms, and high-performance, real-time data processing. These technologies enable precise environmental perception, decision making, and control execution, ensuring robust performance and system-level safety integrity.

4.1 Typical ADAS application diagram including power stages

Key parts of ADAS sensor fusion include different types of sensors like cameras, LiDAR, radar, and ultrasonic sensors, combined with advanced algorithms and powerful computing systems. Together, these allow the system to accurately gather and process data from multiple sources, creating a clear and reliable understanding of the environment. This helps the vehicle to see its surroundings well and make safe, automated driving decisions.

Figure 6 showcases key components of ADAS sensor fusion.

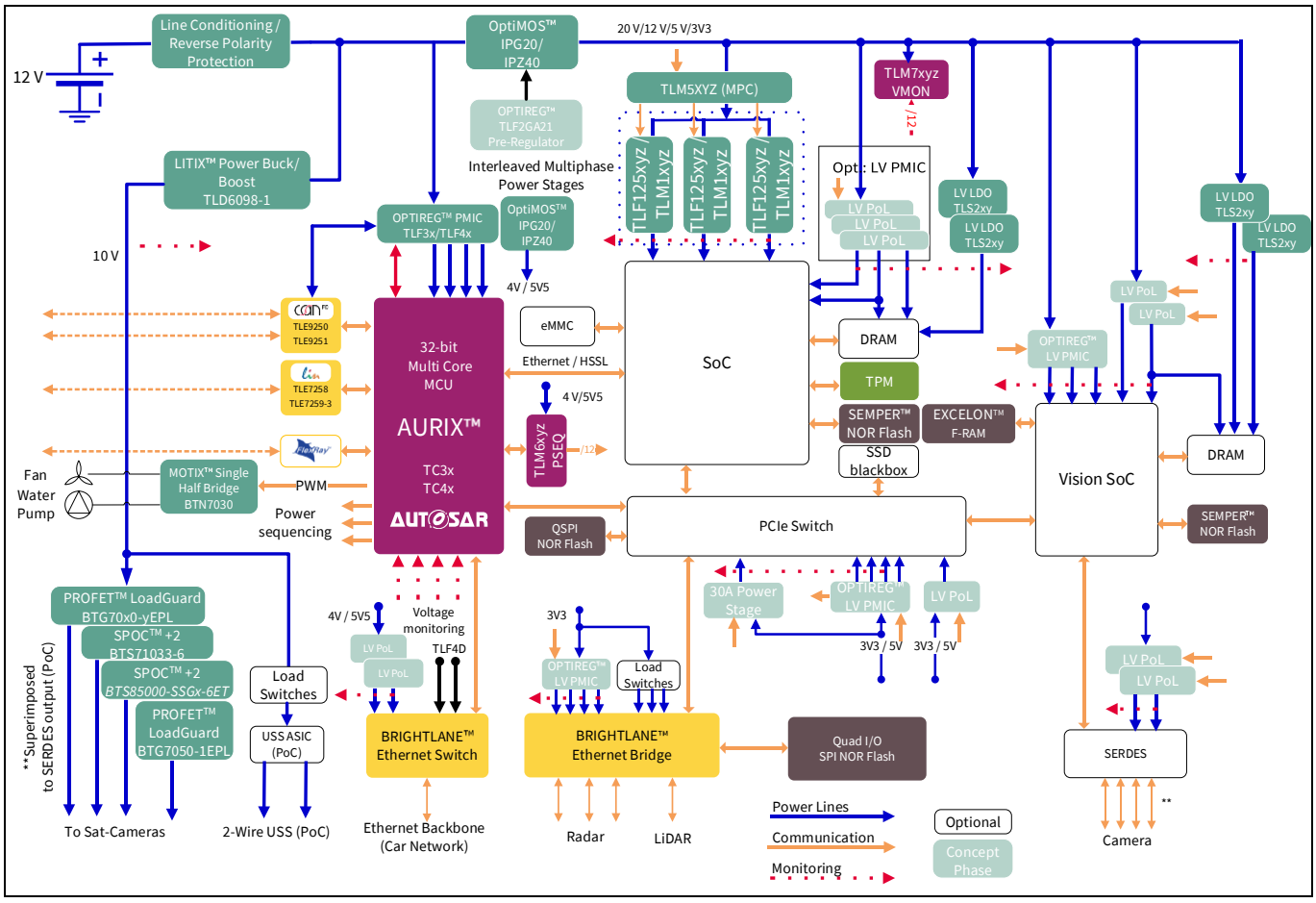


Figure 6 Typical ADAS application diagram including power stages

4.2 Interleaved multiphase power delivery system

A high-level application example of an interleaved multiphase power delivery system is shown in Figure 7 where four TLF12505A stages are configured across two distinct voltage rails, providing efficient, high-current, and stable power supply to different parts of the automotive electronics (e.g., processors, sensors) with improved thermal management and load balancing.

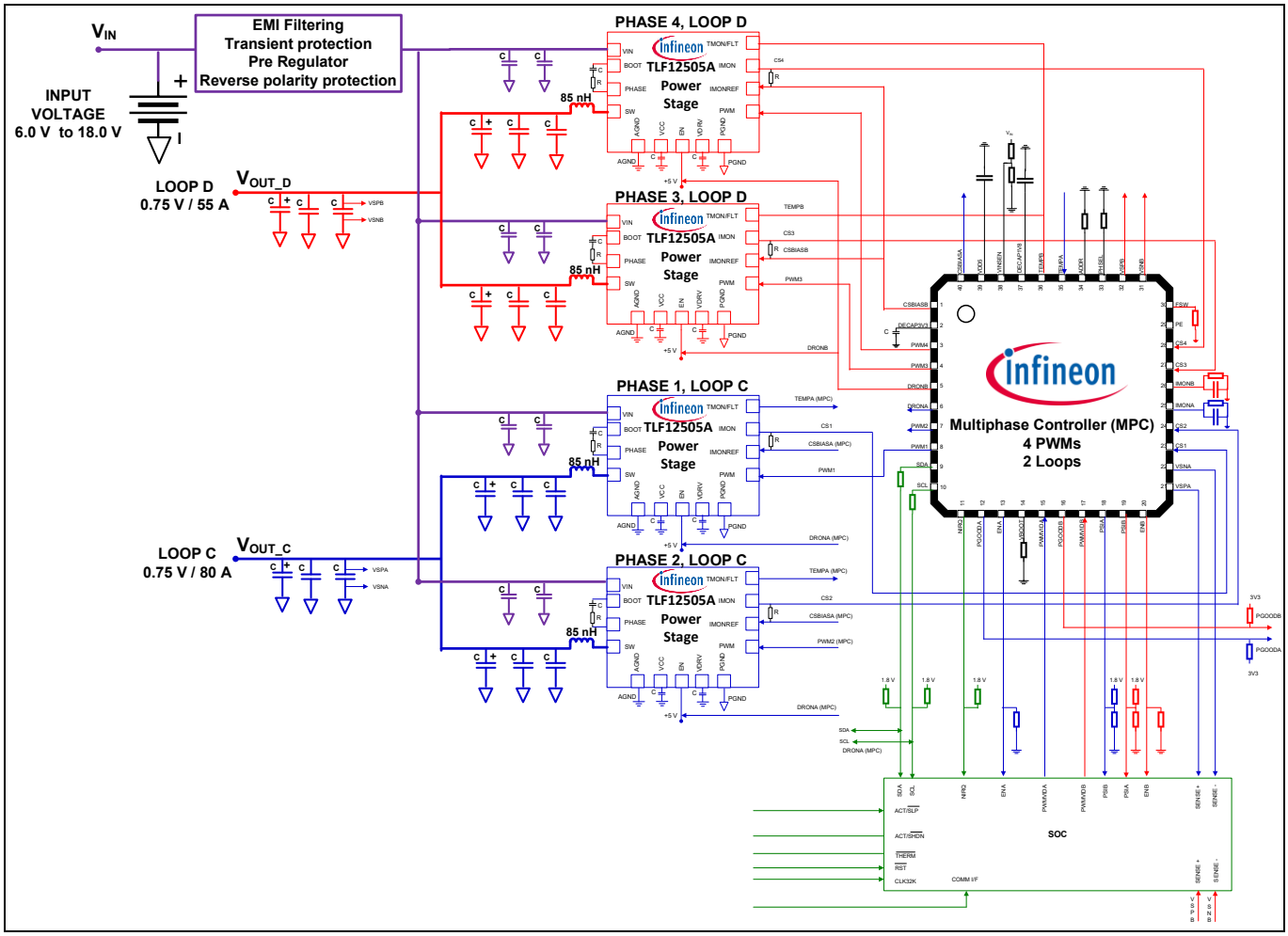


Figure 7 Example of four power stages with two loops in ADAS power delivery

5 Buck converter power components selection

In the given range of input voltage, the choice of converter topology needs to provide a stable output voltage. From the application specifications, the battery (input) voltage to the power stage DC-DC converter will be higher than the required output voltage. The synchronous buck converter topology shown in Figure 8 provides step-down voltage with respect to the input voltage. The power stage solution board hardware components were chosen to meet the automotive standards.

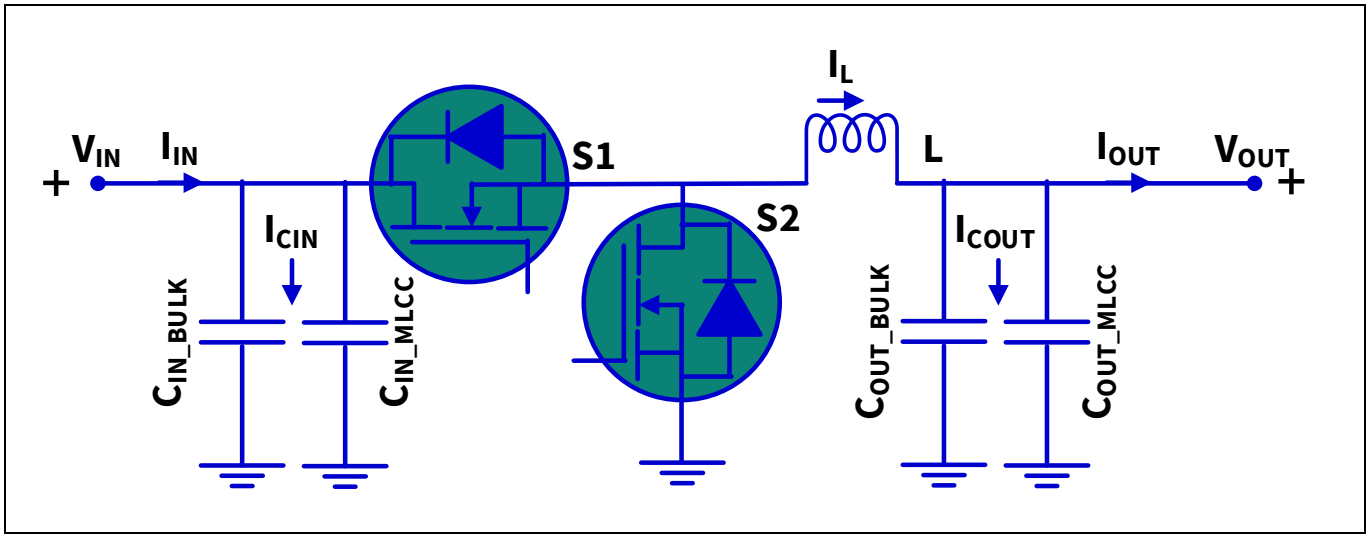


Figure 8 Simplified topology of synchronous buck converter

5.1 Input capacitor selection

The function of input MLCC is to reduce the ripple voltage amplitude on the input line and this, in turn, reduces the RMS ripple current handled by input bulk capacitors. Additionally, these reduce the switching noise on the input lines, thereby reducing conducted electromagnetic interference (EMI). The input capacitor bank comprises a combination of ceramic and electrolytic capacitors. Ceramic capacitors are used to bring down the equivalent series resistance (ESR) of the capacitor bank, as ceramics offer extremely low ESR and limit the input voltage switching ripple. Bulk electrolytic capacitors are used to support the change in the line current during load transients. Bulk electrolytic or polymer capacitors may supplement bulk energy storage.

When the converter is operating in buck mode, the control MOSFET (Q1) in Figure 8 causes a pulsating ripple current with high di/dt at the input. In the absence of input filter capacitors, the DC resistance of PCBs and parasitic inductance generates a larger voltage ripple at the input. Input filter capacitors provide a shorter and lower impedance path for the ripple current, which in turn reduces the conducted and radiated EMI and provides stability to the line voltage during input voltage fluctuations. Note that pulsating input current waves have high RMS values, which cause significant heating and high harmonic content, resulting in EMI.

In an application, a good practice is to keep the input voltage ripple lower than ±5% to ±10% of the input voltage. The input voltage peak-to-peak ripple produced by the input capacitor is equal to the input capacitors ESR multiplied by the capacitor's RMS current (see Equation 7).

The chosen input capacitor's current ratings should be equal to or greater than the RMS capacitor current I_{CIN_RMS} and its voltage rating should be 40–50% higher than the maximum applied input voltage.

5.1.1 Input capacitor RMS current

To determine the RMS value of a pulsed current, integrate the square of the current over a single period, divide by the period, and then take the square root. For a rectangular pulse, this simplifies to

$$I_{CIN\_RMS} = \sqrt{\frac{1}{T}\int_0^T i_{C_{IN}}^2 \, dt}$$

Equation 1 Capacitor RMS current

The input capacitor current, when MOSFET Q1 ON is ($I_{IN} - I_L$) and when MOSFET Q1 OFF is I_{IN}, then I_{CIN_RMS} can be written as

$$I_{CIN\_RMS} = \sqrt{\frac{1}{T}\left(\int_0^{DT} (I_{IN} - I_L)^2 \, dt + \right) + \int_{DT}^{T} (I_{IN})^2 \, dt}$$

Equation 2 Input capacitor current when Q1 is on

By neglecting the inductor ripple current (ΔI_L) in a Buck converter ($I_L = I_{OUT}$) and using the relation ($I_{IN} = D*I_O$), the RMS current of the input capacitor in buck mode is

$$I_{CIN\_RMS} = I_O \sqrt{D_{BUCK}(1 - D_{BUCK})}$$

Equation 3 RMS current of input capacitor in buck mode

Where,

I_L is the inductor current

Duty cycle of a buck converter $D_{BUCK} = \frac{V_{OUT}}{V_{IN} * \zeta}$

ζ is efficiency of the power converter

5.1.2 Input ceramic capacitor selection

The current flowing through the input capacitor (I_{CIN}) is the difference between the input current (I_{IN}), inductor current (I_L) during the MOSFET (Q1) ON state, and only the input current (I_{IN}) during the MOSFET (Q1) OFF state. From this operation, during the MOSFET (Q1) OFF state, the input capacitors (C_{IN}) get charged with input current (I_{IN}), and during the MOSFET (Q1) ON state, the input capacitor (C_{IN}) gets discharged. In steady state, the input capacitors' charge added and removed are equal (i.e., capacitor amp second balance). The input voltage ripple $\Delta V_{IN\ PK\ PK}$ goes from its minimum to maximum value during the MOSFET (Q1) OFF state, that is, the charging period.

As we know

$$I_{CIN} = C\frac{dV_{IN}}{dt} = \frac{C*\Delta V_{IN}}{t_{OFF}}; \qquad \text{in buck converter } I_{IN} = D_{BUCK} * I_{OUT} \text{ and } t_{OFF} = (1 - D_{BUCK}) * T_{SW}$$

Equation 4 Input capacitor current

The input multilayer ceramic capacitors (MLCC) value to meet the input voltage ripple requirement in buck mode is

$$C_{IN\_MLCC} \gg = \frac{D_{BUCK} * (1 - D_{BUCK}) * I_{OUT\_MAX}}{\Delta V_{IN\_PK\_PK} * f_{SW}}$$

Equation 5 Input MLCC value

Where,

$\Delta V_{IN\_PK\_PK}$ is the maximum allowable peak-to-peak input voltage ripple

f_{SW} is the operating/switching frequency of the converter

I_{OUT_MAX} is the rated maximum output current

The loss due to the input capacitor's ESR is

$$P_{C_{IN}} = I^2_{C_{IN\_RMS}} * R_{C_{IN\_MLCC}}$$

Equation 6 Loss due to input capacitor's ESR

Where, R_{CIN_MLCC} is the input multilayer ceramic capacitor (MLCC) network's total equivalent series resistance.

5.1.3 Input bulk capacitor selection

The input supply lines are typically incapable of providing the required input current quickly enough for the converter to respond to a fast transient load current. The input bulk capacitor provides the energy necessary to source the current to the buck supply until the host supply can fill the demand. The choice of the input bulk capacitor should meet the allowable ripple current requirement and overshoot/undershoot specifications due to load transients.

The ESR of the input bulk capacitor (R_{CIN_BULK}) and the capacitance (C_{IN_BULK}) need to meet the transient response requirement.

ESR of the input bulk capacitor is

$$R_{CIN\_BULK} \ll 0.5 * \left(\frac{V_{IN\_TRANSIENT}}{I_{OUT_{STEP}} * D_{BUCK_{MAX}}}\right)$$

Equation 7 Input bulk capacitor ESR

Where,

$V_{IN\_TRANSIENT}$: Allowed input voltage transient undershoot or overshoot due to output load current transients

$I_{OUT_{STEP}}$: Allowed change in output load current

$D_{BUCK_{MAX}}$: Maximum duty cycle in buck mode

The capacitance of the input bulk capacitor to meet the output load transients is

$$C_{IN\_BULK} \gg \frac{D_{BUCK} * I_{OUT_{STEP}}}{2 * \pi * f_{BW\_EMI\_FILTER} * V_{IN\_TRANSIENT}}$$

Equation 8 Input bulk capacitance to meet output load transients

Where,

$f_{BW\_EMI\_FILTER}$: Bandwidth of the EMI LC filter

D_{BUCK} : Duty cycle in buck mode

Input voltage transient undershoot/overshoot due to load step is

$$V_{IN\_TRANSIENT} = \frac{I_{OUT_{STEP}} * D_{BUCK}}{2 * \pi * f_{BW\_EMI\_FILTER} * (C_{IN\_BULK} + C_{IN\_MLCC})} + I_{OUT_{STEP}} * D_{BUCK} * (R_{CIN\_BULK})$$

Equation 9 Input voltage transient undershoot/overshoot due to load step

Input voltage ripple is

$$V_{IN\_RIPPLE} = \frac{I_{OUT} * D_{BUCK} * (1 - D_{BUCK})}{f_{SW} * (C_{IN\_BULK} + C_{IN\_MLCC})} + I_{OUT\_MAX} * D_{BUCK} * (R_{C_{IN\_MLCC}}$$

Equation 10 Input voltage ripple

5.2 Power inductor selection

The chosen power inductor value must satisfy buck mode conditions. The lower the inductor value, the smaller the size, but with a higher peak current.

5.2.1 Power inductor value

The basic inductor current and voltage relation can be written as $V_L = L\frac{dI_L}{dt}$. In a buck converter, the change in inductor current during the MOSFET (Q1) ON time is equal to the change in current during the MOSFET (Q1) OFF time. The change in the inductor current (I_L) during the MOSFET (Q1) ON time can be written as $\frac{\Delta I_L}{DT_{sw}}$

$$L_{BUCK} = \frac{(V_{IN\_MAX} - V_{OUT}) * D_{BUCK}}{\Delta I_L * f_{SW}}$$

Equation 11 Power inductor value – buck mode

ΔI_L can be fraction (0.2 to 0.4) of the I_{OUT_MAX}

Where V_{IN_MAX}: Maximum input voltage

5.2.2 Inductor peak current

The maximum current passing through the power inductor in buck mode is

$$I_{L\_MAX\_BUCK} = \frac{\Delta I_L}{2} + I_{OUT\_MAX}$$

Equation 12 Maximum current passing through power inductor in buck mode

MOSFETs Q1 and Q2 must withstand this peak current.

5.2.3 Inductor RMS current

The RMS current passing through the power inductor in buck mode is

$$I_{L\_RMS\_BUCK} = \sqrt{(I_{OUT\_MAX})^2 + \frac{(\Delta I_L)^2}{12}}$$

Equation 13 RMS current passing through power inductor in buck mode

5.3 Power MOSFETs

TLF12505A is an integrated power stage containing a low quiescent current synchronous buck gate driver IC which is co-packed with control (Q1) and synchronous (Q2) MOSFETs. Choose the power stage based on the design parameters.

The power losses of a converter depend on the chosen MOSFET characteristics like drain-source on-state resistance ($R_{DS)}$), rise time (t_r), fall time (t_f), total gate charge (Q_g), MOSFET diode reverse recovery charge (Q_{rr}) and switching frequency (f_{SW}) of the converter. Compute the efficiency of the converter a few basic empirical formulas provided in the following sections.

5.3.1 Power MOSFET RMS current

When the MOSFET (Q1) is turned on, the current passed through the MOSFET (Q1) I_{Q1} is the current drawn from the input line. The switch RMS current $I_{Q1\_RMS\_ON}$ is

$$I_{Q1\_RMS\_ON} = \sqrt{\left(I_{OUT}^2 + \frac{\Delta I_L^2}{12}\right)(D_{BUCK})}$$

Equation 14 MOSFET Q1 RMS current

When the MOSFET (Q2) is turned on the current passed through the MOSFET (Q2) RMS current $I_{Q2\_RMS\_ON}$ is

$$I_{Q2\_RMS\_ON} = \sqrt{\left(I_{OUT}^2 + \frac{\Delta I_L^2}{12}\right)(1 - D_{BUCK})}$$

Equation 15 MOSFET Q2 RMS current

5.3.2 Power MOSFET losses

In a synchronous buck converter, the power MOSFETs' (Q1 and Q2) losses can be conduction losses, switching losses, body diode reverse recovery losses, dead time losses, and gate charge losses. The empirical formulas for each of the losses are given for MOSFETs Q1 and Q2 separately.

Conduction losses in MOSFET (Q1):

$$P_{Q1\ CONDUCTION\ LOSSES} = (I_{Q1\_RMS\_ON})^2 * R_{DS(ON)}$$

Equation 16 MOSFET Q1 conduction losses

Switching losses in MOSFET (Q1):

$$P_{Q1\ SWITCHING\ LOSSES} = V_{IN} * \left(I_{OUT} - \frac{\Delta I_L}{2}\right) * 0.5 * (t_{r\_Q1}) * f_{SW} + V_{IN} * (I_{OUT} + \frac{\Delta I_L}{2}) * 0.5 * (t_{r\_Q1}) * f_{SW}$$

Equation 17 MOSFET Q1 switching losses

Diode reverse recovery losses:

$$P_{Q1\ REVERSE\ RECOVERY\ LOSSES} = V_{IN} * Q_{rr} * f_{SW}$$

Equation 18 Diode reverse recovery losses

Conduction losses in MOSFET (Q2):

$$P_{Q2\ CONDUCTION\ LOSSES} = (I_{Q2\_RMS\_ON})^2 * R_{DS(ON)}$$

Equation 19 Conduction losses in MOSFET (Q2)

Switching losses in MOSFET (Q2):

$$P_{Q2\ SWITCHING\ LOSSES} = V_{IN} * (I_{OUT} - \frac{\Delta I_L}{2}) * 0.5 * (t_{f\_Q2}) * f_{SW}$$

Equation 20 Switching losses in MOSFET (Q2)

Dead-time losses and gate charge losses are for both Q1 and Q2 MOSFETs:

$$P_{Q1\ Q2\ DEADTIME\ LOSSES} = \text{Dead-time losses} = 2 * V_{Q2DIODE} * (I_O) * (T_{DEADTIME}) * f_{SW}$$

Equation 21 Dead-time losses and gate charge losses

MOSFET gate charge losses

$$P_{Q1\ Q2\ GATE\ CHARGE\ LOSSES} = 2 * Q_g * fsw * V_{GD}$$

Equation 22 MOSFET gate charge losses

Where,

$T_{DEADTIME}$: Dead-time between Q1 and Q2 MOSFETs

t_{r_Q1} : Rise time of Q1

t_{f_Q1} : Fall time of Q1

t_{r_Q2} : Rise time of Q2

t_{f_Q2} : Fall time of Q2

Q_{rr} : Reverse recovery charge of the MOSFET

$R_{DS(ON)}$: MOSFET drain-source on-state resistance – datasheet parameter

V_{GD}: Gate driving voltage

Qg : Gate charge

5.4 Output capacitors selection

When there is a change in the load current (load transient), the converter's feedback control loop senses the change and adjusts the duty cycle of the converter. Typically, in an application, the rate of change in load current is faster than the loop response. Hence, to support the load transients, bulk capacitors at the output need to be added, and for output ripple to be in the specified limits, high-frequency bypass capacitors (MLCC) need to be added in parallel to the output bulk capacitors.

5.4.1 Output capacitor selection

Output capacitors are required to maintain a regulated output voltage while the MOSFET (Q1) is off and must be able to respond to changes in the load current. It is necessary to minimize the amount of ripple on the

output voltage. The output capacitors' maximum ESR can be computed using the specified maximum output voltage ripple, ΔV_{OUT_pk-pk} and the maximum load current I_{OUT_MAX}. The maximum ESR of the output capacitors must be lower than the computed R_{COUT_MAX} to have an output voltage ripple below the specification value.

- Output capacitance calculation must address both DC ripple and AC transient requirements, with transient specifications typically dominating the overall capacitance needed
- When sizing output capacitors, transient load conditions generally impose stricter demands than steady state ripple, thus governing the total capacitance selection
- The total output capacitance is primarily determined by transient response criteria, although DC ripple specifications must also be met during design

$$R_{COUT\_MAX} = 0.5 * (\frac{\Delta V_{OUT_{PK\_PK}}}{I_{OUT_{MAX}}})$$

Equation 23 Maximum ESR calculation of output capacitors (should be lower than R_{COUT_MAX})

Where,

$\Delta V_{OUT\_PK\_PK}$ allowed output voltage ripple, typically it will be 3% to 5% of V_{OUT}

The output capacitor value in a buck converter to meet the specified ripple requirement is

$$C_{OUT\_MLCC} \gg \frac{\Delta I_L}{8 * f_{SW} * \Delta V_{OUT\_PK\_PK}}$$

Equation 24 Output capacitor value in a buck converter to meet ripple requirements

Output voltage ripple equation can be written as

$$\Delta V_{OUT\_PK\_PK} = \frac{\Delta I_L}{8 * f_{SW} * C_{OUT\_MLCC}} + \Delta I_L * R_{COUT\_MAX}$$

Equation 25 Output voltage ripple

During a load step the inductance, L (buck converter inductance) or L_{EQ} (in multiphase buck converters, parallel inductance values based on the number of phases, *N*), requires a finite time, $T_{UNDERSHOOT}$, to slew to the high current level, depending on the total number of phases (N). During this interval, a charge equal to $Q_{UNDERSHOOT}$ is drawn from the output capacitors, casuing V_{OUT} to dip below its set point.

Upon load release, the excess charge in the inductor, $Q_{OVERSHOOT}$, is dumped into the output capacitors during time $T_{OVERSHOOT}$, causing V_{OUT} to swing above its regulation point.

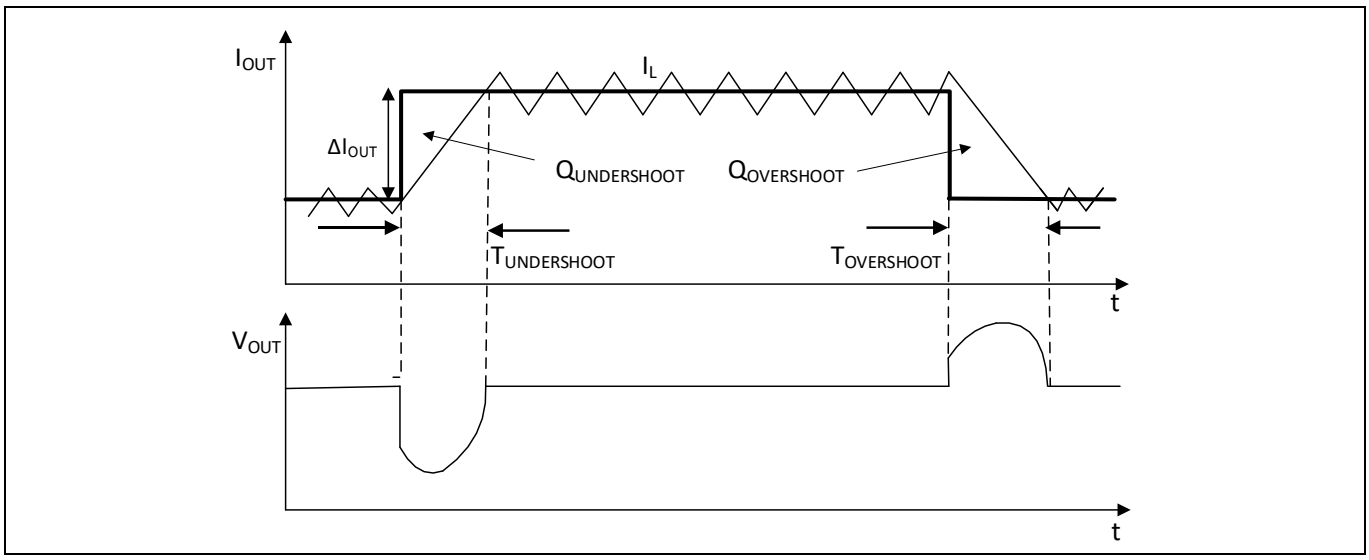


Figure 9 Transient load

During a load step, the inductor current ramps from its initial current $I_{OUT\_INITIAL}$ towards the new load current $I_{OUT\_INITIAL} + \Delta I_{OUT}$. Here ΔI_{OUT} is the load step.

The inductor voltage V_L during the transient is approximately constant and given by:

$$V_L = L \frac{di_L}{dt}$$

Equation 26 Inductor voltage V_L during the transient

The time for the inductor current to ramp through the change ΔI_{OUT} is:

$$T_{UNDERSHOOT} = L \frac{di_L}{V_L}$$

$$T_{UNDERSHOOT} = \frac{L_{EQ} * \Delta I_{OUT}}{V_{IN} - V_{OUT}}$$

$$T_{OVERSHOOT} = \frac{L_{EQ} * \Delta I_{OUT}}{V_{OUT}}$$

Equation 27 Time for inductor current to ramp through ΔI_{OUT}

5.4.1.1 Derivation of $Q_{UNDERSHOOT}$

The inductor current $i_L(t)$ ramps linearly from I_{OUT} to $I_{OUT} + \Delta I_{OUT}$ over $T_{UNDERSHOOT}$

$$i_L(t) = I_{OUT} + \frac{\Delta IOUT}{T_{UNDERSHOOT}} * t$$

Equation 28 Inductor current ramp

The load current steps instantaneously from I_{OUT} to $I_{OUT} + \Delta I_{OUT}$; so, the output capacitor must supply the difference

$$i_{CAP}(t) = (I_{OUT} + \Delta I_{OUT}) - i_L(t) = \Delta I_{OUT}\left(1 - \frac{t}{t_{UNDERSHOOT}}\right)$$

Equation 29 Output capacitor current to balance load current step-up

The total charge drawn from the output capacitor (undershoot charge) is the integral of $i_{CAP}(t)$ over the undershoot time

$$Q_{UNDERSHOOT} = \int_0^{t_{UNDERSHOOT}} i_{CAP}(t)dt = \int_0^{t_{UNDERSHOOT}} \Delta I_{OUT}\left(1 - \frac{t}{t_{UNDERSHOOT}}\right)dt$$

Performing integration

$$Q_{UNDERSHOOT} = \Delta I_{OUT}\left(t_{UNDERSHOOT} - \frac{1}{t_{UNDERSHOOT}} * \frac{t_{UNDERSHOOT}^2}{2}\right) = \frac{\Delta I_{OUT} * t_{UNDERSHOOT}}{2}$$

$$C_{UNDERSHOOT} = \frac{Q_{UNDERSHOOT}}{\Delta V_{OUT\_UNDERSHOOT}}$$

Equation 30 Total charge drawn from the output capacitor

Where $\Delta V_{OUT\_UNDERSHOOT}$ is the allowed voltage undershoot.

5.4.1.2 Derivation of $Q_{OVERSHOOT}$

Conversely, on load release, the inductor current decreases from $I_{OUT} + \Delta I_{OUT}$ back to I_{OUT} over $T_{OVERSHOOT}$, and the excess charge $Q_{OVERSHOOT}$ is delivered back to the output capacitor.

$$Q_{OVERSHOOT} = \int_0^{t_{OVERSHOOT}} (i_L(t) - I_{OUT})\ dt = \frac{\Delta I_{OUT} * t_{OVERSHOOT}}{2}$$

$$C_{OVERSHOOT} = \frac{Q_{OVERSHOOT}}{\Delta V_{OUT\_OVERSHOOT}}$$

Equation 31 Excess charge delivered back to the output capacitor

5.4.1.3 Optimizing output capacitors using DC Load Line (DCLL)

The concept of the DC load line in power stages relates to plotting the relationship between output voltage and load current under steady state as shown in Figure 10 for sizing output capacitors. In buck converter power stages, this approach can aid in computing the output capacitor values by considering the voltage drop (or ripple/undershoot) due to load changes and the capacitor's energy storage. The implementation of a DC Load Line (DCLL) allows for a significant reduction in output capacitance by expanding the allowable voltage window during load transients.

DC load line in power stages:

- The DC load line represents the output voltage as a function of the load current assuming steady state
- In a buck converter, during a load transient, the output voltage drops as the output capacitor supplies the instantaneous current demand while the inductor current remains limited by its di/dt and the finite bandwidth of the control loop
- Output voltage drops along this line due to dynamic load changes, capacitor voltage droop, and ESR
- Voltage drop and ripple are limited by the output capacitor's ability to store and supply charge

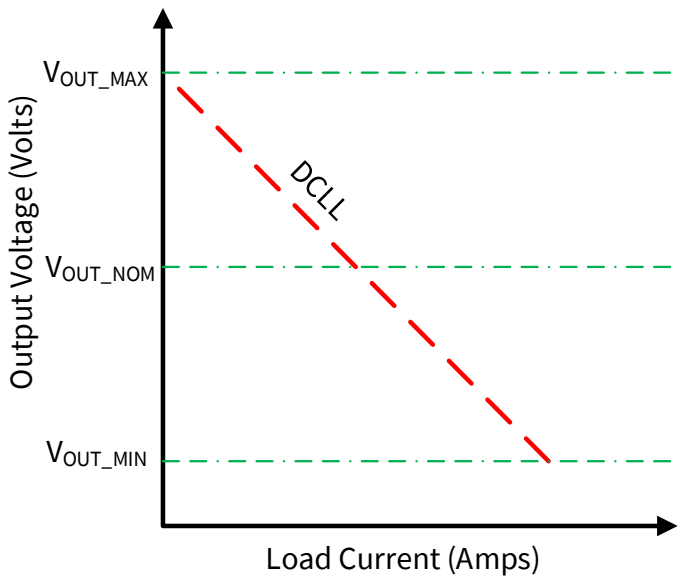


Figure 10 DC load line slope

Load transient with DC load line in power stages to compute output capacitors is shown in Figure 11. Set DCLL to '0' if a DC load line is not required.

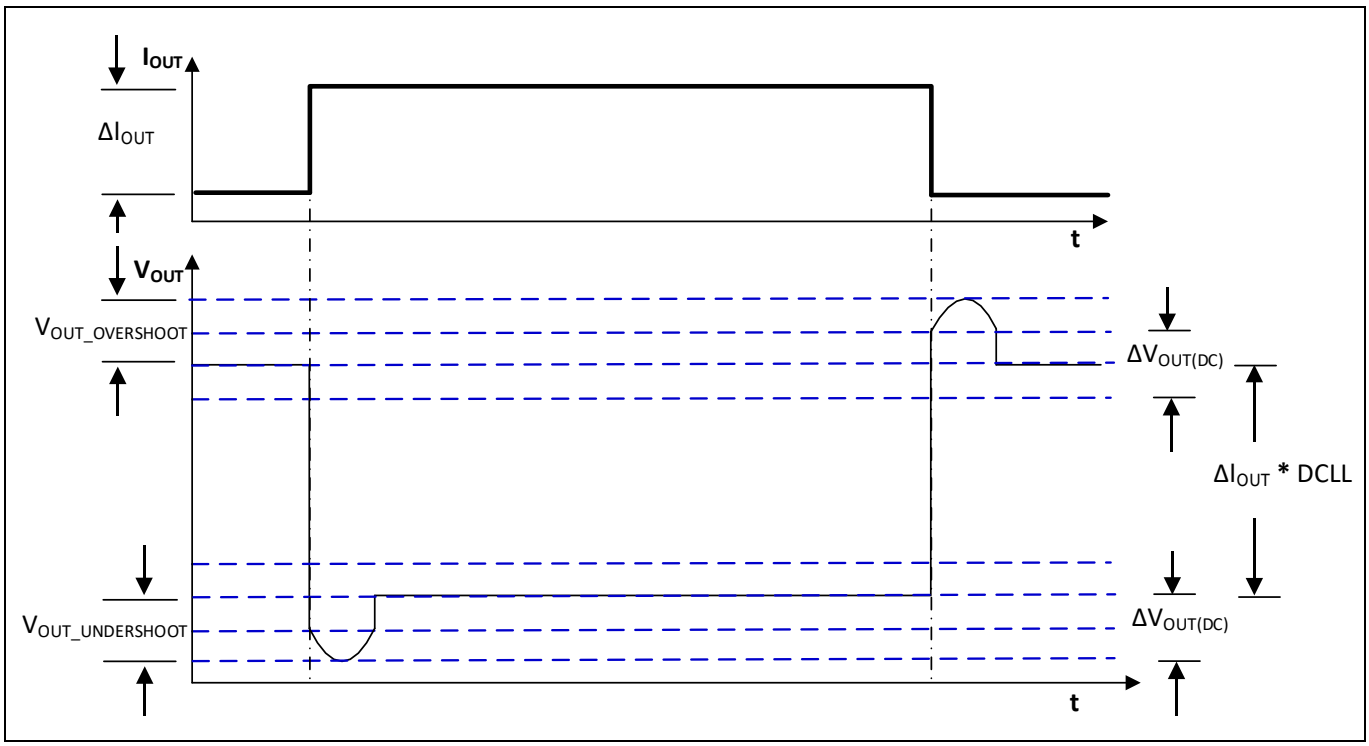


Figure 11 Load transient with DC load line in power stages

The total capacitance is determined by the application's maximum transient load, when DC load line (DCLL) set is,

$$C_{UNDERSHOOT} = \frac{Q_{UNDERSHOOT}}{\Delta V_{OUT_{UNDERSHOOT}} + \Delta I_{OUT} * DCLL}$$

Equation 32 Total capacitance based on max. transient load

The total capacitance is determined by the application's transient load release when DC load line (DCLL) set is,

$$C_{OVERSHOOT} = \frac{Q_{OVERSHOOT}}{\Delta V_{OUT\_OVERSHOOT} + \Delta I_{OUT} * DCLL}$$

Equation 33 Total capacitance based on transient load release

The load release transient dictates the total capacitance needed for regulation, as the required $C_{OVERSHOOT}$ is typically much larger than $C_{UNDERSHOOT}$. This occurs because during a load step, the capacitors absorb energy from the inductor, helping to prevent a voltage undershoot. During a load release, however, the inductor's excess energy is rapidly dumped into the capacitors, causing a more significant voltage overshoot.

5.4.2 Output capacitor RMS current

The ripple current flowing through the output capacitor in buck mode is

$$I_{COUT\_RMS} = \sqrt{I_{L\_MAX\_BUCK}^2 - I_{OUT\_MAX}^2}$$

Equation 34 Ripple current through the output capacitor in buck mode

or

RMS current in the output capacitor in buck mode is

$$I_{COUT\_RMS} = \frac{\Delta I_L}{\sqrt{12}} \cong 0.3\Delta I_L$$

Equation 35 RMS current in the output capacitor in buck mode

Where,

ΔI_L is the power inductor peak-to-peak ripple current (continuous conduction mode).

5.4.3 Power component design in interleaved multiphase buck converters

Interleaved multiphase buck converters are commonly used in Advanced Driver Assistance Systems (ADAS) due to their ability to reduce input and output current ripple, improve transient response, and increase power density and efficiency. These benefits are critical for ADAS, which require a stable, reliable, low-voltage power supply for sensitive electronics that must function correctly during frequent, fast switching transients.

5.4.3.1 Interleaved multiphase buck converter input capacitor RMS current

- An interleaved multiphase buck converter lowers the RMS current per phase, thereby reducing capacitor stress and enabling a smaller capacitor size
- Interleaving partially cancels the input ripple currents across phases, thereby lowering the net ripple and the input capacitor's RMS current as shown in Figure 12
- Consequently, the input capacitor banks in multiphase converters can be designed to be smaller, more efficient, and more reliable than those employed in single phase implementations

Normalized input capacitors RMS current in interleaved multiphase buck converter is

$$I_{CIN\ (RMS)\ Normalized} = \sqrt{\left(D_{Buck} - \frac{m}{N}\right) * \left(\frac{1+m}{N} - D_{Buck}\right)}$$

$$I_{CIN\ (RMS)} = I_{CIN\ (RMS)\ Normalized} * I_{OUT}$$

Equation 36 Normalized input capacitors RMS current in interleaved multiphase buck converter

Where,

Duty cycle of a buck converter $D_{BUCK} = \frac{V_{OUT}}{V_{IN} * \zeta}$

ζ is efficiency of the power converter

N = Number of interleaved buck converters

m = floor (N * D_{Buck})

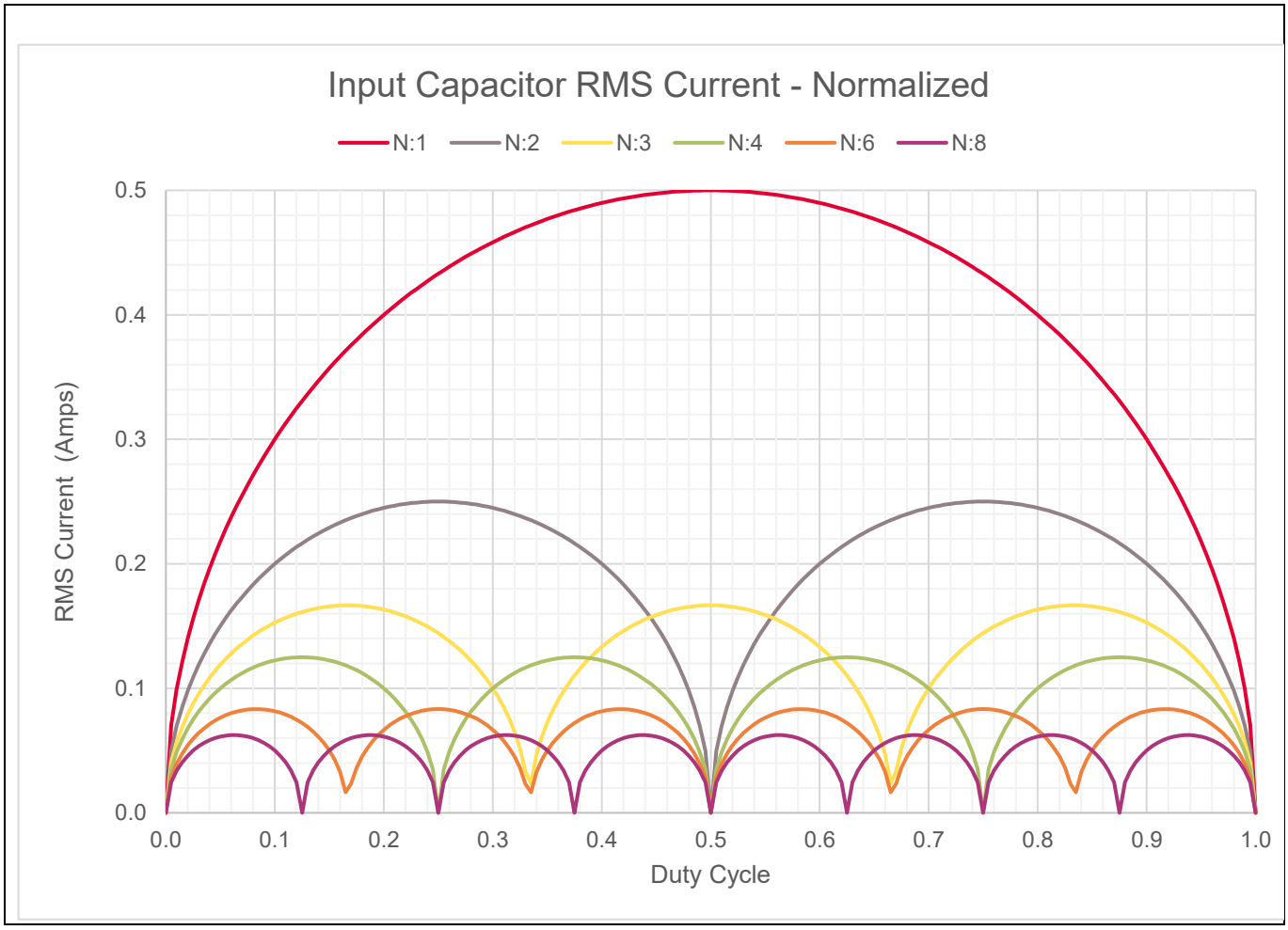


Figure 12 Normalized input capacitor RMS current vs. duty ratio; N = phase count

5.4.3.2 Ripple current of the output capacitor in an interleaved multiphase buck converter

In an interleaved multiphase buck converter, the output capacitor's ripple current is partially cancelled by the interleaving effect, which reduces the current ripple. The output capacitor's ripple current can be approximated by considering the combined ripple currents from all phases. This significantly mitigates the capacitor's ripple current stress compared to a single-phase buck converter, as illustrated in Figure 13.

Key points for output capacitor ripple current:

- The capacitor ripple current depends on the inductor ripple currents of each phase and the phase interleaving angle
- Interleaving phases shift the switching waveforms, causing a partial ripple cancellation at the output, which in turn reduces the total ripple current in the output capacitors
- The ripple current of the capacitor is typically less than the sum of individual phase ripple currents due to this cancellation effect
- For ideal equal phase currents and 180° phase shift in a two-phase system, the output capacitor ripple current can be substantially reduced, often around 0.3 to 0.5 times the ripple current of a corresponding single phase
- The exact ripple current is influenced by the duty cycle, number of phases, and load conditions

Normalized output capacitors ripple current in an interleaved multiphase buck converter is

$$I_{COUT\ (RIPPLE)\ Normalized} = \frac{N}{D_{Buck} * (1 - D_{Buck})} * \left(D_{Buck} - \frac{m}{N}\right) * \left(\frac{1+m}{N} - D_{Buck}\right)$$

$$I_{COUT\ (RIPPLE)} = I_{COUT\ (RIPPLE)\ Normalized} * \Delta I_L$$

Equation 37 Normalized ripple current of output capacitors in an interleaved multiphase buck converter

Where ΔI_L = Inductor ripple current

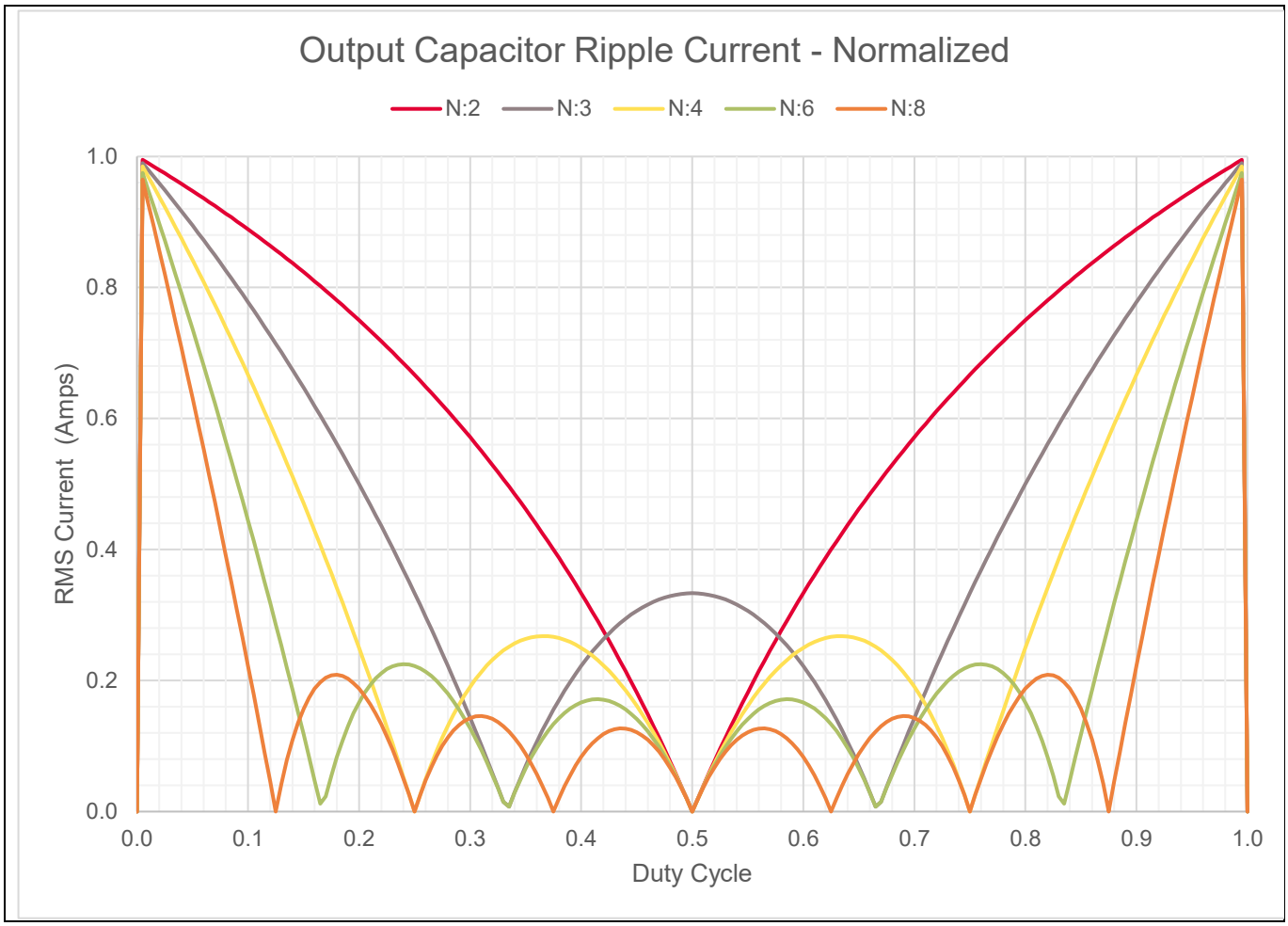


Figure 13 Normalized output capacitor ripple current vs. duty; N = phase count

5.5 Bootstrap circuit design

A bootstrap circuit is used in half-bridge configurations to supply the bias voltage to the high-side MOSFET (Q1) as it requires a voltage supply referenced at the source of the high-side MOSFET as shown in Figure 3.

For the bootstrap circuit, connect a 0.22 µF 0402 X7R multilayer ceramic capacitor (MLCC) between the BOOT and PHASE pins. The capacitor supplies the necessary charge to turn on the control MOSFET. If the input voltage (VIN) exceeds 13.2 V, a 2 Ω resistor must be added in series with the bootstrap capacitor to reduce switching node (SW) ringing and minimize electromagnetic interference (EMI). Acceptable capacitor values range from 0.22 µF to 0.56 µF, but 0.22 µF is the recommended value.

The bootstrap capacitor should be placed on the same side of the PCB as TLF12505A and as close as possible to the BOOT pin.

TLF12505A also features internal protection circuitry to automatically replenish the voltage across the bootstrap capacitor as shown in Figure 4. It avoids the gradual depletion of capacitor energy when the power stage is in High-Z state for a long period of time.

5.6 V_{CC} and V_{DRV} decoupling capacitors

A 1 µF X7R multilayer ceramic decoupling capacitor must be connected between the VCC and AGND pins. A 1 Ω resistor is also recommended between the external power supply and the VCC pin.

Connect a 1 µF X7R decoupling capacitor between the VDRV and PGND pins. This capacitor can be directly connected to the 5 V supply, as shown in Figure 3.

Mount both decoupling capacitors on the same side of the PCB as TLF12505A. For optimal performance, position them adjacent to the VCC-AGND and VDRV-PGND pins to minimize physical distance. Additionally, use a low-inductance routing method, specifically wide and short traces, to reduce parasitic loop inductance.

6 Fault protections

The TLF12505A power stage integrates a comprehensive set of protection features designed for automotive applications, ensuring high reliability in harsh conditions. For fault threshold specifics, refer to the TLF12505A datasheet [2].

6.1 VCC/VDRV undervoltage lockout (UVLO)

TLF12505A features an active VDRV undervoltage lockout (UVLO) that monitors the VDRV voltage. When the VDRV voltage falls below the UVLO threshold, the TMON/FAULT pin is pulled LOW by a weak internal pull-down, indicating a non-catastrophic fault, as shown in Figure 3.

If the power stage has not started up, the power stage PWM pin is also pulled down to 0 V with a weak pull-down. This can be monitored by the PWM multiphase controller as a signal from the power stage indicating that it is not ready yet for power-up.

As soon as the VDRV voltage is above the UVLO threshold, the PWM pin is in High-Z state instead of 0 V. This indicates to the multiphase controller that it is ready to send the PWM signals. Once the power stage is in normal operation, if it encounters a VDRV UVLO condition, the power stage stops switching, and both TMON pins and IMON-IMONREF signal are pulled down to 0 V. If there are multiple phases connected in the same loop, the TMON pin voltage, being connected to other power stage TMON pins, will continue reporting the highest power stage temperature.

6.2 Thermal shutdown/overtemperature protection (OTP)

TLF12505A has an internal temperature sensor that monitors the device's temperature. It reports the sensed temperature on the TMON/FAULT pin, which produces a linear voltage output with a slope of 8 mV/°C and an offset of 0.6 V at 0°C.

$$V_{TMON/\,FAULT}(V) = \quad 0.6\ V + 0.008\ V/°C\ * T_J\ (°C)$$

Equation 38 Linear voltage output for overtemperature protection

The TMON/FAULT pin has a dual function. It is pulled to 3.3 V for catastrophic faults and pulled to 0 V for non-catastrophic faults. When no fault is present, the pin reports the device's temperature if the VCC supply is within the recommended operating range. Below a junction temperature of –25°C, the TMON voltage is clamped at 0.4 V to prevent false triggering of the VDRV undervoltage.

If the temperature rises above the overtemperature rising threshold (e.g., 155°C), the TMON/FAULT pin is immediately pulled HIGH. The driver will cease switching and ignore the PWM signal from the multiphase controller, with both high-side and low-side MOSFETs being turned off. The TMON/FAULT pin will remain HIGH until the temperature drops below the overtemperature falling threshold (e.g., 143°C).

Thermal features

- Integrated temperature sensing with a slope of about 8 mV/°C at the TMON/FAULT pin, allowing precise junction temperature monitoring
- Overtemperature protection (OTP) with rising threshold at 155°C and falling threshold at 143°C, shutting down the device to prevent thermal damage
- The device reports faults and temperature status via the TMON/FAULT pin, enabling real-time thermal management in the system
- Designed for high thermal cycle reliability and long-term robust operation in demanding automotive power stages

6.3 Cycle-by-cycle overcurrent protection (OCP)

With cycle-by-cycle self-preservation, the currents of the high-side control MOSFET (Q1)) and the low-side synchronous MOSFET (Q2) are monitored during every PWM cycle. If the overcurrent threshold (for example, 90 A) is exceeded, the PWM pulse's on time is immediately truncated. This allows the inductor current to reduce. If TLF12505A detects overcurrent events for more than 10 consecutive PWM cycles, the TMON/FAULT pin is flagged HIGH to alert the multiphase controller (MPC) of the fault.

Note: For the overcurrent protection to function accurately, the PWM pulse on time must be at least 50 ns.

6.4 Cycle-by-cycle negative overcurrent protection (NOCP)

Cycle-by-cycle negative overcurrent protection (NOCP) protects the system during high negative current events, which can occur during rapid load changes, ensuring a safe operation even under extreme or anomalous conditions.

TLF12505A features negative overcurrent protection in the device to protect from very high negative currents. If the power stage detects that the (negative) current reported by IMON exceeds the negative overcurrent threshold (OCPn), the high-side FET is enabled for 200 ns before the power stage continues following the PWM input signal. TMON continues reporting the power stage temperature during a negative overcurrent fault event.

TLF12505A supports diode emulation mode through the PWM tri-state signal, controlled by Infineon's multiphase PWM controller. Therefore, the PWM tri-state signal will force the low-side FET to remain off when the inductor current is about to go negative. The light-load efficiency can be increased by preventing conduction loss caused by the negative inductor current.

6.5 Control MOSFET short detection (high-side MOSFET short – HSS)

Control/high-side MOSFET short detection (High-side MOSFET short – HSS) in power stages is an integrated protection feature. As shown in Figure 4, it monitors the high-side MOSFET for short-circuit faults to prevent damage to the device and the system. TLF12505A uses an internal comparator to monitor the drop between SW-PGND. If the voltage drop exceeds a typical value of 560 mV, an HSS fault is flagged internally and reported via the TMON/FAULT pin by pulling it HIGH. Upon detection, protective actions are taken to disable the PWM gate drive signal and shut down switching to prevent further damage.

This integrated approach is key for reliability and safety in modern power stages.

6.6 Bootstrap capacitor undervoltage detection

TLF12505A features a bootstrap capacitor undervoltage circuitry that detects a missing bootstrap capacitor before powering up, or a damaged bootstrap capacitor during normal operation. Once a bootstrap capacitor undervoltage condition is determined, the TMON/FAULT pin is pulled HIGH to report a catastrophic fault to the multiphase PWM controller.

7 Thermal design

The thermal design of a power stage is crucial for ensuring the reliability, performance, and longevity of power electronic systems. The primary objective is to manage the heat generated by power losses within the components to keep the junction temperatures T_j below their specified maximum limits.

7.1 Thermal design for TLF12505A

A careful thermal design for a TLF12505A-based power stage is essential to deliver higher efficiency, higher current, and higher power with greater reliability. The thermal performance of the TLF12505A power stage is characterized by the following key thermal resistance parameters and features, designed for robust temperature management in automotive environments.

7.1.1 Key thermal parameters

$R_{\Theta JA}$ and $R_{\Theta JC}$ are often treated as fixed, universally applicable device properties, but these values are highly dependent on the test setup and environment, leading to misuse in real designs.

$R_{\Theta JA}$ is fundamentally a system-level parameter, not an intrinsic package constant. It varies significantly with PCB characteristics (board size, layer count, copper thickness, via count, etc.) and other design differences, which strongly influence actual thermal performance.

Datasheet $R_{\Theta JA}$ values are typically measured or simulated on JEDEC standard boards. Consequently, using these values directly in dissimilar applications can cause large junction-temperature estimation errors if the actual PCB and operating conditions differ from the standard setup.

Different package types and mounting/cooling (e.g., TO-263 vs VQFN, with/without heatsink) have different heat flow paths, so their effective ‘θ’ (thermal resistance) differs.

Generally, $R_{\Theta JA}$ is best used for comparing devices in the same package on similar boards, not for estimating junction temperature in actual applications.

$R_{\Theta JC\_PCB}$: Junction to PCB thermal resistance; typical value = 1.5°C/W

$R_{\Theta JC\_TOP}$: Junction to top of package thermal resistance; typical value = 17.8°C/W

$R_{\Theta JA}$: Junction to ambient thermal resistance; typical value (measured on test board in free air) = 28.4°C/W

To calculate the TLF12505A junction temperature from power loss, use the standard thermal calculation formula relating power dissipation and thermal resistance:

$$T_J : P * R_{\theta JC} + T_C$$

Equation 39 Calculating the junction temperature from power loss

Where,
T_J = Junction temperature (°C)
T_C = Case temperature (°C)
P = Power loss in the device (W)
$R_{\Theta JC}$ = Junction to case thermal resistance (°C/W)

1. Identify the power loss (P) of the power stage by measuring or estimating the power loss during your operating conditions
2. Obtain $R_{\Theta JC}$ from the power stage datasheet
3. Measure or estimate the case temperature T_J, with a thermocouple on the device package or near to it

Example:

T_J: Junction temperature (°C)

T_C: Case temperature = 80°C

P: Power loss in the device = 0.6 W

$R_{\Theta JA}$: Junction to case thermal resistance = 17.8°C/W

$$T_J = 0.6 * 17.8 + 80 = 90.68\ (°C)$$

Equation 40 Example calculation of junction temperature from power loss

In the absence of case temperature data, junction temperature can be calculated using the ambient temperature.

$$T_J = P * R_{\theta JA} + T_A$$

Equation 41 Calculating junction temperature using ambient temperature

$R_{\Theta JA}$: Thermal resistance from junction to ambient (°C/W), depends heavily on PCB design and cooling

T_A: Ambient temperature (°C)

Note that $R_{\Theta JC}$ is board-dependent, and the published values are based on Infineon's standard test board. If your board differs from that standard, you should estimate thermal performance using $R_{\Theta JC}$ and derive $R_{\Theta CA}$ for your design. A package with a low $R_{\Theta JC}$ transfers heat effectively to the case, typically via an exposed pad. $R_{\Theta JC}$ is a strong indicator of a package's thermal performance. In general, a low $R_{\Theta JC}$ corresponds to a low $R_{\Theta JC}$.

7.1.2 Thermal performance implications

The low junction-to-PCB thermal resistance means efficient heat transfer to the PCB, improving cooling with a suitable layout. The integrated sensing and shutdown features ensure device protection during thermal stress and overloads. The robust package and thermal design enable reliable operation at high currents (up to 60 A thermal design current) with safe junction temperatures maintained under recommended operating conditions.

This combination makes TLF12505A well-suited for automotive applications requiring high current handling with active thermal monitoring and protection for safe, reliable performance.

7.1.3 Heatsink recommendation

Care should be taken in mounting heatsinks to ensure that even pressure is applied on the power stage surface. A thermal interface material (TIM) should be used between the power stage and the heatsink to solve planarity issues and ensure even thermal conduction.

Thermal design

The VCC, VDRV, VIN, and bootstrap capacitors are typically located on the same side of the PCB as the power stage. The height of these capacitors must be considered when using heatsinks. The heatsink should dissipate the heat generated considering maximum power loss, maintaining junction temperature below 150°C.

Overtemperature protection (OTP) will be activated between 145°C and 165°C. (150°C is the nominal OTP value to prevent damage from long high-temperature operation.) Refer to the respective power stage datasheets for more details. A low thermal resistance interface between TLF12505A and the heatsink is important for efficient cooling.

The thermal resistance $R_{\Theta SA}$ required for the heatsink can be calculated using

$$R_{\theta SA} = \frac{T_J - T_A}{P} - R_{\theta JC} - R_{\theta CS}$$

Equation 42 Calculating the heatsink's thermal resistance

Where,
T_J: max junction temperature (e.g., 150°C)
T_A: ambient temperature (e.g., 105°C)
P: power dissipation (W)
$R_{\Theta JC\_PCB}$: Junction to PCB thermal resistance; typical value = 1.5°C/W
$R_{\Theta JS}$ case to heatsink thermal resistance (depends on thermal interface material (TIM), around 0.5 °C/W typical)
$R_{\Theta JA}$: heatsink thermal resistance

Example:

$$R_{\theta SA} = \frac{150-105}{0.6} - 1.5 - 0.5 = 73°C/W$$

Equation 43 Example calculation of the heatsink's thermal resistance

This means that the chosen heatsink's thermal resistance must be less than or equal to approximately 73 °C/W for the power stage to keep its junction temperature within safe limits at 0.6 W dissipation with these temperature assumptions.

If the ambient temperature is higher or a more conservative junction temperature is needed, this value will decrease accordingly.

For a good heatsink design, consider the following design recommendations.

- Consider heatsink base dimensions and optimize the fin design for airflow and heat dissipation
- For natural convection, a large surface area with a moderate fin height and spacing is recommended. For forced convection, a smaller fin spacing and airflow velocity enhance the heat dissipation
- Choose a heatsink material with good thermal conductivity (e.g., aluminum, ~205 W/m-K)
- For natural convection, heatsink size might be approximately a few mm in all dimensions (e.g., 50 mm × 50 mm × 25 mm), with fin spacing optimized at approximately 2.5 mm to 5 mm based on airflow
- If forced airflow is available, smaller heatsinks or closer fin spacing may be used to achieve the target thermal resistance

7.1.4 Mounting recommendations

- Use a thermal interface material (TIM) like thermal pads or paste to reduce the case-to-heatsink thermal resistance
- Mount the heatsink securely and flat against the TLF12505A package or the PCB area with exposed thermal pads
- Ensure good electrical isolation via insulated heatsink mounts or pads (if required)
- Provide clearance for air circulation through fins
- Arrange heatsinks in a staggered manner to maximize airflow if multiple units are being used

7.1.5 Copper area recommendations for PCB

- A large, exposed copper area under TLF12505A on the PCB helps transfer heat away from the device
- The typical recommended copper area for TLF12505A is at least several square centimeters (~4 cm^2 or more) to achieve a lower thermal resistance and better heat spreading
- Surface-mount TLF12505A on the PCB with optimized copper area and thermal vias underneath as part of the thermal path
- Use multiple PCB layers with thermal vias connected to this exposed pad area for enhanced heat dissipation
- Ensure good thermal connection by soldering the exposed pad of the PQFN 5 mm × 6 mm package properly to the copper area

8 PCB layout guidelines for TLF12505A power stage

Note: This PCB layout guideline is intended to assist CAD designers in achieving the best layout practices when using Infineon power stages. However you should review the layout with PCB design experts before fabricating the PCB.

For optimal performance, power density, and thermal management of the TLF12505A power stage, a robust PCB copper pour, layer stackup, and via strategy are essential.

8.1 Layer stackup recommendations

- A minimum of 6 to 8 layers are preferred for handling high current and effective heat spreading. Higher-layer boards (8 to 10 layers) offer low-noise systems and greater reliability in high-power-density applications
- Assign multiple layers (at least 20–30%) for ground and power planes for heat spread and noise suppression
- Maintain good symmetry across the stack to avoid warping during manufacturing
- Route high-current/power layers between two solid, unbroken ground planes to minimize electromagnetic interference and increase heat dissipation

Infineon's solution development board "SDB901-The OPTIREG™ Multiphase Multiloop Power Solution for AD and ADAS" [7] layer stackup recommendations are mentioned in Table 3.

Table 3 Layer stackup recommendations

Layer	Name	Description
1	TOP	Power components like TLF12505A power stages, inductors, input and output capacitors
2	GND_PWR	Solid ground plane
3	SIG	Signals like PWM gate drive, current measurement, temperature measurement
4	GND_PWR	Power plane/ground plane
5	GND_PWR	Power plane/ground plane
6	GND_PWR	Power plane/ground plane
7	GND_PWR	Power plane/ground plane
8	SIG	Signals like PWM gate drive, Current measurement, temperature measurement
9	GND_PWR	Solid ground plane
10	Bottom	Components, signals, ground, or power pour

TLF12505A power stage placement on the top layer is shown in Figure 14 along with filter capacitors.

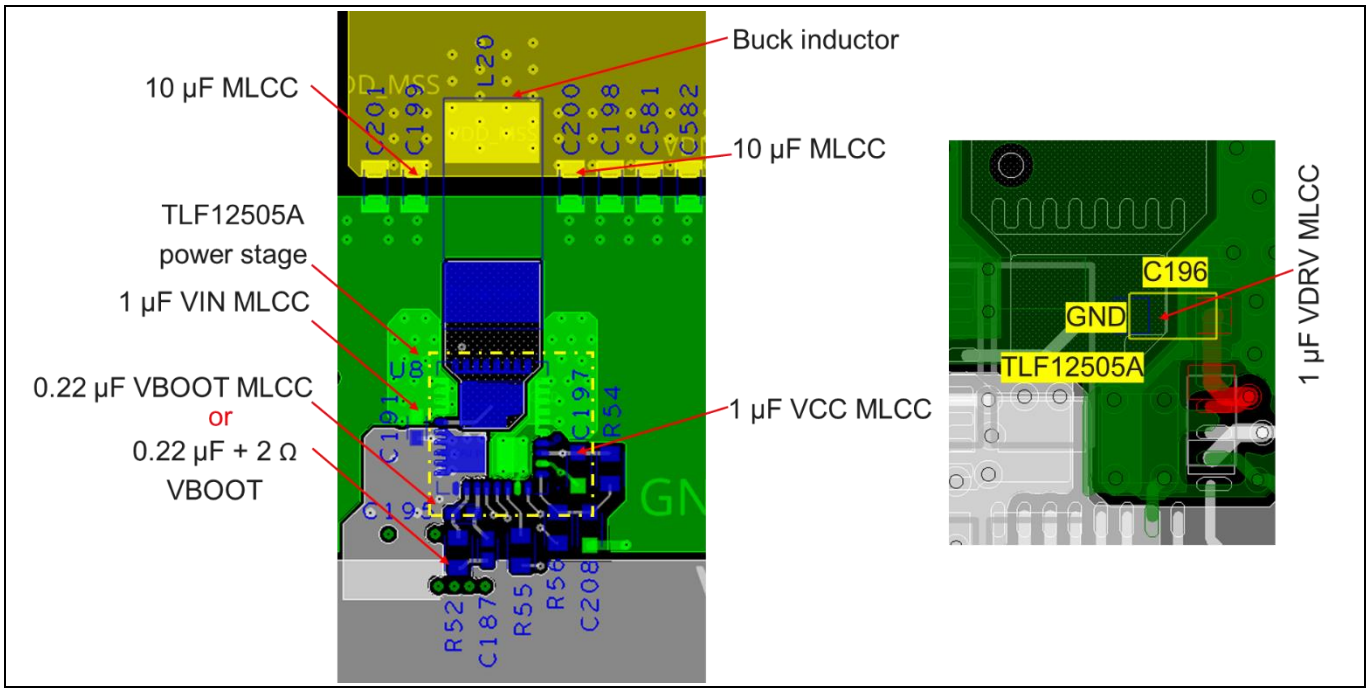


Figure 14 Components placement; top layer (left) and bottom layer (right)

Figure 15 shows the placement of the TLF12505A power stage for a multiphase application along with the filter capacitors on the top layer. Note that strategically placed thermal vias within an inductor's pads improve thermal performance by efficiently transferring heat to an internal or bottom copper plane.

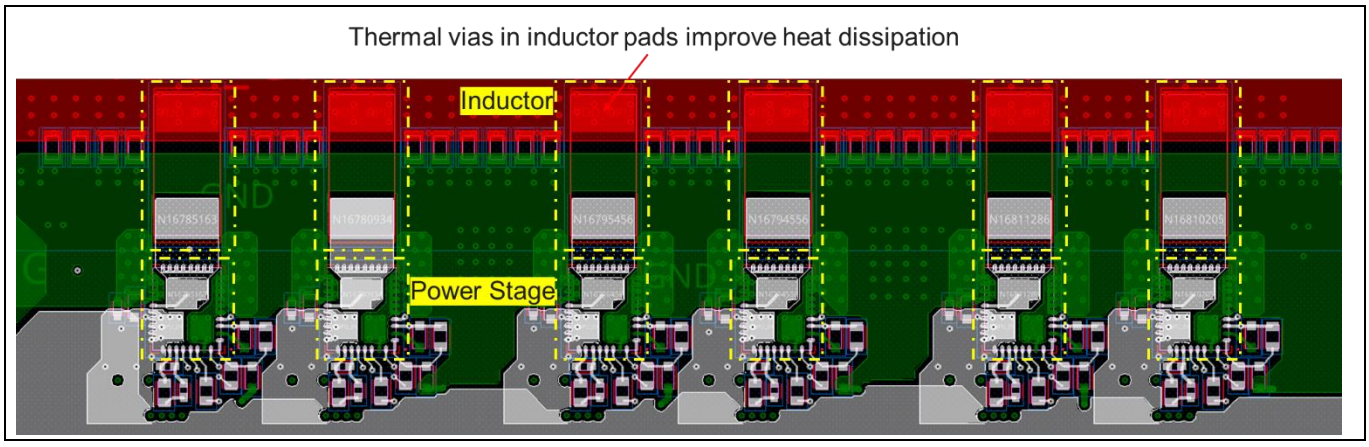


Figure 15 TLF12505A in multiphase configuration

Follow the best practices for routing the IMON and IMONREF differential pair traces, as shown in Figure 16.

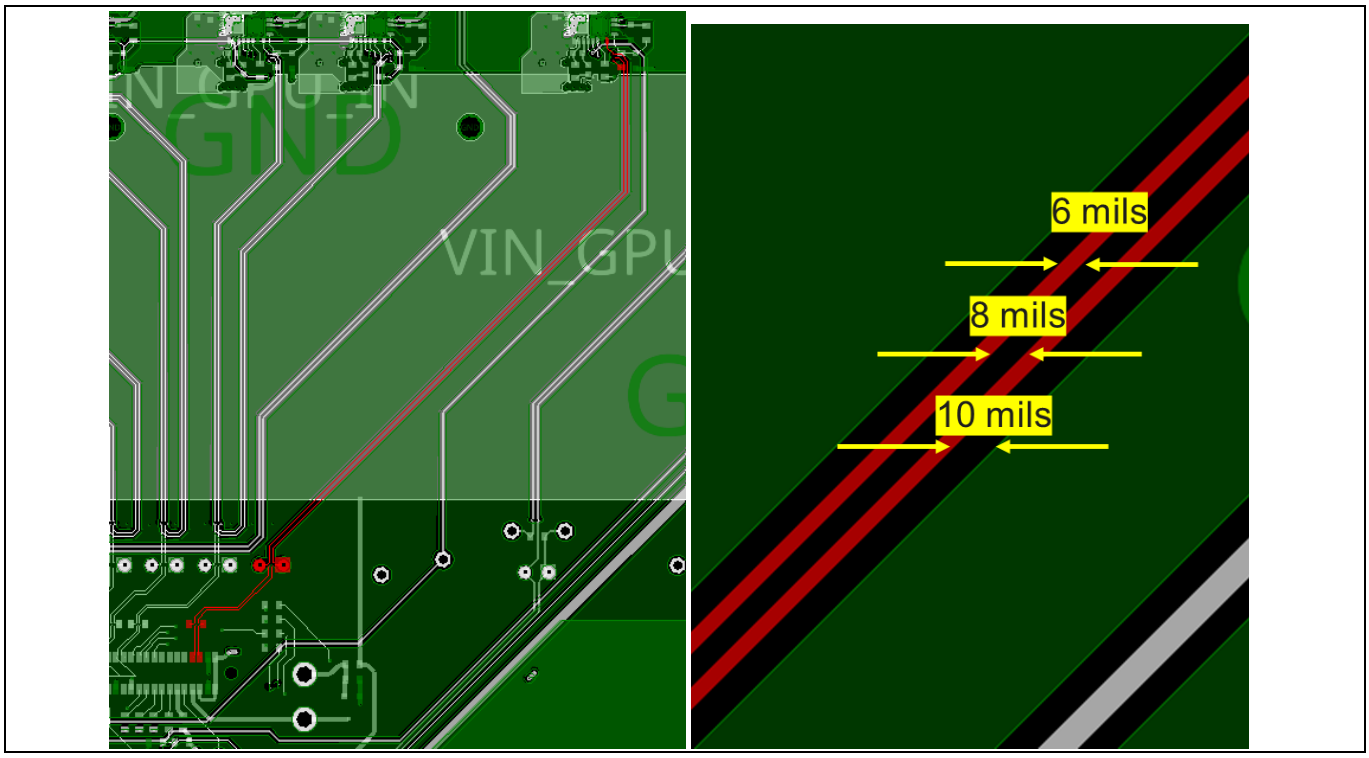


Figure 16 IMON and IMONREF traces routing

- Minimum trace width = 5–10 mil
- Minimum air gap between the traces = 6 mil
- Typical trace to shape distance = 10–15 mil
- For optimal performance, use the shortest possible traces to connect a 1 kΩ resistor between the IMON and IMONREF pins
- In this example, the IMON and IMONREF traces are routed on the top and third layers of the PCB

Follow the best practices for routing PWM signals from MPC to power stage TLF12505 A, as shown in Figure 17

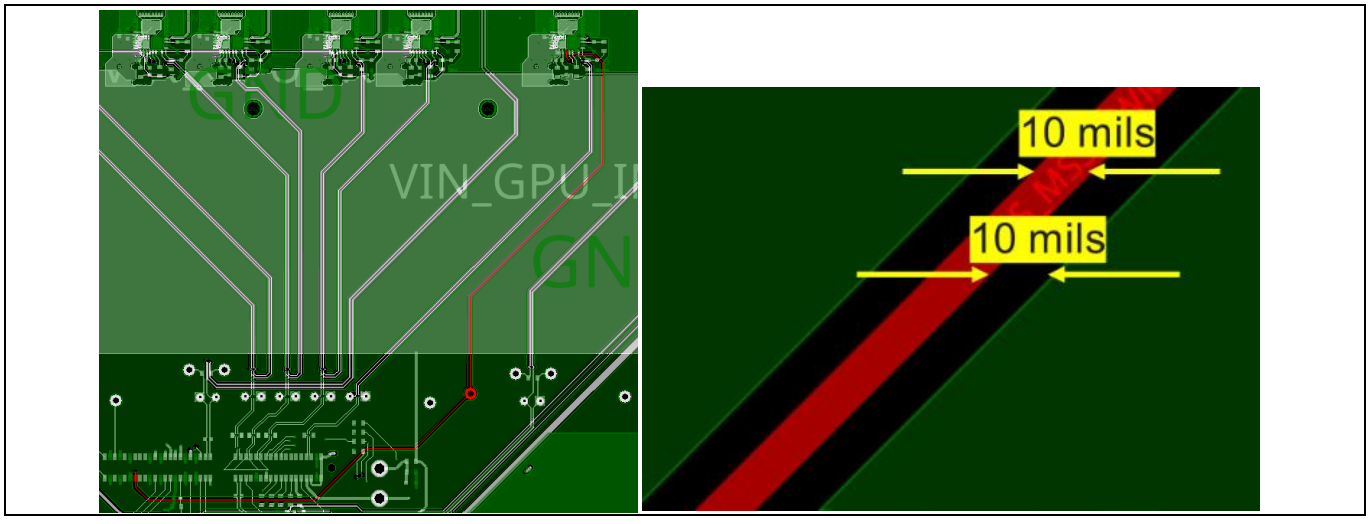


Figure 17 PWM signals traces routing

- Route the PWM gate traces away from noisy power traces to avoid signal interferences
- When two power stages are driven by the same PWM signal, route the signals into a star configuration with equal length traces. This ensures that each power stage receives the signal at the same time with minimal degradation, preventing timing errors and maintaining system efficiency
- Minimum trace width = 8–10 mil
- Typical trace to shape distance = 10–12 mil
- The PWM signal trace is routed on the top and third layers of the PCB

Figure 18 shows the component placement and routing of VCC and VDRV circuits.

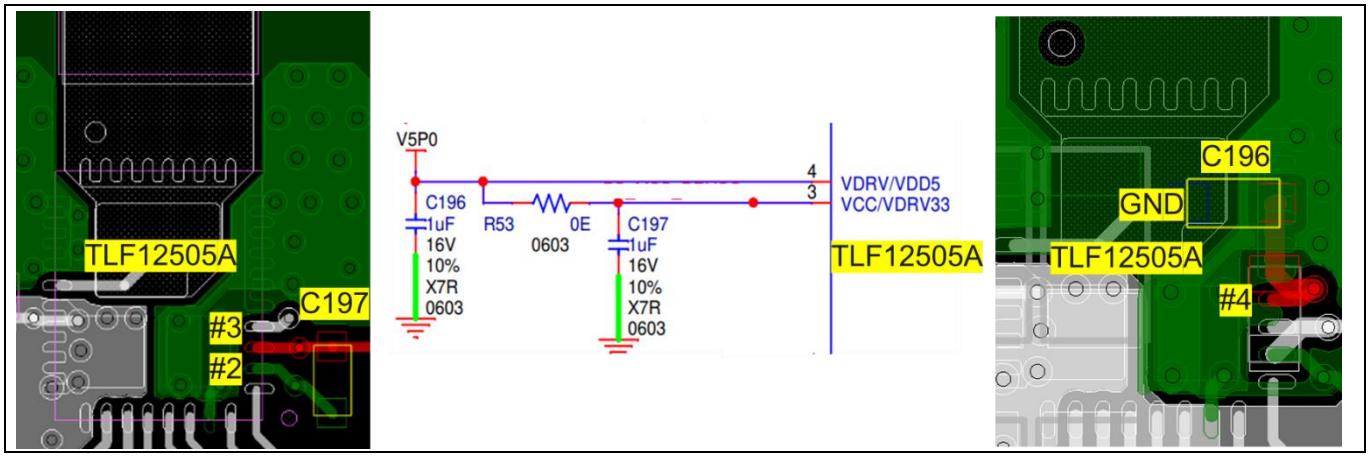


Figure 18 Component placement and routing of VCC and VDRV signals

- Place a 1 µF X7R decoupling MLCC close to the VDRV pin, connecting it between VDRV and PGND
- Place a 1 µF X7R decoupling MLCC close to the VCC pin, connecting it between VCC and AGND

Figure 19 shows the component placement and routing of boot circuits.

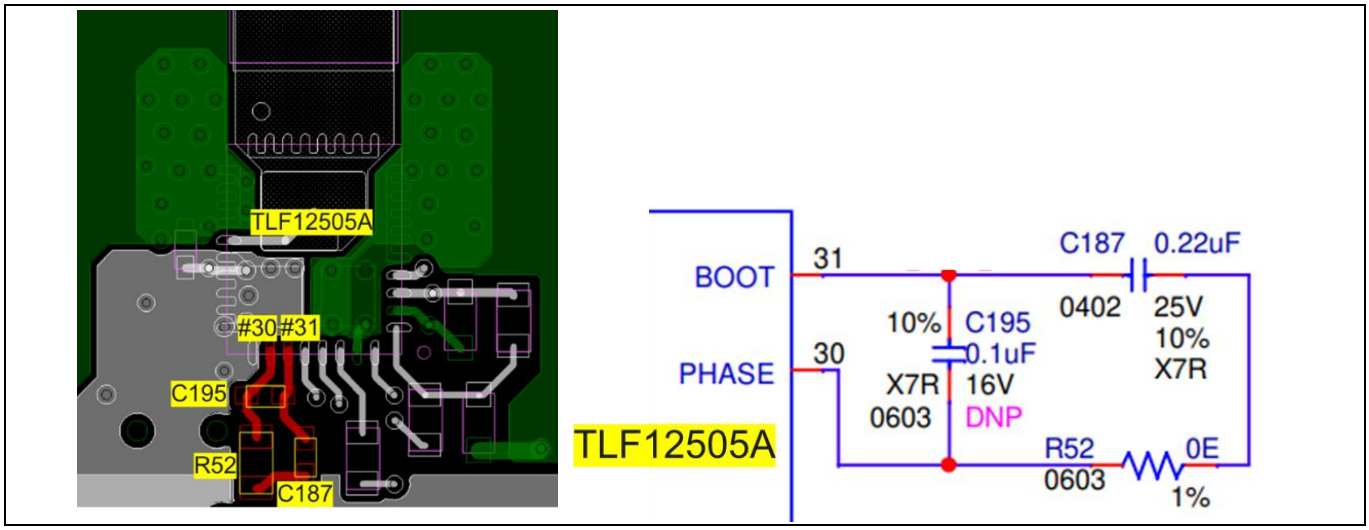


Figure 19 Placement and routing of boot signals

- 2 X7R multilayer ceramic capacitor between the BOOT and PHASE pins. The capacitor value should be between 0.22 µF and 0.56 µF, with 0.22 µF being the recommended value
- For input voltages above 13.2 V, a 2 Ω resistor should be placed in series with the multilayer ceramic bootstrap capacitor to mitigate switching node (SW) ringing and electromagnetic interference (EMI)

Figure 20 showos the routing of output voltage feedback traces.

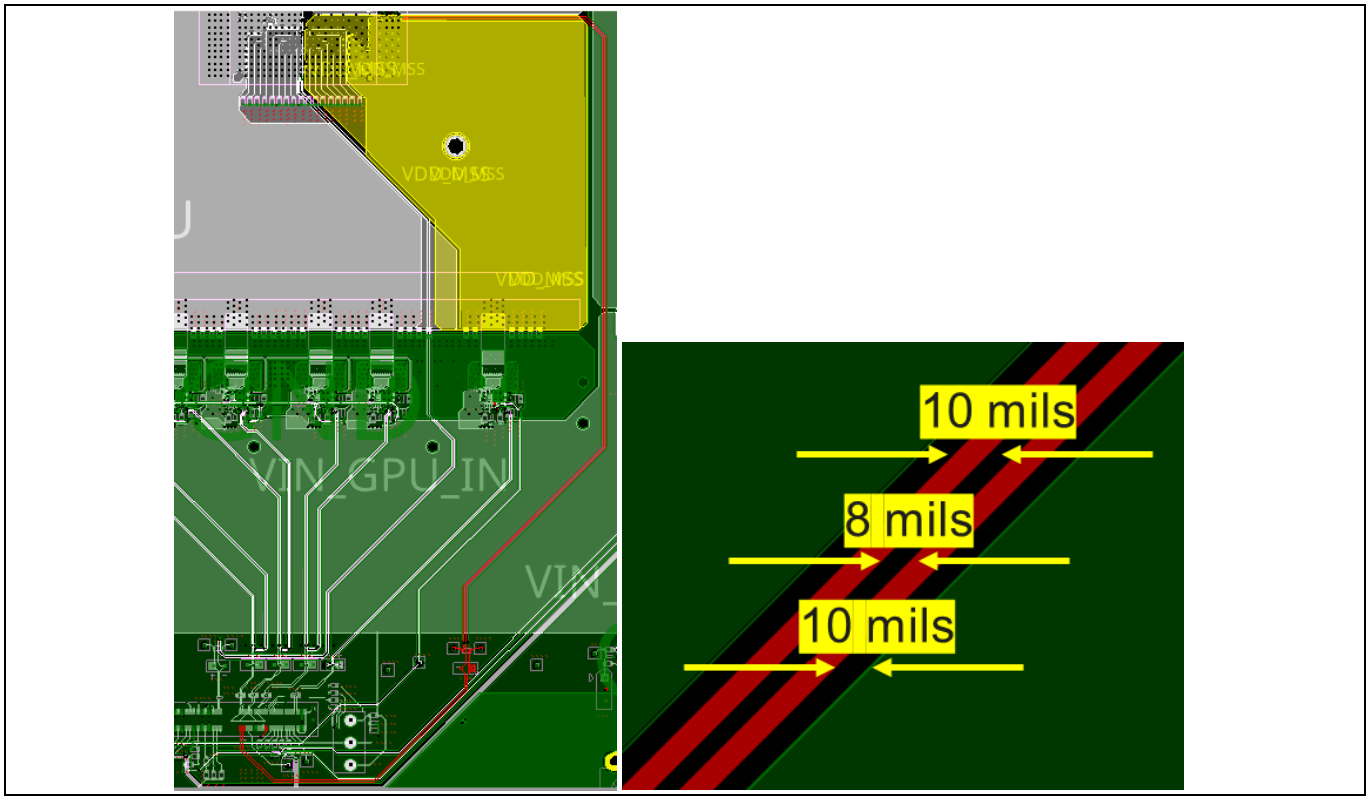


Figure 20 Routing of output voltage feedback traces

- Route the feedback trace from the buck converter output to the multiphase controller (MPC), ideally shielded by a ground plane and sandwiching between ground layers is preferred. The feedback signal is a high-impedance, noise-sensitive trace that should be kept away from the noisy switching node and inductor
- In this example, the differential signals for VOUT and GND are routed from the power stage's output to the multiphase controller (MPC) using both the top and third layers of the PCB

Figure 21 shows the placement of input multilayer ceramic capacitors, bulk capacitor, and buck inductor.

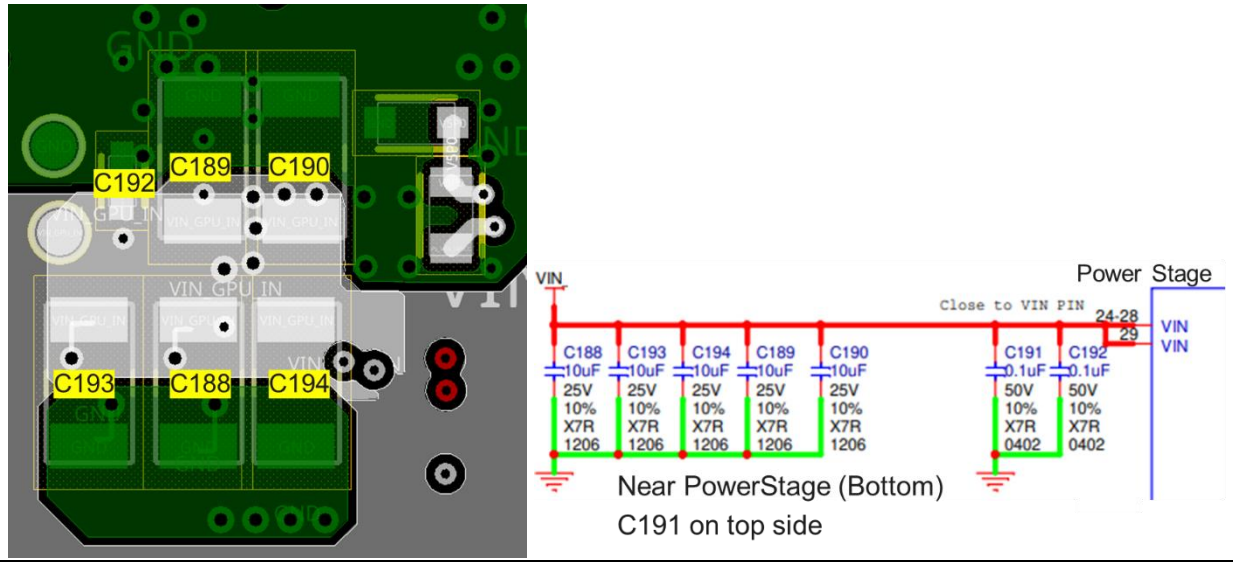


Figure 21 Input capacitors placement

- The placement of the input capacitor is a critical aspect of the PCB layout that directly impacts performance, noise, and reliability. The primary goal is to minimize the high-frequency current loop formed by the input capacitor, the power MOSFET, and the ground return
- The high-frequency MLCC should be placed close to TLF12505A's VIN and PGND pins. Note that trace length adds parasitic inductance, which can cause significant voltage spikes
- The MLCCs should be on the same PCB layer as TLF12505A. Avoid using vias for these critical connections, as vias add extra inductance that reduces the capacitor's effectiveness
- The loop formed by the input capacitor, TLF12505A's VIN pin, power ground (PGND) pin, and the capacitor's ground connection, must be as small as possible. Use wide, short traces or copper planes to reduce inductance
- The rapidly changing switching currents in the input stage generate electromagnetic interference (EMI), therefore, a compact, well laid out input capacitor loop is crucial to significantly reduce EMI and improve overall system performance
- Input bulk capacitors for a buck converter primarily handle lower-frequency energy storage and transient current demands from the input power supply, which is distinct from the high-frequency bypassing handled by ceramic capacitors
- The primary role of a bulk capacitor is to stabilize the voltage of the overall power bus. Therefore, a bulk capacitor should be placed near the voltage entry point, such as the power input connector or power supply output, to stabilize the voltage for all circuits on that bus
- Placing the bulk capacitor on the same side as the MLCC and TLF12505A is the most common practice. However, if space is limited, it can be placed on the opposite side of the board from TLF12505A, as their ground connection via inductance is less critical than that of the high-frequency multilayer ceramic capacitors

Figure 22 shows the placement of output capacitors.

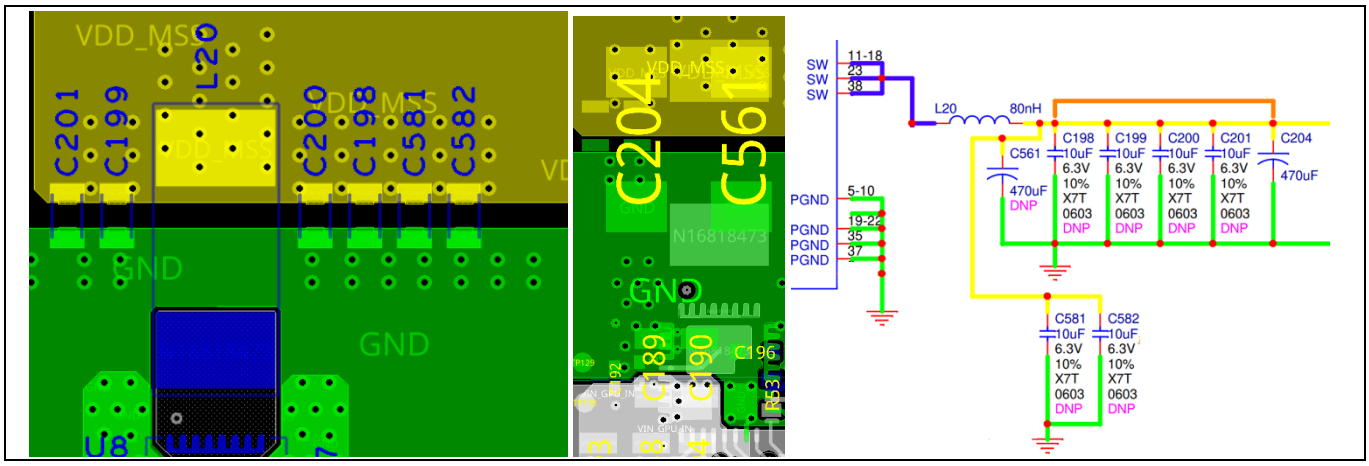


Figure 22 Placement of output capacitors

- Position the output capacitors immediately next to the inductor. This minimizes the length of the trace between the inductor and the capacitors, which helps smooth the output voltage ripple
- For sensitive loads like GPU, CPU, or FPGA, place some of the output capacitors directly at their input pins. This provides a low-inductance path to high-frequency current spikes, improving the transient load response
- Connect the ground terminal of the output capacitors to a solid ground plane with multiple vias. This creates a low-impedance, low-inductance return path for the output current
- The traces connecting the output capacitors to the inductor and the load should be as short and wide as possible. This minimizes parasitic inductance and resistance in the high-current path
- When using multiple output capacitors, the best practice is to combine low-ESR ceramic capacitors for high-frequency decoupling with bulk capacitors (such as electrolytic or polymer) for low-frequency filtering. The ceramic capacitors are placed close to the load to handle fast transients, while the bulk capacitors provide a larger energy reserve to improve load transients
- To efficiently dissipate the heat caused by high currents, an array of vias connects the inductor pad to large internal copper planes. This distributes the thermal load, preventing the formation of localized hot spots that can cause overheating. Place multiple numbers of 10 mil vias on each side of buck converter inductor mounting pads

Stencil aperture for solder paste is shown in Figure 23.

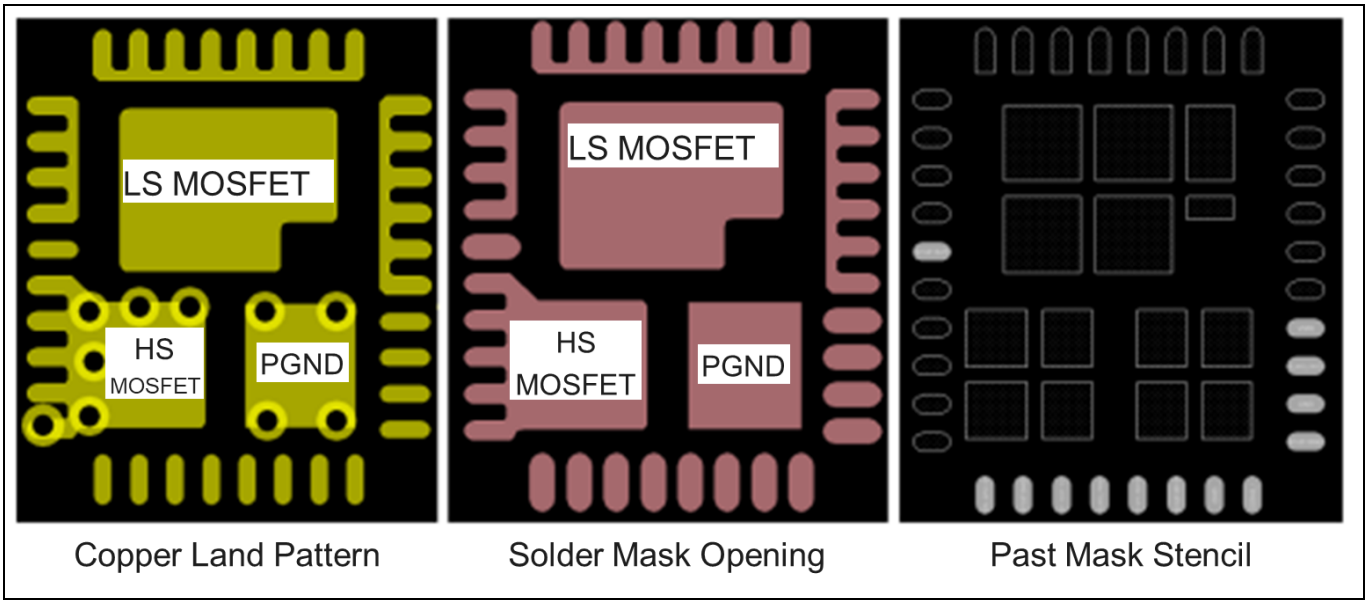


Figure 23 Stencil aperture for solder paste applied between VIN and GND vias under package

- 5 mm × 6 mm power stages are designed to work with VIN and GND vias under the package
- The recommended footprint and stencil design prevents solder from wicking into the vias under the package
- This via count maintains solder voids equal to or less than 35%

8.2 Via strategy

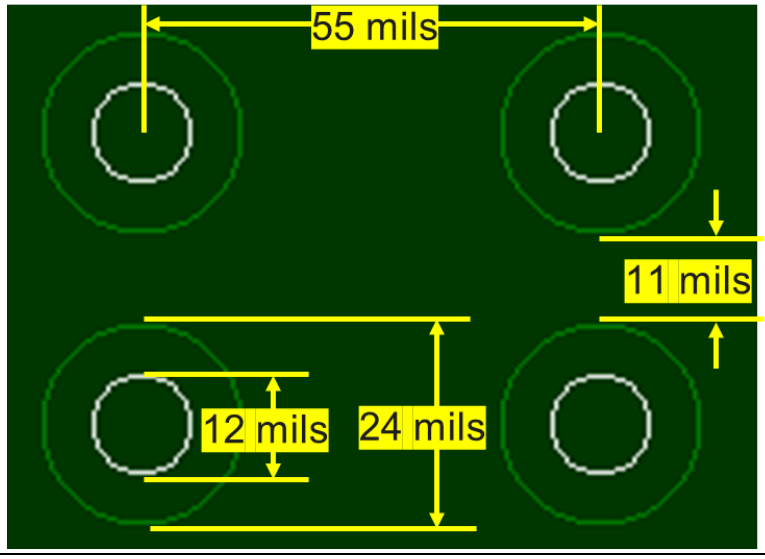


Figure 24 Vias strategy example

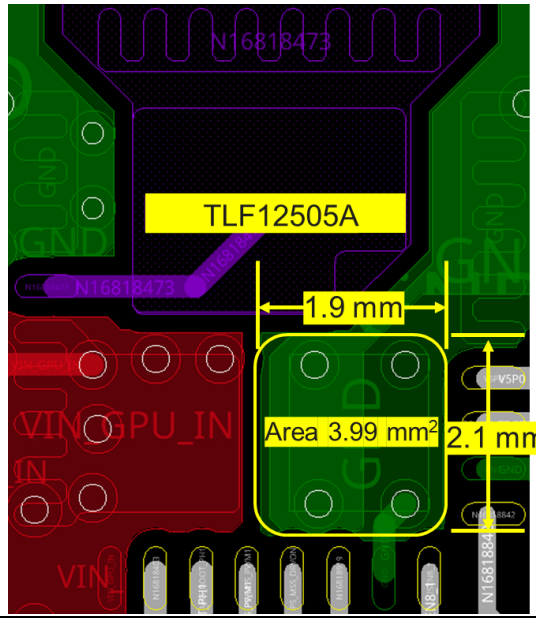


Figure 25 Thermal vias under power stage (exposed pad)

- Use dense via stitching (at least 1 via per mm^2) beneath TLF12505A's exposed pad. Connect all exposed pad vias to solid copper GND planes as shown in Figure 25
- Place thermal vias in a grid beneath copper pours in VIN, VOUT, and GND areas to allow efficient vertical heat transfer between layers
- For power and ground structures, stitch copper pours using rows or grids of vias along the edges and especially under/around high-power components
- Ensure that via current handling is adequate. Use multiple 0.3–0.5 mm vias in parallel for each high-current path
- Where EMI is a concern, implement via "fences" along board edges and beneath signal/ground transitions
- Recommended finished via hole size diameter: 12 mil with 24 mil via pad 12 mil drill bit. See Figure 24 for an example of vias strategy

Note: 8-mil finished hole size vias is the current industry standard for board thickness up to 120 mil.

- Minimum via to via center distance: 55 mil
- For 10-mil via drill, the allowed total thickness of the PCB is 63 mil (8 layers), 73 mil (10-12 layers), 93 mil (14-layers), 150 mil (22 layers)
- Use Type 7 vias for best thermal performance, especially if the board is wave-soldered or exposed to harsh environments
- Stitch additional thermal vias along the length of the main high-current pours (VIN and VOUT). Every 2–3 mm, insert a via down the length of the trace, plus at all choke and power FET connection points

8.3 Important practical tips

- Mount all decoupling capacitors (especially input, output, and bootstrap caps) as close as possible to their respective pins. Place them on the same layer as TLF12505A for minimal loop inductance
- Use low-inductance routing for the bootstrap capacitor, especially from BOOT to PHASE pins. Short, direct PCB traces are best
- Keep all high-current paths (gate, power, and ground) short and thick to minimize voltage drops and EMI
- Route the gate traces away from noisy power traces
- Place the thermal vias under the package's exposed pad and connect them to inner GND planes. This greatly reduces the junction temperature and improves the current handling
- Avoid slitting or segmenting ground planes beneath TLF12505A. An unbroken ground provides the most efficient thermal and electrical performance
- Ensure a proper separation between high- and low-voltage traces to prevent crosstalk and maintain signal integrity, complying with best automotive EMC practices
- Wherever possible, use polygon pours for high-power traces instead of narrow tracks to support high currents and thermal spreading
- Use wide copper pours for all high-current paths (VIN, VOUT, GND) connected to TLF12505A, especially on top and bottom layers
- Connect copper pours on all layers to a common net (usually GND) to minimize impedance and maximize both electrical and thermal conductivity
- Avoid "floating" or unconnected copper islands to prevent unwanted EMI and thermal hotspots
- Place ground planes adjacent to all high-current power planes or signal layers to serve as both return paths and heat spreaders
- Use dedicated, uninterrupted copper planes for both VIN and VOUT beneath the IC and output chokes for maximum current carrying and heat dissipation capacity
- Use thick copper (e.g., 2 oz or more) for all power and ground layers
- Avoid long, narrow pours. Keep all traces and pours as wide and short as possible
- Always connect thermal vias directly between exposed pads/pours and their referenced planes. Never connect thermal vias using long traces

8.4 Circuit schematic and PCB layout review checklist

Table 3 is a checklist for the key circuit schematic component choices. Table 4 is a checklist for the PCB layout guidelines. Please provide an answer to each checklist item to find out the extent to which your hardware design meets these guidelines.

Note: The silicon pinout details are based on TLF12505A [2]

Table 4 Circuit schematic checklist

Sl. No	Schematic checklist	Answer (Yes/No/NA)
1	Are the components chosen for the automotive application solution compliant with AEC-Q standards?	
2	Is the recommended bypass capacitor X7R 1.0 µF connected between VCC and AGND?	
3	Is the recommended bypass capacitor connected between VDRV and PGND a X7R 1 µF?	
4	Is the recommended configuration of 0402 MLCC with a value of 0.22 µF in series with a 2 Ω resistor, connected between the BOOT and PHASE pins?	
5	Is the recommended 1 kΩ resistor connected between IMON and IMONREF?	
6	Does the chosen power inductor support the maximum inductor current plus ripple current?	
7	Is the chosen power inductor a shielded, molded type?	

Table 5 PCB layout guidelines checklist

Sl. No	Schematic checklist	Answer (Yes/No/NA)
1	Have the recommended layer stackup guidelines been followed?	
2	Is the decoupling MLCC connected between VCC and AGND, and is it placed close to the VCC pin?	
3	Is the decoupling MLCC connected between VDRV and PGND, and is it placed close to the VDRV pin?	
4	To reduce trace inductance, were the bootstrap capacitor and resistor between the BOOT and PHASE pins routed with the shortest traces?	
5	Is a 1 kΩ resistor connected between IMON and IMONREF pins routed with the shortest traces?	
6	Are the input filter capacitors placed close to the VIN pin?	
7	Were the high frequency capacitors placed close to the half bridges to minimize the high di/dt loop area?	
8	Are the MLCCs on the same layer as TLF12505A?	
9	Are the MLCCs obstructing the heat sink?	
10	To ensure proper heat dissipation, has a large, exposed copper area been placed under TLF12505A on the PCB?	
11	To avoid signal interference, have the PWM gate traces been routed away from noisy power traces?	

Sl. No	Schematic checklist	Answer (Yes/No/NA)
12	Is a solid ground plane placed in layers adjacent to the MOSFET gate driver signal traces?	
13	To avoid noise pickup, were the MOSFET gate driver traces routed with short and wide paths?	
14	To ensure that each power stage receives the PWM signal at the same time and with minimal degradation, preventing timing errors and maintaining system efficiency, are the PWM signals routed in a star configuration with equal length traces when two power stages are driven from same PWM signal?	
15	To avoid signal interference, have the high frequency and low frequency signal traces been kept separated?	
16	Are there ground guarding traces running on either side of the IMON and IMONREF signals?	
17	Are the IMON and IMONREF signals routed differentially with a 6-mil air gap, using a 6 to 8 mil trace width?	
18	When using multiple power stages, is the EN (ENABLE) signal routed in a star configuration, and does it use 8 to 10 mil trace width?	
19	When using multiple power stages, is the TMON signal routed in a star configuration, and does it use 8 to 10 mil trace width?	
20	Are the PWM, TMON, and EN signals ground-guarded and sandwiched between two ground planes?	
21	Is a gap of 30 mils maintained between two different signals?	
22	Is a gap of 10 mils maintained between signal trace and its ground guarding trace?	
23	Is a trace width of 10 mils maintained for PWM trace?	
24	Have the high current paths (power, and ground) been designed to be short and wide to minimize voltage drops and EMI?	
25	Were polygon pours used for the high current traces, instead of narrow traces, to support high currents and improve thermal spreading?	
26	Have ground plane slits or segments been avoided beneath TLF12505A to ensure the most efficient thermal and electrical performance?	
27	Was a single ground plane placed beneath the power stage layer?	
28	Has the PCB layout incorporated sufficient ground vias adjacent to component ground pins to ensure a low impedance connection to the dedicated ground plane?	
29	Have the high and low voltage traces been separated to prevent crosstalk and maintain signal integrity, in compliance with automotive EMC practices?	
30	Have ground planes been placed adjacent to all high current power and signal layers to provide clear return paths, avoid crosstalk, and help with thermal spreading?	
31	For maximum current carrying and heat dissipation, have dedicated, uninterrupted copper planes been provided for both VIN and VOUT beneath the IC and output chokes?	
32	Were all floating or unconnected copper islands removed to prevent unwanted EMI and thermal hotspots?	
33	Have all unused areas been filled with copper and connected to the ground plane?	

Sl. No	Schematic checklist	Answer (Yes/No/NA)
34	Was the SW node area minimized to reduce EMI and noise?	
35	To prevent noise coupling, are high dv/dt nodes separated from sensitive small signal nodes?	
36	To avoid signal integrity and manufacturing issues, were sharp right-angle bends avoided?	
37	Given the high currents and thermal demands, is thick copper (e.g., 2 oz or more) being used for all power and ground layers?	
38	To reduce voltage drop and improve thermal efficiency, were wide copper pours used for the high current VIN, VOUT, and GND paths connected to TLF12505A on the top and bottom layers?	
39	Have the copper pours on all layers been connected to a common ground-net to minimize impedance and maximize electrical and thermal conductivity?	
40	To ensure minimal noise coupling, are the analog small signal and power grounds separated and connected at a single, quiet point?	
41	To minimize EMI, was the return current path kept as short as possible?	
42	Does the recommended PCB layout for TLF12505A include thermal vias beneath its exposed pad for heat transfer?	
43	Is dense via stitching (at least 1 via/mm^2) used for thermal dissipation underneath the TLF12505A's exposed pad, as recommended for power devices?	
44	Is the current handling for the thermal vias sufficient for optimal heat dissipation?	
45	To control EMI, has the design incorporated ground via fences as a shielding measure along the board edges and beneath signal return path transitions?	

9 Design example

Figure 26 is an example of ADAS in automotive applications. Typical ADAS application diagram including power stages shown in Figure 6.

Figure 26 Artistic rendering of ADAS applications – maintaining a safe distance from the vehicle in front (left) and pedestrian detection (right)

9.1 Role of TLF12505A in ADAS

The TLF12505A power stage device is an integrated smart power stage, essentially a power unit combining the gate driver, control MOSFET, and synchronous MOSFET in one package. In ADAS, it works with a digital multiphase controller (MPC) to create a robust and highly efficient multiphase buck converter.

The board shown in Figure 27 is based on Infineon OPTIREG™ TLF12505A power stages, designed to meet the demanding power delivery requirements of next-generation vehicles, particularly those equipped with artificial intelligence (AI)-driven Autonomous Driving (AD) and Advanced Driver Assistance Systems (ADAS) capabilities. The SDB901 board features four power delivery loops controlled by two multiphase controllers (MPC). The configuration of the loops is as follows:

- Loop A: Three phases with six power stages
- Loop B: Single-phase with one power stage
- Loop C: Two phases with two power stages
- Loop D: Two phases with two power stages

“SDB901: Solution Demo Board Test Report” [7] provides a detailed performance evaluation, including an in-depth analysis of efficiency, ripple, regulation, transient response, and thermal behavior under various operating conditions. The findings outlined in this document are intended to support system designers in optimizing performance and reliability for automotive applications.

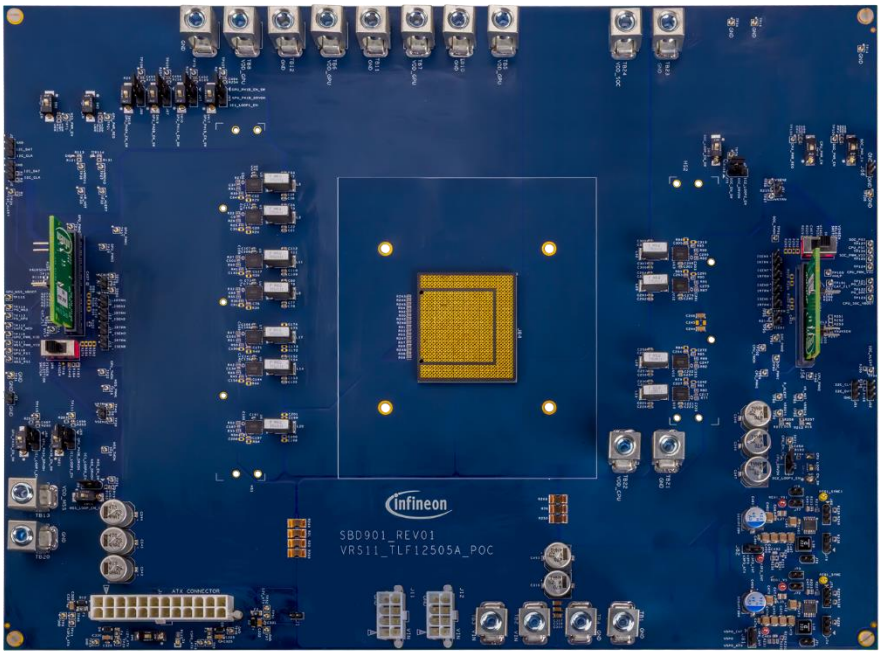


Figure 27 A design example of the SDB901 Solution Development Board for automotive ADAS applications

9.2 Key functions

- **High current supply:** Advanced ADAS SoCs which often include high-performance CPUs and GPUs can draw hundreds of amperes of current. The TLF12505A power stage device is designed to provide up to 60 A and can also be used in interleaved multiphase configurations to scale for even higher currents
- **High efficiency:** The TLF12505A power stage device minimizes resistance and inductance, which reduces power losses and allows the power supply to operate at very high switching frequencies (up to 2 MHz). This is vital for managing the heat generated by the dense electronics in a compact ADAS
- **Fast transient response:** ADAS have dynamic power needs, with instantaneous spikes in current when the SoC workload changes, such as when switching between applications. TLF12505A's quick response ensures that the core voltage remains stable during these sudden load changes
- **Compact design:** By integrating the critical components into a single, small package, it helps engineers design smaller, more compact electronic control units (ECUs). This is essential for modern vehicle interiors where space is a premium
- **Monitoring and protection:** Built in features like temperature reporting, over current protection, and thermal shutdown prevent from damage to the sensitive SoC and other components

9.3 Key features provided in the solution board

- High efficiency despite a compact design with minimal external components
- Automotive grade reliability (AEC-Q100 Grade 1) power stage
- Fast transient response and accurate voltage for sensitive ADAS electronics
- Deep sleep mode (<32 µA) for low standby current
- Fault/monitor outputs to automotive diagnostics system

9.3.1 TLF12505A integrated power stage

DC-DC converter:

- The TLF12505A integrated power stage acts as a high-efficiency DC-DC buck converter, taking the intermediate voltage rail (e.g., 12 V) and stepping it down to the very low voltage (e.g., 0.8 V) and high current (e.g., hundreds of amperes) required by the core processing units.
- The board has a total of four rails; loop A, loop B, loop C, and loop D showcase the functionality of interleaved multiphase buck converters and loop B delivers power with a single-phase buck converter

Output filter:

- An inductor (L) and capacitors (C) are used at the output of each rail to smooth the DC voltage supplied to the load, filtering out switching noise

“SDB901: Solution Demo Board User Guide” [8] provides clear, step-by-step instructions for setting up, operating, and evaluating the performance metrics of the multiphase, multiloop power stage board shown in Figure 27.

9.3.2 ADAS components in typical applications, loading the power stages

- **System on chip (SoC):** This is the ADAS central processing unit, which integrates the main processor, GPU, VPU, and other logic
- **Memory (DDR):** High-speed DDR memory for the SoC
- **Graphics processing unit (GPU):** In a high-end ADAS, dedicated GPUs accelerate AI models and process high-resolution sensor data
- **Central processing unit (CPU):** Manages overall system tasks, including task scheduling and managing data flow
- **Memory subsystem (MSS) and DDR:** High-speed DDR memory supports the processors, while the MSS controller manages access
- **FPGAs and accelerators:** Used for specific, high-speed, parallel tasks like preprocessing sensor data
- **Peripheral modules:** Other components that require high current, low voltage power, such as graphics processors and interface circuits

9.4 Design example calculations

The design specifications in Table 6 are for loop B of the solution board shown in Figure 27. These specifications help in calculating the power stage buck converter component values as shown in Table 7. The SDB901 power stage design calculator supports computing component values and ratings [10].

Table 6 Design inputs for Loop B

Parameter	Value	Units	Remarks
Input voltage	12.0	volts	V_{IN_MAX}
Output voltage	0.75	volts	V_{OUT}
Load current (TDC)	40	amps	I_{OUT}
Load current (Max)	55	amps	I_{OUT_MAX}
Switching frequency	650	kHz	f_{SW}
Number of power stages	1	–	N
PWM to power stage ratio	1	–	–
Chosen power inductor	80	nH	L
Inductor ripple current PK	27	%	ΔI_L
Input ripple peak-to-peak	0.24	volts	$\Delta V_{IN\_PK\_PK}$
DCLL Value	0	ohms	DCLL
V_{OUT} transient overshoot	0.2	volts	$\Delta V_{OUT\_OVERSHOOT}$
V_{OUT} transient undershoot	0.2	volts	$\Delta V_{OUT\_OVERSHOOT}$
Load transient current	55	A	ΔI_{OUT}
Efficiency	85	%	Estimated

Table 7 Power stage buck converter components calculation for Loop B

Parameter	Formula	Values
Input capacitor MLCC	$\frac{D_{BUCK} * (1 - D_{BUCK}) * I_{OUT\_MAX}}{\Delta V_{IN\_PK\_PK} * f_{SW}}$	24 µF
Input capacitor RMS current	$I_{CIN\_RMS} = I_{OUT\_MAX}\sqrt{D_{BUCK}(1 - D_{BUCK})}$	14.35 A
Output capacitor value (overshoot) without DCLL	$C_{OVERSHOOT} = \frac{Q_{OVERSHOOT}}{\Delta V_{OUT\_OVERSHOOT} + \Delta I_{OUT} * DCLL}$	807 µF
Output capacitor value (overshoot) with DCLL (0.01 Ω)		215 µF
Output capacitor value (undershoot) without DCLL	$C_{UNDERSHOOT} = \frac{Q_{UNDERSHOOT}}{\Delta V_{OUT\_UNDERSHOOT} + \Delta I_{OUT} * DCLL}$	54.0 µF
Output capacitor value (undershoot) with DCLL (0.01 Ω)		14 µF
Output capacitor RMS current	$I_{COUT\_RMS} = \frac{\Delta I_L}{\sqrt{12}} \cong 0.29\Delta I_L$	3.9 A
Power inductor peak-to-peak ripple current	$\Delta I_L = \frac{(V_{IN\_MAX} - V_{OUT}) * D_{BUCK}}{L_{BUCK} * f_{SW}}$	13.52 A
Power inductor RMS current	$I_{L\_RMS\_BUCK} = \sqrt{(I_{OUT\_MAX})^2 + \frac{(\Delta I_L)^2}{12}}$	55.19 A
Power inductor peak current	$I_{L\_MAX\_BUCK} = \frac{\Delta I_L}{2} + I_{OUT\_MAX}$	62.95 A
Power inductor	$L_{BUCK} = \frac{(V_{IN\_MAX} - V_{OUT}) * D_{BUCK}}{\Delta I_L * f_{SW}}$	86 nH

The design specifications in Table 8 are for loop A of the solution board shown in Figure 27. These specifications help in calculating the power stage buck converter component values as shown in Table 9. The SDB901 power stage design calculator supports computing component values and ratings [10].

Table 8 Design inputs for Loop A

Parameter	Value	Units	Remarks
Input voltage	12.0	volts	V_{IN_MAX}
Output voltage	0.75	volts	V_{OUT}
Load current (TDC)	240	amps	I_{OUT}
Load current (Max)	420	amps	I_{OUT_MAX}
Switching frequency	650	kHz	f_{SW}
Number of power stages	3	–	N
PWM to power stage ratio	2	–	–
Chosen power inductor	80	nH	L
Inductor ripple current PK	27	%	ΔI_L
Input ripple peak to peak	0.24	volts	$\Delta V_{IN\_PK\_PK}$
DCLL Value	0.0005	ohms	DCLL
V_{OUT} transient overshoot	0.2	volts	$\Delta V_{OUT\_OVERSHOOT}$
V_{OUT} transient undershoot	0.2	volts	$\Delta V_{OUT\_OVERSHOOT}$
Load transient current	420	A	ΔI_{OUT}
Efficiency	85	%	Estimated

Table 9 Power stage buck converter components calculations for Loop A

Parameter	Formula	Values
Input capacitor MLCC	$\frac{D_{BUCK} * (1 - D_{BUCK}) * I_{OUT\_MAX}}{\Delta V_{IN\_PK\_PK} * f_{SW}}$	183 µF
Input capacitor RMS current	$I_{CIN\_RMS} = I_{OUT\_MAX}\sqrt{D_{BUCK}(1 - D_{BUCK})}$	29.3 A
Output capacitor value (overshoot) without DCLL	$C_{OVERSHOOT} = \frac{Q_{OVERSHOOT}}{\Delta V_{OUT\_OVERSHOOT} + \Delta I_{OUT} * DCLL}$	8000 µF
Output capacitor value (overshoot) with DCLL (0.0013 Ω)		2000 µF
Output capacitor value (undershoot) without DCLL	$C_{UNDERSHOOT} = \frac{Q_{UNDERSHOOT}}{\Delta V_{OUT\_UNDERSHOOT} + \Delta I_{OUT} * DCLL}$	523.0 µF
Output capacitor value (undershoot) with DCLL (0.0013 Ω)		139 µF
Output capacitor ripple current	$I_{COUT\ (ripple)} = \frac{N}{D_{Buck} * (1 - D_{Buck})} * \left(D_{Buck} - \frac{m}{N}\right) * \left(\frac{1 + m}{N} - D_{Buck}\right) * \Delta I_L$	6.69 A
Output capacitor RMS current	$I_{COUT\ (ripple)}$ / sqrt(12)	1.93 A
Power inductor peak-to-peak ripple current	$\Delta I_L = \frac{(V_{IN\_MAX} - V_{OUT}) * D_{BUCK}}{L_{BUCK} * f_{SW}}$	15.9 A
Power inductor RMS current	$I_{L\_RMS\_BUCK} = \sqrt{(I_{OUT\_MAX})^2 + \frac{(\Delta I_L)^2}{12}}$	70.15 A
Power inductor peak current	$I_{L\_MAX\_BUCK} = \frac{\Delta I_L}{2} + I_{OUT\_MAX}$	77.95 A
Power inductor	$L_{BUCK} = \frac{(V_{IN\_MAX} - V_{OUT}) * D_{BUCK}}{\Delta I_L * f_{SW}}$	67 nH

10 Troubleshooting

10.1 VCC/VDRV undervoltage lockout (UVLO)

The VCC/VDRV undervoltage lockout (UVLO) functionality has been described in Section 6.1. To test and troubleshoot the feature:

1. Test by gradually lowering the supply voltages (VCC and VDRV) below the UVLO threshold. Limits are mentioned in the data sheet [2]
2. Confirm that the device stops switching, PWM pin is pulled LOW, and TMON/FAULT pin pulls LOW, indicating a non-catastrophic fault
3. Restore the voltage and verify that the normal operation resumes

10.2 Thermal shutdown/overtemperature protection (OTP)

The thermal shutdown/overtemperature protection (OTP) functionality has been described in Section 6.2. Thermal limits are mentioned in the datasheet [2]. To test and troubleshoot the feature:

1. Test with controlled temperature increase of the device junction using a thermal chamber or hot plate
2. Confirm that at approximately 155°C, switching stops, both MOSFETs turn off, and TMON/FAULT pin pulls HIGH
3. Reduce temperature and verify the device resumes operation below 143°C threshold

10.3 Cycle-by-cycle overcurrent protection (OCP)

The cycle-by-cycle overcurrent protection (OCP)functionality has been described in Section 6.3. OCP limits are mentioned in the datasheet [2]. To test and troubleshoot the feature:

1. Apply a current exceeding the nominal threshold (example ≈ 100 A) to the inductor load
2. Verify that during overcurrent events, PWM high pulses are truncated to allow current relaxation

10.4 Negative overcurrent protection

The negative overcurrent protection (NOCP) functionality has been described in Section 10.4. NOCP limits are mentioned in the datasheet [2].

1. Induce a negative current spike exceeding the NOCP value
2. Verify that the high-side MOSFET is enabled for 200 ns to suppress negative current
3. Confirm that the normal operation continues after suppression

10.5 Control MOSFET short detection (High-side MOSFET short – HSS)

The control MOSFET short detection (high-side MOSFET short – HSS) functionality has been described in Section 6.5. HSS limits are mentioned in the datasheet. To test and troubleshoot the feature:

1. Create a short-circuit condition on the high-side MOSFET node to raise the voltage difference across the MOSFET (Q2) and power ground above 560 mV
2. Confirm fault detection with TMON/FAULT pin pulling HIGH after an approximately 150 ns delay

10.6 Bootstrap capacitor undervoltage

The bootstrap capacitor undervoltage functionality has been described in Section 6.6. Bootstrap capacitor undervoltage limits are mentioned in the datasheet [2]. To test and troubleshoot the feature:

1. Remove or disable the bootstrap capacitor or reduce its voltage below the required threshold
2. Confirm that the TMON/FAULT pin pulls HIGH indicating a catastrophic fault
3. Verify that the power stage does not operate without sufficient bootstrap voltage

These procedures involve applying appropriate electrical and thermal stresses while monitoring the TMON/FAULT pin, PWM signal behavior, and device temperature, ensuring that each protection mechanism activates as specified in the datasheet. This comprehensive validation ensures reliable protection and fault signaling in real-world applications.

10.7 PWM input to TLF12505A

Confirm the PWM level compatibility (3.3 V, tolerant up to 5 V). A High-Z condition on the PWM sets body braking or diode emulation modes. Typical symptoms and actions are mentioned in Table 10.

Table 10 Typical symptoms and actions

Symptoms	Likely cause	Action
No switching, TMON/FAULT = 0 V	VDRV UVLO	Check VCC/VDRV supply, raise voltage
No switching, TMON/FAULT = 3.3 V	Overtemperature or boot fault	Check cooling/replace bootstrap cap
Cyclic fault under load	Overcurrent protection active	• Reduce load • Check inductor/MOSFET ratings
Device remains in deep sleep	EN pin low	Pull EN high
Unexpected high temperature reading	Faulty TMON pin or sensing	• Verify TMON wiring • Correct offset/gain
No switching	PWM input is lower than 3 V	Check the functionality of MPC output

11 Reliability and lifetime costs of power stage options

The reliability and lifetime cost comparison between TLF12505A and alternative power stages for automotive AI loads involves several key factors:

11.1 Reliability factors

Thermal cycling stress: Power stages, including TLF12505A, undergo thermal cycling due to load changes. The magnitude and frequency of temperature swings significantly impact device lifetime. TLF12505A's optimized thermal design and package improve resistance to thermal fatigue relative to typical alternatives.

Electrothermal behavior: Lifetime depends not only on average junction temperature but on fluctuations caused by load and ambient conditions. TLF12505A with integrated temperature telemetry enables better real time monitoring for predictive maintenance and enhanced reliability planning.

Robust protections: Integrated protections in TLF12505A (overcurrent, undervoltage, thermal shutdown) reduce stress and failure risks during transient events versus some alternatives lacking full integration.

Automotive qualification: TLF12505A's AEC-Q100 Grade 1 qualification assures strict automotive reliability standards that may exceed those of generic or non-automotive power stages.

11.2 Lifetime cost considerations

Maintenance and replacement frequency: Higher reliability reduces downtime and maintenance costs. TLF12505A's telemetry and protections extend operational life, reducing lifecycle expenses compared to less integrated designs which may require earlier replacements.

Efficiency impact: Higher efficiency reduces operating losses and cooling requirements, decreasing total energy cost and auxiliary system complexity over product lifetime. TLF12505A's OptiMOS™ devices typically achieve higher efficiency, decreasing lifetime power losses.

System level cost: Initial cost differences must be balanced with savings from lower system sizing (e.g., smaller heatsinks, fewer replacements). Simulation studies show that converters with better efficiency and reliability can lower total lifetime cost despite slightly higher initial prices.

Predictive lifetime modeling: Infineon's Power System Reliability Modeling (PSRM) technology, present in TLF12505A ecosystems, enables real-time health monitoring and lifetime estimation, facilitating optimized operation and minimizing risk of unexpected failures.

TLF12505A offers superior thermal performance, integrated protections, telemetry capabilities, and automotive grade reliability translate to longer device lifetime, less frequent replacements, and reduced system operational costs. The net effect is a lower total cost of ownership (TCO) and improved availability for critical AD and ADAS applications. This holistic reliability and cost assessment is essential for the demanding environments of automotive AI power systems.

12 Summary

TLF12505A is an automotive grade integrated power stage from Infineon featuring an integrated driver and control and synchronous MOSFETs. It supports a wide input voltage range from 4.25 V to 20 V, delivers an output current of up to 60 A (with a max of 100 A), and operates at frequencies up to 2 MHz. TLF12505A includes advanced features such as integrated current sensing, temperature reporting, and comprehensive protection mechanisms like overcurrent, thermal shutdown, and bootstrap undervoltage protection. It is qualified to meet AEC-Q100 Rev H Grade 1 standards, optimized for automotive applications like ADAS and automotive computing, ensuring high efficiency, reliability, and reduced component count in power supply designs [1], [2].

In short, TLF12505A is a high-performance, automotive grade power stage optimized for AD and ADAS applications, providing reliable, efficient power management critical for the operation of autonomous and driver assistive systems in modern vehicles.

Acronyms and abbreviations

Table 11 Acronyms and abbreviations

Acronyms/abbreviations	Expansion
AD	Autonomous Driving
ADAS	Advanced Driver Assistance System
AEC-Q100	Automotive Electronics Council qualification standard
CAN	Control Area Network
DDR	Double Data Rate (a type of high-speed memory)
ESR	Equivalent Series Resistance
HTOL	High-Temperature Operating Life
HSSL	High-Speed Serial Link
LIN	Local Interconnect Network
MLCC	Multilayer Ceramic Capacitor
MSS	Memory Subsystem
OTP	Overtemperature Protection
OVP	Overvoltage Protection
PMIC	Power Management Integrated Circuit
PoL	Point of Load
PCIe	Peripheral Component Interconnect Express
PSEQ	Power Sequencer
SERDES	Serializer/deserializer
UVP	Undervoltage Protection
VMON	Voltage Monitor
VPU	Vision Processing Unit

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