Latest Infineon trench 120 V power MOSFET technology

Three-phase power inverter board using OptiMOS™ 120 V TOLL MOSFET

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About this document

Scope and purpose

This application note introduces Infineon's new OptiMOS™ 6 120 V power MOSFET technology in the TO-leadless (TOLL) power package. It is based on Infineon's latest trench MOSFET technology, which provides exceptionally low on-state resistance combined with faster switching performance. The best-in-class (BiC) 120 V MOSFET IPT017N12NM6 is primarily targeted for applications where 100 V MOSFETs do not provide enough V_{DS} margin for switch-off transients but at the same time benefit from lower $R_{DS(on)}$ than 150 V devices. These power MOSFETs are used to address high-power applications, such as battery-powered power tools, solar inverters, and SMPS. Additionally, in this document a detailed description of the functionalities of the Infineon EVAL_TOLL_72VDC_2kW evaluation power board for battery-powered brushless direct current (BLDC) motor-drives is presented. This board is used to drive three-phase BLDC motors with Hall sensors used for rotor position detection, using pulse-width modulation (PWM) six-step (block) commutation control to regulate the speed of the motor. This power board uses OptiMOS™ 6 120 V power MOSFETs on each phase of the three-phase inverter to showcase the performance achieved by this state-of-the-art device technology. The control firmware is developed to operate with Infineon's XMC1300 drive card.

Intended audience

This document is intended for manufacturers of battery-powered power tools and engineers familiar with three-phase motor-drive systems and motor controls.

Infineon components featured

- **IPT017N12NM6**, 120 V, 1.7 mΩ TOLL N-channel power MOSFET
- **IRLML6346TRPBF**, 30 V, 3.4 A, SOT-23, N-channel MOSFET
- **1EDN8550B**, single-channel non-isolated gate driver IC family with truly differential inputs
- **ILD8150EXUMA1**, buck regulator controller with integrated MOSFET
- **KIT_XMC1300_DC_V1**, motor-drive control card



Figure 1 Isometric image of evaluation power board (EVAL_TOLL_72VDC_2kW)

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Note: Please note the following warnings regarding the hazards associated with development systems.

Table 1 Safety precautions

	**Warning:** *The DC link potential of this board is up to 100 V DC. Ensure the polarity is correct, otherwise the board will be damaged!* *When measuring voltage waveforms by oscilloscope, high-voltage differential probes are required. Failure to use correct probes may result in damage, personal injury or death.*
	**Warning:** *The evaluation or reference board contains DC bus capacitors, which take time to discharge after removal of the main supply. Before working on the drive system, wait five minutes for capacitors to discharge to safe voltage levels. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Warning:** *The evaluation or reference board is connected to the grid input during testing. Hence, high-voltage differential probes must be used when measuring voltage waveforms by oscilloscope. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Warning:** *Remove or disconnect power from the drive before you disconnect or reconnect wires, or perform maintenance work. Wait five minutes after removing power to discharge the bus capacitors. Do not attempt to service the drive until the bus capacitors have discharged to zero. Failure to do so may result in personal injury or death.*
	**Caution:** *The heatsink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.*
	**Caution:** *Only personnel familiar with the drive, power electronics and associated machinery should plan, install, commission and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.*
	**Caution:** *The evaluation or reference board contains parts and assembly's sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	**Caution:** *A drive that is incorrectly applied or installed can lead to component damage or reduction in product lifetime. Wiring or application errors such as undersizing the motor, supplying an incorrect or inadequate AC supply, or excessive ambient temperatures may result in system malfunction.*
	**Caution:** *The evaluation or reference board is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials that are unnecessary for system installation may result in overheating or abnormal operating conditions.*

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1 Introduction

1.1 Overview

Recent trends toward higher efficiency, higher power density, and higher system reliability are the key factors driving Infineon to constantly introduce new highly innovative power MOSFET technologies to enhance system performance. Infineon's extensive experience in trench MOSFET technology together with the knowledge gained from customer feedback are behind the development of the new OptiMOS™ 6 120 V MOSFETs [1]. The new OptiMOS™ 6 120 V power MOSFET technology offers devices with extremely low on-state resistance as well as very low gate charges, yielding the industry's best figure-of-merit (FOM). Thus, these devices are optimized for high-frequency SMPS and high-power motor-drive applications. The new OptiMOS™ 6 120 V in TOLL package has a 50 percent bigger solder contact area enabling lower current density, leading to reduced electromagnetic-interference (EMI) at high current levels and temperatures, resulting in higher system reliability [2].

The new OptiMOS™ 6 120 V technology introduces a novel cell design taking advantage of a full tri-dimensional charge compensation principle, leading to a significant improvement in $R_{DS(on)}$. Additionally, the new cell structure design leads to a completely redesigned gate trench, enabling a reduction of gate-drain charge (Q_{gd}) and total gate charge (Q_g) [1].The introduction of metal gate technology leads to uniform switching within the die area by accurately controlling the R_G [1]. Moreover, the metal gate technology proves to be an effective intrinsic barrier against false turn-on of the MOSFETs [1]. Figure 30 shows the device structure of a conventional trench MOSFET vs. latest trench MOSFET.

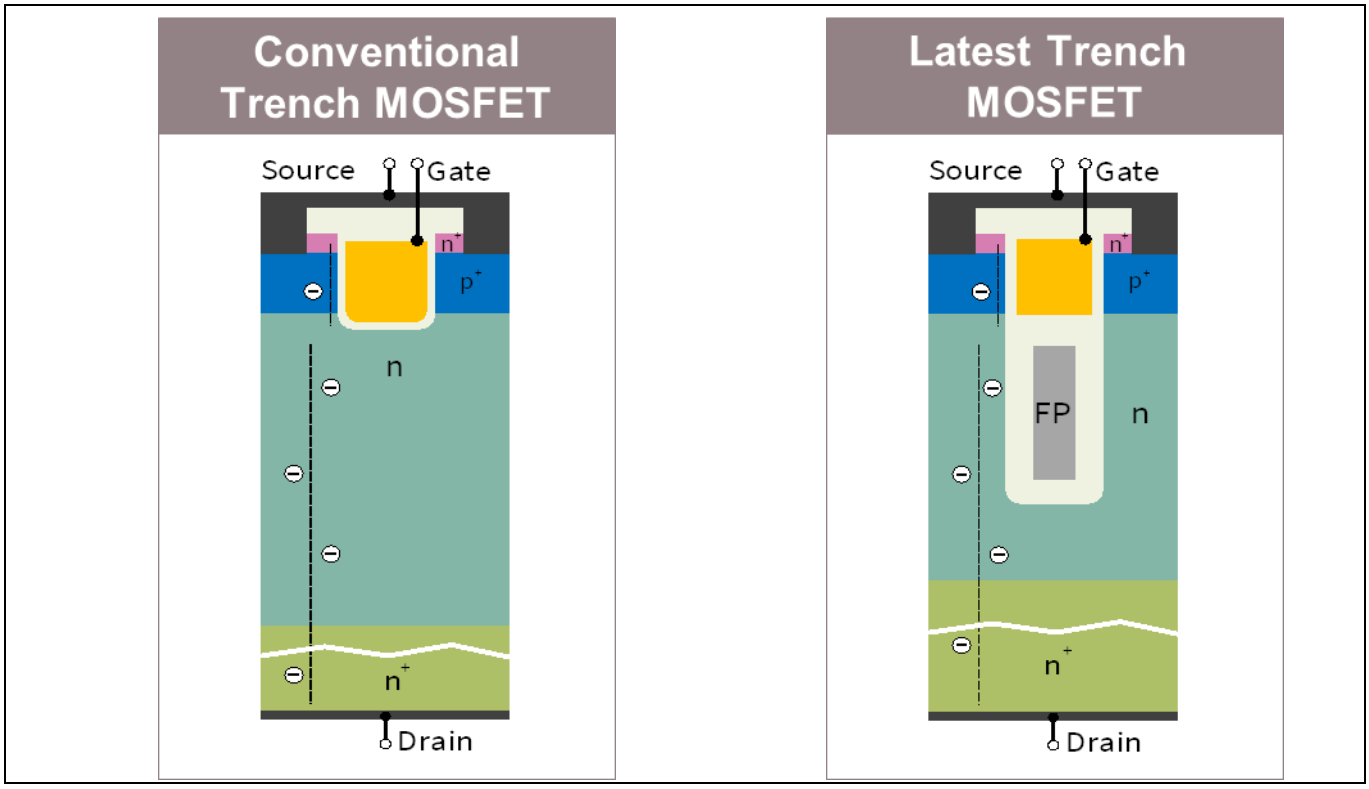


Figure 2 Conventional trench MOSFET vs. OptiMOS™ 6 MOSFET

Some of the key benefits of this new technology are:

1) High efficiency
    a. Lower conduction losses – 36 percent lower $R_{DS(on)typ.}$ compared to OptiMOS™ 3
    b. Lower switching losses – 28 percent lower $Q_{gtyp.}$ compared to OptiMOS™ 3
2) Cost savings from cooling systems, and use of less expensive PCB material
3) High power density in high-power application enabling reduction in the number of paralleled MOSFETs and reduction of bill of materials (BOM)
4) Comparing TOLL vs. D²PAK7 package – TOLL package has 30 percent smaller footprint, and 50 percent reduction in height leading to overall 60 percent reduction in space compared to D²PAK7 package

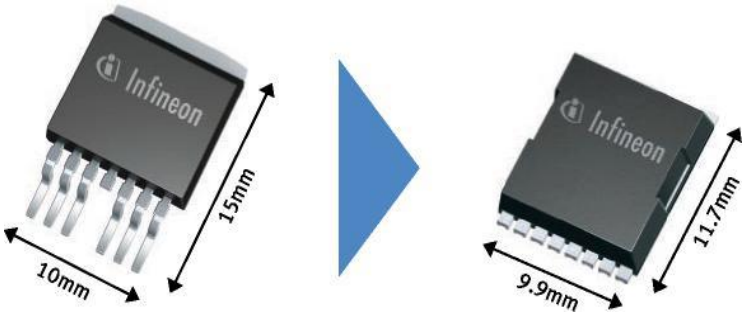


Figure 3 TOLL vs. D²PAK7 package

1.2 Target applications

The new technology is specifically designed for high-power applications. Since TOLL MOSFETs are drain-down MOSFET packages, it is possible to add a heatsink on the bottom of the PCB to be able to address power-demanding applications without increasing system cost and size. Thus, the focus applications for the new 120 V TOLL packages are high-power 60 to 84 V powered systems. The main target applications for this new technology are battery chargers and motor-drive applications up to 2 kW of continuous power. Additionally, these power MOSFETs suit applications above 1 kW such as adapters and solar inverters.

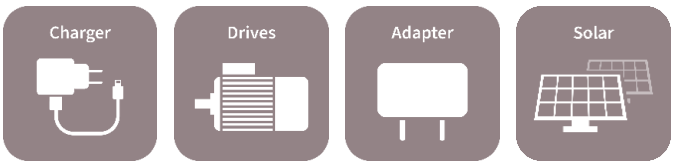


Figure 4 Target applications for the new OptiMOS™ 6 120 V TOLL MOSFETs

1.3 Key features

In the following section some of the key features of the OptiMOS™ 6 120 V power MOSFET technology will be compared with its predecessor OptiMOS™ 3 technology.

1.3.1 On-state resistance ($R_{DS(on)}$)

The new OptiMOS™ 6 120 V power MOSFET technology shows significant reduction in $R_{DS(on)}$ compared to the previous-generation OptiMOS™ 3 120 V MOSFET. This has several advantages for the end applications:

1) 36 percent lower conduction losses due to reduction of $R_{DS(on)typ.}$ when compared to OptiMOS™ 3 120 V MOSFET
2) For high-power application, reduction in the number of paralleled MOSFETs and BOM costs, leading to higher power density
3) Higher efficiency, leading to cost savings from cooling systems, and improved thermals

Figure 5 shows the comparison of $R_{DS(on)typ.}$ of OptiMOS™ 6 and OptiMOS™ 3 120 V power MOSFET technologies at V_{GS} = 10 V based on the datasheet of BiC products. The new OptiMOS™ 6 120 V TOLL MOSFET records a decrease of 36 percent in $R_{DS(on)typ.}$ compared to previous generations.

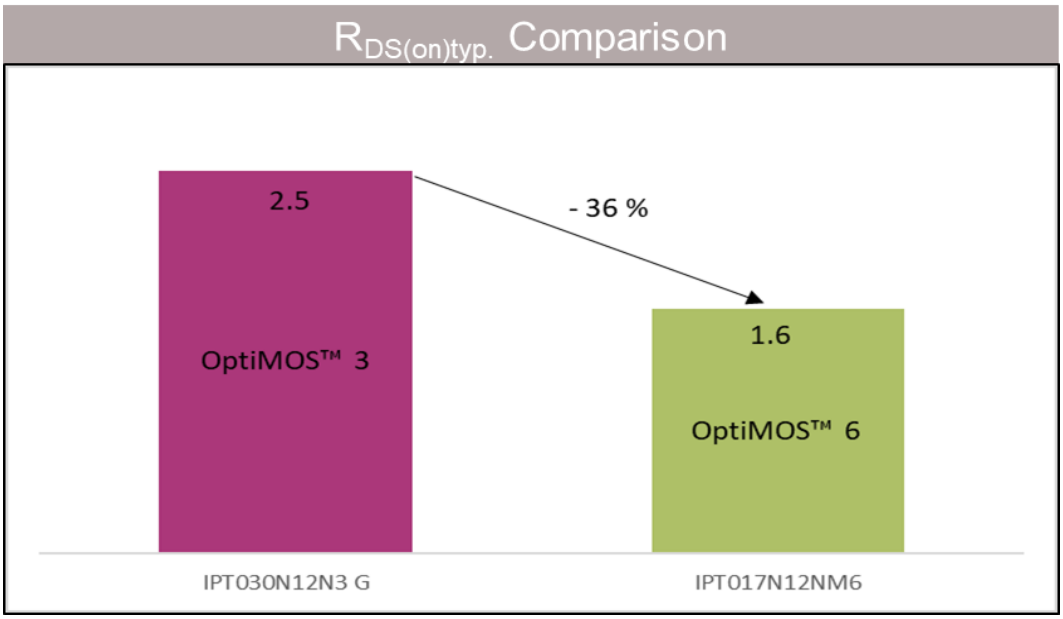


Figure 5 Comparison between $R_{DS(on)typ.}$ for new OptiMOS™ 6 and BiC OptiMOS™ 3 120 V MOSFETs in TOLL package

1.3.2 Gate charge characteristics

Figure 6 shows the comparison of gate charge characteristics for new OptiMOS™ 6 and BiC OptiMOS™ 3 120 V power MOSFETs based on the datasheet. The new OptiMOS™ 6 120 V TOLL MOSFET records a decrease of 28 percent and 32 percent in $Q_{gtyp.}$ and $Q_{gdtyp.}$, respectively, compared to previous generations. This has several advantages for end applications:

1) 28 percent lower switching losses when compared to OptiMOS™ 3 120 V MOSFET
2) Higher efficiency, leading to cost savings from cooling systems, and improved thermals

3) Lower driving current requirements from the gate driver due to lower gate charge characteristics leading to faster turn-on of MOSFETs and lower switching losses

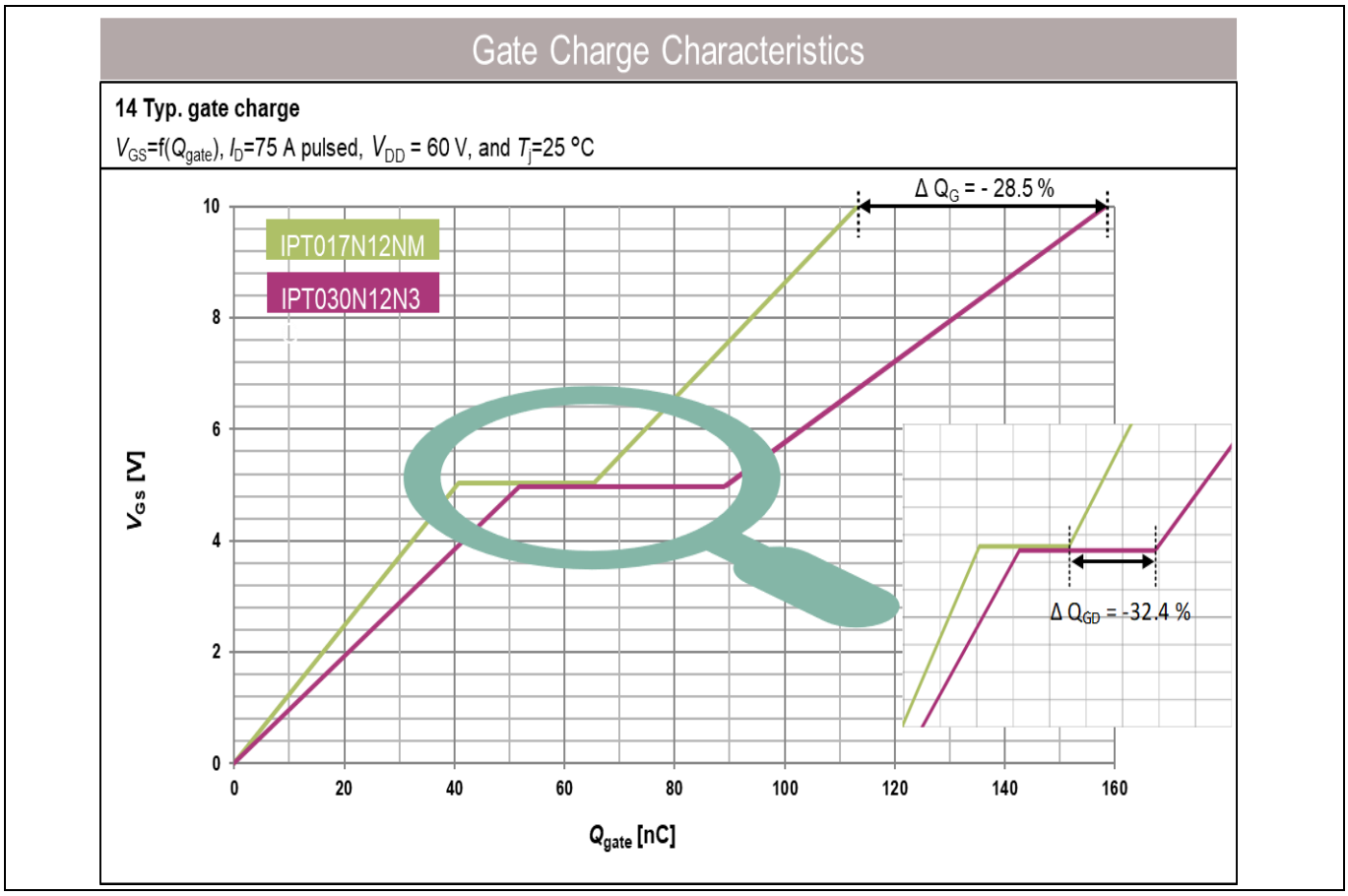


Figure 6 Comparison between gate charge characteristics for new OptiMOS™ 6 and BiC OptiMOS™ 3 120 V MOSFETs in TOLL package

1.3.3 Technology FOM

FOM_g is specific to a particular technology and is defined as the product of gate charge (Q_g) and on-state resistance ($R_{DS(on)}$), mΩ x nC. For a particular technology, it is not possible to reduce the $R_{DS(on)}$ without increasing Q_g, since FOM_g is a constant for a given technology. Thus, in order to improve both the $R_{DS(on)}$ and Q_g it is necessary to move to a new technology, leading to the improvement of FOM_g – shown in **Figure 7**.

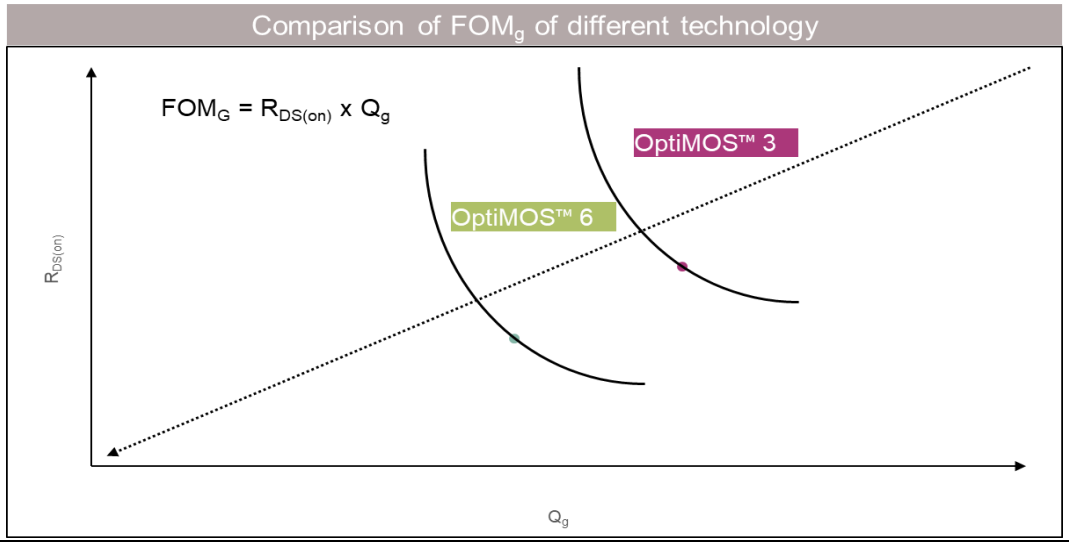


Figure 7 Tradeoff between $R_{DS(on)}$ and Q_g for a given technology

Figure 8 and **Figure 9** show the comparison of FOM_g and FOM_{gd} of OptiMOS™ 6 and OptiMOS™ 3 120 V power MOSFETs, respectively, based on the datasheet. The new OptiMOS™ 6 120 V TOLL MOSFET records a decrease of 54 percent and 56 percent in FOM_g and FOM_{gd}, respectively, compared to previous generations. This leads to higher efficiency, higher power density, and higher system reliability.

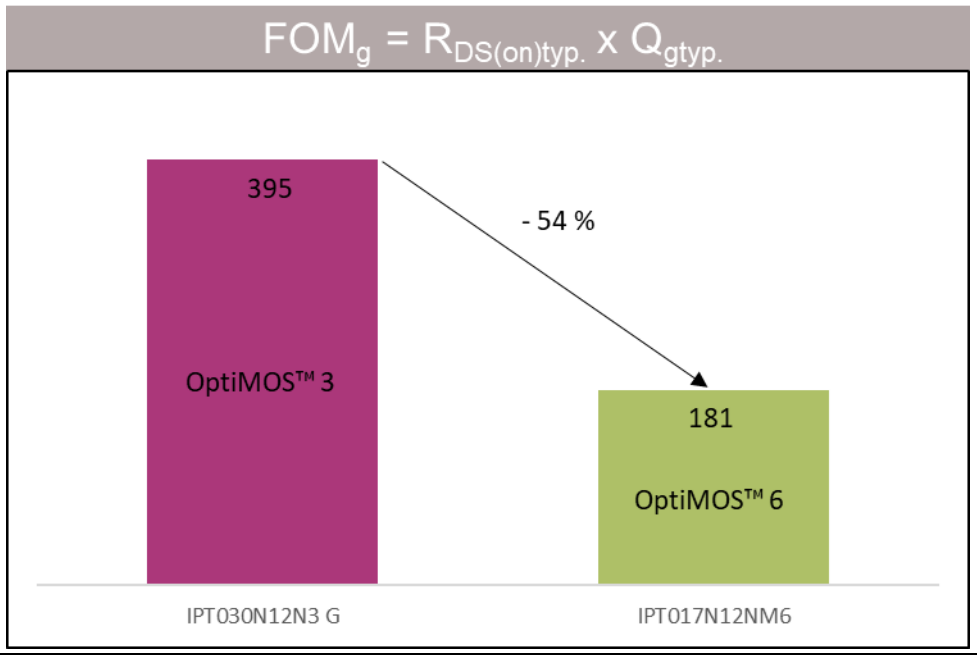


Figure 8 Comparison of FOM_g between new OptiMOS™ 6 and BiC OptiMOS™ 3 120 V MOSFETs in TOLL package

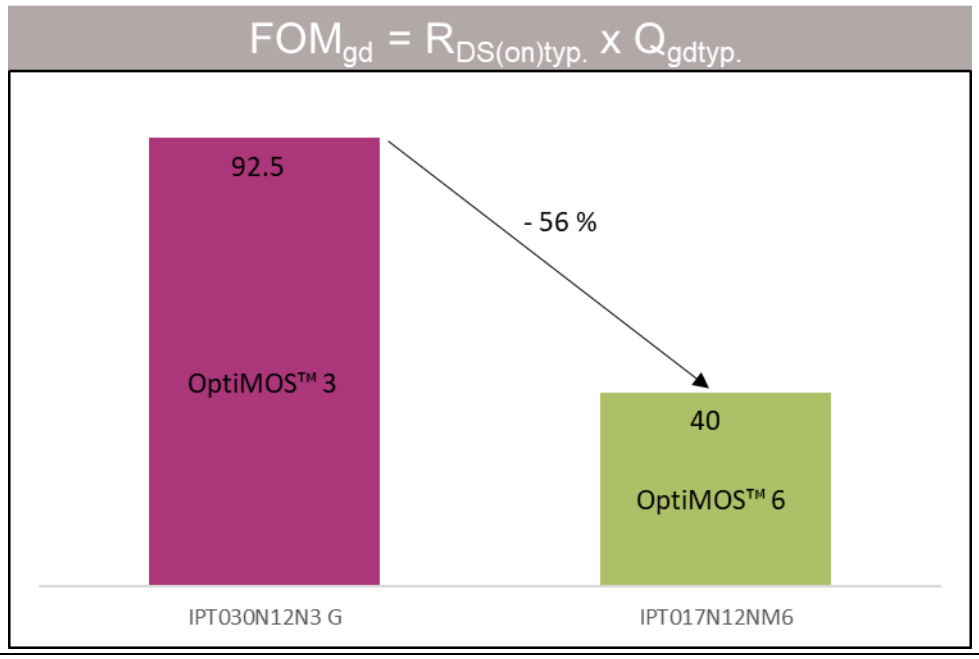


Figure 9 Comparison of FOM_{gd} between new OptiMOS™ 6 and BiC OptiMOS™ 3 120 V MOSFETs in TOLL package

1.3.4 Technology FOM_{OSS}

The output capacitance (C_{OSS}) of a MOSFET is charged every switching cycle, leading to energy being stored in the output capacitor. In hard-switching applications this extra energy stored in the output capacitor leads to switching losses, especially in high-frequency applications since this energy cannot be recovered, leading to lower efficiency and temperature rise of the MOSFET.

FOM_{OSS}, which is defined as Q_{OSS} x $R_{DS(on)}$, improves by 6 percent when comparing new OptiMOS™ 6 with the BiC OptiMOS™3 120 V power MOSFET, as shown in **Figure 10**. This is very significant, as this new technology shows improvements in all three FOMs: FOM_G, FOM_{GD}, and FOM_{OSS}, which provide higher efficiency and improved thermal performance in high-frequency and high-voltage switching applications. Moreover, the linearity of the output capacitance at higher voltages for new OptiMOS™ 6, as shown in **Figure 11**, helps in the reduction of V_{DS} overshoot during MOSFET turn-off.

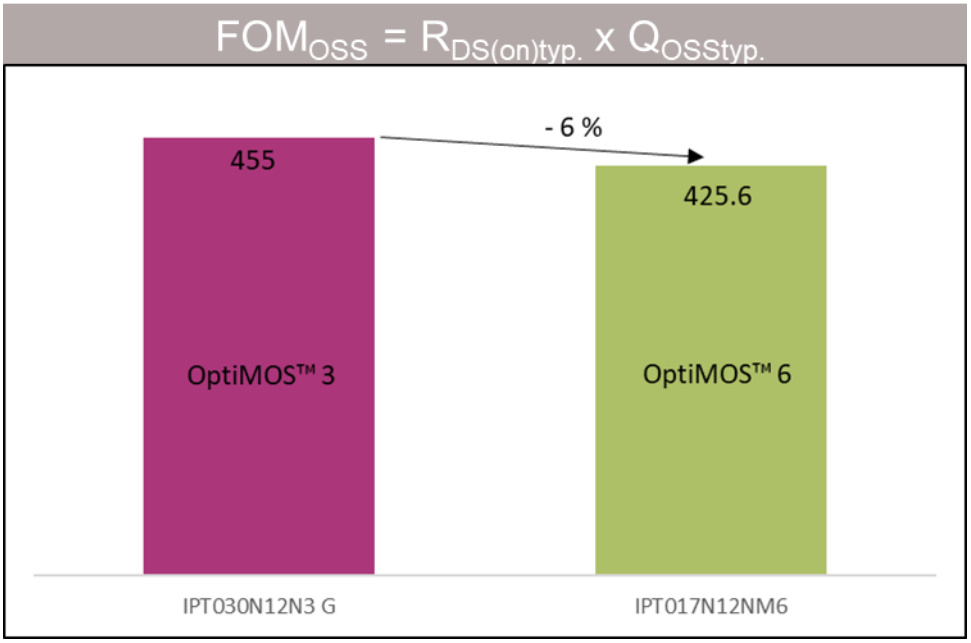


Figure 10 **Comparison of FOM_{OSS} between new OptiMOS™ 6 and BiC OptiMOS™ 3 120 V MOSFETs in TOLL package**

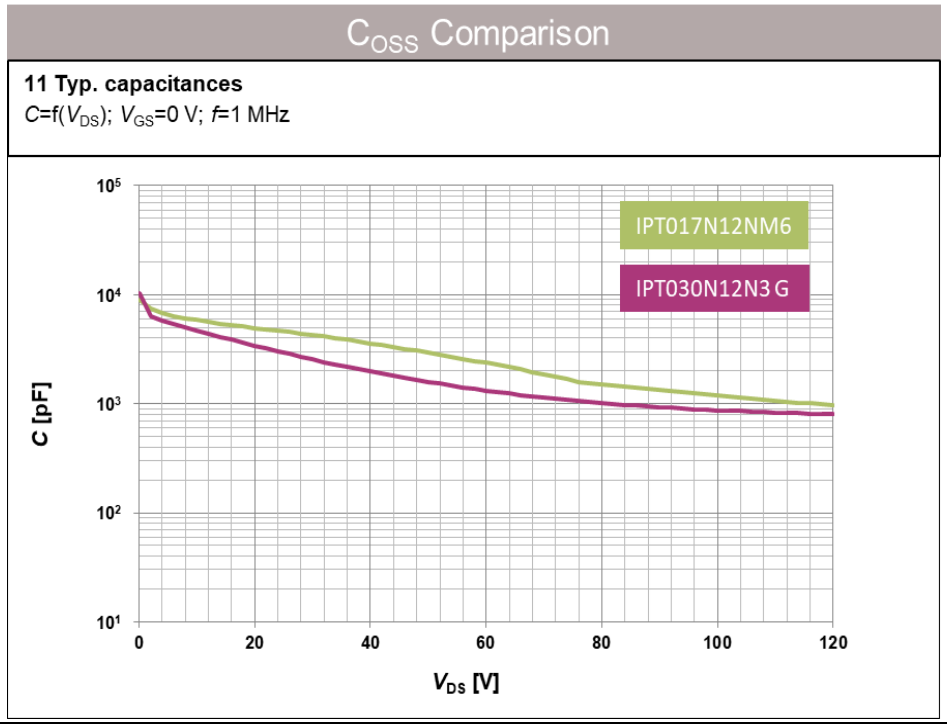


Figure 11 **Comparison of output capacitance (C_{OSS}) between new OptiMOS™ 6 and BiC OptiMOS™ 3 120 V MOSFETs in TOLL package**

1.3.5 Transfer characteristics and safe operating area

The transfer characteristics of MOSFETs show the drain current (I_D) as a function of gate-source voltage (V_{GS}) curve at a fixed junction temperature, as shown in **Figure 12** for new OptiMOS™ 6 and BiC OptiMOS™ 3 120 V MOSFETs in TOLL package. The zero-temperature coefficient (ZTC) is a point where the 175°C and 25°C curves

intersect, as shown in **Figure 12** – it corresponds to the device temperature remaining constant at a certain V_{GS}. Below the ZTC point, transconductance of the device is higher, leading to any increase in device cell temperature resulting in more I_D, in turn leading the device cell to pull in more current from its surrounding cells and further increase in device temperature (positive feedback) **[3]**. Due to these conditions, thermal runaway might occur at low I_D, which depends on the device die size and the negative temperature coefficient (NTC) of the threshold voltage (V_{TH}) of the MOSFET **[3]**. Moreover, above the ZTC point, the transconductance is lower, leading to any device cells that are running hotter channeling less current from surrounding cells, resulting in uniform temperature in the device due to negative thermal feedback.

Figure 13 shows the zoomed-in transfer characteristics for new OptiMOS™ 6 and BiC OptiMOS™ 3 120 V MOSFETs in the TOLL package. This figure clearly shows lower transconductance in OptiMOS™ 6 over the junction temperature of 25°C and 175°C when compared to OptiMOS™ 3 at a point below ZTC. This leads to improved robustness against thermal runaway at lower V_{GS}. However, the ZTC point for OptiMOS™ 6 is placed at a higher drain current than for the OptiMOS™ 3, which can lead to thermal instability for MOSFETs operating in the linear region of operation as in a battery-management system.

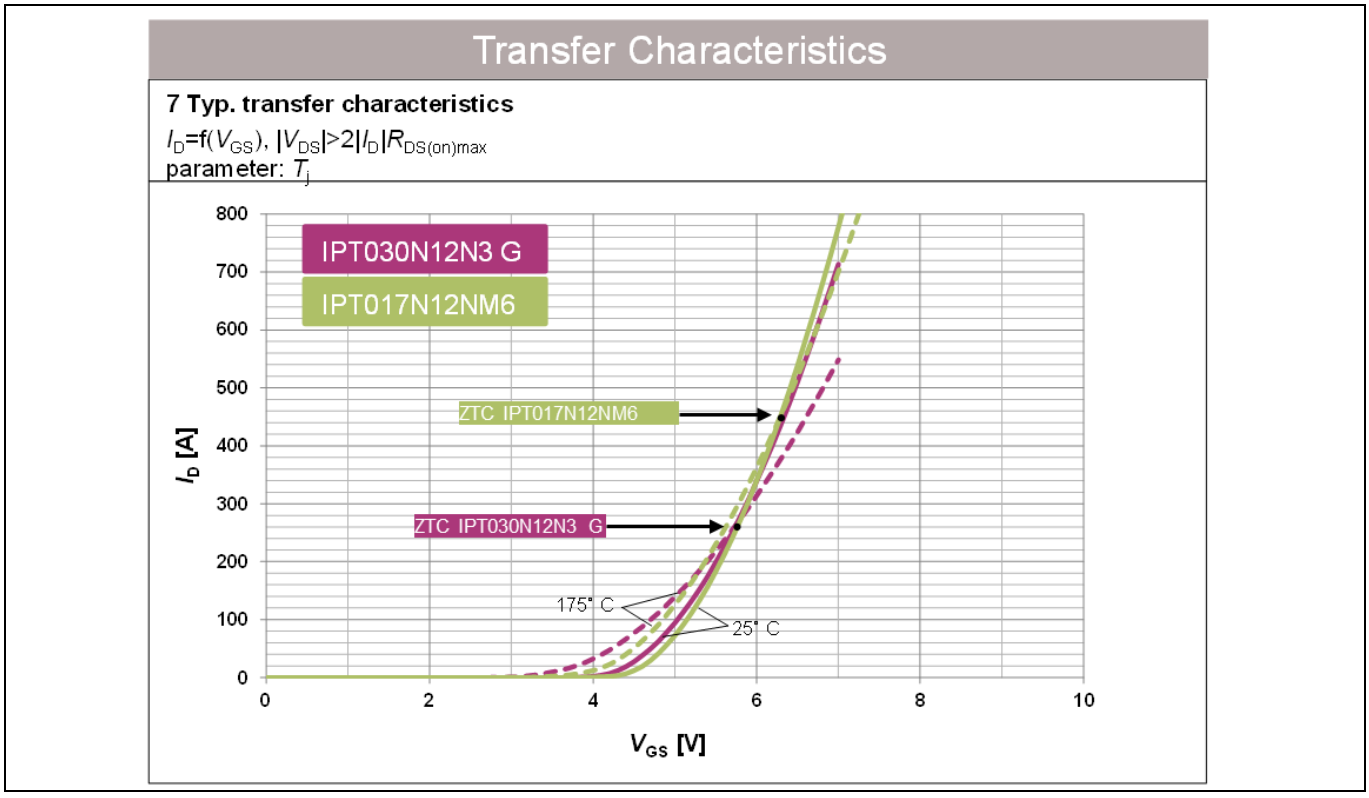


Figure 12 Comparison of transfer characteristics between new OptiMOS™ 6 and BiC OptiMOS™ 3 120 V MOSFETs in TOLL package

Additionally, when comparing the safe operating area (SOA) for new OptiMOS™ 6 and BiC OptiMOS™ 3 120 V MOSFETs in a TOLL package, the new technology shows improvement in all regions except thermal instability, which is also highlighted by lower ZTC in the transfer characteristic curve for OptiMOS™ 3. Thus, OptiMOS™ 6 120 V power MOSFETs are not ideal for battery-management systems due to possible thermal runaway in the linear region of operation.

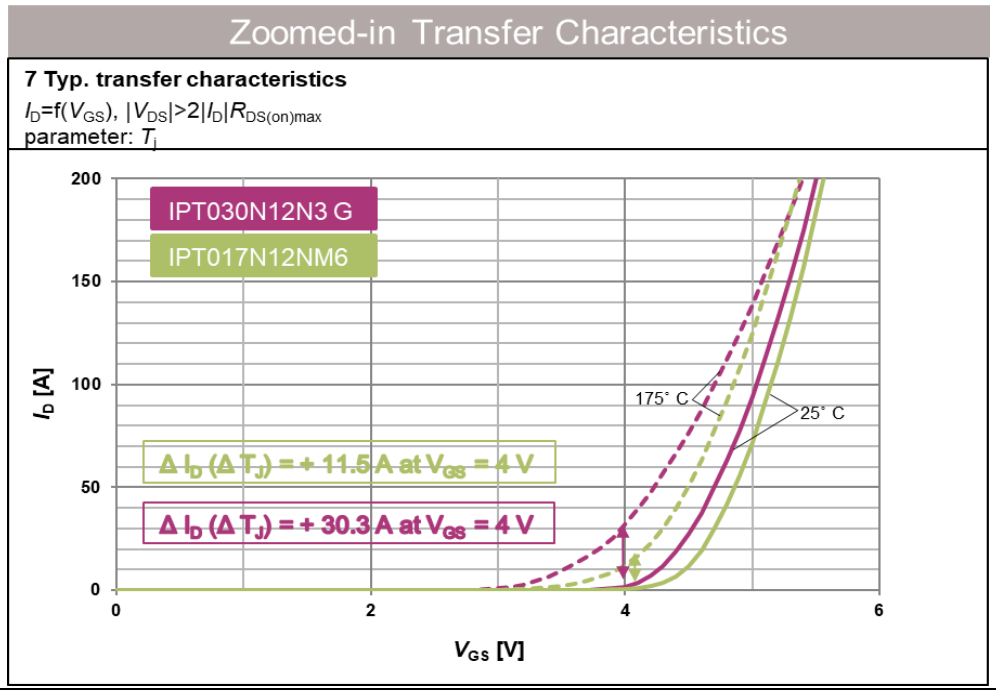


Figure 13 Zoomed-in transfer characteristics

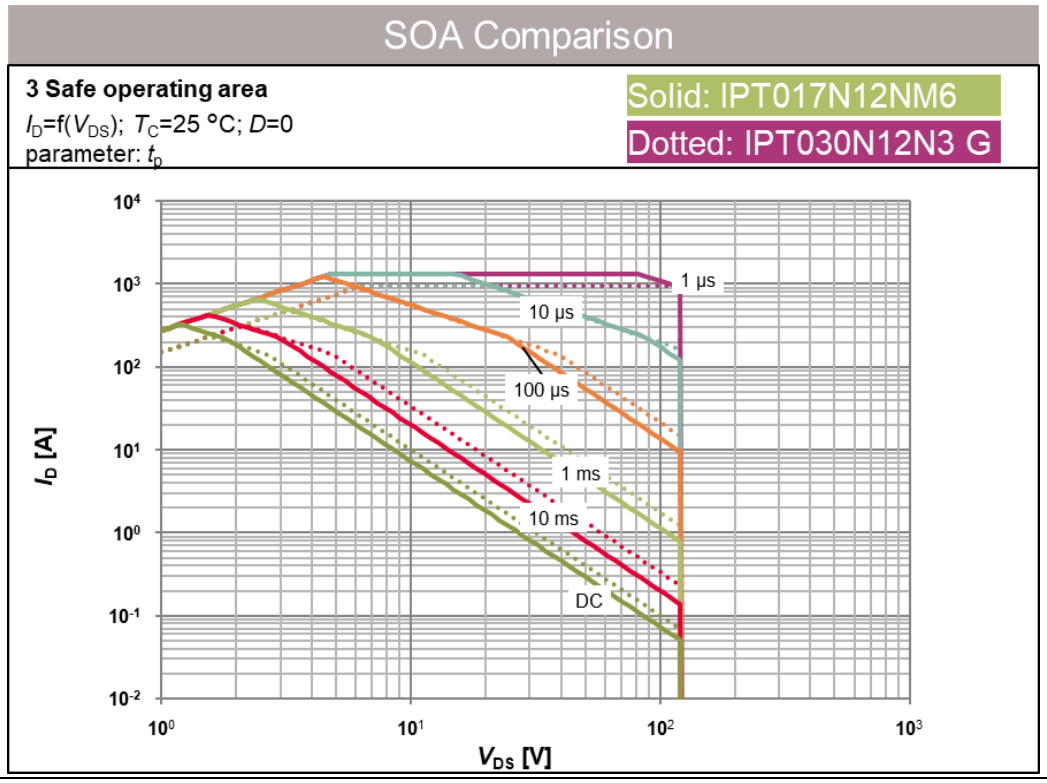


Figure 14 Comparison of SOA curve between new OptiMOS™ 6 and BiC OptiMOS™ 3 120 V MOSFETs in TOLL package

1.3.6 Datasheet comparison for BiC devices

In **Table 2**, a datasheet comparison is given for BiC devices with OptiMOS™ 6 (IPT017N12NM6) and OptiMOS™ 3 (IPT030N12N3) 120 V power MOSFET technology. The table focuses on parameters that are most important for SMPS and motor-drive applications.

Table 2 Datasheet comparison between BiC OptiMOS™ 6 and OptiMOS™ 3 120 V power MOSFET technology

Parameter	Symbol	Conditions	IPT017N12NM6	IPT030N12N3 G	Unit
Technology			OptiMOS™ 6 120 V	OptiMOS™ 3 120 V	
Maximum on-state resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 150 A* / 100 A**	1.7*	3.0**	mΩ
Maximum operating temperature	T_j	-	175	175	°C
Maximum current rating	I_D	-	333	237	A
Maximum thermal resistance, junction – case	R_{thJC}	-	0.38	0.4	°C/W
Gate threshold voltage	$V_{GS(th)}$ (min.)	V_{DS} = V_{GS}, I_D = 275 µA* / 270 µA**	2.6*	2.0**	V
	$V_{GS(th)}$ (typ.)		3.1*	3.0**	V
	$V_{GS(th)}$ (max.)		3.6*	4.0**	V
Typical gate charges	Q_g	V_{DD} = 60 V, I_D = 75 A* / 100 A**, V_{GS} = 0 to 10 V	113*	158**	nC
	Q_{gd}		25*	37**	nC
	Q_{gs}		41*	52**	nC
Typical input capacitance	C_{ISS}	V_{GS} = 0 V, V_{DS} = 60 V, f = 1 MHz	8100	10000	pF
Typical output capacitance	C_{OSS}	V_{GS} = 0 V, V_{DS} = 60 V, f = 1 MHz	2400	1300	pF
Typical reverse transfer capacitance	C_{RSS}	V_{GS} = 0 V, V_{DS} = 60 V, f = 1 MHz	40	61	pF
Typical reverse recovery time	T_{rr}	V_R = 60 V, di_F / dt = 1000 A/µs* / 100 A/µs**	35*	85**	ns

2 Evaluation board

The EVAL_TOLL_72VDC_2kW evaluation power board uses new OptiMOS™ 6 120 V power MOSFET technology devices for battery-powered 60 - 84 V BLDC motor-drive applications suitable for high-power power tools. This evaluation board is designed to be driven by the Infineon XMC1300 drive card KIT_XMC1300_DC_V1 (or higher) loaded with the correct firmware. Both power board and drive card are needed for this application. A 32-pin male–female connector (MAB32B2-FAB32Q2) is needed to connect the power board and drive card, as shown in **Figure 15**.

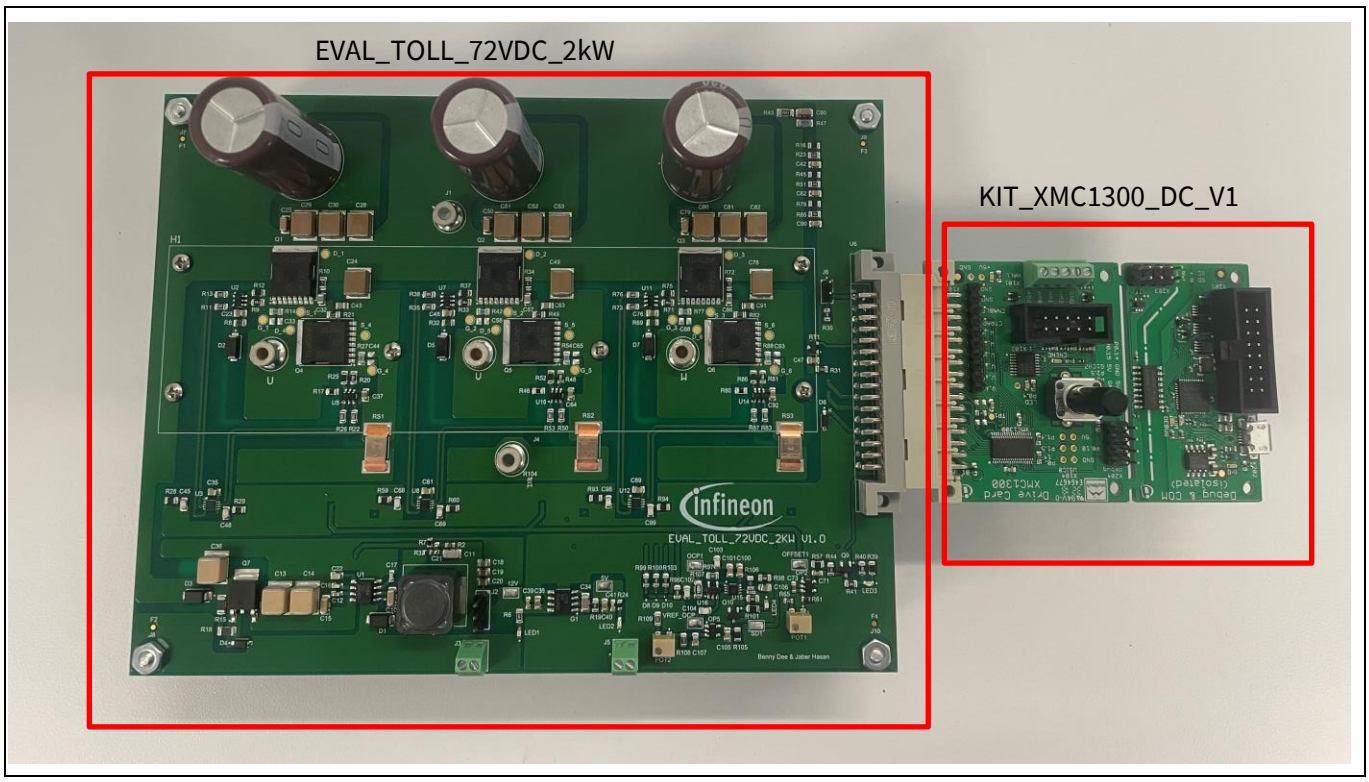


Figure 15 Evaluation power board EVAL_TOLL_72VDC_2kW and control card KIT_XMC1300_DC_V1 motor-drive system

The EVAL_TOLL_72VDC_2kW evaluation power board generates onboard 12 V and 5 V DC rails to power the gate driver ICs and the microcontroller in the XMC1300 drive card. The power board also provides protection against overcurrent (OC) and overtemperature (OT). The OC threshold level can be changed by adjusting the potentiometer (POT2). Meanwhile, the OT threshold can be changed only by firmware. Because this evaluation board is designed to be able to work with both six-step block commutation control and field-oriented control (FOC) for three-phase BLDC motors there are three low-side shunt resistors to measure the current in the three phases of the inverter. The Hall sensors for the BLDC motors need to be connected to connector X101 on the XMC1300 drive card, as shown in **Figure 15**.

2.1 Board parameters and technical data

Table 3 includes the evaluation board parameters.

Table 3 Board parameters

Parameter	Symbol	Conditions	Value	Unit
Input DC voltage	V_{IN}	DC voltage input	60~84	V
12 V output voltage	+12 V	Maximum 200 mA output current	12 ±5 percent	V
5 V output voltage	+5 V	Maximum 200 mA output current	5 ±5 percent	V
Max. switching frequency	f_{SW}	V_{CC} = 12 V	10	kHz
Max. output phase current	I_{phase_peak}	T_A = 20°C, T_C = 100°C, air cooling, f_{SW} = 10 kHz	80	A_{peak}
Maximum output power	P_{OUT}	Sufficient cooling applied to maintain heatsink temperature below 120°C	2000[2]	W
PCB characteristics				
Material		1.6 mm thickness, 2 oz. copper each layer, six layers	FR4	
Dimensions		Length x width x height	172 x 129.77 x 1.6	mm
System environment				
Max. ambient temperature	T_{amb}	Non-condensing, maximum RH 95 percent	40	°C

2.2 Main features

The main features of the EVAL_TOLL_72VDC_2kW evaluation power board using OptiMOS™ 6 120 V power MOSFET technology for battery-powered motor-drive applications are:

- Single MOSFET at each leg of the inverter
- Standard 32-pin male–female connector to interface power board and XMC1300 drive card
- 72 V nominal input voltage
- 60 to 84 V input voltage range
- 80 A_{peak} maximum phase current for each phase
- Latched shutdown overcurrent protection (OCP) by sensing the current through the shunt resistor of each phase
- Programmable overtemperature protection (OTP)
- 12 V and 5 V onboard power supplies for gate driver ICs and microcontroller, respectively
- Hardware supports both block commutation control and FOC control using Hall senors or back EMF

[2] It is recommended to use short cables for the input power supply to limit the ripple current passing through the input bulk capacitors.

2.3 Block diagram

A block diagram of the three-phase inverter board is shown in **Figure 16**. In this design, a buck (step-down) converter is used to convert the input voltage to 12 V for gate driver ICs. Alternatively, for ease of debugging, by changing the position of jumper J3, an external 12 V supply can be used. The 12 V rail is converted to 5 V by a linear dropout (LDO) regulator to provide power to the analog circuits on the power board and to power the XMC™ drive card via the 32-pin connector. Moreover, by removing the resistor R1, an external 5 V supply can be used.

OCP is achieved by measuring the voltage drop across each shunt of each phase. The output of the current amplifier is also fed to the XMC™ drive card after passing through a low-pass RC filter for FOC. OTP is achieved by using an onboard temperature sensor. The output voltage of the temperature sensor is also passed to the XMC™ drive card after filtering using an RC filter for OTP. Back EMF signals are provided to the XMC™ drive card after reducing the voltage below 5 V through the resistive divider for sensorless control. The Hall sensor signals are directly connected to the XMC™ 1300 drive card.

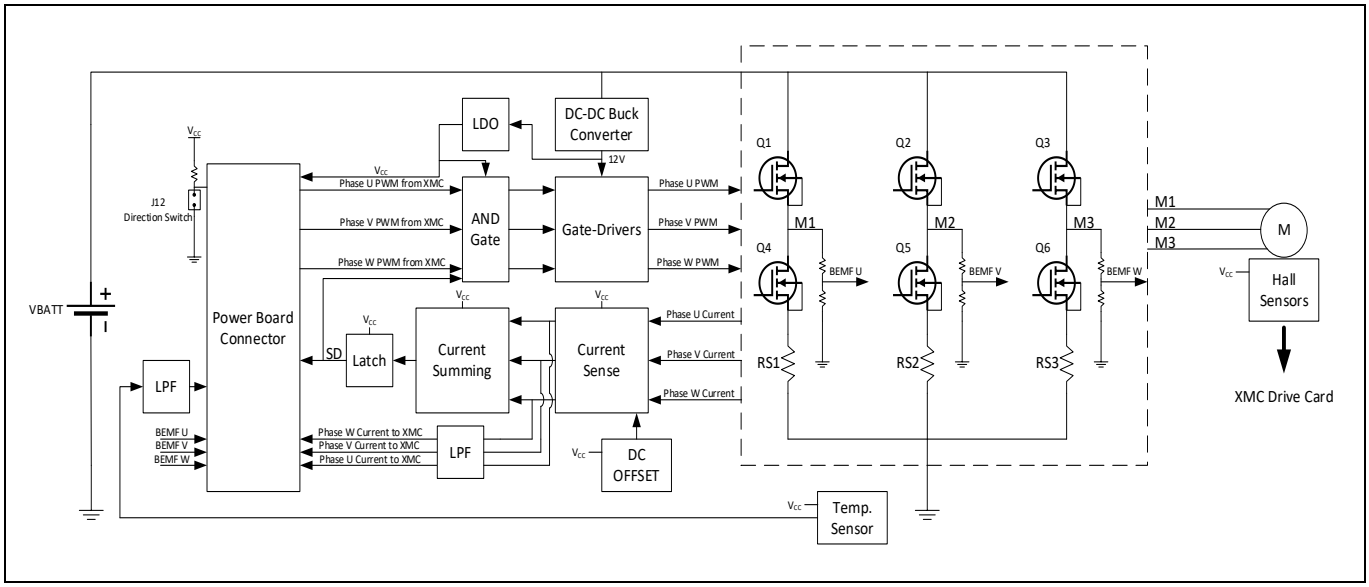


Figure 16 EVAL_TOLL_72VDC_2kW block diagram

2.4 Hardware description

Different sections of the evaluation board are shown in **Figure 17** and **Figure 18**. An aluminum heatsink is attached to the bottom of the TOLL MOSFET to push more power to the load, because the maximum temperature rating of the FR4 PCB is 130°C. An insulator made of thermal insulating material (TIM) is placed between the heatsink and the PCB. The heatsink is connected to ground to reduce EMI.

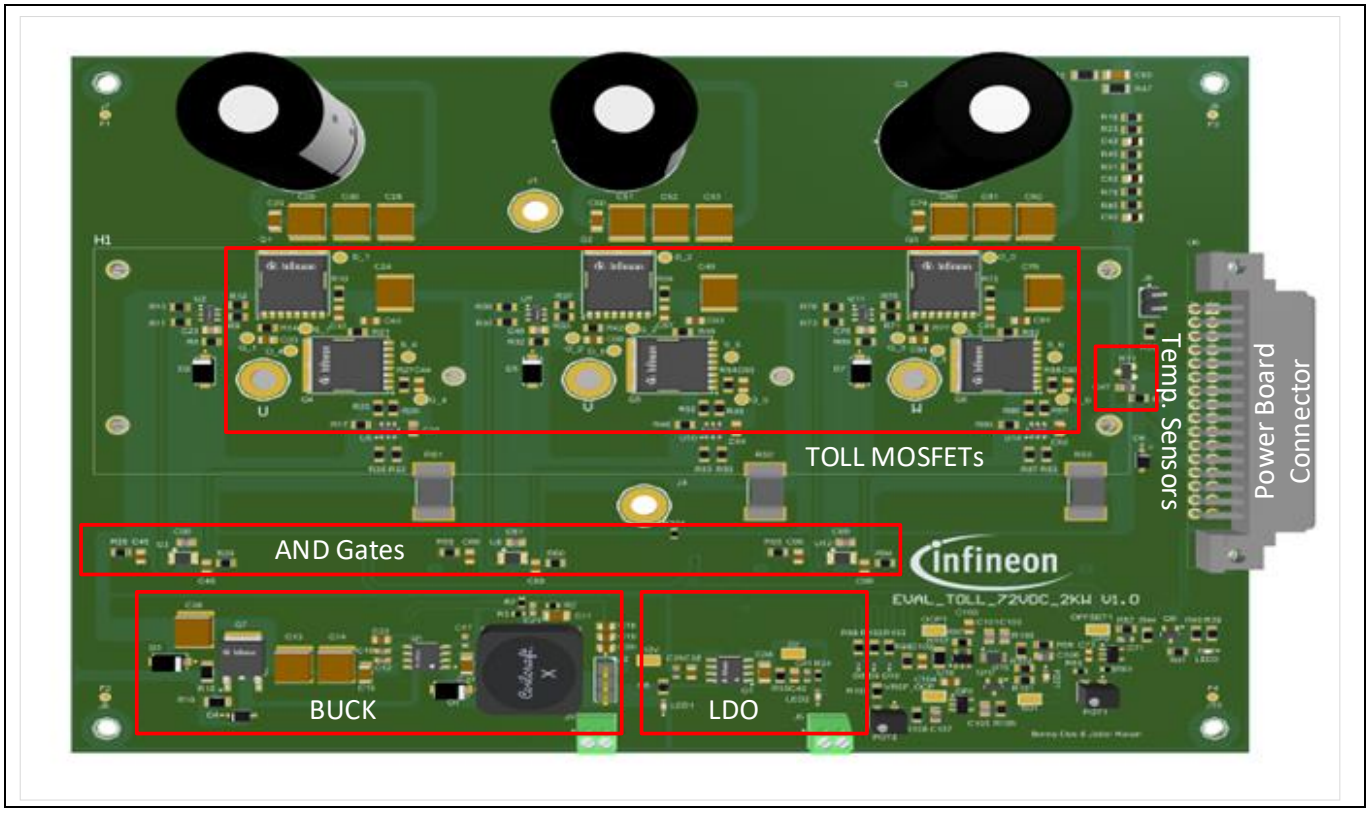


Figure 17 Different sections of the demo board – top side

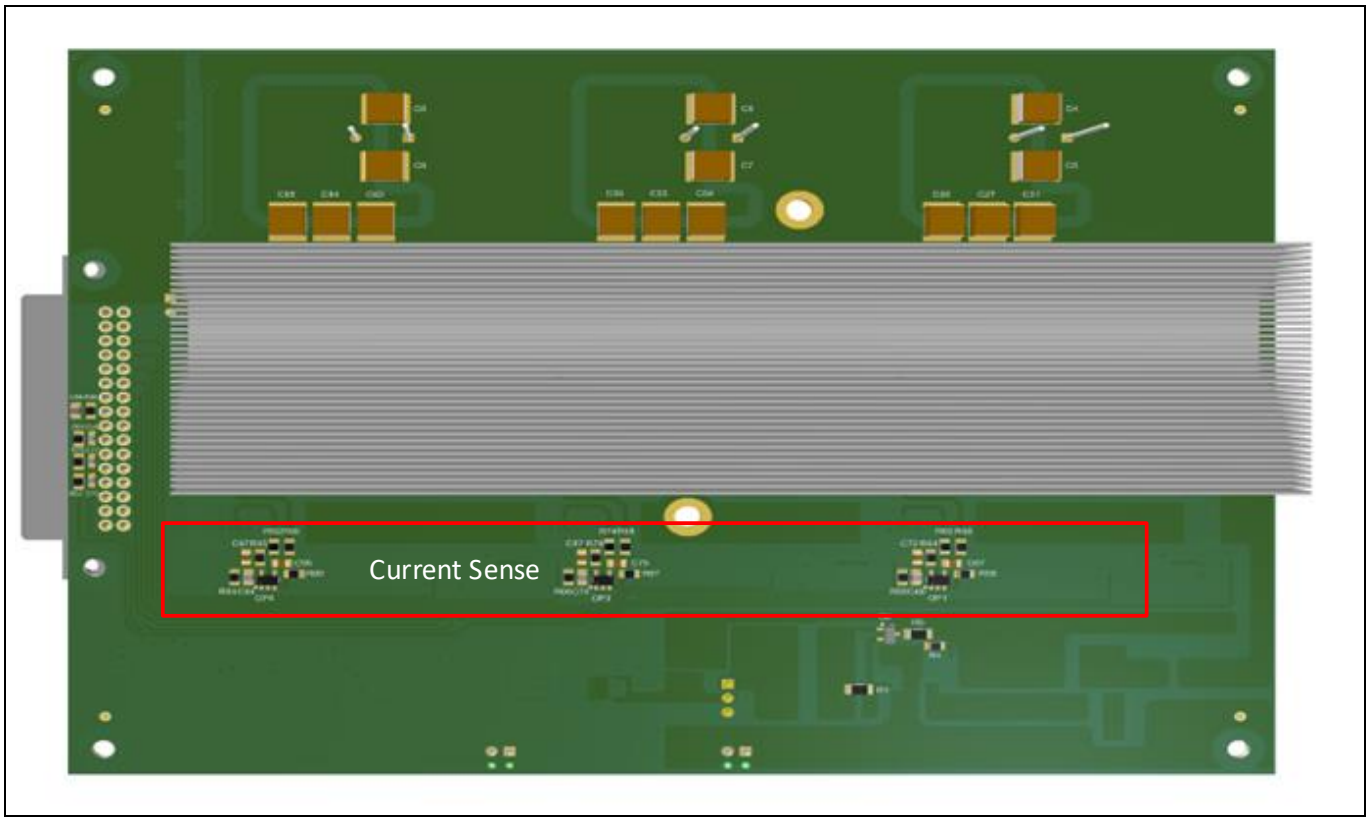


Figure 18 Different sections of the demo board – bottom side

2.4.1 Power supplies

Infineon's ILD8150 buck LED driver IC has been used in this design to reduce the battery voltage (voltage range of 60 V-84 V) to a regulated value of 12 V to supply the gate driver ICs. The maximum rated input voltage and the maximum rated voltage at the bootstrap pin of this LED driver IC are 90 V, respectively, per the datasheet of the device. Therefore, in order for this device to operate all the way up to a battery voltage of 84 V (3 V x 28 V), a simple voltage regulator is formed by the Zener diodes and transistor, as shown by R15, R18, D4, and Q7. Since D4 is rated at 68 V, gate-source voltage required to maintain 0.2 A at the output of the LED driver IC is 2 V. Therefore, the maximum input voltage (source voltage of the MOSFET Q7) seen by this LED driver IC is 66 V, which is below its maximum voltage rating. The maximum power loss across the MOSFET Q7 is 3.6 W at maximum battery voltage of 84 V. For powering the microcontroller in the XMC™ drive card and other analog circuits in the power evaluation board, the 12 V is further reduced to 5 V by the LDO. The onboard power supply architecture is shown in **Figure 19**.

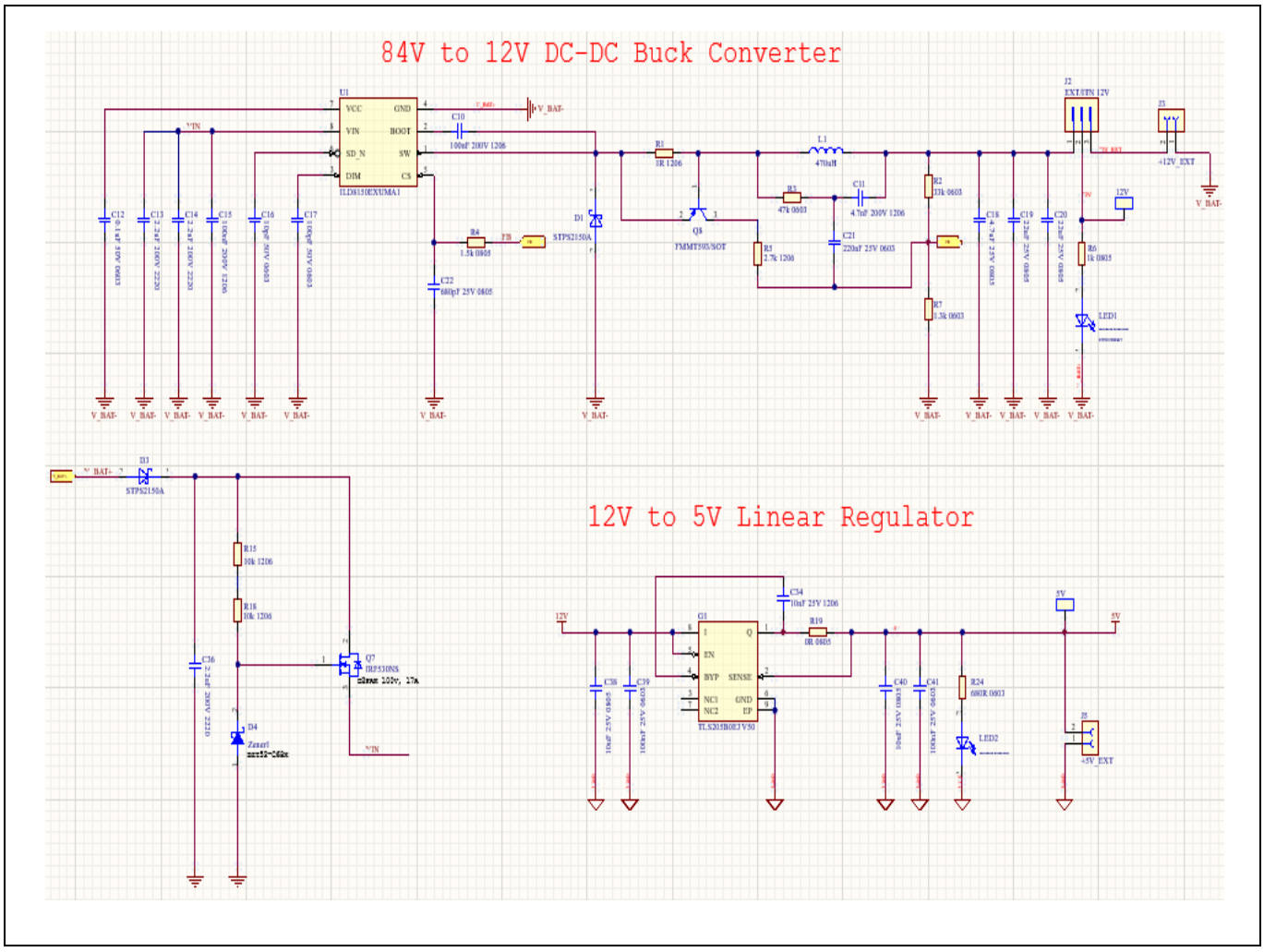


Figure 19 Buck and LDO regulators used in the demo board

The ILD8150, originally designed for constant current control in LED drivers, uses a hysteretic controller, which has been modified to provide constant voltage regulation at the output. The hysteretic control in the ILD8150 provides extremely fast regulation and stable output voltage combined with good EMI performance. The ILD8150 is rated to supply output current of up to 1.5 A. The hysteretic controller stability depends on the ramp of the feedback voltage. The ramp of the feedback voltage should be large enough to reduce jitter. The ILD8150 implements two voltage thresholds, V_{CSH} and V_{CSL}, so that when the feedback voltage crosses above the V_{CSH}

threshold, the internal MOSFET turns off and when the feedback voltage crosses below the V_{CSL} threshold, the internal MOSFET turns on. The feedback ramp is largely dependent on the equivalent-series resistance (ESR) current of the inductor or from the external RC (R3, C11) components used to generate the ripple when a small ESR ceramic output capacitor is used. R4 and C22 act as a low-pass filter (LPF) to extract high-frequency noise. Additionally, to protect the LED driver IC from short-circuit, a simple circuit using a PNP Bipolar-Juntion-Transistor (BJT) (Q9) has been implemented, which limits the load current to 0.7 A. Therefore, as the load current is increased, it will create 0.7 V across R1, turning on the PNP transistor (Q8) and pulling the feedback pin high and dropping the output voltage low. As mentioned, an external power supply may also be used to provide 12 V to the gate driver ICs by changing the position of the jumper J2.

The TLS205B LDO (G1) provides a fixed 5 V power to the microcontroller in the XMC™ drive card and other analog circuits in the power board. An external bypass capacitor (C34) provides low output voltage ripple. This device is capable of supplying a maximum output current of 500 mA. By removing jumper R1, an external power supply can be used to provide 5 V to the microcontroller and the analog circuitry.

2.4.2 Gate drivers

Infineon's EiceDRIVER™ 1EDN8550B, a single-channel high-side and low-side gate driver IC, has been implemented in this design to drive the three-phase inverter MOSFETs. The 1EDN8550B has truly differential input (TDI) circuitry, which provides excellent common-mode robustness (common-mode input voltage range ±200 V, and configurable with common-mode resistors) and eliminates the risk of false triggering **[4]**. Additionally, due to its differential behavior IEDN8550B can handle floating voltage up to the battery voltage using external input common-mode resistors. The gate driver circuit for phase U is shown in **Figure 20**.

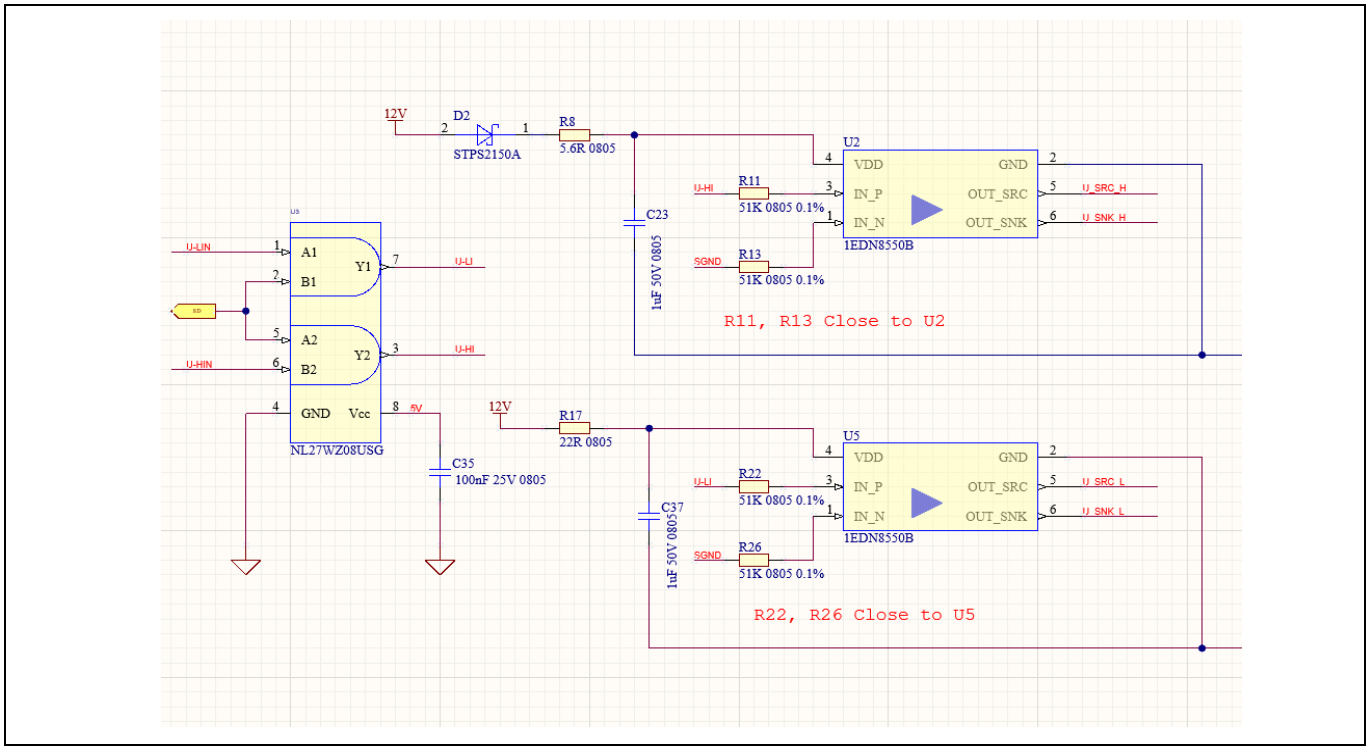


Figure 20 Gate driver circuit for phase U

For normal operation of the circuit, shutdown (SD) is high, which allows PWM signals (U-H and U-L) to pass through the dual-input AND gates, generating PWM drive signals for the high-side and low-side MOSFETs (U-HO and U-LO). When there is OC in any of the phases, SD is pulled low by the latch circuit and thus turns off the switching of the MOSFETs. Additionally, the firmware also has control of the SD signal via the driver enable

signal ($\overline{DR_EN}$). During normal operation of the circuit, the $\overline{DR_EN}$ is pulled low and thus MOSFET Q9 is off. In this scenario, the green LED (LED3) is turned on and SD is pulled high. However, during an OC situation, the microcontroller pulls $\overline{DR_EN}$ high and the MOSFET Q9 is turned on and the SD is pulled low to provide firmware OCP, which is set to 80 A_{peak}, as shown in **Figure 21**.

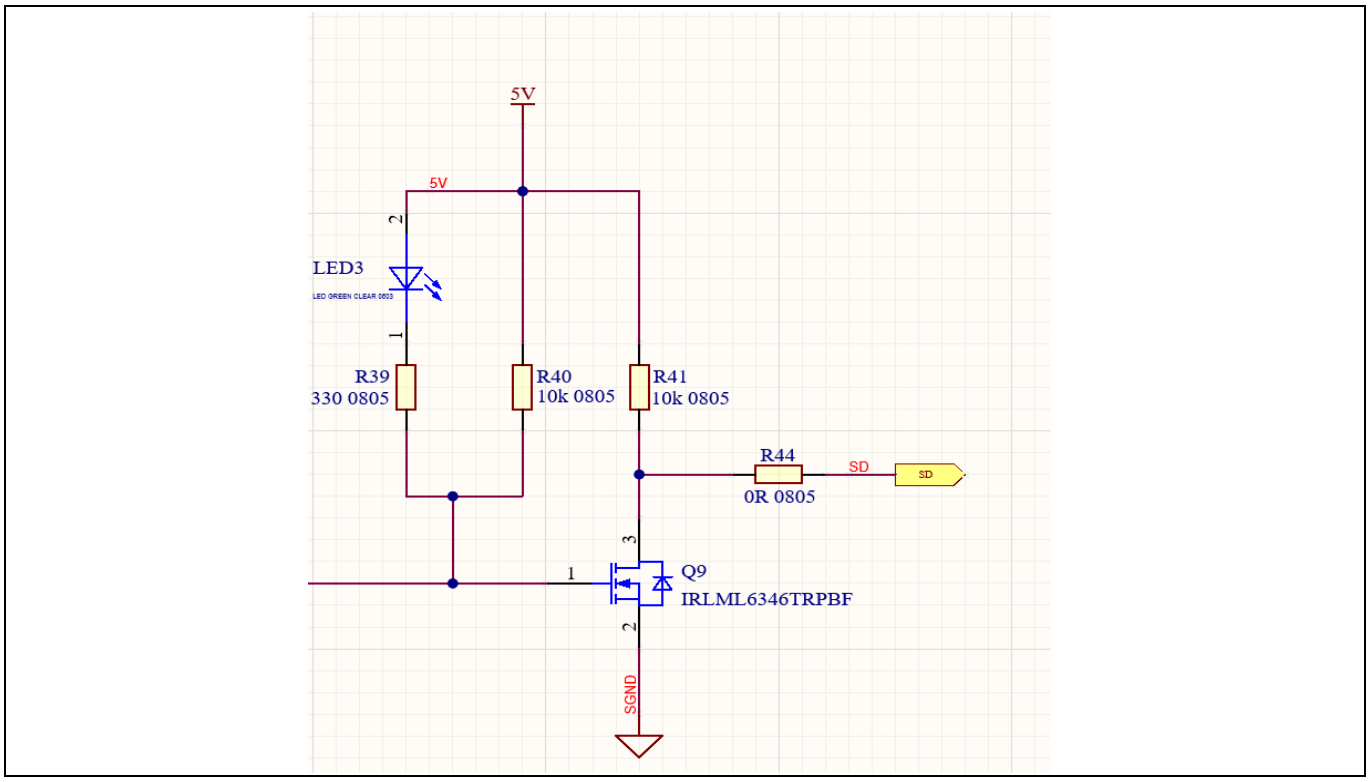


Figure 21 Firmware OCP circuit

2.4.3 Protection circuitry

To protect the MOSFETs of the three-phase inverter from OC, OCP circuitry is implemented in this design, as shown in **Figure 22** and **Figure 23**. Each leg of the three-phase inverter has a 1 mΩ shunt resistor with respect to power ground, as shown in **Figure 17**. The voltage drop across the shunt resistor for phase U is measured using differential amplifier OP1, with a gain of 12.0 for phase U. To protect against leading-edge blanking (LEB), an integrator is implemented using R64 and C72. Because the voltage drop across the shunt resistor needs to be sensed by the microcontroller in the XMC™ drive card, there is a need to create an offset, as the voltage drop across the shunt resistor will be both positive and negative. Thus, OP2 is a buffer which applies a DC offset of 2.5 V to the differential amplifier OP1. The output of OP1 passes through a LPF and connects through the board connector to the microcontroller in the XMC™ drive card to be processed by the control algorithm and protection implemented in the firmware. Similar functions are performed by differential amplifiers OP2 and OP3 for phases V and W. The outputs of all the differential amplifiers of all the phases are summed using diodes D8, D9 and D10 to detect the peak voltage. This peak voltage is compared against a reference voltage of 4.8 V by comparator U16. During normal operation, the output of this comparator will be low and thus the output of the D-flip-flop U15 remains low. However, during a short-circuit condition the output of the comparator goes high, as the detected peak voltage exceeds 4.8 V and thus the output of the U15 will transition high, turning on the MOSFET Q10 to pull SD low and turn off the inverter. With this setup the OC trip level is set at 192 A_{peak}.

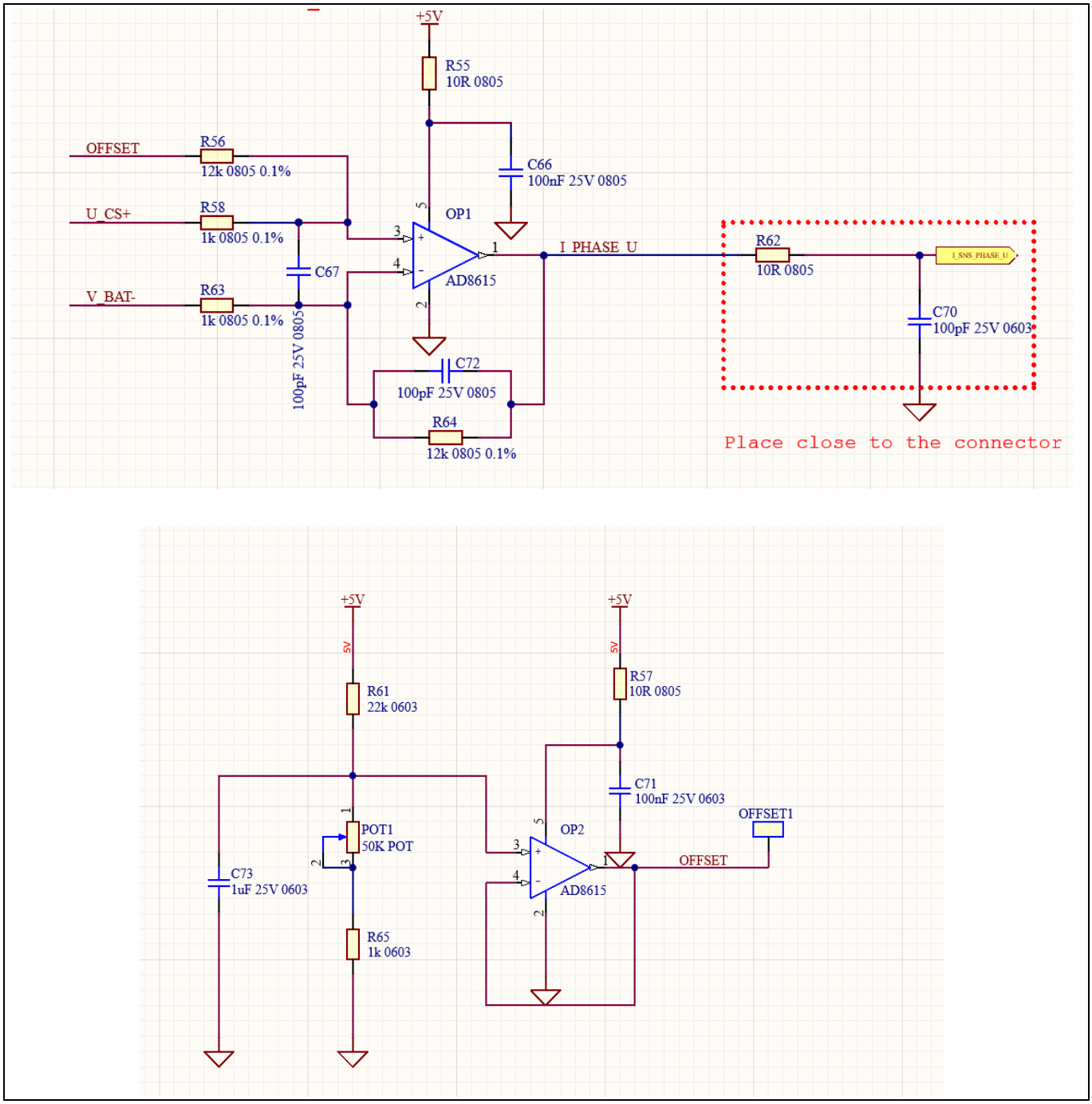


Figure 22 Current amplifier

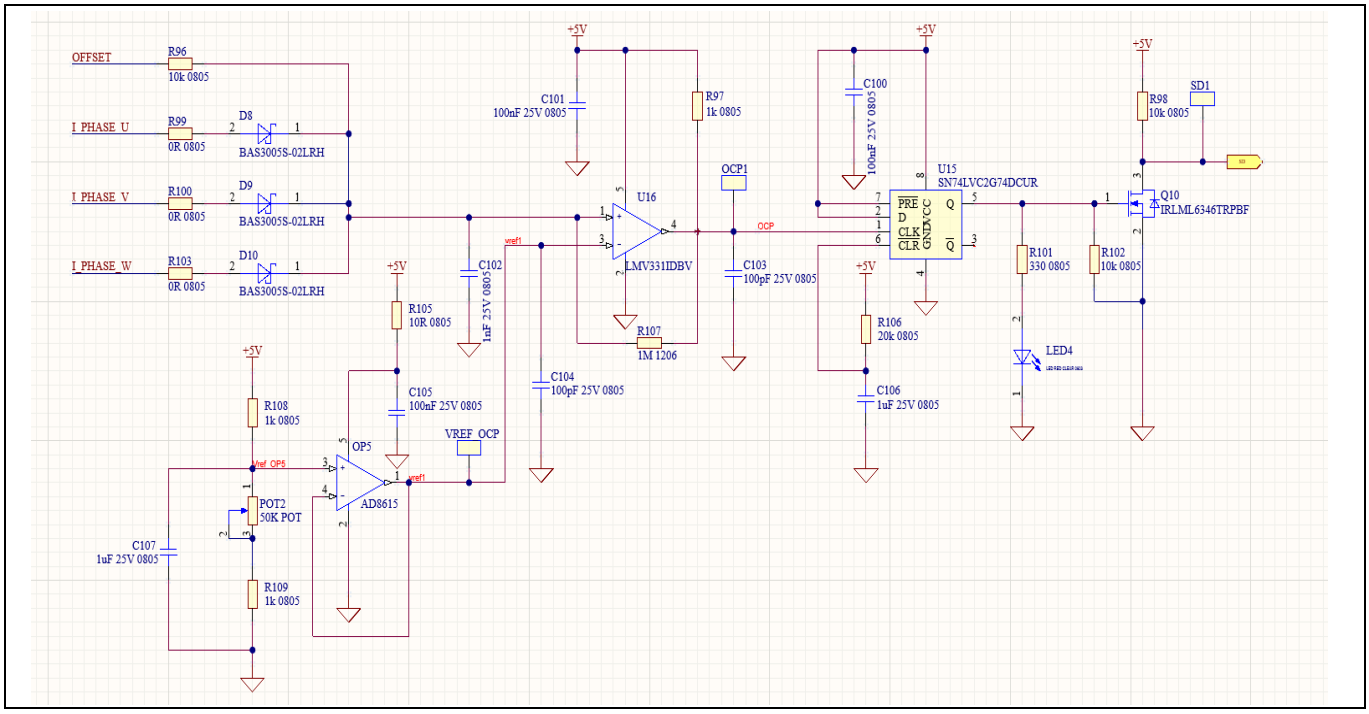


Figure 23 OCP circuitry

2.4.4 Power board connector

Figure 24 shows the interface using the 32-pin connector U12. The pin assignments are shown in **Table 4**.

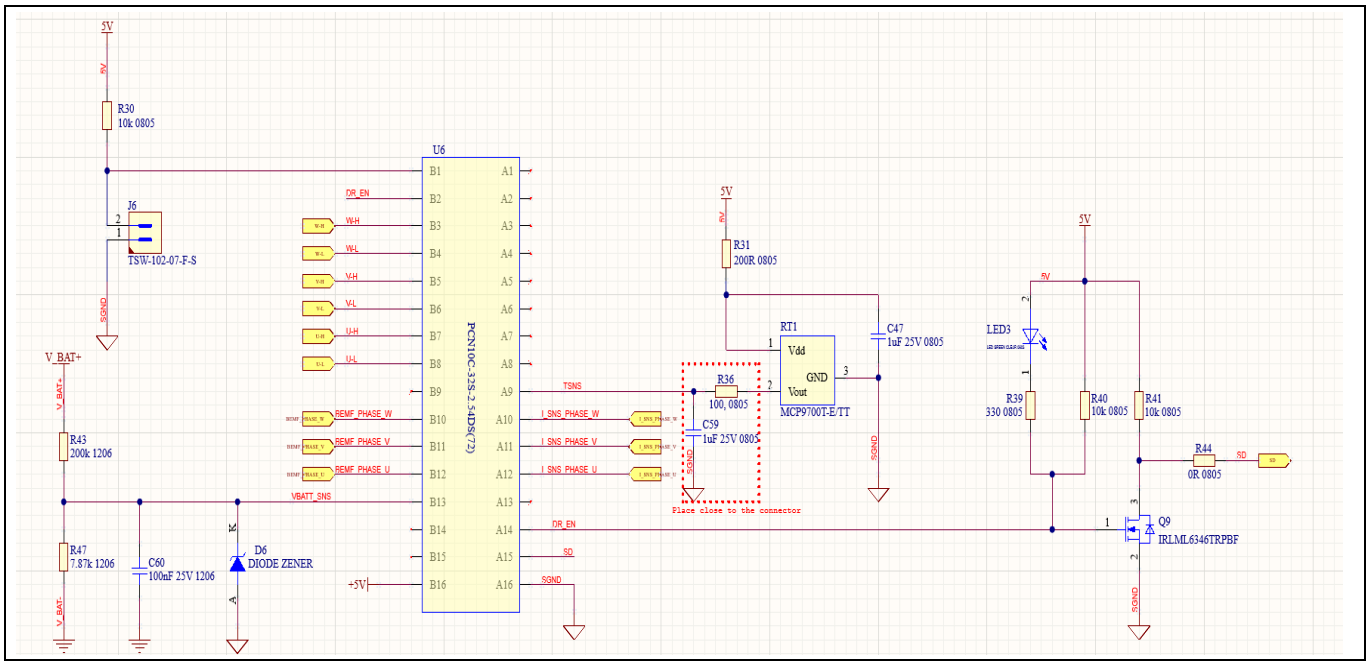


Figure 24 Power board connector

Table 4 Power board connector

X302 MAB32B2	U12 FAB32Q2	Function on power board	Port	Peripherals	
A1	A16	GND	VSS, VSSP		
A2	A15	SD	P0.5	CCU40.CC40	CMP2.OUT
A3	A14	$\overline{\text{DR_EN}}$	P2.2	VADC0.G0CH7	ACMP2.INN
A4	A13	-	P2.4		VADC0.G1CH6
A5	A12	I_SNS_PHASE_U	P2.9	VADC0.G0CH2	VADC0.G1CH4
A6	A11	I_SNE_PHASE_V	P2.10	VADC0.G0CH3	VADC0.G1CH2
A7	A10	I_SNS_PHASE_W	P2.11	VADC0.G0CH4	VADC0.G1CH3
A8	A9	TSNS	P2.1	VADC0.G0CH6	
A9	A8	–	–		
A10	A7	–	–		
A11	A6	–	–		
A12	A5	–	–		
A13	A4	–	–		
A14	A3	–	–		
A15	A2	–	–		
A16	A1	–	–		
B1	B16	V_{CC}	VDD, VDDP		
B2	B15	–	–		
B3	B14	–	–		
B4	B13	VBATT_SNS	P2.3		VADC0.G1CH5
B5	B12	BEMF_U	P2.6	VADC0.G0CH0	
B6	B11	BEMF_V	P2.8	VADC0.G0CH1	VADC0.G0CH0
B7	B10	BEMF_W	P2.0	VADC0.G0CH5	
B8	B9	–	P2.7		VADC0.G1CH1
B9	B8	U-L	P0.1	CCU80.OUT01	
B10	B7	U-H	P0.0	CCU80.OUT00	
B11	B6	V-L	P0.6	CCU80.OUT11	
B12	B5	V-H	P0.7	CCU80.OUT10	
B13	B4	W-L	P0.9 and P0.3	CCU80.OUT21	CCU80.OUT03
B14	B3	W-H	P0.8 and P0.2	CCU80.OUT20	CCU80.OUT02
B15	B2	$\overline{\text{DR_EN}}$	P0.12	CCU80.IN0A, IN1A, IN2A, IN3A	
B16	B1	Direction switch	P0.11	GPIO	

2.4.5 TOLL MOSFET

Infineon's IPT017N12NM6 TOLL MOSFET is used in the power inverter section of this design to drive the BLDC motor phases. The TOLL MOSFET is designed with a drain-down package, as shown in **Figure 25**. For high-current applications, the pads for drain and source should be as large as possible in the PCB to increase the conductivity **[2]**. Additionally, by adding a heatsink at the bottom of the PCB, heat can be passed onto the heatsink through the TIM, enabling the inverter to push more power to the load. **Figure 26** shows the standard cooling technique (bottom-side) resulting in cost savings from cooling systems and the ability to achieve higher power with the same system concept.

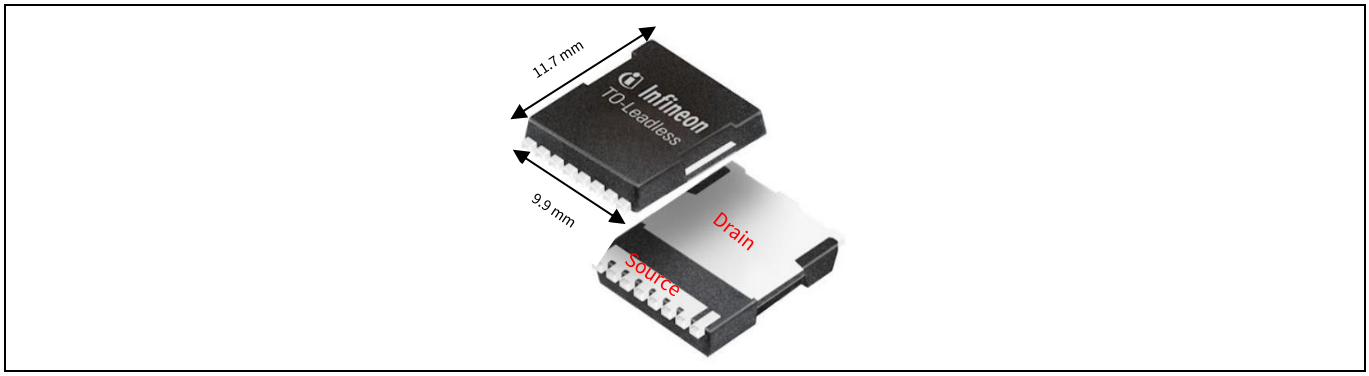


Figure 25 TOLL MOSFET package

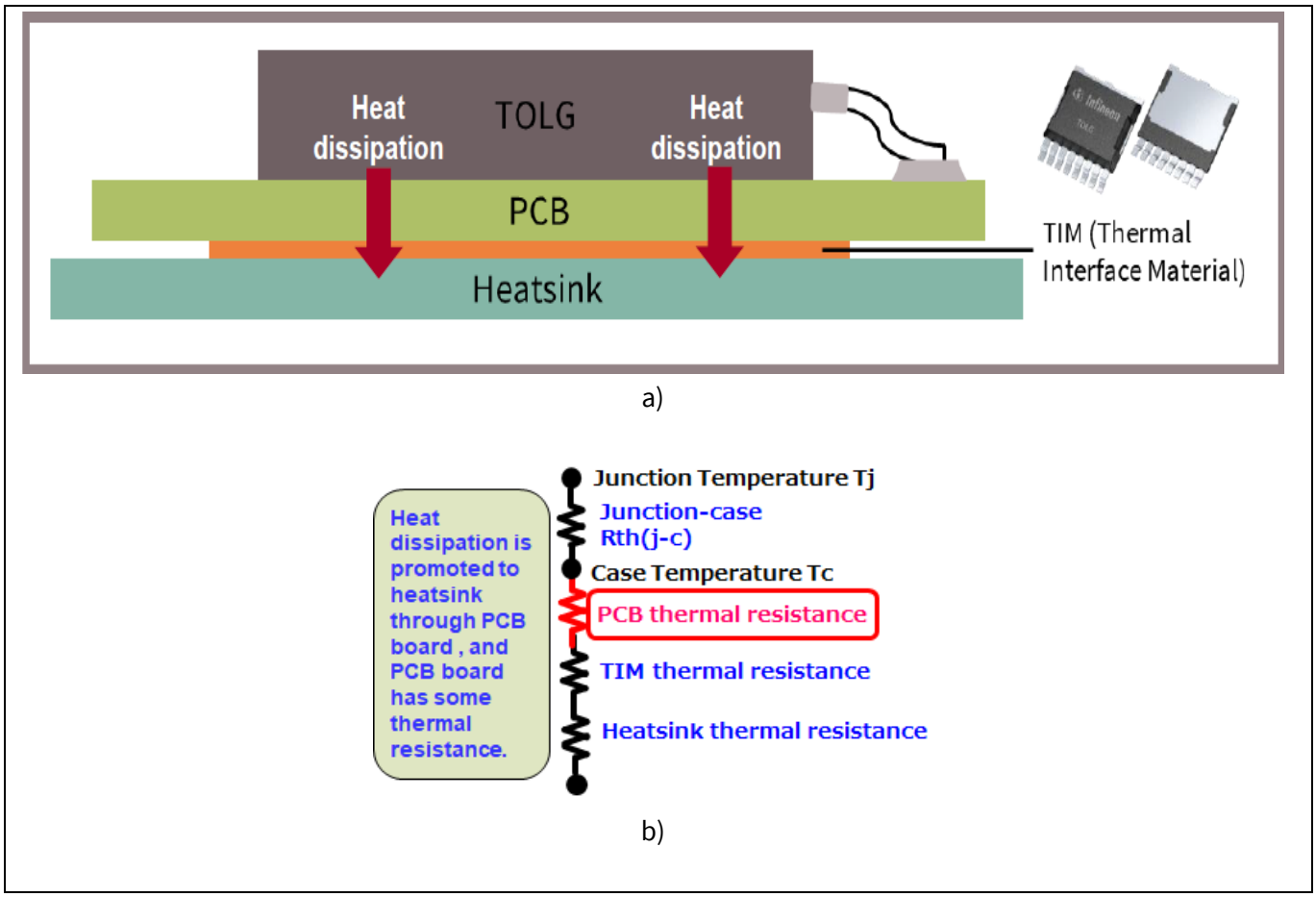


Figure 26 Bottom-side cooling system

2.4.6 Heatsink and thermal insulation material

For a standard (bottom-side) cooling system, a heatsink needs to be added at the bottom of the PCB, resulting in savings from cooling systems and less paralleling of MOSFETs to achieve higher power. A heatsink supplied by Advanced Thermal Solutions (part number ATS-EXL2-254-R0) has been customized for this evaluation board to reach the rated maximum power for this board. **Figure 27** shows the dimensions of the heatsink used in this design.

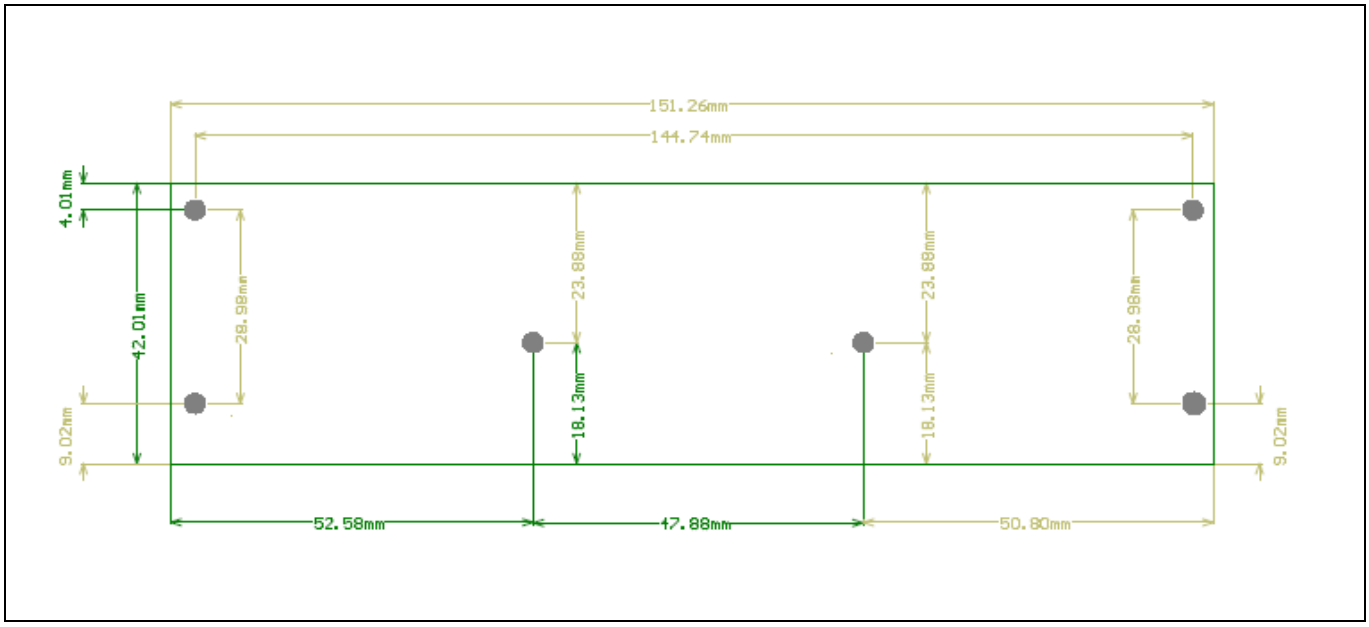


Figure 27 Customized heatsink

The heatsink is mounted to the bottom side of the board, with screws inserted from the top side. The heatsink is drilled and tapped to accept screw size 2-56 with the holes located to line up with the PCB holes. The torque setting for the screws is between 1 in-lb and 2 in-lb.

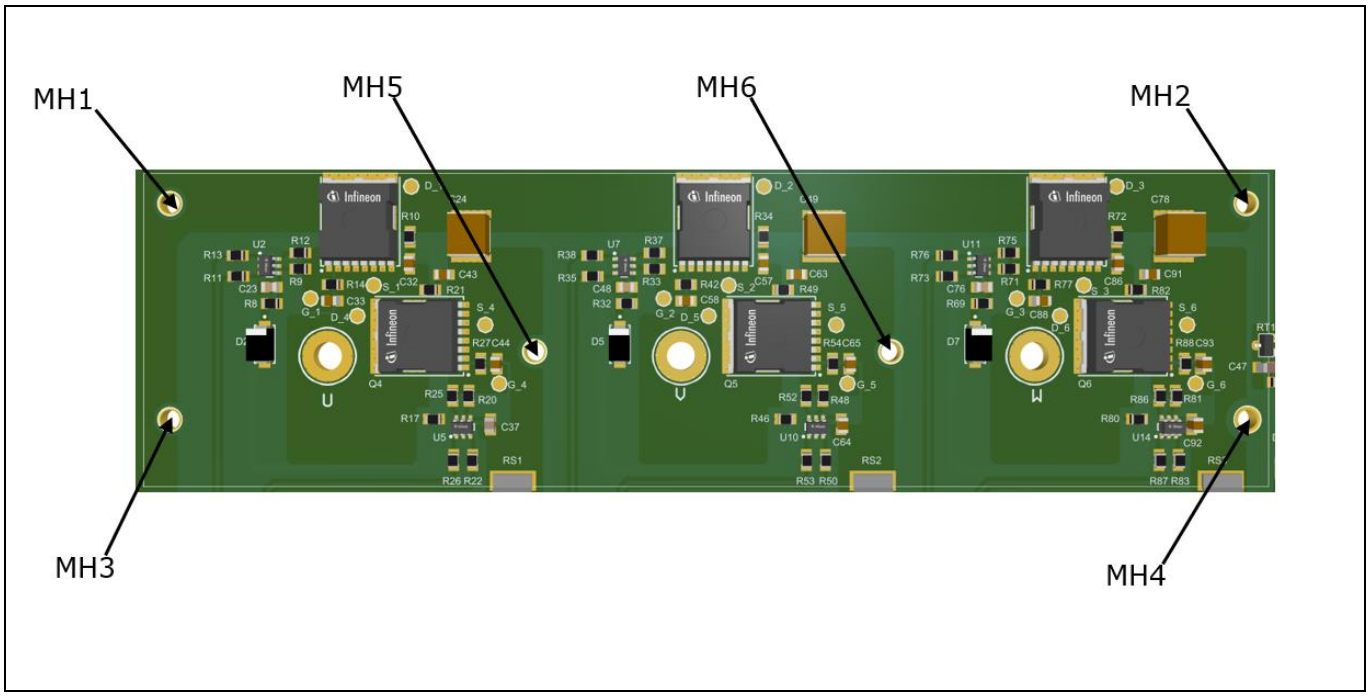


Figure 28 Heatsink mounting hole locations

For this design, a BERGQUIST® GAP PAD® TGP 5000 (gap pad® 5000S35) with 500 µm thickness and 5 W/m-K thermal conductivity is used for the TIM. **Figure 29** shows the typical properties of the selected TIM. Thermal resistance as a function of airflow of this TIM is shown in **Figure 30**.

TYPICAL PROPERTIES OF BERGQUIST® GAP PAD® TGP 5000

PROPERTY	IMPERIAL VALUE	METRIC VALUE	TEST METHOD
Color	Light Green	Light Green	Visual
Reinforcement Carrier	Fiberglass	Fiberglass	—
Thickness (in.) / (mm)	0.020 to 0.125	0.508 to 3.175	ASTM D374
Inherent Surface Tack (1-sided)	2	2	—
Density, Bulk, Rubber (g/cc)	3.6	3.6	ASTM D792
Heat Capacity (J/g-K)	1.0	1.0	ASTM E1269
Hardness, Bulk Rubber (Shore 00)(1)	35	35	ASTM D2240
Young's Modulus (psi) / (kPa)(2)	17.5	121	ASTM D575
Continuous Use Temp. (°F) / (°C)	-76 to 392	-60 to 200	—
ELECTRICAL			
Dielectric Breakdown Voltage (VAC)	> 5,000	> 5,000	ASTM D149
Dielectric Constant (1,000 Hz)	7.5	7.5	ASTM D150
Volume Resistivity (Ω-m)	10^9	10^9	ASTM D257
Flame Rating	V-O	V-O	UL 94
THERMAL			
Thermal Conductivity (W/m-K)	5.0	5.0	ASTM D5470

THERMAL PERFORMANCE VS. STRAIN			
Deflection (% strain)	10	20	30
Thermal Impedance (°C-in.²/W) 0.040 in.(3)	0.37	0.32	0.29

(1) Thirty-second delay value Shore 00 hardness scale.
(2) Young's Modulus, calculated using 0.01 in./min. step rate of strain with a sample size of 0.79 in.².
(3) The ASTM D5470 test fixture was used. The recorded value includes interfacial thermal resistance. These values are provided for reference only. Actual application performance is directly related to the surface roughness, flatness and pressure applied.

Figure 29 Typical properties of GAP PAD® TGP 5000

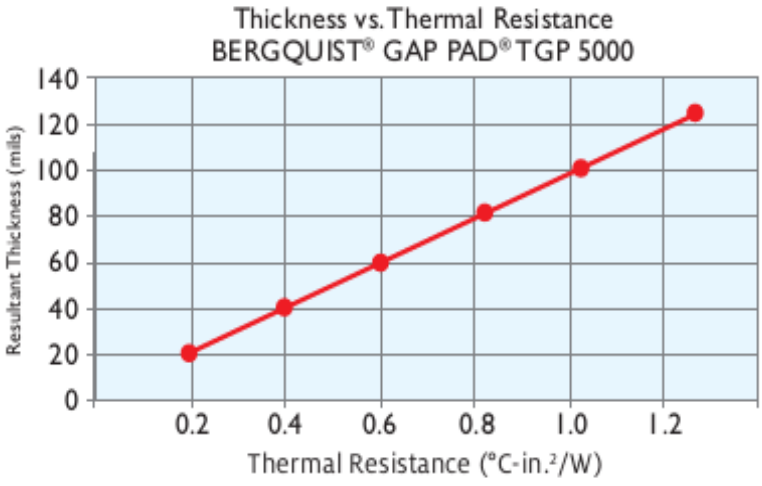


Figure 30 Thermal resistance of GAP PAD® TGP 5000

2.5 Control and firmware

2.5.1 Trapezoidal control also known as six-step or block commutation

In contrast to common synchronous machines, which are driven with sine wave voltages, BLDC motors are most commonly driven with a block-shaped voltage, resulting in a trapezoidal-shaped current. Trapezoidal control is also known as block commutation or six-step control because there are six commutation intervals for each revolution, which are 60 degrees apart. This is the simplest BLDC motor-control algorithm. Although the performance is acceptable for power tools, block commutation is known to create a torque ripple with six times the frequency of the electrical rotary frequency of the three-phase motor. This leads to vibrations and acoustic noise due to the discrete switching between the phases such that the stator and rotor fields are not always perpendicular to each other. This generates high torque ripple, resulting in some inevitable vibration and noise.

In three-phase machines during each commutation step, a current path is formed between a pair of windings, leaving the third winding disconnected. The Hall sensor outputs are either high or low, depending on which pole of the rotor permanent magnet they are in close proximity with, in the current position. During rotation, when one of the rotors' north–south pole interfaces passes a Hall sensor, its output toggles and the controller then switches the DC voltage to the next phase (shown below as "A", "B", or "C"). The XMC1300 series microcontroller has sufficient processing power to execute this control algorithm. As shown below, the voltage has a rectangular shape, which results in a trapezoidal current and a back-EMF shape in the machine.

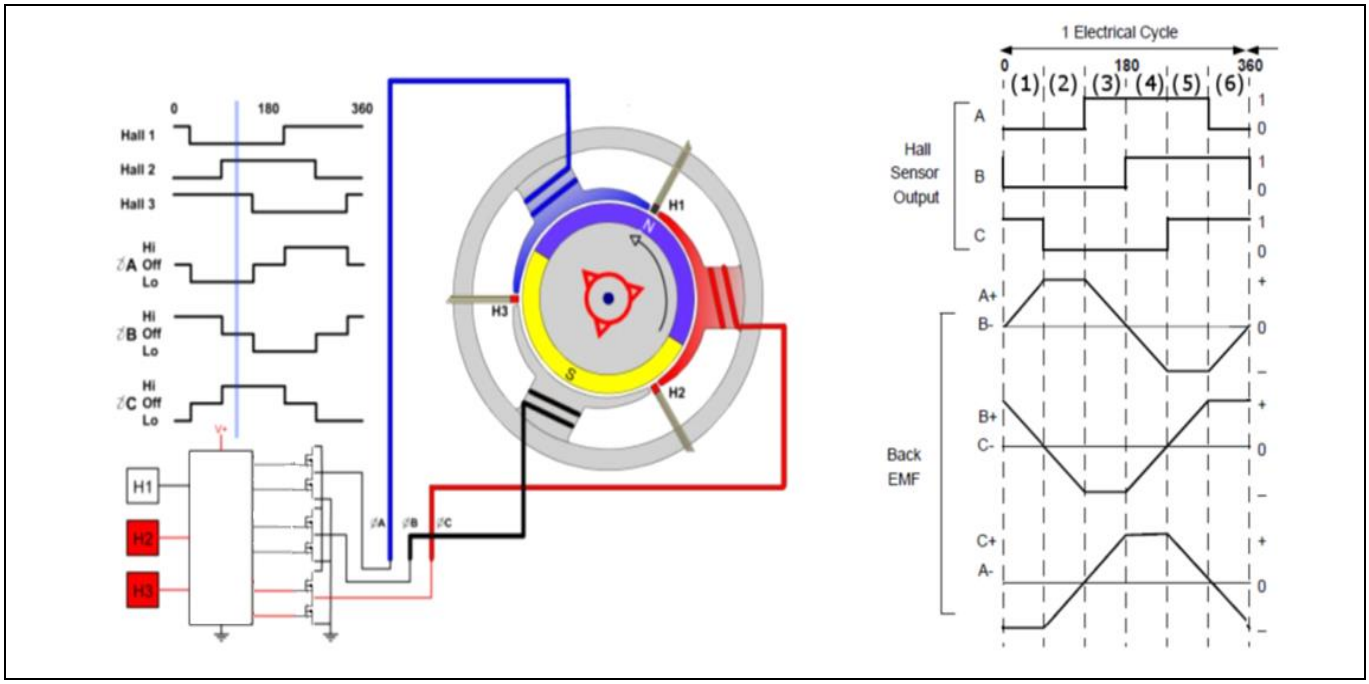


Figure 31 Control of a BLDC motor with Hall sensors

During each commutation step, one of the windings is energized with current entering into it, the second winding has current exiting it, and the third is in a non-energized open-circuit condition. The torque is produced because of the interaction between the magnetic field generated by the stator coils and the permanent magnets. Ideally, the peak torque occurs when these two fields are at 90 degrees to each other and falls off as the fields move together. The block diagram of a typical BLDC trapezoidal control block commutation system with Hall sensors is shown in **Figure 32**.

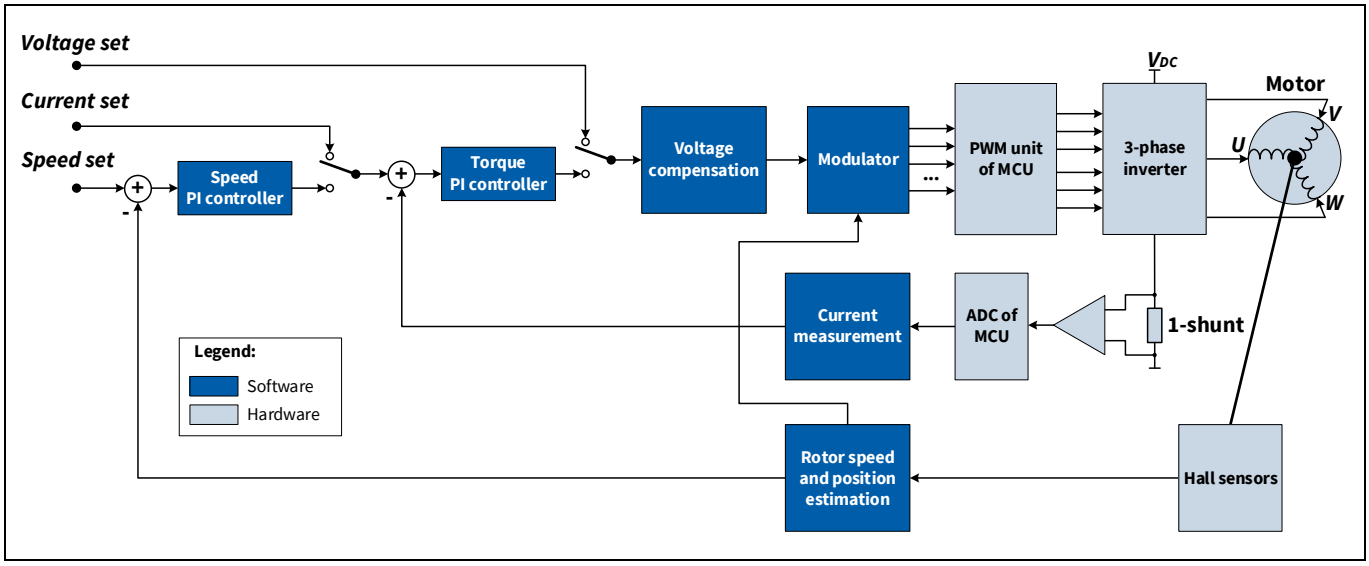


Figure 32 Block diagram of trapezoidal/block commutation algorithm

The switching patterns are shown in **Figure 33**. In the EVAL_TOLL_72VDC_2kW implementation, the 6PWM mode is used, where all of the high- and low-side gate drive pulses are generated by the microcontroller, which also senses the Hall sensor outputs. The firmware is based on the BLDC_SCALAR_HALL_XMC13 platform developed by Infineon and customized for the EVAL_TOLL_72VDC_2kW board.

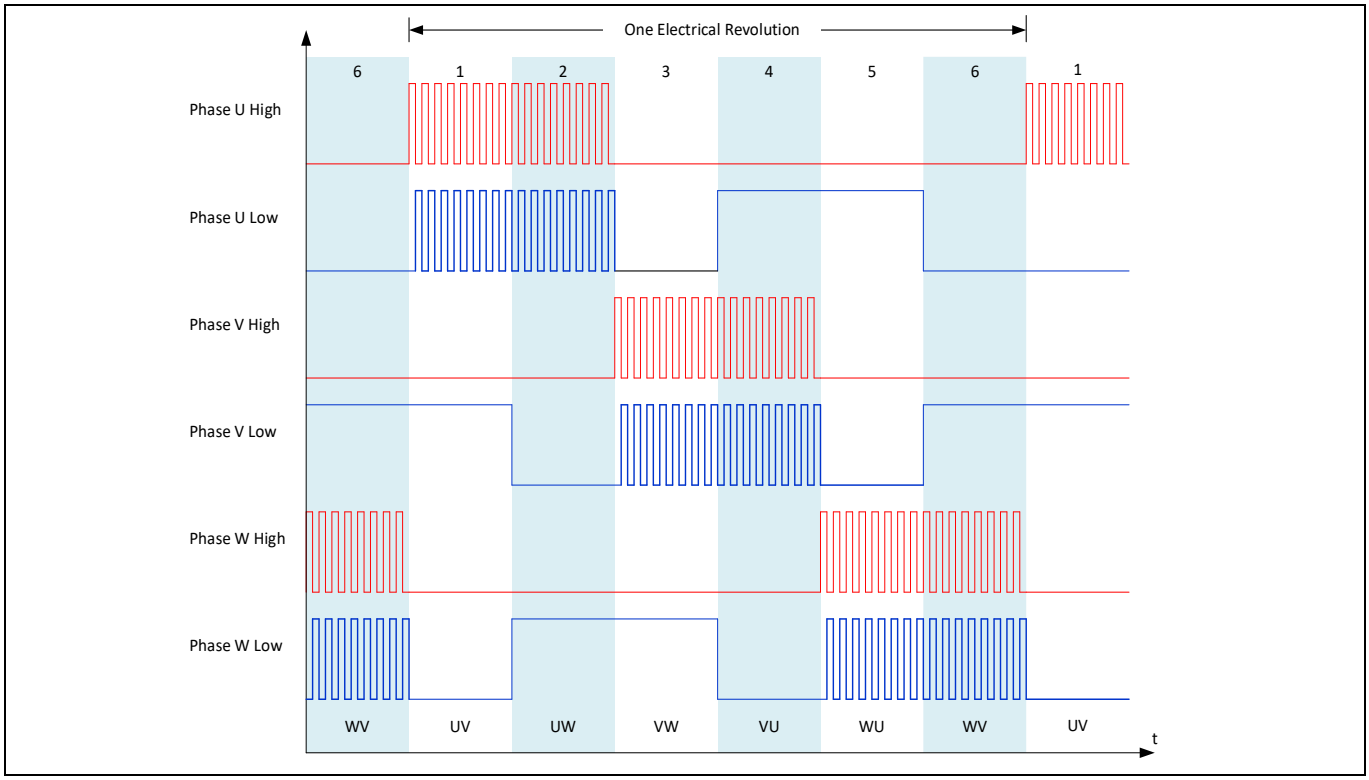


Figure 33 Switching patterns for trapezoidal/block commutation

2.5.2 P-I control

As illustrated in the block diagram above, a closed-loop control system is used to regulate the speed. A command value is applied to the system through the potentiometer on the XMC1300 drive card board. The firmware implements a proportional-integral (P-I) control loop, as shown:

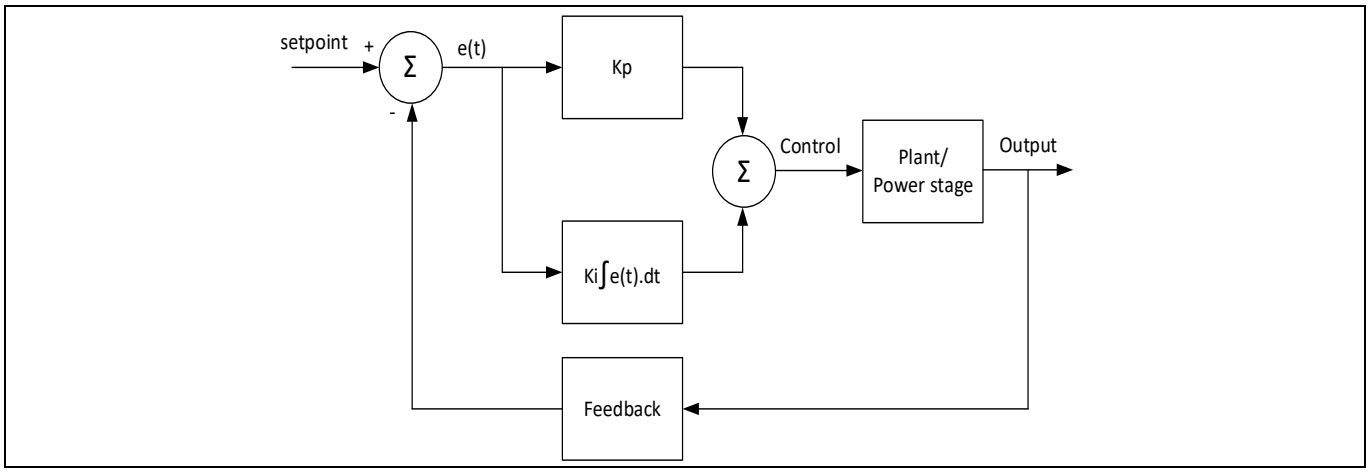


Figure 34 P-I control block diagram

The P-I controller is a widely used feedback control mechanism, which continuously calculates an error value e(t) that is the difference between the setpoint of the measured output quantity (here, speed in RPM) and the actual measured value. In this case the speed is derived by the firmware from the Hall sensor input signals. The error value is fed to the proportional calculator, where it is multiplied by K_P, and to the integral calculator, where it is integrated with respect to time and the result multiplied by K_I. These two results are then summed to provide a control value, which is applied to the power stage to provide a correction that will adjust the output to match the setpoint. The goal is to optimize the values of K_P and K_I for the specific system (inverter and motor) to achieve minimal delay and overshoot when changes are made to the commanded speed.

3 Experimental results

3.1 New OptiMOS™ 6 vs. BiC OptiMOS™ 3 120 V MOSFETs

In the following sections, the experimental results are reported using new OptiMOS™ 6 120 V (IPT017N12NM6) MOSFETs and BiC OptiMOS™ 3 120 V (IPT030N12N3) MOSFETs in a three-phase BLDC motor-drive application. In this application, both conduction and switching losses impact the overall system efficiency because the high-side MOSFET is hard-switching and the low-side MOSFET is soft-switching. EVAL_TOLL_72VDC_2kW is used as the evaluation board to test these devices in the specified application without adding RC snubbers and a heatsink in order to highlight the advantages of the OptiMOS™ 6 technology. In **Table 5**, applied test conditions for the specified application are highlighted. For this case, the operating waveforms for different transitions of the MOSFETs, power loss calculations, power measurements from the power analyzer, and thermal data are provided for comparison of the devices.

Table 5 Test conditions

Parameter	Value/description	Unit/type
Ambient temperature	25	°C
DC input voltage	72	V
Target output power	950[3]	W
Maximum motor speed	1700	RPM
Commutation method	Trapezoidal/Block commutation	
Rectification	Synchronous	
Switching frequency	10	kHz
Dead time	2	µs
Cooling	Air	
Test duration	12	Minutes

[3] The test was performed without RC snubbers and bottom-side heatsink in order to highlight the advantages of the OptiMOS™ 6 MOSFET technology. During the test, maximum output power was controlled by limiting the maximum MOSFET temperature to 100°C after 12 minutes of continuous operation at maximum load.

3.1.1 Test setup description

3.1.1.1 Evaluation board

The motor speed is set by adjusting POT1/R103 in the drive card. **Figure 35** shows the three-phase power board connected to an XMC1300 drive card.

The following order is recommended to power up the board:

1) Output phases are connected to the BLDC motor. The order of the phases is important, as the motor will not operate correctly if the phases are connected incorrectly. **Table 6** shows the connector for each of the phases.

Table 6 Motor phase connectors

Motor phase	Connector
Phase U	U
Phase V	V
Phase W	W

2) The three Hall sensors are connected directly to the XMC1300 drive card via connector X101. **Table 7** shows the pinout for the Hall sensor interface.

Table 7 Hall sensor interface (X101)

Pin	Description
1	GND
2	Phase U Hall sensor
3	Phase V Hall sensor
4	Phase W Hall sensor
5	V_{DD} (+5 V)

3) The XMC1300 drive card is connected to the power board through the power board connector.
4) If using onboard power supplies, pin 1 and pin 2 should be shorted via J2.
5) If using external power supplies, pin 2 and pin 3 should be shorted using J2 if using an external 12 V power supply, and R1 should be removed if using an external 5 V power supply.
6) The input power supply to the power board should be connected to J1 (+) and J4 (-).[4]

[4] It is recommended to use short cables for the input power supply to limit the ripple current passing through the input bulk capacitors.

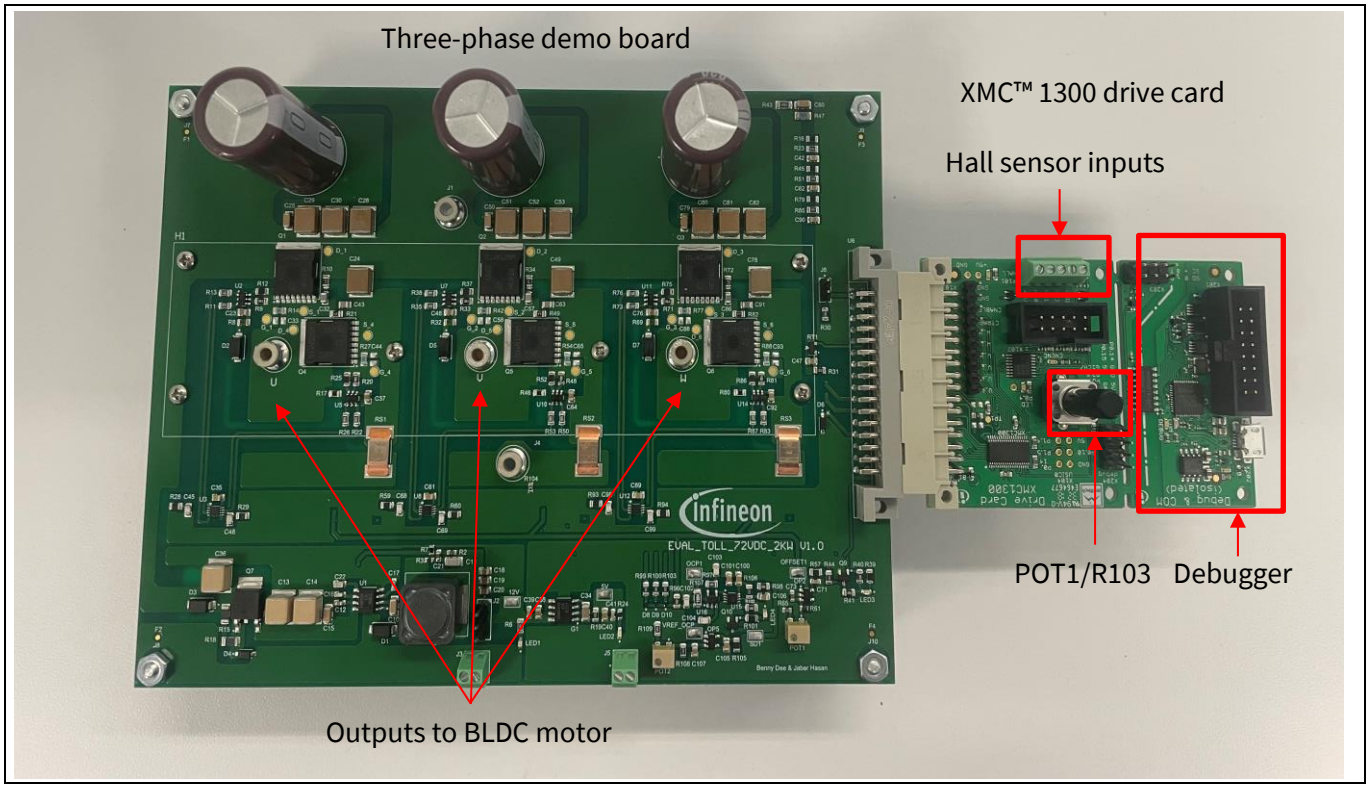


Figure 35 Three-phase power board connected to XMC1300 drive card

3.1.1.2 Description of the test setup

In this test setup, in order to load the motor, it was coupled with another motor (generator), rectifying the phase voltages of the generator and loading it with a resistive load. The schematic of the test setup and actual test bench setup is shown in **Figure 36** and **Figure 37**, respectively. **Table 8** lists the test bench equipment used during testing of the evaluation board.

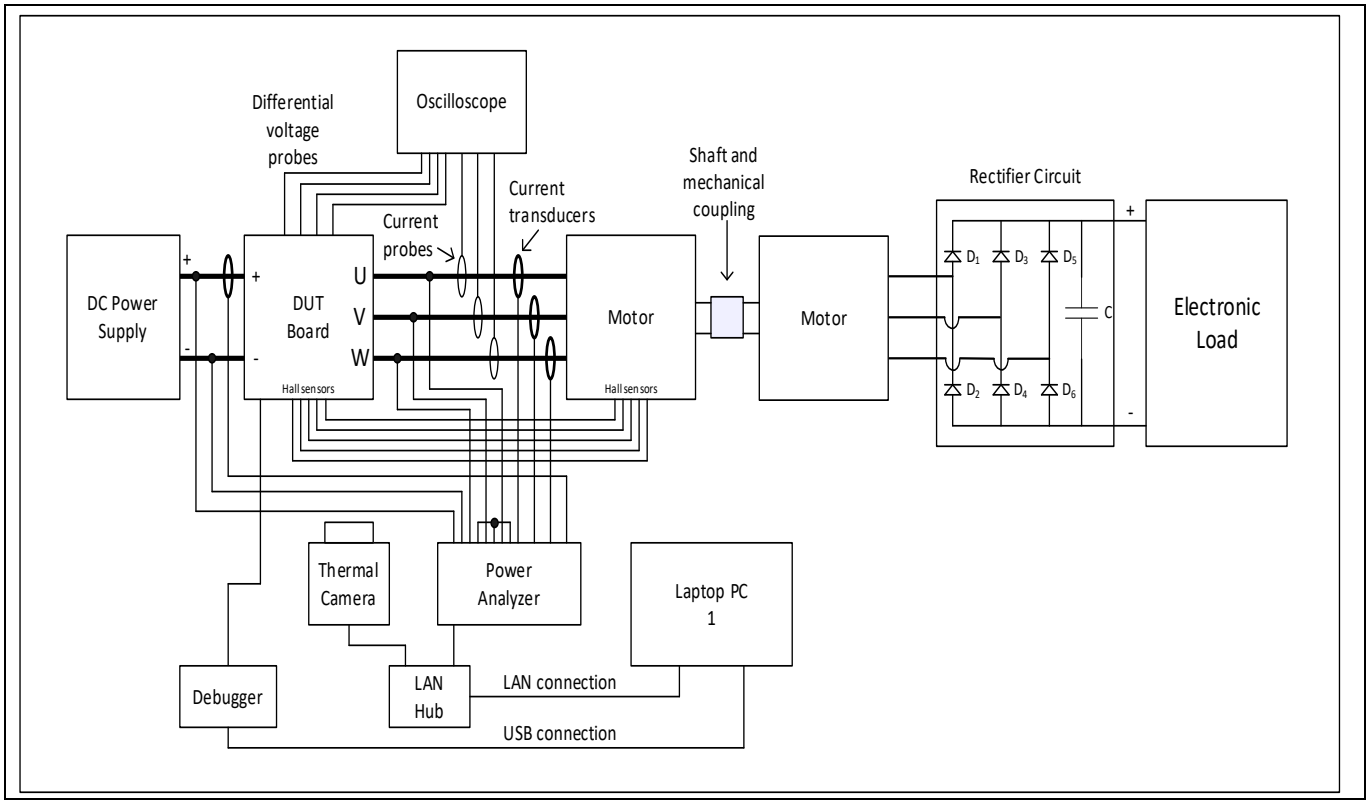


Figure 36 Schematic of the test setup

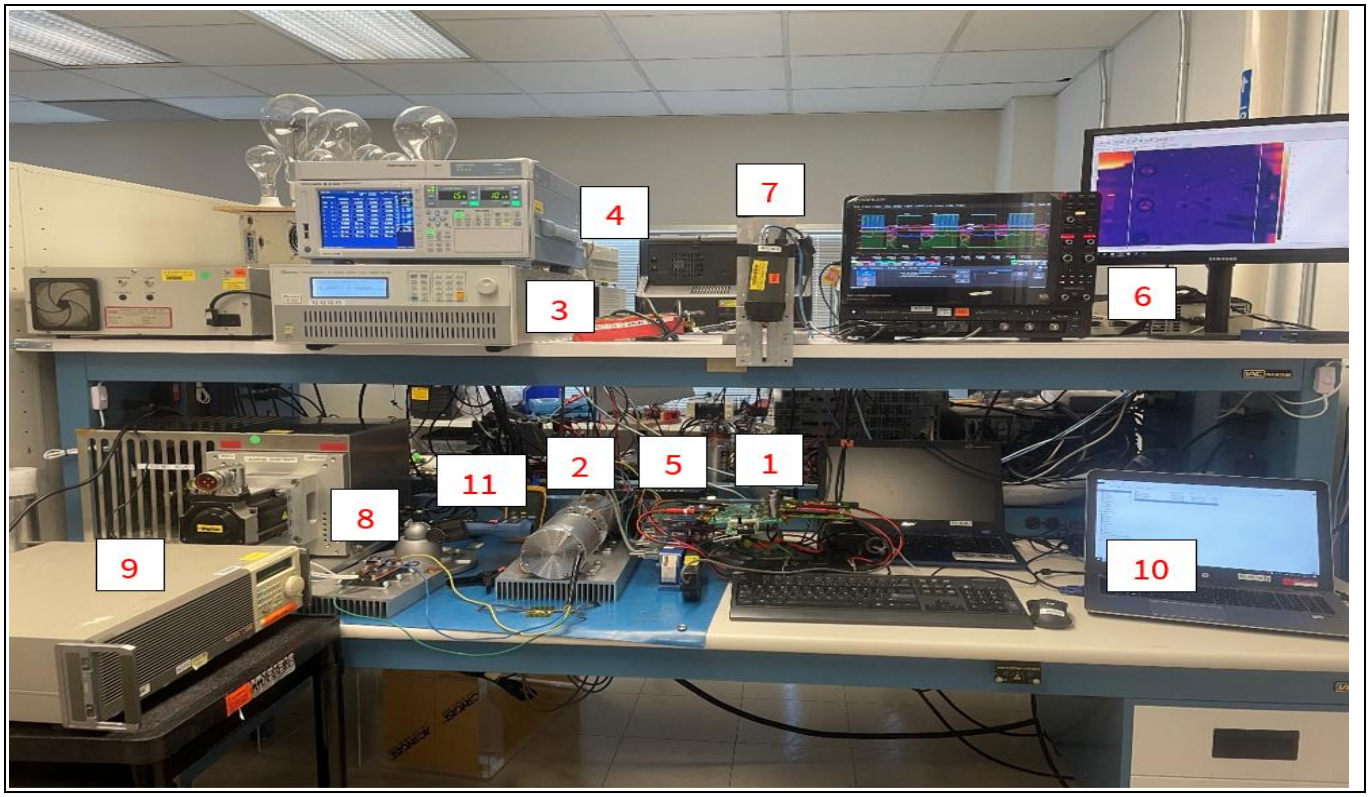


Figure 37 Test bench setup

Table 8 Test bench equipment

Test	Description
1	Device under test (DUT)
2	Motor under test
3	Power supply (100 V, 100 A)
4	Power analyzer (four-channel)
5	Current transducer (200 A)
6	Oscilloscope (eight-channel)
7	Thermal camera
8	Rectifier
9	Electronic load
10	Laptop PC (1)
11	Tachometer

3.1.2 Gate drive circuitry

The gate of the MOSFET is an uncharged capacitor at turn-on. The current is limited only by the internal gate resistor – a typical internal gate resistor for the OptiMOS™ 3 (IPT030N12N3) MOSFET is 1.3 Ω and for the OptiMOS™ 6 (IPT017N12NM6) is 1.1 Ω. In a motor-drive application, a typical external gate resistor is more than 30 Ω for turn-on and more than 10 Ω for turn-off in order to prevent the MOSFETs' drain-source voltage from avalanching at maximum load.

In a motor-drive application, the high-side MOSFET is hard-switching and the low-side MOSFET is soft-switching in a half-bridge topology, as shown in **Figure 38**. **Figure 38** shows the external gate resistor used for turn-on and turn-off for the high-side and low-side MOSFETs for a three-phase motor-drive application for both OptiMOS™ 6 and OptiMOS™ 3 devices. The resistors were adjusted to prevent high-side MOSFET drain-source voltage from avalanching and false turn-on of the low-side MOSFET at maximum load. The external gate turn-on and turn-off resistor is adjusted to 49.9 Ω and 6.8 Ω, respectively, for OptiMOS™ 6 devices. Similarly, the external gate turn-on and turn-off resistor is adjusted to 62 Ω and 3.3 Ω, respectively, for OptiMOS™ 3 devices; the OptiMOS™ 6 devices require a lower-value turn-on resistor to obtain dv/dt slew rate lower than 3 V/ns leading to lower turn-on losses and improved thermals. Additionally, in order to prevent false turn-on of the low-side MOSFET, a 3.3 nF capacitor across gate-source is placed on the low-side MOSFET in order to satisfy $\frac{Q_{gd}}{Q_{gs(th)}} < 1$.

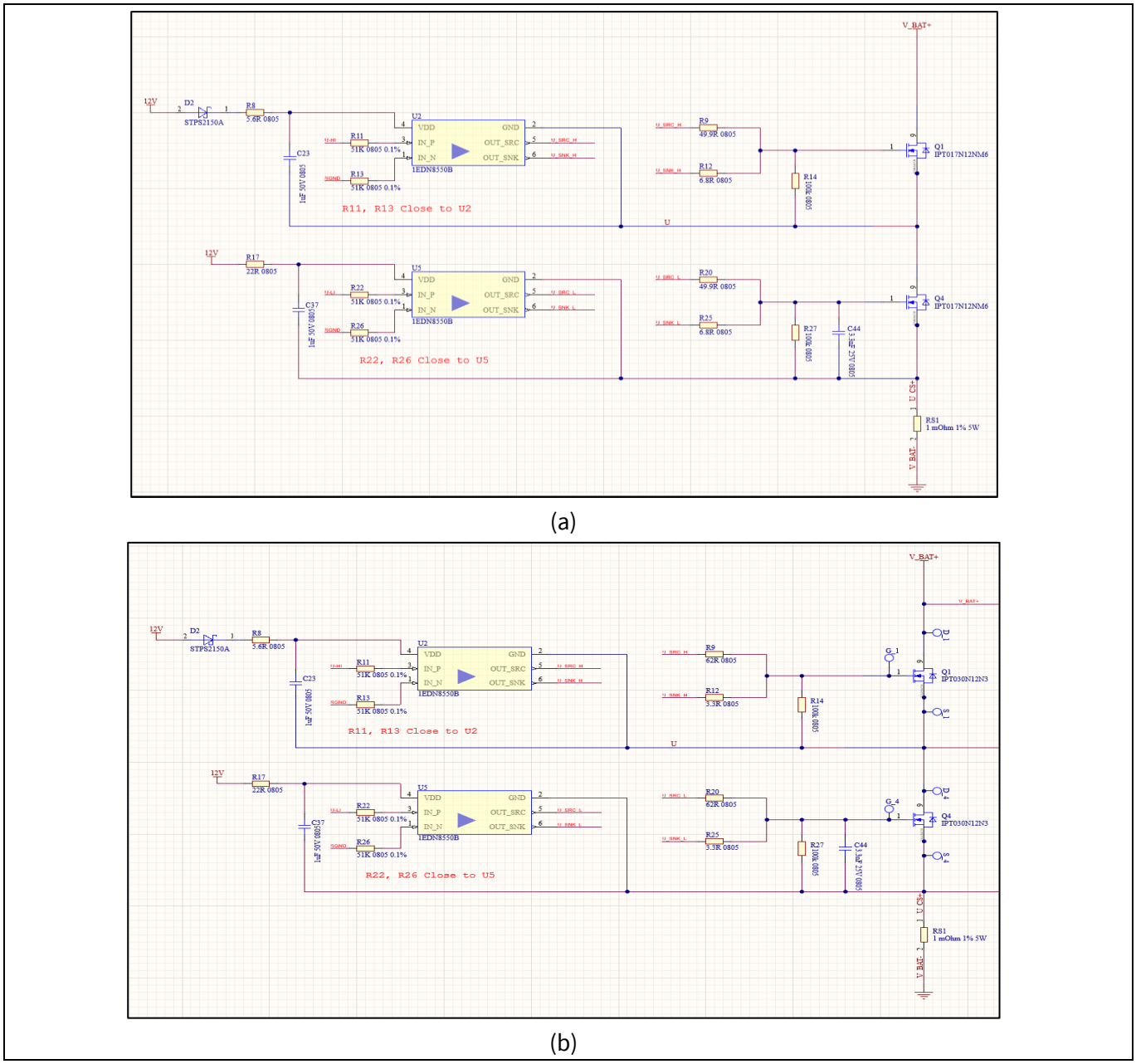


Figure 38 Single phase leg of three-phase inverter a) OptiMOS™ 6; b) OptiMOS™ 3

3.1.3 Operating waveforms

Figure 39 and **Figure 40** show gate-source and drain-source voltages of both high-side and low-side MOSFETs for phase V, and also the phase V current using the synchronous rectification trapezoidal control method at 1700 RPM with an input power of 985 W for OptiMOS™ 6 (IPT017N12NM6) devices at 72 V input voltage for 1 ms/div and 500 µs/div.

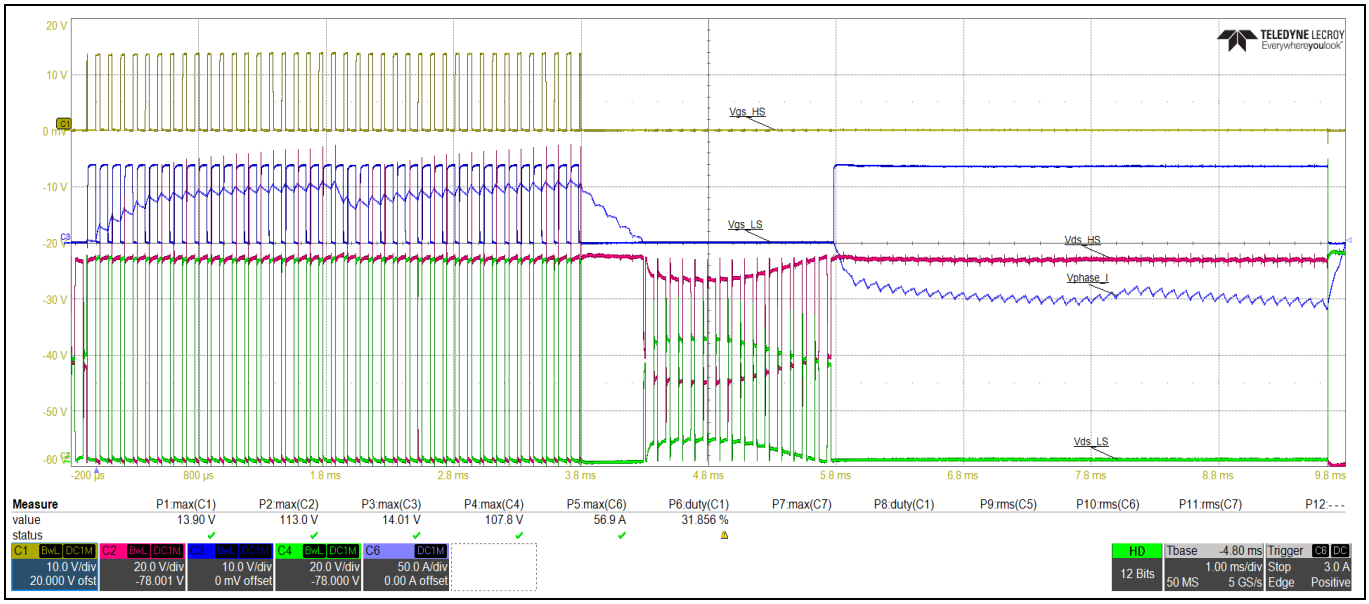


Figure 39 **High-side and low-side MOSFET gate-source and drain-source voltages for phase V (1 ms/div) for OptiMOS™ 6 devices; V_{GS_HS} (yellow), V_{GS_LS} (blue), V_{DS_HS} (pink), V_{DS_LS} (green), I_{PHASE_V} (blue)**

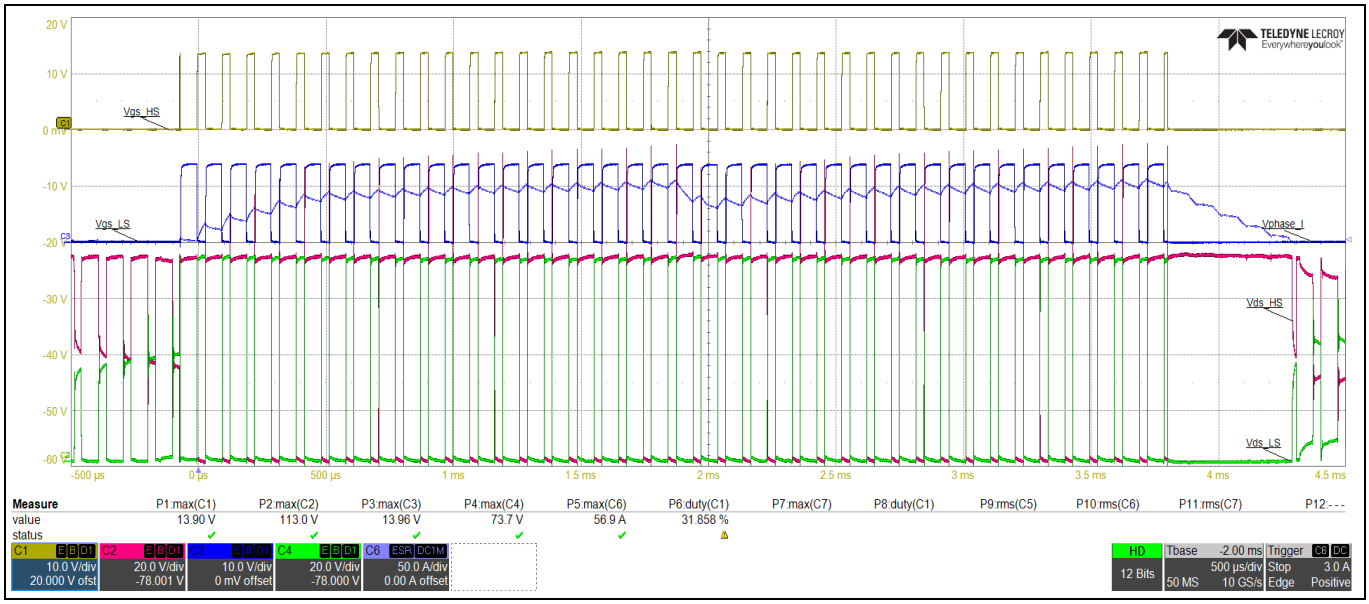


Figure 40 **High-side and low-side MOSFET gate-source and drain-source voltages for phase V (500 µs/div) for OptiMOS™ 6 devices; V_{GS_HS} (yellow), V_{GS_LS} (blue), V_{DS_HS} (pink), V_{DS_LS} (green), I_{PHASE_V} (blue)**

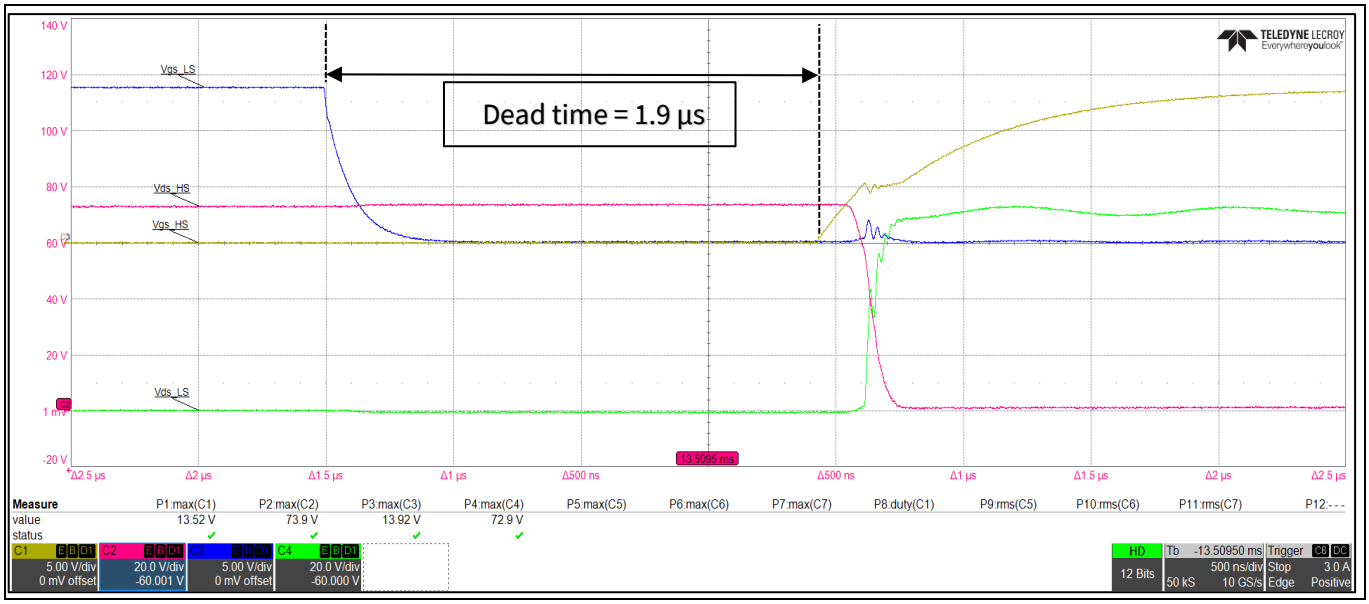


Figure 41 **High-side and low-side MOSFET gate-source and drain-source voltages for phase V for high-side MOSFET turn-on and low-side MOSFET turn-off (500 ns/div) for OptiMOS™ 6 devices; V_{GS_HS} (yellow), V_{GS_LS} (blue), V_{DS_HS} (pink), V_{DS_LS} (green)**

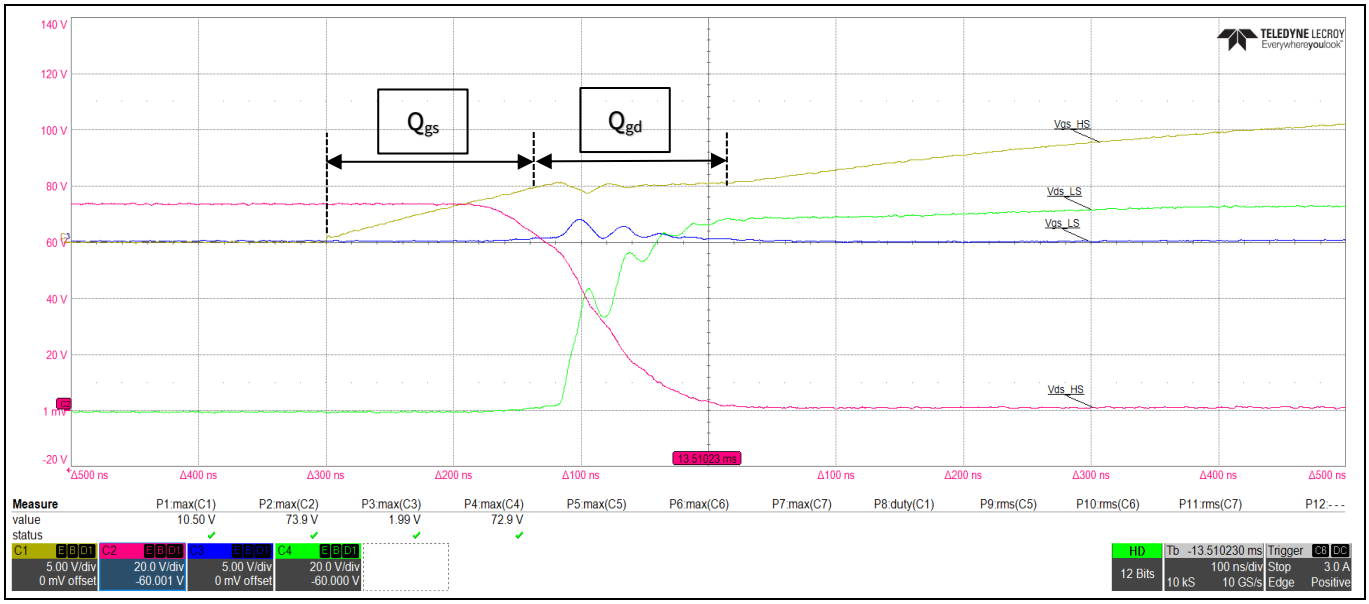


Figure 42 **High-side and low-side MOSFET gate-source and drain-source voltages for phase V for high-side MOSFET turn-on and low-side MOSFET turn-off (100 ns/div) for OptiMOS™ 6 devices; V_{GS_HS} (yellow), V_{GS_LS} (blue), V_{DS_HS} (pink), V_{DS_LS} (green)**

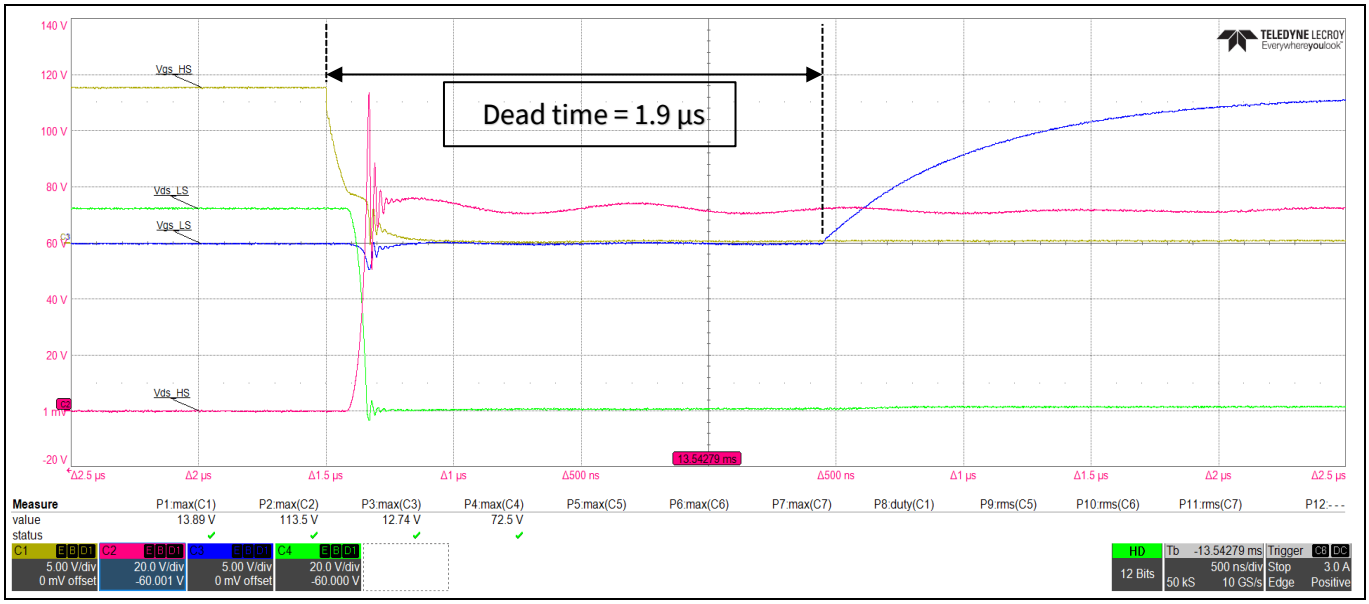


Figure 43 **High-side and low-side MOSFET gate-source and drain-source voltages for phase V for high-side MOSFET turn-off and low-side MOSFET turn-on (500 ns/div) for OptiMOS™ 6 devices; V_{GS_HS} (yellow), V_{GS_LS} (blue), V_{DS_HS} (pink), V_{DS_LS} (green)**

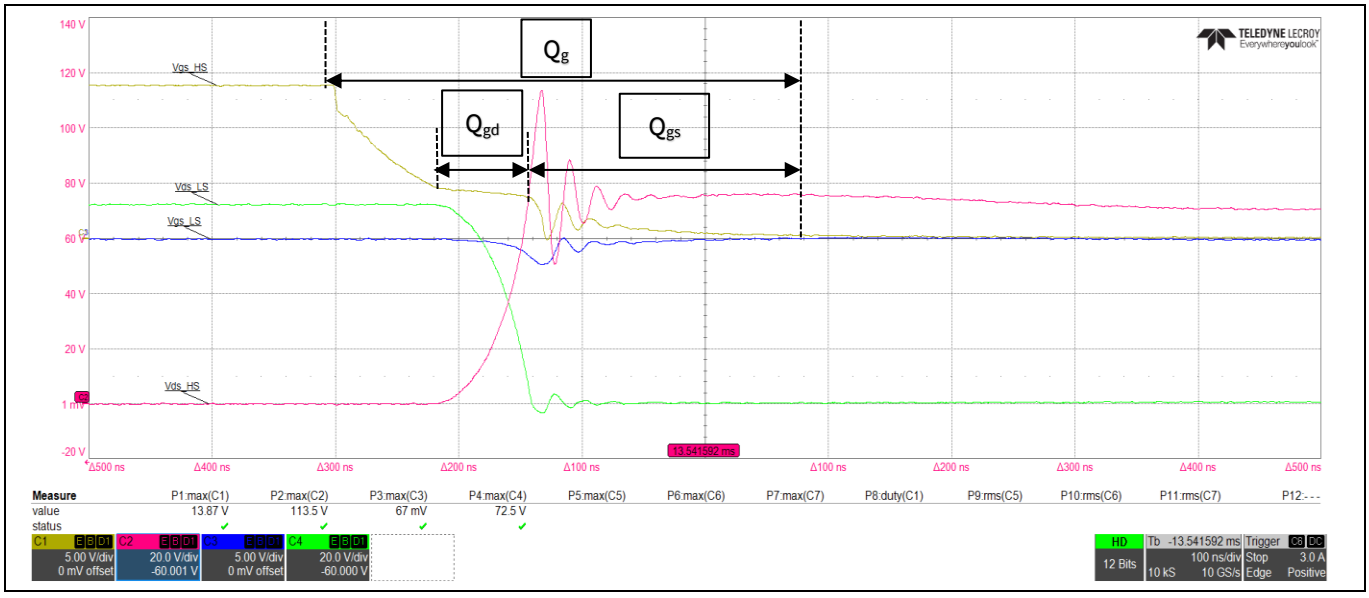


Figure 44 **High-side and low-side MOSFET gate-source and drain-source voltages for phase V for high-side MOSFET turn-off and low-side MOSFET turn-on (100 ns/div) for OptiMOS™ 6 devices; V_{GS_HS} (yellow), V_{GS_LS} (blue), V_{DS_HS} (pink), V_{DS_LS} (green)**

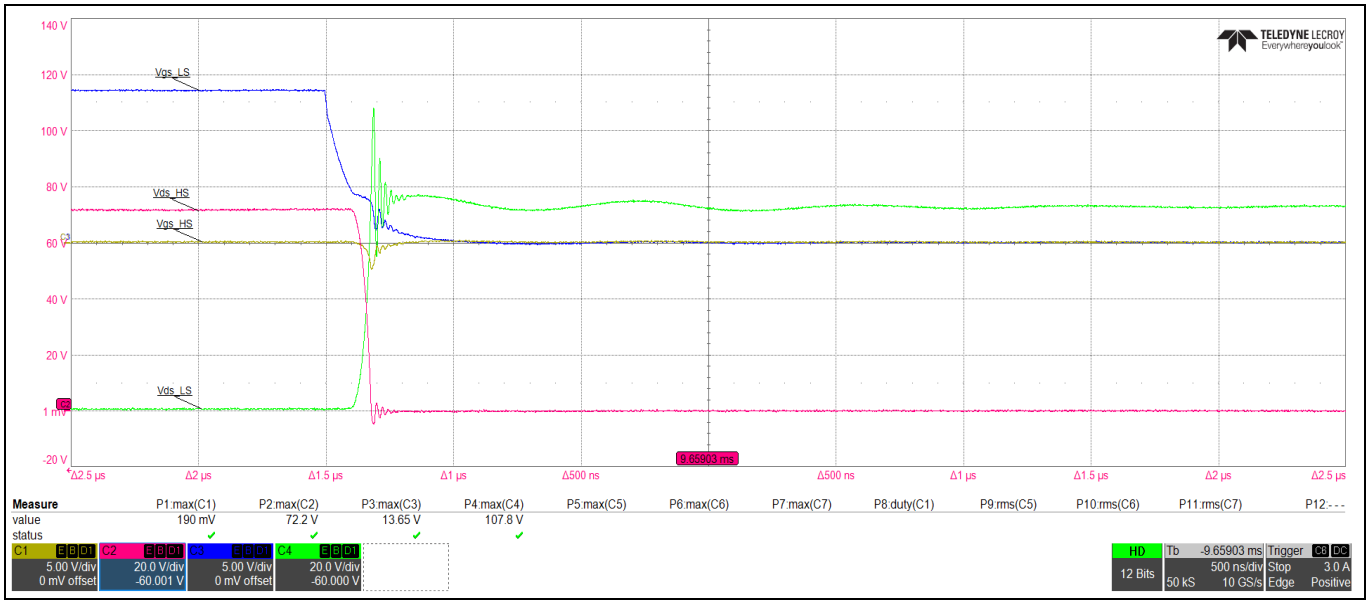


Figure 45 **High-side and low-side MOSFET gate-source and drain-source voltages for phase V during demagnetization period for phase V (500 ns/div) for OptiMOS™ 6 devices; V_{GS_HS} (yellow), V_{GS_LS} (blue), V_{DS_HS} (pink), V_{DS_LS} (green)**

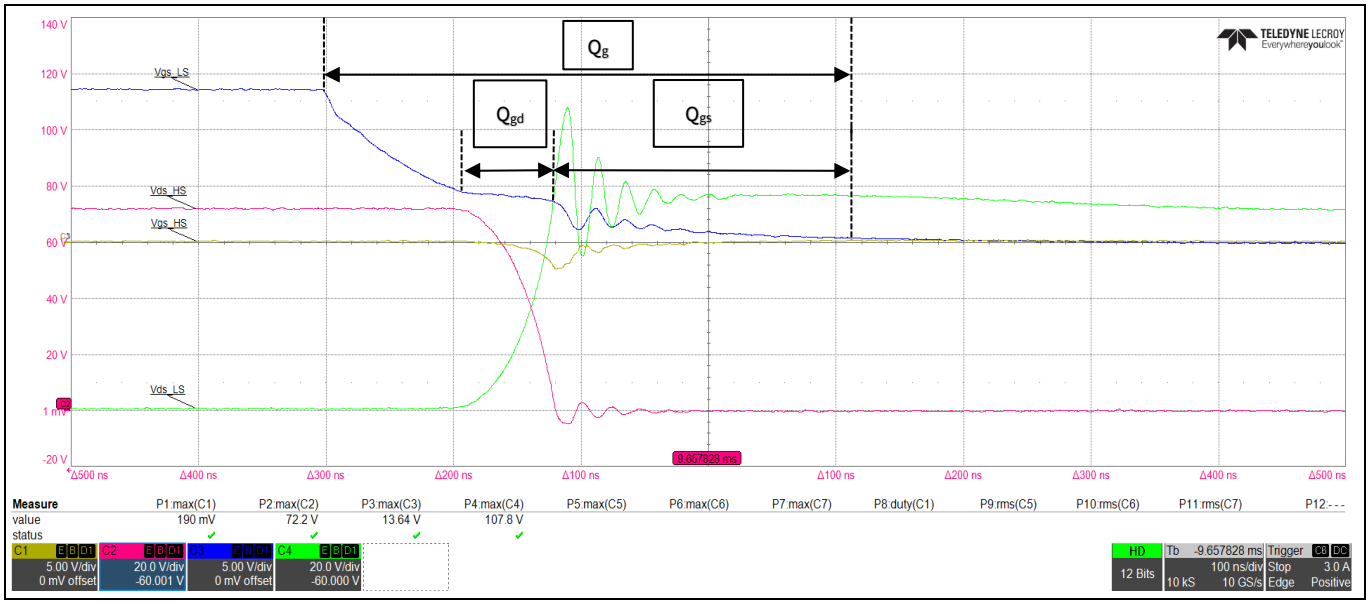


Figure 46 **High-side and low-side MOSFET gate-source and drain-source voltages for phase V during demagnetization period for phase V (100 ns/div) for OptiMOS™ 6 devices; V_{GS_HS} (yellow), V_{GS_LS} (blue), V_{DS_HS} (pink), V_{DS_LS} (green)**

Figure 47 and **Figure 48** show gate-source and drain-source voltages of both high-side and low-side MOSFETs for phase V, and also the phase V current using the synchronous rectification trapezoidal control method at 1700 RPM with an input power of 850 W for OptiMOS™ 3 (IPT030N12N3) devices at 72 V input voltage for 1 ms/div and 500 µs/div.

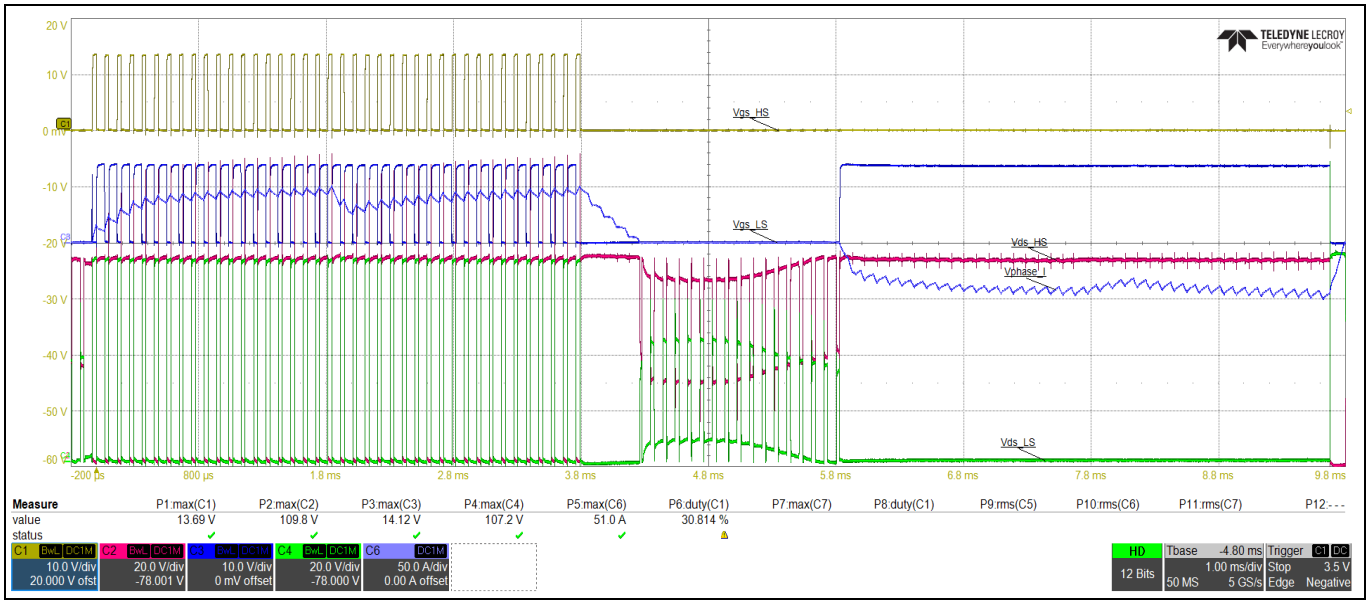


Figure 47 **High-side and low-side MOSFET gate-source and drain-source voltages for phase V (1 ms/div) for OptiMOS™ 3 devices; V_{GS_HS} (yellow), V_{GS_LS} (blue), V_{DS_HS} (pink), V_{DS_LS} (green), I_{PHASE_V} (blue)**

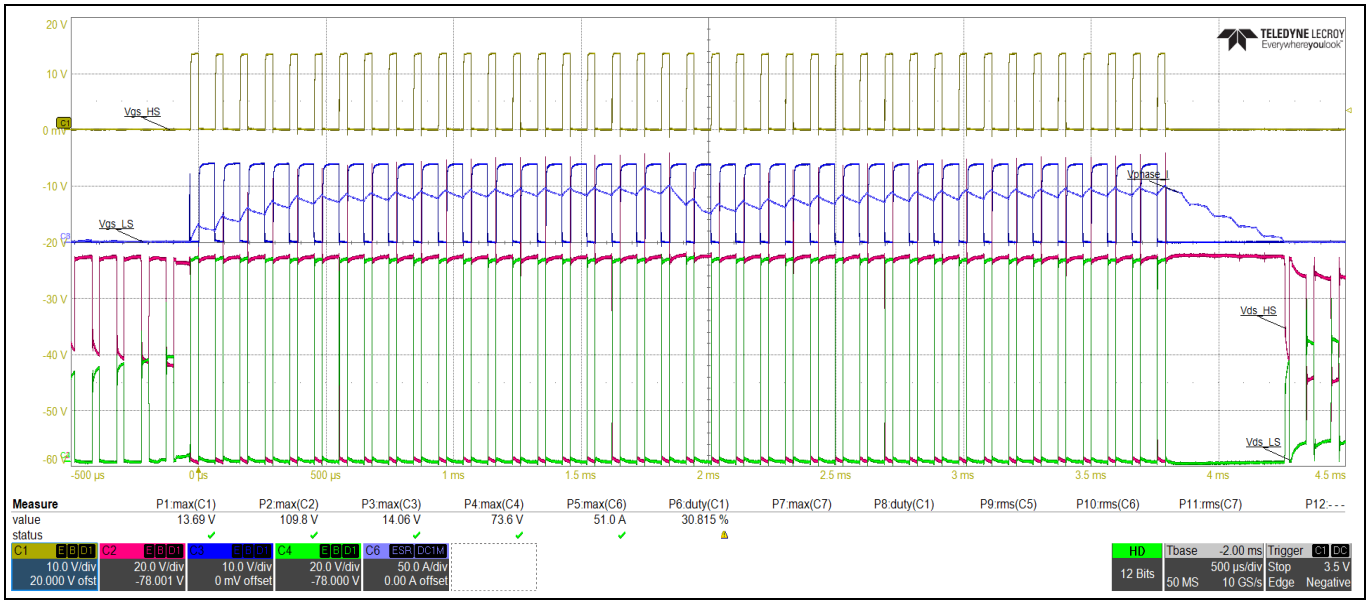


Figure 48 **High-side and low-side MOSFET gate-source and drain-source voltages for phase V (500 µs/div) for OptiMOS™ 3 devices; V_{GS_HS} (yellow), V_{GS_LS} (blue), V_{DS_HS} (pink), V_{DS_LS} (green), I_{PHASE_V} (blue)**

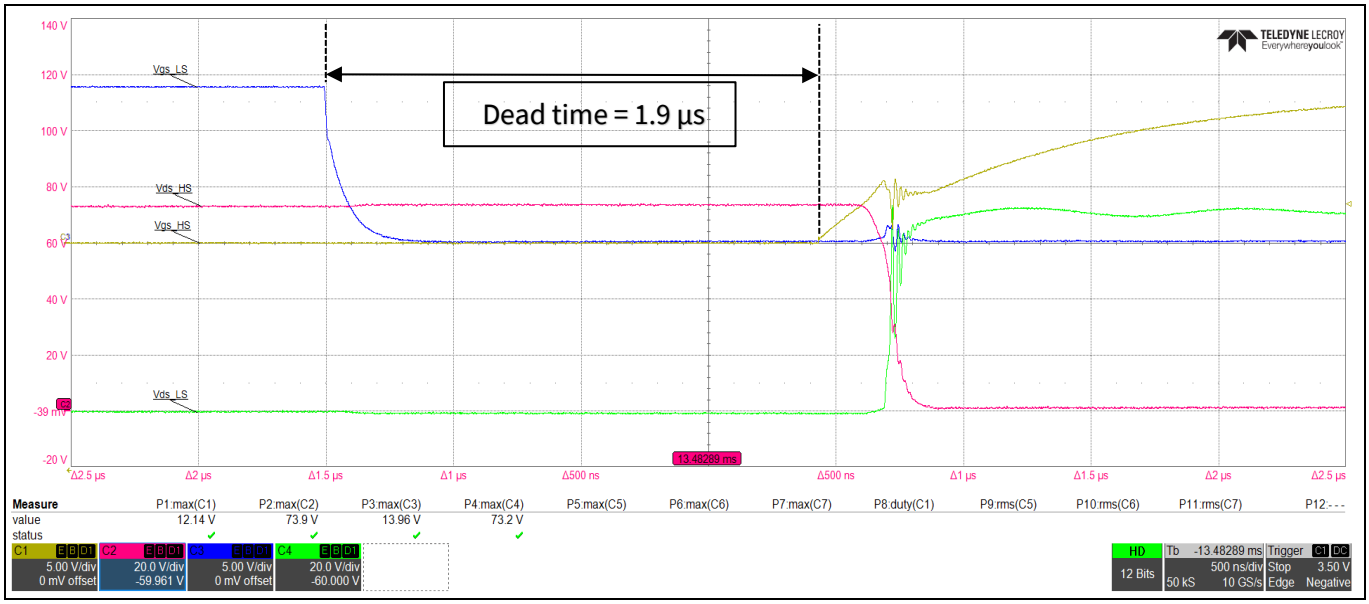


Figure 49 **High-side and low-side MOSFET gate-source and drain-source voltages for phase V for high-side MOSFET turn-on and low-side MOSFET turn-off (500 ns/div) for OptiMOS™ 3 devices; V_{GS_HS} (yellow), V_{GS_LS} (blue), V_{DS_HS} (pink), V_{DS_LS} (green)**

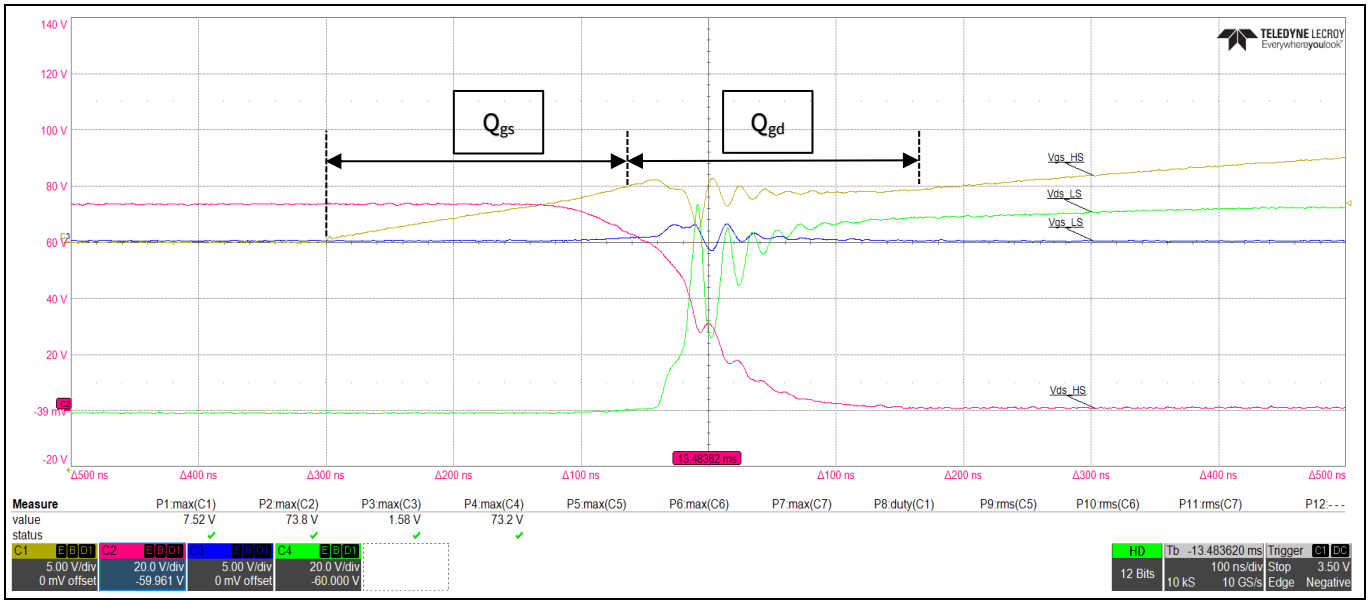


Figure 50 **High-side and low-side MOSFET gate-source and drain-source voltages for phase V for high-side MOSFET turn-on and low-side MOSFET turn-off (100 ns/div) for OptiMOS™ 3 devices; V_{GS_HS} (yellow), V_{GS_LS} (blue), V_{DS_HS} (pink), V_{DS_LS} (green)**

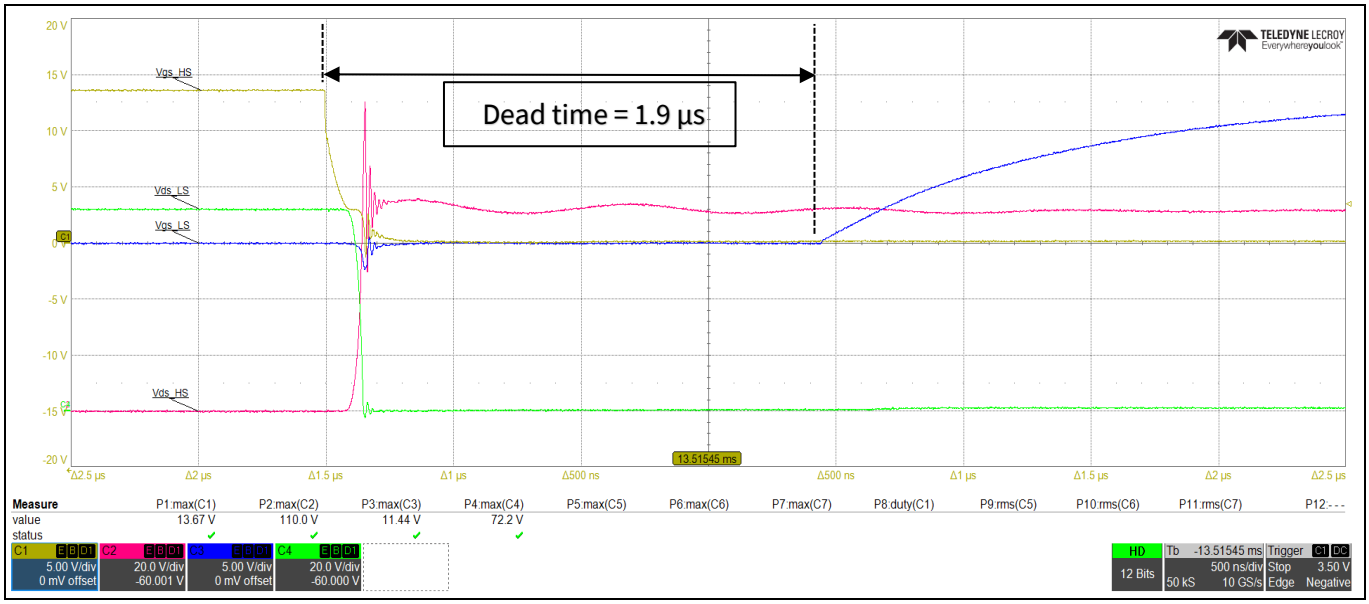


Figure 51 **High-side and low-side MOSFET gate-source and drain-source voltages for phase V for high-side MOSFET turn-off and low-side MOSFET turn-on (500 ns/div) for OptiMOS™ 3 devices; V_{GS_HS} (yellow), V_{GS_LS} (blue), V_{DS_HS} (pink), V_{DS_LS} (green)**

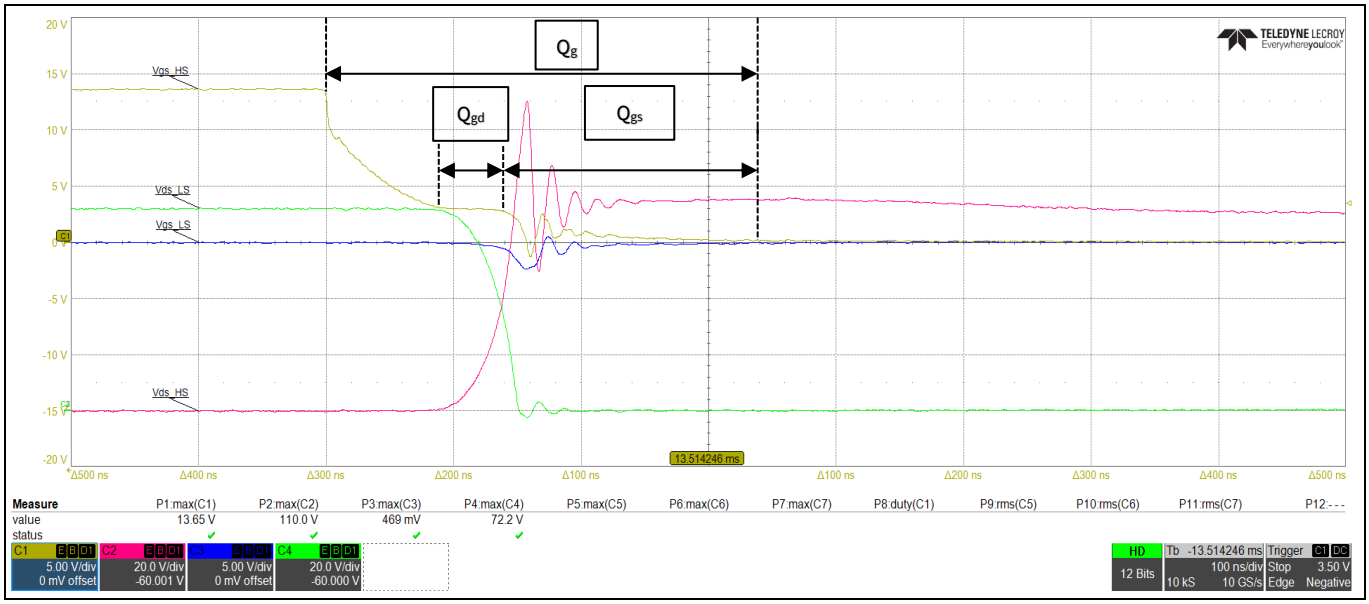


Figure 52 **High-side and low-side MOSFET gate-source and drain-source voltages for phase V for high-side MOSFET turn-off and low-side MOSFET turn-on (100 ns/div) for OptiMOS™ 3 devices; V_{GS_HS} (yellow), V_{GS_LS} (blue), V_{DS_HS} (pink), V_{DS_LS} (green)**

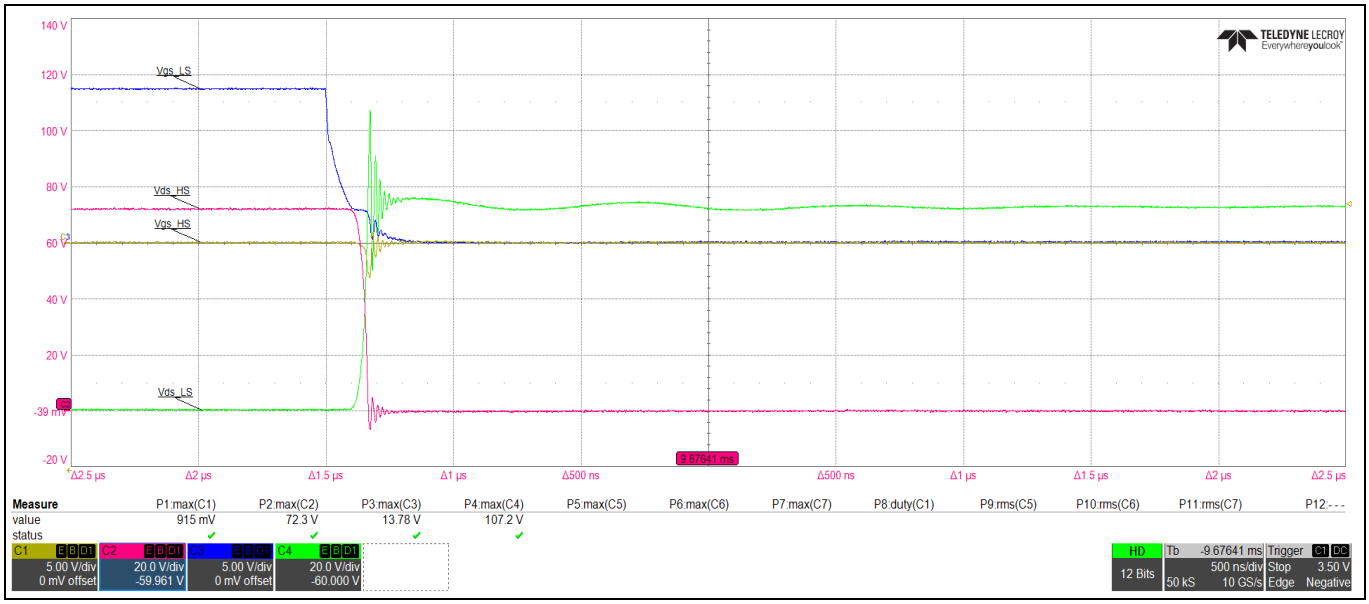


Figure 53 **High-side and low-side MOSFET gate-source and drain-source voltages for phase V during demagnetization period for phase V (500 ns/div) for OptiMOS™ 3 devices; V_{GS_HS} (yellow), V_{GS_LS} (blue), V_{DS_HS} (pink), V_{DS_LS} (green)**

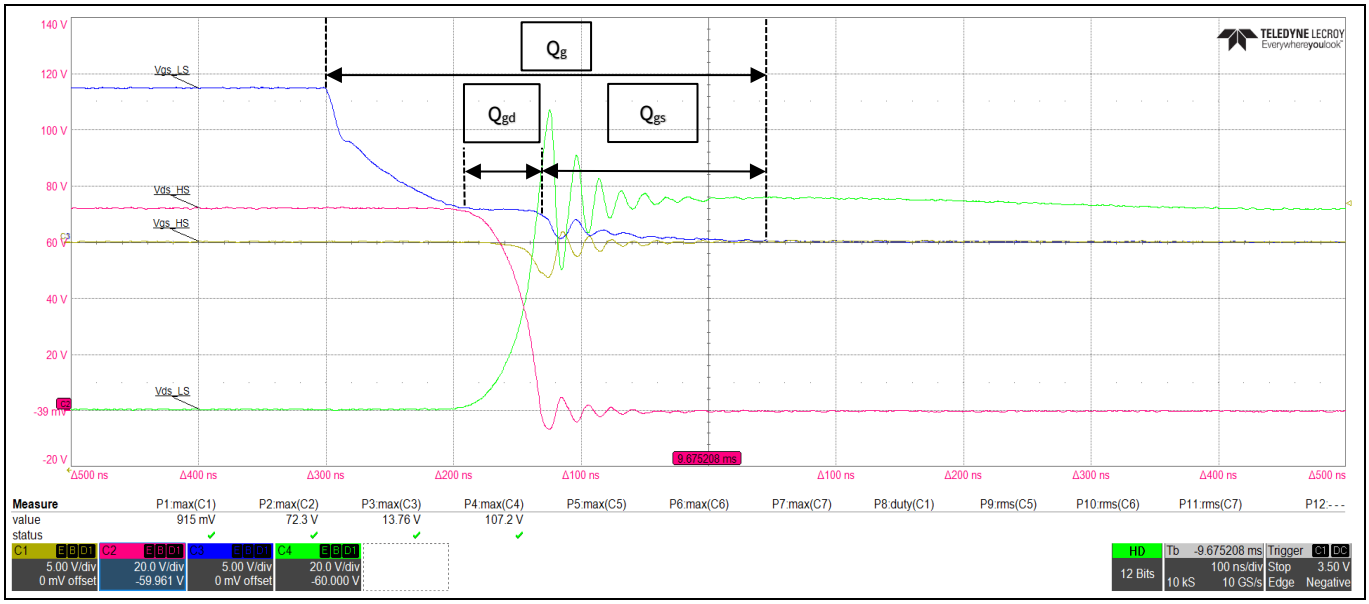


Figure 54 **High-side and low-side MOSFET gate-source and drain-source voltages for phase V during demagnetization period for phase V (100 ns/div) for OptiMOS™ devices; V_{GS_HS} (yellow), V_{GS_LS} (blue), V_{DS_HS} (pink), V_{DS_LS} (green)**

3.1.4 Power loss analysis

Figure 55 and **Figure 56** show the total power loss for the high-side MOSFET and low-side MOSFET at maximum load for OptiMOS™ 6 (IPT017N12NM6) and OptiMOS™ 3 (IPT030N12N3) devices at 72 V input voltage, respectively.

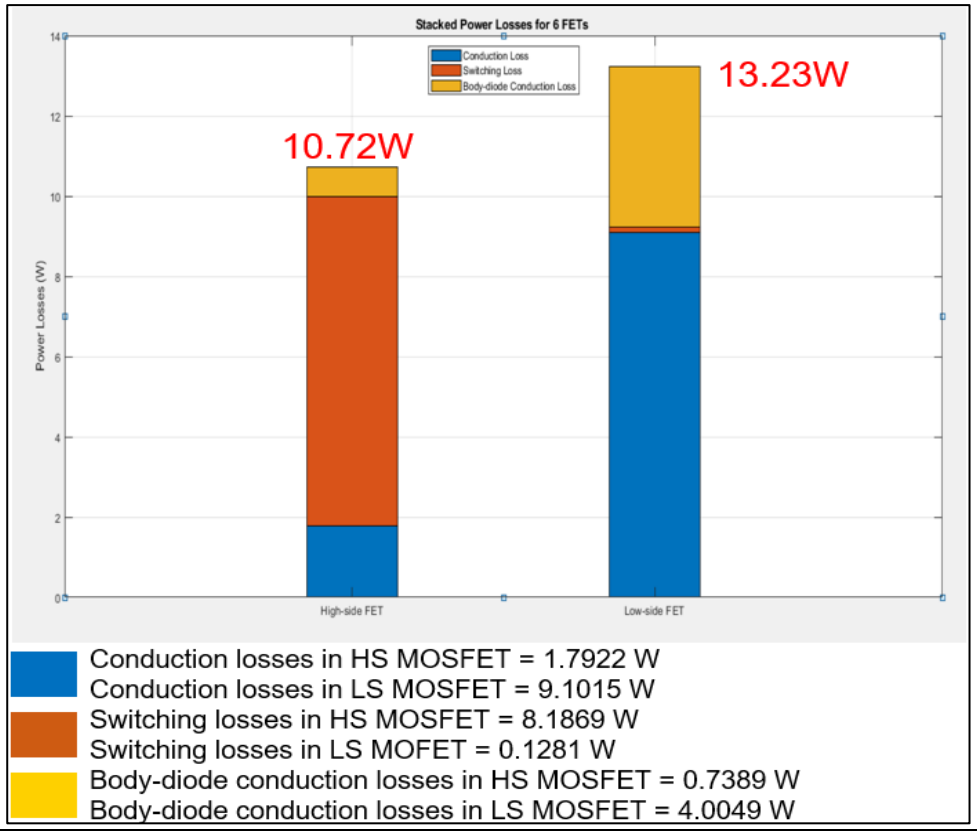


Figure 55 High-side and low-side MOSFET total power loss at maximum load for OptiMOS™ 6 devices

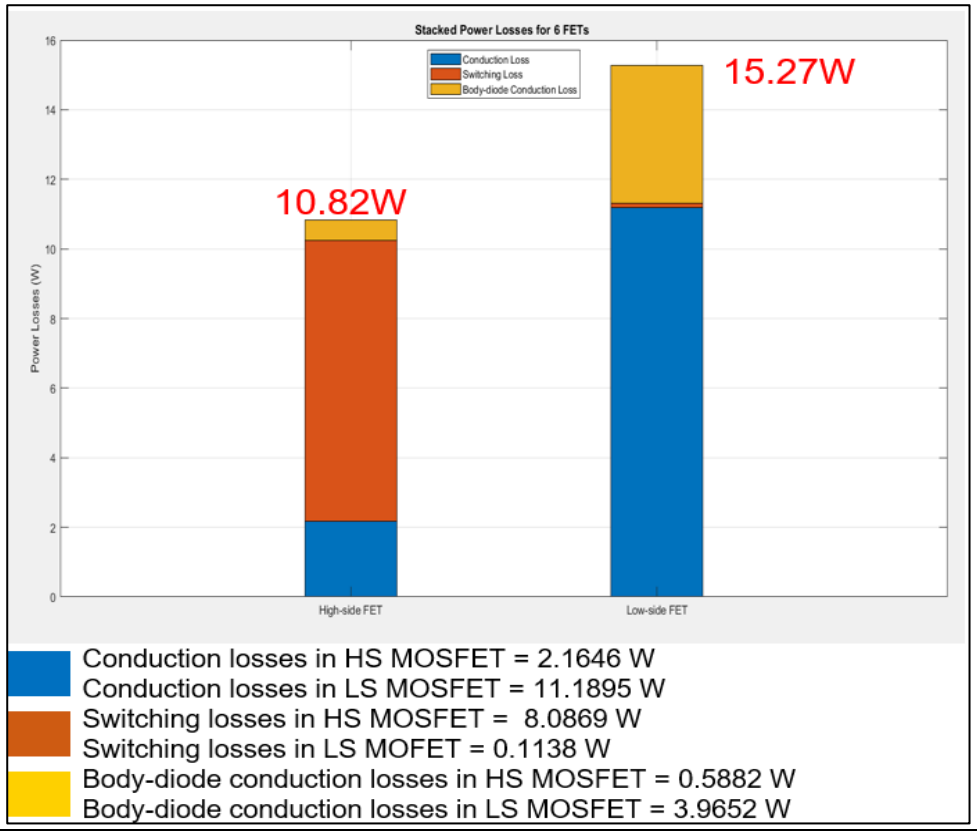


Figure 56 High-side and low-side MOSFET total power loss at maximum load for OptiMOS™ 3 devices

3.1.5 Power measurements

		Element 1	Element 2	Element 3	Element 4
Urms	[V]	71.87	21.58	21.21	21.50
Irms	[A]	14.60	37.77	37.54	38.61
P	[W]	986.23	315.89	316.54	324.07

Figure 57 Input and output measurements with an input power of 986 W at 72 V input voltage for OptiMOS™ 6 devices

		Element 1	Element 2	Element 3	Element 4
Urms	[V]	71.87	21.20	20.84	21.09
Irms	[A]	12.51	33.18	32.99	33.93
P	[W]	856.36	272.50	273.12	279.46

Figure 58 Input and output measurements with an input power of 856 W at 72 V input voltage for OptiMOS™ 3 devices

In **Figure 57** and **Figure 58**, results element 1 represents the DC input to the inverter. Elements 2, 3, and 4 are connected to the output phases U, V and W, respectively.

For OptiMOS™ 6, the total output power is equal to 315.89 W + 316.54 W + 324.07 W = 956.50 W for an input power of 986.23 W.

This gives an efficiency of 956.50/986.23 x 100 = 96.98 percent with losses of 29.73 W.

For OptiMOS™ 3, the total output power is equal to 272.50 W + 273.12 W + 279.46 W = 825.08 W for an input power of 856.36 W.

This gives an efficiency of 825.08/856.36 x 100 = 96.35 percent with losses of 31.28 W.

Additionally, by looking at **Figure 57** and **Figure 58**, OptiMOS™ 6 devices were able to handle 130 W more power than OptiMOS™ 3 devices in the three-phase BLDC motor-drive application before the MOSFET temperature reached 100°C.

3.1.6 Thermal measurement

Thermal images were taken after 12 minutes of operation to allow the components to rise and reach steady-state at an input power of 985 W and 850 W at 72 V input voltage for new OptiMOS™ 6 and BiC OptiMOS™ 3 devices, respectively, as shown in **Figure 59** and **Figure 60**. No forced air cooling was used.

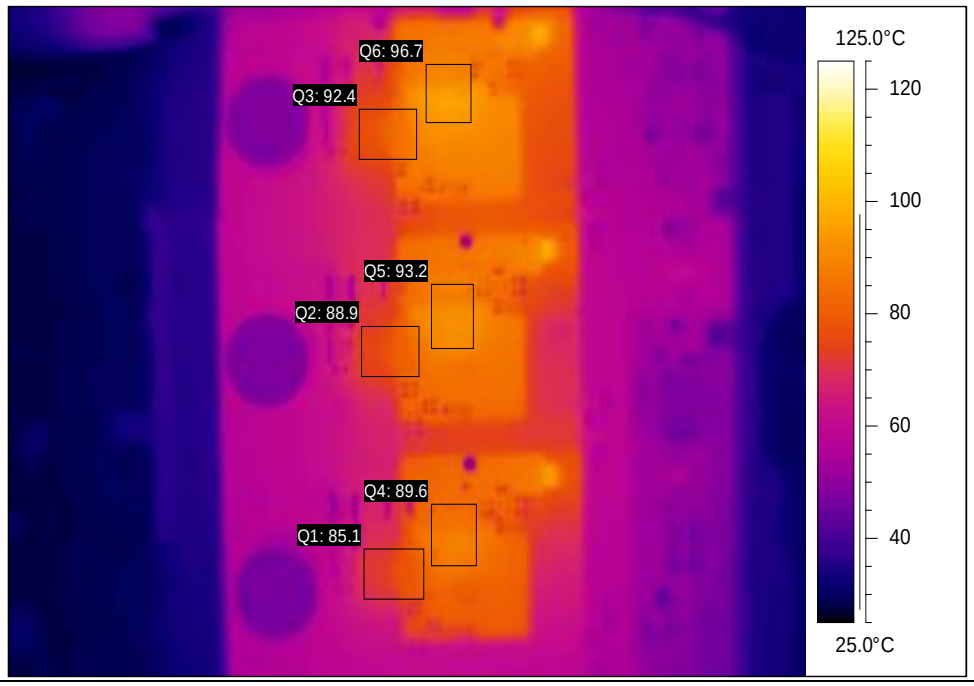


Figure 59 Thermal measurement at 72 V input and 956 W load for OptiMOS™ 6 devices

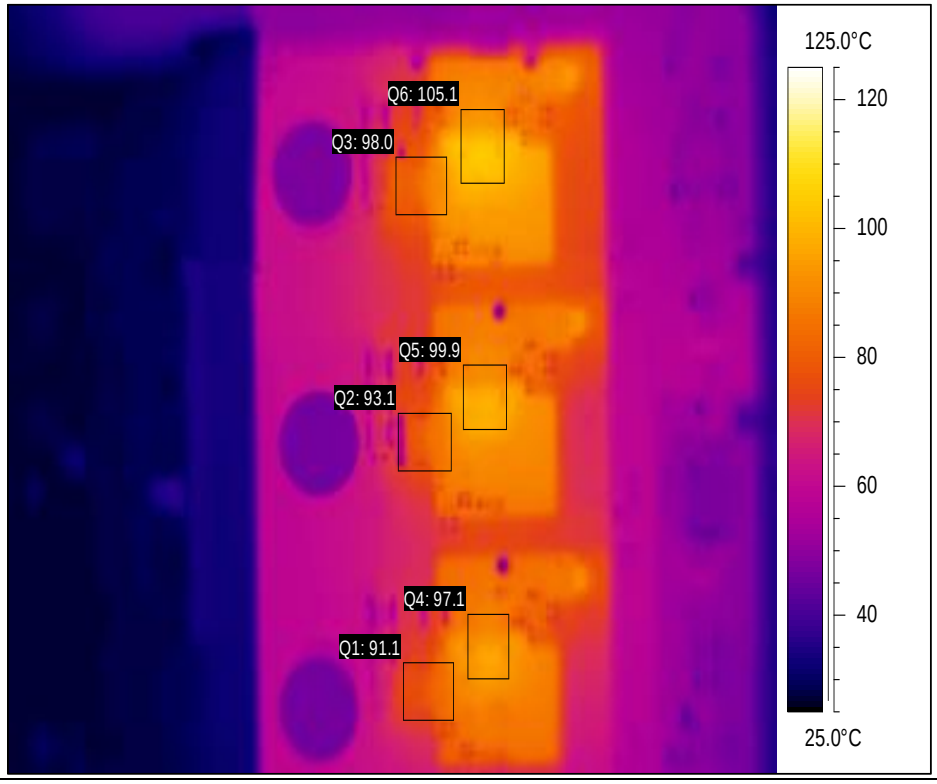


Figure 60 Thermal measurement at 72 V input and 825 W load for OptiMOS™ 3 devices

The temperature rise at 72 V input voltage for 985 W input power is 71.7 °C without heatsink for OptiMOS™ 6 devices.

3.2 High power test

Similar to section above, the experimental results are reported using new OptiMOS™ 6 120 V (IPT017N12NM6) MOSFETs in a three-phase BLDC motor-drive application at maximum rated power of the evaluation board (2 kW). For this test, RC snubber has been added for high-side and low-side MOSFETs for each phases of the three-phase motor-driver and a heatsink has also been added in order to be able to push higher power. In **Table 5**, applied test conditions for the specified application are highlighted. For this case, the operating waveforms for different transitions of the MOSFETs, power loss calculations, power measurements from the power analyzer, and thermal data are provided.

Table 9 Test conditions

Parameter	Value/description	Unit/type
Ambient temperature	25	°C
DC input voltage	72	V
Target output power	2000	W
Maximum motor speed	2000	RPM
Commutation method	Trapezoidal/Block commutation	
Rectification	Synchronous	
Switching frequency	10	kHz
Dead time	2	µs
Cooling	Air	
Test duration	12	Minutes

3.2.1 Test setup description

3.2.1.1 Evaluation board

The motor speed is set by adjusting POT1/R103 in the drive card. **Figure 61** shows the three-phase power board connected to an XMC1300 drive card.

The following order is recommended to power up the board:

1) Output phases are connected to the BLDC motor. The order of the phases is important, as the motor will not operate correctly if the phases are connected incorrectly. **Table 10** shows the connector for each of the phases.

Table 10 Motor phase connectors

Motor phase	Connector
Phase U	U
Phase V	V
Phase W	W

2) The three Hall sensors are connected directly to the XMC1300 drive card via connector X101. **Table 11** shows the pinout for the Hall sensor interface.

Table 11 Hall sensor interface (X101)

Pin	Description
1	GND
2	Phase U Hall sensor
3	Phase V Hall sensor
4	Phase W Hall sensor
5	V_{DD} (+5 V)

3) The XMC1300 drive card is connected to the power board through the power board connector.
4) If using onboard power supplies, pin 1 and pin 2 should be shorted via J2.
5) If using external power supplies, pin 2 and pin 3 should be shorted using J2 if using an external 12 V power supply, and R1 should be removed if using an external 5 V power supply.
6) The input power supply to the power board should be connected to J1 (+) and J4 (-).[5]

[5] It is recommended to use short cables for the input power supply to limit the ripple current passing through the input bulk capacitors.

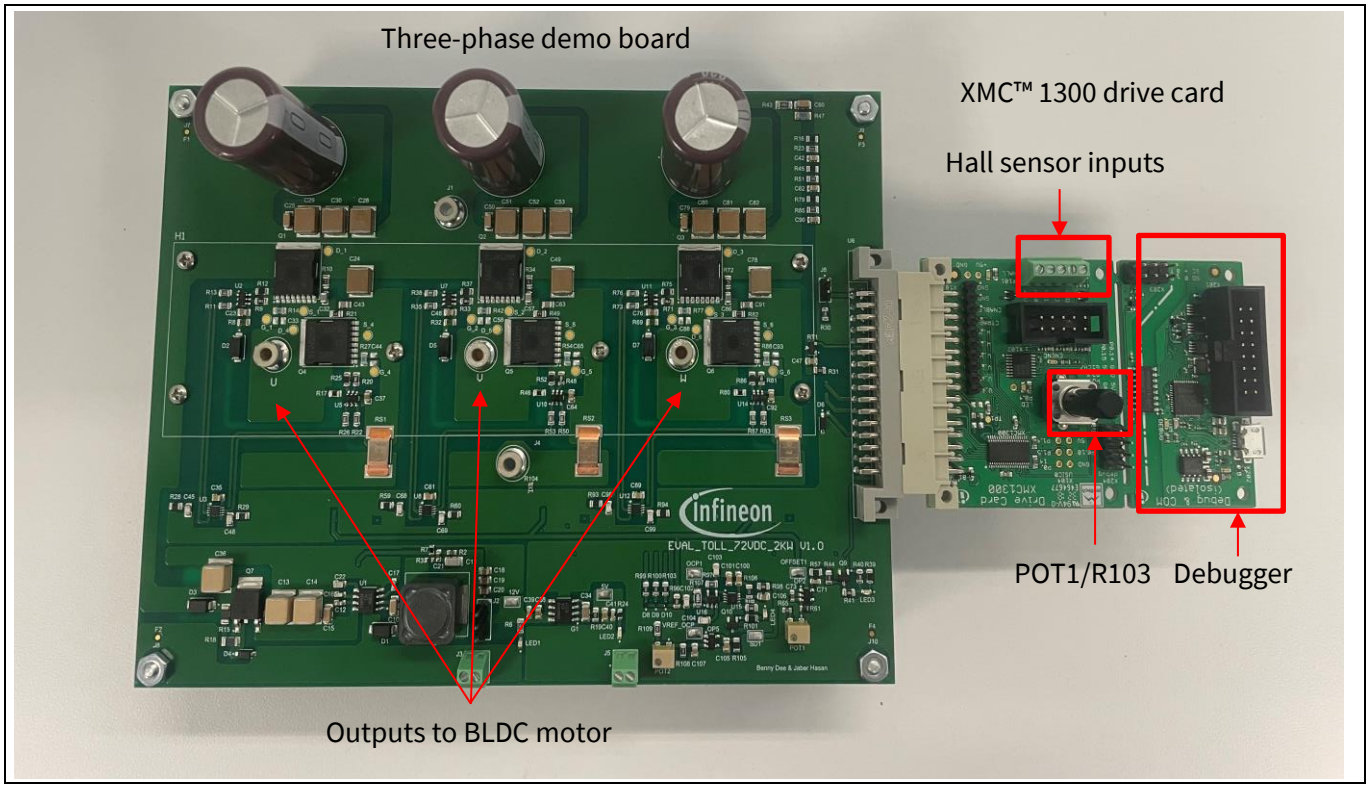


Figure 61 Three-phase power board connected to XMC1300 drive card

3.2.1.2 Description of the test setup

In this test setup, in order to load the motor, it was coupled with a dynamometer in order to be able to load the motor. The schematic of the test setup and actual test bench setup is shown in **Figure 62** and **Figure 63**, respectively. **Table 12** lists the test bench equipment used during testing of the evaluation board.

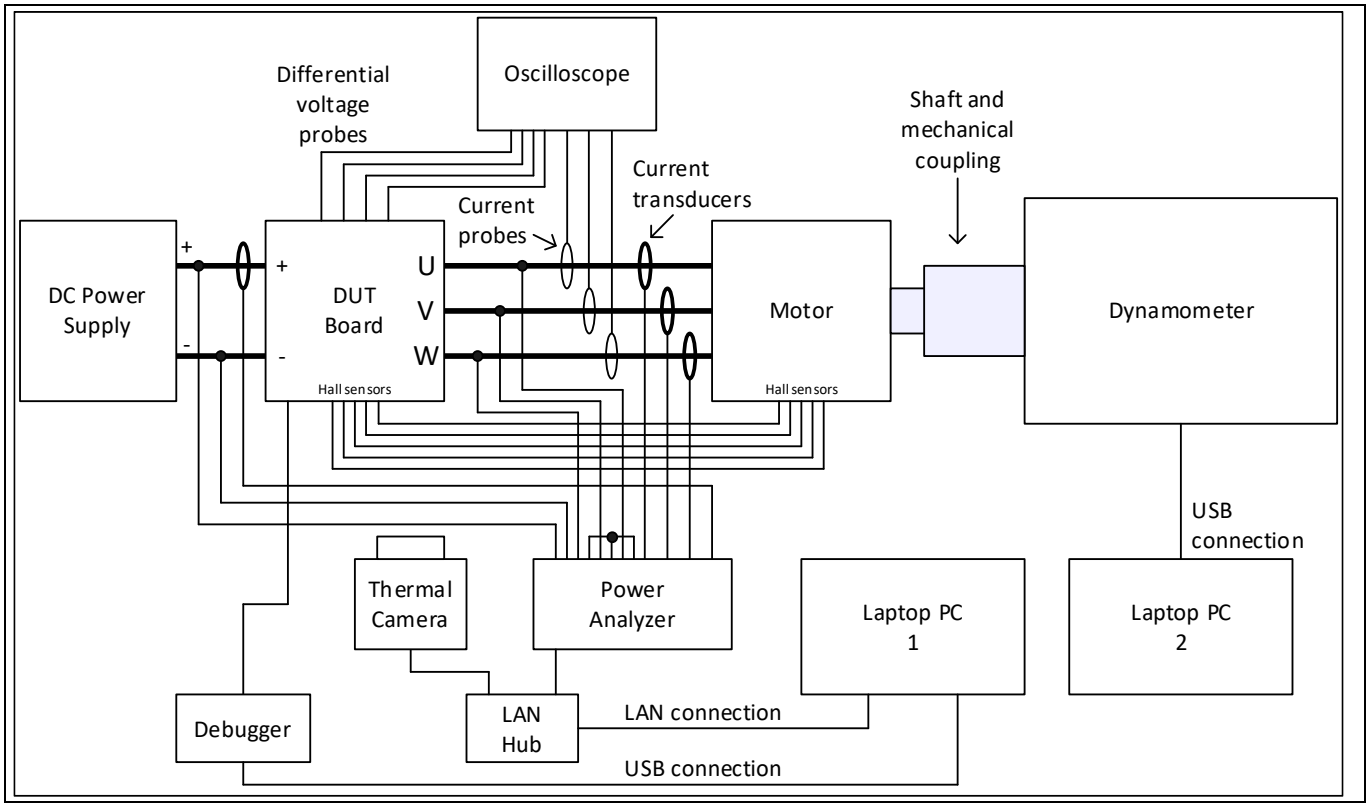


Figure 62 Schematic of the test setup

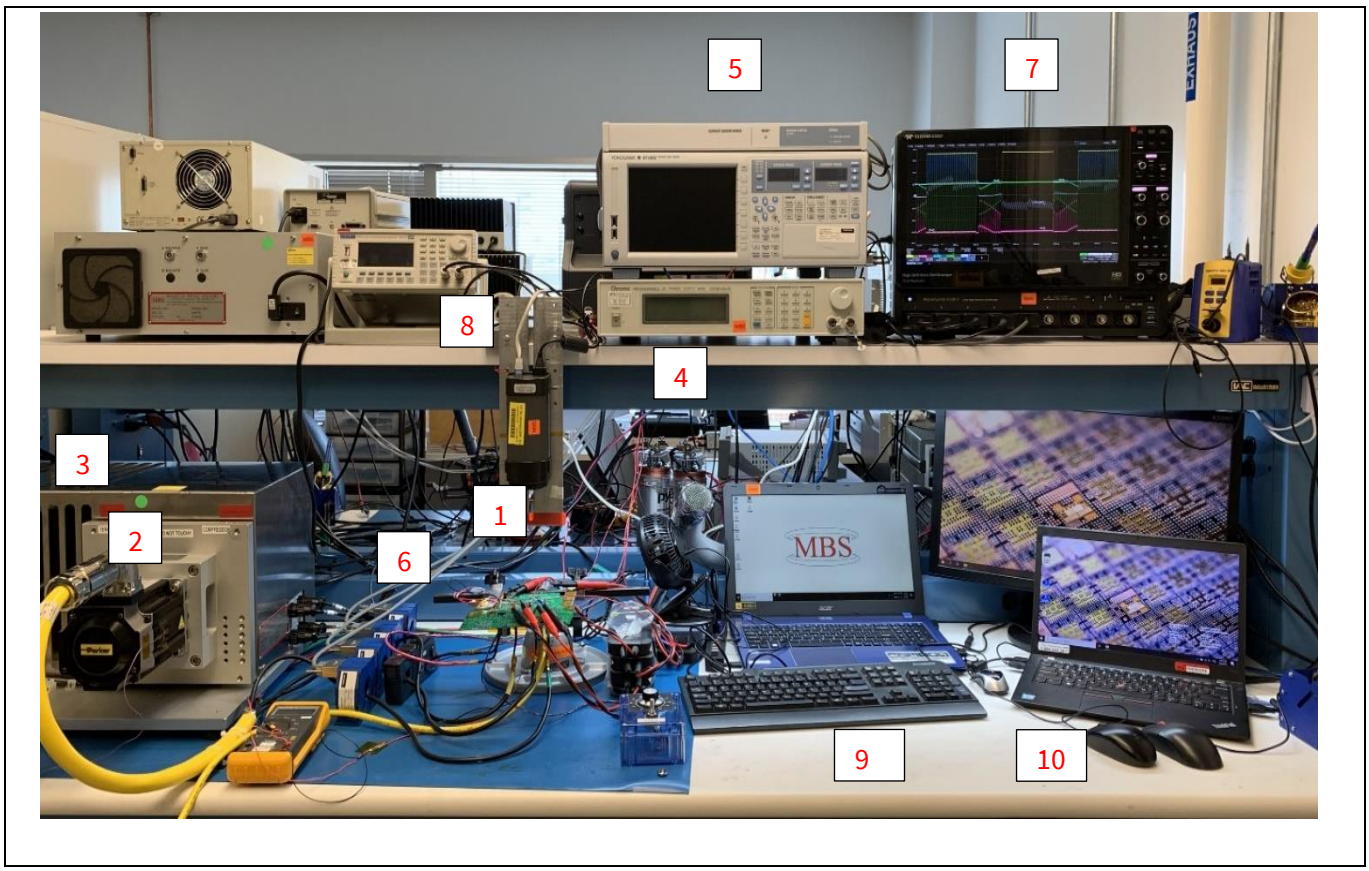


Figure 63 Test bench setup

Table 12 Test bench equipment

Test	Description
1	Board under test (DUT)
2	Motor
3	Dynamometer/Magnetic braking system
4	Power supply (100V, 100A)
5	Power analyzer (4 channel)
6	Current transducer (200A)
7	Oscilloscope (8 channel)
8	Thermal camera
9	Laptop PC (2)
10	Laptop PC (1)

3.2.2 Gate drive circuitry

Figure 64 shows the external gate resistor used for turn-on and turn-off and RC snubbers used across drain-source for the high-side and low-side MOSFETs for this three-phase high power motor-drive application. The external gate resistors and RC snubbers were adjusted to prevent high-side MOSFET drain-source voltage from avalanching and false turn-on of the low-side MOSFET at maximum load. The external gate turn-on and turn-off resistor is adjusted to 47 Ω and 3.3 Ω, respectively, for OptiMOS™ 6 devices. Similarly, a resistor value of 1.2 Ω and 10 nF was used as RC snubber across drain-source of both high-side and low-side MOSFETs – leading to dv/dt slew rate lower than 3 V/ns. Additionally, in order to prevent false turn-on of the low-side MOSFET, a 3.3 nF capacitor across gate-source is placed on the low-side MOSFET in order to satisfy $\frac{Q_{gd}}{Q_{gs(th)}} < 1$.

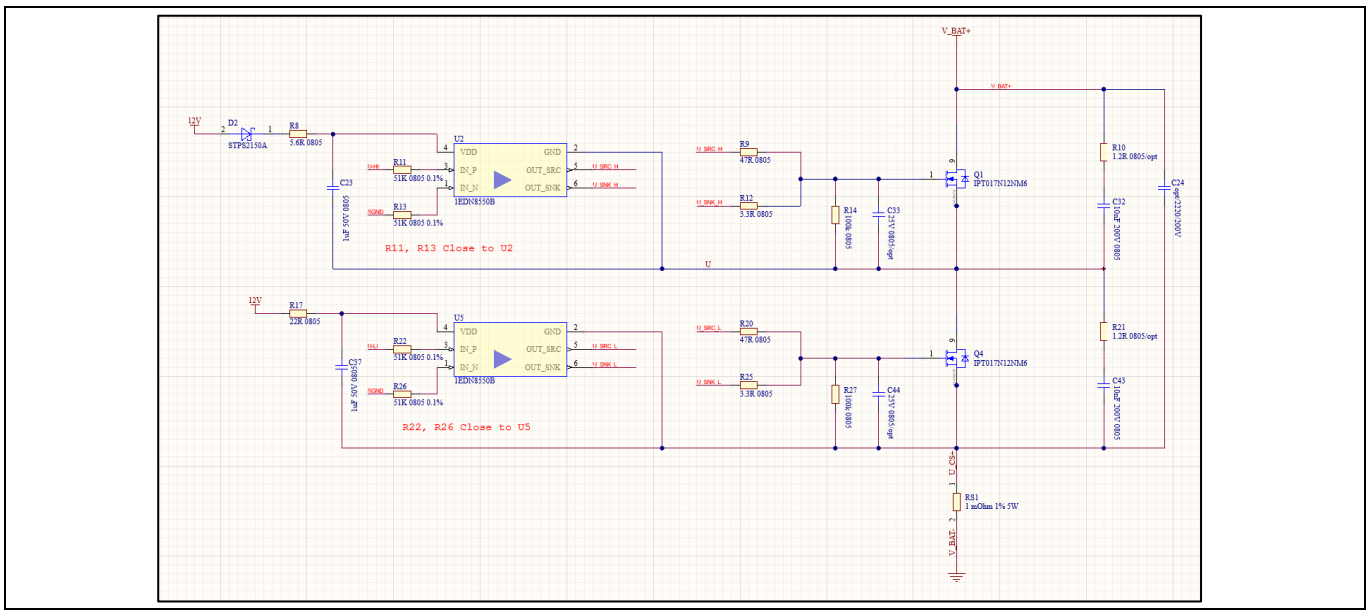


Figure 64 Single phase leg of three-phase inverter

3.2.3 Operating waveforms

Figure 65 and **Figure 66** show gate-source and drain-source voltages of both high-side and low-side MOSFETs for phase V, and also the phase V current using the synchronous rectification trapezoidal control method at 2000 RPM with an input power of 2000 W for OptiMOS™ 6 (IPT017N12NM6) devices at 72 V input voltage for 1 ms/div and 500 µs/div.

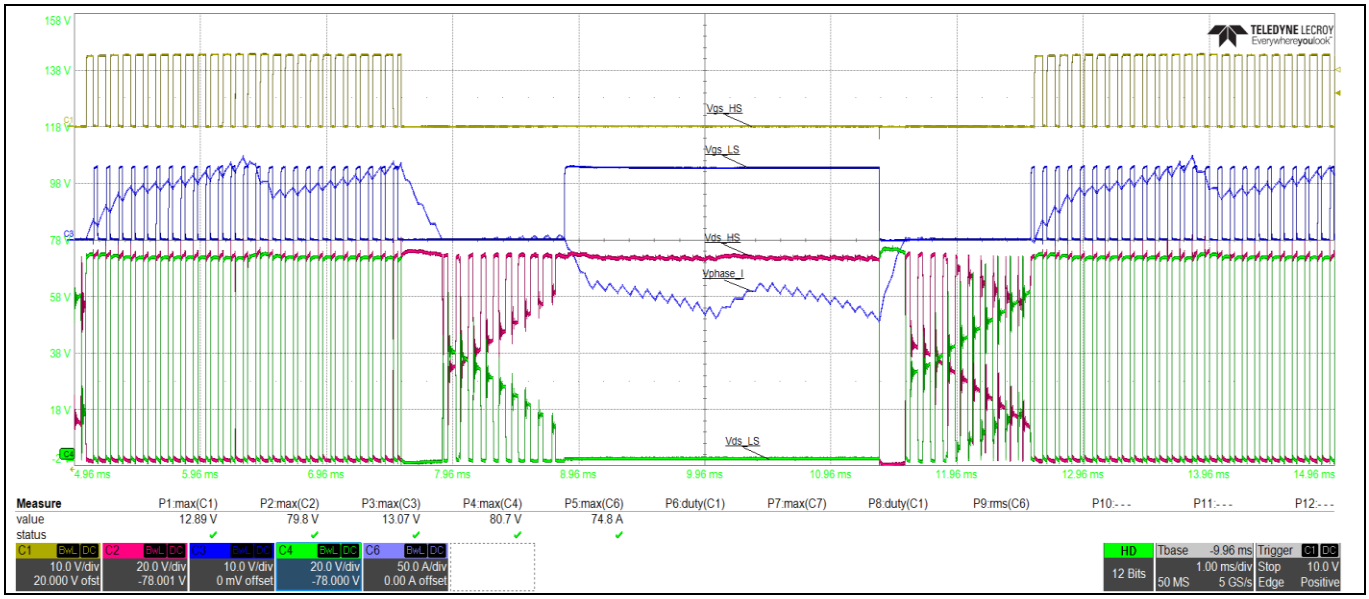


Figure 65 High-side and low-side MOSFET gate-source and drain-source voltages for phase V (500 µs/div) for OptiMOS™ 6 devices; V_{GS_HS} (yellow), V_{GS_LS} (blue), V_{DS_HS} (pink), V_{DS_LS} (green), I_{PHASE_V} (blue)

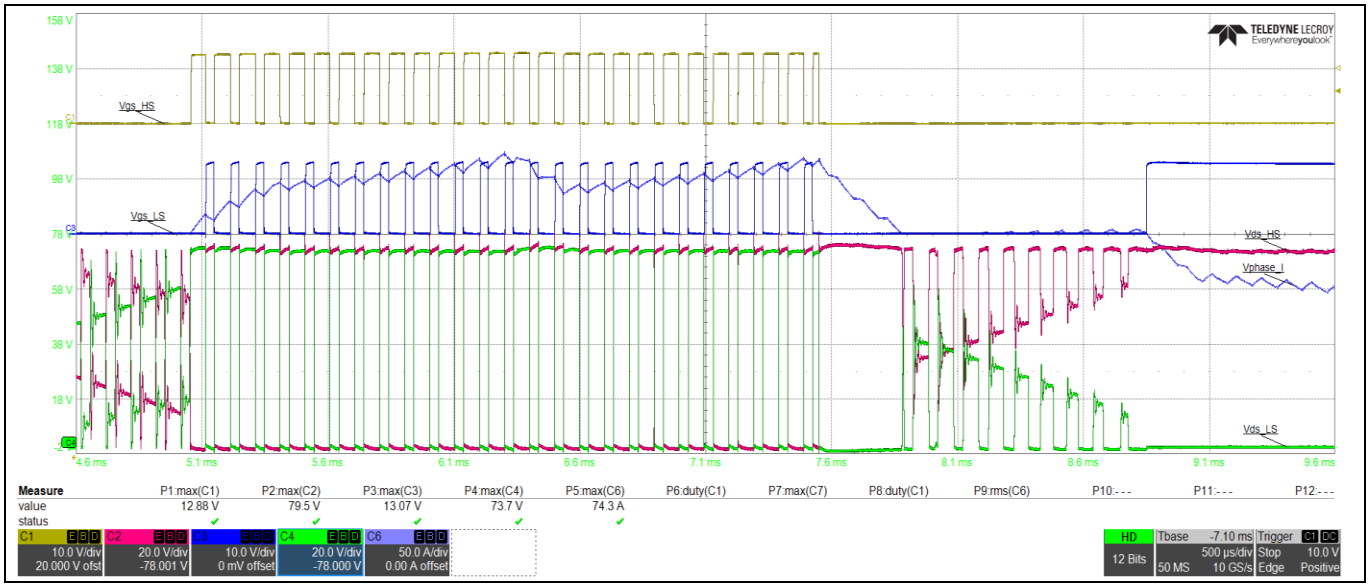


Figure 66 High-side and low-side MOSFET gate-source and drain-source voltages for phase V (500 µs/div) for OptiMOS™ 6 devices; V_{GS_HS} (yellow), V_{GS_LS} (blue), V_{DS_HS} (pink), V_{DS_LS} (green), I_{PHASE_V} (blue)

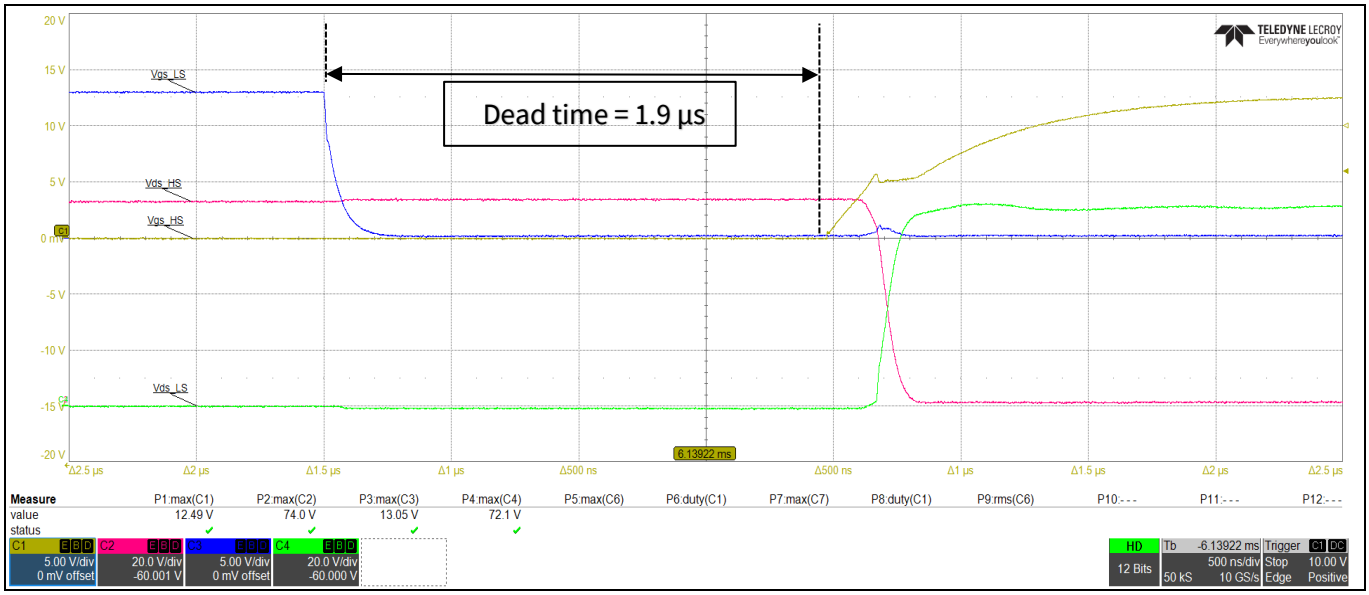


Figure 67 **High-side and low-side MOSFET gate-source and drain-source voltages for phase V for high-side MOSFET turn-on and low-side MOSFET turn-off (500 ns/div) for OptiMOS™ 6 devices; V_{GS_HS} (yellow), V_{GS_LS} (blue), V_{DS_HS} (pink), V_{DS_LS} (green)**

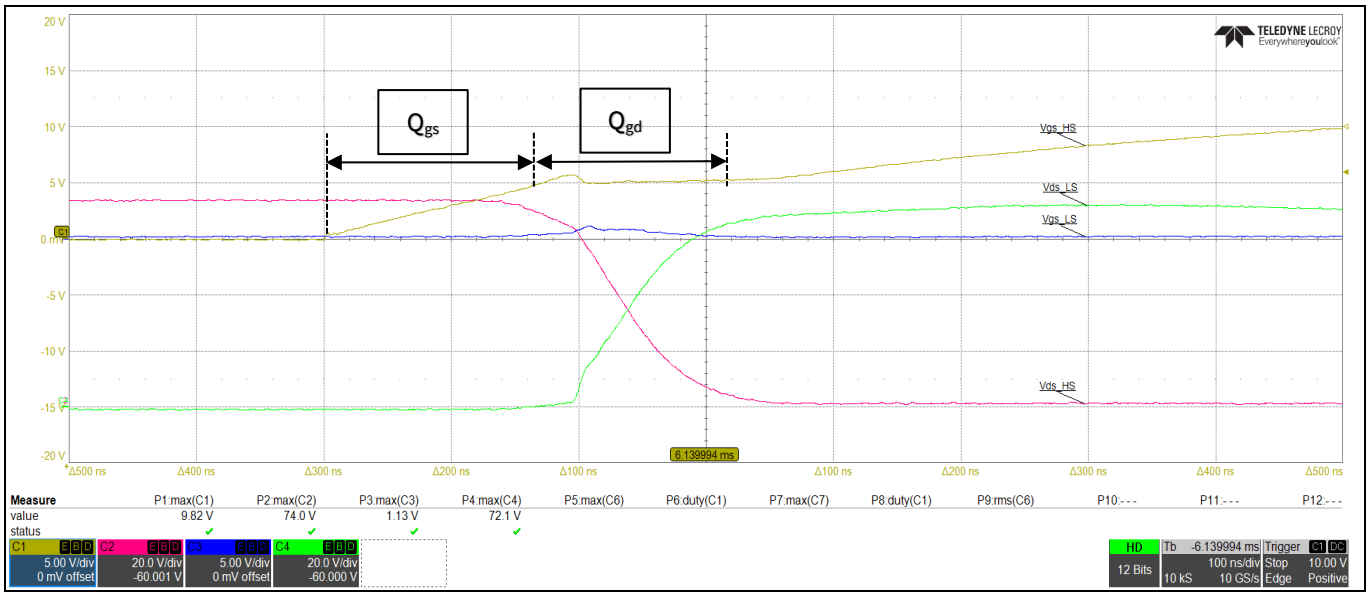


Figure 68 **High-side and low-side MOSFET gate-source and drain-source voltages for phase V for high-side MOSFET turn-on and low-side MOSFET turn-off (100 ns/div) for OptiMOS™ 6 devices; V_{GS_HS} (yellow), V_{GS_LS} (blue), V_{DS_HS} (pink), V_{DS_LS} (green)**

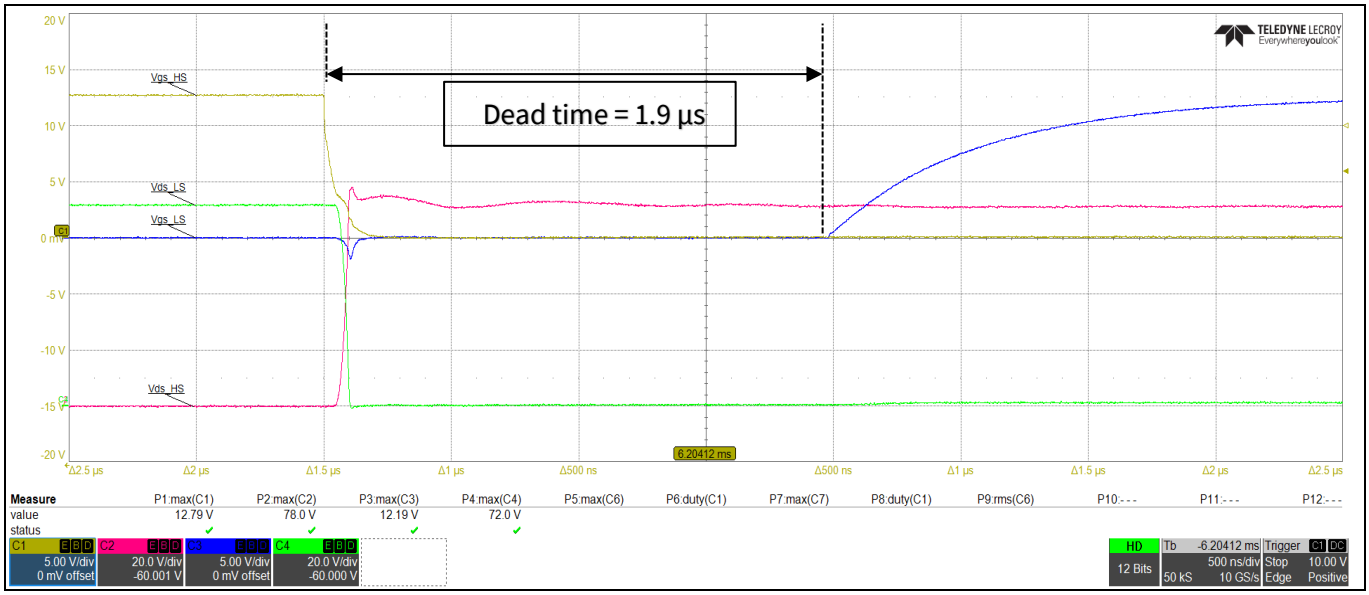


Figure 69 **High-side and low-side MOSFET gate-source and drain-source voltages for phase V for high-side MOSFET turn-off and low-side MOSFET turn-on (500 ns/div) for OptiMOS™ 6 devices; V_{GS_HS} (yellow), V_{GS_LS} (blue), V_{DS_HS} (pink), V_{DS_LS} (green)**

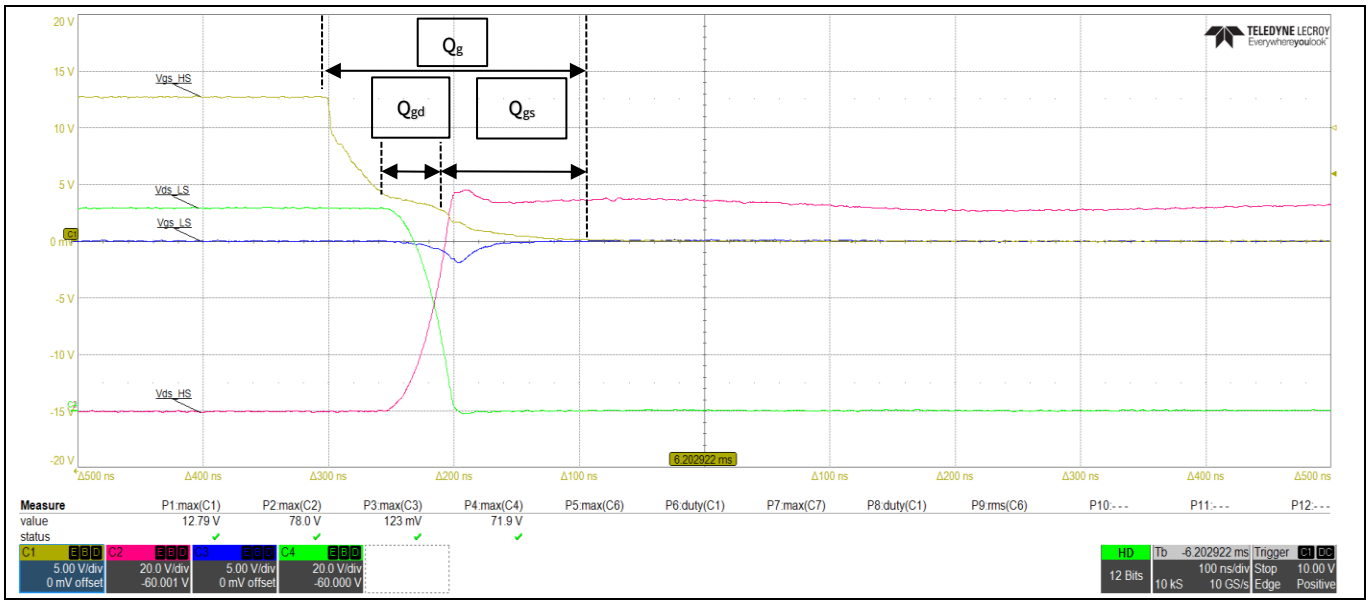


Figure 70 **High-side and low-side MOSFET gate-source and drain-source voltages for phase V for high-side MOSFET turn-off and low-side MOSFET turn-on (100 ns/div) for OptiMOS™ 6 devices; V_{GS_HS} (yellow), V_{GS_LS} (blue), V_{DS_HS} (pink), V_{DS_LS} (green)**

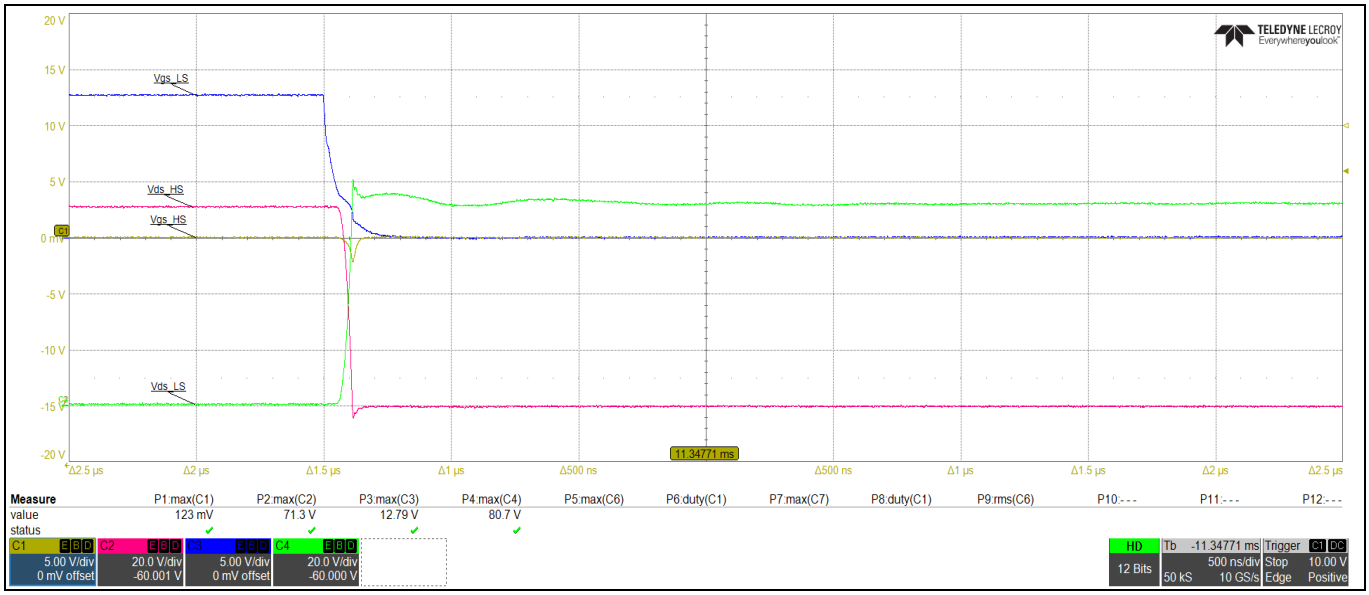


Figure 71 **High-side and low-side MOSFET gate-source and drain-source voltages for phase V during demagnetization period for phase V (500 ns/div) for OptiMOS™ 6 devices; V_{GS_HS} (yellow), V_{GS_LS} (blue), V_{DS_HS} (pink), V_{DS_LS} (green)**

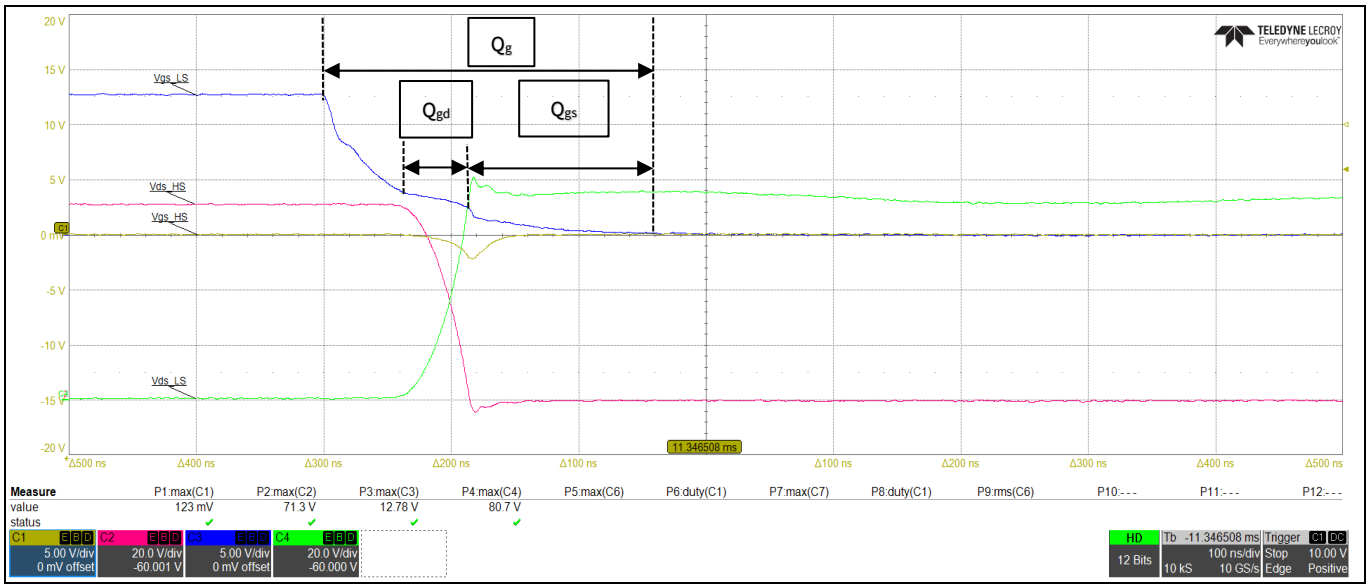


Figure 72 **High-side and low-side MOSFET gate-source and drain-source voltages for phase V during demagnetization period for phase V (100 ns/div) for OptiMOS™ 6 devices; V_{GS_HS} (yellow), V_{GS_LS} (blue), V_{DS_HS} (pink), V_{DS_LS} (green)**

3.2.4 Power loss analysis

Figure 73 show the total power loss for the high-side and low-side MOSFETs at maximum load of 1.96 kW for OptiMOS™ 6 (IPT017N12NM6) devices at 72 V input voltage.

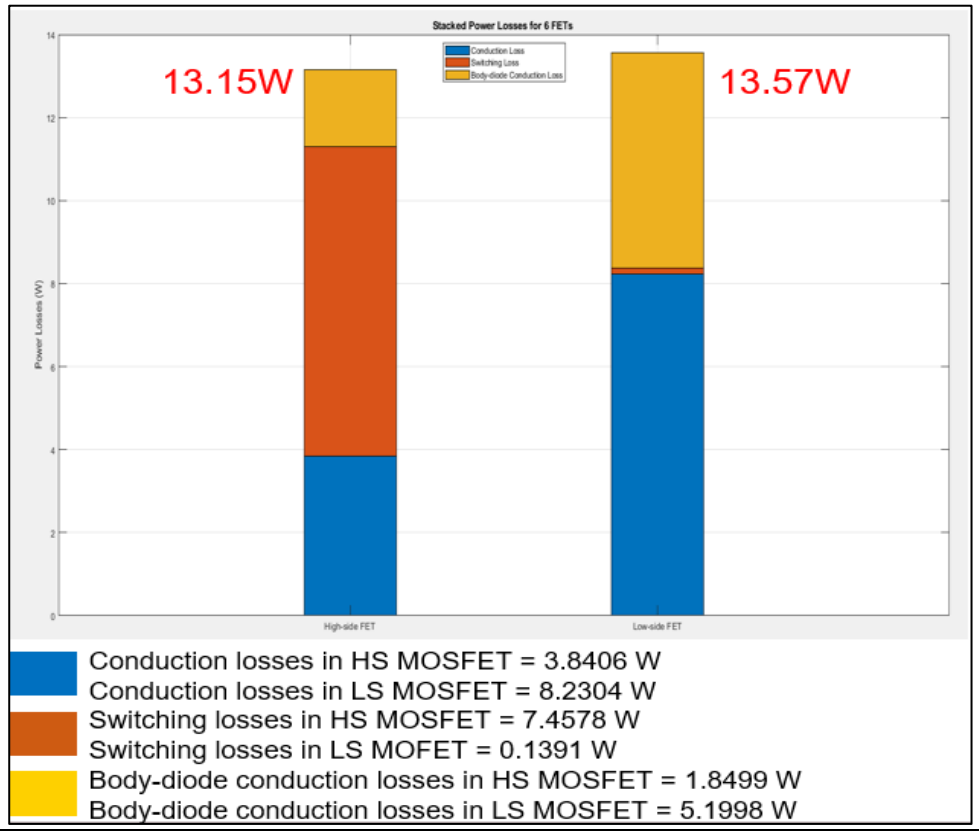


Figure 73 High-side and low-side MOSFET total power loss at maximum load of 1.96 kW for OptiMOS™ 6 devices

3.2.5 Power measurements

		Element 1	Element 2	Element 3	Element 4
Urms	[V]	71.71	28.32	27.77	28.07
Irms	[A]	27.85	41.64	41.52	41.76
P	[W]	1994.20	655.43	653.83	652.46

Figure 74 Input and output measurements with an input power of 2 kW at 72 V input voltage for OptiMOS™ 6 devices

In **Figure 74**, results element 1 represents the DC input to the inverter. Elements 2, 3, and 4 are connected to the output phases U, V and W, respectively.

For th new OptiMOS™ 6, the total output power is equal to 655.43 W + 653.83 W + 652.46 W = 1961.72 W for an input power of 1994.20 W.

This gives an efficiency of 1961.72/1994.20 x 100 = 98.37 percent with losses of 32.48 W.

3.2.6 Thermal measurement

Thermal images were taken after 12 minutes of operation to allow the components to rise and reach steady-state at an input power of 2 kW at 72 V input voltage for new OptiMOS™ 6 devices, as shown in **Figure 75**. No forced air cooling was used.

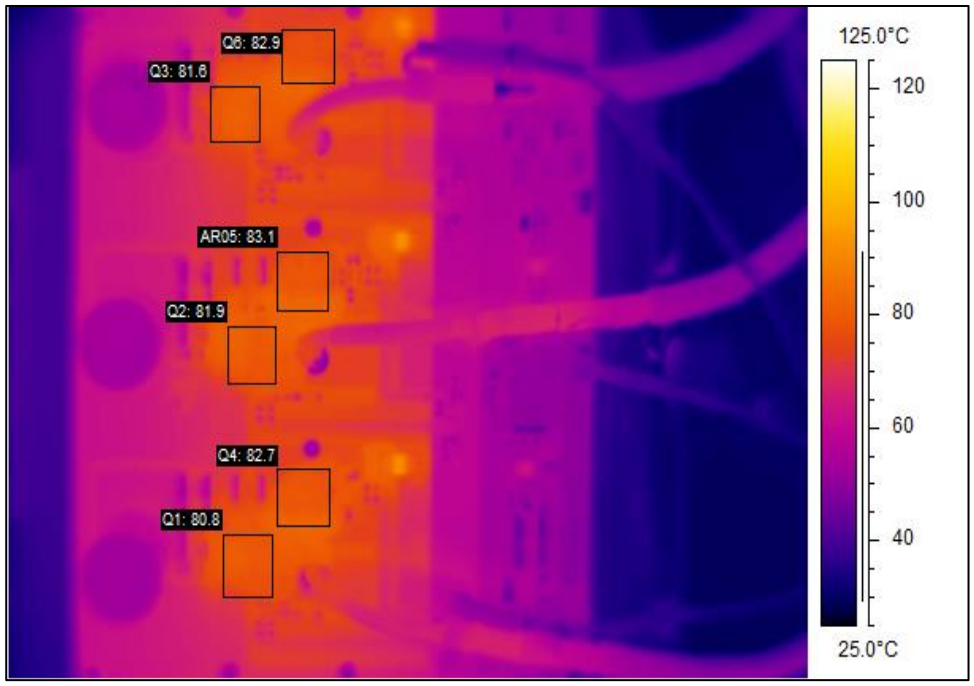


Figure 75 Thermal measurement at 72 V input and 1960 W load for OptiMOS™ 6 devices

The temperature rise at 72 V input voltage for 2 kW input power is only 58.1 °C with heatsink for the new OptiMOS™ 6 devices.

3.3 Schematic and PCB layout

3.3.1 Schematic

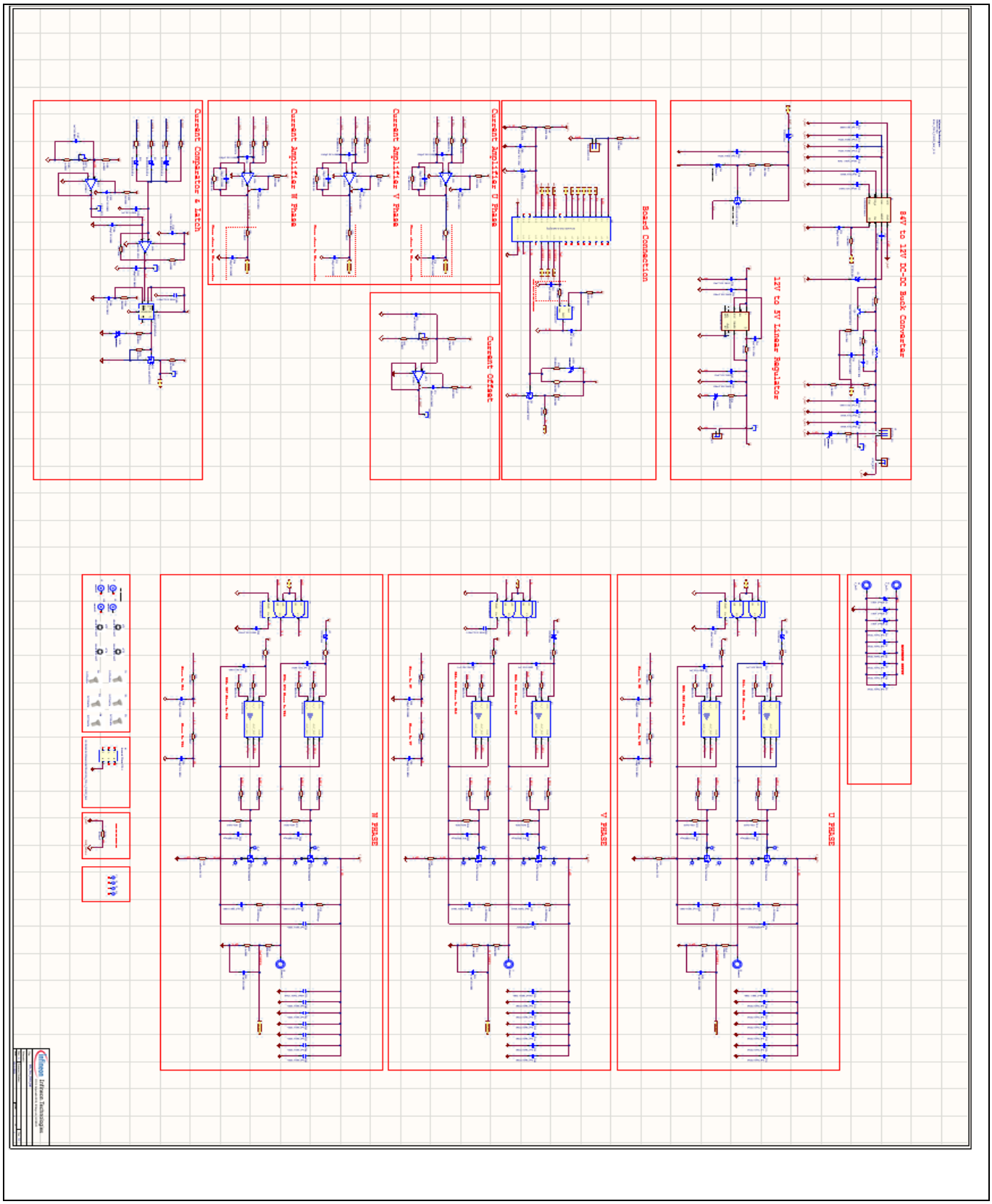


Figure 76 EVAL_TOLL_72VDC_2kW schematic

3.3.2 PCB Layout

The EVAL_TOLL_72VDC_2kW board consists of six copper PCB layers. All the layers have 2 oz. copper and the board size is 172 mm x 129.77 mm. The board material is FR4 grade with 1.6 mm thickness. The Gerber files are available from the downloads section of the **Infineon website**. A login is required to download this material.

The top layer, mid 1 layer, mid 2 layer, mid 3 layer, mid 4 layer, and bottom layer PCB layouts are shown in **Figure 77** to **Figure 82**.

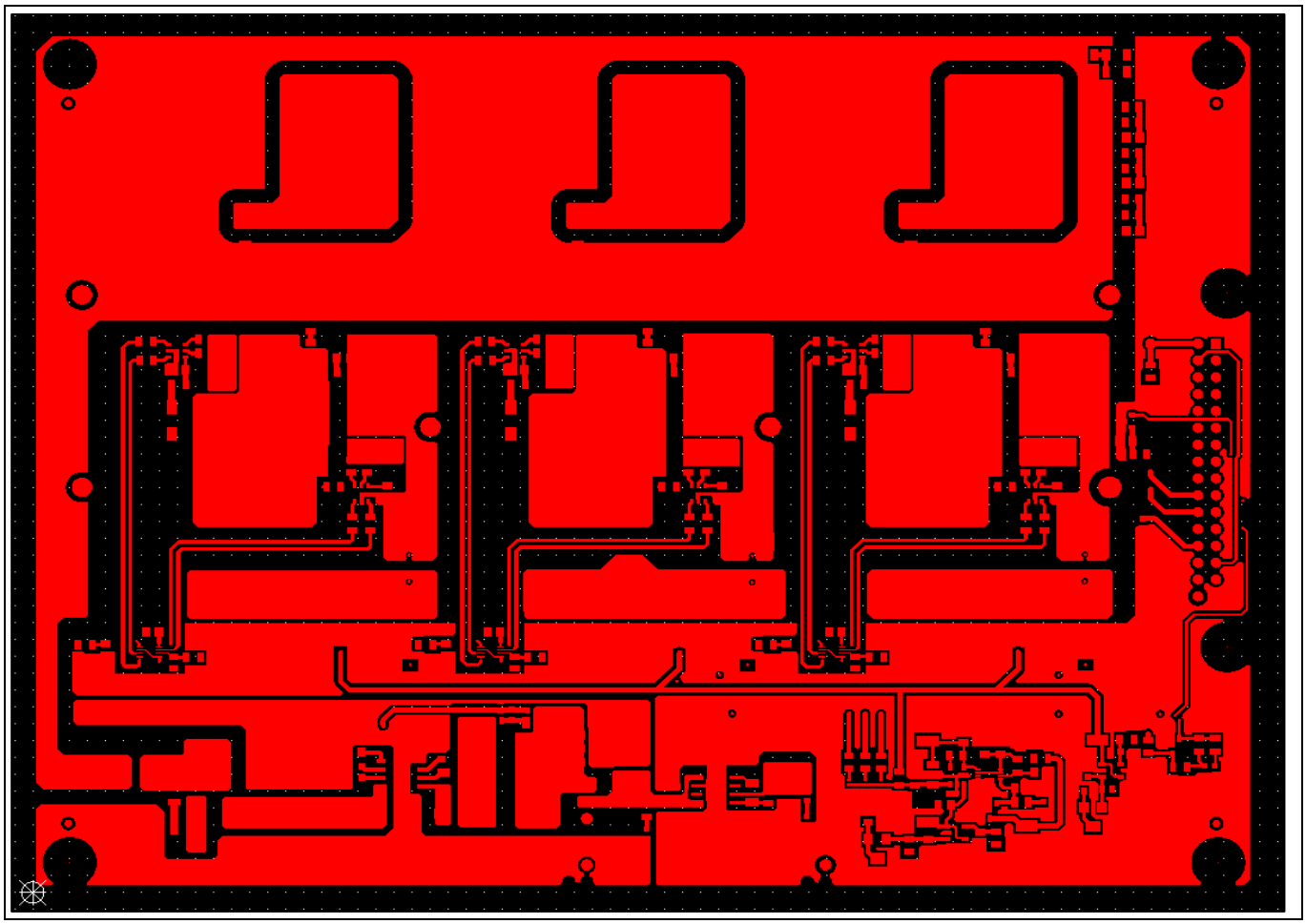


Figure 77 Top layer

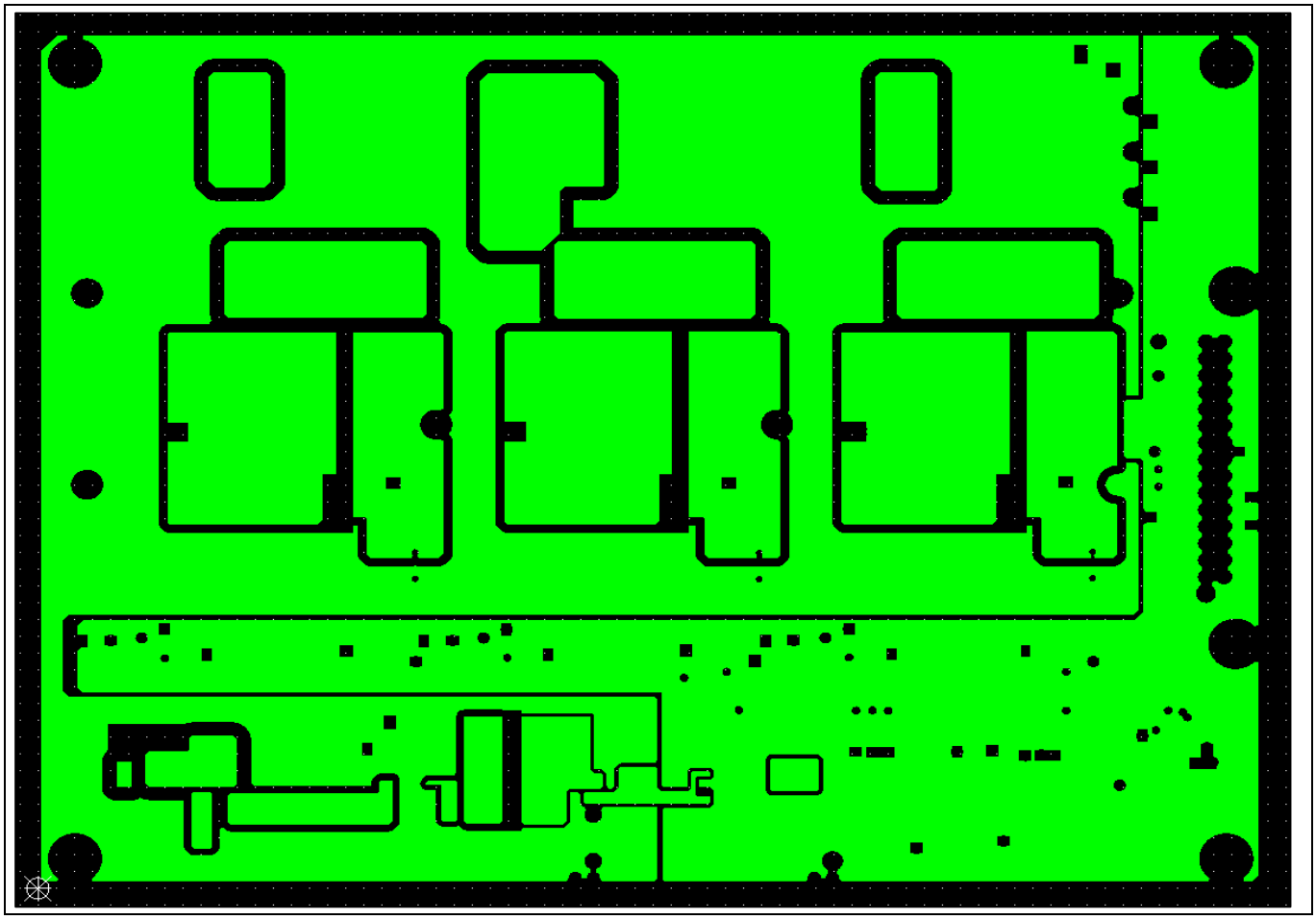


Figure 78 Mid 1 layer

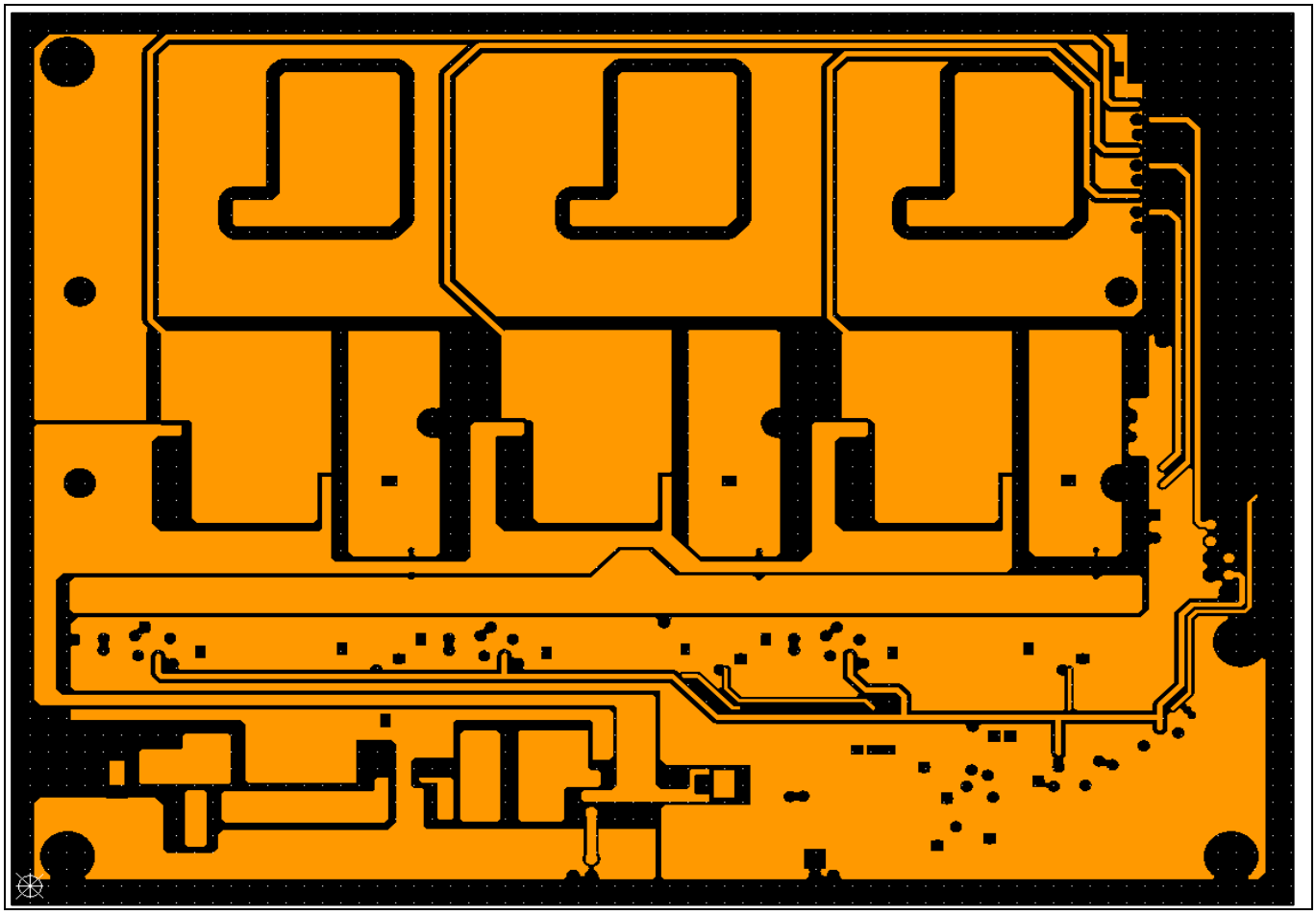


Figure 79 Mid 2 layer

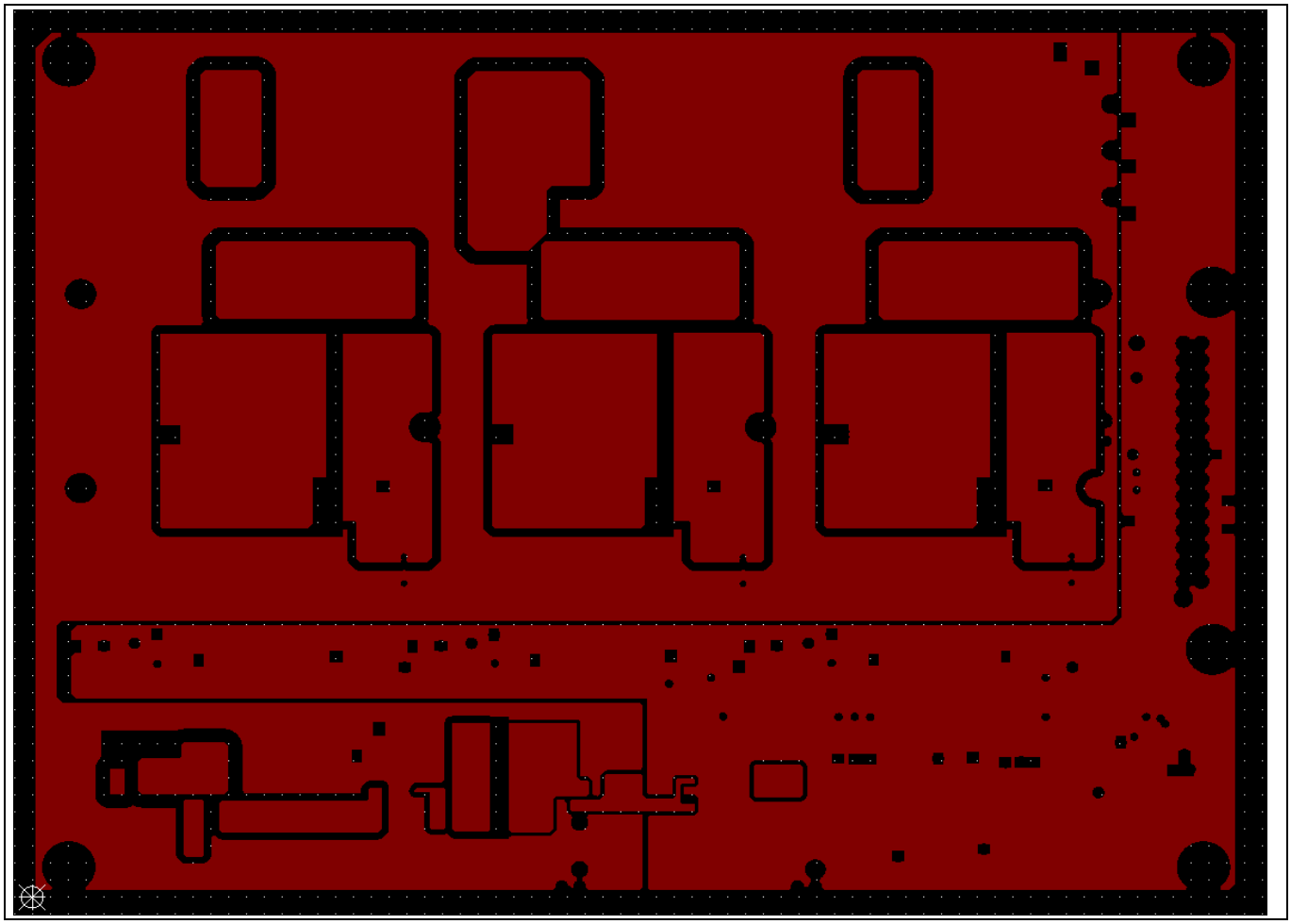


Figure 80 Mid 3 layer

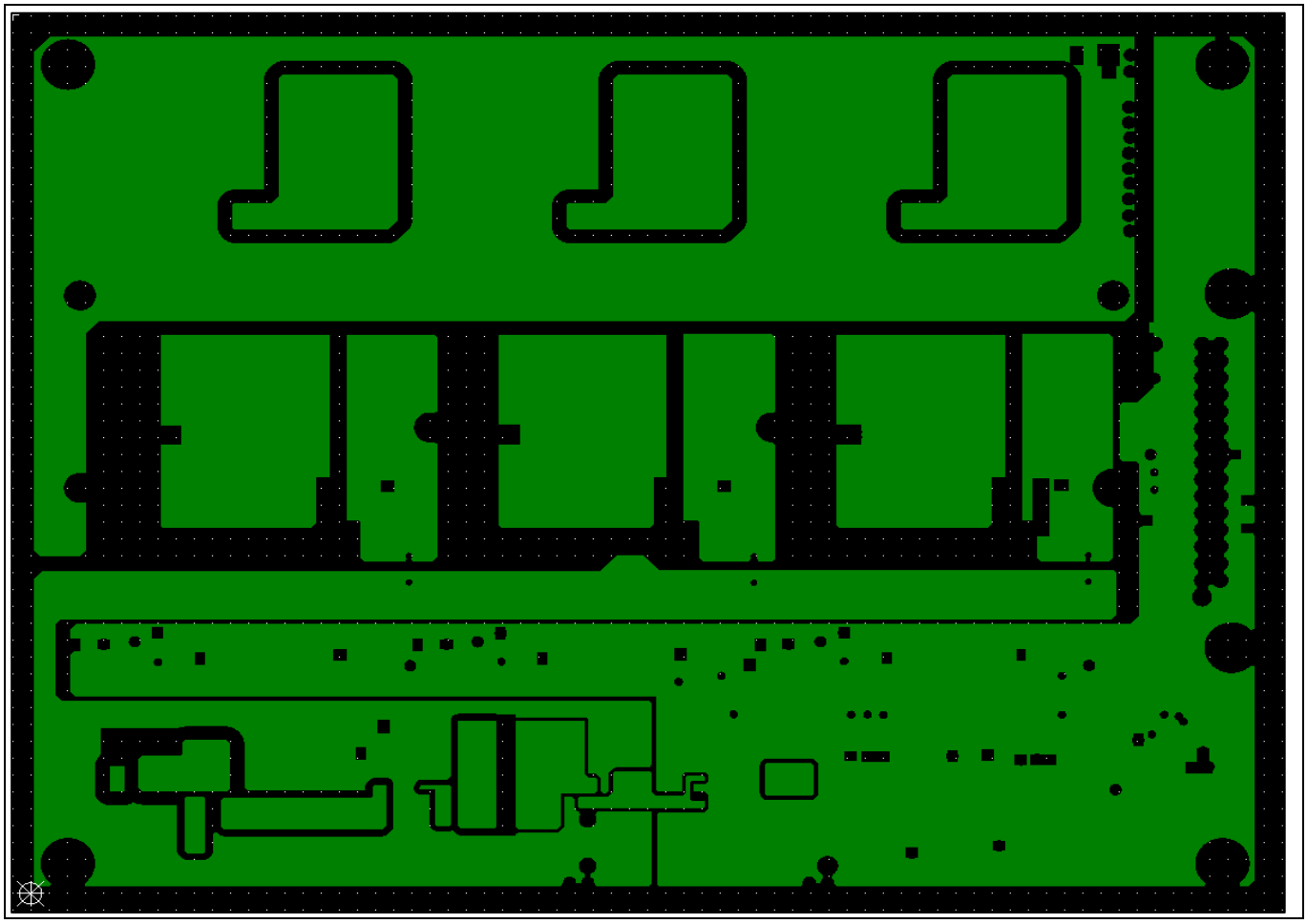


Figure 81 Mid 4 layer

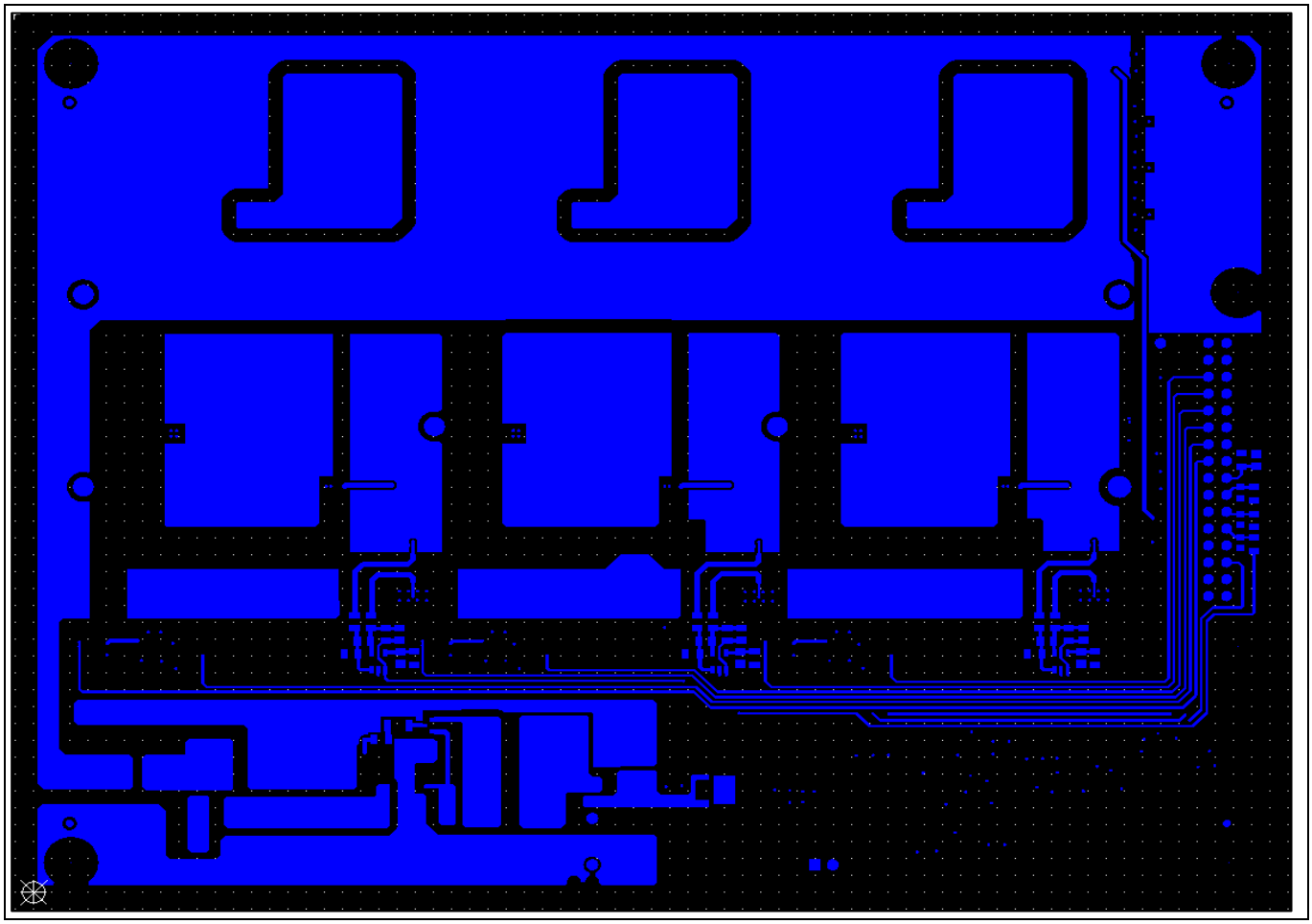


Figure 82 Bottom layer

3.4 Bill of materials

The complete BOM is available from the downloads section of the **Infineon website**. A login is required to download this material.

Table 13 BOM of the evaluation board EVAL_TOLL_72VDC_2kW

Item	Part references	Quantity	Type	Value/Rating/ Tolerance/ Package/Other	Manufacturer	Part number
1	C1, C2, C3	3	Capacitor	820 µF, 100 V, 20%, radial	United Chemi-Con	EKZE101ELL821MM40S
2	C4, C5, C6, C7, C8, C9, C24, C26, C27, C28, C29, C30, C31, C49, C51, C52, C53, C54, C55, C56, C78, C80, C81, C82, C83, C84, C85	27	Capacitor	2 µF, 200 V, 20%, 2220, X7R	Kemet	C2220X205K2RLCAUTO
3	C10, C15, C25, C50, C79	5	Capacitor	100 nF, 200 V, 10%, 1206, X7R	Yageo	CC1206KKX7RABB104
4	C11	1	Capacitor	4.7 nF, 200 V, 10%, 1206, X7R	Kemet	C1206C472K2RAC7800
5	C12	1	Capacitor	0.1 µF, 50 V, 10%, 0603, X7R	Samsung Electro-Mechanics	CL10B104KB8WPND
6	C13, C14, C36	3	Capacitor	2.2 µF, 200 V, 10%, 2220, X7R	Knowles Syfer	2220Y2000225KXTWS2
7	C16	1	Capacitor	10 pF, 50 V, 5%, 0603, X7R	Kemet	C0603C100J5RACTU
8	C17	1	Capacitor	100 pF, 50 V, 10%, 0603, X7R	Kemet	C0603C101K5RAC7867
9	C18	1	Capacitor	4.7 µF, 25 V, 10%, 0805, X5R	Kemet	C0805C475K3PAC7800
10	C19, C20	2	Capacitor	22 µF, 25 V, 20%, 0805, X5R	Murata Electronics	GRT21BR61E226ME13L
11	C21	1	Capacitor	220 nF, 25 V, 10%, 0603, X7R	Yageo	AC0603KRX7R8BB224
12	C22	1	Capacitor	680 pF, 25 V, 10%, 0805, X7R	Kyocera AVX	08053C681KAT2A

13	C23, C48, C76	3	Capacitor	1 µF, 50 V, 10%, 0805, X7R	Kemet	C0805C105K5RAC7800
14	C32, C43, C57, C63, C86, C91	6	Capacitor	10 nF, 200 V, 10%, 0805, X7R	Kemet	C0805C103K2RECAUTO
15	C34	1	Capacitor	10 nF, 25 V, 1%, 1206, NP0	Kemet	C1206C103F3GECAUTO
16	C35, C61, C66, C74, C89, C94, C100, C101, C105	9	Capacitor	100 nF, 25 V, 10%, 0805, X7R	Kemet	C0805X104K3RACAUTO
17	C37, C64, C92	3	Capacitor	1 µF, 50 V, 20%, 0805, X7R	Kemet	C0805C105M5RACTU
18	C38, C40	2	Capacitor	10 µF, 25 V, 10%, 0805, X5R	Kemet	C0805C106K3PAC7800
19	C39, C41, C71	3	Capacitor	100 nF, 25 V, 10%, 0603, X7R	Kemet	C0603C104K3RAC7013
20	C42, C62, C90	6	Capacitor	0.1 µF, 50 V, 10%, 0805, X7R	Samsung Electro-Mechanics	CL21B104KBFXPJE
21	C44, C65, C93	3	Capacitor	3.3 nF, 50 V, 10%, 0805, X7R	Kemet	C0805X332KARAC3316
22	C45, C46, C67, C68, C69, C72, C75, C87, C95, C97, C98, C99, C103, C104	14	Capacitor	100 pF, 25 V, 10%, 0805, X7R	Kemet	C0805C101K3RAC7800
23	C47, C59, C106, C107	4	Capacitor	1 µF, 25 V, 20%, 0805, X7R	Kemet	C0805C105M3RAC7800
24	C60	1	Capacitor	100 nF, 25 V, 10%, 1206, X7R	Yageo	AC1206KRX7R8BB104
25	C70, C77, C96	3	Capacitor	100 pF, 25 V, 10%, 0603, X7R	Kemet	C0603C101K3RACAUTO
26	C73	1	Capacitor	1 µF, 25 V, 10%, 0603, X7R	Kemet	C0603C105K3RAC7411
27	C101, C105	9	Capacitor	100 nF, 25 V, 10%, 0805, X7R	Kemet	C0805X104K3RACAUTO
28	C102	1	Capacitor	1 nF, 25 V, 1%, 0805, X8R	Kemet	C0805C102F3HACAUTO
29	D1, D2, D3, D5, D7	5	Schottky diode	150 V, 2A, DO-214AC (SMA)	Micro Commercial Co.	STPS2150A

30	D4	1	Zener diode	68 V, 500 mW, SOD-123	OnSemi	MMSZ5266BT1G
31	D6	1	Zener diode	5.1 V, 500 mW, SOD-123	Micro Commercial Co.	MMSZ4689-TP
32	D8, D9, D10	3	Schottky diode	30 V, 500 mW, SOD-882D	Nexperia USA, Inc.	PMEG3005ELD,315
33	G1	1	IC	IC linear regulator, 5 V, 500 mA, 8DSO E-PAD	Infineon Technologies	TLS205B0EJV50XUMA1
34	H1	1	Heatsink	Heatsink 151.253 x 42.01 x 20 mm	Advanced Thermal Solutions, Inc.	ATS-EXL2-254-R0
35	J2	1	Connector	Vertical header connector three-position 2.54 mm	Samtec	TSW-101-07-T-T
36	J3, J5	2	Connector	Terminal block 2P side ent. 2.54 mm PCB	Phoenix Contact	1725656
37	J6	1	Connector	Vertical header connector two-position 2.54 mm	Samtec	TSW-102-07-F-S
38	L1	1	Inductor	Fixed inductor 470 µH 1.4 A 560 mΩ SMD	Würth Elektronik	7447709471
39	LED1, LED2, LED3	3	LED	Clear green LED 0603	Lite-On, Inc.	LTST-C190KGKT
40	LED4	1	LED	Clear red LED 0603	Lite-On, Inc.	LTST-C190KRKT
41	OP1, OP2, OP3, OP4, OP5	5	IC	IC op-amp GP 10 MHz RRO SOT-23-5	Analog Devices	AD8615AUJZ-REEL7
42	POT1, POT2	2	Potentiometer	Trimmer, 50 kΩ, 0.25 W, J lead top	Bourns, Inc.	3224W-1-503E
43	Q1, Q2, Q3, Q4, Q5, Q6	6	MOSFET	N-channel, 120 V, 328 A, TOLL	Infineon Technologies	IPT017N12NM6
44	Q7	1	MOSFET	N-channel, 100 V, 42 A, DPAK	Infineon Technologies	IRLR3110ZTRLPBF
45	Q8	1	Transistor	PNP, 100 V, 1 A, SOT-23-3	Diodes Incorporated	FMMT593QTA
46	Q9, Q10	2	MOSFET	N-channel, 30 V, 3.4 A, SOT-23	Infineon Technologies	IRLML6346TRPBF
47	R1	1	Resistor	1, 0.75 W, 1%, 1206	Vishay Dale	CRCW12061R00FKEAHP
48	R2	1	Resistor	33k, 0.25 W, 1%, 0603	TE Connectivity	CRGP0603F33K

					Passive Product	
49	R3	1	Resistor	47k, 0.25 W, 1%, 0603	Vishay Dale	RCS060347K0FKEA
50	R4	1	Resistor	1.5k, 0.25 W, 1%, 0805	Stackpole Electronics, Inc.	RNCP0805FTD1K50
51	R5	1	Resistor	2.7k, 0.75 W, 1%, 1206	Vishay Dale	CRCW12062K70FKEAHP
52	R6, R97, R108, R109	4	Resistor	1k, 0.125 W, 1%, 0805	Vishay Dale	CRCW08051K00FKEAC
53	R7	1	Resistor	1.3k, 0.25 W, 1%, 0603	Vishay Dale	RCS06031K30FKEA
54	R8, R32, R69	3	Resistor	5.6, 0.25 W, 1%, 0805	KOA Speer Electronics, Inc.	SG73P2ATTD5R60F
55	R9, R20, R33, R48, R71, R81	6	Resistor	49.9, 0.125 W, 1%, 0805	Vishay Dale	CRCW080549R9FKEAC
56	R10, R21, R34, R49, R72, R82	6	Resistor	1.2, 0.5 W, 1%, 0805	Panasonic Electronic Components	ERJ-6DQF1R2V
57	R11, R13, R22, R26, R35, R38, R50, R53, R73, R76, R83, R87	12	Resistor	51k, 0.25 W, 0.1%, 0805	Panasonic Electronic Components	ERJ-PB6B5102V
58	R12, R25, R37, R52, R75, R86	6	Resistor	6.8, 0.125 W, 1%, 0805	Vishay Dale	CRCW08056R80FKEA
59	R14, R27, R42, R54, R77, R88	6	Resistor	100k, 0.25 W, 1%, 0805	KOA Speer Electronics, Inc.	RK73H2ARTTD1003F
60	R15, R18	2	Resistor	10k, 1 W, 0.1%, 1206	Vishay Dale Thin Film	PHPA1206E1002BST1
61	R16, R45, R79	3	Resistor	200k, 0.5 W, 1%, 0805	Vishay Dale	CRCW0805200KFKEAHP
62	R17, R46, R80	3	Resistor	22, 0.5 W, 1%, 0805	Panasonic Electronic Components	ERJ-P6WF22R0V
63	R19, R44, R99, R100, R103	5	Resistor	0, 0.25 W, 1%, 0805	KOA Speer Electronics, Inc.	RK73Z2ARTTD
64	R23, R51, R85	3	Resistor	5.1k, 0.4 W, 1%, 0805	Vishay Dale	RCS08055K10FKEA
65	R24	1	Resistor	680, 0.25 W, 1%, 0603	Vishay Dale	RCS0603680RFKEA

66	R28, R29, R55, R57, R59, R60, R62, R66, R84, R70, R91, R93, R94, R105	14	Resistor	10, 0.25 W, 1%, 0805	Stackpole Electronics, Inc.	RNCP0805FTD10R0
67	R30, R40, R41, R96, R98, R102	6	Resistor	10k, 0.25 W, 0.1%, 0805	Panasonic Electronic Components	ERA-6VEB1002V
68	R31	1	Resistor	200, 0.25 W, 1%, 0805	KOA Speer Electronics, Inc.	RK73H2ARTTD2000F
69	R36	1	Resistor	100, 0.25 W, 1%, 0805	KOA Speer Electronics, Inc.	RK73H2ARTTD1000F
70	R39, R101	2	Resistor	330, 0.25 W, 1%, 0805	Vishay Dale	RCC0805330RFKEA
71	R43	1	Resistor	200k, 0.25 W, 1%, 1206	Vishay Dale	CRCW1206200KFKTA
72	R47	1	Resistor	7.87k, 0.25 W, 1%, 1206	KOA Speer Electronics, Inc.	RK73H2BTTD7871F
73	R56, R64, R67, R78, R89, R95	6	Resistor	12k, 0.25 W, 0.1%, 0805	Panasonic Electronic Components	ERJ-PB6B1202V
74	R58, R63, R68, R74, R90, R92	6	Resistor	1k, 0.25 W, 0.1%, 0805	Panasonic Electronic Components	ERJ-PB6B1001V
75	R61	1	Resistor	22k, 0.25 W, 1%, 0603	Panasonic Electronic Components	ERJ-UP3F2202V
76	R65	1	Resistor	1k, 0.25 W, 1%, 0603	Vishay Dale	RCS06031K00FKEA
77	R104	1	Resistor	0, 0.1 W, 1%, 0603	Yageo	AC0603FR-070RL
78	R106	1	Resistor	20k, 0.25 W, 1%, 0805	Vishay Dale	RCC080520K0FKEA
79	R107	1	Resistor	1M, 0.25 W, 1%, 1206	Vishay Dale	CRCW12061M00FKEAC
80	RS1, RS2, RS3	3	Current sensor	0.001, 5 W, 1%, 3920	Stackpole Electronics, Inc.	HCS3920FT1L00
81	RT1	1	Temperature sensor	Analog sensor, 40°C to 125°C SOT-23-3	Microchip	MCP9700T-E/TT
82	U1	1	IC	LED driver IC single-output DC-DC step-down regulator	Infineon Technologies	ILD8150EXUMA1

				(buck) PWM dimming 1.5 A PG-DSO-8-27		
83	U2, U5, U7, U10, U11, U14	6	IC	Single-channel high-side and low-side gate driver with high-CMR TDI inputs	Infineon Technologies	1EDN8550B
84	U3, U8, U12	3	IC	IC gate and two-channel two-input US8	OnSemi	NLV27WZ08USG
85	U6	1	IC	Connector DIN RCPT 32POS PCB RA GOLD	Hirose Electric Co. Ltd	PCN10C-32S-2.54DS(72)
86	U15	1	IC	IC FF D-type single 1-bit 8VSSOP	Texas Instruments	SN74LVC2G74MDCUTEP
87	U16	1	IC	IC tiny comparator LV SOT-23-5	Texas Instruments	LMV331M5
88	–	1	Thermal pad	Thermal pad 457.20 x 457.20 mm pink	Laird Technologies – Thermal Materials	A17536-02
89	NT1, NT2, NT3, NT4	4	Hex nut	#4-40 hex nut 0.250 in (6.35 mm) ¼ in	B&F Fastener Supply	HNZ 440
90	J7, J8, J9, J10	4	Hex standoff	HEX standoff #4-40 aluminum 1-1/4 in	Keystone Electronics	8407
91	S1, S2, S3, S4, S5, S6	6	Phillips screw	Passivated 18-8 stainless-steel pan head Phillips screw 2-56 thread, 1/8 in long	McMaster	91772A074
92	U, V, W, J1, J2	5	Connector	Miniature banana connector jack SLDR	Keystone Electronics	476-4

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Revision history

Document version	Date of release	Description of changes
V 1.0	2023-05-31	Initial release
V 1.2	2023-08-14	Updated Figure 2 and added 2 kW testing data on Section 3.2

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