PCB design guidelines for MV GaN power transistors in high-reliability switch-mode applications

Focused on parts housed within the PowIR-SMD package

About this document

Scope and purpose

This application note clarifies several important PCB board design rules (from board stackup to placement and layout of key components) to aid the switching ability and power dissipation of RH SMD GaN power transistors in applications like DC-DC converters and motor drive topologies. Infineon Technologies International Rectifier HiRel (Infineon IR HiRel)'s first JANS-qualified 100 V RH GaN power transistor, IG1NT052N10R within the PowIR-SMD package, will be used in several examples throughout this document [1] and [2].

Intended audience

This document is intended for PCB layout engineers, switch-mode power system designers, and technicians interested in the proper implementation of the PowIR-SMD housed parts like IG1NT052N10R.
See The PowIR-SMD for medium voltage rad hard GaN power transistors for more information on how the PowIR-SMD package supports RH MV GaN power transistors [3].

Keypoints

- Outlines PCB design rules to optimize switching and thermal performance of MV RH GaN power transistors
- Compares IG1NT052N10R GaN device metrics against space-grade silicon MOSFETs, emphasizing faster switching speeds
- Explains inductive and capacitive parasitic effects on switching efficacy in half-bridge circuits and techniques to mitigate voltage overshoot
- Provides guidelines for PCB stackup, PCB layout of power stage commutation loop and gate drive loops, and key capacitor placements to reduce parasitic inductance and capacitance to improve performance
- Demonstrates the importance of current distribution in PowIR-SMD package for minimizing losses and enhancing efficiency

About this product family

Product family

Infineon IR HiRel's rad hard GaN transistors in PowIR-SMD packaging deliver industry-leading efficiency and power density for high-reliability space applications. Featuring ultra-low $R_{DS(on)}$, low total gate charge, zero reverse recovery charge, and a lightweight design, they reduce power losses and minimize payload mass while meeting MIL-PRF-19500 standards for mission-critical environments.

Target applications

- DC-DC converters

About this product family

- Point-of-load (PoL) converters for FPGA, ASIC, and DSP core rails
- Synchronous rectification
- Motor drives

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1 Introduction

Medium voltage (60 V to 200 V devices) radiation hardened (RH) gallium nitride (GaN) power transistors have become widely adopted in high-reliability switching topologies within satellite power systems for all kinds of missions. Their attractive electrical characteristics allow them to outperform traditional silicon (Si) power MOSFETs in the same voltage class.

It is important to mitigate several key circuit board parasitics through proper layout practices to achieve higher levels of performance in such applications. In addition, wicking heat away from these GaN devices using thermal vias need to be considered.

To understand why these PCB design rules are tailored for high-reliability circuits using MV GaN power transistors, two fundamental concepts must be established:

- Compare electrical characteristics related to the commutation action of GaN power transistors with Si power MOSFET counterparts
- Examine the implications of these switching characteristics within the context of a half-bridge (a foundational component of many switching topologies including DC-DC converters and motor drive designs). There are several embedded circuit elements (resistive, inductive, and capacitive parasitics) throughout a half-bridge structure. These could hamper the performance of an MV GaN-based switch-mode topology

Based on these fundamental concepts, this application note provides three categories of PCB development guidelines for mitigation techniques:

- Appropriate PCB stackups
- Copper pour design recommendations and via placement
- GaN power transistor arrangement

These guidelines are presented with a demonstrative half-bridge design as an example. The following sections provide diagrams, PCB renderings, and layout images.

2 RH GaN vs. RH silicon power transistor comparison

Table 1 compares three JANS-qualified parts, the RH 100 V GaN power transistor (IG1NT052N10R/JANSG2N7697UFHC) against two 100 V RH Si power MOSFETs with extensive space-mission heritage (IRHNJC9A7130/JANSR2N7648U3C and IRHNJ67130/JANSR2N7587U3). Several component-level electrical characteristics are shown in Table 1. All three devices have approximately similar die sizes [4] and [5].

Table 1 Electrical characteristics of space-grade 100 V power transistors

Device metric[1]	IG1NT052N10R/ JANSG2N7697UFHC	IRHNJC9A7130/ JANSR2N7648U3C	IRHNJ67130/ JANSR2N7587U3
Nominal die size (mm^2)	11	14	14
Maximum drain-source resistance ($R_{DS(on)}$, mΩ)	6	34	42
Maximum total gate charge (nC)	13	48	50
Typical transconductance (S)[2]	65	24	21
Maximum threshold voltage (V)	2	4	4

In all these devices, a higher current moves through the conduction channel of the device as the switch becomes fully active. This rate of increase in current flow is influenced by the overall transductance (G_M) of the device. In addition, circuit parameters like total gate charge (Q_G) and threshold voltage (V_{TH}) dictate a power transistor's switching speed from a given gate drive supply. Switching times decrease as Q_G and V_{TH} are reduced. As shown in Table 1, IG1NT052N10R has electrical metrics favorable over its Si counterparts – realizing faster switching speeds if this device is placed within an appropriate half-bridge with mitigated parasitics.

[1] For test specifications per metric, see each device's datasheet

[2] Calculated from "Typical Transfer Characteristics" at 25°C curve of each datasheet

3 Half-bridge characteristics

A half-bridge circuit may consist of two switching devices oriented between a power source input (V_{IN}) and a reference return plane (GND) as shown in Figure 1. These two switches can turn on and off asynchronously to invert an input DC voltage. Some of the common applications are as follows:

- Use as a rectifier to convert the switch-node (SW) power signal to a DC structure at a different voltage using a low-pass filter, resulting in a DC-DC converter
- Use in a direct connection to a motor, constructing an AC motor drive circuit
- Form an H-bridge by connecting two half-bridges across a load
- Form a 3-phase motor drive by paralleling three or more half-bridges together

In all these cases, the fundamental legs to construct these circuits are half-bridges. See Figure 1 that shows a half-bridge loop and its two possible applications.

Half-bridge characteristics

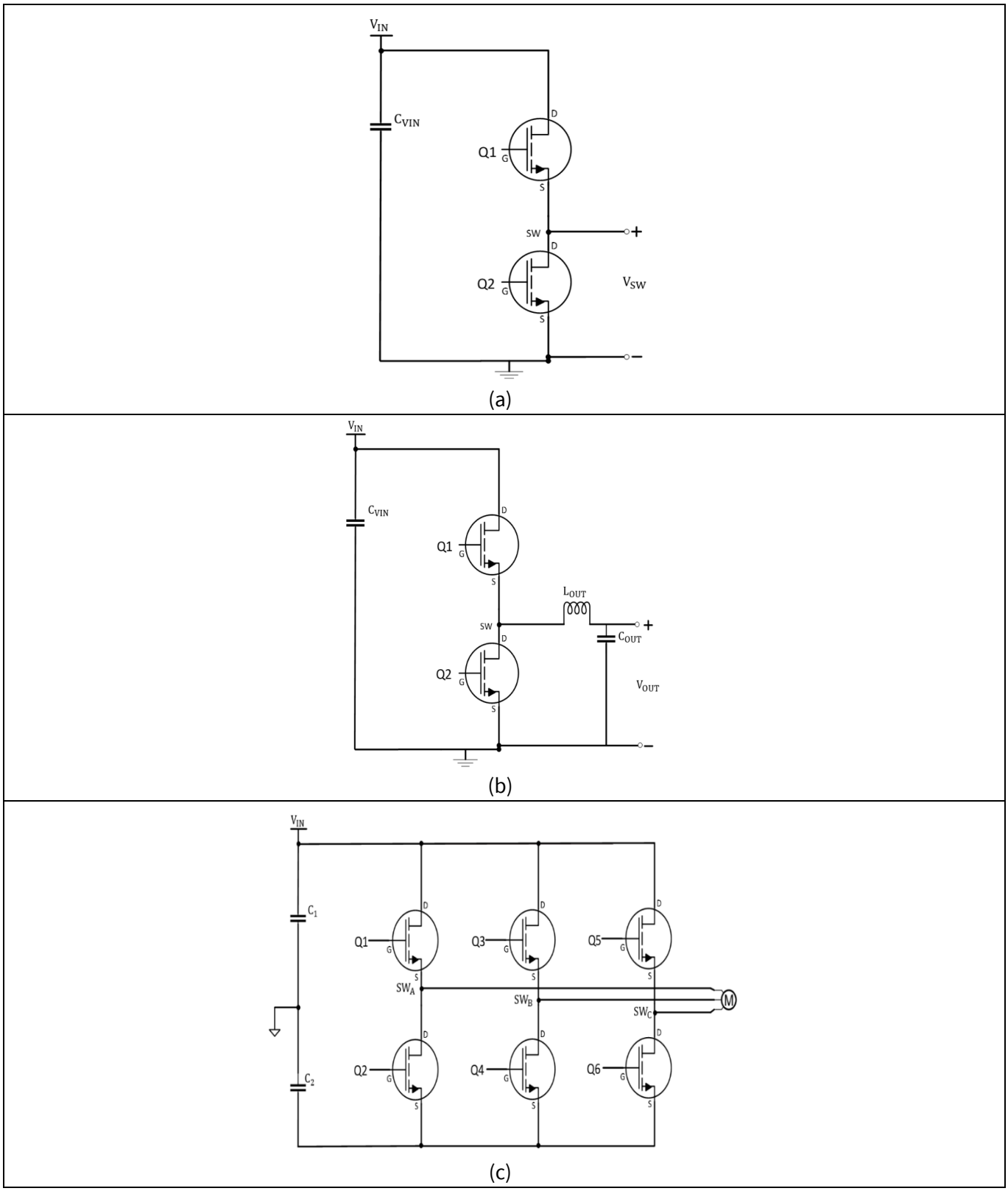


Figure 1 **(a) Diagram of a half-bridge power stage with transistor switches; and two potential applications: (b) Single-phase synchronous buck converter; (c) 3-phase motor drive**

3.1 Switching cycle of a half-bridge at steady state

This section discusses the general behavior of a half-bridge during a switching cycle at steady-state operation.

When Q1 activates in the first half-cycle, current supplied by V_{IN} rushes through the conduction channel of Q1 to charge the capacitance at the switch node (C_{SW}). Charging a large amount of C_{SW} will allow significant levels of displacement current to flow in a loop like the power stage commutation loop – resulting in a manifestation of significant common-mode noise [6].

V_{IN} (referenced to GND per Figure 1) must be stable against various current transients present in the loop (shown by the orange arrows in Figure 1). Strong current transients within this loop could couple with significant amounts of inductance to shift the voltage seen across the two stacked power transistors in the form of voltage ringing.

For example, in a hard-switching buck converter, sufficient inductance present in this loop will cause a voltage overshoot across Q2 to manifest when Q1 fully activates rapidly. This overshoot could be dangerous if it exceeds the drain-to-source voltage (V_{DS}) capabilities of Q2. Figure 2 provides a closer look into the location of prominent reactive circuit parasitics and the current vectors within a half-bridge, power-stage commutation loop (shown in orange color).

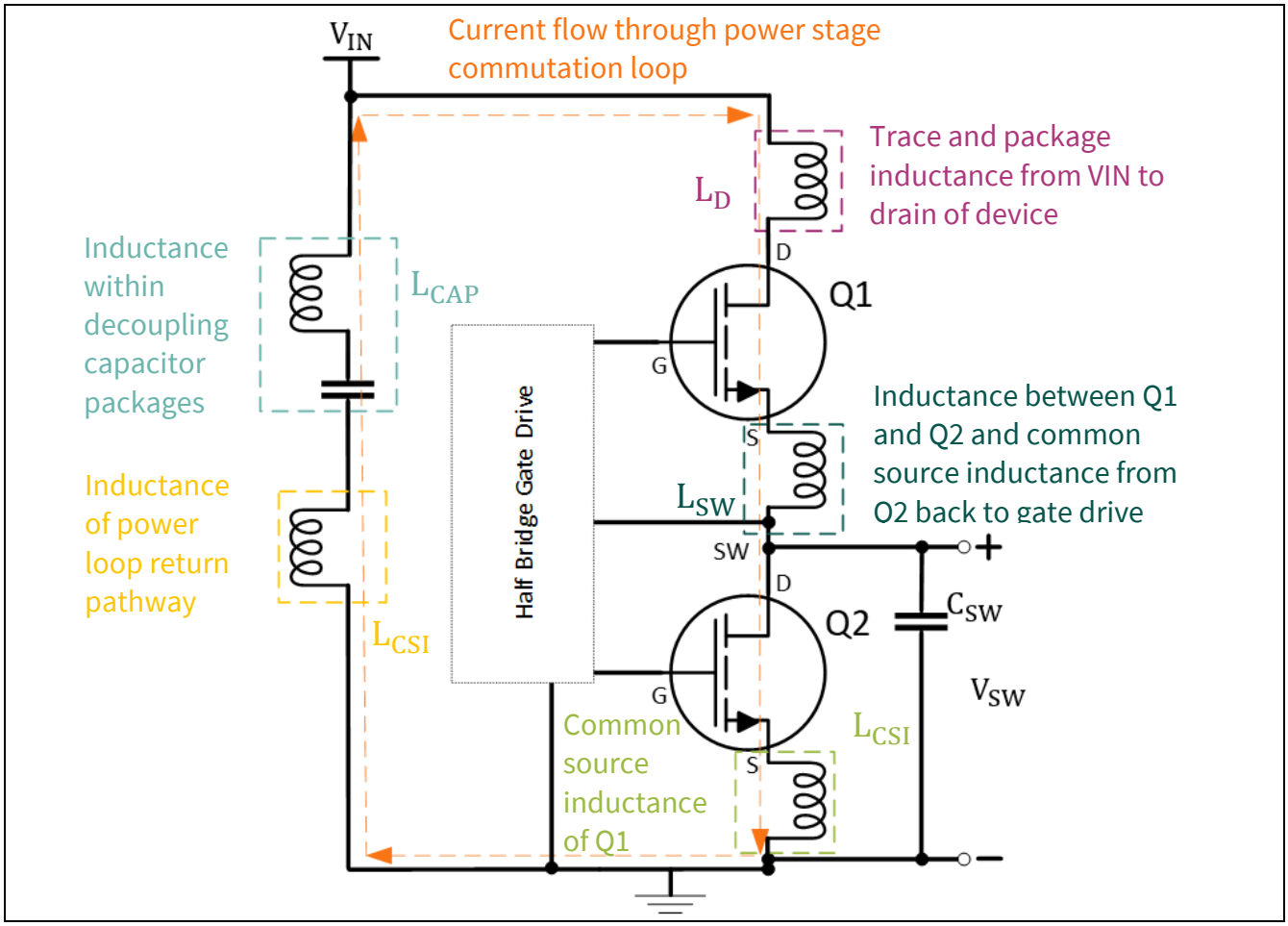


Figure 2 **A closer look on the commutation loop of a half-bridge power stage – some gate drive parasitics have been omitted to simplify picture (see Figure 3 for more information on gate drive)**

3.2 Effect of parasitic inductance coupling

The central principle of parasitic inductance coupling to strong current transients is present in other commutation loops like gate drive circuits as well. Prominent parasitic inductances could potentially slow switching speeds and lead to voltage overshoots at a power transistor's gate electrode, thereby increasing losses (heating up the device) and degrading the part over time.

Decoupling a gate drive loop from a power stage commutation loop (minimizing the common-source inductance for example) with proper layout techniques and potentially a Kelvin-source connection will help stabilize a power transistor's function. Figure 3 expands the scope seen from Figure 2 to include these comments.

For more information on examples of significant inductance disrupting device performance, see the following sections in the application note, The PowIR-SMD for medium voltage rad hard GaN power transistors:

- Section 3.1 "Gate drive parasitics in high-speed power discretes"
- Section 4.1 "Tightening the gate drive loop"

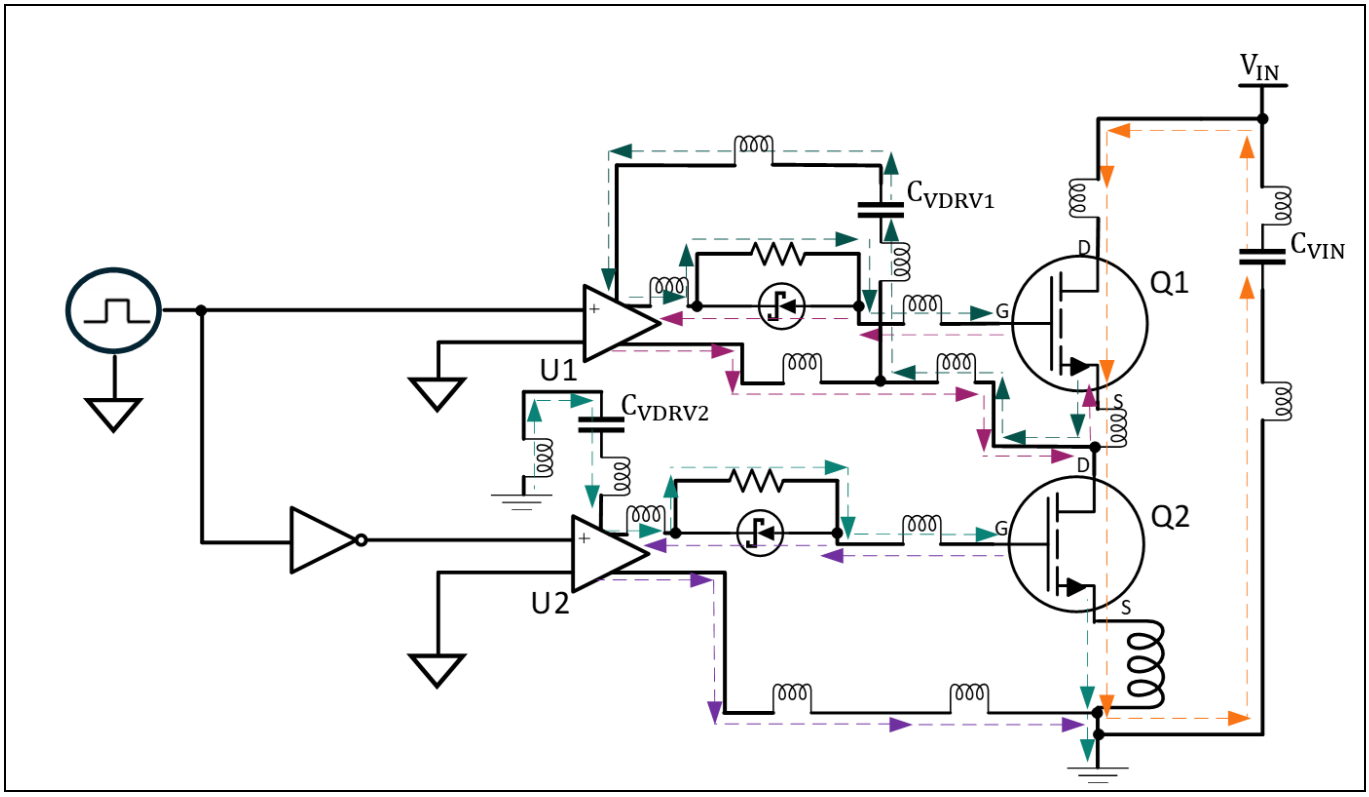


Figure 3 Simplified diagram depicting half-bridge structure with critical displacement current using two single output gate drives – (orange is power stage commutation loop, shades of green are turn-on gate drives, and shades of purple are turn-off gate drives)

All design rules presented in the following sections are also applicable to Si power MOSFETs. However, fast-switching devices with high transconductances like GaN power transistors experience stronger effects from parasitic inductances and capacitances. Therefore, GaN devices require particular attention. With a surface mount, the flip-chip style package used in PowIR-SMD will support circuit designs with low parasitic inductance, suited for high-speed MV RH GaN power transistors.

4 PCB design recommendations

This section provides recommendations for PCB design for fast-switching RH GaN power system topologies in the following topics. Follow these guidelines to minimize parasitic inductances, capacitances, and efficiently transfer heat out of the device in fast-switching circuit loops. These guidelines are especially relevant for any inductance shared between a gate drive loop and a power stage loop.

- PCB stackup
- PCB layout
- Component placement

4.1 PCB stackup

Routing low-inductance gate drive and power stage commutation loops should involve two PCB layers to maximize cancellation of the mutual inductance [7] and [8].

- Use relatively thin dielectrics between the two outer conductor layers to create a differential pair to minimize the size of these critical loops
- Space apart these paired conductor layers with larger dielectric cores to minimize the amount of parallel plate capacitance that parasitically bridges each differential pair
- Using standard conductor thicknesses of 2 oz. copper pours, separate each differential conductor pair by approximately 3 mils (~80 µm) of dielectric material
- For an overall ~62 mils (1.5 mm), 4-layer PCB stackup, use approximately 43 mils (1.1 mm) for the large dielectric core that separates both differential pairs. Figure 4 provides details on a suitable 4-layer PCB stackup for MV RH GaN

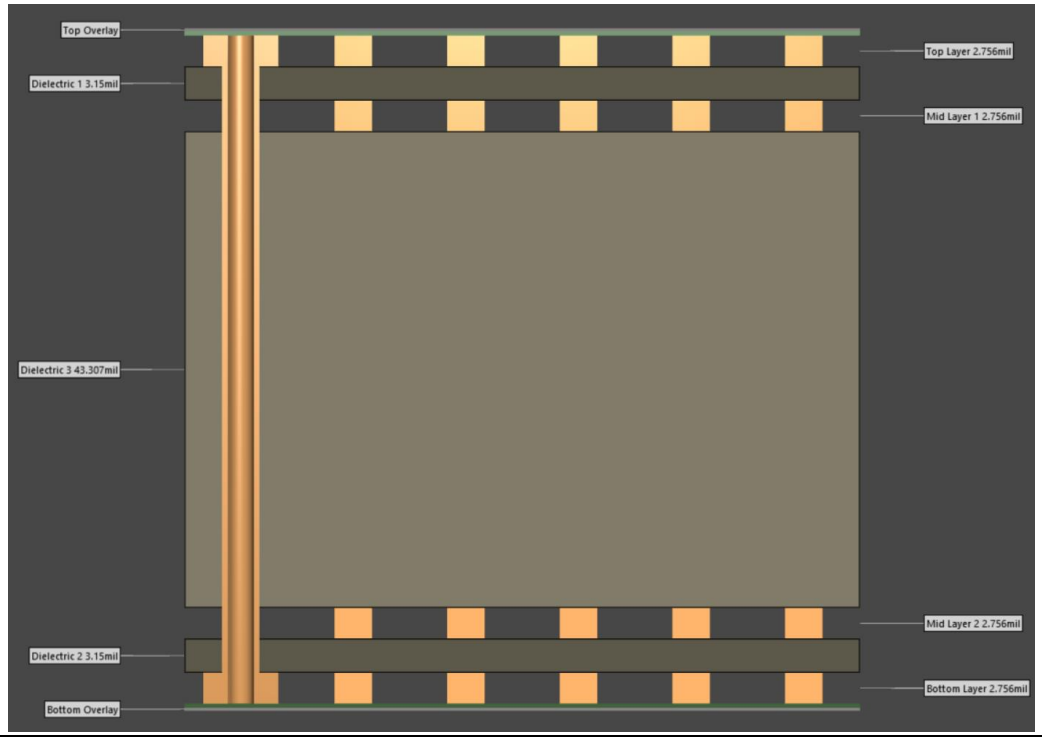


Figure 4 PCB stackup leveraging differential pairs on either side of the board with a larger, center dielectric to minimize stray capacitance between both differential pairs

4.2 PCB layout

This section provides recommendations on PCB layout for two sections:

- Power stage commutation loop
- Gate drive circuits

4.2.1 Optimizing power stage commutation loop

Figure 5 and Table 2 summarize key considerations relevant to the power stage commutation loop.

Table 2 Figure 5 features of interest

Figure	Description
Figure 5(a)	Half-bridge PCB board employing design rules described in Sections 4.1 and 4.2. High-frequency decoupling capacitors (HF caps) are placed close to drain high-side (HS) RH GaN power transistor (Q1) whereas bulk capacitors are allowed to be further away
Figure 5(b)	2-D perspective of top-side copper pour (red polygons). There are several via-in-pad groups (SW_{vias}, C_{vias}, and GND_{vias}) to serve various functions. The three solid green arrows represent current vectors as charge flows from V_{IN} to GND through Q1 and Q2. Q1 and Q2 pads are also annotated (“D” for drain, “G” for gate, “KS” for kelvin-source, “S” for source)
Figure 5(c)	2-D perspective of the first inner copper pour (orange polygons). The same three vias-in-pad groups are present. This layer shows the high-frequency current return pathway to complete the power stage commutation loop (shown with purple arrows)
Figure 5(d)	2-D representation of the second inner copper pour (light blue polygons). This layer is separated from the top two copper pours via a thick dielectric core. Notice the SW_{vias} interface to a polygon in this pour to expand the size of SW and help transfer heat away from Q1 and Q2
Figure 5(e)	2-D view of bottom-side copper pour (dark blue polygons). Another copper polygon is connected to SW_{vias}

4.2.2 Guidelines for reducing parasitic inductance in power stage commutation loop

With a PCB stackup that employs differential conductor pairs, parasitic inductance found throughout a power stage commutation loop can be reduced by leveraging mutual inductance cancellation.

The first inner conductor layer should serve as the return pathway for the power stage current. Ensure that this inner layer maintains a structure similar to the top copper layer to develop an anti-parallel current pathway. Notice in Figure 5(b) and Figure 5(c) how current is allowed to travel in clearly opposite lines per the green arrows. It is preferable to minimize the overall length that this current must travel while simultaneously maximizing the width of this current pathway.

For example, add capped and filled vias into the source pad of Q2. Assuming that anti-parallel current pathways have been incorporated, consider this aspect ratio, (n = length of current travel/width of current passageway), as a simple catch-all metric. Lower values suggest that the current encounters a reduced amount of parasitic impedance, thereby improving the switching performance. An optimal power stage commutation loop places Q1, Q2, the high-frequency decoupling capacitors, and bulk capacitors on the same side of the board. Figure 5(a) shows all these components on the top side of the PCB for example.

4.2.3 Guidelines for capacitor placement

Utilize two distinct groups of decoupling capacitor banks: large, bulk capacitors and smaller, high-frequency capacitors.

- **Bulk capacitors** should have a clear, wide connection between the input power connection, inputs of the HF decoupling capacitors, and the drain of the high-side RH GaN power transistor. They serve to maintain the overall input power stage DC voltage (V_{IN}) when the high-side switch is active
- **High-frequency decoupling capacitors** (see Figure 5(a)) should be placed near the drain pin of the high-side switch to help provide a low-inductance pathway for HF components of current traveling through this power stage

For each capacitor group, ideally utilize several units in a row to again maximize effective current pathway width for a given package size. Place capped and filled vias in the pads of these capacitor groups to bridge the first inner return layer and the top layer as well (see "C_{vias}" in Figure 5(a) and Figure 5(b)).

Some degree of capacitive coupling between SW and DC return is unavoidable but minimize the amount of overlap to limit the circulating displacement current. Optimally, the size of SW copper should be tailored to the expected amount of current flowing to the load – no larger than necessary. Inner layer 1 "Power loop return" helps contain radiating electric fields from SW. Vias within the pads of Q1 and Q2 at SW can be used to route this node to other conductor layers on the opposite side of the PCB to help dissipate heat away from both devices (see "SW_{vias}" in Figure 5(b), Figure 5(c), Figure 5(d), and Figure 5(e)).

As previously mentioned, minimize the collective width these vias possess across the first inner layer current return pathway. In Figure 5(c), SW_{vias} maintain a vertical orientation; if this via group was oriented in a horizontal pattern, they would impede returning current more significantly – demonstrated by greater overlap with the green arrows serving as current vectors.

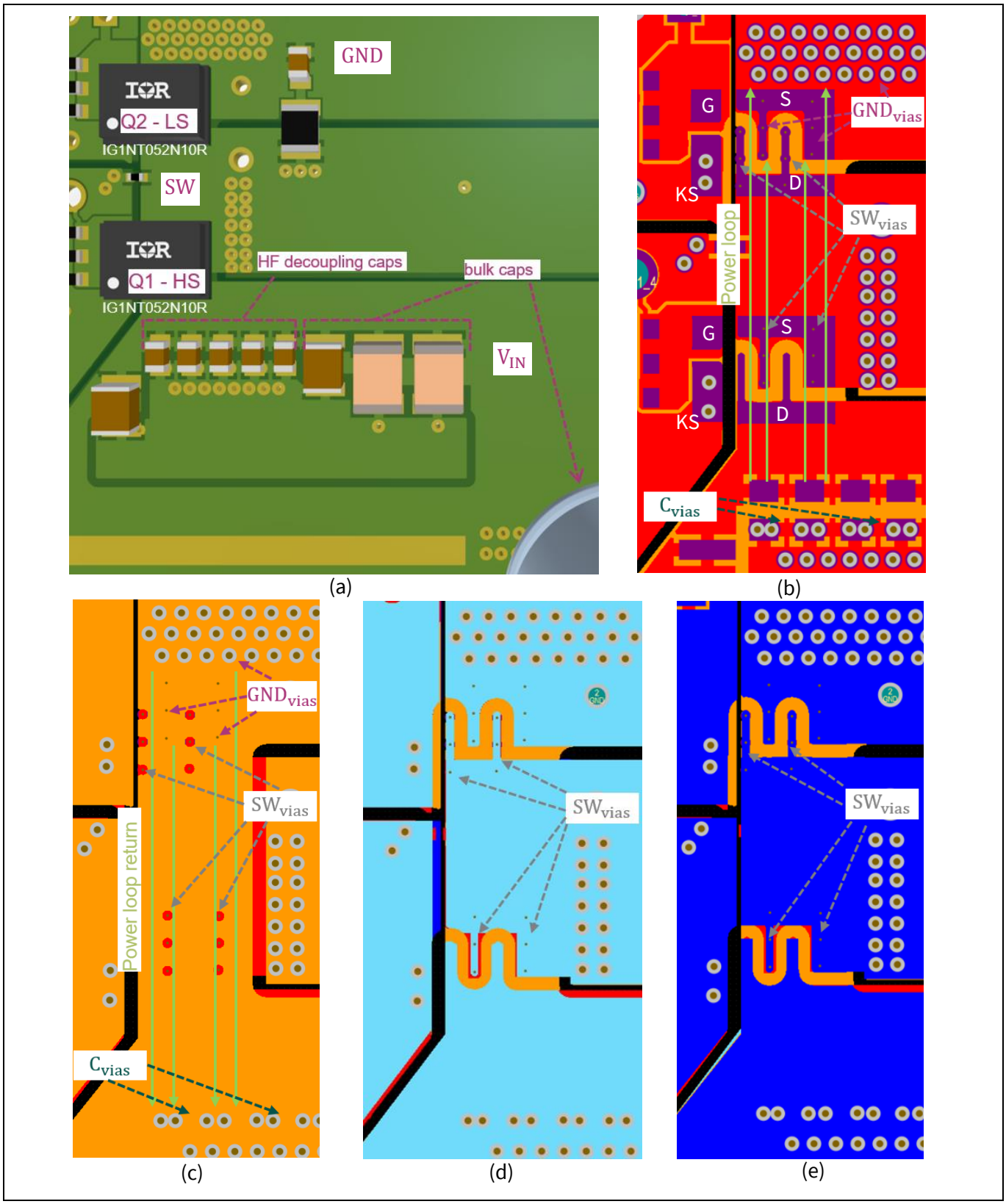


Figure 5 **Half-bridge layout using IG1NT052N10R in PowIR-SMD; (a) 3-D top side view of board, (b) top copper, (c) inner layer 1 copper, (d) inner layer 2 copper, (e) bottom layer copper**

4.2.4 Optimizing the gate drive loop

Several images are presented in Figure 6 on the next page with Table 3 describing key features of interest relevant to the two gate drive commutation loops of Q1 and Q2.

Table 3 Figure 6 features of interest

Figure	Description
Figure 6(a)	Same 3-D representation of half-bridge board shown in Figure 5. Gate drive decoupling capacitors to aid Q1 and Q2 turn-on are annotated (C_{VDRV1} and C_{VDRV2} respectively). HS and low-side (LS) gate drivers also indicated
Figure 6(b)	2-D view of the top layer copper (red polygons). Q1 and Q2 turn-on gate drive pathways shown with groups of arrows (green shades indicate turn-on whereas blue shades indicate turn-off). Both gate drive outputs (DRV_{OUT1} and DRV_{OUT2}) are shown. Two via-in-pad groups ($KS1_{vias}$ and $KS2_{vias}$, respectively) connect the Kelvin source (KS) of Q1 and Q2 to the first inner copper plane to help minimize gate drive loop inductances
Figure 6(c)	2-D perspective of 1st inner copper pour (orange polygons). Direct return pathway to C_{VDRV1} and C_{VDRV2} are shown

Tight, low-inductance gate-drive loops to source and sink the charge away from the gate electrodes of the RH GaN power transistors offer the best solution to minimize switching times and voltage overshoots or undershoots.

Figure 6 shows two main gate drive pathways. The first (most critical) is the turn-on pathway where the charge supplied by decoupling capacitors (C_{VDRV1} for Q1 and C_{VDRV2} for Q2) is sent to the gate electrode of the RH GaN power transistor to activate the device. Place these capacitors close to the gate electrodes of the switching RH GaN power transistor. Figure 6(a) and Figure 6(b) show an example of close decoupling capacitor placement.

It is common for a resistor to be placed in between the gate driver output and RH GaN gate electrode to lower the peak source current, which reduces the peak gate voltage overshoot. Keep in mind that additional components in gate drive pathways will always add more parasitic inductance.

Consider the gate drive turn-on of Q1: Trace a current pathway starting from the gate drive output (DRV_{OUT1}) to the gate electrode of the power transistor (G) out the Kelvin source pad (KS), finally through the decoupling capacitor (C_{VDRV1}). Devices like IG1NT052N10R in PowIR-SMD package offer a low-inductance Kelvin sense connection to support these gate drive loops.

The turn-off pathway should adhere to the same principles to remove the charge. However, decoupling capacitors are no longer involved; the charge will dissipate throughout the gate drive copper pours. Ideally, these gate drive pathways should be orthogonal to the current in the main power stage commutation loop to help minimize magnetic coupling.

Similarly, in the power stage commutation loop, use the first inner layer as a gate drive reference plane for each driver to incorporate mutual inductance cancellation (see Figure 6(c)). For example, these first inner layer reference pours should be connected to KS of IG1NT052N10R. This maintains a common potential with the power stage source pad (S) without introducing a significant common-source inductance. Inner copper layer 2 and bottom side copper do not play a significant role for gate driving; thus, they have been omitted. Figure 6 shows these recommendations.

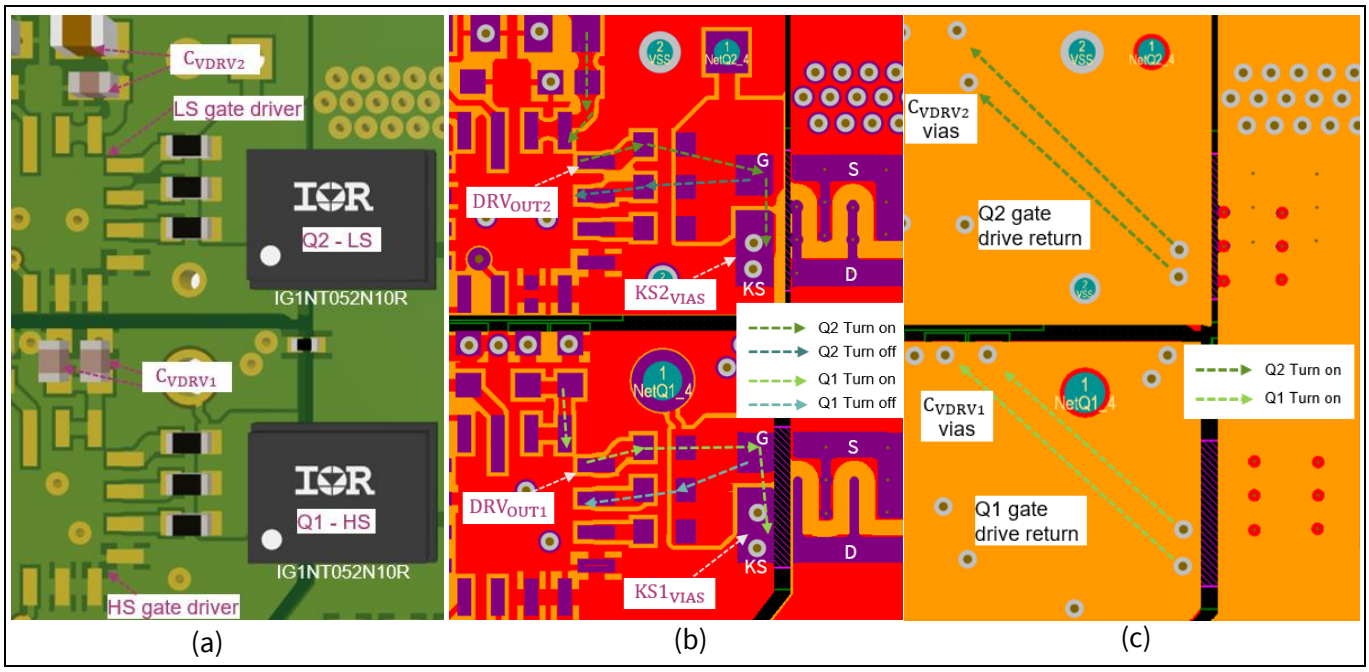


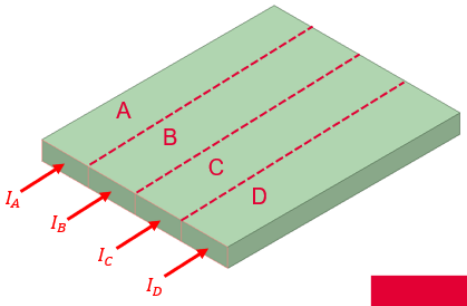
Figure 6 **Multiple views of half-bridge layout using IG1NT052N10R in PowIR-SMD; (a) 3-D top-side view of board to show component placement, (b) top copper to identify top-side gate drive pathways, (c) inner layer 1 copper with annotated gate drive return copper pour**

4.3 Placement of the PowIR-SMD device

The PowIR-SMD package has been specially designed to support proper operation of enhancement mode RH GaN power transistors up to 100 V with its low-impedance construction for high current carrying capability in a small form factor. To minimize parasitic resistances introduced by this package when placed on a PCB, consider how the power stage current will pass through the drain to the source of the device housed within the PowIR-SMD package.

Ideally, this current should be allowed to propagate in clear pathways with minimal tight corners. Otherwise, current densities within a copper layer region will partition unevenly and losses will arise. Figure 7 demonstrates this unequal current carrying concept where different proportions of current are shared between four sections of the conductive block (A, B, C, and D sections).

When all four quadrants share an equal amount of current (designated as “Uniform load”), the overall resistance of the block is minimized. However, when some quadrants carry a greater percentage of current than others, the cumulative resistance becomes greater; the conductive block becomes a less efficient conductor (“Non-uniform load, v1 to v5” provides several examples). The worst-case scenario occurs at “Non-uniform load v5” where all the available current flows through a single quadrant, resulting in a 48% increase in effective resistance from the “Uniform load” baseline value. Spreading the current across the entire width of the conductor will result in the lowest losses.



› Total current through the conductor remains the same, but the pad area (where input current is applied) may change.

Various options of the input current assignments:

	Currents applied to pads A, B, C and D				Total input current, A	Resistance, mOhm	Resistance increase, %
	I_A	I_B	I_C	I_D			
Uniform load	0.25	0.25	0.25	0.25	1	0.108	--
Non-uniform load, v1	0.4	0.3	0.2	0.1	1	0.111	+3%
Non-uniform load, v2	0.5	0.3	0.15	0.05	1	0.116	+7%
Non-uniform load, v3	0.5	0	0	0.5	1	0.122	+13%
Non-uniform load, v4	0.5	0.5	0	0	1	0.133	+23%
Non-uniform load, v5	1	0	0	0	1	0.160	+48%

Figure 7 **Several instances of current distributions with uniform load (first row) providing equal partition of current across the 4 quadrants of the conductor (resulting in lowest resistance) whereas non-uniform load v1 through v5 present greater resistance from unequal current sharing**

Now, consider the simulation of the PowIR-SMD package shown in Figure 8. Here, 1 A of current was uniformly applied through the drain (blue) and source pad (red). This package offers wide drain and source pads to distribute the power stage current across its width. As a result, a die-free package resistance of 1.5 mΩ was achieved.

Ensure that the HF capacitors, bulk capacitors, and input power connections are all oriented across the width of these two pads to avoid congestion around sharp corners (see Figure 5(a) for an example).

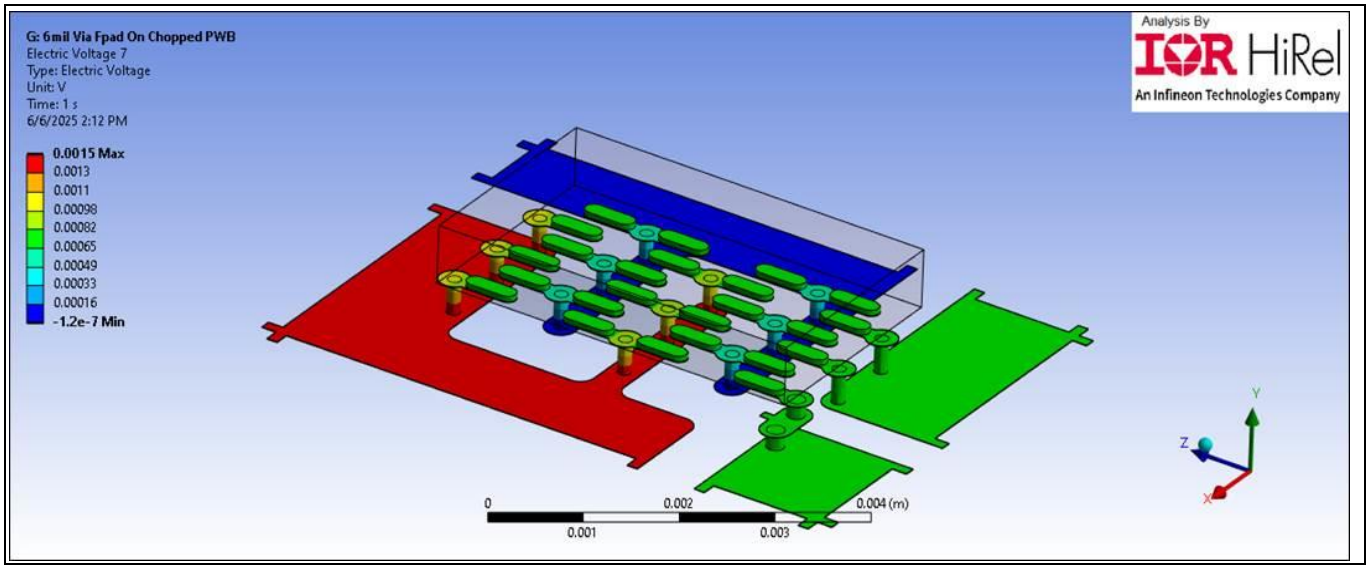


Figure 8 **FEA simulation of PowIR-SMD variant where 1 A of current is partitioned evenly across the drain pad to the source pad – resulting in a voltage drop of 1.5 mV**

5 Conclusion

This application note presented several recommendations to help high-reliability power system designers in properly utilizing MV RH GaN power transistors like the IG1NT052N10R in switching topologies. For an example half-bridge, the general design flow should adhere to the following guidelines:

- Incorporate a PCB stackup that leverages closely spaced differential conductor layers where each conductor pair is separated by thick dielectrics
- Strategically place the RH GaN devices, HF decoupling capacitors, and interconnecting vias within a wide straight line to allow HF displacement current to flow in the shortest loop possible and avoid bulk current congestion
- Place thermal vias within the transistor pads carefully to not disrupt the HF current. Additionally, route vias connected to the switch node to a second differential layer pair to help transfer the heat away from the GaN devices
- Minimize the parasitic inductance within gate drive loops by closely spacing the driver, decoupling capacitors, and transistors. Also use the first inner differential layer to provide a wide plane for the HF gate drive displacement current to flow, thereby leveraging mutual inductance cancellation
- Optimize the size of the SW conductor pour to be appropriate for the expected power stage current to flow in the application. Excessively large SW conductors can potentially introduce excessively large electromagnetic interference

Demo designs with schematics, PCB layout files, and fabrication information are available upon request. Visit the Rad hard GaN webpage for the latest information on RH GaN power transistors.

6 Related resources

- Rad hard GaN webpage
- High Reliability community forum from Infineon

References

[1] Infineon Technologies AG: IG1NT052N10R (JANSG2N7697UFHC) datasheet; Available online

[2] MIL-PRF-19500/794 performance specification sheet; Available online

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[6] IEEE: Mapping the Interdependence of Parasitic Capacitances in Isolated Phase-Shifted Full-Bridge DC/DC Converter; Available online

[7] Infineon Technologies AG: Optimizing PCB layout for HV CoolGaN™ power transistors; Available online

[8] Infineon Technologies AG: Designing an optimized half-bridge DC-DC converter with medium-voltage CoolGaN™ transistors ; Available online

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