OptiMOS™ 7 40 V switching optimized power MOSFETs

Introducing the latest Infineon technology for AI switching topologies

About this document

Scope and purpose

This application note provides a comprehensive introduction to Infineon's latest OptiMOS™ 7 40 V trench power MOSFET technology and highlights the benefits it delivers for AI power conversion and switching applications.

Intended audience

The intended audience for this document includes design engineers, technicians, students, and developers of electronic systems.

Keypoints

- Explains how OptiMOS™ 7 40 V switching optimized MOSFET technology addresses efficiency and power density challenges in AI power conversion systems
- Describes hard-switching and soft-switching converter requirements, highlighting the impact of $R_{DS(on)}$, Q_{OSS}, and gate charge on performance
- Demonstrates the benefits of source-down packaging and application-optimized silicon technology for thermal management and high-current operation
- Presents benchmarking results across SHSC, ZSC, and HVIBC topologies to evaluate efficiency, power loss, and thermal performance improvements
- Compares OptiMOS™ 7 40 V and OptiMOS™ 6 MOSFETs, showing enhancements for high-frequency soft-switching applications and low-voltage gate drive operation

About this product family

Product family

Infineon's OptiMOS™ power MOSFETs provide high-performance operation with increased efficiency, power density, and cost-effectiveness. With ultra-low $R_{DS(on)}$ and low gate charge for high switching frequency, they are well suited for a wide range of applications.

Target applications

- Intermediate bus conversion - Artificial intelligence and high-performance computing
- Industrial power supplies
- Server
- Telecom
- Information and communication technologies

Table of contents

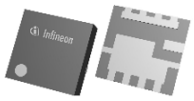
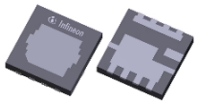
About this document **1**
About this product family **1**
Table of contents **2**
1 Portfolio: OptiMOS™ 7 40 V switching optimized MOSFET **3**
2 Introduction and motivation: OptiMOS™ 7 40 V MOSFET **4**
2.1 Introduction: AI power consumption 4
2.2 OptiMOS™ 7 application optimized – hard switching vs. soft switching 4
2.2.1 High frequency soft-switching applications 5
3 Technical considerations for enhancing data center energy supply **6**
3.1 Topology: Requirements for power MOSFET technology and packaging 6
3.2 Packaging: Source-down package 6
3.3 Technology: OptiMOS™ 7 40 V switching optimized 7
3.3.1 OptiMOS™ 7 40 V induced turn-on ruggedness 8
4 OptiMOS™ 7 40 V 3.3 × 3.3 source down – switching optimized **10**
4.1 Performance benchmarking: SHSC 11
4.2 Performance benchmarking: ZSC 12
4.2.1 ZSC body diode conduction time 13
5 OptiMOS™ 7 40 V 5×6 drain down – switching optimized **15**
5.1 Benchmarking: HVIBC 16
6 Datasheet comparison: OptiMOS™ 6 40 V vs. OptiMOS™ 7 40 V MOSFETs **17**
7 Summary **18**
8 Related resources **19**
References **20**
Revision history **21**
Disclaimer **22**

1 Portfolio: OptiMOS™ 7 40 V switching optimized MOSFET

Infineon's OptiMOS™ 7 switching optimized MOSFET family presents "switching optimized" discrete power MOSFETs, ideally suited for power conversion in AI and SMPS DC-DC converters.

The OptiMOS™ 7 40 V portfolio offers low on-state resistance ($R_{DS(ON)}$) with standard package options like PQFN 3.3 × 3.3 and SuperS08 5 × 6 dual side cooling.

This new family is optimized for GaN device compatibility by enabling a very low $R_{DS(ON)max}$ at V_{GS} of 4.5 V.

Product Name	$R_{DS_{on,max}}$@4.5V (mΩ)	$R_{DS_{on,max}}$@10V (mΩ)	Package	
IQE010N04LM7CG	1.2	1	PG-TTFN-9-1	
IQE010N04LM7CGSC	1.2	1	PG-WHTFN-9-1	

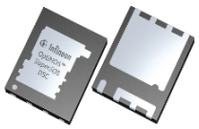
Product Name	$R_{DS_{on,max}}$@4.5V (mΩ)	$R_{DS_{on,max}}$@10V (mΩ)	Package	
ISCH69N04LM7SC	0.9	0.69	PG-WSON-8	
ISC011N04LM7SC	1.45	1.1	PG-WSON-8	

Figure 1 OptiMOS™ 7 40 V portfolio: $R_{DS(on),max}$ values and package variants

2 Introduction and motivation: OptiMOS™ 7 40 V MOSFET

2.1 Introduction: AI power consumption

The rapid growth of digital technologies has led to a significant increase in data center energy consumption in recent years, driven by the increasingly widespread use of cloud computing, big data analytics, and artificial intelligence. This trend is expected to continue in the coming years, with studies suggesting an exponential increase in global data center energy consumption, as shown in Figure 2.

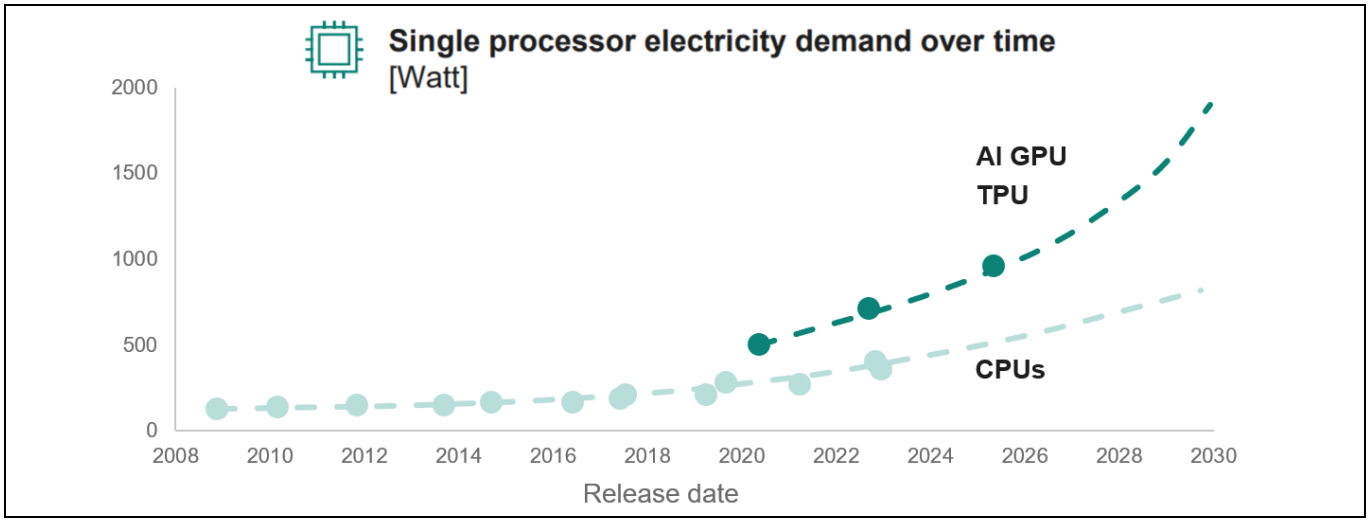


Figure 2 Single-processor power demand over time [1]

As a result, improving the operational efficiency of data centers has become increasingly important. Consequently, continued innovation in technologies that enable more efficient data centers are crucial.

As a semiconductor company, Infineon is committed to advancing both decarbonization and digitalization. By developing and delivering energy-efficient semiconductor solutions, Infineon helps data centers reduce their environmental impact while maximizing system performance.

A general-purpose power MOSFET technologies are no longer sufficient to meet the demands of the next-generation power conversion systems. Therefore, an application-optimized approach is required, as discussed in the following sections.

2.2 OptiMOS™ 7 application optimized – hard switching vs. soft switching

One of the key challenges in modern data centers is to transport power from the grid to the GPU with maximum efficiency. The 48 V ecosystem is now the standard for reducing distribution losses. To maximize performance, optimization has evolved beyond general-purpose MOSFET technologies towards solutions specific to intermediate bus converter (IBC) topologies, focusing on two main approaches based on the switching mode of operation.

- **Hard-switching topology (HSW)** refers to a specific type of converter that uses a ‘hard switching’ technique, a method where the MOSFET (or a switch in general) is turned on and off abruptly, causing a shared presence of current and voltage within the MOSFET. In this type of topology, the current and the voltage overlap in the control MOSFET causing switching losses. Further, it can cause EMI distortions. The advantage of this type of topology is that the output voltage can be regulated in a simple way with least number of components. The switching losses increase with switching frequency, typically limiting the frequency to below 300 kHz to 400 kHz

- **Soft-switching topology (SSW)** refers to a specific type of converter that uses a 'soft-switching' technique, a method in which there is no overlap of current or voltage during switching. This is achieved by keeping either the voltage across the switch and the current through the switch at zero during the switching transition. The two main types are:
  - Zero voltage switching (ZVS), the MOSFET turns on when the voltage is approximately zero. Normally obtained by magnetizing current
  - Zero current switching (ZCS), the MOSFET turns off when the current is approximately zero. Normally obtained using a resonance converter

This technique helps to reduce or eliminate switching losses and EMI effect, while also minimizing voltage overshoot and ringing effect. As a result, it enables operation at switching frequencies above 1 MHz. In contrast, these converters are unregulated or semi-regulated and generally operate with a fixed conversion ratio (4:1, 6:1, or 8:1).

2.2.1 High frequency soft-switching applications

As explained above, in a soft-switching technology, the switching frequency can be increased due to the lack of switching losses. This allows the magnetic components to be optimized by reducing the core volume, thereby increasing power density.

The switching period can be divided into two parts: active-time and dead-time.

- **Active-time** is the period during which the MOSFET is in the ON state and conducting current. For the same amount of energy transferred, the shorter the active-time (resulting from a higher switching frequency), the higher the current value and, consequently, the greater the conduction losses
- **Dead-time** is the time required to complete ZVS, thus avoiding cross conduction between MOSFETs with different phases

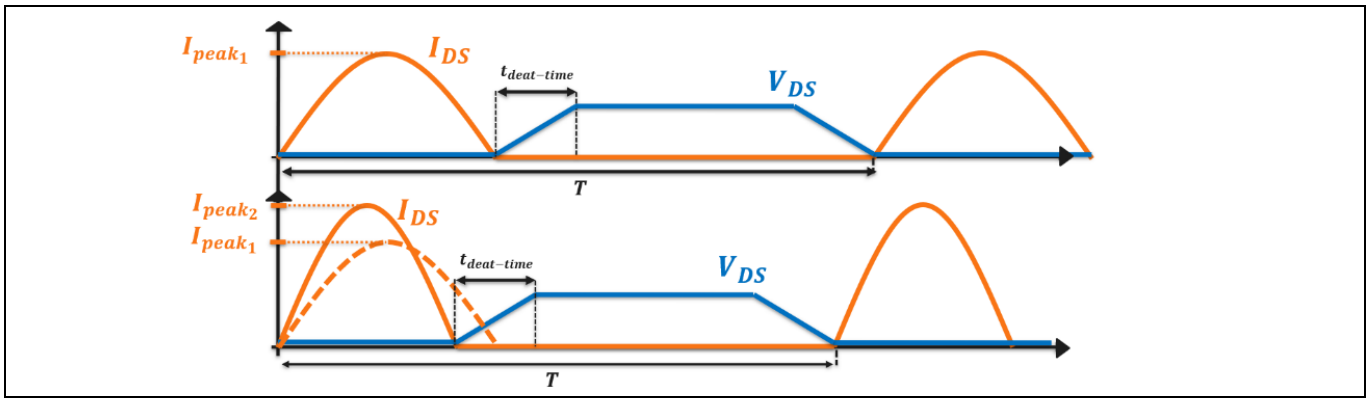


Figure 3 Effect of reduced switching period on current at constant dead-time

To achieve ZVS, when the MOSFET transitions from the OFF state to the ON state, its C_{oss} must first be discharged (that is, zero voltage between the drain and source). Only then can the MOSFET be turned ON. In topologies such as HSC or ZSC, the total Q_{oss} of the MOSFETs affects both the required dead-time and the magnetizing current. The magnetizing current stores energy during the ON phase and releases it during the dead-time interval, providing a constant current that charges and discharges the C_{oss} capacitors. A higher magnetizing current enables faster discharge of the C_{oss} capacitors, but it also increases inductor losses and temperature. Reducing the magnetizing current leads to reduction of core losses and can help to reduce the core volume. As frequencies increase, the trade-off between capacitance, magnetizing current, and dead time becomes critical.

3 Technical considerations for enhancing data center energy supply

As the power demands of data centers continue to increase, more efficient and compact power conversion solutions are required to enable substantial growth of capacity. However, this trend has created a trade-off challenge. On one hand, reducing converter size makes it increasingly difficult to dissipate the power losses effectively. On the other hand, converters with higher power density are desired to reduce the form factor in the system or increase output power while maintaining the same size.

Three main aspects can be identified for increasing power density: topology, packaging, and technology.

3.1 Topology: Requirements for power MOSFET technology and packaging

State-of-the-art power converters have already reached exceptional levels of efficiency, and further improvements are increasingly constrained by physical limitations and design requirements. New converter topologies are required to overcome the challenge of increasing power density while reducing form factor and maintaining or improving full-load efficiency within temperature limits. A possible solution at the topology level is to increase the switching frequency, which enables the size reduction of magnetic components. This extra space can be used to redesign the MOSFET routing and PCB layout, allowing an optimization of the conduction losses or to improve the design of the magnetic windings integrated into the PCB. To fully use the potential of a given topology, the characteristics of the power MOSFET must align with the specific requirements of that topology to maximize full-load efficiency.

3.2 Packaging: Source-down package

Traditional data centers rely on a 48 V ecosystem, using intermediate bus converters (IBCs) to convert the bus voltage to 12 V or lower. In this distribution system, the conversion to lower voltages result in higher output currents. As data center power consumption continues to grow, current levels will increase accordingly, leading to higher conduction losses in the system. Furthermore, the high currents flowing through the PCB contribute to increased temperatures, which in turn raise the resistance of conductive paths and can trigger the thermal runaway effect. To mitigate this effect, techniques such as active cooling and MOSFET paralleling, and as previously discussed, higher switching frequencies are employed. However, these techniques require a package that delivers the best performance to allow for optimal thermal dissipation, optimal paralleling, and switching accuracy.

In this scenario, source-down (SD) packages offer a better solution than traditional drain-down packages for the following reasons:

- Bigger die: SD packages allow the use of the given footprint area in the most effecting way, resulting in a lower total $R_{DS(ON)}$ allowing for higher current handling or reduced conduction losses (and therefore lower heat generation)
- Better thermal management: SD packages have a lower $R_{th_{JA}}$. These packages feature the dual-side cooling variant, which provides a thicker clip and full area contact to the drain for optimal heat transfer to the top
- Greater layout flexibility: SD center-gate packages enable easy MOSFET parallelling and facilitate PCB interconnection, resulting in uniform current distribution
- Reduced parasitic parameters:
  - SD packages have lower parasitic inductance (Ld + Ls is half that of drain-down packages and Lg is 1/100th that of drain-down packages). This results in faster transient switching and a more robust connection to the driver
  - SD packages have lower package resistance, reducing the contribution of the $R_{DS(on)}$ of the MOSFET

3.3 Technology: OptiMOS™ 7 40 V switching optimized

Power trench silicon MOSFETs have achieved a high level of performance, making further advances increasingly challenging. Nevertheless, silicon remains a highly competitive solution for applications with breakdown voltages below 60 V, offering an optimal balance between cost and performance. Furthermore, silicon technology continues to provide significant opportunities for optimization and innovation.

However, with silicon approaching its physical limits, wide-bandgap semiconductors such as GaN are emerging as promising alternative. It is important to note that, within the 48 V ecosystem (particularly in synchronous rectifiers (SR)), current management and distribution are key design considerations. This discussion regarding the further improvement of datacenter was intentionally divided into three distinct aspects, as topology, packaging, and technology are all critical and closely interconnected. Consequently, it is essential to integrate superior technology within an optimized package. [2].

As mentioned in Section 2.2.1, selecting MOSFETs for IBCs requires balancing charges (Q_{OSS} Q_G) specifically to optimize dead-time against $R_{DS(on)}$ to minimize conduction losses. In these topologies, MOSFETs with breakdown voltages below 60 V are typically used as synchronous rectifiers (SR). Because SRs are positioned near the output, they must handle high currents, and this might lead to elevated temperatures.

Reducing temperature is a primary design goal, as the local maximum temperature on the board defines the compliance limit and, consequently, the maximum output power of the system. SRs can operate at very high temperatures; a common solution to mitigate this high temperature is paralleling MOSFETs, which shift the thermal bottleneck from the SRs to the magnetic components (inductor/transformer cores). The 175°C thermal specification of the technology (such as OptiMOS™ 7 technology) provides a valuable operating margin to operate at higher junction temperatures, facilitating a design shift toward greater output power and more compact power density.

However, adding more MOSFETs conflicts with the original mentioned goal of increasing power density. Therefore, it is essential to use MOSFETs with lower $R_{DS(on)}$ to reduce the total number of them. For instance, in an IBC using four SRs in parallel, a 33% reduction of $R_{DS(on)}$ per MOSFET allows for a transition from four devices to three, freeing up 25% of the board space dedicated to SRs.

Another method to increase power density is to raise switching frequency to reduce the form factor of the magnetics. In this scenario, it becomes crucial to maintain or reduce total MOSFETs charge in the system. The new MOSFET must offer similar or lower charges.

For example, at a switching frequency of 200 kHz, a 50 ns dead-time accounts for 1% of the total period. At 1.2 MHz, the same dead-time accounts for 6%. Since a typical period includes two dead times, the contribution rises from 2% at 200 kHz to 12% at 1.2 MHz. This clearly shows how deadtime and Q_{OSS} becomes a critical parameter in the design phase.

Additionally, gate charge must be minimized, as higher switching frequencies lead to higher gate-driver power consumption. One way to reduce gate-driver power consumption is to reduce the voltage, for example, moving from 10 V to 6 V. To achieve this, it is important to prioritize the reduction of $R_{DS(on)}$ at lower values of V_{GS}.

OptiMOS™ 7 MOSFETs feature lower V_{GS} values due to a reduced Q_{gs} . While a lower Q_{gs} typically increases the Miller ratio, the OptiMOS™ 7 technology compensates by significantly reducing Q_{gd}.This maintains a low Miller ratio, resulting in excellent induced turn-on ruggedness, as discusses in the next section.

In conclusion, the goal for the new technology is to reduce the $R_{DS(on)}$ of the MOSFET at low V_{GS} while keeping the charges same as the previous generation.

3.3.1 OptiMOS™ 7 40 V induced turn-on ruggedness

Induced turn-on in a MOSFET refers to an unintended condition where a MOSFET switches as a result of external factors, rather than a deliberate signal applied to its gate terminal. This occurs when a MOSFET turning off induces a voltage spike of transient on the gate of the control MOSFET (because of parasitic capacitances like the gate-to-drain capacitance, C_{gd}). If this transient voltage exceeds the threshold voltage (V_{GSth}), the MOSFET may spuriously turn on. Comparing OptiMOS™ 6 and OptiMOS™ 7 MOSFETs in Table 3, it is notable that the V_{GSth} of OptiMOS™ 7 40 V MOSFET is lower than that of the OptiMOS™ 6 40 V MOSFET, providing advantages, as described in Section 3.3.

This technology allows the OptiMOS™ 7 40 V MOSFET to be used in hard-switching topologies while ensuring excellent transient behavior. To demonstrate this robustness, a buck converter circuit with the specifications shown in Figure 4 was used for testing.

V_{IN} [V]	V_{OUT} [V]	I_{OUT} [A]	F_{SW} [kHz]	Duty cycle [%]	DTon [sec]	V_{DS_LS} , V_{DS_HS} [V]	R_{G_LS} , R_{G_HS} [Ω]	L [uH]
24	12	5 & 25	500	50	50	10	0	4.7

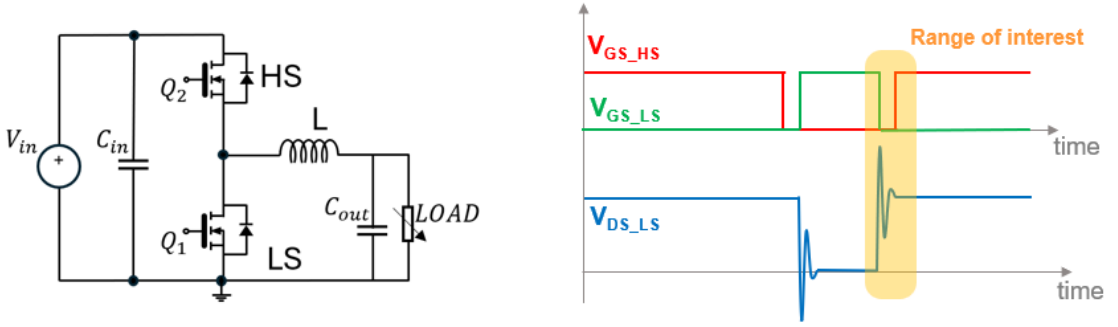


Figure 4 Buck converter and range of interest

The OptiMOS™ 6 40 V BSZ018N04LS6 MOSFET is used on the high side of the converter, while the OptiMOS™ 7 40 V MOSFET under analysis is used on the low side. To evaluate its robustness against induced turn-on, two tests with different output currents were chosen: I_{OUT}= 5 A and I_{OUT}= 25 A. These conditions were selected because the OptiMOS™ 7 40 V MOSFET reaches a temperature of 60°C in the first case (reducing the V_{GSth} by approximately 150 mV) and 115°C in the second case (reducing the V_{GSth} by about 400 mV), allowing the MOSFET to be tested under worst-case real-world conditions.

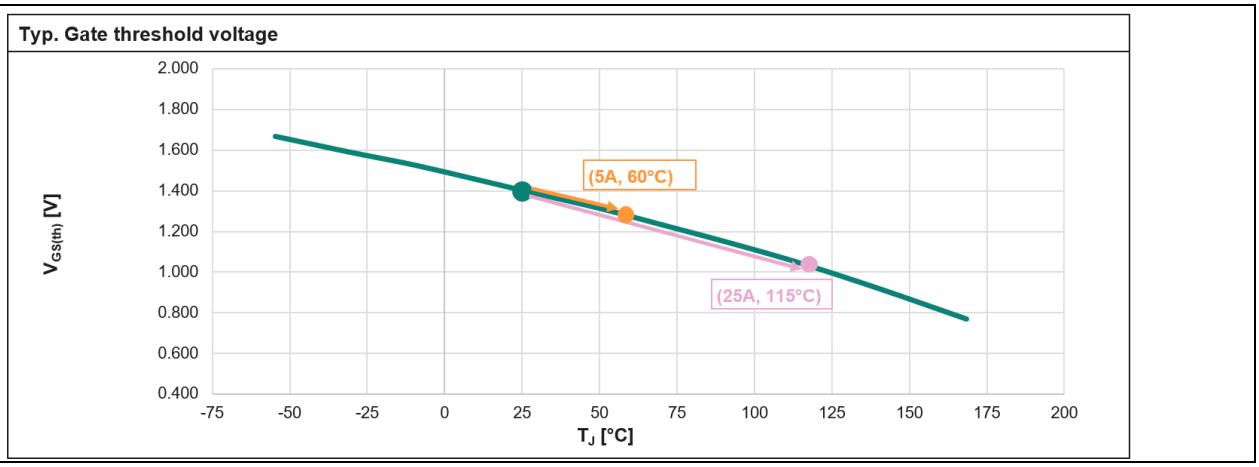


Figure 5 Gate threshold temperature variation

Additionally, three OptiMOS™ 7 40 V MOSFET variants with different V_{GSth} values were available. Two MOSFETs feature V_{GSth} values of 1.4 V and 1.2 V, which fall within the specified datasheet range. The third MOSFET features a V_{GSth} of 1.0 V, which is below the minimum datasheet specification of 1.1 V, to illustrate the exceptional robustness. This specific OptiMOS™ 7 variant (though not commercially available) is used to demonstrate the induced turn-on ruggedness, even beyond its rated limits, offering a robust operation margin in applications with fast voltage transients.

Table 1 40 V OptiMOS™ 7 MOSFET parameters

#	$R_{DS_{on}}$ at $V_{GS} = 4.5\ V$	$R_{DS_{on}}$ at $V_{GS} = 10\ V$	$V_{GS_{th}}$ at $I_D = 0.45\ mA$	Q_{gs} at $V_{DS} = 20\ V$	Q_{gd} at $V_{DS} = 20\ V$	Miller ratio Q_{gd}/Q_{gs}	Q_{oss} at $V_{DS} = 20\ V$	Q_g at $V_{DS} = 20\ V$
	(mΩ)	**(mΩ)**	**(V)**	**(nC)**	**(nC)**		**(nC)**	**(nC)**
1	1.08	0.96	**1**	6.23	3.91	0.63	47.4	40.9
2	1.12	0.67	**1.19**	7.12	4.01	0.56	46.4	40.7
3	1.04	0.83	**1.4**	6.54	4.2	0.64	40.6	43

Figure 6 shows that at both 60°C and 115°C, no induced turn-on occurs for any of the three curves. This demonstrates the exceptional robustness of this technology, even under elevated thermal conditions with impact on V_{GSth}, as shown in Figure 6.

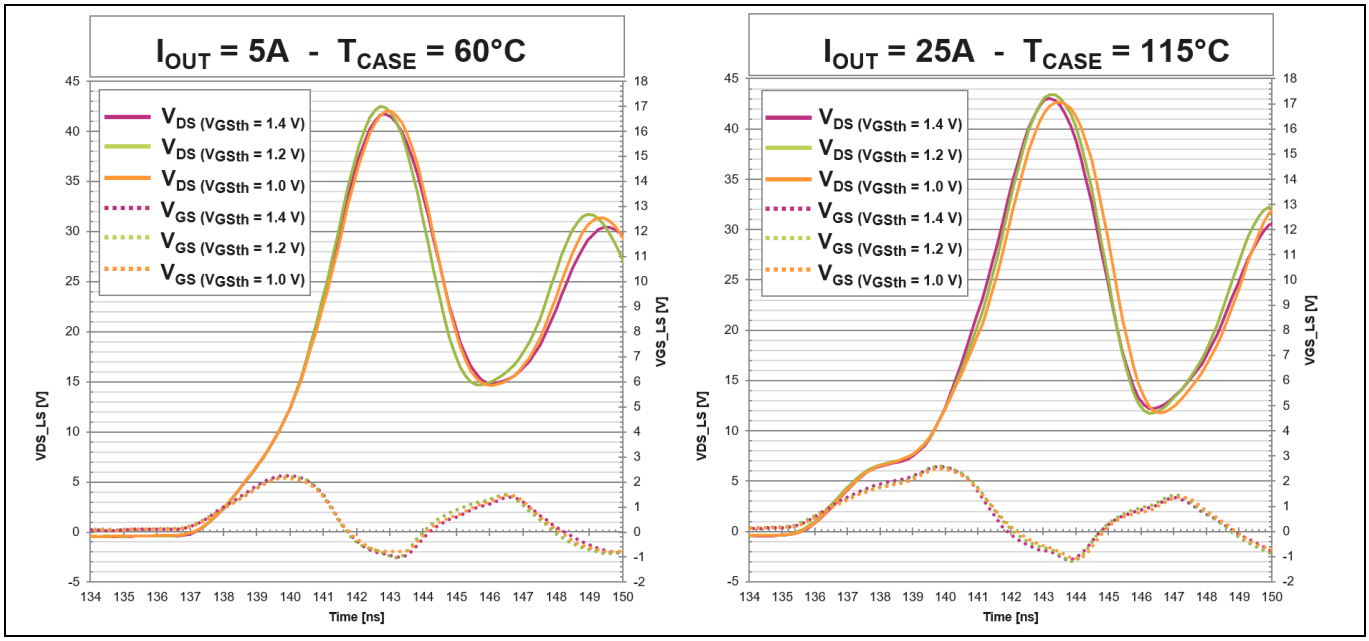


Figure 6 Inducted turn-on ruggedness: V_{DS} and V_{GS} waveform for different threshold voltage variants

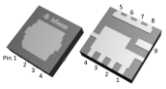
4 OptiMOS™ 7 40 V 3.3 × 3.3 source down – switching optimized

The new OptiMOS™ 7 40 V silicon MOSFET is specifically designed for high-frequency switching applications. The OptiMOS™ 7 40 V MOSFET is available in a 3.3 × 3.3 source-down package with a center gate footprint configuration in two variants: bottom-side cooled and top-side cooled.

Compared to the previous generation (OptiMOS™ 6 40 V MOSFET), this new MOSFET reduces the $R_{DS(on)4.5}$ by 33% while maintaining the low level of charges, particularly Q_{OSS}.

Table 2 summarizes the key parameters of the new OptiMOS™ 7 40 V technology in comparison to the OptiMOS™ 6 40 V.

Table 2 Datasheet comparison: OptiMOS™ 7 40 V application optimized versus OptiMOS™ 6 40 V

	$R_{DS_{on,max}}$ at $V_{GS} = 4.5\,V$ (mΩ)	$R_{DS_{on,max}}$ at $V_{GS} = 6\,V$ (mΩ)	$R_{DS_{on,max}}$ at $V_{GS} = 10\,V$ (mΩ)	$V_{GS_{th}}$ (V)	Q_{oss} at $V_{DS} = 20\,V$ (nC)	Q_g at $V_{DS} = 20\,V$ (nC)
OptiMOS™ 6 40 V IQE013N04LM6CGSC	1.9	1.5	1.35	1.6±0.4	45	41
OptiMOS™ 7 40 V IQE010N04LM7CGSC	1.2	1.1	1	1.4±0.3	43	39

Graphically, the comparison highlights the reduction in $R_{DS(on),typ}$ at low V_{GS} values. In fact, with the new OptiMOS™ 7 MOSFET, it is possible to have a typical $R_{DS(on),typ}$ at V_{GS} = 4.5 V that is lower than the typical $R_{DS(on)typ}$ at V_{GS} = 10 V of the OptiMOS™ 6 MOSFET.

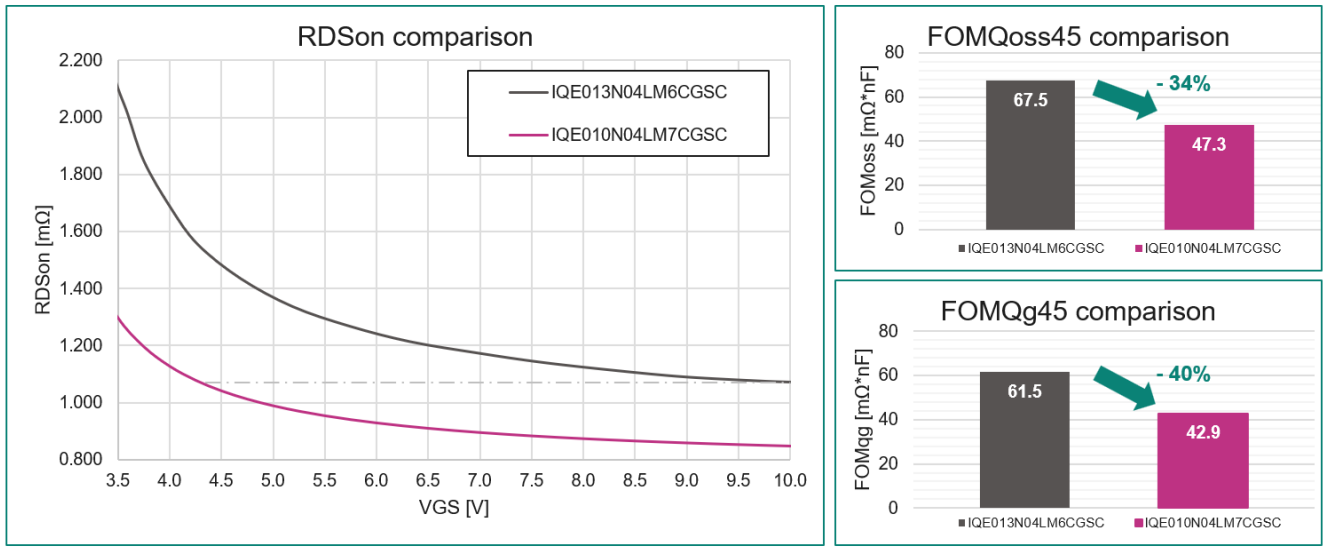


Figure 7 $R_{DS(on)}$ and FOM_{oss}/FOM_g graphical comparison between OptiMOS™ 6 40 V and OptiMOS™ 7 40 V MOSFETs

Due to significant reduction in $R_{DS(on)}$ and the slight decrease in the capacitance parameters, FOM_{oss} and FOM_g are reduced by 35% to 40% compared to the previous technology generation.

4.1 Performance benchmarking: SHSC

The OptiMOS™ 7 40 V power MOSFET was benchmarked in an SHSC topology (an unregulated, high-efficiency 4:1 soft-switching converter). The SHSC is a variation of the common HSC, offering improved current redistribution and more effective utilization of the autotransformer windings [3].

The converter operates at around 300 kHz with a gate-drive voltage of 7.2 V. Prior to measurement, the board was operated at full load for 30 minutes to reach thermal equilibrium. The load was then reduced by 2 A every 60 seconds to ensure highly accurate efficiency evaluation. No active cooling was used during the test.

Figure 8 displays the efficiency and power loss curves for the board. The only variable changed was the 40 V MOSFET generation, transitioning from OptiMOS™ 6 to OptiMOS™ 7. As illustrated, a simple drop-in replacement resulted in an efficiency improvement of 0.08% and a reduction in power losses of 0.82 W.

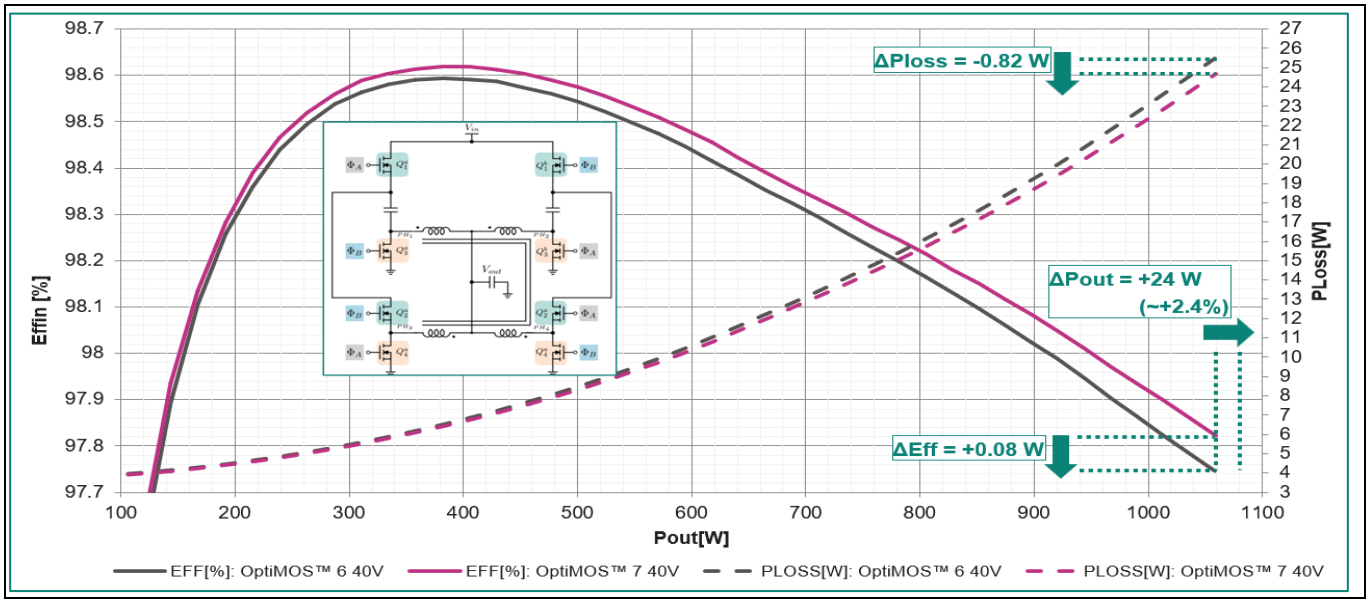


Figure 8 Efficiency and power losses comparison on SHSC topology

This reduction in power loss at a constant output power directly lowers the MOSFET temperature by approximately 2°C and the overall board temperature by about 3°C. Since the hottest point on the board is the magnetic core rather than the MOSFET, these lower operating temperatures allow the output power to be extended to a new thermal limit. In numerical terms, switching from OptiMOS™ 6 MOSFET to OptiMOS™ 7 MOSFET enables an increase in P_{OUT} of 24 W, representing a +2.4% increase in power capacity.

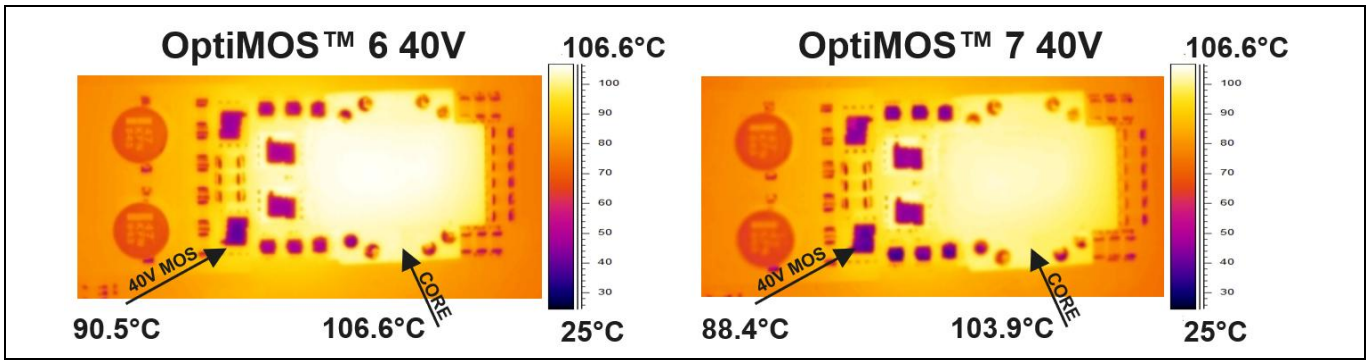


Figure 9 Temperature comparison on SHSC topology

4.2 Performance benchmarking: ZSC

The OptiMOS™ 7 40 V power MOSFET was benchmarked in a ZSC (zero-voltage-switching switched capacitor) topology, which is a high-efficiency, unregulated 2:1 soft-switching converter. Although typically not used as an IBC, this topology is valuable for evaluating MOSFET performance under high-frequency conditions and highlighting the benefits of this technology [4].

The converter operates at around 1200 kHz with a dead time of ~90 ns and a gate-drive voltage of 6.5 V. Before starting the measurement, the board was operated at full load for 15 minutes to reach thermal equilibrium. The load was then reduced by 2 A every 120 seconds to ensure a highly accurate efficiency evaluation. No external cooling was applied to the board during testing.

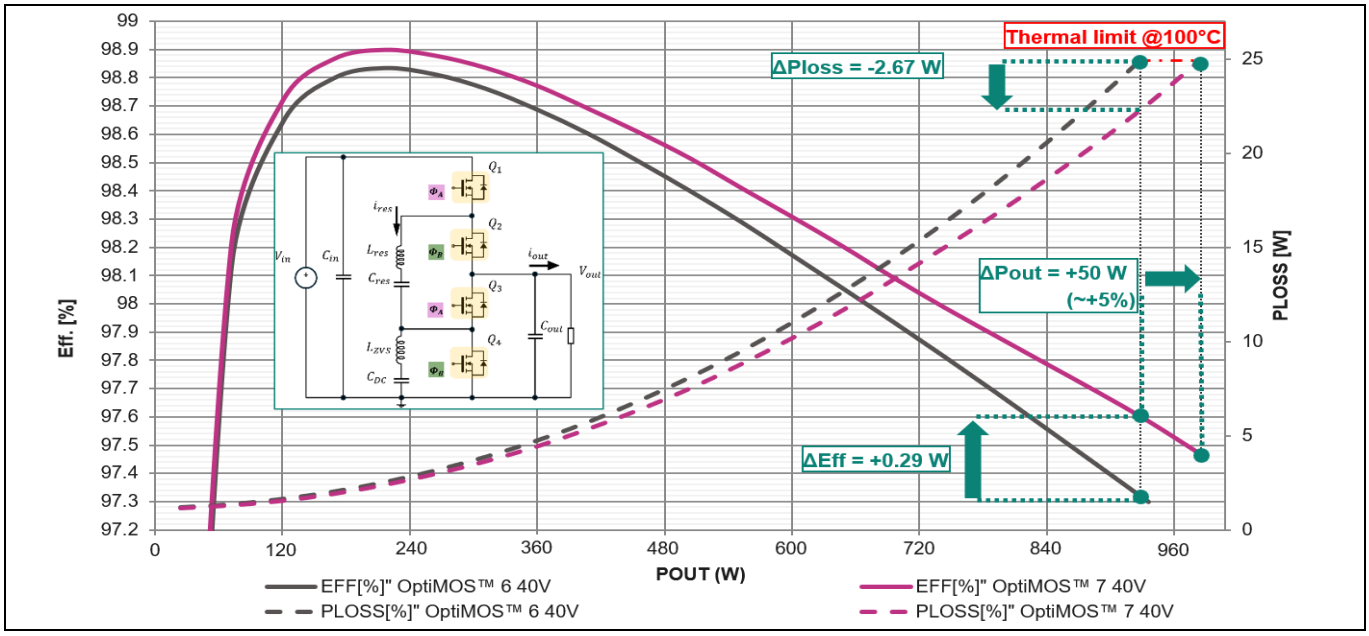


Figure 10 Efficiency and power loss comparison on ZSC topology

As in the previous benchmark, the reduction in losses compared to the OptiMOS™ 6 40 V MOSFET results in a board temperature reduction of almost 7°C. Due to this thermal improvement, the maximum output power rating can be increased by 5% for reaching compliance temperature of 110°C.

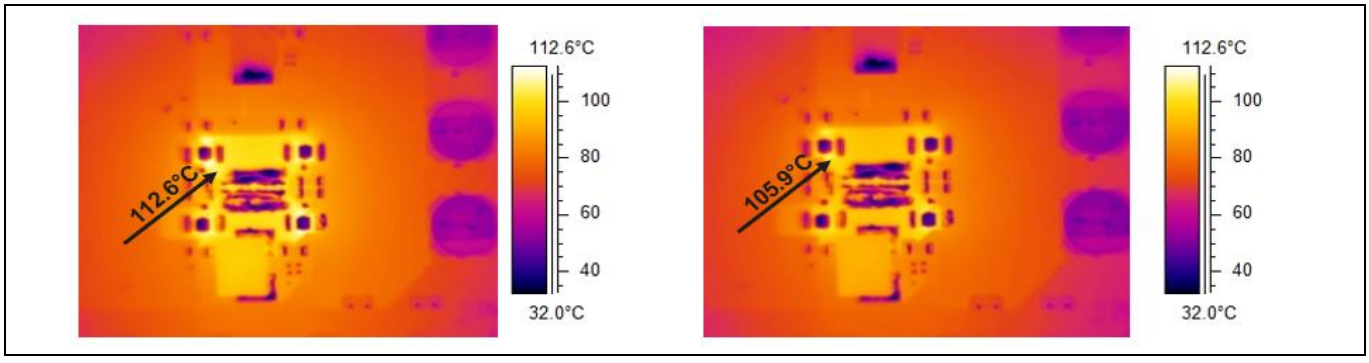


Figure 11 Temperature comparison on ZSC topology

In this board, the impact of the new OptiMOS™ 7 40 V MOSFET is even more significant due to the topology because the MOSFETs are the bottleneck in the system. Consequently, a variation in the device performance leads to a substantial improvement in the overall board performance. In the following section, reduction of body diode conduction will be presented.

4.2.1 ZSC body diode conduction time

Section 4.2 presents a comparison between OptiMOS™ 6 and OptiMOS™ 7 MOSFETs under equivalent operating conditions. This specific topology highlights the significant impact of output charge (Q_{OSS}) on converter performance, particularly at high frequencies. At 1200 kHz, the switching period is exceptionally short (~830 ns). As detailed in Section 2.2.1, because the period consists of both active-time and dead-time, reducing Q_{OSS} allows for a shorter dead-time and a longer active-time, which directly enhances efficiency.

As shown in Table 2, OptiMOS™ 7 MOSFET offers both lower $R_{DS(on)}$ and lower Q_{OSS} than OptiMOS™ 6 MOSFET. To isolate the specific impact of Q_{OSS}, the previous test was repeated using body diode conduction time parity rather than constant dead-time. To improve measurement repeatability and minimize experimental error, a relatively long body diode conduction time of 13 ns was selected as the reference.

Figure 12 shows the V_{DS} and V_{GS} waveforms. The V_{DS} traces (solid lines) clearly show differing slopes during the transition. The first test was performed at constant dead-time of 90 ns (first two curves from the left): the OptiMOS™ 7 MOSFET discharges faster due to its lower Q_{OSS}, resulting in a body diode conduction time of ~25 ns. In the second test, the dead-time is reduced by 10 ns, allowing the OptiMOS™ 7 MOSFET (the curve on the right) to match the 13 ns conduction time of the OptiMOS™ 6 MOSFET, fully using the lower Q_{oss}.

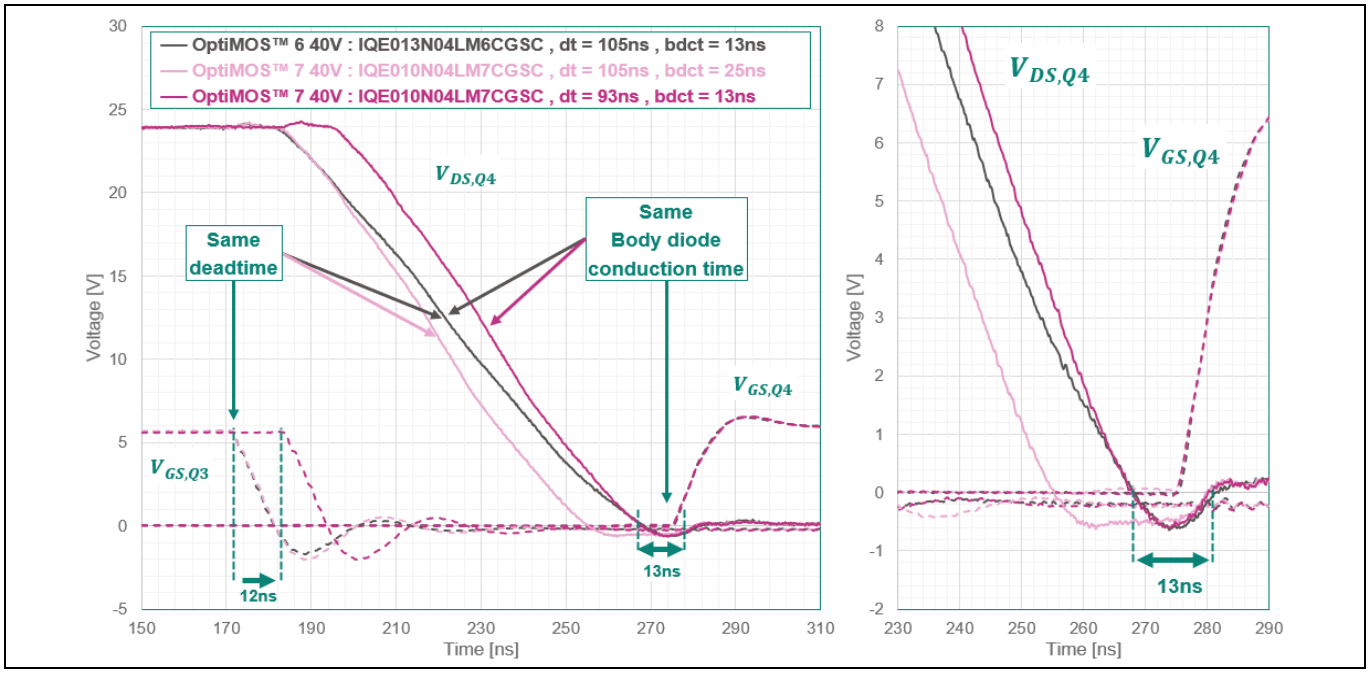


Figure 12 Waveform comparison between OptiMOS™ 6 40 V and OptiMOS™ 7 40 V MOSFETs with the same dead-time (dt) and the same body diode conduction time (bdct). The dark gray curve indicates OptiMOS™ 6 MOSFET, light purple indicates OptiMOS™ 7 MOSFET with the same dead-time (dt), and dark purple identifies OptiMOS™ 7 MOSFET with the same body diode conduction time

Maintaining a constant body diode conduction time while increasing the active-time reduces the RMS current for the same output current, further lowering conduction losses.

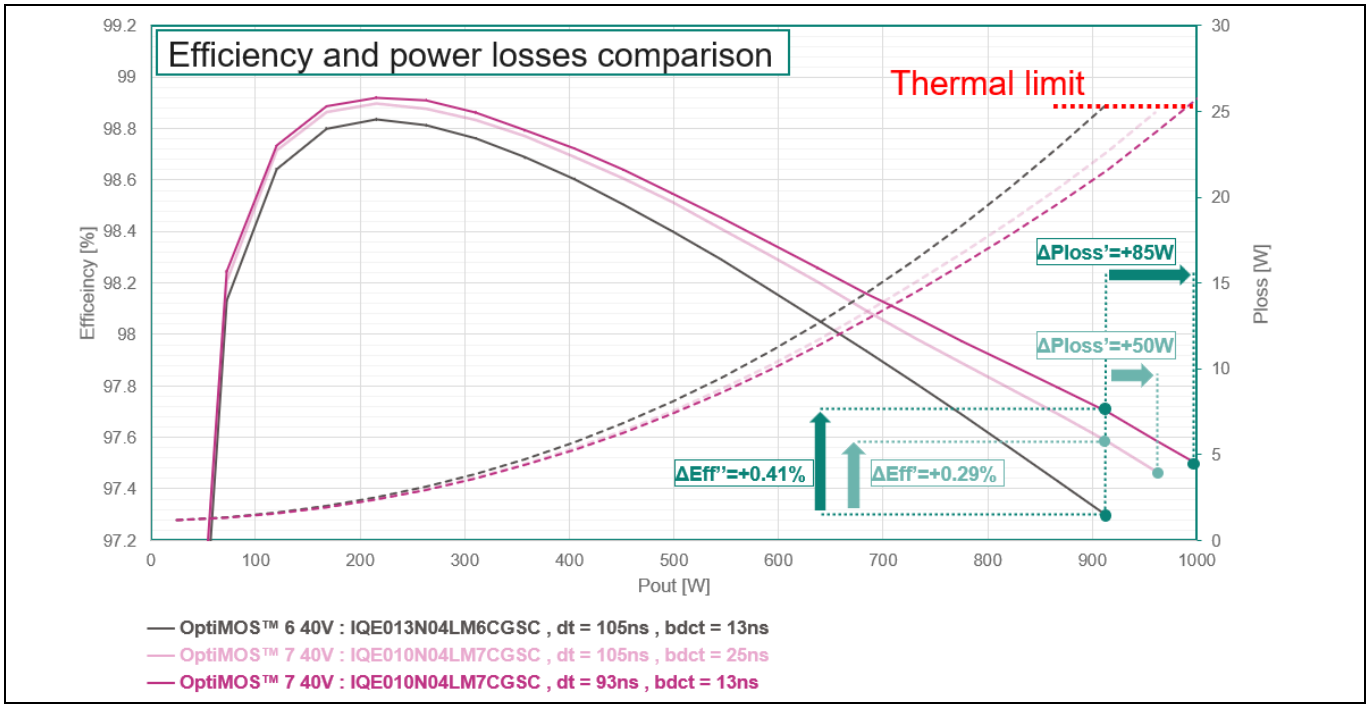


Figure 13 Efficiency and power losses comparison on ZSC topology with the same dead-time (dt) and the same body diode conduction time (bdct)

This dead-time adjustment enables a reduction in power losses (P_{loss}) at a constant output power or, conversely, allows for higher output power at the same P_{loss} level. By utilizing the new OptiMOS™ 7 MOSFET, the output power can be increased by 85 W, representing a +9.4% improvement. At an output current of 39 A, efficiency increases by 0.41%, while the MOSFET operating temperature is reduced by approximately 9°C.

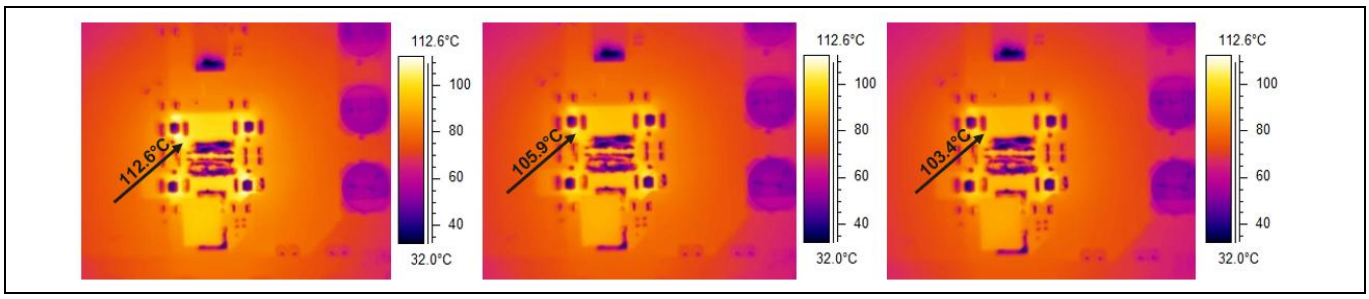


Figure 14 Temperature comparison on ZSC topology with the same dead-time (dt) and the same body diode conduction time (bdct)

This demonstrates that the reduction in Q_{OSS} directly enables a measurable improvement in overall efficiency. Nonetheless, the OptiMOS™ 7 MOSFET offers a 33% improvement in $R_{DS(ON)45}$, significantly reducing conduction losses. Therefore, it provides a good balance between $R_{DS(ON)}$ and Q_{oss}. Further, operation at V_{GS} = 6.5 V gives an extra reduction of gate losses while having the full benefit of a low $R_{DS(ON)}$.

5 OptiMOS™ 7 40 V 5×6 drain down – switching optimized

The new OptiMOS™ 7 40 V silicon MOSFET is available in a 5 × 6 drain-down, top-side cooled package.

Compared to its predecessor OptiMOS™ 6 40 V MOSFET, for the 5 × 6 drain-down package, the new OptiMOS™ 7 40 V MOSFET comes with same $R_{DS(on)}$ with improved charges.

Table 3 shows the key parameters of the new OptiMOS™ 7 40 V MOSFET compared to the previous generation.

Table 3 Datasheet comparison: OptiMOS™ 7 40 V application optimized vs. OptiMOS™ 6 40 V MOSFET

	$R_{DS_{on,max}}$ at $V_{GS} = 4.5\ V$ (mΩ)	$R_{DS_{on,max}}$ at $V_{GS} = 10\ V$ (mΩ)	$V_{GS_{th}}$ (V)	Q_{oss} at $V_{DS} = 20\ V$ (nC)	Q_{g45} at $V_{DS} = 20\ V$ (nC)
OptiMOS™ 6 40 V BSC007N04LS6SC	0.9	0.7	1.8±0.5	103	45
OptiMOS™ 7 40 V ISCH69N04LM7SC	0.9	0.69	1.4±0.3	78	32

Graphically, the comparison highlights the reduction of charge values while keeping $R_{DS(on)}$ constant.

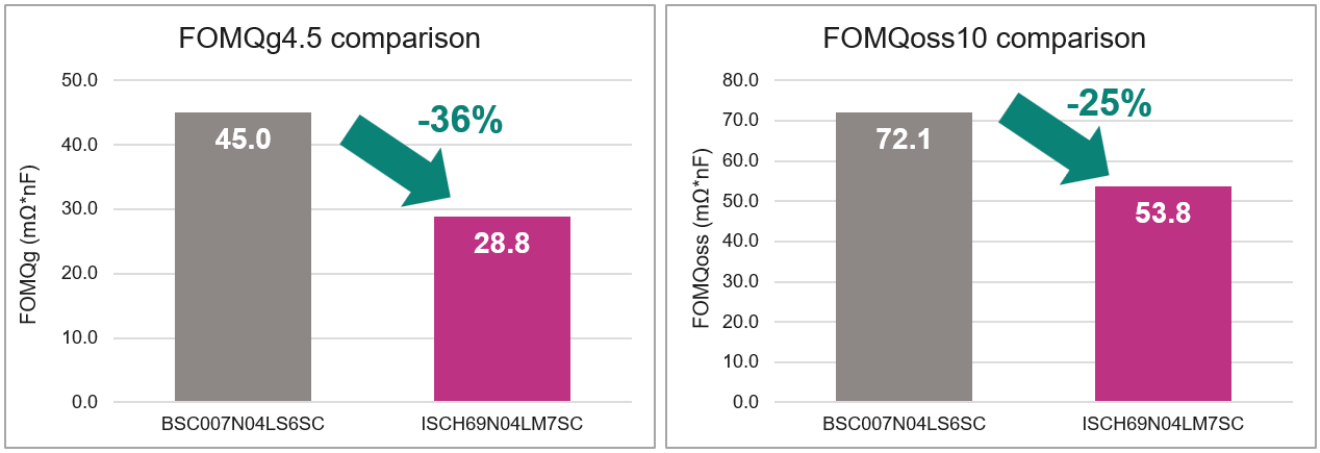


Figure 15 $R_{DS(ON)}$ and FOM_{oss}/FOM_g graphical comparison between OptiMOS™ 6 40 V MOSFET and OptiMOS™ 7 40 V MOSFET

Due to the reduction in charges and the slight decrease in $R_{DS(on)}$, FOM_{oss}, and FOM_g have improved by 27% compared to the previous product.

5.1 Benchmarking: HVIBC

The OptiMOS™ 7 40 V MOSFET in the 5×6 package was benchmarked in a 6 kW HVIBC (high-voltage Intermediate bus converter) topology, an unregulated, high-efficiency soft-switching converter with a 64:1 transformation ratio. The design utilizes a half-bridge center-tapped (HBCT) configuration. This converter is engineered to deliver high power directly to the load while maintaining manageable current levels, stepping down an 800 V input to a 12 V output [5].

To deliver the rated output current of 500 A, 32 MOSFETs are utilized on the secondary side. This high component count makes the system sensitive to total Q_{OSS} (affecting zero-voltage switching) and total Q_G (impacting gate-driver stress).

The operating frequency is around 750 kHz with a secondary-side gate-drive voltage of 5.7 V, which highlights the benefit of the $R_{DS(ON)45}$ optimization of OptiMOS™ 7 40 V to minimize charges at low V_{GS} values.

Prior to testing, the board was operated at full load (6 kW/500 A) for 15 minutes to reach thermal equilibrium. The load was then decreased by 10 A every 15 seconds to ensure a high-precision efficiency evaluation. A water-cooling system was employed to maintain stable thermal conditions during the test.

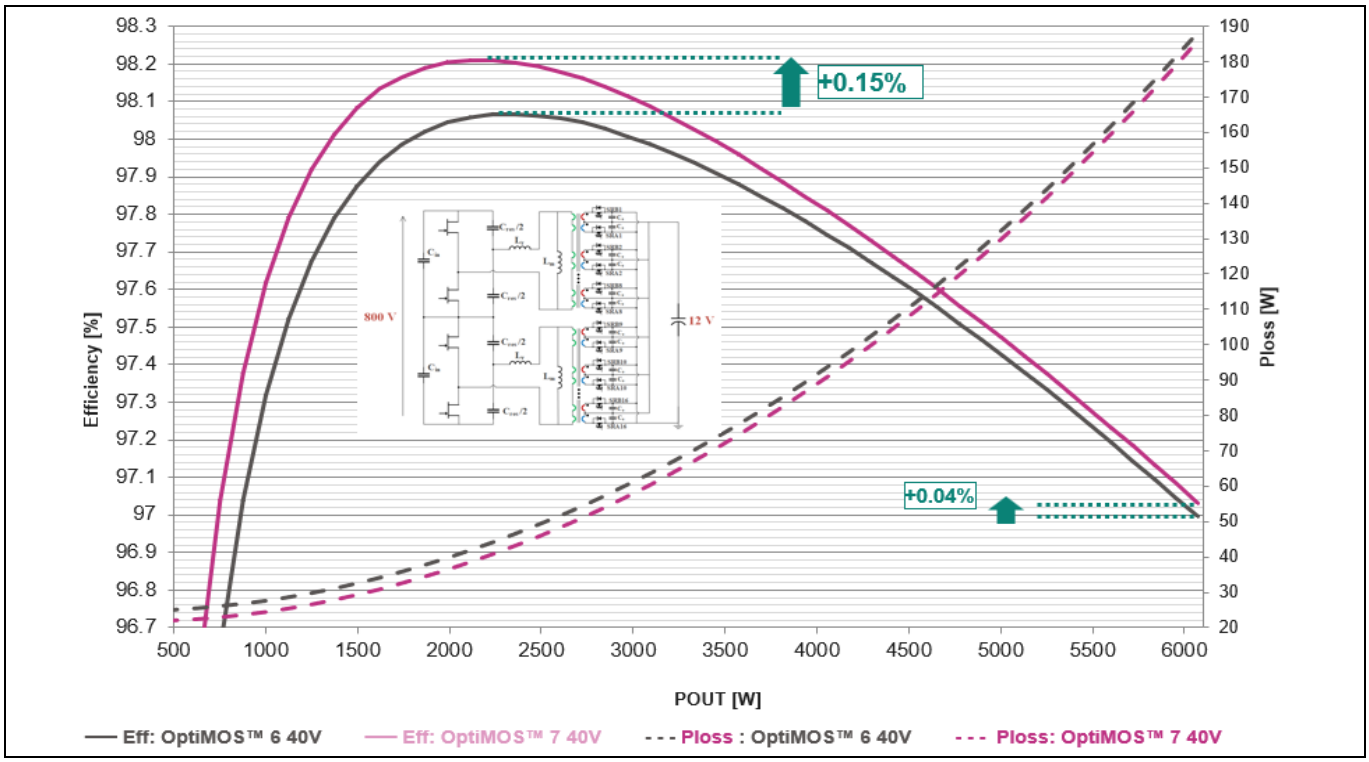


Figure 16 Efficiency and power losses comparison on HVIBC topology

Due to time constraints, this test was conducted only for one dead-time setting, even though the lower total Q_{OSS} of the OptiMOS™ 7 MOSFET would have permitted a dead-time reduction to further lower conduction losses and increase efficiency. The efficiency improvement shown in Figure 16 results from the reduced power dissipation in the gate drivers, that since OptiMOS™ 7 MOSFET requires less charges, the gate drivers are under less stress and so under less temperature. This temperature difference contributes to a lower $R_{DS(on)}$, reducing power conduction. However, as the system is water-cooled, the MOSFETs temperature reading was not accessible but the temperature of the board at full load was around 90°C.

6 Datasheet comparison: OptiMOS™ 6 40 V vs. OptiMOS™ 7 40 V MOSFETs

Table 1 and Table 2 provide a side-by-side comparison between Infineon's latest silicon trench MOSFET technology OptiMOS™ 7 40 V, and its predecessor, OptiMOS™ 6 40 V MOSFET in both package-dimension variants, 3.3 × 3.3 mm^2 and 5 × 6 mm^2.

Table 4 Datasheet comparison: OptiMOS™ 7 40 V MOSFET switching optimized vs. OptiMOS™ 6 40 V MOSFET in 3.3×3.3 mm^2 package dimension

3.3 × 3.3 mm^2 PQFN SD BSC **3.3 × 3.3 mm^2 PQFN SD DSC**	V_{GS} (V)	$V_{GS_{th}}$ (V)	$R_{DS(on),max}$ at $V_{GS}=4.5\,V$ (mΩ)	$R_{DS(on),max}$ at $V_{GS}=10\,V$ (mΩ)	[1]Miller ratio Q_{gd}/Q_{gs}	$FOMQ_{oss}$ at $V_{DS}=20\,V$ (nC mΩ)	$FOMQ_g$ at $V_{DS}=20\,V$ (nC mΩ)
OptiMOS™ 7 40 V							
IQE010N04LM7CG	±16	1.4	1.3	1.0	0.55	[2]55.9/[3]43	[4]24.6/[5]39
IQE010N04LM7CGSC		±03	1.3	1.0	0.55	[2]55.9/[3]43	[4]24.6/[5]39
OptiMOS™ 6 40 V – reference							
IQE013N04LM6CG	±20	1.6	1.9	1.35	0.71	[2]85.5/[3]60.8	[4]38/[5]55.4
IQE013N04LM6CGSC		±04	1.9	1.35	0.68	[2]85.5/[3]60.8	[4]38/[5]55.4

Table 5 Datasheet comparison: OptiMOS™ 7 40 V MOSFET switching optimized vs. OptiMOS™ 6 40 V MOSFET in 5×6 mm^2 package dimension

5 × 6 mm^2 SuperS08 SD BSC **5 × 6 mm^2 SuperS08 SD**	V_{GS} (V)	$V_{GS_{th}}$ (V)	$R_{DS_{on,max}}$ at $V_{GS}=4.5\,V$ (mΩ)	$R_{DS_{on,max}}$ at $V_{GS}=10\,V$ (mΩ)	[1]Miller ratio Q_{gd}/Q_{gs}	$FOMQ_{oss}$ at $V_{DS}=20\,V$ (nC ·mΩ)	$FOMQ_g$ at $V_{DS}=20\,V$ (nC ·mΩ)
OptiMOS™ 7 40 V							
ISCH69N04LM7SC	±12	1.4 ±0.3	0.9	0.69	0.37	[2]70.2/[3]53.8	[4]28.8/[5]47.6
ISC011N04LM7SC			1.45	1.1	0.37	71.1/53.9	29.0/47.3
OptiMOS™ 6 40 V – reference							
BSC007N04LS6SC	±20	1.8 ±0.4	1	0.7	0.66	[2]103.0/[3]72 1	[4]45/[5]65.8

[1] $Q_{gd,typ}$ /$Q_{gs,typ}$
[2] $R_{DSon45(max)}$ • $Q_{OSS(typ)}$
[3] $R_{DSon10(max)}$ • $Q_{OSS(typ)}$
[4] $R_{DSon45(max)}$ • $Q_{g45(typ)}$
[5] $R_{DSon10(max)}$ • $Q_{g10(typ)}$

7 Summary

The OptiMOS™ 7 40 V switching optimized MOSFET represents Infineon's latest trench MOSFET technology, offering improved figures of merit (FOM) that enable enhanced application performance through higher efficiency and lower operating temperatures. This technology is available in two packages (3.3 × 3.3 mm^2 and 5 × 6 mm^2) and improves the performance of IBCs by addressing various key characteristics, especially for high-frequency soft-switching converters with low driving voltages.

8 Related resources

- OptiMOS™ 7 switching optimized
- Developer Community

References

[1] Infineon Technologies AG: *We power AI - online media briefing*; Available online

[2] Infineon Technologies AG: *Source-down PQFN*; Available online

[3] Infineon Technologies AG: *Hybrid switched-capacitor converter (HSC)*; Available online

[4] Infineon Technologies AG: *Zero-voltage-switching switched capacitor converter (ZSC) IBC*; Available online

[5] Infineon Technologies AG: *Power Conversion Solutions for Future Server Boards Operating Directly from High-Voltage DC*; Available online

Revision history

Document revision	Date	Description of changes
V 1.0	2026-08-13	Initial release

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition: 2026-08-13

Published by
Infineon Technologies AG
Am Campeon 1-15
85579 Neubiberg, Germany

© 2026 Infineon Technologies AG.
All rights reserved

Do you have a question about this document?
Email: erratum@infineon.com

Document reference:
AN151047

Important Notice

Products which may also include samples and may be comprised of hardware or software or both ("Product(s)") are sold or provided and delivered by Infineon Technologies AG and its affiliates ("Infineon") subject to the terms and conditions of the frame supply contract or other written agreement(s) executed by a customer and Infineon or, in the absence of the foregoing, the applicable Sales Conditions of Infineon. General terms and conditions of a customer or deviations from applicable Sales Conditions of Infineon shall only be binding for Infineon if and to the extent Infineon has given its express written consent.

For the avoidance of doubt, Infineon disclaims all warranties of non-infringement of third-party rights and implied warranties such as warranties of fitness for a specific use/purpose or merchantability.

Infineon shall not be responsible for any information with respect to samples, the application or customer's specific use of any Product or for any examples or typical values given in this document.

If this document is marked as 'Preliminary', 'Target', 'Draft' or 'Proposal', Infineon reserves the right to change all information given in this document at any time without notice. Subject to the development and release of a Product for series supply by Infineon, the technical specifications of the Product are set forth in the relevant datasheet provided by Infineon without such marking.

The data contained in this document is exclusively intended for technically qualified and skilled customer representatives. It is the responsibility of the customer to evaluate the suitability of the Product for the intended application and the customer's specific use and to verify all relevant technical data contained in this document in the intended application and the customer's specific use. The customer is responsible for properly designing, programming, and testing the functionality and safety of the intended application, as well as complying with any legal requirements related to its use.

Unless otherwise explicitly approved by Infineon, Products may not be used in any application where a failure of the Products or any consequences of the use thereof can reasonably be expected to result in personal injury. However, the foregoing shall not prevent the customer from using any Product in such fields of use that Infineon has explicitly designed and sold it for, provided that the overall responsibility for the application lies with the customer.

Infineon expressly reserves the right to use its content for commercial text and data mining (TDM) according to applicable laws, e.g. Section 44b of the German Copyright Act (UrhG).

If the Product includes security features:
Because no computing device can be absolutely secure, and despite security measures implemented in the Product, Infineon does not guarantee that the Product will be free from intrusion, data theft or loss, or other breaches ("Security Breaches"), and Infineon shall have no liability arising out of any Security Breaches.

If this document includes or references software:
The software is owned by Infineon under the intellectual property laws and treaties of the United States, Germany, and other countries worldwide. All rights reserved.

Therefore, you may use the software only as provided in the software license agreement accompanying the software.

If no software license agreement applies, Infineon hereby grants you a personal, non-exclusive, non-transferable license (without the right to sublicense) under its intellectual property rights in the software (a) for software provided in source code form, to modify and reproduce the software solely for use with Infineon hardware products, only internally within your organization, and (b) to distribute the software in binary code form externally to end users, solely for use on Infineon hardware products. Any other use, reproduction, modification, translation, or compilation of the software is prohibited.

For further information on the Product, technology, delivery terms and conditions, and prices, please contact your nearest Infineon office or visit https://www.infineon.com.