Innovative “Source Down” technology

About this document

Scope and purpose

This application note is intended to explain the new “Source Down” power package.

It shows its differences from the industry’s standard “Drain Down” concept and offers detailed information about the advantages of this concept. Examples demonstrate how to get the optimum performance from this technology.

A separate chapter concentrates on design-in recommendations with layout proposals.

Intended audience

Power electronic designers

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1 Introduction to “Source Down” technology

New packages are developed and introduced to the market every few years. The main requirement of a new package is always more or less the same: it should be very small, able to contain maximum chip area with a minimum of package parasitics (especially ohmic resistance). With the PQFN 3.3 x 3.3 a very good solution (with a massive source clip instead of bond wires) was introduced years ago. Step-by-step optimization has already led to very low-ohmic devices, e.g. down to 0.9 mΩ in 25 V.

Without changing the mechanical concept a further reduction in $R_{DS(on)}$ was only possible with a new silicon generation.

The “Source Down” concept is not only a “flip chip”. The complete package was optimized. The chance was taken to optimize the chip and also the clip, resulting in a lower $R_{DS(on)}$ and also in a significantly reduced thermal resistance R_{thJC}. Together with the increased maximum continuous and pulsed drain currents I_D (see Table 1) the electronic engineer is now able to increase the power density of the design dramatically. Additional measurements will be available soon.

It is now possible to replace a Super SO8 (30mm^2 PCB area) with a “Source Down” in PQFN 3.3 x 3.3 (10 mm^2) resulting in an even better performance.

Advantages of the “Source Down” concept at a glance:

- Lower $R_{DS(on)}$
- Lower R_{thJC}
- Layout advantages (see chapter 2.2)

In the following chapters the differences from the (standard) “Drain Down” concept are shown, along with their impact on some applications.

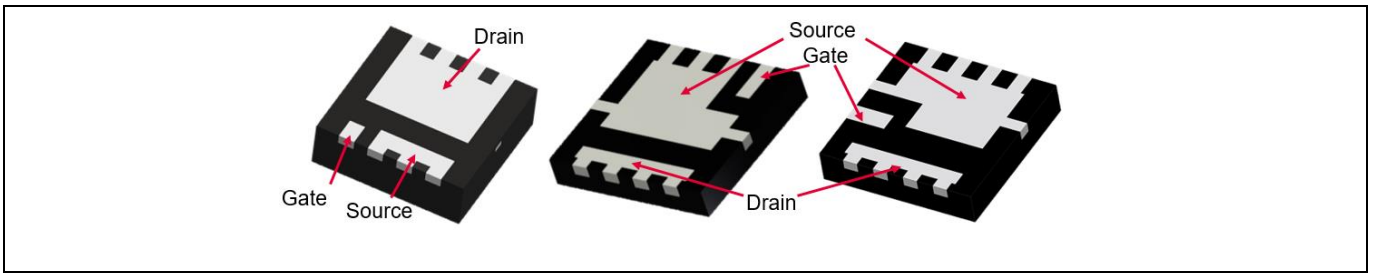


Figure 1 “Drain Down” (left), “Source Down Standard Gate” (center) and “Source Down Center Gate”

Figure 1 shows the “Drain Down” on the left and two different available “Source Down” versions. With the “Center Gate” (right picture) it’s much easier to connect devices in parallel. An increased creepage distance of 0.75 mm between drain and source/gate enables routing of the gate signal between these contacts, connecting all gate pads without the need for another PCB layer. More details are shown in chapter 2.1.2.

2 “Drain Down” vs. “Source Down” concept

To understand the differences between the “Drain Down” and “Source Down” concepts, it’s helpful to have a closer look at a modern power MOSFET.

Figure 2 shows on the left a section through a trench MOSFET. The silicon chip is soldered onto the copper lead-frame. On top the bond wires are connected to the source metalization of the chip. A detail picture on the right shows the “trenches”, the only active region of the MOSFET. The losses created here must pass the complete silicon chip on their way to the copper lead-frame and the PCB.

In a “Source Down” MOSFET the silicon die is flipped and the metalization of the active region (the “trenches”) is connected directly to the lead-frame, resulting in a much better thermal resistance R_{thJC} (see Table 1).

Additionally the design of the copper clip (drain contact) was optimized, resulting in a lower package resistance and $R_{DS(on)}$.

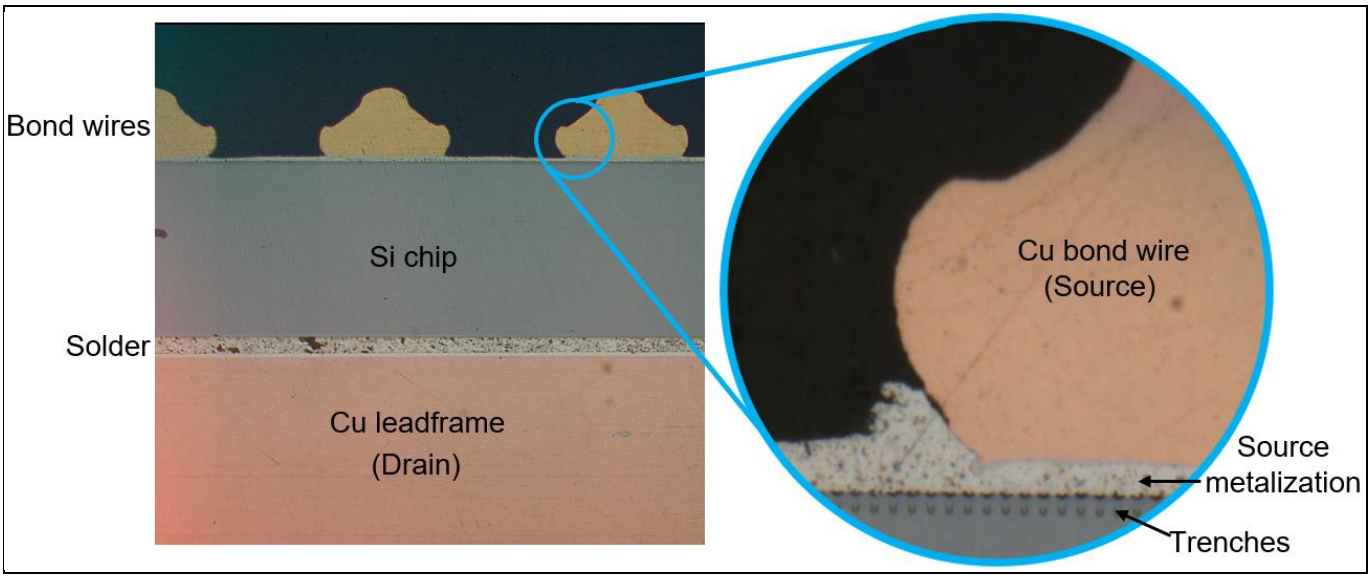


Figure 2 Section through a bonded power MOSFET (detail on the right) in “Drain Down” configuration

2.1 Comparison key parameters in 25 V

2.1.1 Main device parameters

Table 1 shows a comparison between the new IQE006NE2LM5 and IQE006NE2LM5CG and two different existing solutions in PQFN 3.3 x 3.3. The BSZ009NE2LS5 was $R_{DS(on)}$ optimized for ORing, the BSZ010NE2LS5 for switched applications (low charges). The “Source Down” technology combines the advantages in one package: a very low $R_{DS(on)}$ with low charges.

Table 1 Comparison of main device parameters

Parameter	BSZ009NE2LS5	BSZ010NE2LS5	IQE006NE2LM5 IQE006NE2LM5CG
$R_{DS(on),max}$	0.9 mΩ	1.0 mΩ	**0.65 mΩ**
$I_{D,cont}$	40 A	40 A	**298 A**
$I_{D,pulse}$	160 A	160 A	**1192 A**
FOM_G	64.4 nC*mΩ	35.6 nC*mΩ	**30.85 nC*mΩ**
R_{thjC}	1.8 K/W	1.8 K/W	**1.4 K/W**

2.1.2 Increased creepage distance source/drain

The Center Gate version comes with an increased creepage distance from drain to source, making parallelization of devices possible without the need for another layer for the gate signal. For details see chapter 2.2.2.

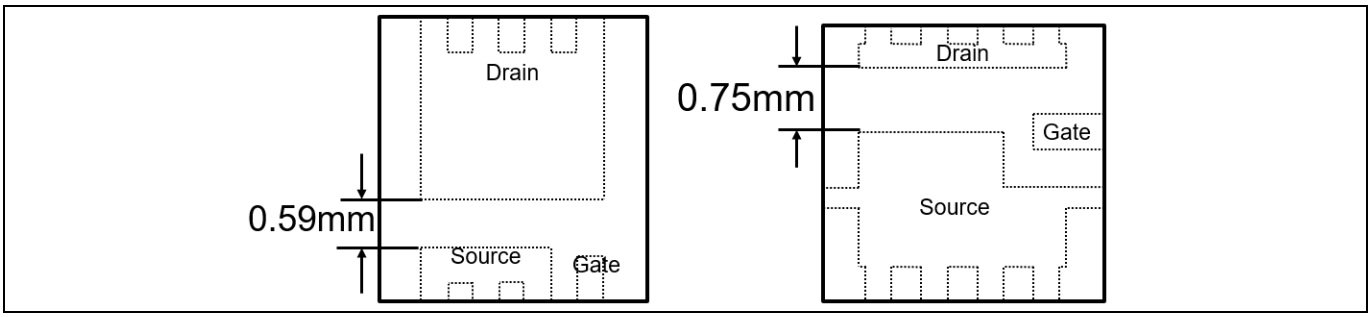


Figure 3 0.75 mm creepage distance source/gate to drain vs. 0.59 mm allows routing between the pads on the same layer

2.2 Layout optimization with “Source Down”

2.2.1 Thermal management optimization

In applications where the drain is connected to the switched node (e.g. the low-side MOSFET in a buck converter or synchronous rectifiers on the SMPS’s secondary side) it’s not recommended or even not allowed to connect the drain pad to a large copper area, acting as a heatsink. In this case the only way to get rid of the losses is via the source copper clip and then to the ground plane (Figure 4, upper picture).

With the “Source Down” the thermal management in ground-referenced set-ups is much easier. Source can be connected to all ground planes via thermal vias, resulting in a much better heat transfer to the ambient.

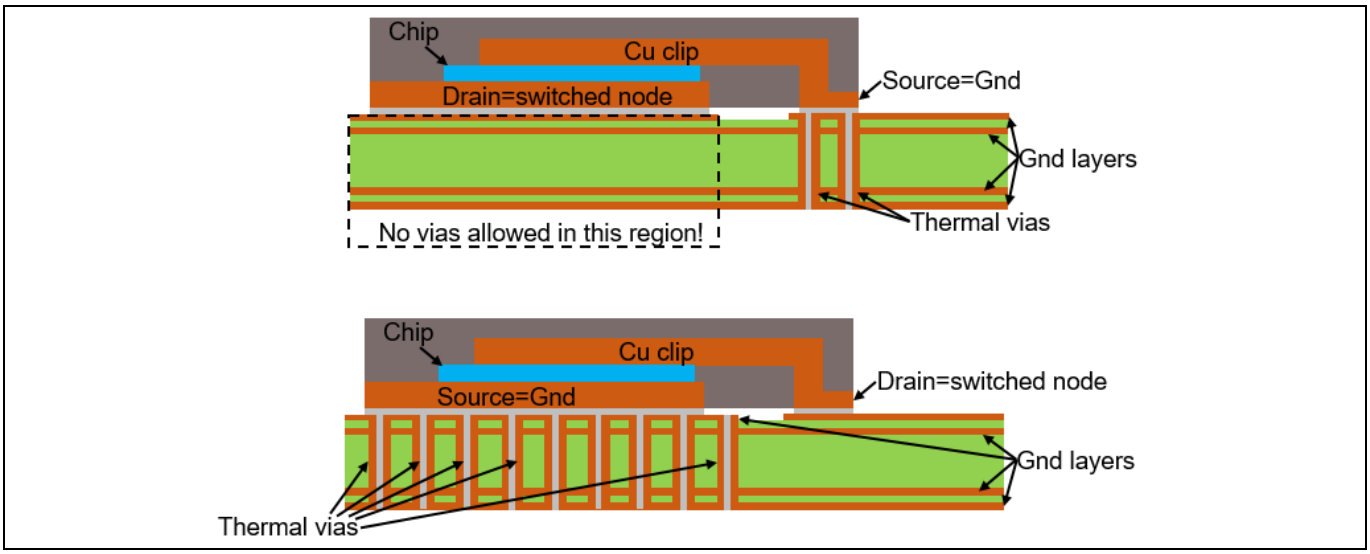


Figure 4 Thermal management with “Drain Down” (top) and “Source Down” (bottom)

2.2.2 Paralleling made easy

Reducing $R_{DS(on)}$ further requires a parallelization of devices. With “Drain Down” the distance from drain to source is not high enough to route the gate signal under the device. It is necessary to use another PCB layer to connect the gates together (Figure 5, left, gate signal in blue). The “Center Gate” variant with its creepage distance (drain to source) of 0.75 mm offers the possibility to route the gate signal of paralleled devices without the use of another layer.

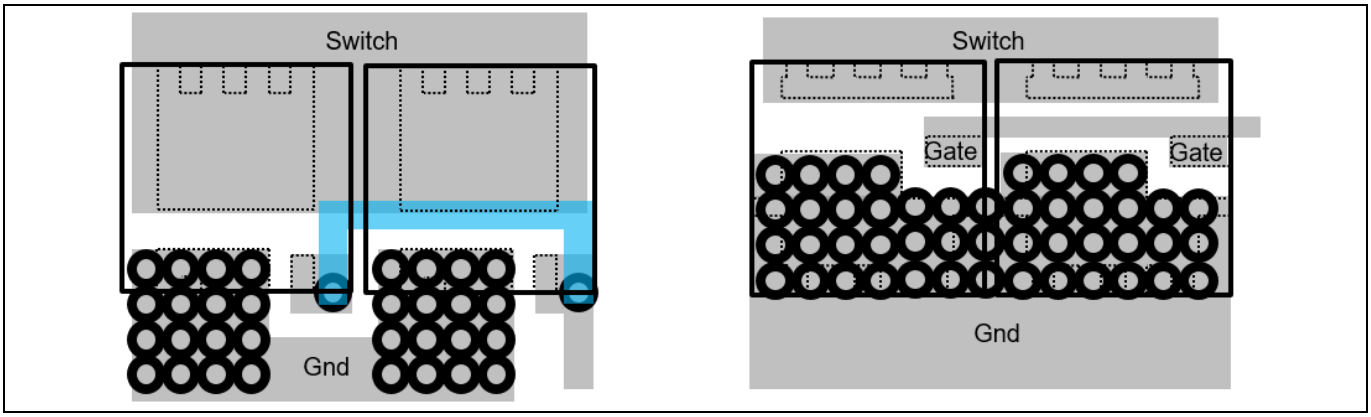


Figure 5 Parallelization with “Drain Down” (left) and “Source Down” (right). Gate signal (blue) on another layer.

3 Applications gaining most benefit from “Source Down”

3.1 ORing

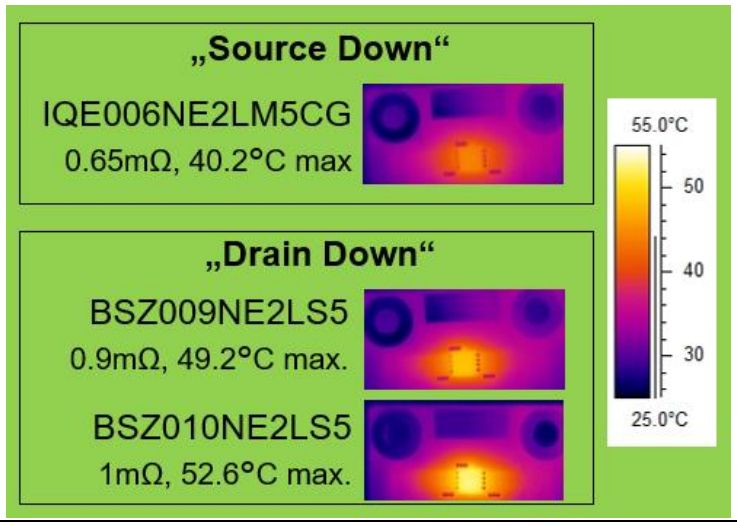


Figure 6 ORing with 30 A showing the advantages of “Source Down”: 40.2°C max. vs. 49.2/52.6°C

Applications like “ORing” or e-fuse benefit especially from the low $R_{DS(on)}$ of the “Source Down”. The impact on the design is shown in Figure 6. Even with a high current of 30 A the “Source Down” stays cool at 40.2°C, whereas the compared “Drain Down” devices heat up to 49.2/52.6°C.

This results in a higher reliability and fewer parts in parallel.

3.2 Synchronous rectification (secondary SMPS)

“Source Down” can improve the design of synchronous rectifiers on an SMPS’s secondary side. The switches are normally ground-referenced, i.e. the source is connected to the ground planes.

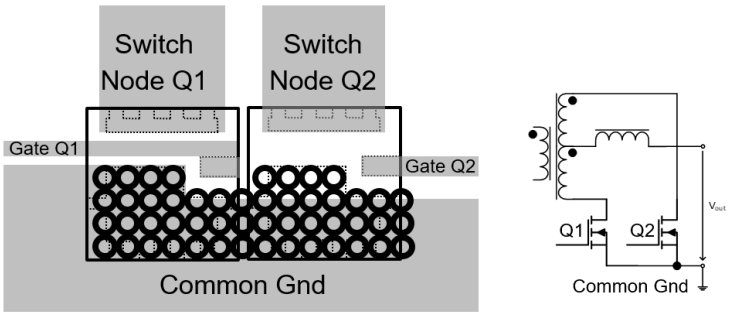


Figure 7 Multiple ground-referenced MOSFET

3.3 Buck converter

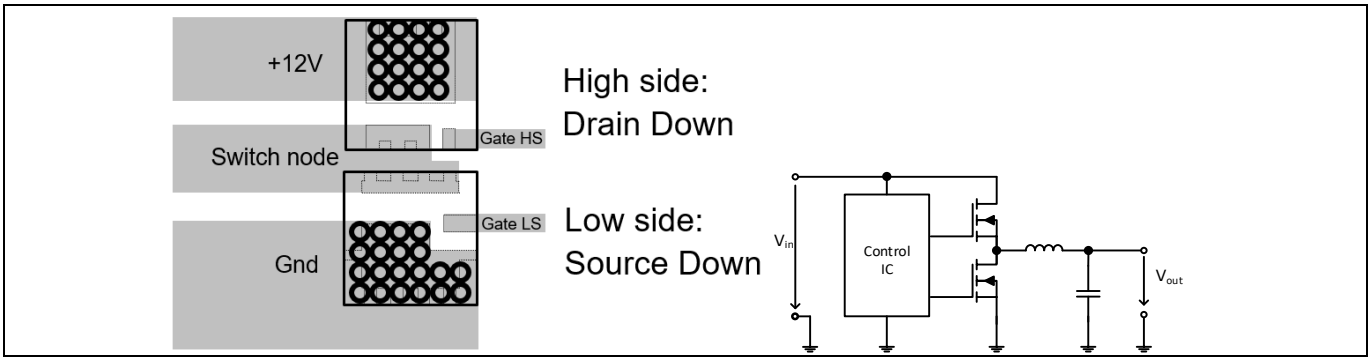


Figure 8 Buck converter with a Drain Down/Source Down combination

In half-bridge configurations like buck converters the “Source Down” allows the optimization of the thermal management. A “Drain Down” is used as the high-side and a “Source Down” as the low-side switch (Figure 8). Both devices are now connected to big copper areas. The switch node doesn’t have to be connected to a large copper area, avoiding possible EMI issues.

Figure 9 shows different configurations for a buck converter design.

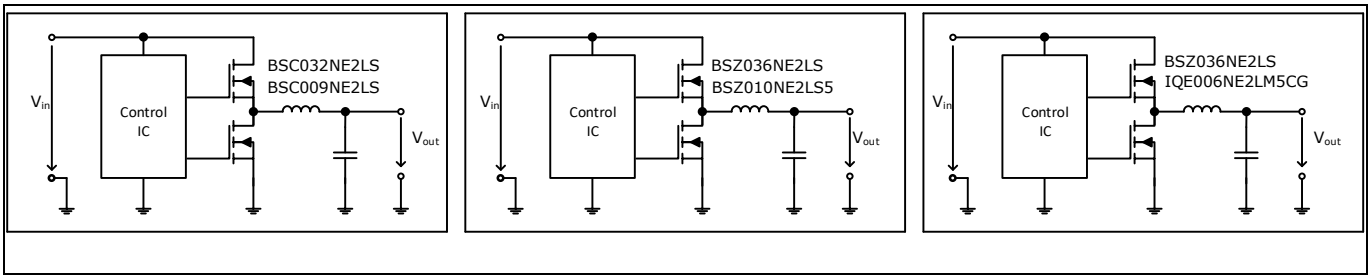


Figure 9 Buck converter with two Super SO8 (left), two PQFN 3.3 x 3.3 “Drain Down” (center) and the combination “Drain Down”/“Source Down” (right)

Measurements show at one glance the advantages of the new “Source Down” concept. In a buck converter the combination of “Drain Down” on the high-side and “Source Down” on the low-side (both PQFN 3.3 x 3.3) shows the highest efficiency with the lowest temperatures (Figure 10 and Figure 11).

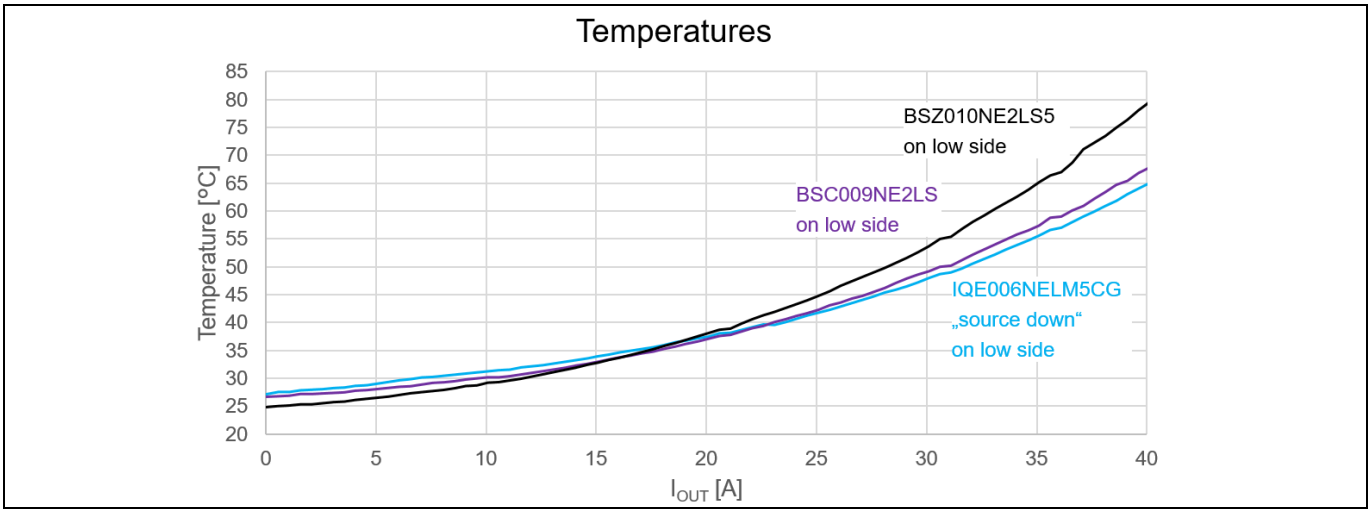


Figure 10 Thermal comparison

Applications gaining most benefit from “Source Down”

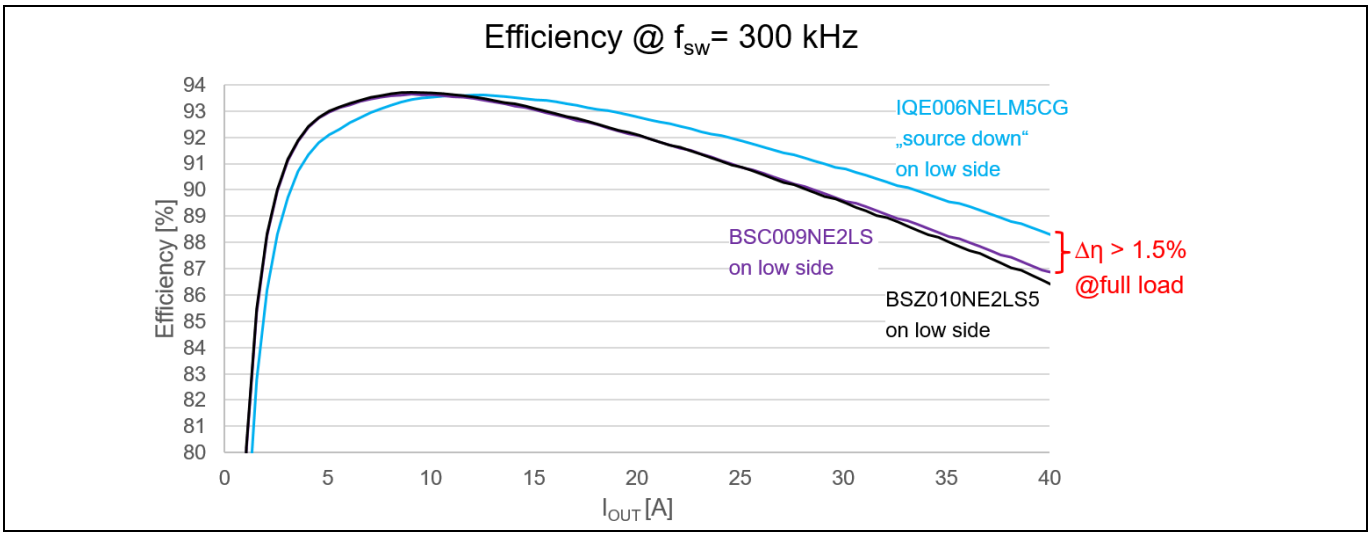


Figure 11 Efficiency comparison of all three designs

4 Summary

The new “Source Down” in PQFN 3.3 x 3.3 provides significantly improved $R_{DS(on)}$ and R_{thJC}, and continuous and pulsed drain current. The designs can now be optimized in terms of PCB space and efficiency. Combined with Infineon’s leading MOSFET technology those products enable a performance which was unattainable before with devices with a 10 mm^2 footprint.

Revision history

Document version	Date of release	Description of changes
V 1.0	27.01.2020	Initial release

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