950 V CoolMOS™ PFD7

Infineon's new MOSFET developed for mid- to high-power applications

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About this document

Scope and purpose

Infineon is extending its 950 V high-voltage (HV) metal oxide semiconductor field-effect transistor (MOSFET) solution portfolio on 300 mm production for mid- to high-power applications.

The **950 V CoolMOS™ PFD7** offers a competitively priced solution for industrial and consumer applications such as chargers and adapters, industrial switched mode power supplies (SMPS) and lighting in the power range from 200 W to 2000 W.

Going forward, it will be possible to equip the full system solution with 950 V MOSFETs – the **950 V P7** for the hard-switching part, with the 950 V PFD7 being suited to the soft-switching part of the SMPS.

Until now there has been a limited portfolio in the 950 V section (toward lower $R_{DS(on)}$); the 950 V CoolMOS™ PFD7 can also be used in the hard-switching stage of the power supply (e.g., the PFC section).

The portfolio includes frequently used packages that can directly replace existing MOSFETs, enabling improved performance in comparison to any other technology targeting this mid- to high-power market.

The 950 V CoolMOS™ PFD7 can fit into several SMD packages with the lowest $R_{DS(on)}$ available on the market, as well as the best-in-class (BiC) 60 mΩ device in TO-247-3.

This application note explains the new CoolMOS™ technology, and describes the technical and technological benefits of the 950 V CoolMOS™ PFD7. Additionally, this document details what the 950 V CoolMOS™ PFD7 offers in comparison to older technologies and competitor products. Furthermore, it will present evaluations of internal designs to show the thermal and efficiency performance that can be achieved with the 950 V CoolMOS™ PFD7.

With 950 V CoolMOS™ PFD7, Infineon Technologies is closing a portfolio gap and providing a solution to the main challenges faced by designers of mid- and high-power applications, maintaining a low bill of materials (BOM) while not sacrificing technical specifications and meeting safety requirements.

Intended audience

This application note is intended for SMPS design engineers.

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1 Target applications

The 950 V CoolMOS™ PFD7 is suited for use in several sections of SMPS, rather than just one.

Wherever the $R_{DS(on)}$ ranges from 60 mΩ up to 450 mΩ in terms of thermals and losses, whether in hard- or soft-switching topology, the 950 V CoolMOS™ PFD7 will provide switching benefits, make the target application smaller and increase form factor by using the SMD package approach.

For further information on hard- and soft switching topologies, please read Infineon's **950 V CoolMOS™ P7 application note**.

Figure 1 shows an overview of Infineon's superjunction MOSFET portfolio. The 950 V CoolMOS™ PFD7 covers a broad voltage range and can be used in consumer and industrial applications, as well as in the growing horticultural lighting and industrial SMPS markets, with higher input voltages.

Specifically, this means the 950 V CoolMOS™ PFD7 can be used beyond flyback and power-factor correction (PFC) topologies; it also addresses LLC and zero voltage switching (ZVS) topologies. This is achieved through the integrated fast body diode and an ultralow Q_{rr} level.

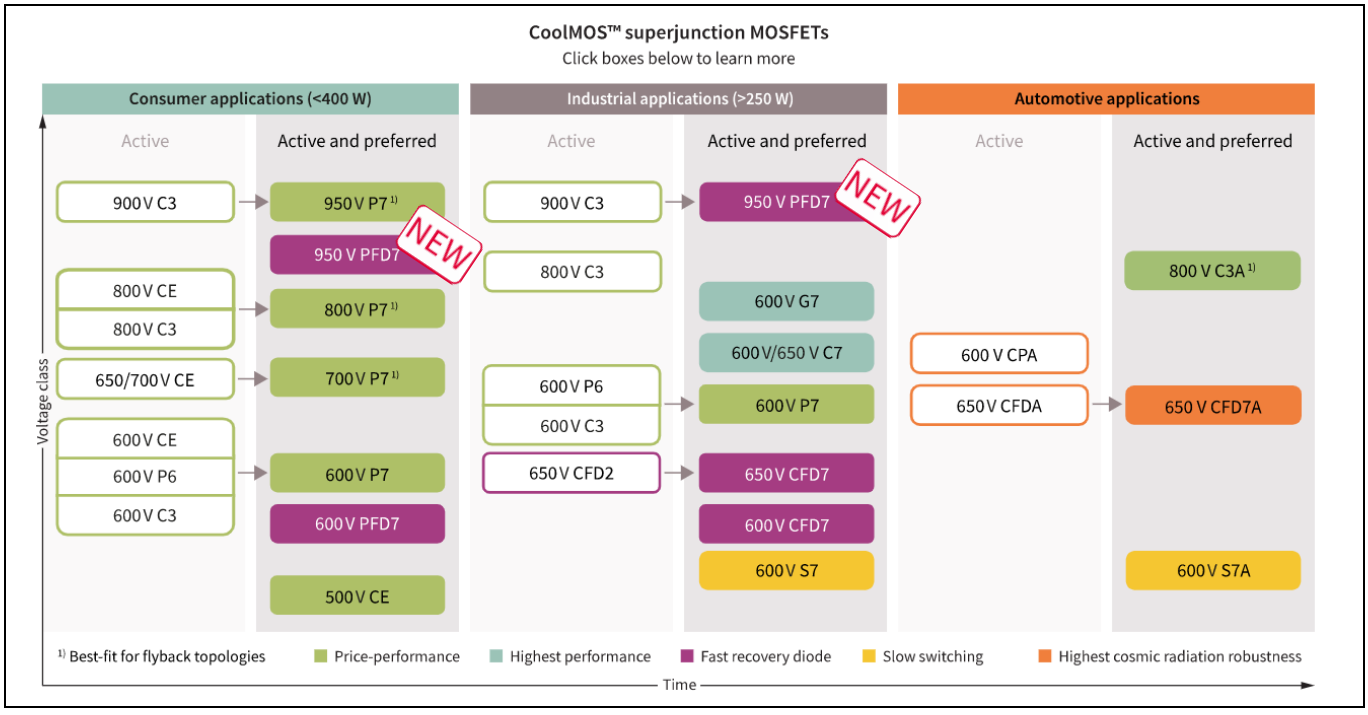

Figure 1 CoolMOS™ superjunction MOSFET portfolio overview

2 Technology parameters

This chapter describes all technology-related parameters that influence behavior in the target applications.

2.1 Q_g – gate charge

The gate charge influences the driving losses, which heavily influence efficiency during light load operation or at increased switching frequency.

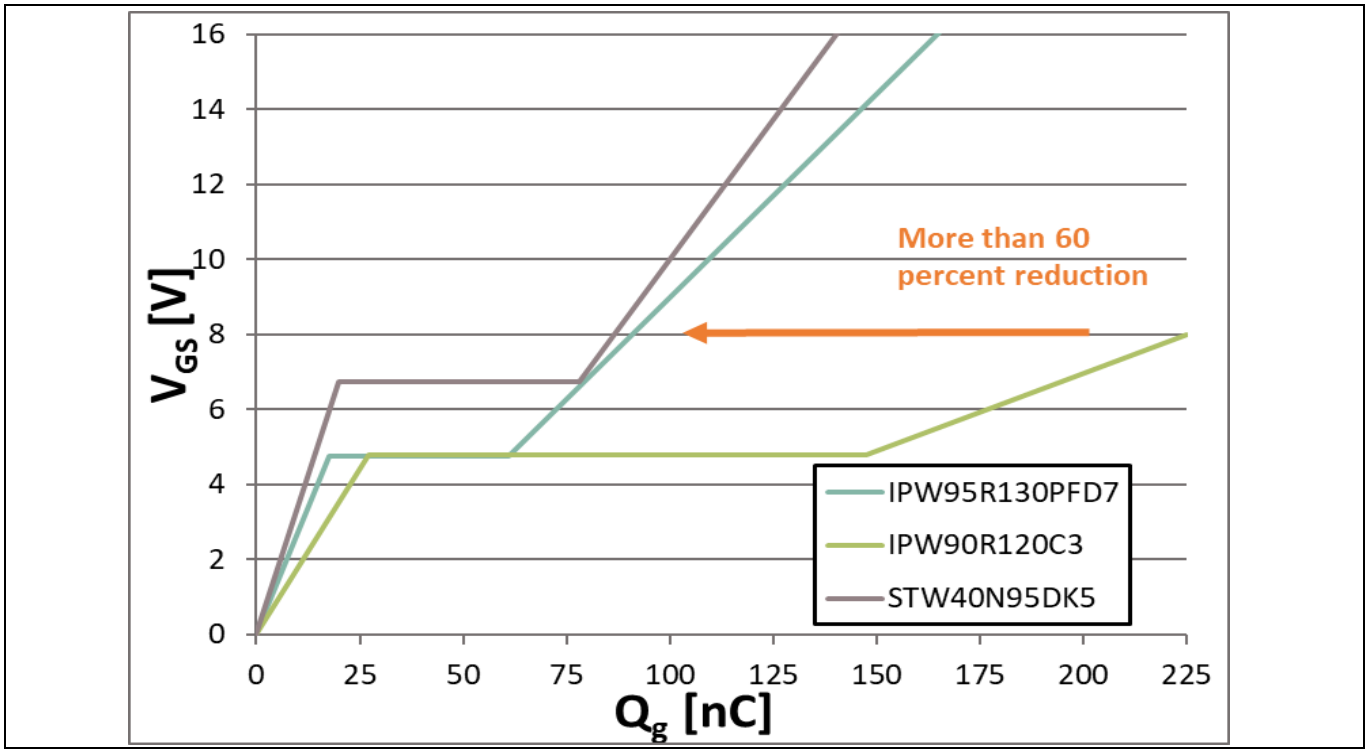

Figure 2 Gate charge of 130 mΩ equivalent devices (datasheet equivalent comparison)

As shown in **Figure 2**, the 950 V CoolMOS™ PFD7 shows the lowest Q_g (over 60 percent reduction already at 8 V driving voltage) in comparison to the mature 900 V CoolMOS™ C3 technology and favorable performance to the main competitor (validated via Infineon internal characterization measurement).

With this behavior the 950 V CoolMOS™ PFD7 can allow high switching frequencies (more than 100 kHz), which can be beneficial to reduce the magnetic components of the design, resulting in a smaller form factor and higher power density.

It can be clearly seen that driving losses are reduced in comparison to the previous C3 technology, and it is closing the gap between Infineon's long-established and leading technology and competitors' latest innovations.

2.2 $R_{DS(on)}$ – temperature dependency of on-state resistance

With the increased power levels targeted by the 950 V CoolMOS™ PFD7, conduction losses will have a huge influence on the efficiency and the thermal behavior of the overall system – especially at lower input voltages of 90 V AC or 110 V AC.

In this case, the 950 V CoolMOS™ PFD7 can offer a perfect replacement in terms of $R_{DS(on)}$. Thanks to the MOSFET structure, the 950 V CoolMOS™ PFD7 offers the same $R_{DS(on)}$ change driven by increasing junction temperature as the product STW40N95DK5 by STMicroelectronics. **Figure 3** shows this behavior.

At normal/standard working temperatures of the MOSFET, customers can expect an equivalent thermal behavior in the end application when replacing competitor technology.

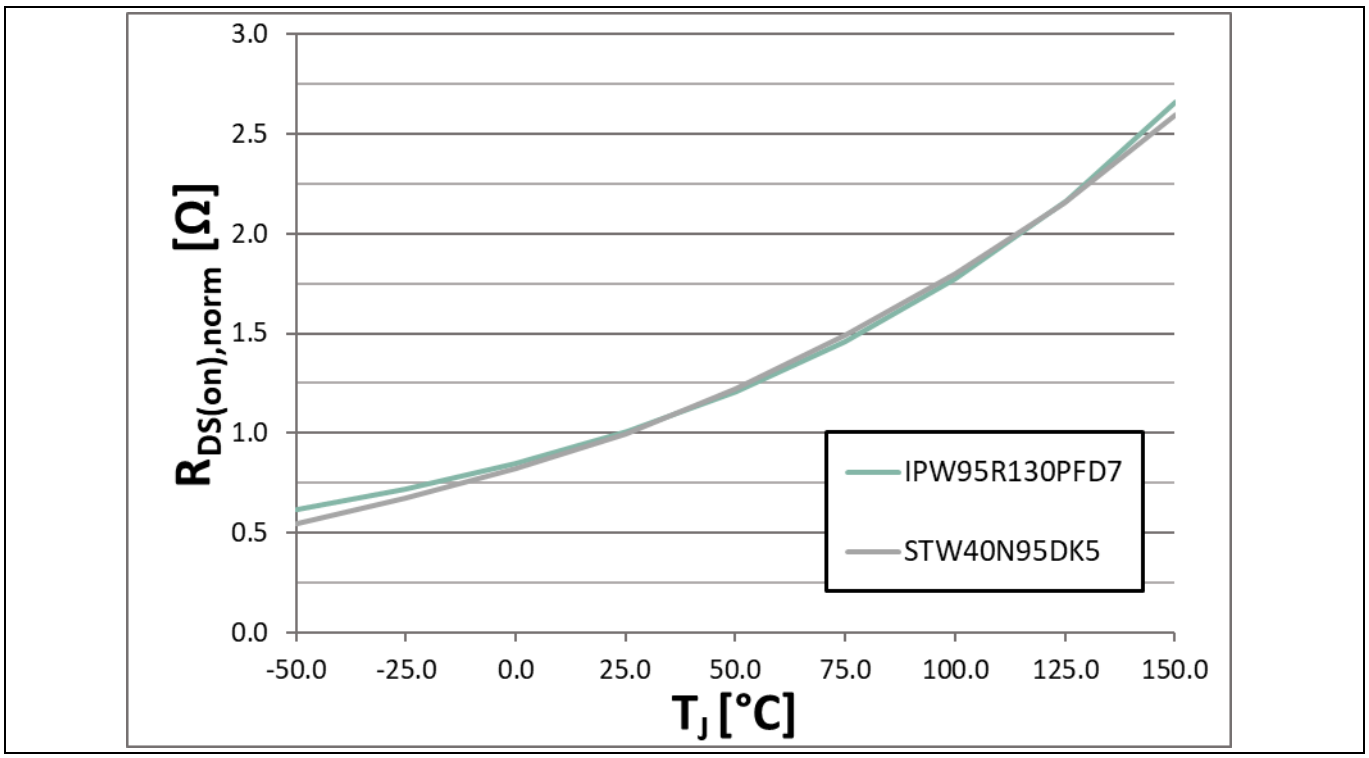

Figure 3 $R_{DS(on)}$ **behavior over junction temperature (normalized)**

2.3 E_{oss} – energy stored in output capacitance

The E_{oss} is one of the main causes of loss during the turn-on of the MOSFET. This is the energy that translates into losses during the turn-on at a certain V_{DS} voltage.

In quasi-resonant (QR) flyback converters, for example, there are no E_{on} losses as there is no overlap between I_D and V_{DS} as the current through the main transformer is 0 A; nevertheless, additional losses are generated inside the MOSFET at every turn-on and -off based on the amount of energy stored in the internal capacitances.

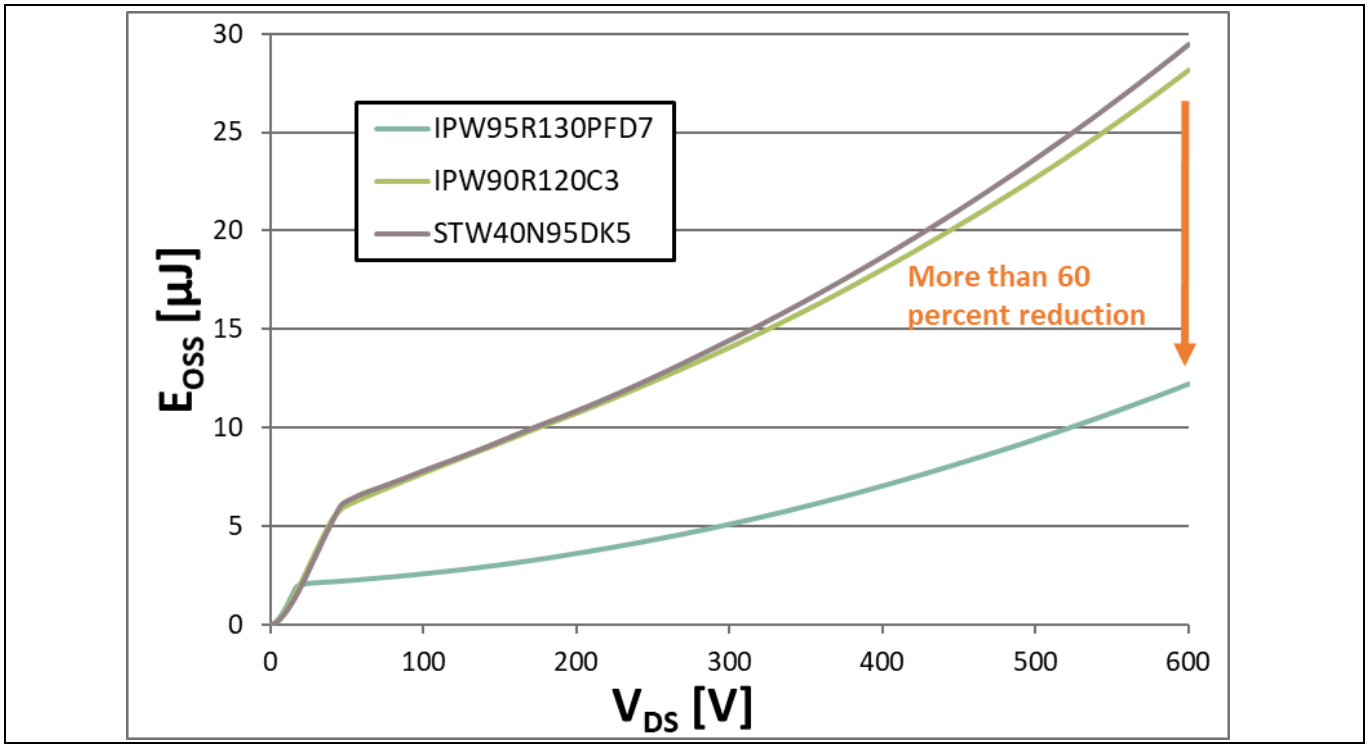

Figure 4 E_{oss} comparison of 130 mΩ devices

Figure 4 shows that the 950 V CoolMOS™ PFD7 offers the lowest E_{oss} starting from 30 V_{DS}. At 600 V the difference from the previous C3 technology is more than 60 percent, which is a big step between generations.

In hard-switching applications, this energy is a fixed loss. E_{oss} is stored in the C_{oss} during the turn-off phase. In the next turn-on transient, it is dissipated in the MOSFET channel. This loss can be significant at light load conditions, because most of the other losses are load dependent and decrease considerably at light load; thus, the E_{oss} reduction contributes to an improvement of the light load efficiency.

In soft-switching applications, with zero voltage turn-on, this energy is recycled back to the circuit (before the turn-on) rather than dissipated.

Although E_{oss} is assumed to be recycled in ZVS applications, it is still desirable to have lower E_{oss}. In topologies such as resonant LLC or phase-shifted full-bridge (PSFB), the designer must ensure proper sizing of the primary inductance and its stored energy that is required to complete recycling of E_{oss} and reach complete ZVS.

The 950 V CoolMOS™ PFD7 also offers the possibility to go to higher switching frequencies, with the same possibilities as already described in the gate charge section of this chapter.

2.4 Q_{oss} – charge stored in output capacitance

Due to the non-linear capacitance of superjunction MOSFETs, the stored charge in the output capacitance is mostly concentrated in the low-voltage region. Nearly 90 percent of the Q_{oss} charge will be generated between 0 V and 20 V, and 10 percent from 20 V up to 400 V.

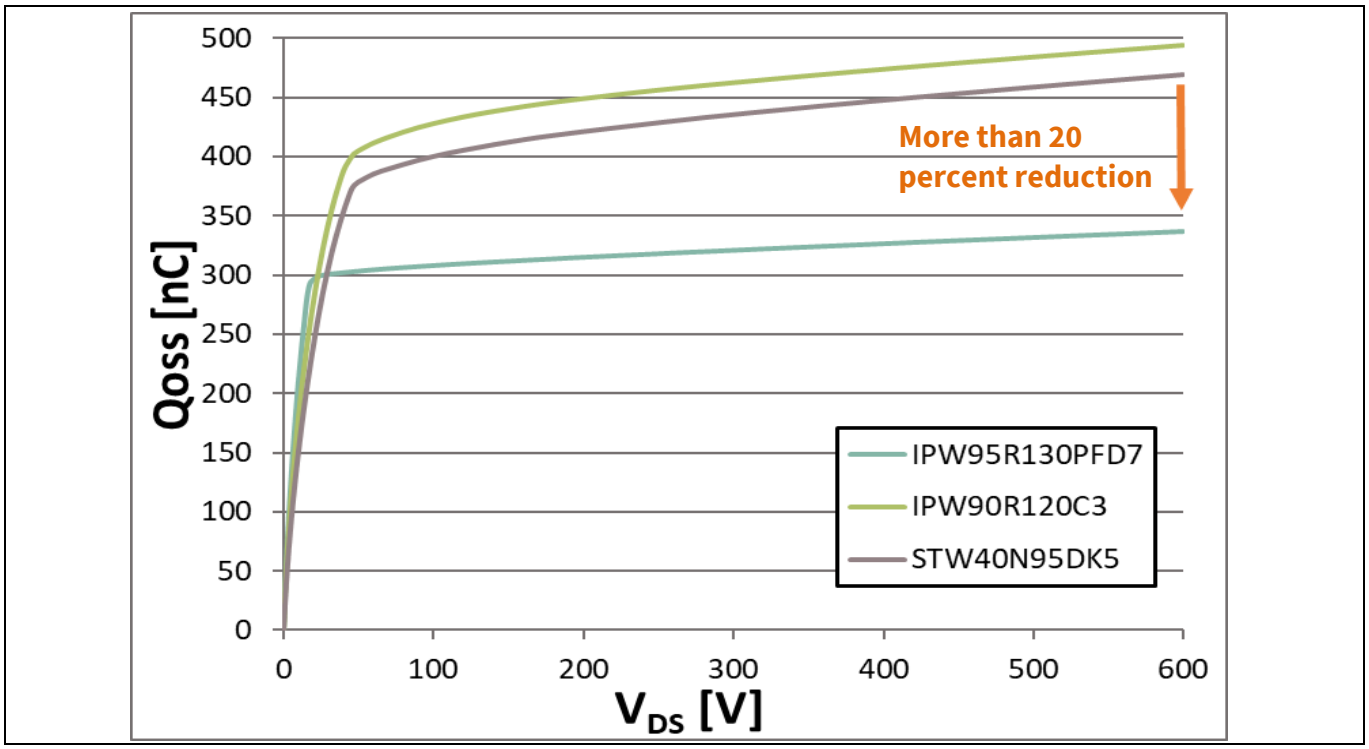

Figure 5 Q_{oss} comparison of 130 mΩ devices

The reduction in Q_{oss} is also valuable in ZVS applications; apart from having sufficient energy to achieve ZVS, the dead time between the two MOSFETs in the switching leg must also be long enough to allow the voltage transition.

950 V CoolMOS™ PFD7 needs the lowest circulating current to charge and discharge the C_{oss} in comparison to internal and external competitor devices from ~10 V V_{DS} upward.

2.5 Transfer characteristics

There is a well-known failure mode in low-power applications when the gate source voltage is dropping, for example during burst mode operation when the MOSFET cannot carry enough current to reach the peak current.

In this case the MOSFET is operating in the linear region and the MOSFET is not turning off, resulting in a destruction of the application.

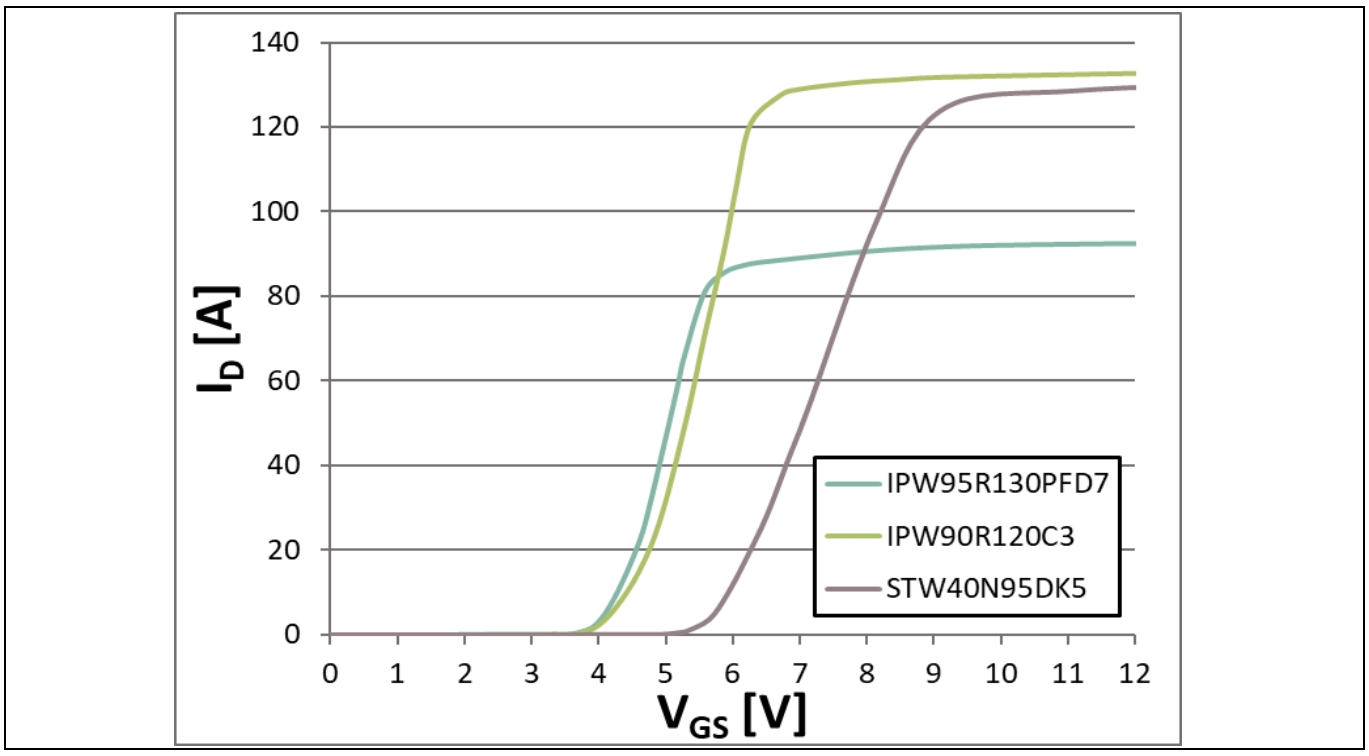

Figure 6 Transfer characteristics – comparison of 130 mΩ devices at 25°C

The 950 V CoolMOS™ PFD7 shows the BiC transconductance behavior thanks to the current capability at low gate source voltage – unmatched on the market. This leads to the possibility of reducing the gate source voltage intentionally to minimize the overall driving losses, and the possibility of meeting new no-load operation requirements.

Additionally, the 950 V CoolMOS™ PFD7 can offer a very narrow $V_{GS(th)}$ (gate source threshold voltage) window from 2.5 V to 3.5 V with a typical value of 3 V, illustrated in **Figure 11**, which makes the deviation even narrower and the design of the shutdown voltage even more exact.

2.6 Q_{rr} (reverse recovery charge)

One of the main differentiators between the well-known 950 V CoolMOS™ P7 and the upcoming 950 V CoolMOS™ PFD7 is the integrated fast body diode. As this was the limiting factor for the 900 V CoolMOS™ C3 replacement for many target applications, the PFD7 comes with improved performance parameters in the 900 V to 950 V area.

Hard commutation on a conducting body diode can occur in any half- or full-bridge configuration. The need for PFD7/CFD7, or a similar fast body diode technology, is clear under certain operating conditions in an LLC or ZVS PSFB where hard commutation can occur, for example if there is a sudden change of duty cycle or frequency, and there are also other operating conditions in which a repetitive hard commutation can be present for a period of time.

In this case, it is very important to reduce the generated losses due to the Q_{rr} and resulting reverse recovery energy (E_{rr}) to a minimum, to avoid thermal problems during this operation, which could lead to defects.

However, the 950 V CoolMOS™ PFD7 offers the lowest Q_{rr} on the market in comparison to other fast body diode superjunction MOSFETs, and this reduces the possibility of failure to a minimum and increases the reliability of the whole system.

All derived data in sections 2.6 and 2.7 have been measured in Infineon Technologies' characterization lab under the same conditions. The test circuit used is described in the dedicated product datasheet in chapter 5 "Test Circuits" – Table 8 "Diode characteristics".

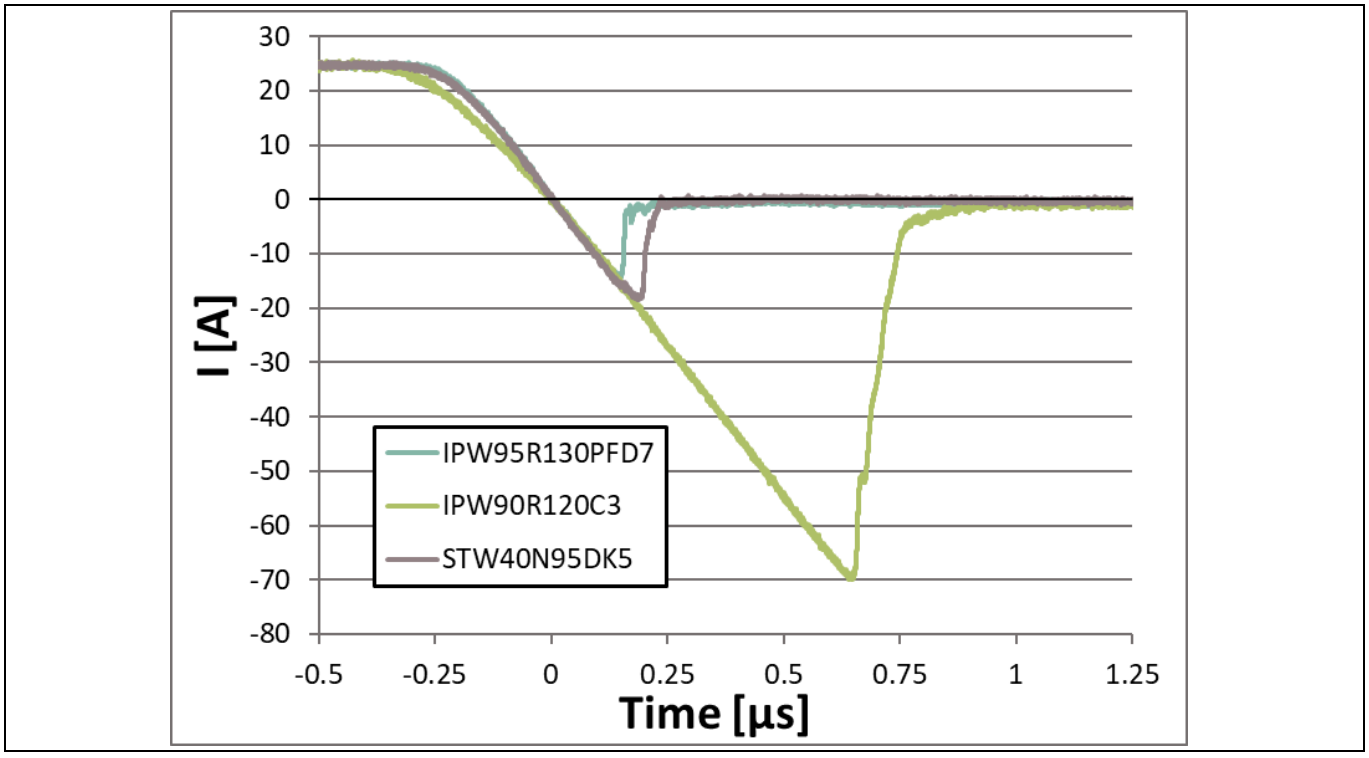

Figure 7 Improved t_{rr} and Q_{rr} of IPW95R130PFD7 vs. competitors in 130 mΩ class

The Q_{rr} needs to be removed from the body diode during a hard commutation event, which results in a high current flow, high di/dt, high dv/dt and inductive driven drain source voltage (V_{DS}) overshoots.

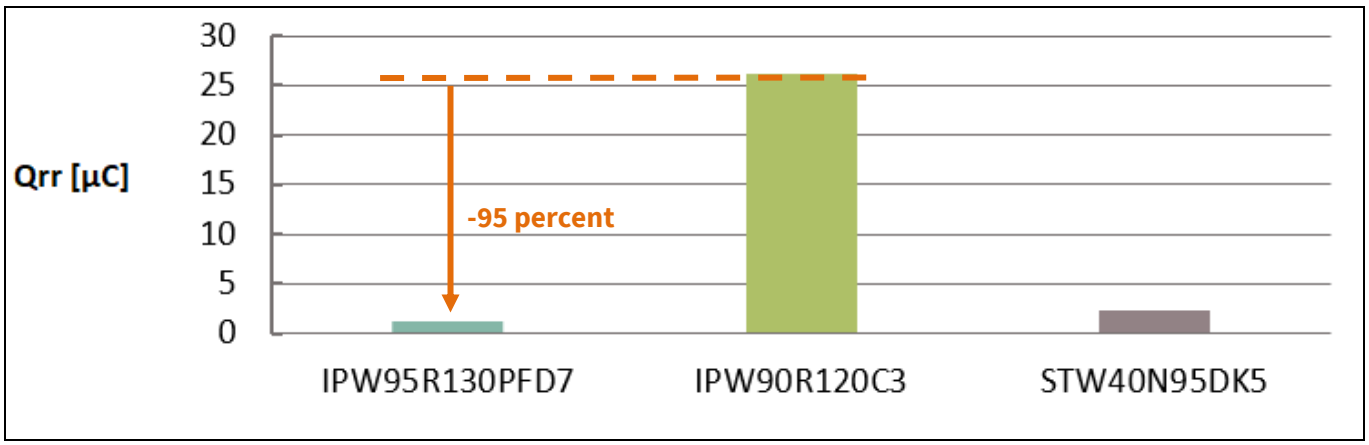

Figure 8 Characterization data comparison of Q_{rr} (IPW95R130PFD7 vs. competition)

The CFD2 technology already offered the world's lowest Q_{rr}, due to the need for higher reliability in operating conditions in which repetitive hard commutation can occur. But for the 900 V to 950 V voltage class, this additional improvement step was not available for the previous 900 V CoolMOS™ C3 technology. Therefore, **Figure 8** shows the drastic reduction and evolution of the technology and its Q_{rr} value reduced by 95 percent.

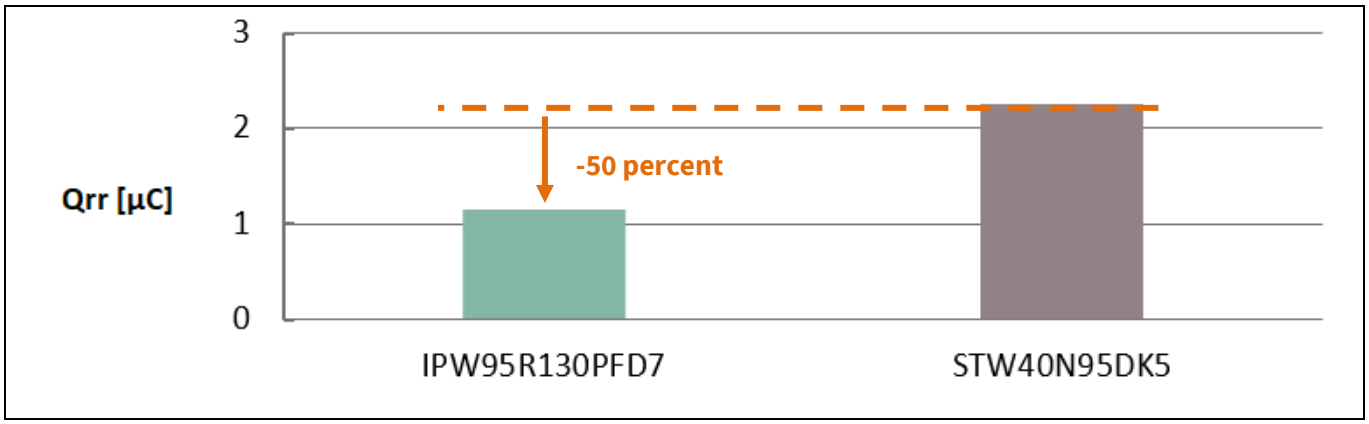

Figure 9 Detailed comparison of Q_{rr} (IPW95R130PFD7 vs. STW40N95DK5)

Furthermore, the 950 V CoolMOS™ PFD7 offers an additional ~50 percent lower Q_{rr} than the main competitor.

2.7 t_{rr} (reverse recovery time) and I_{rrm} (maximum reverse recovery current)

Due to this reduced Q_{rr}, the t_{rr} and I_{rrm} and the resulting E_{rr} are much lower than those of any other competitor on the market.

In contrast to the internal reference part 900 V CoolMOS™ C3, the 950 V CoolMOS™ PFD7 offers around 80 percent lower t_{rr} and I_{rrm}, as shown in **Figure 10**.

In comparison to the competitor product (950 V STM DK5), the 950 V PFD7 offers around 25 percent lower t_{rr} and I_{rrm}, which is a further improvement in this superjunction voltage class segment.

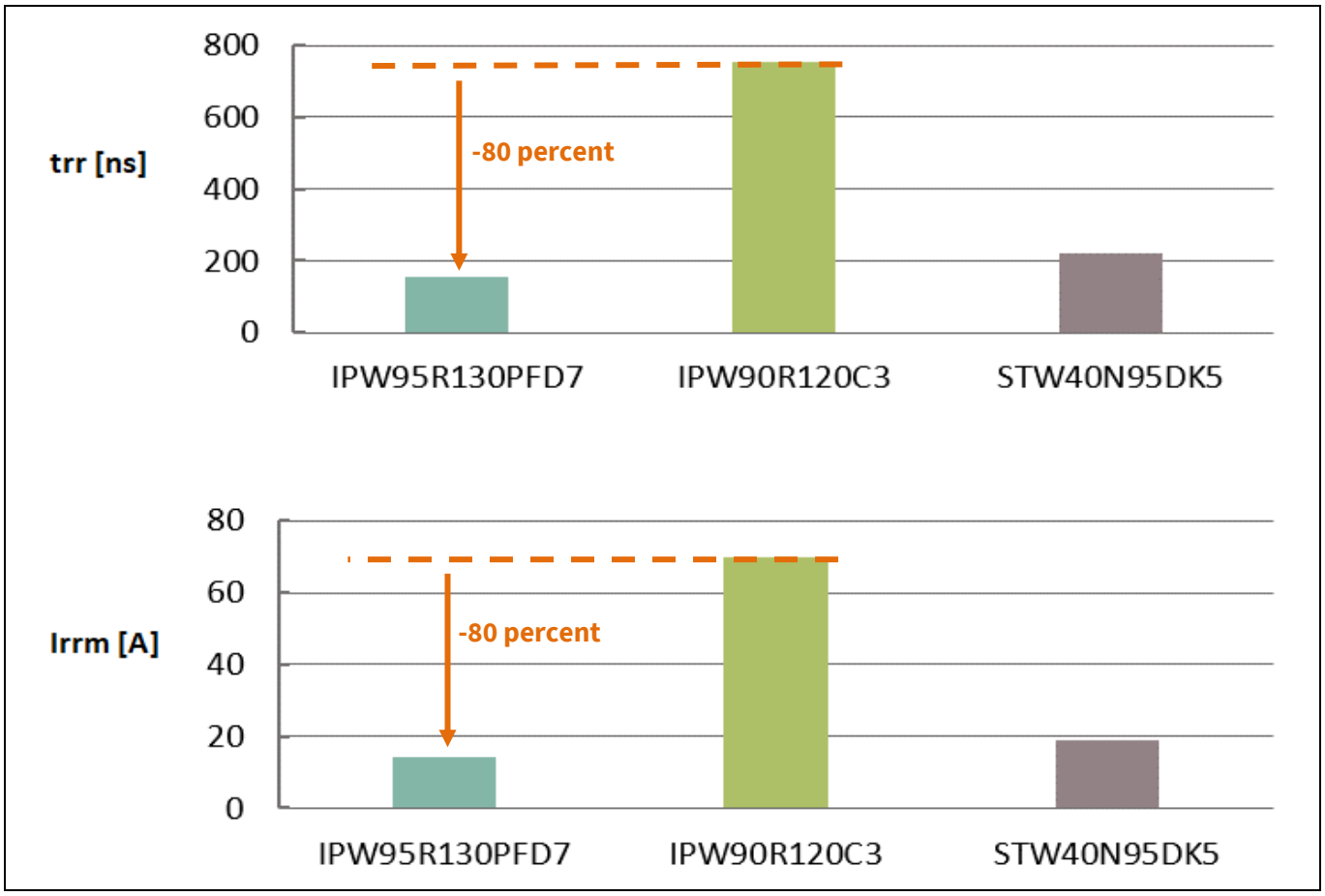

Figure 10 t_{rr} and I_{rrm} comparison of IPW95R130PFD7 vs. competitors in 130 mΩ class

Repetitive hard commutation at a high application switching frequency is generally not recommended for any superjunction MOSFET, but in some operating conditions it cannot be avoided, at least for short periods of time. Therefore, the reduced reverse recovery benefits of the 950 V CoolMOS™ PFD7's body diode results in much lower power dissipation during these events against internal and external competitors.

2.8 Gate threshold voltage ($V_{GS(th)}$)

Keeping in mind ease of use, Infineon looked to launch the technology with a low $V_{GS(th)}$ of 3 V and a very narrow tolerance of ±0.5 V.

This makes both the P7 and PFD7 easy to design in and allows the use of lower gate source voltage, which makes it comfortable to drive, avoiding MOSFET linear mode, and leads to reduced idle losses, ultimately increasing light load efficiency.

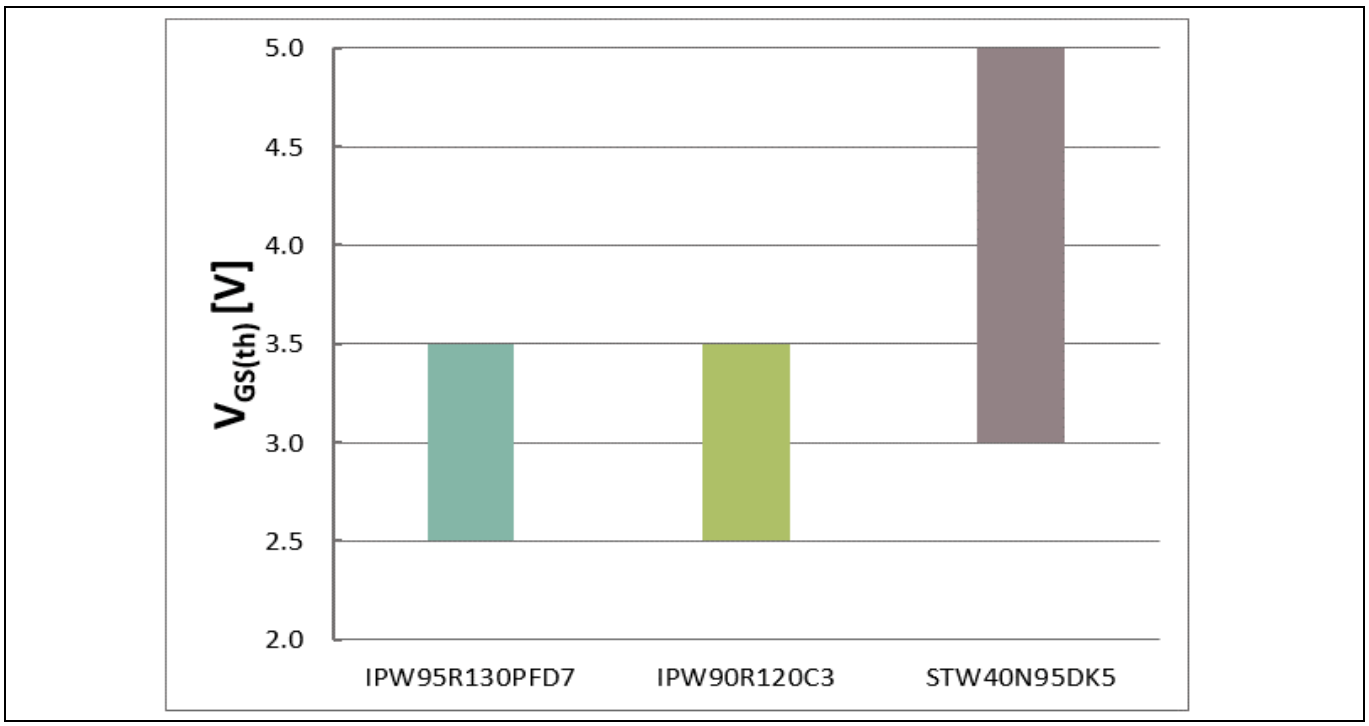

Figure 11 Low $V_{GS(th)}$ and tight $V_{GS(th)}$ deviation

2.9 ESD capabilities

It was possible to design the chips in a robust way and maintain the electrostatic discharge (ESD) ruggedness up to HBM class 2 level, without the need for an extra integrated Zener diode.

In the end, a high ESD class (as the P7 and PFD7 are designed for) helps to support increased assembly yield, leads to fewer production-related failures and results in manufacturing cost savings on the customer side.

Figure 12 illustrates the overall human-body model (HBM) and charge-device model (CDM) performance of all CoolMOS™ 7 series with a focus on the 950 V CoolMOS™ PFD7 in the highlighted section.

ESD protection			
600 V P7	HBM	0.12-0.60 Ω: 2-4 kV	Class 2
	CDM	>1 kV	Class C3
700 V P7	HBM	0.75-2.00 Ω: 1–2 kV	Class 1C
		0.36-0.60 Ω: 2–4 kV	Class 2
	CDM	>1 kV	Class C3
800 V P7	HBM	2.00-4.50 Ω: 1–2 kV	Class 1C
		0.28-1.40 Ω: 2–4 kV	Class 2
	CDM	>1 kV	Class C3
950 V P7	HBM	3.70 Ω: 1-2 kV	Class 1C
		0.45-2.0 Ω: 2-4 kV	Class 2
	CDM	>1 kV	Class C3
950 V PFD7	HBM	0.06-0.45Ω: 2-4 kV	Class 2
	CDM	>1 kV	Class C3

Figure 12 ESD protection levels – 600 V up to 950 V CoolMOS™

2.10 Cosmic ray performance

Single-event burnouts (SEBs) caused by cosmic radiation contribute to the random failure rate in HV MOSFETs. Even though the event is random, its probability can be predicted by knowing the application conditions.

Because of this, Infineon Technologies recommends establishing proper de-rating on the rated breakdown voltage of the MOSFET in the range of 20 to 30 percent, depending on several application parameters. There is no global rule on how large this de-rating should be, but in general the Infineon Technologies support team can help if use cases need to be analyzed.

A detailed description of cosmic rays and their influence on MOSFET lifetime has been prepared to give guidance to SMPS designers. An application note was specifically created for the automotive area (with a focus on CFDA and CFD7A), where even harsher and tougher requirements apply compared to the industrial world.

As the 950 V CoolMOS™ PFD7 is rated as an industrial product and can also be used for consumer applications, it is more relaxed compared to automotive areas, but de-rating should always be taken into account to extend lifetime and prevent early failures in the field. With the help of the customer (knowing use cases of systems and components by the end customer + specification details such as min./max. allowed ambient/working temperatures), a "mission profile" can be derived, giving all necessary inputs for a later failure in time (FIT) rate calculation.

For more details and some examples, refer to Infineon's application note **Cosmic radiation effects on high-voltage semiconductors in automotive onboard chargers**.

3 Benchmarking of 950 V CoolMOS™ PFD7 in mid- and high-power designs

As already anticipated in the target applications, the 950 V CoolMOS™ PFD7 is suited to mid- to high-power applications using soft- or hard-switching topologies. So as not to limit the possible usage and to give an indication for all customers of the latest Infineon technology, some basic evaluations have been carried out.

This chapter will show which performance benefits customers can expect with the 950 V CoolMOS™ PFD7 in comparison to the main competitor in this market, as well as the predecessor 900 V CoolMOS™ C3.

3.1 Efficiency comparison in a 2.5 kW CCM PFC

Figure 13 shows the efficiency chart for a 2.5 kW hard-switching continuous conduction mode (CCM) PFC at 65 kHz with 5 Ω external R_g for the high-line condition with an input voltage of 230 V AC and 50 Hz.
As can be seen, the 950 V CoolMOS™ PFD7 offers the best performance over the whole load range with the benefit of at least 0.1 percent better efficiency.

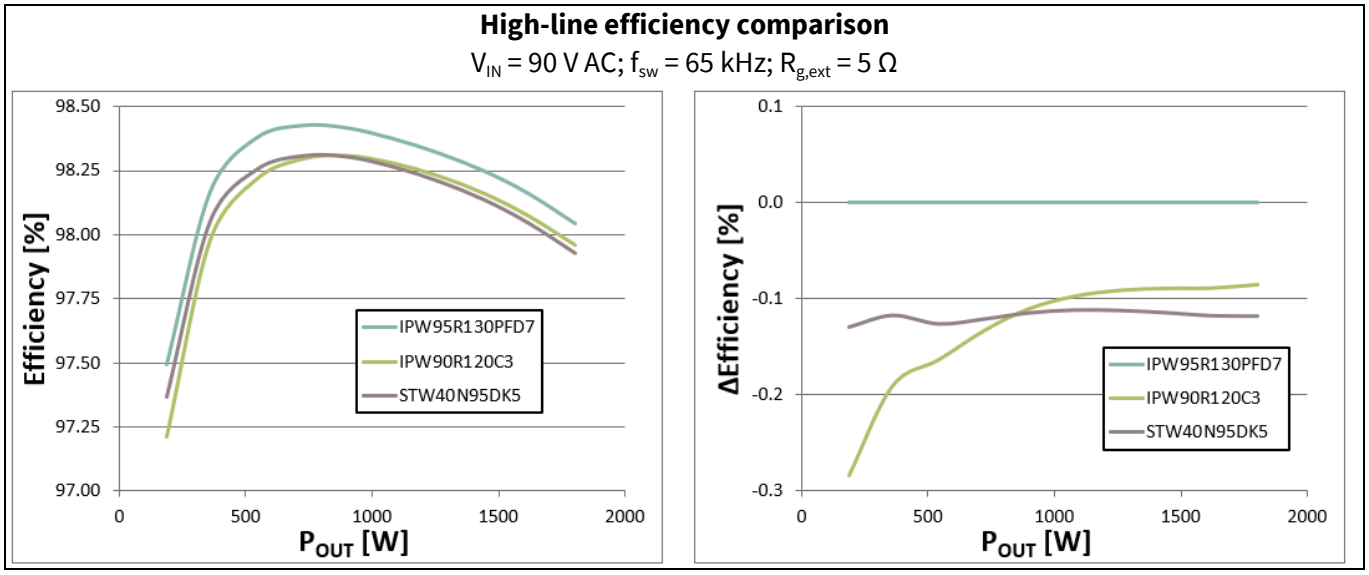

Figure 13 High-line efficiency comparison in a 2.5 kW CCM PFC demo board

Figure 14 shows the same measurement for the low-line input voltage condition with 90 V AC at 60 Hz. An efficiency gain between 0.2 percent and up to more than 0.6 percent can be seen in a direct one-to-one comparison with the main competitor.

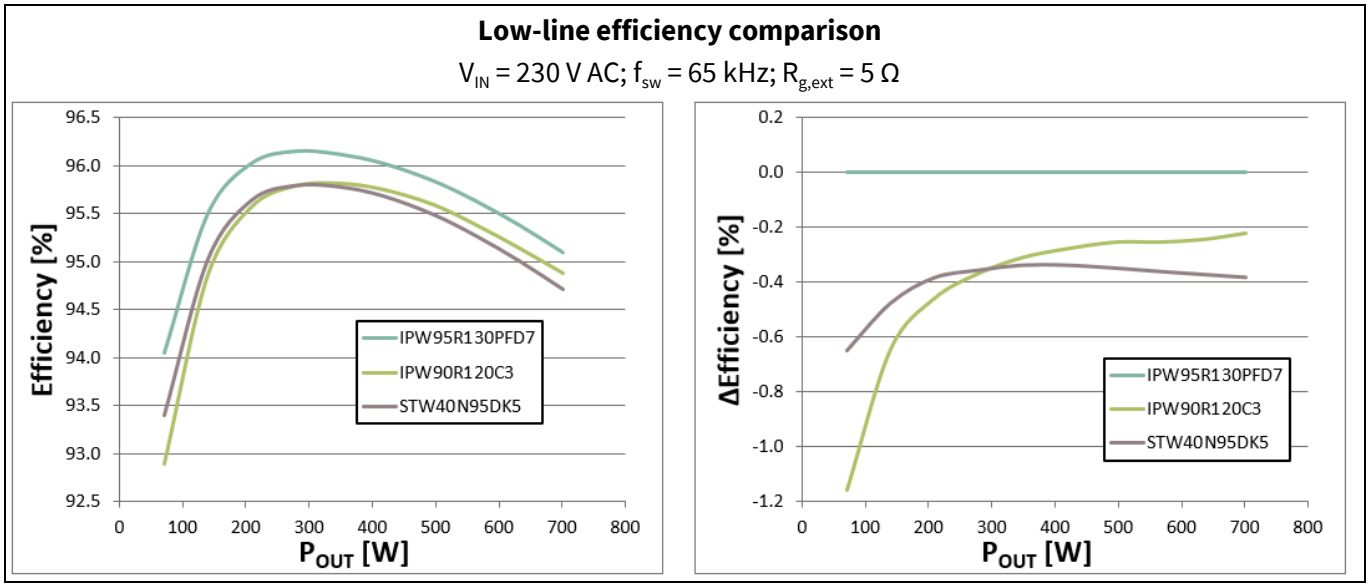

Figure 14 Low-line efficiency comparison in a 2.5 kW CCM PFC demo board

3.2 Efficiency comparison in an 800 W ZVS demo board

As another example for a soft-switching application in this power class, Infineon's 800 W ZVS demo board was chosen. **Figure 15** shows an efficiency comparison between the new 950 V CoolMOS™ PFD7 technology, the precursor 900 V CoolMOS™ C3 and the main competitor.

Figure 15 shows that the PFD7 has an up to 0.8 percent better performance in terms of efficiency compared to both other devices in the mid-load section. In comparison to the C3, the mid-load efficiency is up to 1.6 percent better, which is a massive improvement.

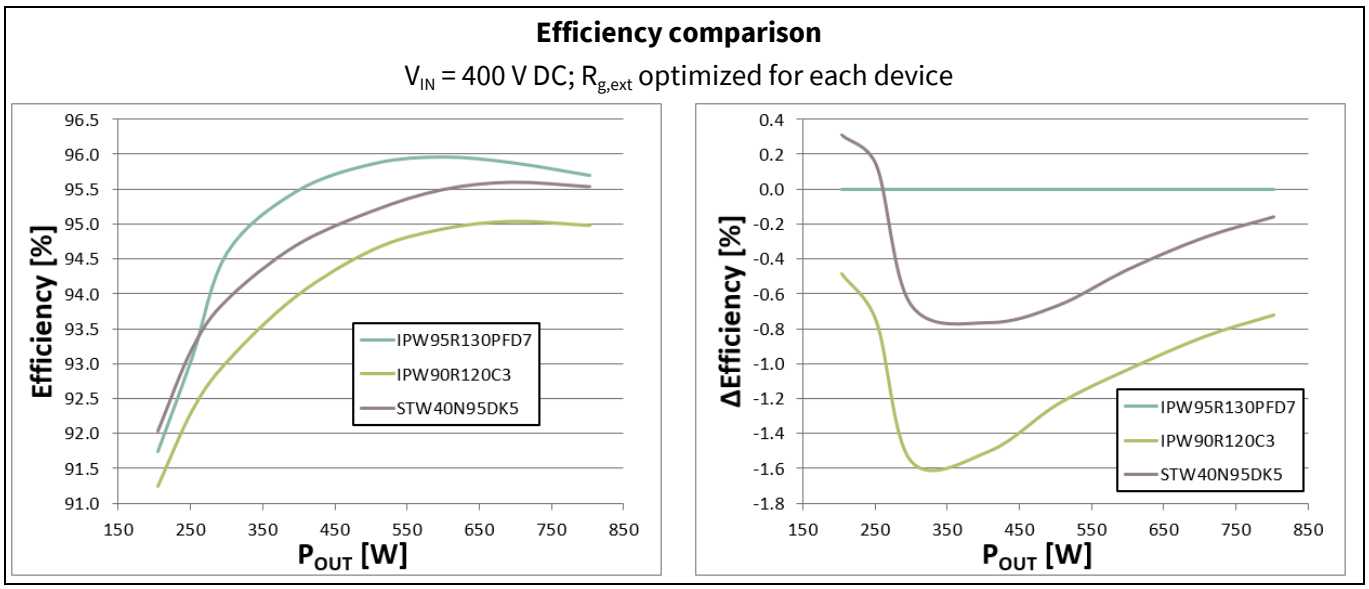

Figure 15 Efficiency comparison in an 800 W ZVS demo board

3.3 Ringing behavior in a PFC (internal test board)

To prove and justify the ringing tendency of the newly developed technology, an internal ringing test board was used.

Figure 16 shows a typical switching waveform for IPW95R130PFD7 in a special ringing test board. This test circuit is configured with an additional external gate-to-drain capacitance with 7.2 pF for capacitive coupling between gate and drain, emulating PCB parasitic capacitance.
Designers should take care with the layout to minimize this parasitic capacitance to enable the highest performance of the MOSFET.

In this measurement, a 5 Ω external R_g for a 130 mΩ device is used.

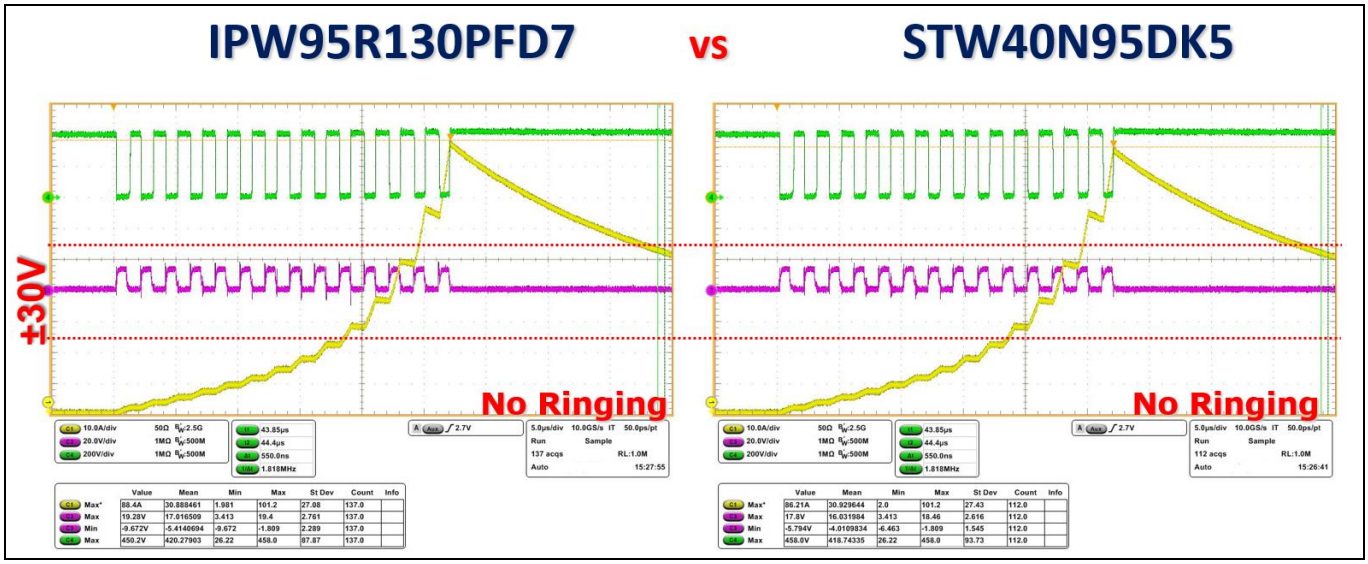

Figure 16 Ringing tendency of CoolMOS™ PFD7 vs. competitor part in a ringing test setup

Switching waveforms are measured with V_{DS} = 400 V (shown in green) and V_{GS} = 13 V (shown in magenta). The current waveform shown in yellow is increasing with every pulse up to saturation, which is represented with an offset in V_{DS} at the peak current level of around 80 A. The 950 V CoolMOS™ PFD7 as well as the DK5 with optimized $R_{g,\,ext}$ shows a very nice switching waveform with plenty of margin on the +/-30 V_{GS} limitation.

4 Portfolio

The 950 V CoolMOS™ PFD7 represents a further upgrade of the existing 950 V P7 products with respect to $R_{DS(on)}$ classes and offers the most relevant packages for mid- to high-power applications.

All main target applications are covered, including lighting and industrial SMPS applications.

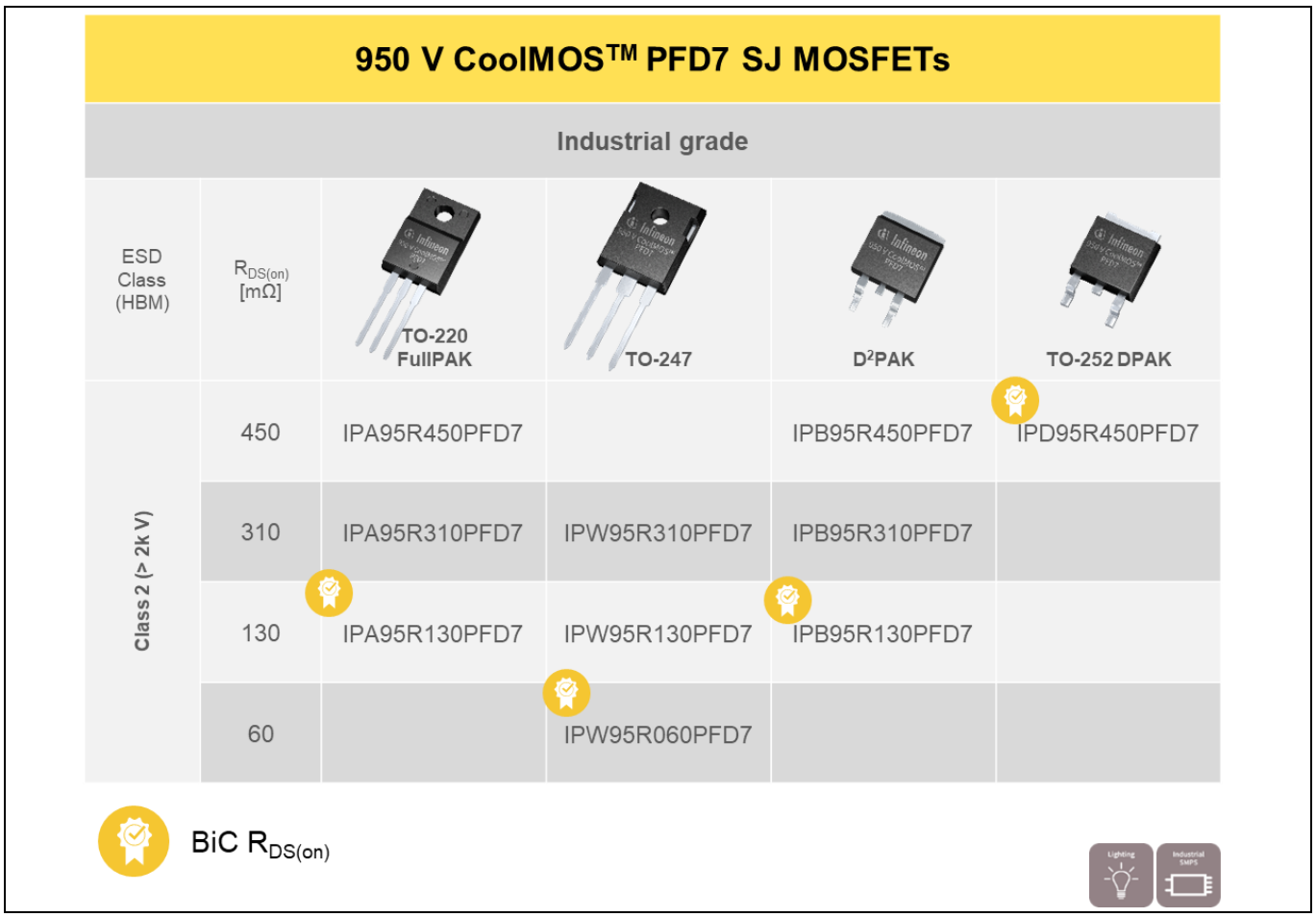

Figure 17 950 V CoolMOS™ PFD7 portfolio

Already well known for its P7 families, the high ESD class level of 2 (more than 2 kV) with protection function for the gate structure can be guaranteed over the full product range.

With further packages to come with BiC $R_{DS(on)}$, Infineon Technologies has set a new benchmark in the industry (**Figure 18**).

Where competitors only offer leaded packages, Infineon offers SMD D²PAK and DPAK devices while enabling and supporting customers with smaller designs and lower BOM costs.

On the market, we can offer now a much lower $R_{DS(on)}$ than our main competitor, enabling change in terms of package selection.

Infineon's lowest $R_{DS(on)}$ in its 900 V CoolMOS™ C3 technology was 120 mΩ in a TO-247 housing. The new solution puts a 60 mΩ chip in the same package size, which opens up new application possibilities. Instead of paralleling MOSFETs it can be used as a single device (if thermal capabilities are given). In the surface-mount device (SMD area), the lowest possible $R_{DS(ON)}$ is 130 mΩ in D²PAK.

The benefit for the customer is obvious. The customer can design an application that is much smaller, thinner and more efficient, even when coming from leaded packages such as TO-220/TO-247 to an SMD solution.

A further benefit is lower production cost due to machine assembly, with the wave soldering process already proven with several customers.

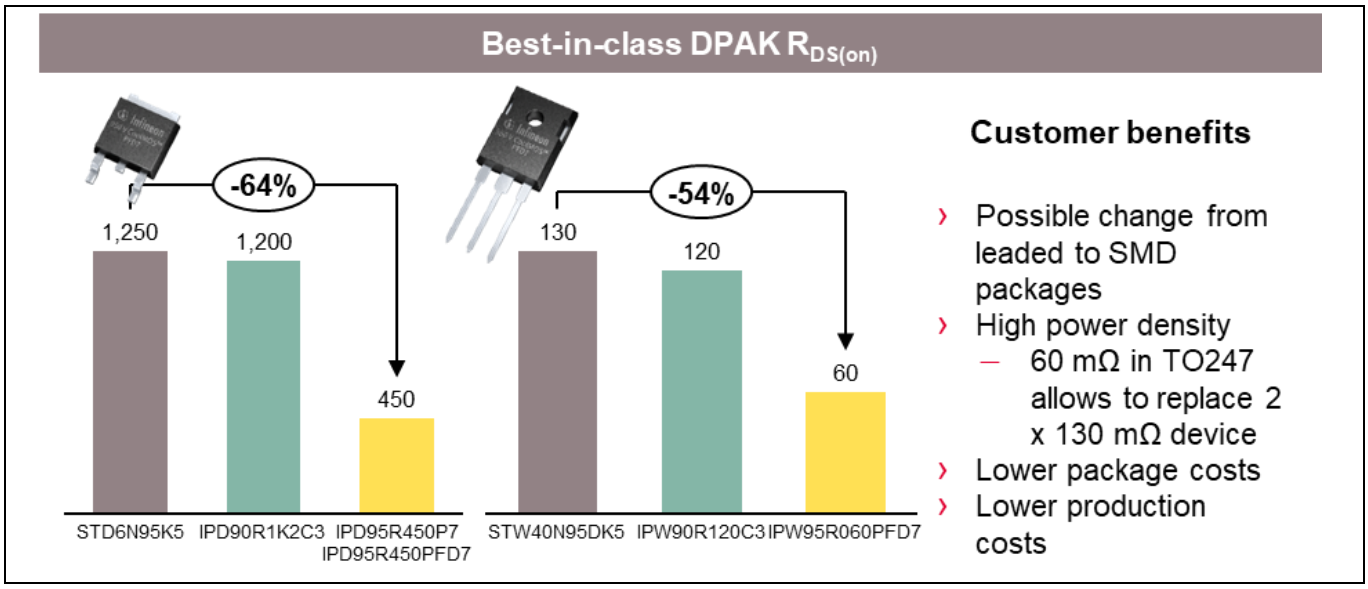

Figure 18 BiC $R_{DS(on)}$ for DPAK and TO-247

Before reading the final chapter, which includes some design recommendations and general rules, please note that there is a lot of additional material available for the 950 V CoolMOS™ PFD7, such as demo boards, simulation models, etc. These materials can be found on the **Infineon webpage**.

Note that Infineon currently does not offer bare dies for this product family.

5 Design considerations

This chapter describes design considerations for use with the 950 V CoolMOS™ PFD7.

5.1 Paralleling of MOSFETs

These applications typically do not use paralleled MOSFETs. However, to parallel MOSFETs, a gate bead is always recommended, depending on the parasitics of the PCB itself.

5.2 Source impedance (source bead)

Source impedances are used to slow down the di/dt on the drain path, resulting in a lower drain source overvoltage peak.

However, this also induces a voltage drop during turn-on and turn-off that can lead to oscillations in the gate drive loop. This influences the general EMI behavior and could also lead to the destruction of any MOSFET if this voltage oscillation drives the gate source voltage over +30 V or under -30 V.

Therefore, a source bead is not recommended to limit a possible overvoltage peak from drain to source. For more details and practical examples to optimize the EMI behavior of the MOSFET in the application, see the application note **Optimizing CoolMOS™ CE based power supplies to meet EMI requirements** from the former CE series. All optimization steps shown can also be used for Infineon's latest P7 technologies.

5.3 Target applications

The 950 V CoolMOS™ PFD7 is designed to be used in PFC as well as half- or full-bridge configurations, where the biggest differences to the well-known 950 V CoolMOS™ P7 are given. Both new technologies combined will partly replace the mature CoolMOS™ 900 V C3 technology in many applications.

6 Support material

Dedicated support material, not only for the 950 V CoolMOS™ PFD7 but also for the full P7 series, can be found at:

www.infineon.com/P7 and **www.infineon.com/950v-pfd7**

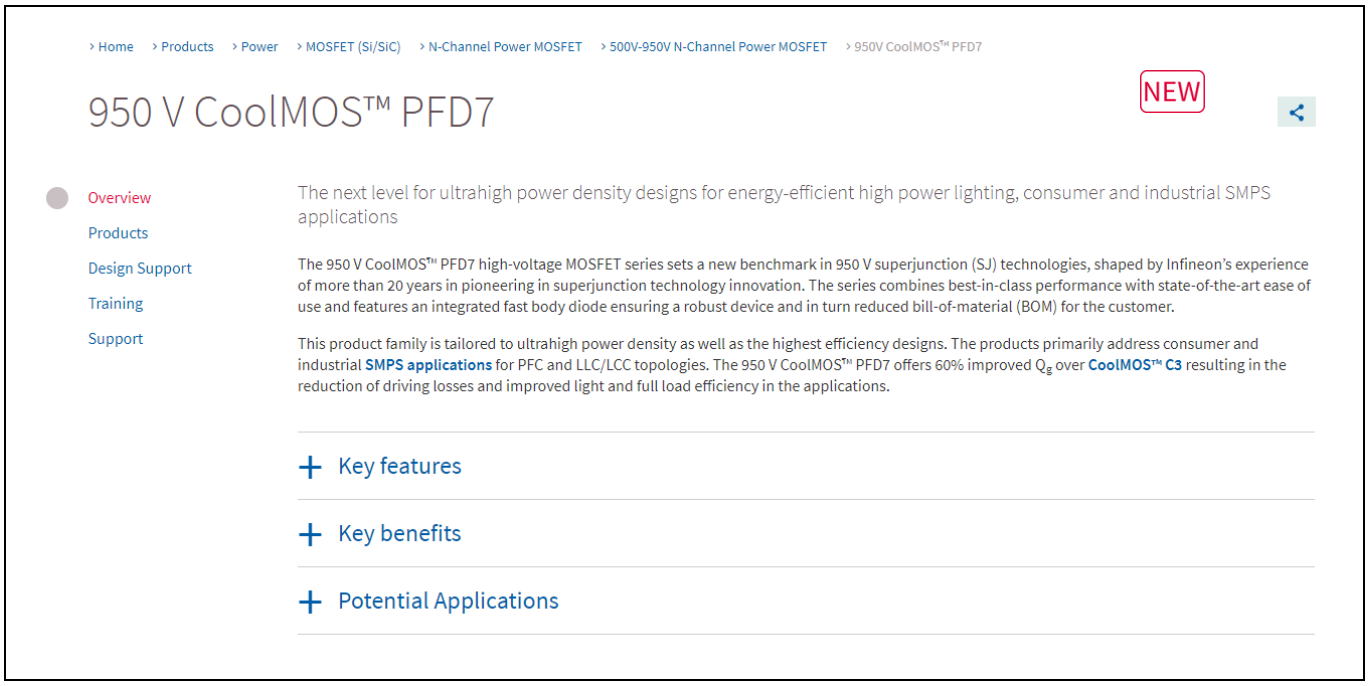

Figure 19 Dedicated PFD7 support material webpage

Under the section "boards" a dedicated board equipped with 950 V CoolMOS™ PFD7 MOSFETs can be found and ordered via the Infineon internal order system or as an external partner/customer via the online purchasing system at the end of 2022.

To make the design-in of our MOSFETs easier, the benefits of the 950 V CoolMOS™ PFD7 have been covered in detail.

Furthermore, Infineon Technologies offers controllers for a full system solution. A design tool can help especially in the starting phase of a new product design project.

This LCC design tool has been specifically developed for ICL5102HV (**Figure 20**), a combo controller for boost PFC + resonant half-bridge topology such as LLC and LCC. It can be broadly used for LED lighting and other power supplies where the system BOM cost, input power quality, power density, standby power and product reliability are critical design indices.

Based on ICL5102, several interesting reference boards have been designed for (but not limited to) LED lighting applications, to demonstrate the unique values that ICL5102 can deliver to customers. More details can be found in the design guide **Design of efficient LCC based on ICL5102/HV combo controller IC**.

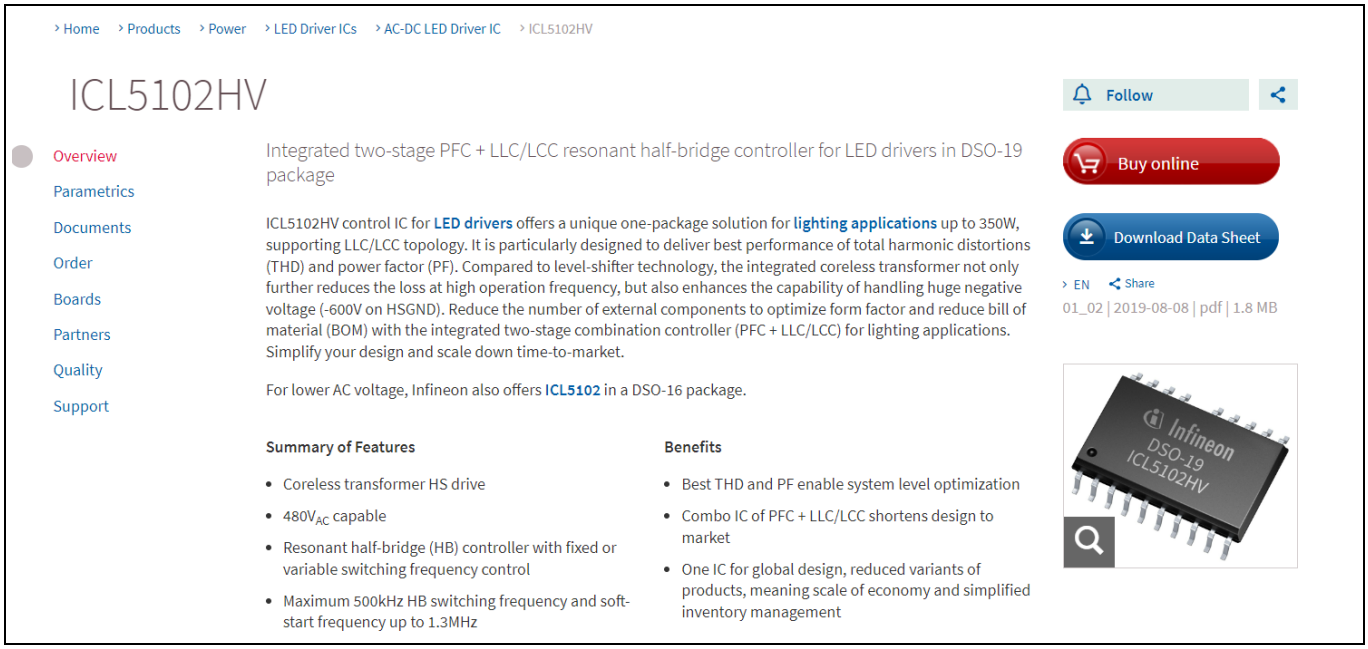

Figure 20 Support material for half-bridge controller fitting to 950 V CoolMOS™ P(FD)7 series

Revision history

Document version	Date of release	Description of changes
V 1.0	2022-10-17	Initial release

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Edition 2022-10-17
Published by
Infineon Technologies AG
81726 Munich, Germany

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Document reference
AN_2203_PL52_2210_121615

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