600 V CoolMOS™ CFD7 comes in a new top-side cooling package – the QDPAK

A further option for integration

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About this document

Scope and purpose

This document is intended to describe Infineon's latest top-side cooled (TSC) quadruple DPAK (QDPAK) surface-mount device (SMD) package for high-voltage (HV) applications, fitted with the high-performance 600 V CoolMOS™ CFD7 superjunction MOSFET.

The major advantages of a TSC SMD package for HV and high-power applications are the possibility of increasing power density to the next level, to enable low parasitic switching and reduced PCB temperatures, which you can read about in detail in the following chapters. The document will focus on applying the CoolMOS™ CFD7 in the HV QDPAK SMD package in order to increase power density and optimize switching performance.

Intended audience

This document is intended for SMPS designers and engineers who want to enhance their HV applications to achieve increased power density and the highest energy efficiency.

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1 Introduction

Every year, new benchmarks in terms of power density are set in worldwide SMPS developments. Infineon Technologies will further contribute to this trend, launching in 2021 a new TSC package – the QDPAK.

This trend of bringing more power into a smaller space/form factor is ongoing, enabling new levels of integration and previously unimaginable W/inch^3 power density ratings.

Fastest switching speeds, highest efficiency levels and optimized space usage with minimized total cost of ownership (TCO) are among the critical challenges facing today's power supply designers.

By driving down the on-state resistance, in our case with the latest 600 V CoolMOS™ CFD7 technology down to 15 mΩ, and further improvements in terms of gate charge and reduced switching losses, the latest superjunction MOSFET technologies in combination with enhanced CoolSiC™ diode technologies are the key to addressing challenges in modern hard- and soft-switching applications.

Until now the most common packages on the market have been the well-established through-hole devices (THDs), such as TO-220 and TO-247. Based on the steadily increasing requirements in the semiconductor market, a trend toward using SMDs to support fast-switching and reduce the parasitic inductance associated with the long leads on many THD packages can be seen. Despite all the advantages of the available SMDs, there is still a significant difficulty in terms of cooling. This remains one of the major challenges for high-power factor correction (PFC) circuits, and is the main reason that TO-220 and TO-247 are still the dominant package types used for high-power SMPS applications. In the DC-DC stage, like LLC or ITTF, SMD packages have already been used for years.

This application note will describe how the QDPAK, in combination with the latest 600 V CoolMOS™ CFD7, 600 V CoolMOS™ G7 and CoolSiC™ 650 V G6 technologies, offers the possibility to move away from THD packages toward SMD solutions, and further shapes the trend of highest efficiency and power density levels.

The new QDPAK is a further step toward full TSC system solutions, eanabling higher power levels and increased power density designs.

For a dedicated deep dive into the 600 V CoolMOS™ CFD7 technology, check out the latest **technology application note**.

1.1 600 V CoolMOS™ CFD7 applications and portfolio extension including QDPAK

Figure 1 shows the use of a full TSC SMPS solution with 600 V CoolMOS™ CFD7/600 V CoolMOS™ G7, with CoolSiC™ diodes from Generation 6, whereas the synchronous recitification (SR) stage will be completed with SMD OptiMOS™ 5 devices.

Furthermore, an application example was designed (QDPAK/DDPAK version) and will be shown in a later section of this document.

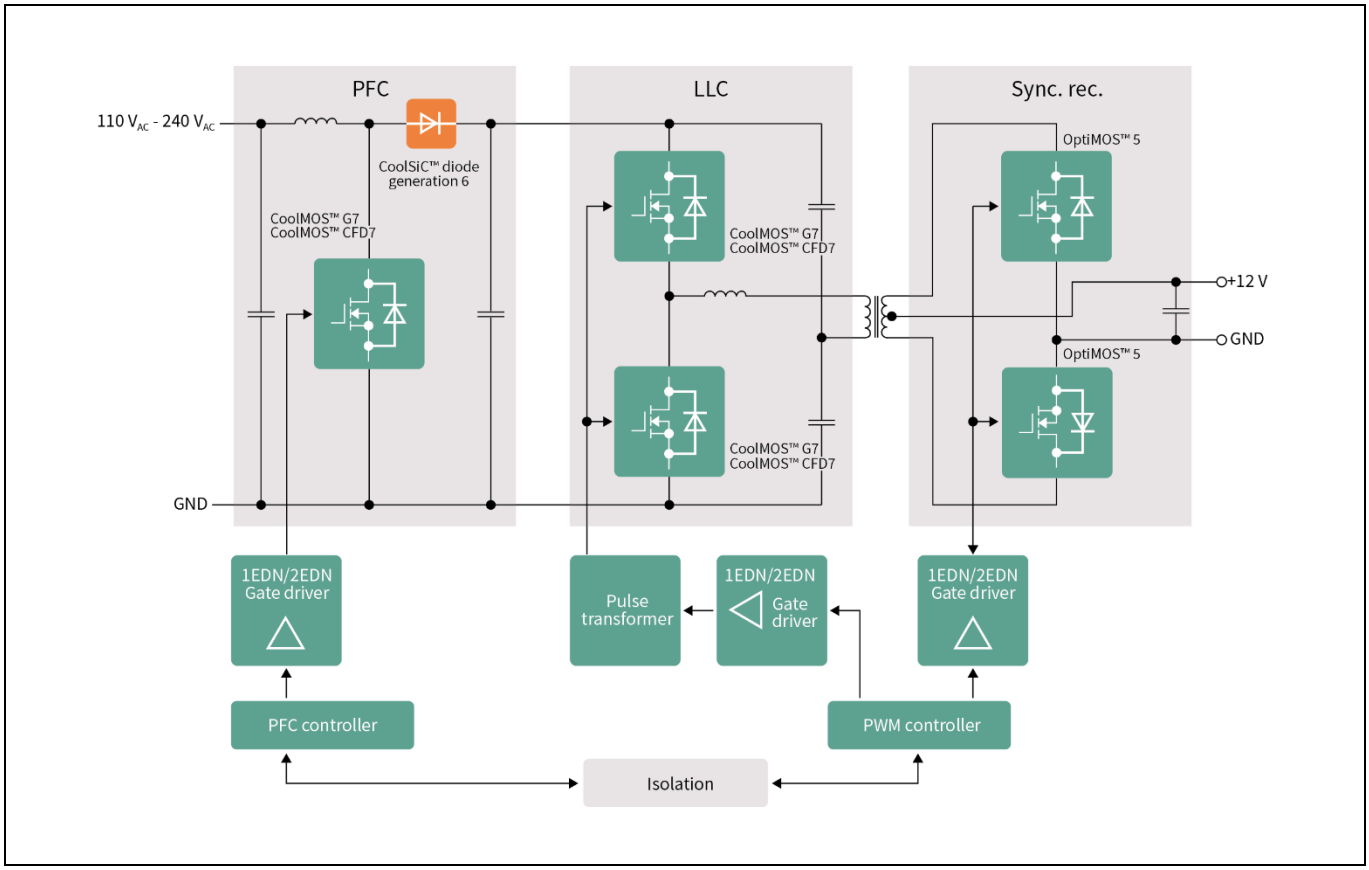


Figure 1 AC-DC stage with use of 600 V CoolMOS™ CFD7 in PFC and LLC stage

The 600 V CoolMOS™ CFD7 superjunction MOSFET is Infineon's latest HV superjunction MOSFET technology with an integrated fast body diode, completing the CoolMOS™ 7 series. It is the ideal choice for resonant topologies in high-power SMPS applications, such as **servers**, **telecoms** and **EV charging** stations.

The new **CoolMOS™ CFD7** is the successor to the **CoolMOS™ CFD2** superjunction MOSFET family. The CoolMOS™ CFD7 comes with reduced gate charge (Q_g), improved turn-off behavior and up to 69 percent lower reverse recovery charge (Q_{rr}) compared to the competition, as well as the lowest reverse recovery time (t_{rr}) on the market. These features mean the devices offer highest efficiency and best-in-class reliability in soft-switching topologies such as LLC and ZVS phase-shift full-bridge (PSFB). In addition, the CoolMOS™ CFD7 enables higher power density thanks to its optimized $R_{DS(on)}$.

All together, this latest fast body diode series brings clear benefits compared to competitor offerings by combining the advantages of a fast-switching technology with superior commutation ruggedness without sacrificing easy implementation in the design-in process.

If your design requires higher voltages, see our **650 V CoolMOS™ CFD7** superjunction MOSFET family.

Introduction

As well as all the known features and benefits of the 600 V CoolMOS™ CFD7 superjunction family, in 2021 Infineon is introducing the innovative QDPAK TSC package as part of the HDSOP family, addressing the most demanding application requirements for increased power density and thermal handling.

The QDPAK is a compact SMD, which can handle even higher currents compared to the well-known DDPAK and achieves a thermal performance comparable to a TO-247. The QDPAK leverages the full advantages of an SMD, limiting drawbacks such as heat spread through the PCB and enabling high flexibility in PCB design.

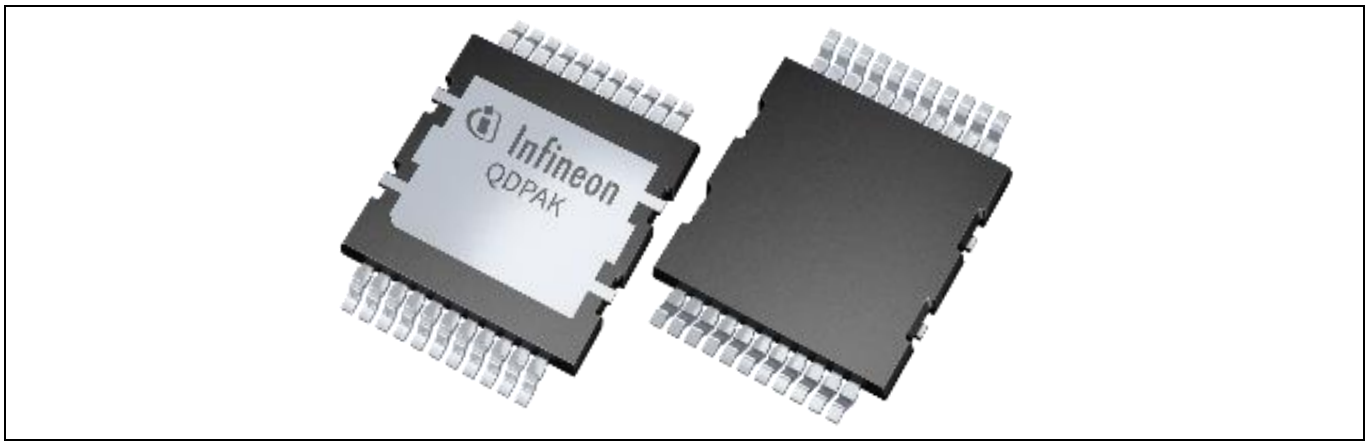


Figure 2 QDPAK package from Infineon

Figure 2 shows a front and back view of Infineon's QDPAK, where the solderable top side is connected to drain potential. The pin-out of the package is illustrated below (**Figure 3**).

This shows that the QDPAK comes with the well-established pin functionality, supporting low-inductive and low-loss driving.

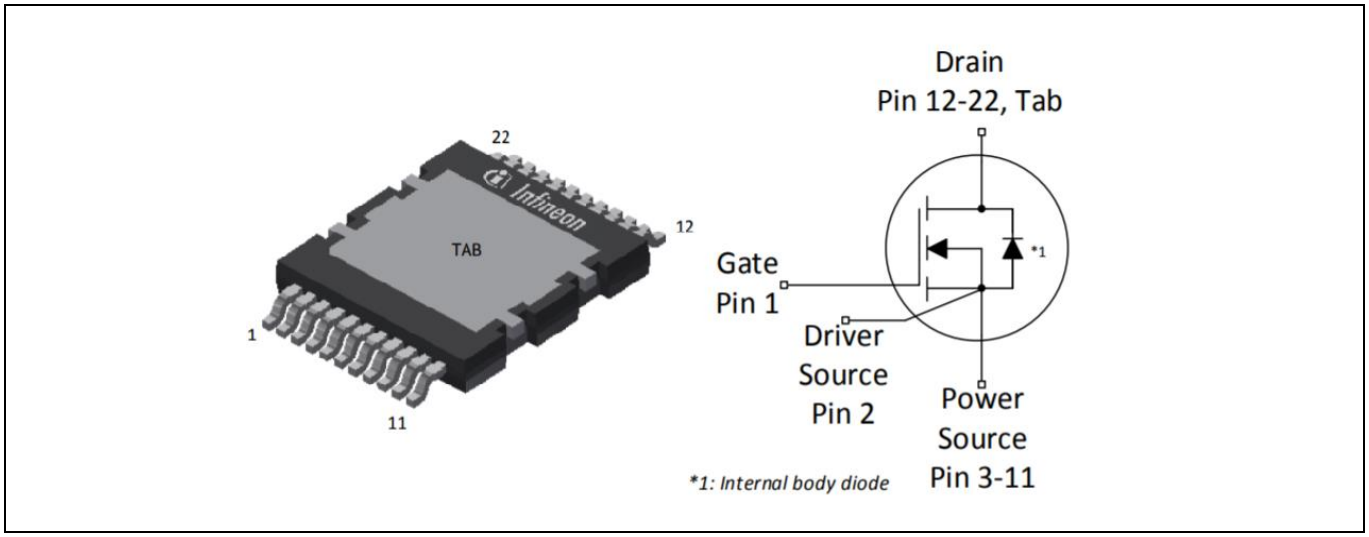


Figure 3 Pin-out of QDPAK package

Figure 4 shows the upcoming 600 V CoolMOS™ CFD7 QDPAK $R_{DS(on)s}$, giving the customer a broad and granular option to select the right product for the application and enable scalability of different power levels with SMDs.

Details of launch dates will be communicated via different internal and external channels. The first half of the portfolio, meaning 75 mΩ down to 35 mΩ, will be released in Q4 of 2021. For the lower part, 15 mΩ up to 25 mΩ, a release in early 2022 is likely. These last three $R_{DS(on)s}$ of the QDPAK portfolio will not only complete the rollout of this project, but will also be the last wave and release of the full 600 V CoolMOS™ CFD7 project.

600V CoolMOS™ CFD7

	$R_{DS(on)}$ max [mΩ]	Partname
QDPAK	75	IPDQ60R075CFD7*
	55	IPDQ60R055CFD7*
	45	IPDQ60R045CFD7*
	35	IPDQ60R035CFD7*
	25	IPDQ60R025CFD7*
	20	IPDQ60R020CFD7*
	15	IPDQ60R015CFD7*

*Coming soon

Figure 4 Portfolio – 600 V CoolMOS™ CFD7

1.2 Further Infineon products in TSC packages

1.2.1 600 V CoolMOS™ S7 (in QDPAK)

The 600 V CoolMOS™ S7 HV superjunction MOSFET family delivers the best performance for low-frequency switching applications at the best price.

Infineon's high-performing CoolMOS™ superjunction MOSFET technology makes it easy to design new high-power products with enhanced speed and superior quality. The S7 family of HV superjunction MOSFETs sets a new benchmark for power density, by uniquely fitting the smallest-known CoolMOS™ chip into an innovative SMD TSC package.

The highlight of this product family is the **IPDQ60R010S7**, which comes with an unprecedented $R_{DS(on)}$ as low as 10 mΩ, housed in a novel TSC SMD package.

- For further information, please visit the **S7 web page** and check out the latest **product brief**.

1.2.2 600 V CoolMOS™ G7 (in DDPAK)

The well-known 600 V CoolMOS™ G7 has been available in the DDPAK SMD package since 2018, meeting the needs of existing and future markets, and enabling a full system solution via TSC package types.

- For further information, see the **G7 web page**.

1.2.3 CoolSiC™ Schottky diode 650 V Generation 6 (in DDPAK)

Infineon Technologies introduced double DPAK (DDPAK) in 2018, which was the first TSC SMD package to address high-power SMPS applications such as PC power, solar, servers and telecoms. The benefits of the existing HV **CoolSiC™ Schottky diode 650 V G6** technology is combined with the innovative concept of top-side cooling, providing a system solution for high-current hard-switching topologies such as PFC and a high-end efficiency solution for LLC topologies.

- For information and collaterals, see: **https://www.infineon.com/coolsic**
- Additional benchmarking is available inside all demo board application notes from CoolSiC™ G6 and 600 V CoolMOS™ G7: **https://www.infineon.com/demoboards**

2 QDPAK as a perfect fit for latest-generation MOSFETs

The latest 600 V CoolMOS™ CFD7 in QDPAK enables a new approach to systems in high-power density SMPS solutions with TSC SMDs.

The QDPAK dimensioning and the benefits of a power device in a TSC SMD package are described in the **first subchapter** of this section. The positive standoff, minimal creepage and clearance distances of the package, which must be considered by the system manufacturer, are also described.

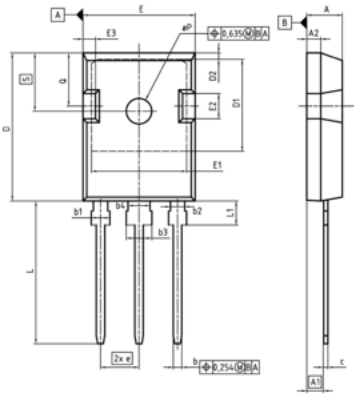
All mechanical details shown in the following chapters and a general recommendation for how to handle Infineon's SMDs can be found at **https://www.infineon.com/packages**.

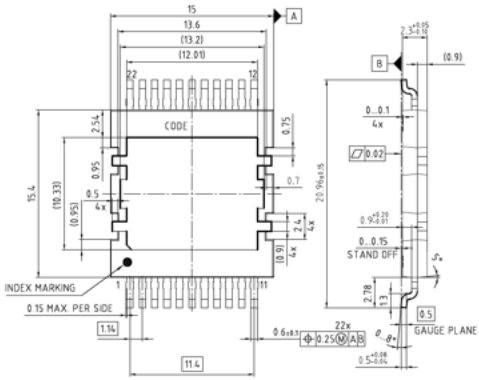
Detailed mechanical information about the QDPAK (PG-HDSOP-22-1) is also available **here**.

2.1 Package dimensioning and SMD "replacement" for TO-247

It's clear that switching from a leaded package to an SMD package results in a smaller form factor and less height, but requires different cooling concepts.

Whether horizontal or vertical, the positioning inside the SMPS is most often driven by the cooling concept. With the new TSC QDPAK (and DDPAK), new methods of cooling and new form factors can be included in the design.





	TO-247	QDPAK
Outer dimensions	15.92 mm x 20.95 mm	15.00 mm x 15.4 mm
Outer surface	333.5 mm²	231 mm²
Heat slug dimensions	13.63 mm x 16.95 mm	12.01 mm x 10.33 mm
Heat slug surface	231 mm²	124 mm²
Thickness	5.02 mm	2.3 mm

Figure 5 Package dimensions (TO-247 vs. QDPAK)

The reduction in height and inductance gives the designer the opportunity to make the design much thinner and much more power-dense.

The reduced cooling area seems to be a drawback at first, but the reduced R_{thJC} (which is directly related to the heat transfer from chip to package) and a proper cooling concept (as shown in the application section later on) result in nearly equal performance, with the benefit of a much more compact realizable size.

In the thermal design of the power board itself, a lot of boundary conditions must be considered.

A thermal optimization on the MOSFET level in a dedicated application requires the lowest possible thermal resistance of the overall system (R_{that}) in combination with the highest possible junction temperature (T_j) of the switching devices.

This can be reached by:

- maximizing the heat flow into the heatsink
- minimizing the heat flow into the PCB

As the DDPAK and QDPAK are decoupling the heat generated in the MOSFET from the PCB itself, the main cooling path has to be enabled via the top side of the package. What this means and how much of a temperature difference (between MOSFET and PCB) can be expected is shown in **Figure 25**.

2.2 Positive package standoff

As already described and discussed in the **DDPAK application note**, the pins of the package concept (DDPAK + QDPAK) are acting like springs. For industrial applications it is known that this can be beneficial in terms of reliability and aging of solder connections.

The TSC SMD device QDPAK comes with the industry standard of a positive standoff. As shown in **Figure 5** and in the outline drawing in **Figure 8**, the positive standoff is 0 to 150 µm.

The positive standoff also enables easier assembly of the QDPAK. The device only needs to be picked up and placed on the PCB, before the devices can be soldered via reflow soldering. In comparison, the leads of a common THD such as TO-247-3 must be bent if a small form factor with reduced height is needed. The lead-bending process increases the stress on the leads, and may also cause failure due to stress on the casing.

Another advantage is the reduced risk of particles underneath the body of the package. With a positive standoff, no board cleaning is required before the SMD device is placed on the PCB for reflow soldering. This enables direct contact between the pins and the solder stencils. Furthermore, the positive standoff gives the possibility of using adhesion between the bottom of the package and the PCB. The QDPAK device can be fixed with an adhesive material (e.g., SMD glue) to the board, avoiding dropping down of the device when parts on the other side of the PCB are mounted with reflow soldering. The package can be reflow soldered three times, which may be necessary if SMD devices are placed on both sides of the PCB or an additional heatsink is placed on top of the package.

The right size and position of the adhesive material can also increase the temperature cycling on-board (TCOB) reliability of the package. Please refer to **chapter 4.2** for more detailed information on TCOB reliability with compression of the device.

Taking everything into account, it can be summarized that the SMD solution enables a fully automated manufacturing process. The positive standoff reduces the cost of the assembly process while reducing yield losses for the manufacturer.

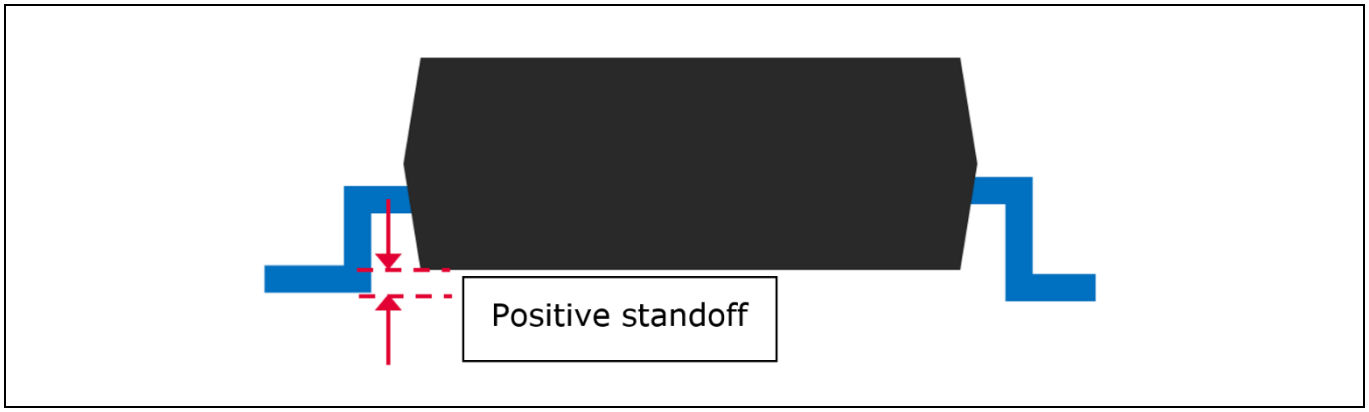


Figure 6 Positive package standoff (DDPAK + QDPAK)

Advantages of the positive standoff can be summarized as follows:

- Easy to use (standard machine assembly process can be used – faster, cheaper)
- Reduced risk of particles underneath package body
- Reduced manufacturing costs (no bending of THD needed to achieve a slim form factor)
- Improved quality (solder inspection possible at the leads)

2.3 4-pin functionality included

The new QDPAK package, like the DDPAK, comes with proven 4-pin functionality. The separate source-sense connection allows low-loss driving of the MOSFET, enabling higher switching speeds and resulting in greater efficiency compared to packages without this feature. This can be seen in **Figure 3** and **Figure 7**, pin number 2.

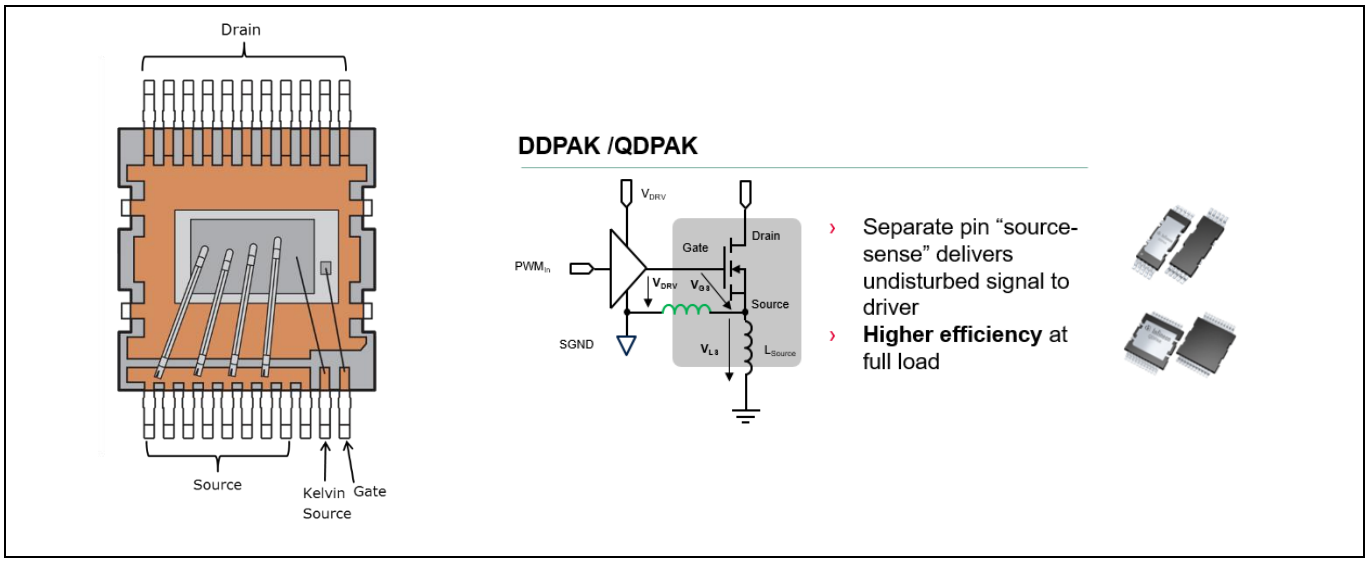


Figure 7 QDPAK source-sense (Kelvin source) capability (flipped view)

For further information, please see chapter 2.3 in the **DDPAK application note** from Infineon.

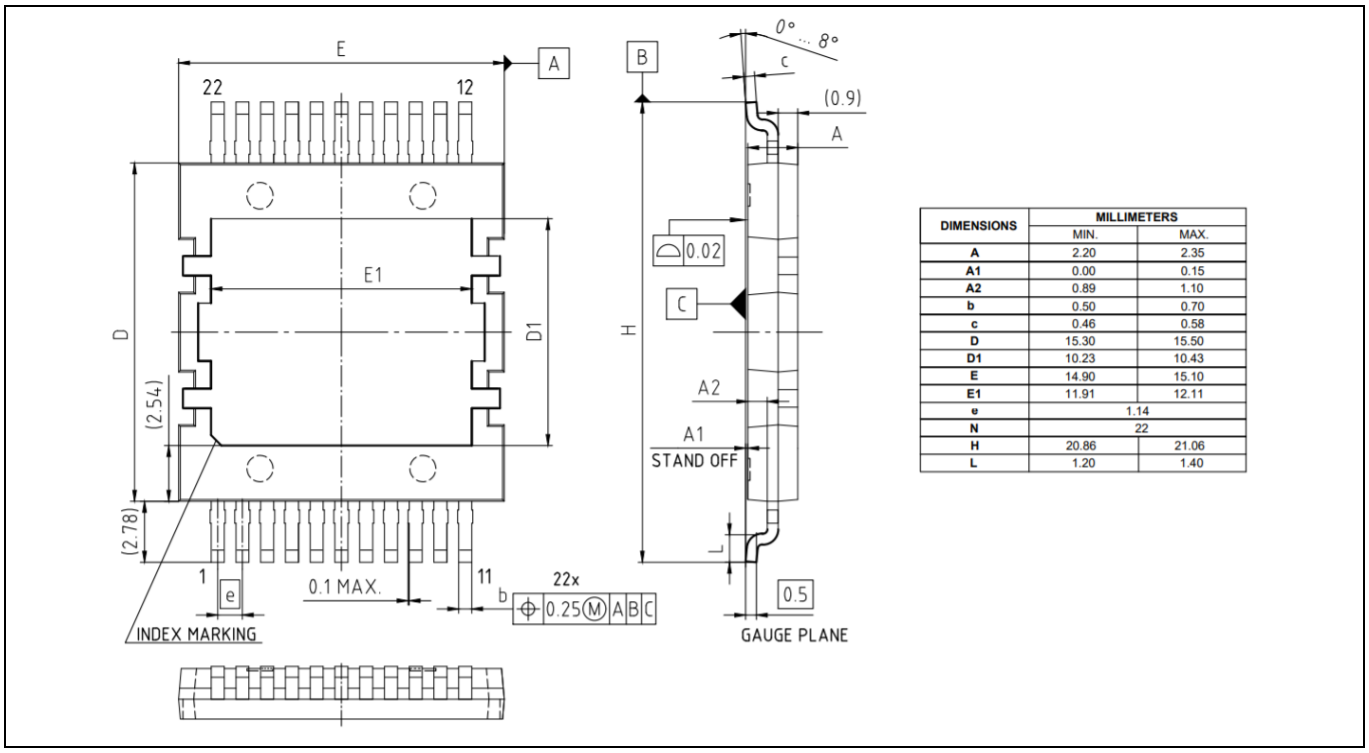
3 Assembly considerations for the QDPAK

The assembly process for SMDs offers advantages in mass production. First, SMDs save space on the board, and second, the placement can be automated (most THDs are inserted manually, which increases cost and reduces quality as well as reliability).

The PCB design and construction are key factors for achieving highly reliable solder joints. For example, TOLL packages should not be placed in the same location on opposite sides of the PCB (if double-sided mounting is used), because this results in a stiffening of the assembly, which can lead to earlier solder joint failure compared to a design where the component locations are offset. Furthermore, it is known that board stiffness has a significant influence on the reliability (temperature cycling) of the solder joint, if the system is used in fluctuating temperature conditions.

For a QDPAK/DDPAK package, this has no influence at all because the package and PCB are decoupled from each other with the positive standoff (A1 in **Figure 8**) featured in these package types (typical ~100 µm, maximum 150 µm). Furthermore, the leads act like little springs, giving an additional advantage over other SMD variants.

The outline of the QDPAK device is shown in **Figure 8**. More detailed information about the physical dimensions is available in the relevant datasheets available on the **Infineon website**.



DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	2.20	2.35
A1	0.00	0.15
A2	0.89	1.10
b	0.50	0.70
c	0.46	0.58
D	15.30	15.50
D1	10.23	10.43
E	14.90	15.10
E1	11.91	12.11
e	1.14	
N	22	
H	20.86	21.06
L	1.20	1.40

Figure 8 Outline drawing of the QDPAK (PG-HDSOP-20-1), dimensions in mm

For the solder process itself **Figure 9** illustrates the recommended PCB pad designs (including appropriate dimensions) for the QDPAK. This design is also used for TCOB testing according to IPC-9701 standards at Infineon. Please note that the recommendations can only give dimensions for the solder-mask openings. Generally, the copper dimensions depend on the capability of the board manufacturer. For high-current applications, the copper dimensions for drain and source pads should be as large as possible to increase the conductor's cross-sectional area.

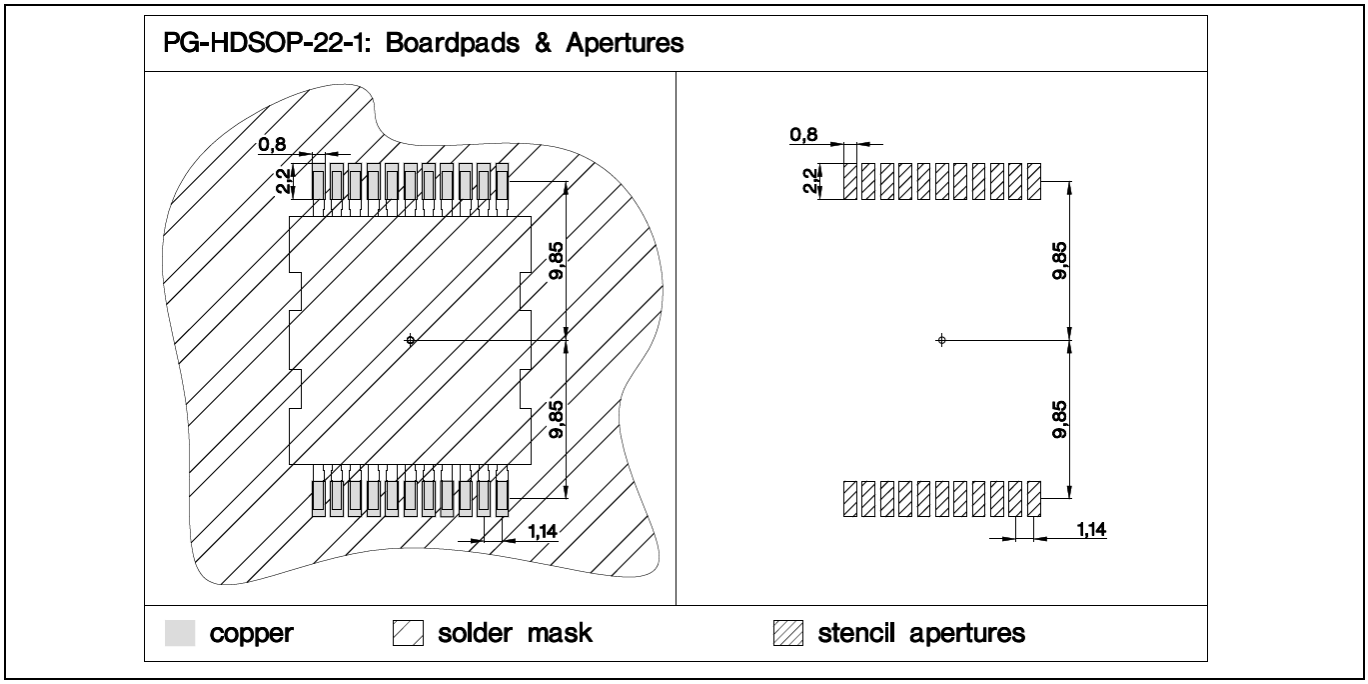


Figure 9 Footprint and stencil recommendation for PCB assembly

In **Figure 9** the final footprint and stencil recommendations for the PCB assembly are shown. For more details and tolerances check the last page of the final datasheets (also check the revision number) for the specific part in the dedicated DDPAK package. The drain copper area on the top side of the DDPAK package further allows a direct soldering of the external heatsink. An example buildup with the QDPAK soldered onto the PCB, including a small copper heatsink on top, is shown in **Figure 12**. The stencil recommendation for this can be found in **Figure 10**.

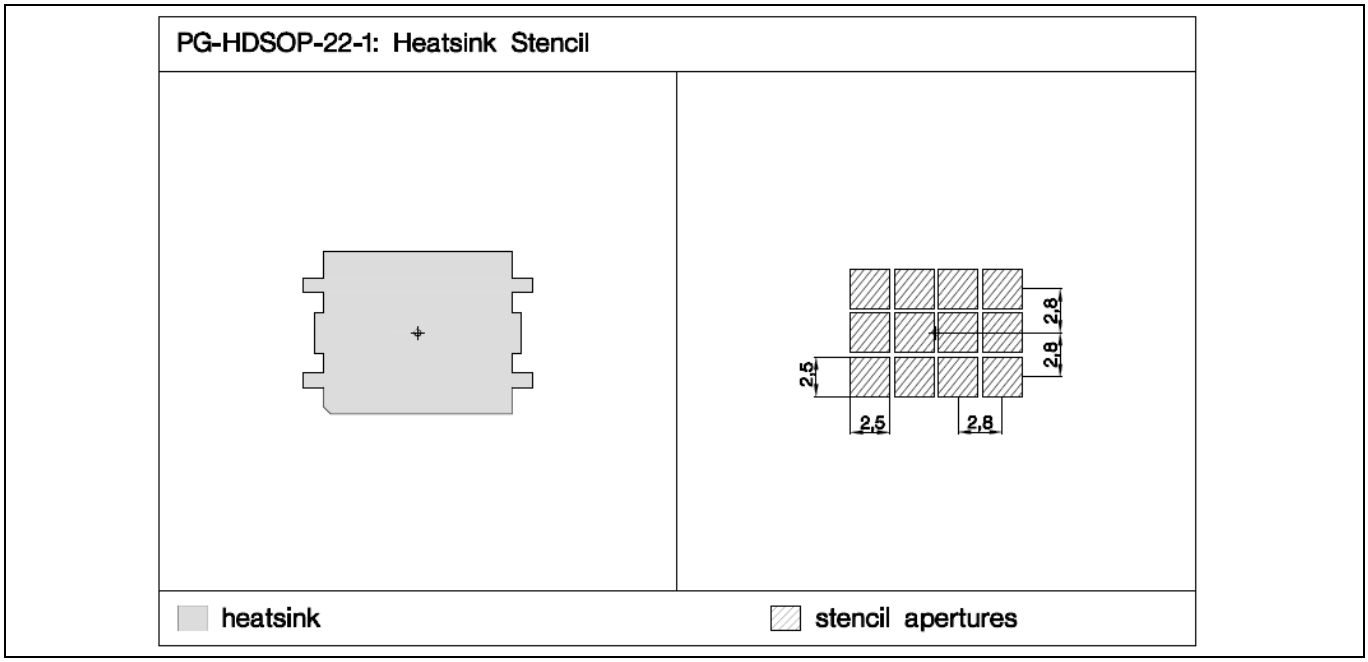


Figure 10 Heatsink stencil recommendation for top-side soldering (drain potential)

For further information, a separate application note describing the same general recommendations for the assembly process can be found **here** (“General Recommendations for Assembly of Infineon Packages”).

3.1 Top-side soldering investigations

Recent decades of high-power SMPS development have been dominated by the trend toward higher power density and cost optimization. Fastest switching and highest efficiency as well as optimized board space at minimized TCO are among the critical challenges facing today's high-power supply designers.

Considering the steadily increasing power density requirements, customers are looking for even smaller packages, as the target is to keep the form factor stable but increase the output power level or reduce the form factor while keeping the output power stable.

The reduction of the package size goes hand in hand with cost, and therefore the package selection is key to enable an overall reduction in the bill of materials (BOM).

Different types of mounting, starting with standard through-hole assembly (e.g., screwing TO-247 to heatsink) in the horizonatal direction, toward SMD packages in the vertical direction (already benefiting assembly cost and handling effort), means the TSC packages have now guided the industry toward higher power density and easier, faster and more automatized assembly methods. This evolution is illustrated in **Figure 11**.

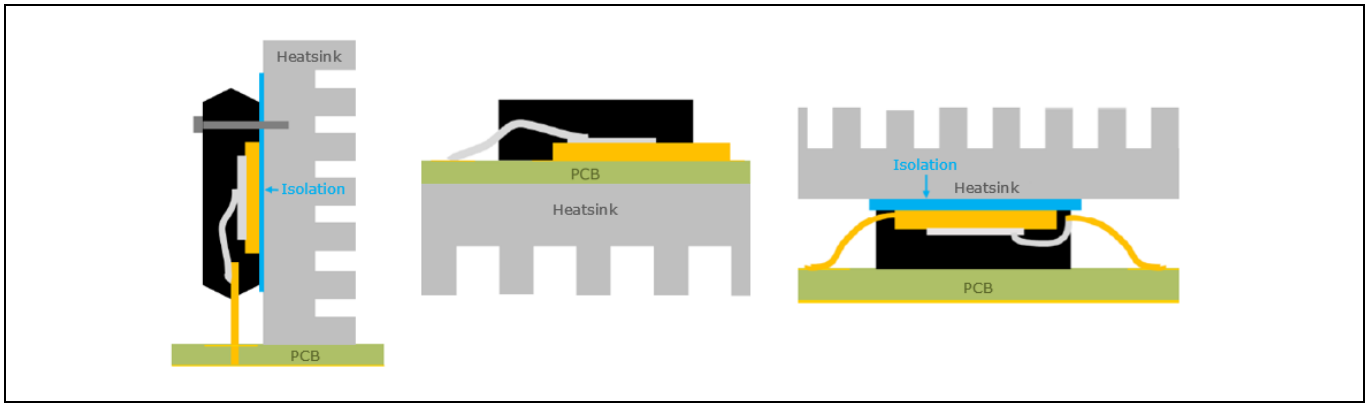


Figure 11 Evolution in cooling packages (THD – SMD – TSC)

Power dissipation is linked to the thermal capabilities of a package; both are important for the performance. Therefore, depending on the power range of the designed application, larger or smaller packages are chosen.

The following chapters cover the special characteristics of the new QDPAK package, supported by practical examples and visualizations. Many of the methods described are applicable to other TSC packages from Infineon Technologies, and are also discussed in the **DDPAK application note**.

3.2 Solderable top side

The heatsink on top can be soldered via a second reflow process (first, package to PCB; second, heatsink on top of package. Or vice versa, depending on manufacturing capabilities – remember to inspect the solder).

All our TSC packages described here offer a solderable top side, which means a heatsink can be soldered directly to the top side of the package in a separate soldering process in production. A T-shaped heatsink is recommended, as the heatsink should not overtop the leads of the package (creepage/clearance). Additional isolation from the surroundings or a housing is necessary, as the top side of the solderable package is on drain potential (HV).

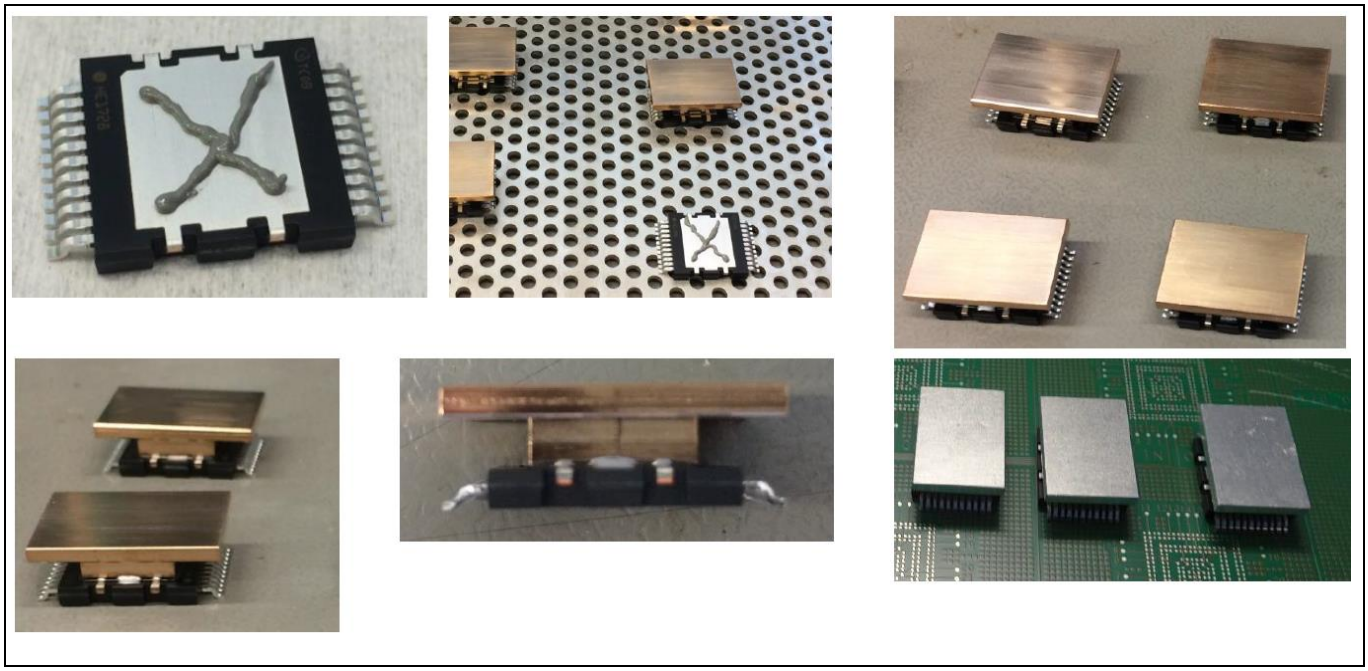


Figure 12 Copper heatsink (T-shape) for QDPAK package (heatsink should not overtop pins)

Figure 12 shows the steps from the individual part to the final assembled component, with a heatsink on top, mounted on the PCB itself, starting with applying the solder on the top of the package, followed by a reflow solder step where the package is connected with the copper heatsink. After cooling down, the heatsink is connected to the MOSFET and a solder inspection can be carried out on both sides. As a solder material with high melting characteristics was used, a second solder step can follow with a lower solder melting temperature to assemble via a reflow step on the PCB.

In **Figure 13**, a schematic buildup of a single heat spreader (vaild for DDPAK and QDPAK) is described from the bottom up to increase the thermal performance of a single package:

- PCB
- Package
- Interconnect material (~20 µm solder)
- Heat spreader (Au, Cu…) attention: HV potential

With/additional:

- Isolation foil (e.g., K10 with 152 µm)
- Customer cooling (e.g., water cooling, standard heatsink or system housing)

By assembling the complete structure as described, a full system solution can be realized. Depending on the thermal characteristics of each step (material), the performance of the system can be optimized.

Thermal simulation can help the customer avoid thermal hotspots inside the system. This is especially important when placing packages side by side (paralleling over top-side solderable copper plate). Monitoring the temperature of the central components is a safe method to avoid overload or thermal runaway of the system itself. In many cases it is possible to keep a hole directly below the packages so that a thermal resistor can be placed from the back side directly on the package.

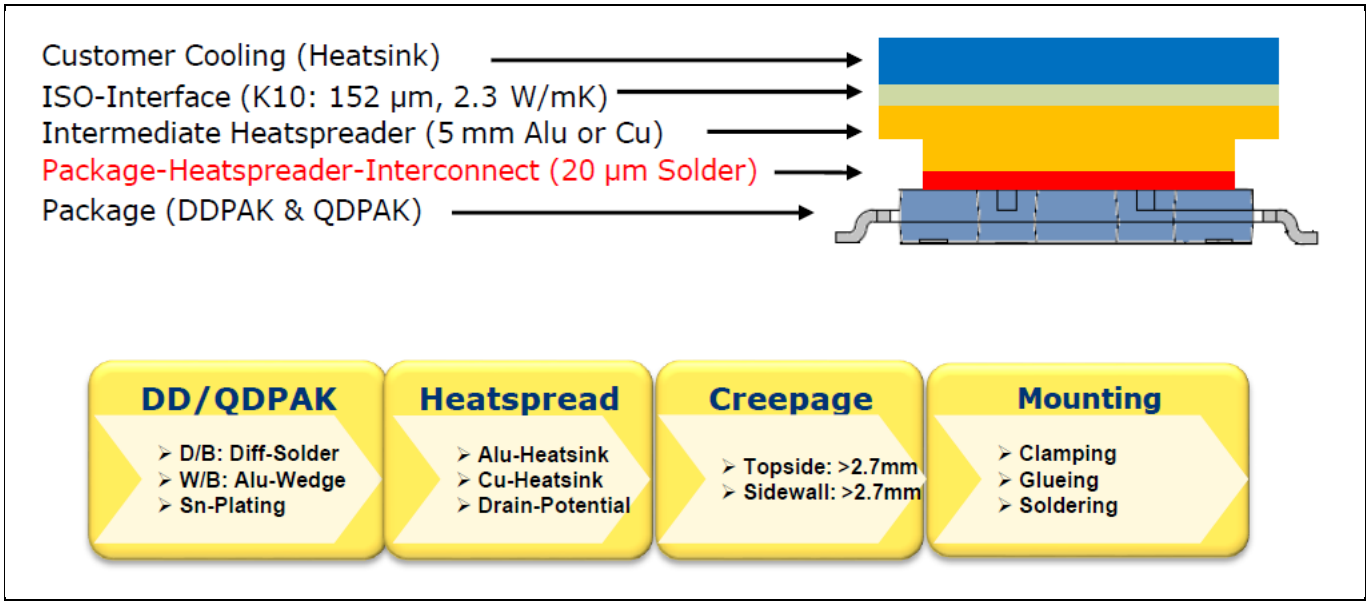


Figure 13 Single-device heat spreader mounting (schematic)

3.3 Connection via push-pins

As already shown with the DDPAK (chapter 4.2.2 in the **DDPAK application note**) heatsink mounting via push-pins is also possible for a full system solution. This method benefits the overall system height.

Small bolts with springs press the heatsink toward the packages, mounted via holes in the PCB. As an example, push-pins are widely used in desktop PCs to connect a heatsink with thermal isolation material in between.

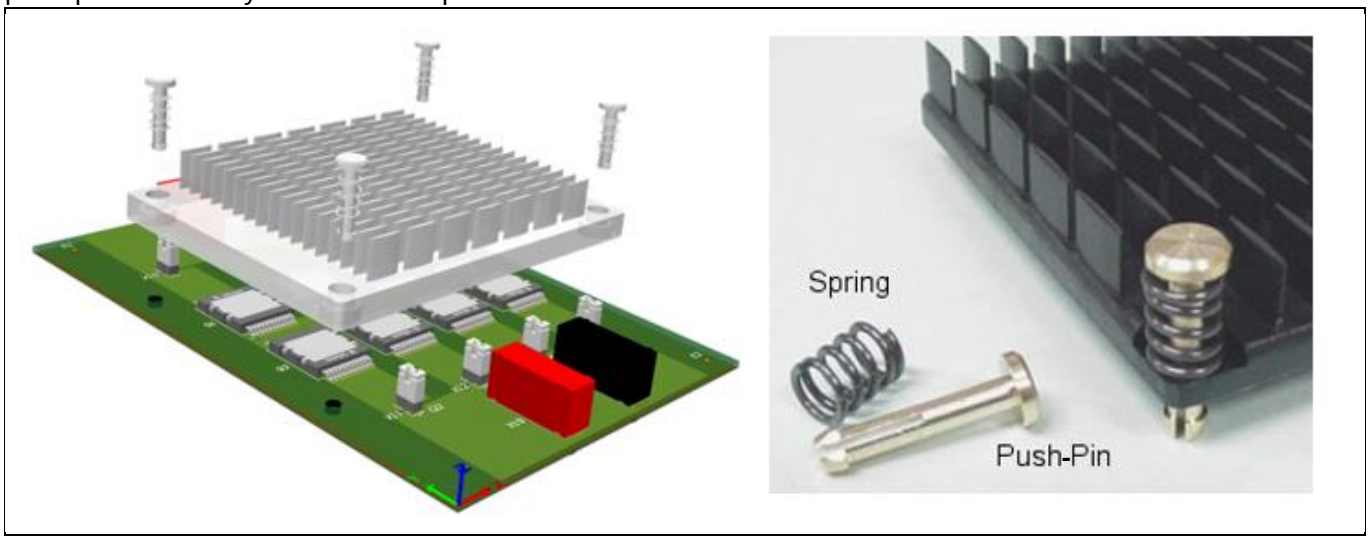


Figure 14 Mounting of heatsink via push-pins

3.4 Standard mounting of heatsink with screws

Screw down the heatsink to the PCB, including thermal interface material (TIM), with screws and adequate force. The screwing force and hole positioning must be well chosen (bending/warpage of PCB must be considered; homogeneous cooling of all components must also be ensured via the correct foil thickness – tolerances of all packages have to be known and evaluated).

Figure 15 Standard mounting via screws

3.5 Clip mounting

The standard clip-mounting method is also common in the industry. Clips with a special spring force are used. Size and strength depend on the number of components, thickness of the PCB, component height, and thermal performance of the TIM (force vs. thermal resistance). A modular approach, which can be used in mass production where power levels are scaled over daughter cards (using different power MOSFETs $R_{DS(on)}$ and diode current ratings), is also possible.

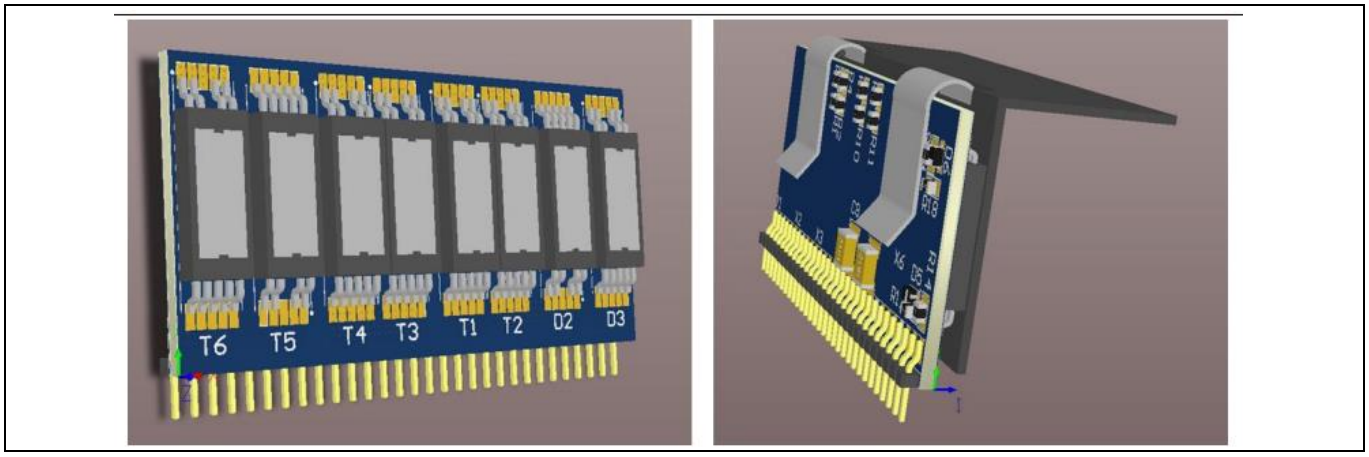


Figure 16 Clip mounting of heatsink to PCB, applicable for DDPAK and QDPAK (with isolation foil in between)

3.6 Cooling via thermal adhesives (e.g., Bond-Ply®)

Another option would be the connection between MOSFET and heatsink, with a pressure-sensitive adhesive tape self-fixing isolation foil without the use of special fasteners or springs.

An example solution is Bond-Ply® tape, which bonds strongly to a variety of surfaces, as shown in **Figure 17** (blue foil).

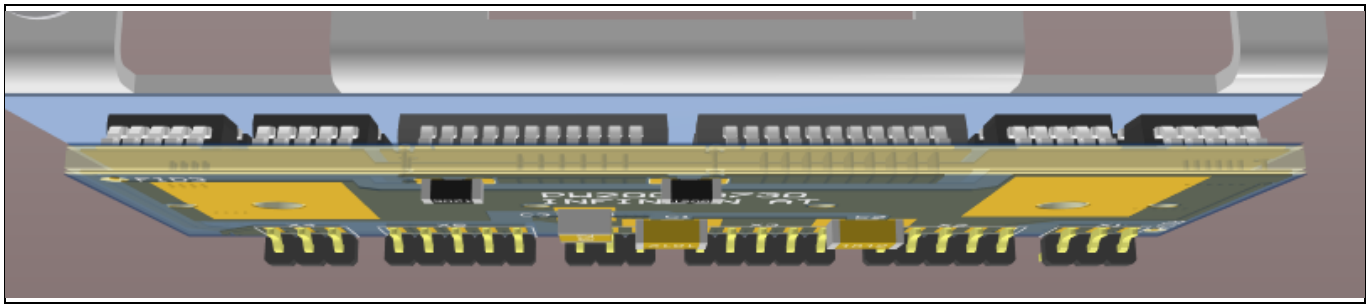


Figure 17 Bond-Ply® mounting of DDPAK and QDPAK package to heatsink

More details on the different variants and thermal characteristics of such materials can be found here:

- e.g., Henkel™/Bergquist™ Bond-Ply®

Liquid adhesives create a mechanical attachment between a component and a heatsink. Additionally, the thermal transfer properties are guaranteed, and additional fasteners are not needed.

Furthermore, the low-modulus silicone design effectively absorbs mechanical stresses induced by the assembly process, as well as shock and vibration, while providing exceptional thermal performance and long-term reliability. The correct thickness of the isolation material itself (able to compensate for all tolerances) must be considered carefully.

3.7 Combination of isolation foil and gap-filler

Compensation for bigger height differences can be achieved via a standard isolation material (for electrical isolation of the component's top side – it can be ultrathin) combined with a gap-filler (to ensure proper cooling of all components).

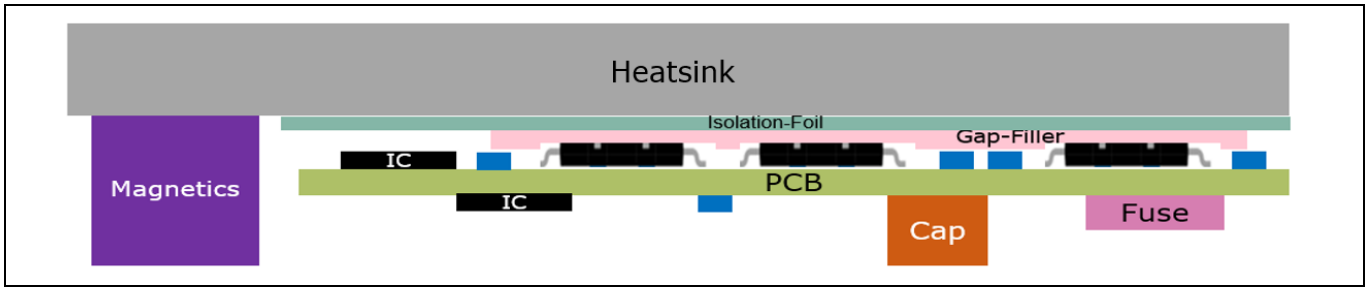


Figure 18 Full SMPS mounting (with gap-filler, isolation foil, MOSFETs, IC, passives, heatsink)

As the customer is also likely interested in mass production, the most common solution is a combination of isolation materials and gap-fillers. The big benefit is the option to also overcome larger tolerances of packages and the different package heights of power MOSFETs and other SMD components used.

In terms of structure, the following arrangement of components is suggested:

- Position the isolation foil (~100 µm) on the heatsink (this provides the electrical isolation for the system).
- Mount all SMD components (both sides possible, as QDPAK allows reflow soldering three times).
- Assemble the gap-filler material (~500 µm or more) on the top side of the power components.
- Mount the heatsink with isolation foil on top of the gap-filler.
- The most common mounting technique for this approach is screwing the PCB to a cooling plate or housing.

3.8 Soldering specifications

One of the most important specifications, which is also stated in our datasheet, is for the soldering technique. For QDPAK and DDPAK Infineon recommends reflow soldering only.

The result if wave soldering is used without any special solder masks (as used when soldering SMDs combined with microcontrollers or processors) can be seen in **Figure 19**.

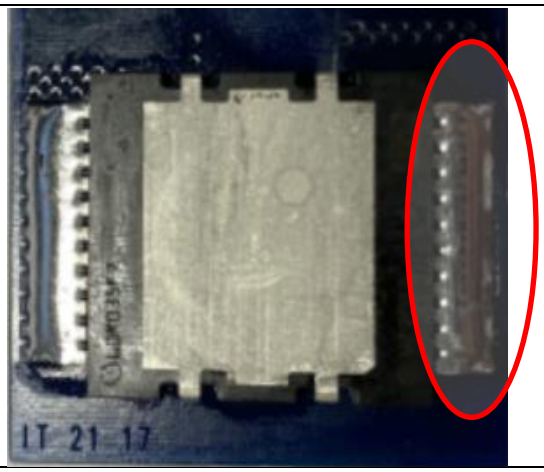


Figure 19 Short on pins due to wave soldering

All pins are shorted, and this will cause a failure (if not detected via the solder inspection) immediately on first turn-on of the MOSFET. This is why Infineon recommends reflow soldering of the DDPAK and QDPAK package only. The specification for soldering can be found in the dedicated datasheet for the product, and is also shown in **Figure 20**.

Reflow soldering temperature	T_{sold}	-	-	260	°C	reflow MSL1

Figure 20 Reflow soldering temperature specification in datasheet (DDPAK and QDPAK)

A reflow process with the QDPAK devices (PG-HDSOP-22) has been executed to evaluate the feasibility of reflow soldering.

The specification and the temperature profile used for the reflow soldering process are shown in the following figures (**Figure 21** and **Figure 22**).

Topic	Description		Comment
	Value	Unit	
Stress Boards			
Board material	high T_g FR4	-	
Board thickness/ layer	1.6 mm/ 4-layer	-	
Finishing	Chem. Sn	-	
Solder material	SAC305	-	
Stencil thickness	120	µm	

Figure 21 Specification of QDPAK stress boards (in-house)

Special test boards have been produced to standardize the testing, ensuring it reflects actual customer usage and requirements.

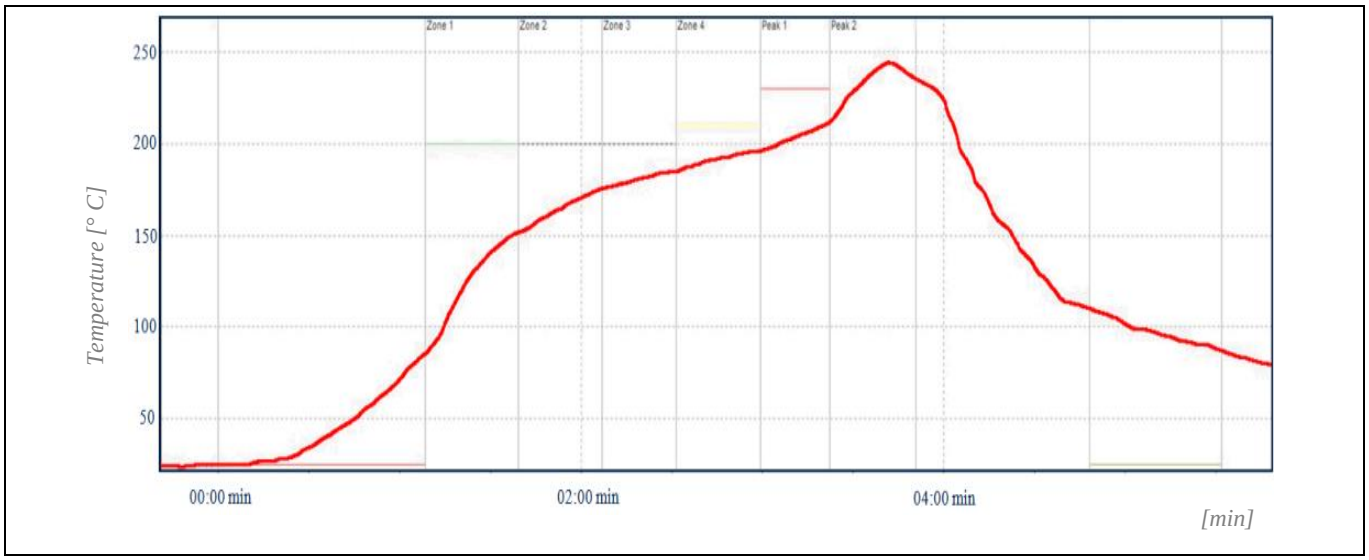


Figure 22 Temperature profile of reflow soldering process for QDPAK package

As a further feature, the QDPAK package is released for three-times reflow solder process, enabling customers to mount not only the package to the board itself, but also to make the soldering of heatsinks on top possible, not damaging the chip or mold compound with additional thermal stress.

After all tests have been processed, and x-ray and visual inspections have been done, the results can be seen in **Figure 23**. No issues or electrical failures appeared. For the design-in phase, it is recommended to check the soldering process carefully to avoid later failures in the field, especially when a heatsink on top is used for cooling. The extra weight of the heatsink must be considered, as well as the allowed solder void rates.

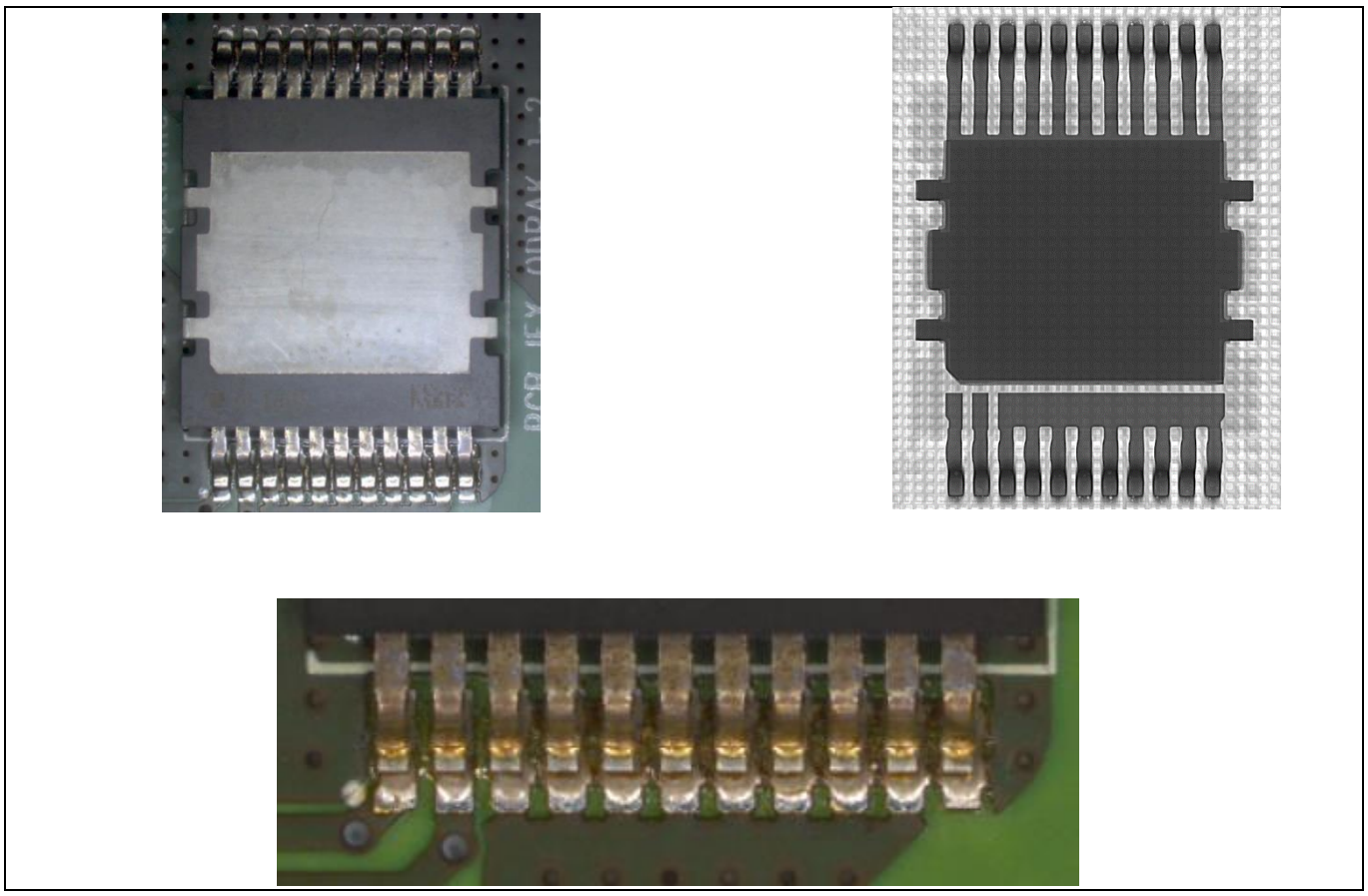


Figure 23 Optical image top view, x-ray image after reflow soldering, and optical microscope image

In summary, this is a mandatory test to proof the solder joints after the soldering process, and to reduce customer effort in the solder inspection steps (can be done optically via automatized processes in the manufacturing line).

Conclusion:

- Solder void check within typical voiding rate (maximum 30 percent)
- Good solder joint quality for both SAC and Pb solder on FR4 PCB
- Good reproducible results for standard reflow soldering process
- No rotation/tilting of devices during soldering process
- No short on the leads; electrically functional afterward

3.9 Special focus – tie-bars

Based on past experience, the so-called tie-bars warrant a closer look. To eliminate some concerns about the construction of the top-side of the package, **Figure 24** shows a close-up and detail view of that section of the package top-side.

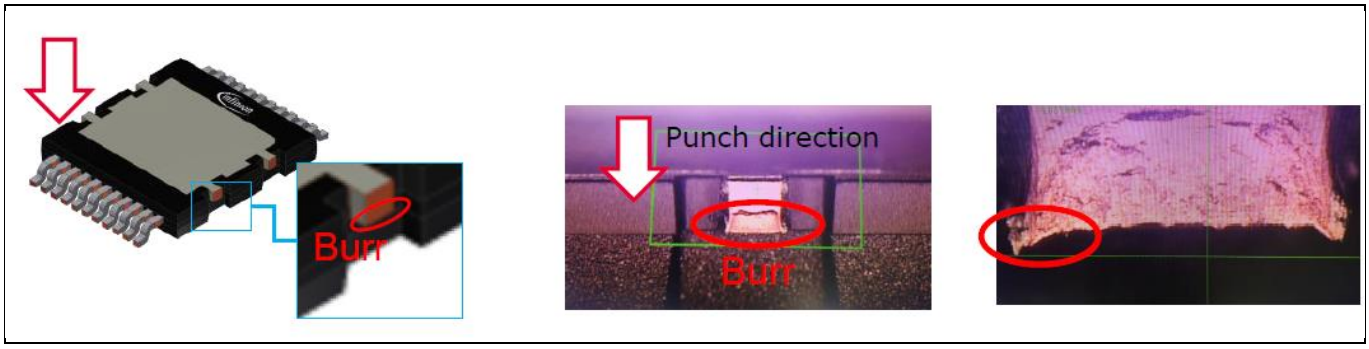


Figure 24 Tie-bars of QDPAK including punch direction (top down)

In the past there have been concerns that the stamping direction of the metal leadframe leads to the creation of small burrs, which can destroy or crack the isolation foil. These have been analyzed, and the direction of stamping was adapted accordingly.

In fact, the stamping direction from the bottom up can lead to small burr cuts into the isolation foil, which results in a reduction of the isolation strength. As the packages are pressed toward the foil during the final assembly/mounting process, an issue can arise due to vibrations or simply as a result of the mounting process itself.

Therefore, this quality improvement, i.e., stamping the leadframe from the top side (shown in **Figure 24**), means the burrs are appearing on the bottom side of the package, where a failure – in combination with the isolation fail – cannot happen again. This further reduces possible failures in handling the QDPAK package.

4 Thermal handling

In the last few years there has been a move from THDs to SMDs due to the need for increased power density.

This trend is not only coming from the application side, but also from the need to reduce costs and to fully automate mass production.

The integration density that has been achieved so far, as well as newly developed functions, results in very large amounts of lost heat.

This situation has become ever more critical as smaller packages will be used in future, which represents a problem in terms of heat dissipation (from package to surroundings, or external cooling area) and requires great innovation and creativity to achieve heat reduction.

There is now the difficulty that with high packing densities on the PCBs, the large copper areas required are not suitable for heat reduction and the SMD component advantage could disappear.

Therefore, the DDPAK as well as the QDPAK, with its top-side cooling opportunity meaning the PCB is not touched anymore, led to the possibility of getting rid of heat (see **Figure 25**).

4.1 Thermal decoupling (package and board level)

The system can be driven to higher power levels compared to other SMD packages (e.g., TOLL) while not violating FR4 thermal limits, for example, due to the fact that the package body is decoupled from the PCB. On the right of **Figure 25** a thermal picture was taken to show the homogeneous heat spreading through the package, driving the package to its limits (not application relevant; the temperature of the body was set at 150°C).

The graph should represent the thermal decoupling from the PCB, avoiding hotspots, delamination or lifetime reduction resulting from extra heat injected into the PCB. As SMPS design is mostly cost-driven, extra benefit can be gained with the top-side cooling approach, pushing the package to its limit and increasing the output power of the SMPS. A laboratory study is also described in the **DDPAK application note**.

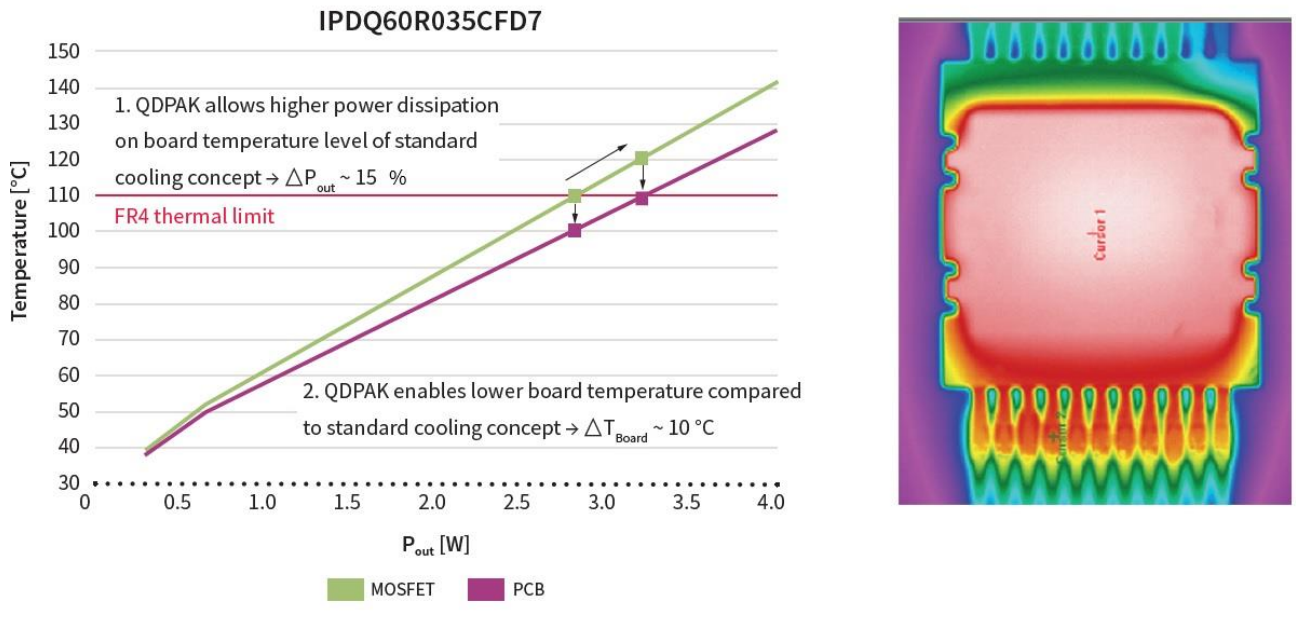


Figure 25 Package vs. board temperature

If the use of heatsinks is now considered for heat reduction of the SMD components, then the type of fixing, tolerances on the package and board level must be clarified.

Further parameters such as thermal resistance, dimensions (volume) and weight of the heatsink must be considered to apply a suitable cooling concept to the entire system. The customers themselves must find the optimal solution for their needs. The possibilities to solder a heatsink on top or even connect a heatsink via TIM to an external cooling system are nearly infinite. One important factor for reliability will be discussed in the next subchapter: the TCOB.

4.2 TCOB for QDPAK

The international standard IPC-9701 defines the thermal cycling test at the PCB level. The TCOB test is designed to detect failure modes, which are due to thermo-mechanical mismatch between devices (e.g., MOSFETs) and the PCB. These are mainly as a result of solder joint fatigue, but also include potential internal package defects from the stress related to the coefficient of thermal expansion (CTE) mismatch to the PCB (e.g., delamination, cracks or anything else).

A standard failure criterion during in-situ monitoring is a resistance increase of the daisy chain (contact resistance monitoring between two contacts) of more than 20 percent (according to IPC-9701). In the case of very small daisy-chain resistances, a higher resistance threshold is used and documented within the test report.

The specification for the TCOB test is shown in **Figure 26**. The tests were performed for four-layer PCB and FR4 materials. The PCB pad design shown in **Figure 9** was used for TCOB testing according to IPC-9701 standards at Infineon. Even after 2000 cycles, no electrical fails were detected with online monitoring, and there were also no objections to the solder joints after an optical inspection. Furthermore, the test showed no indication of solder joint degradation in cross-section.

Topic	Description		Comment
	Value	Unit	
Test Vehicle			
PG-HDSOP-22	16 x 21	mm²	
Chip	12	mm²	Infineon reference chip
Stress Boards			
Board material	high T_g FR4	-	
Board thickness/ layer	1.6 mm/ 4-layer	-	
Finishing	Chem. Sn	-	
Solder material	SAC305	-	
Stencil thickness	120	µm	
Stress Condition			
Temperature range	-40° C ... 125° C	° C	1 cycle/ hour according to IPC 9701
Monitoring	Electrical readout & Cross sectioning	-	Online readout

Figure 26 TCOB test setup specification for the QDPAK (PG-HDSOP-22) (in-house)

4.3 Compression reliability of the QDPAK

As already performed with the DDPAK package, a test is then performed with QPDAK to check the mechanical capability of the top-side heatsink mounting (single-device study).

The importance of the test will be clear, if the positive standoff is understood, as the 150 µm standoff acts like a spring force when heatsinks are soldered under pressure from the top. To avoid cracking of the QDPAK itself, the tests were standardized to ensure maximum safety for our customers in assembly lines.

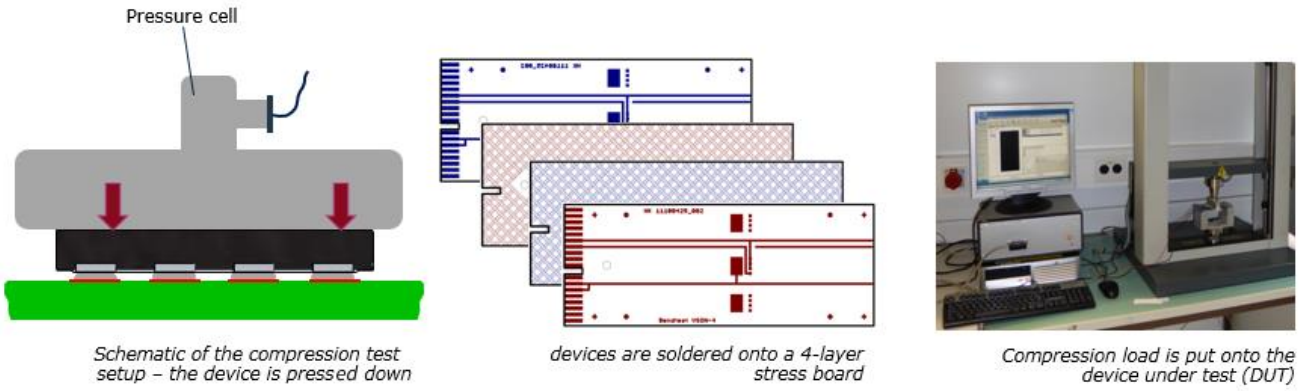


Figure 27 Compression test setup

Measurement procedure and setup (**Figure 27**):

- Devices are soldered onto a test PCB.
- Online readout equipment is connected to the test PCB.
- Pressure is applied on top of the devices until the device fails or maximum force (2500 N) is reached.

Compression Test Setup for PG-HDSOP-22 *devices*

Topic	Description		Comment
	Value	Unit	
Test Vehicle			
PG-HDSOP-22	16 x 21	mm²	
Chip	12	mm²	CoolMOS
Stress Boards			
Board material	high T_g FR4	-	
Board thickness/ layer	1.6 mm/ 4-layer	-	
Finishing	Chem. AuSn	-	
Solder material	SAC305	-	
Stencil thickness	120	µm	
Stress Condition			
Load Force	0 ... 2500	N	Ramp up to max load -> ramp down
Monitoring	Online electrical readout	-	Check for electrical fail during stress test

Figure 28 Specification of compression test setup for the QDPAK (in-house)

The outcome of this compression test is summarized in the following points:

- PG-HDSOP-22 devices are soldered onto a test board and put into a compression test.
- Load stress was increased up to machine limit (2500 N).
- All devices passed the compression test up to the maximum stress limit (machine limit).
- Destruction of the package is nearly impossible in case of heatsink soldering/mounting with force from top.
- For real application use, the customer must ensure that the force on the package or a heatsink is well balanced over the whole surface (avoid decentralized forces).

5 Application results

In the following sections several application measurements will be described for different platforms.

For a first feasibility study, a PFC test board with the option to mount adapter PCBs was chosen. This board provides the possibility of measuring and evaluating different package variants, and the freedom to easily access and change external components such as $R_{G,ext}$, or set different frequency levels.

Additionally, to prove the new hardware in a more specific and real-world application segment, Infineon decided to make a state-of-the-art form-factor power supply with increased power density to show the strength of the new package. This platform is available in two versions, one fully equipped with DDPAK packages and one a combination of DDPAK and QDPAK. More details and order codes can be found via our **top-side cooling web page**.

5.1 2.5 kW PFC stage

5.1.1 Introduction to the board

The application testing for the CFD7 devices in QDPAK shown in this document is performed by adding a daughter board to the 2.5 kW PFC evaluation board [1] – including the Infineon constant current mode (CCM) PFC controller (ICE3PCS01G), as shown in **Figure 29**.

The same board was also used for the former DDPAK evaluation – a multifunctional setup with a variety of options in terms of evaluation purposes. For further details, please refer to this **application note** and the **DDPAK application note** (chapter 5.1).

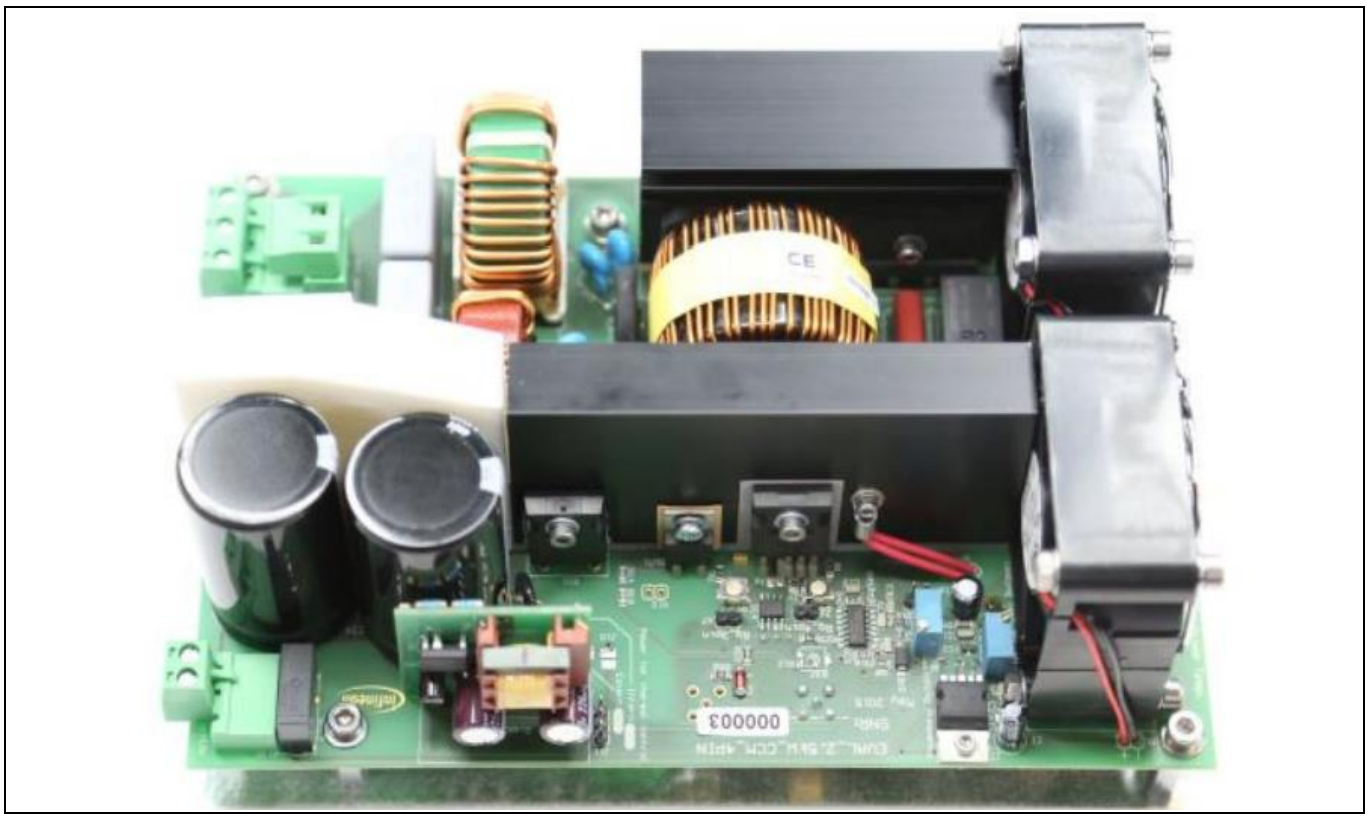


Figure 29 EVAL_2.5kW_CCM_4PIN evaluation board

5.1.2 Measurements and results

The original design of this evaluation board is fitted with a TO-247 MOSFET (see **Figure 29**). In order to use the QDPAK CFD7 and SiC diode devices in this evaluation board, some modifications with daughter boards are required.

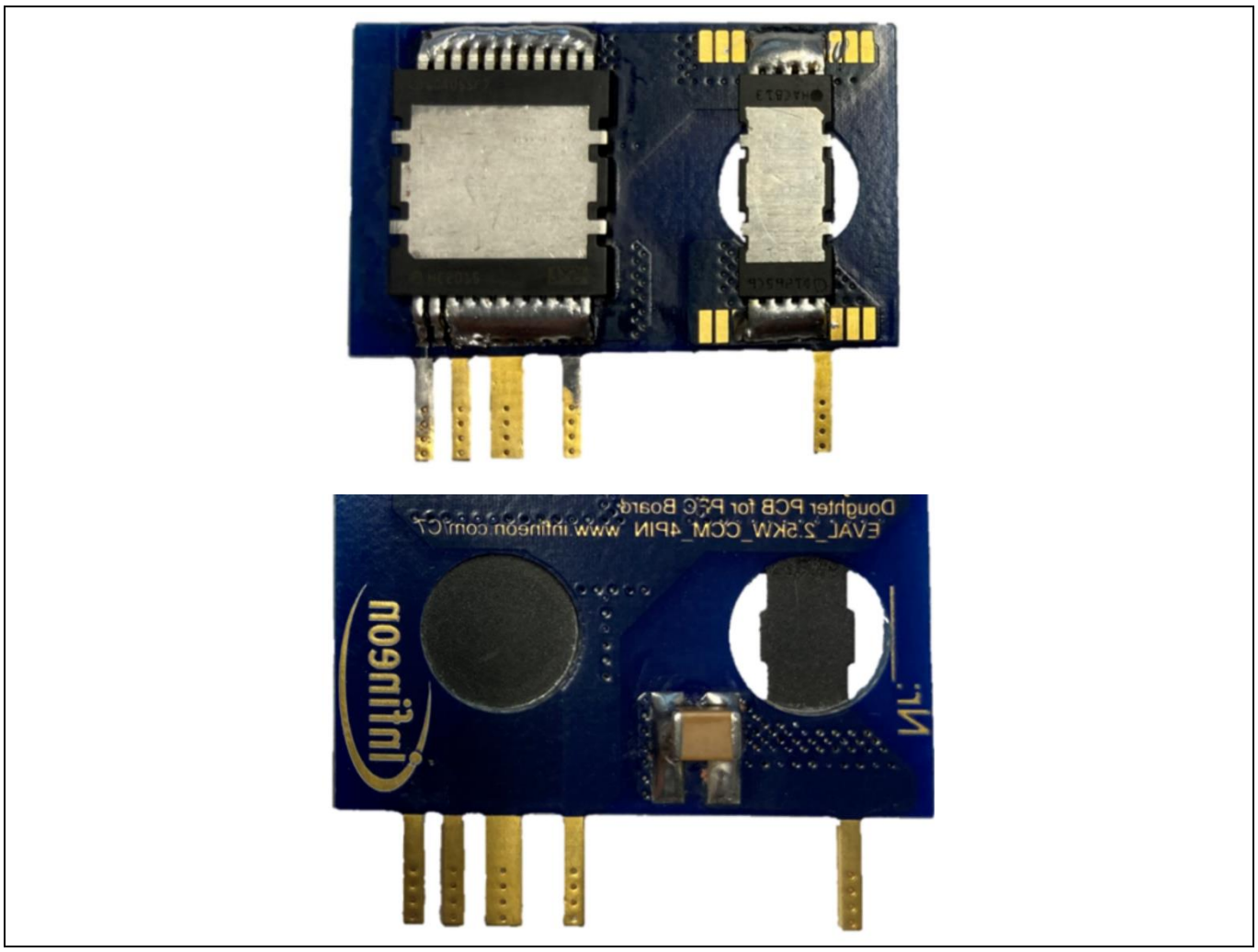


Figure 30 Daughter boards/cards for the QDPAK MOSFET and DDPAK diode (top and back side)

On the QDPAK daughter card, the diode, the MOSFET and a capacitor are assembled. Thermal conductive paste has to be added to the packages through the holes (openings in the PCB back for connection of the fasteners). The QDPAK and DPPAK are fixed through these holes with two plastic screws. For thermal sensing two thermocouples can be connected to the back of the QDPAK and DDPAK package and read out via a data logger unit.

A bolt makes it possible to adjust the pressure that fixes the parts to the PFC board's heatsink. To ensure the right isolation between the heatsink and package top side, insulating foil has to be added. Depending on the characteristics of the foil, its behavior and the overall performance can vary (efficiency and component temperature).

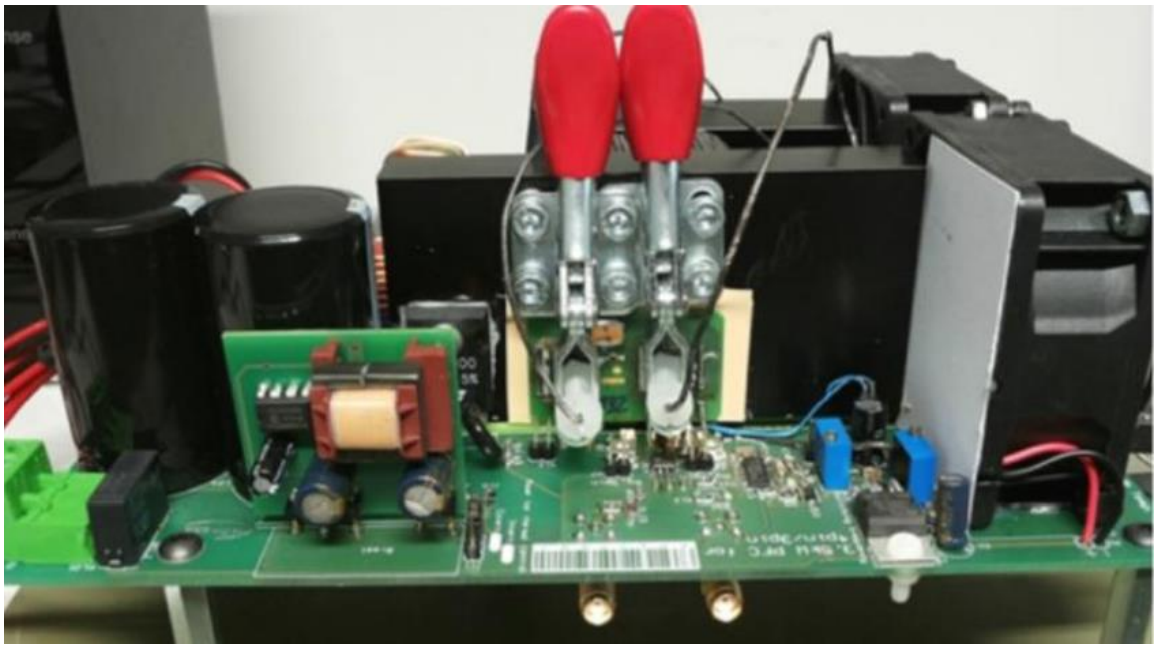


Figure 31 Modified demo board with QDPAK/DDPAK fixture of adapter platine

For efficiency and thermal measurement a $R_{DS(on)}$ range from 35 to 55 mΩ (from the forthcoming CFD7 QDPAK portfolio) was chosen. As a comparison to the original TO-247 device, mounted with K10 isolation foil, a Bando Heatex® TS103 with 0.5 mm was selected (see **Figure 32**).

TIM	Rth per cm² [K·cm²·W⁻¹]	Relative dielectric constant	Dielectric breakdown voltage [V_{rms}]	Area (TO-247) [cm²]	Rth (TO-247) [K·W⁻¹]	Capacitance (heat slug to heatsink) [pF]
K10 0.152 mm	2.12	3.7	6000	3.33	0.64	72
Heatex TS103 0.5 mm	0.6	3.5	10000	3.33	0.18	21

Figure 32 TIM used for evaluation

As can be seen in the specification of the foils used, the Bando foil shows a dramatically better R_{th} with even higher breakdown voltage capability. For the height differences and a possible board bending, a 0.5 mm thickness of the foil is mandatory.

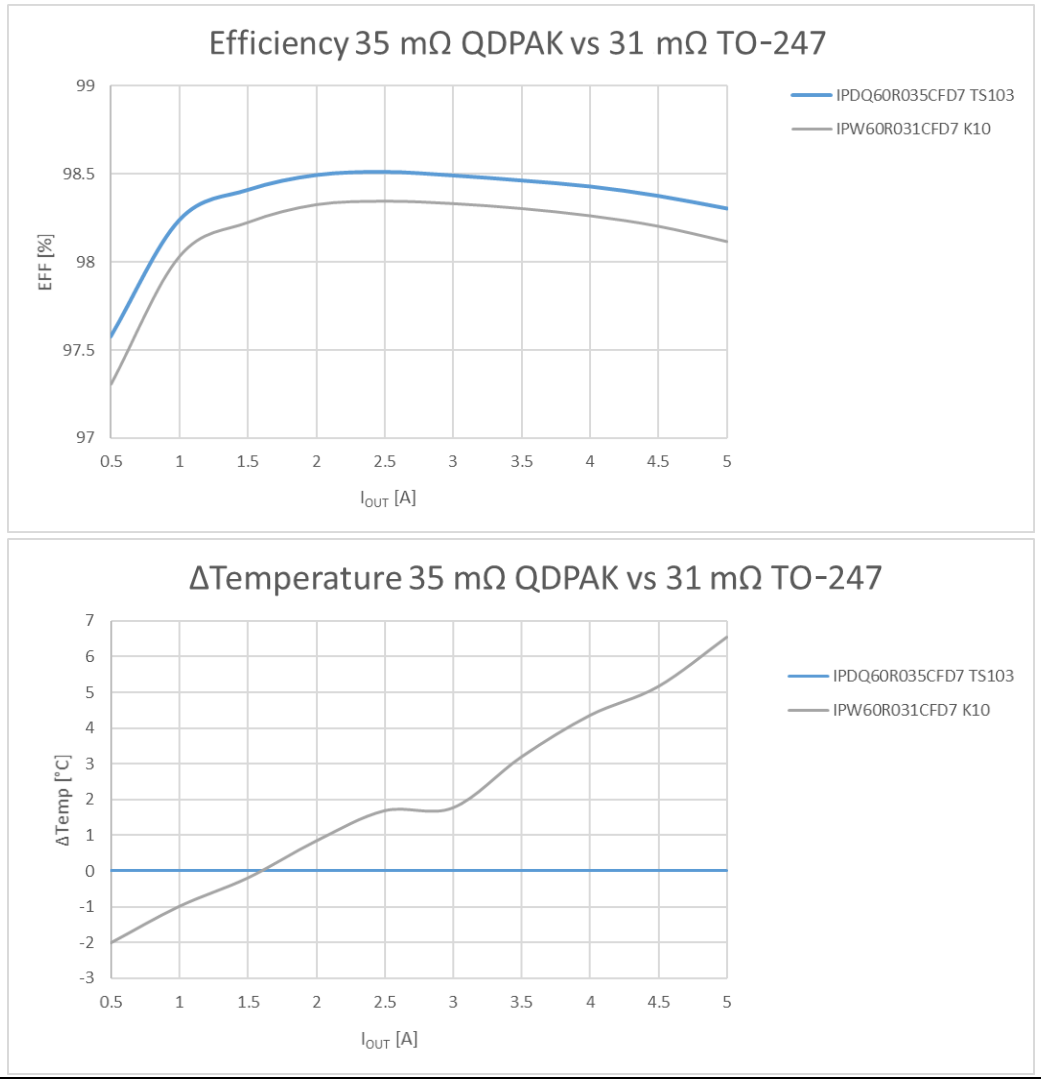


Figure 33 Efficiency/thermal measurement of the QDPAK MOSFET (IPQD60R035CFD7, 230 V_{AC}, 65 kHz, $R_{G,ext}$ = 5 Ω)

Due to the fact that Infineon does not have the same $R_{DS(on)}$ in the QDPAK and TO-247 (3-pin) available, two comparable $R_{DS(on)}$ values in TO-247 are shown (35 mΩ and 31 mΩ) in **Figure 33**.

The top chart shows that the difference in efficiency is in the range of 0.15 to 0.2 percent better over the whole load range. The tolerance level of the measurement itself is below 0.1 percent.

On the lower chart (where the temperature is compared) the strength of the 4-pin approach is more evident at the full-load point where the current is at its maximum. The clear signal quality on the gate helps to reduce overall losses inside the MOSFET, giving best efficiency at the full-load point. Furthermore, the selection of a high-performance isolation foil shows up any improvements in the temperature behavior. The combination of foil, top-side cooling and the 4-pin approach is transformed to a 5 to 6°C lower MOSFET temperature of the QDPAK package.

To complete this short cross-check of the QDPAK performance, a further evaluation with 55 mΩ devices was performed.

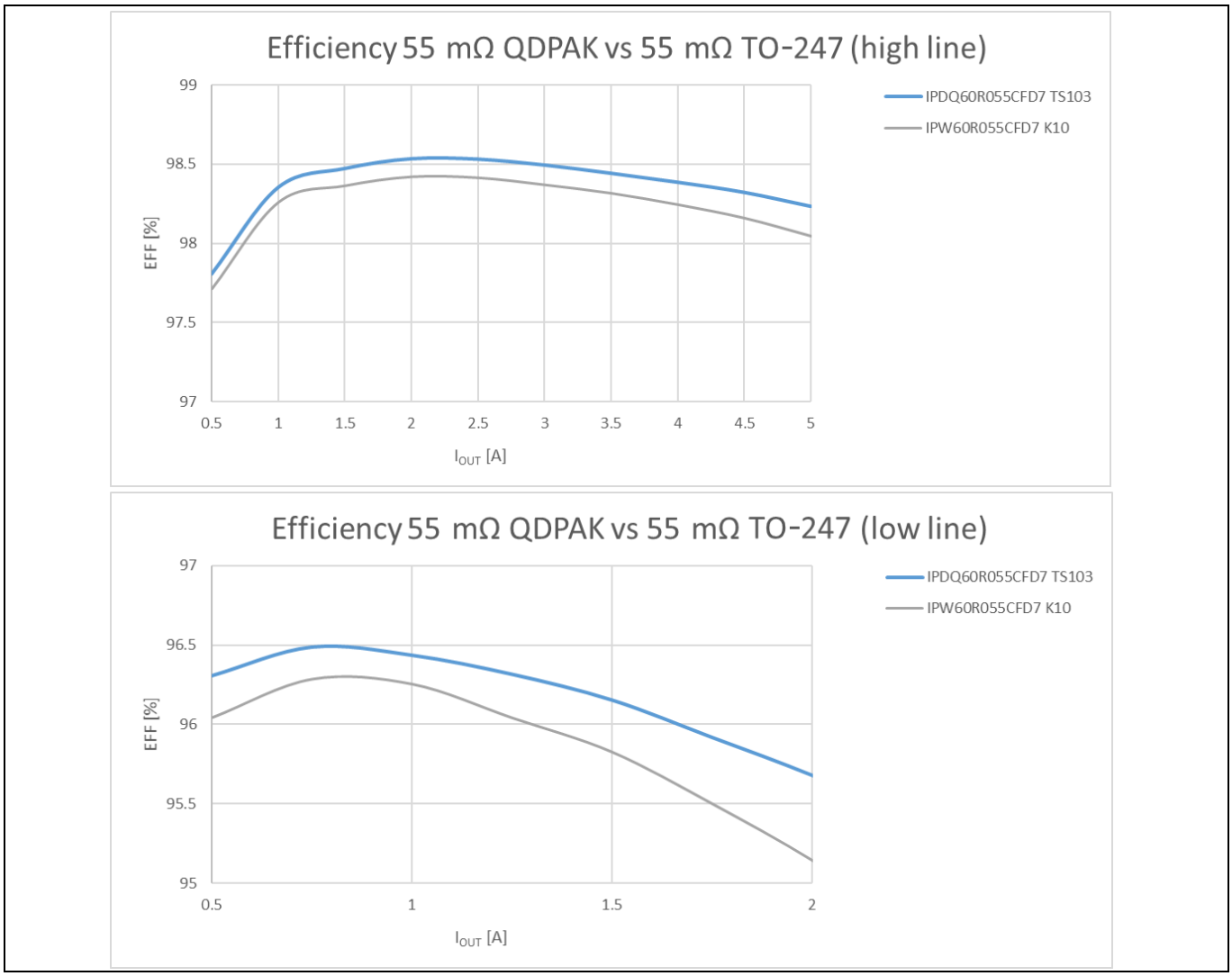


Figure 34 Efficiency of the QDPAK MOSFET (IPDQ60R055CFD7, 90/230 V_{AC}, 65 kHz, $R_{G,ext}$ = 5 Ω)

In **Figure 34** a high line (AC_{in} = 230 V_{AC}/50 Hz) and a low line (AC_{in} = 90 V_{AC}/60 Hz) is shown. For the high line measurement, a slightly better performance can be realized (~0.2 percent).

Furthermore, a low line measurement with an input voltage of 90 V_{ACin} was taken. Due to the fact that the MOSFET sees the highest possible current under these conditions, the system was driven up to 800 W with a 55 mΩ switching device and a 12 A diode to keep the losses as small as possible.

At the full-load point, a 0.4 percent better efficiency can still be realized. The main driver of this good result was the Bando Heatex® isolation foil with its perfect thermal characteristics, in addition to the 4-pin capability of the QDPAK, giving a lower loss driving compared to the standard TO-247.

This measurement illustrates impressively how important it is to choose different thermal interfaces during your application evaluation, and to test out new SMD packages with totally different thermal connections (cooling via TSC packages, e.g., DDPAK and QDPAK).

In conclusion, the QDPAK package was not intended to be a direct one-to-one replacement of a TO-247 package, as the main benefit comes with a real optimized SMD solution and adapted cooling. Nevertheless, the strong performance of TSC packages have already been shown in the **DDPAK application note** and emphasized by the results in this chapter.

Thermal handling, choosing the correct foil and thinking about the connection of components and the overall cooling environment are topics to be covered in an SMPS development.

5.2 3.3 kW LLC stage

In the new QDPAK TSC package, we also implemented fast diode devices such as the 600 V and 650 V CFD7, as well as the 650 V CFD7A. This package brings a clear advantage in resonant topologies for DC-DC converters for industrial applications such as solar, servers/telecoms, EV charging and ATV applications.

Having a thin package with a high-power dissipation capability raises the power density of designs and the possibilities of advances for passive cooling, for example in 5G applications.

5.2.1 Introduction to the board

To work out the benefits of our latest fast diode technologies with best-in-class $R_{DS(on)}$, our team designed the EVAL_3K3W_LLC_HB_CFD7 evaluation board. This board offers the possibility to simulate the mounting and use of THT and SMD packages (e.g., TO-247, QDPAK TSC) in a high-power DC-DC stage. The board comes equipped as standard with IPW60R018CFD7. For detailed information on the EVAL_3K3W_LLC_HB_CFD7, please visit our **website**.

The EVAL_3K3W_LLC_HB_CFD7 design consists of an LLC HB with SR in full-bridge configuration, with split capacitor and clamping diodes on the primary side (**Figure 35**).

The control is implemented with an XMC4200 Infineon microcontroller, which includes voltage regulation functionality, burst mode operation, output overcurrent protection (OCP), overvoltage protection (OVP), undervoltage protection (UVP), undervoltage lockout (UVLO), soft-start, SR control, adaptive dead-times (bridge and SRs) and serial communication interface. Further details on the digital control implementation and additional functionalities of the LLC control with the XMC™ 4000 family can be found in [1].

The converter's nominal output is at telecom level (51.5 V) with wide range capability, also tailored for 48 V battery charger systems working within the 59.5 to 43.5 V range. The converter is operated at a nominal input voltage of 400 V, whereas it can regulate down to 360 V at full load (at nominal 51.5 V output voltage) providing room for hold-up time whenever the design is part of a full AC-DC converter.

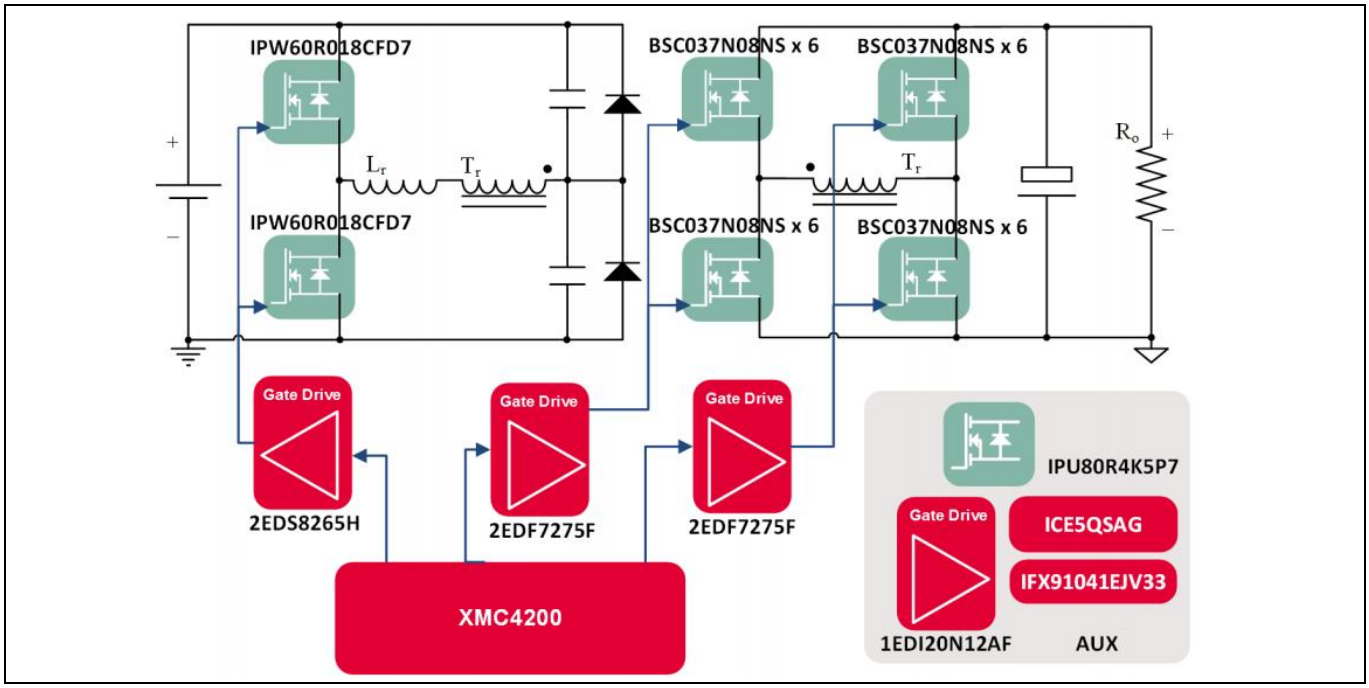


Figure 35 3300 W LLC HB (EVAL_3K3W_LLC_HB_CFD7) – simplified diagram

Figure 36 shows the placement of the different components on the 3300 W LLC half-bridge DC-DC converter. The outer dimensions of the board, designed without enclosure, are 205 mm x 100 mm x 40 mm, which results in a power density in the range of 4 W/cm^3 (66 W/in^3).

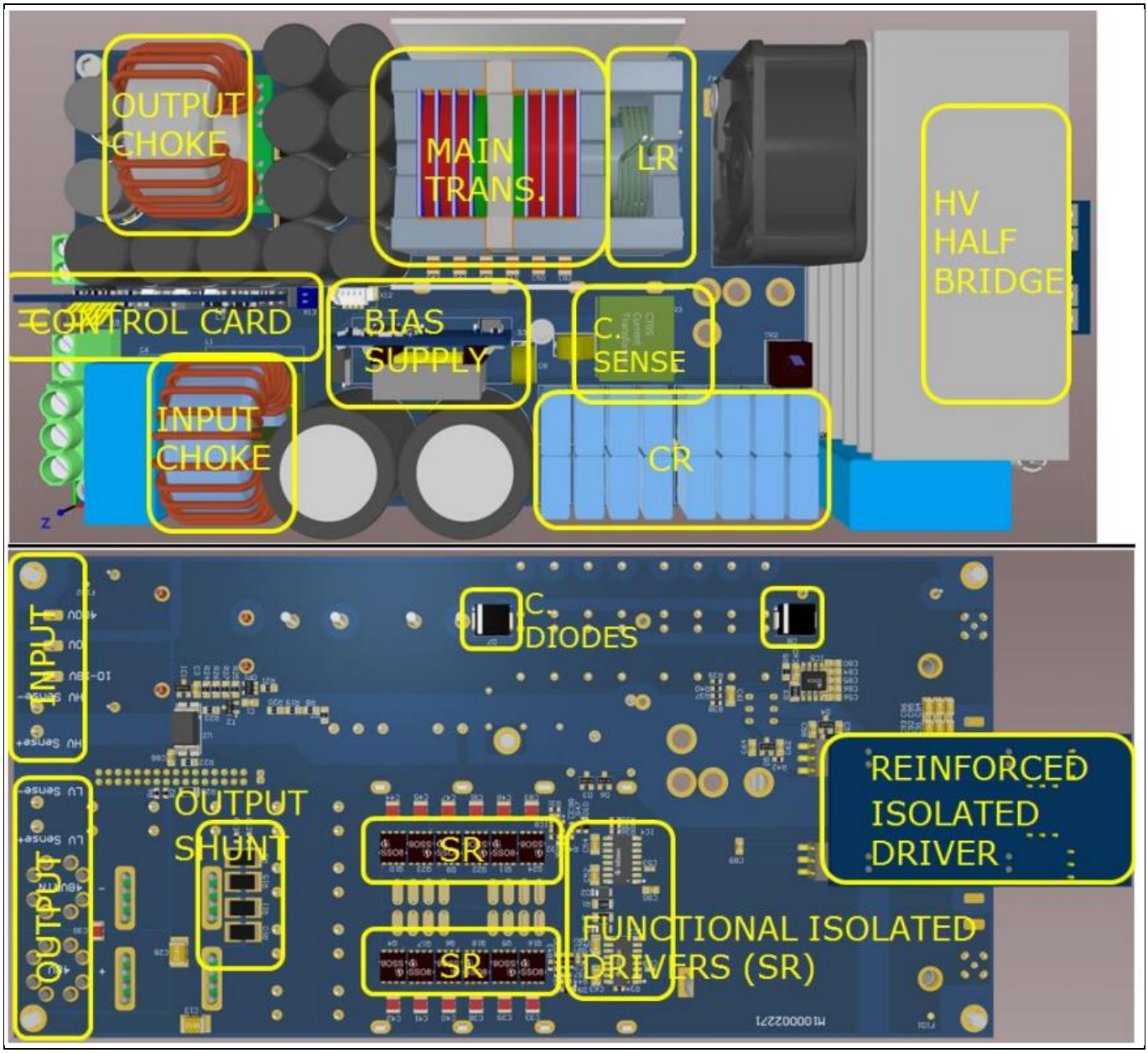


Figure 36 **Placement of different sections in the 3300 W LLC half-bridge: current sense (CS), resonant inductor (LR), synchronous rectifiers (SR), clamping diodes (C. DIODES), resonant capacitor (CR)**

5.2.2 Validation setup

For validation of the operation of the 3300 W LLC half-bridge, the suggested setup includes:

- HV supply capable of 400 V and at least 3500 W (when testing up to full load)
- LV electronic load (0 to 60 V), in CCM, capable of at least 3300 W (when testing up to full load)

Nominal input voltage of the converter is 400 V. The converter starts to operate above 375 V, turning back off under 350 V (hysteresis window), as summarized in **Figure 37**.

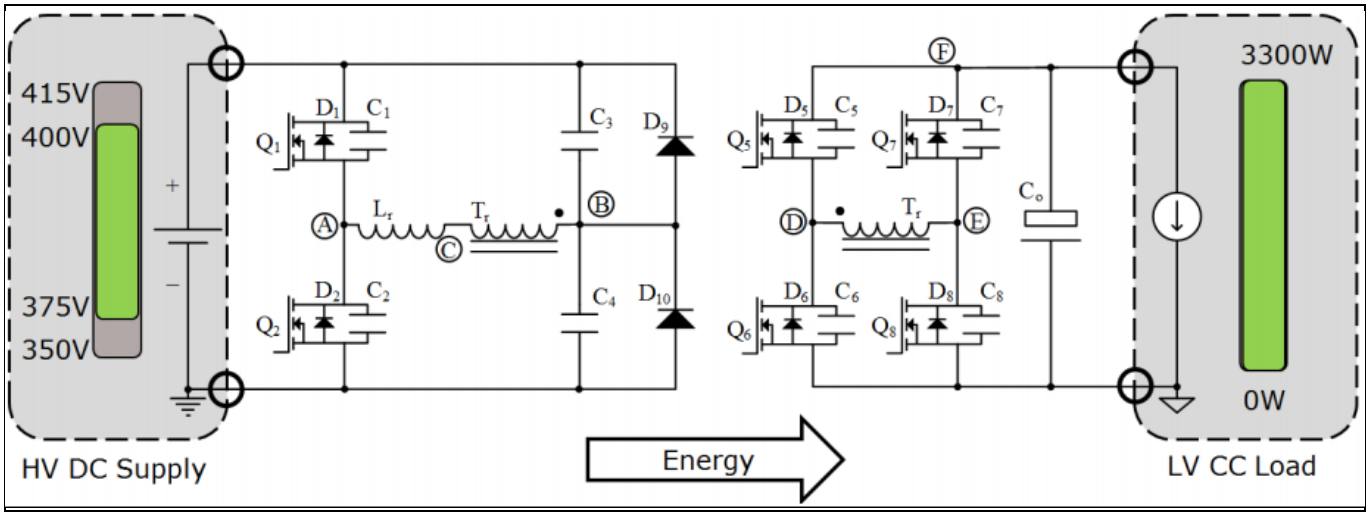


Figure 37 Recommended validation setup

5.2.3 Measurements and results

For the evaluation of the QDPAK in the 3.3 kW LLC stage, we used devices in the 50 mΩ range, having a mid range $R_{DS(on)}$ of the current QDPAK TSC 600 V CFD7 portfolio, with balanced conduction and switching losses. To compensate for warping of the board and the possible deviation in package height due to the soldering process, we used the TIM shown in **Figure 38**. The Bergquist™ Sil-Pad® 1500ST cannot be used for QDPAK in the application due to a 0.15 mm standoff of the package, which leads to a thermal runaway, as the deviation in height on the board can not be balanced between the two MOSFETs. An example of a daughter card can be seen in **Figure 45**.

TIM	Rth per cm² [K·cm²·W⁻¹]	Relative dielectric constant	Dielectric breakdown voltage [V_{rms}]	Area (TO-247) [cm²]	Rth (TO-247) [K·W⁻¹]	Capacitance (heat slug to heatsink) [pF]
K10 0.152 mm	2.12	3.7	6000	3.33	0.64	72
Bergquist 1500ST 0.203 mm	1.29	6.1	3000	3.33	0.39	89
Heatex TS103 1 mm	1	3.5	20000	3.33	0.30	10

Figure 38 TIM used for evaluation

The adapter platine for both MOSFETs (low-side and high-side) was mounted with an M3 screw and a torque set of around 0.3 Nm applied, which resulted in reliable and stable measurement results. The mounting of the daughter cards is similar to the triangular current board and can be seen in **Figure 46**.

First testing was done with the TO-247-3 package with the Bergquist™ Sil-Pad® 1500ST (0.203 mm) vs. the QDPAK with the Heatex® TS103 (1 mm) to overcome possible height differences due to manual soldering (two MOSFETs on adapter card including all tolerances).

Hint: For final machine assembly, the customer must take possible TIM deratings, compression ratings and package and production tolerances into account! The ratings differ between manufacturers.

The following boundary conditions are set for both devices (**Figure 39**):

- Limit $V_{GS,max}$ = +/-30 V (datasheet maximum)
- Limit $V_{DS,max}$ = 480 V (20 percent derating of breakdown voltage)

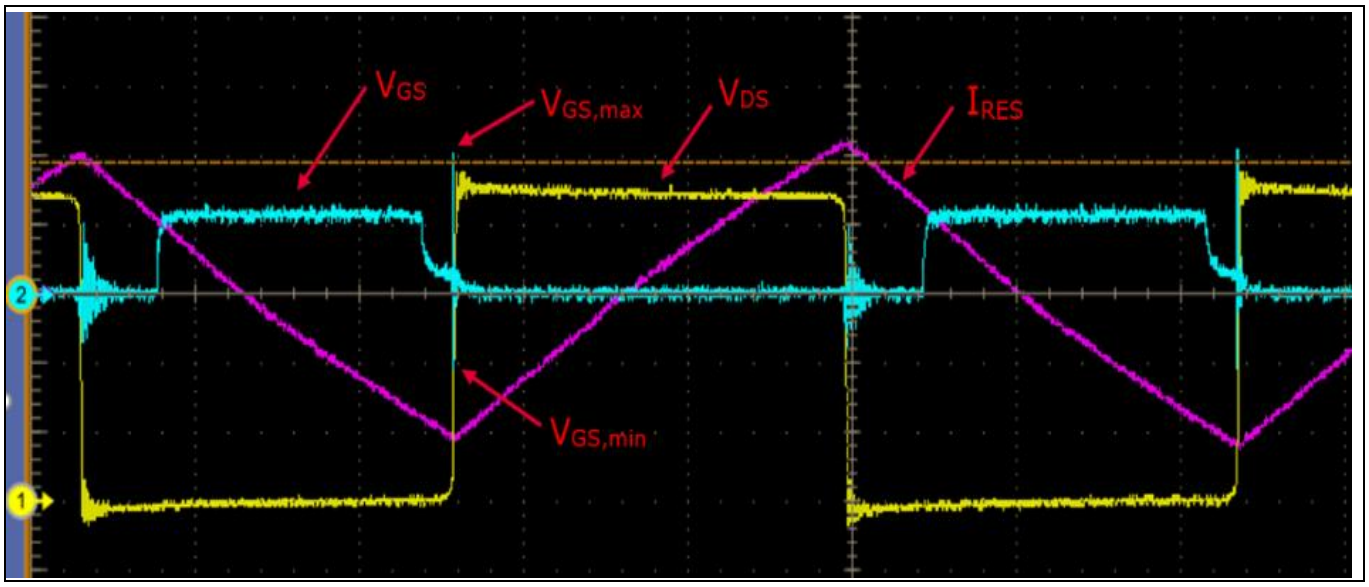


Figure 39 Switching waveforms in the 3.3 kW LLC

From an efficiency point of view there was no significant difference seen between TO-247 and QDPAK TSC, but with full load there is a trend for higher efficiency for the QDPAK TSC (**Figure 40**).

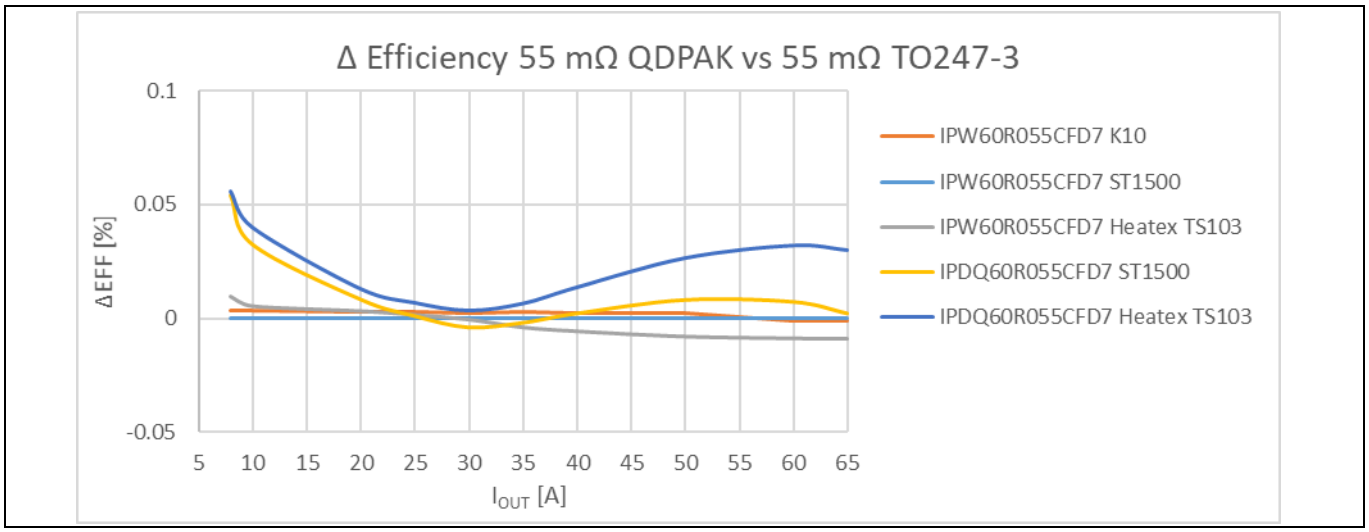


Figure 40 Delta efficiency over output current (55 mΩ range)

This slight trend can also be seen in a lower temperature of roughly 2°C, which can be seen in **Figure 41**.

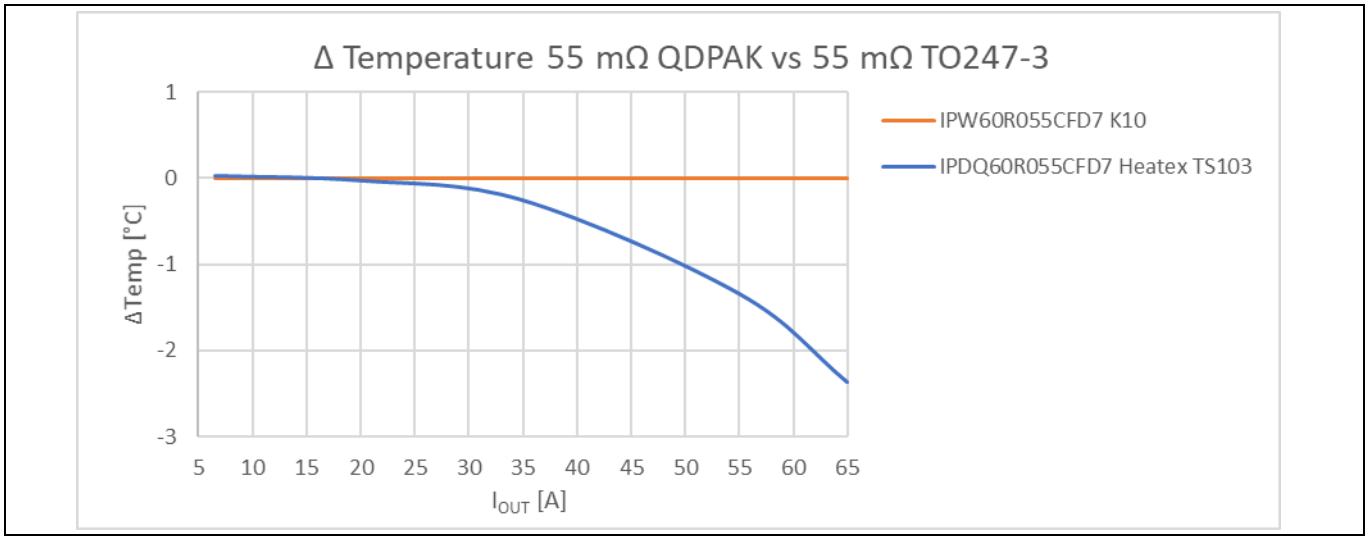


Figure 41 Lower temperature for QDPAK vs. TO-247

It is expected that a thicker foil will show a worse thermal performance, but in the comparison done, the good thermal characteristics from the Heatex® TIM and the 4-pin capability of the QDPAK showed an adequate result. For further information on the benefits of 4-pin devices see **chapter 2.3**.

Overall, the QDPAK devices have the same efficiency as the TO-247 devices. Due to the lower parasitic and the Kelvin-source design of the QDPAK TSC, the MOSFET shows lower oscillations on the gate voltage, leading to a faster and cleaner switching behavior. Although the gate resistance has to be increased to stay within the 80 percent derating of V_{BRSS} (due to the 4-pin configuration), the light load efficiency also showed the tendency to be higher.

The 80 percent derating is recommended to Infineon Technologies customers, but it is not essential, so an optimization to this factor also depends on the application boundaries and cosmic ray needs (e.g., ATV customers). For further information on cosmic rays see the "**Cosmic radiation effects on high-voltage semiconductors in automotive onboard chargers**" application note.

It can be seen that the 1 mm Heatex® TS103 TIM has the best performance for QDPAK. For two QDPAKs on adapter cards, a TIM with at least 0.5 mm thickness is required to overcome height differences of the positive standoff and the warping of the top side surface of the package.

5.3 Triangular current board setup

5.3.1 Introduction to the board

To emulate the stress of power MOSFETs in a DC-DC stage (especially conditions in an EV charging environment) and to prove the capabilities, advantages and disadvantages, this internal setup was created.

The block scheme of an EV charging platform can be simplified as follows.

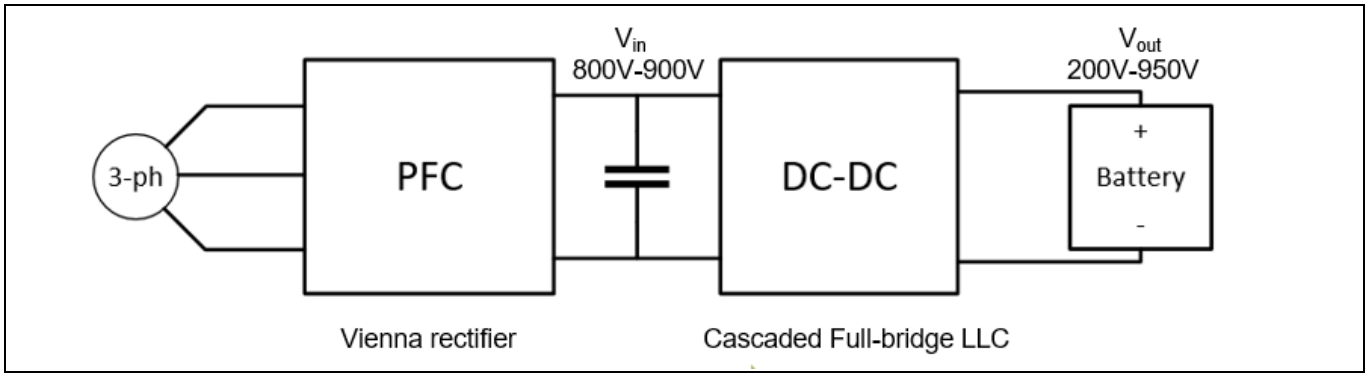


Figure 42 A typical block scheme of an EV charging platform using 600 V/650 V devices

A PFC block, usually implemented as a Vienna rectifier, is connected between the three-phase input and the DC-DC block, which is often implemented as a cascaded full-bridge LLC to allow for the use of 600 V or 650 V devices.

The voltage across the PFC output capacitor is usually regulated between 800 V and 900 V, while the output voltage of the LLC equals the battery voltage. As a result, the required output voltage (battery voltage) range is wide (200 to 950 V).

The power rating of such a system could be up to 40 kW.

A cascaded LLC topology is needed in order to handle with 600 V/650 V switches the ~800 V output of the PFC, which is typically implemented with a Vienna rectifier. The minimum HV switch rating is 1200 V. SiC diodes are a common solution for the secondary-side rectification.

High switching frequencies lead to an almost triangular tank current, which means a high turn-off current for the switches. Since our objective is to test our devices in such conditions, we developed the triangular current board. This enables us to reproduce the application conditions without the need to build a platform in the tens of kW range. A picture of the board can be seen in **Figure 43**.

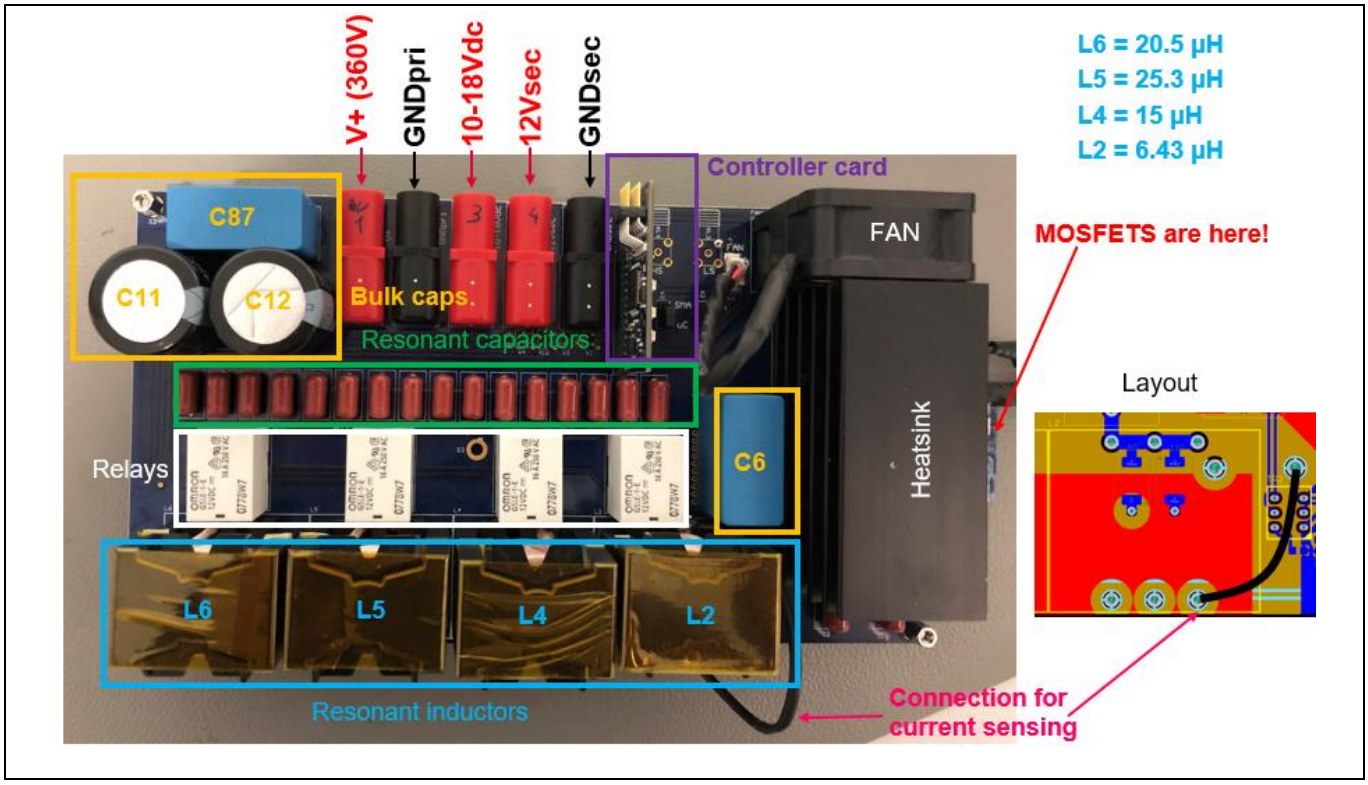


Figure 43 Triangular current setup (top view)

As the setup is an internal one, enabling the test board to operate under different conditions (representing part of a system only), it is not available on the open market.

For testing a broad range of packages, a heatsink design was chosen which offers this flexibility (**Figure 44**). Furthermore, 3 vs. 4-pin functionality was implemented to compare the differences within different technologies and packages. All in all, this is a powerful tool to evaluate MOSFETs for EV charging setups and special conditions, such as the MOSFETs turning off at the highest current levels.

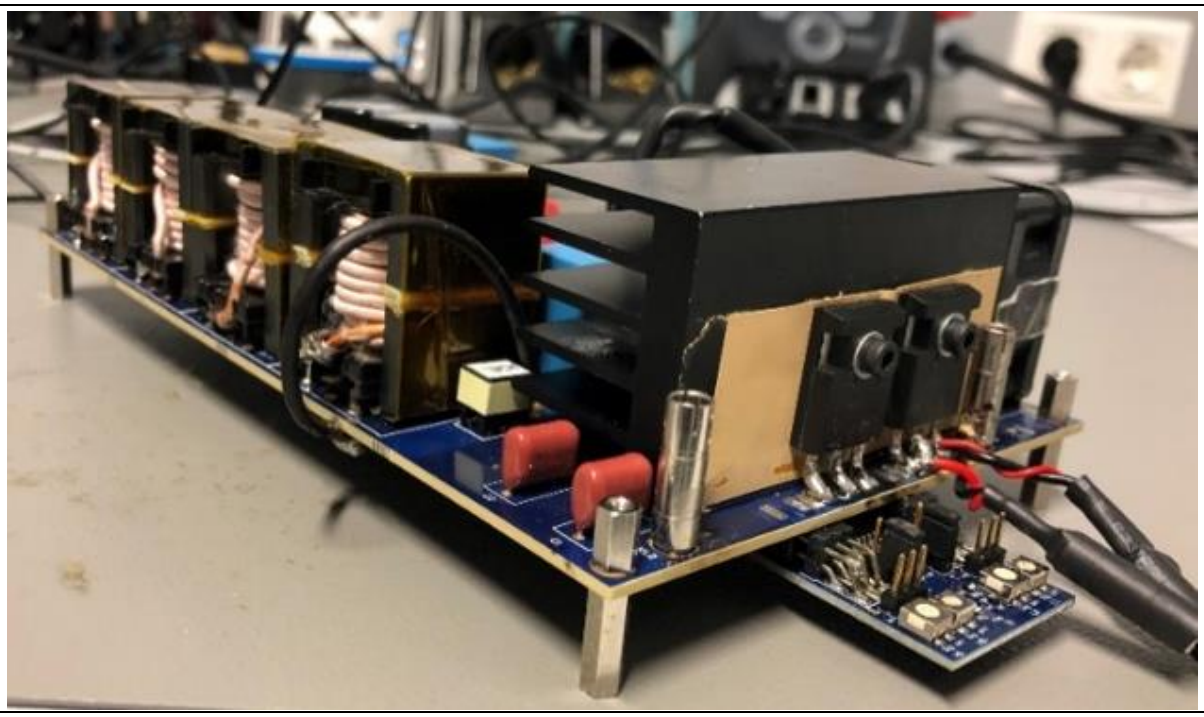


Figure 44 Heatsink design of triangular current board (equipped with standard TO-247-3)

5.3.2 Measurements

As already described in the introduction, the board offers a range of measurable packages. The main focus was to investigate the differences between TO-247 and QDPAK, showing the advantages of moving toward SMD solutions in customers' SMPS designs.

Figure 44 showed the mounting of a standard TO-247, and **Figure 45** shows the mounting of a QDPAK, placed on an adapter card.

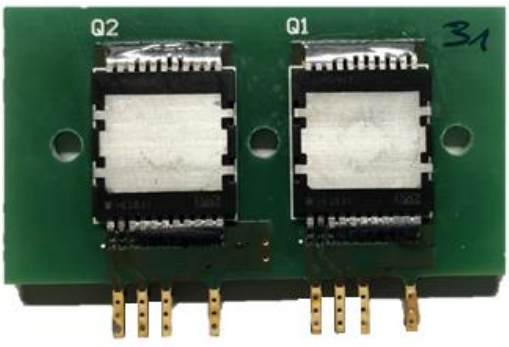


Figure 45 QDPAK adapter card (half-bridge configuration)

Furthermore, it can be seen that for mounting purposes three holes have been made in the adapter board to make an appropriate fixing to the heatsink possible and put balanced force on the PCB.

The diameter of the holes can be chosen by the customer, but should be larger than 3 mm to ensure a proper mounting. For a real SMPS solution, this option of mounting must be optimized, but in our case the test platform itself (heatsink) sets the boundary conditions. For the setup assembly, see **Figure 46**.

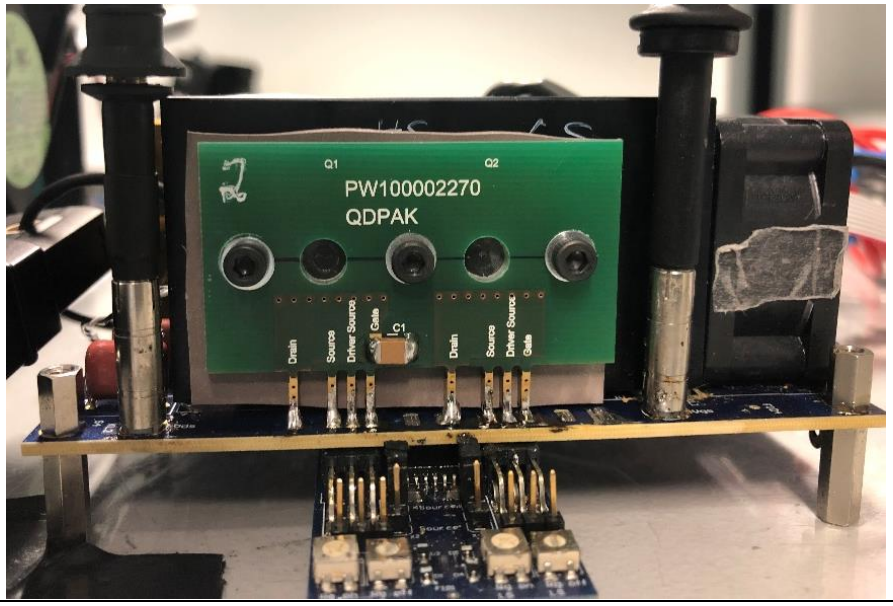


Figure 46 Triangular current board assembly with QDPAK and thermal foil

Mounting an adapter platine for both MOSFETs (low-side and high-side) with an M3 screw and a torque of around 0.3 Nm applied resulted in reproducible and adequate thermal performance.

After each and every test, the isolation foil, no matter what brand, was exchanged, to ensure that all differences and tolerances arising from compression and decompression of the foil itself (leading to a possible decreasing performance) were elimanted.

For all the tests, the following TIMs have been chosen, and by knowing the pressure (~200 PSI) applied to the TIM, referring to the datasheet, it is possible to calculate its thermal resistance:

TIM	Rth per cm² [K·cm²·W⁻¹]	Relative dielectric constant	Dielectric breakdown voltage [V_{rms}]	Area (TO-247) [cm²]	Rth (TO-247) [K·W⁻¹]	Capacitance (heat slug to heatsink) [pF]
K10 0.152 mm	2.12	3.7	6000	3.33	**0.64**	72
Bergquist 1500ST 0.203 mm	1.29	6.1	3000	3.33	**0.39**	89
Heatex TS102 1 mm	1	3.5	20000	3.33	**0.30**	10

Figure 47 Different thermal interfaces and their characteristics

The new TIM from Bando (Heatex® TS102, replaced by TS103 in 2021) outperforms both K10 and Bergquist™ Sil-Pad® 1500ST:

- Lower thermal resistance despite greater thickness
- Higher dielectric breakdown voltage

For former measurements the K10 foil (Bergquist™ Sil-Pad® K10) was used as a standard isolation material for TO-247 and TO-220 measurements, but because it is so thin (~0.15 mm), this foil should not be used for DDPAK and QDPAK packages, as it cannot compensate for the overall height difference of those packages.

Device	$R_{G,int}$ [Ω]	$R_{G,on}$ [Ω]	$R_{G,off}$ [Ω]	dt_{max} [ns]
IPW60R031CFD7	3.8	10	0	212.5
IPDQ60R035CFD7	3.8	10	0	162.5

Figure 48 Component list for triangular current board testing

The first testing was done with the TO-247-3 package with the Bergquist™ Sil-Pad® 1500ST (0.203 mm) vs. the QDPAK with the Bando Heatex® (1 mm) to overcome possible height differences due to manual soldering (two MOSFETs on adapter card, including all tolerances).

Hint: For final machine assembly, the customer must take possible TIM deratings, compression ratings and package and production tolerances into account! The ratings differ between manufacturers.

It is expected that a thicker foil will show a worse thermal performance, but in the comparison done, the good thermal characteristics of the Bando TIM and the 4-pin capability of the QDPAK showed an adequate result, which is illustrated in **Figure 49** and **Figure 50**.

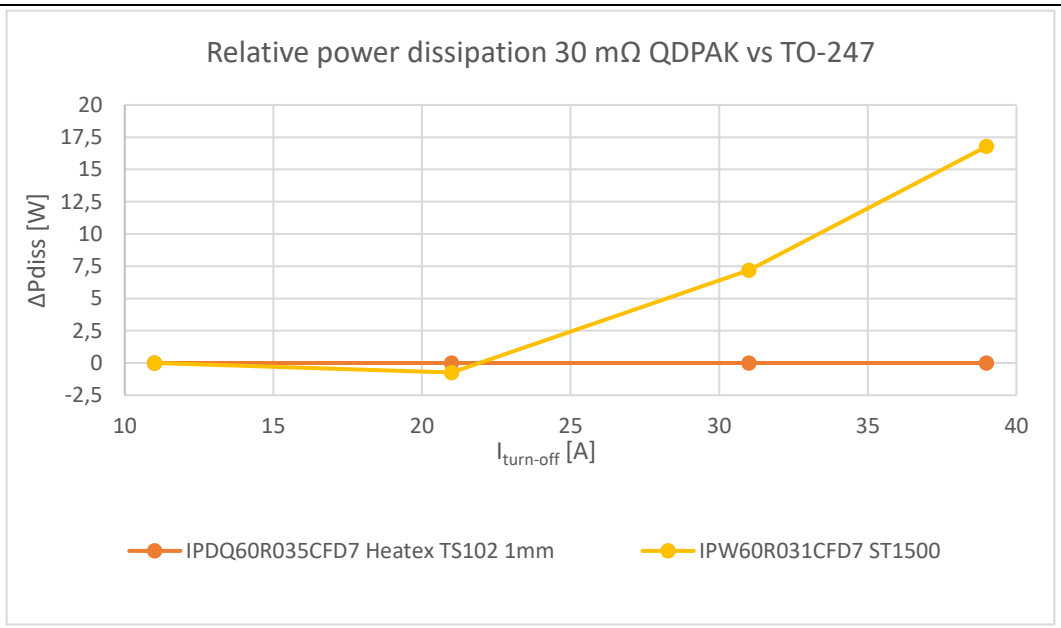


Figure 49 Relative power dissipation 30 mΩ range (TO-247 vs. QDPAK)

The QDPAK shows a much lower power dissipation (~6 W per device lower for 30 mΩ MOSFET) compared to the TO-247-3 pin.

This is possible thanks to the Kelvin source, which greatly reduces the additional losses caused by the return of the device. Such return on issue is well understood, and it occurs at high turn-off currents.

Furthermore, the Bando Heatex® isolation foil also helped to reduce the temperature of the MOSFET and ensure a well-balanced and homogeneous thermal connection between package, foil and heatsink.

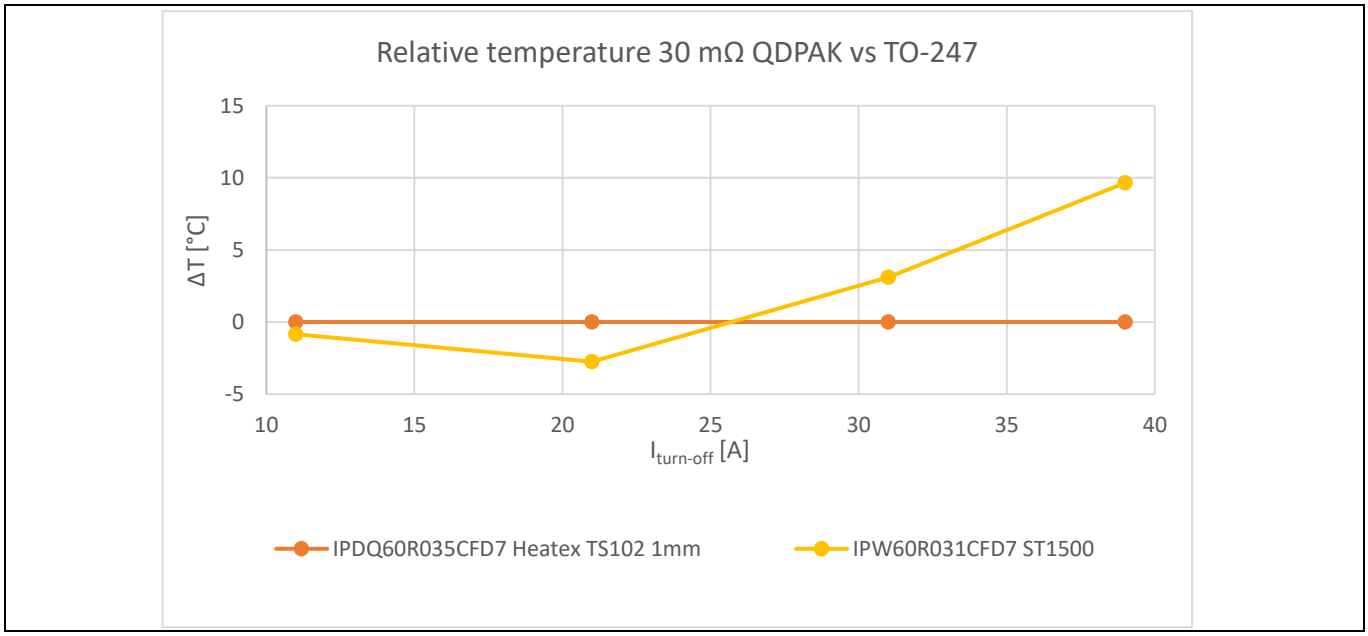


Figure 50 Relative temperature difference 30 mΩ range (TO-247 vs. QDPAK)

The thermal performance of QDPAK is reduced compared to TO-247 due to the smaller heat slug area (see **Figure 5**). As can be seen in the previous slides, the lower $R_{th,JA}$ of the TO-247 is able to offset up to ~6 W higher power dissipation (around the 30 A current/load point – see **Figure 49**) than the QDPAK. If the difference in power dissipation is higher than 6 W per device, the QDPAK will have a lower temperature. At the full-load point, comparing the Bergquist™ Sil-Pad® 1500ST to the Bando Heatex® isolation material, taking the value added by the fourth pin of the QDPAK into account, at around 40 A application current, the QDPAK stays in the range of 10°C cooler compared to the TO-247. In all the evaluations, datasheet specifications in terms of V_{GS} and V_{DS} ringing levels have been considered.

As a result of this evaluation the customer, moving from THT MOSFET mounting and screwing devices to a large heatsink, has the opportunity to reduce space, move to automatized SMD component (MOSFET) assembly, reduce costs, increase reliability and enjoy superior performance from the device and the overall system.

5.4 Application summary

With the top-side cooling approach of the QDPAK and DPAK, whether on the CoolMOS™ or CoolSiC™ side, many benefits have been demonstrated

Summarized, the following aspects are most crucial:

- A new level of power density can be achieved with the top-side cooling approach.
- Selection of the thermal interface has a significant influence on thermal performance.
- The thermal interface must be chosen carefully (R_{th} chain, isolation strength, bending of the board…).
- The top side of the DDPAK and QDPAK allows heatsinks to be soldered on top of the package.
- Positive standoff can increase overall TCOB performance (the pins of the package act like springs and reduce stress between the component and, PCB including thermal decoupling).
- Highest quality and reliability are assured by several internal investigations.

6 Portfolio

For a complete summary of the actual and existing TSC packages and products, refer to the overview in **Figure 51**.

Especially for the QDPAK in CFD7 technology a dedicated product wave including $R_{DS(on)}$ from 35 mΩ up to 75 mΩ will be launched in Q4 of 2021, and a follow-up wave with even smaller target $R_{DS(on)}$ (25 mΩ down to 15 mΩ) will be released in 2022.

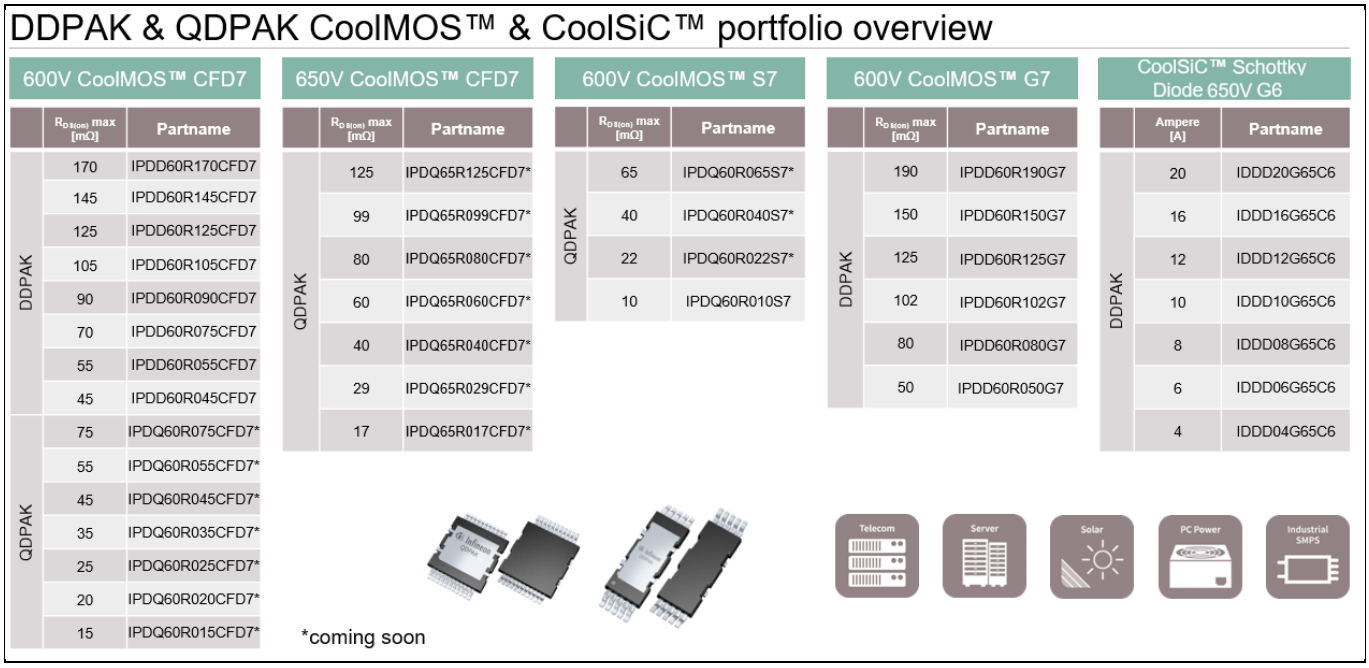


Figure 51 Complete TSC product portfolio (status: Q3 of 2021)

7 Summary

Considering all these technical features and parameters, the 600 V CoolMOS™ CFD7 offers outstanding reliability in soft-switching and hard-switching topologies.

CFD7 also enables high-power density solutions and achieves the highest efficiency in all target markets. Furthermore, it offers an attractive price and competitive long-term price roadmap. The following efficiency comparison verifies the performance gain of the 600 V CoolMOS™ CFD7.

CFD7 offers a granular portfolio in a large number of packages, enabling customers to choose the product that is the best fit for their designs. With the next step, moving toward the QDPAK package with $R_{DS(on)}$ down to 15 mΩ, the way is prepared for higher power levels in the smallest form factors.

Summing up all the technical and commercial aspects described in this application note, the 600 V CoolMOS™ CFD7 in the QDPAK will shape the market and support the trend to move from THD packages to SMD-based SMPS designs.

SMD packages support fast switching and help reduce the parasitic inductance associated with long-lead packages such as the common TO-220/TO-247 package. In today's SMD-based designs thermal management remains a limiting factor.

The innovative top-side cooling concept of the DDPAK and QDPAK allows thermal decoupling of the PCB and the semiconductor. Customers can use this feature to do the following:

- Increase the power density of their designs by driving the MOSFET to higher output levels.
- Improve the robustness of the design by reducing the board temperature, which leads to longer system lifetimes.
- Achieve low parasitic switching due to the SMD approach and Kelvin-source gate-driver connection, boosting full-load efficiency at the highest power levels. As the DDPAK and QDPAK are fitted with Infineon's highly efficient MOSFET technologies, they support TSC system solutions for PFC as well as high-end MOSFET solutions for soft-switching topologies (e.g., LLC).

In addition, the DDPAK and QDPAK exceed the industry's quality requirements. They survive many more than 2000 TCOB cycles, are MSL1 compliant and totally lead free, and support reduction of the TCO by reducing the manufacturing costs on the customer's side.

Also, Infineon is working on more scaleable package solutions. The evolution from DDPAK toward QDPAK in 2021 was a further step in the direction of broader SMD package portfolios, enabling higher power levels with innovative cooling capabilities.

8 References and materials

[1] F. Stueckler, "**2.5 kW PFC evaluation board with CCM PFC controller ICE3PCS01G**"

[2] M. Kutschak, D. Meneses Herrera, "**1600 W titanium server power supply with 600 V CoolMOS™ G7 in DDPAK and digital control by XMC™**", AN_1712_PL52_1802_095809, Infineon Technologies, May 2018

[3] M. Kutschak, M. Escudero, "**3300 W 52 V LLC with 600 V CoolMOS™ CFD7 and XMC™**", AN_1906_PL52_1906_094110, Infineon Technologies, January 2020

Along with all references and application notes, Infineon Technologies provides extra material not only in written format; in addition, there are training videos available and hands-on training in the use of demo boards and full system solutions.

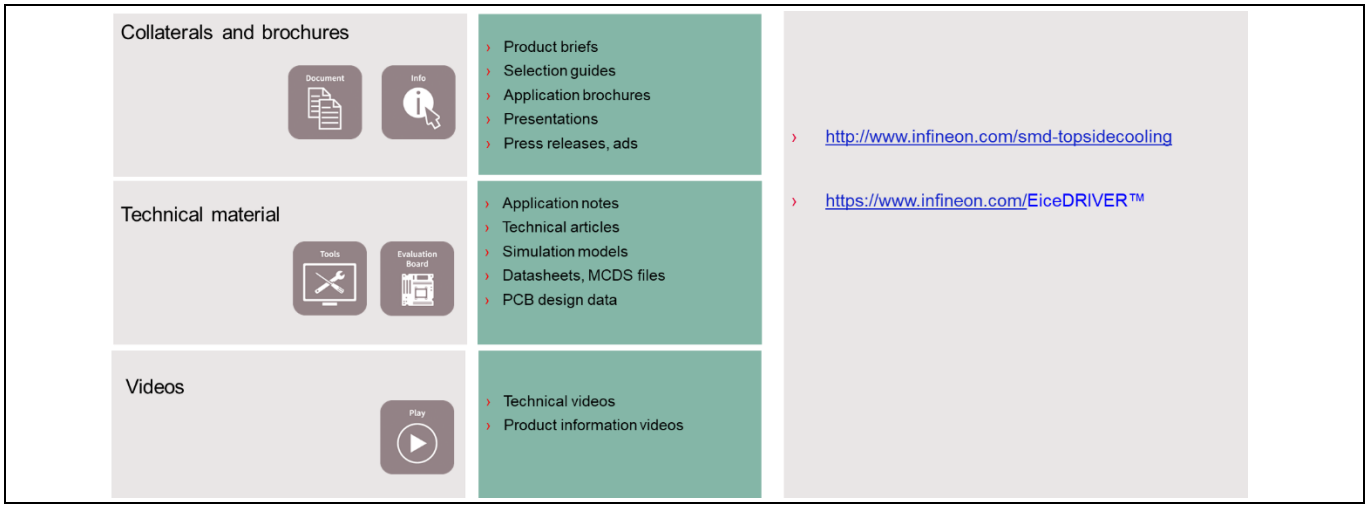


Figure 52 Collaterals

For further information, visit **this page**.

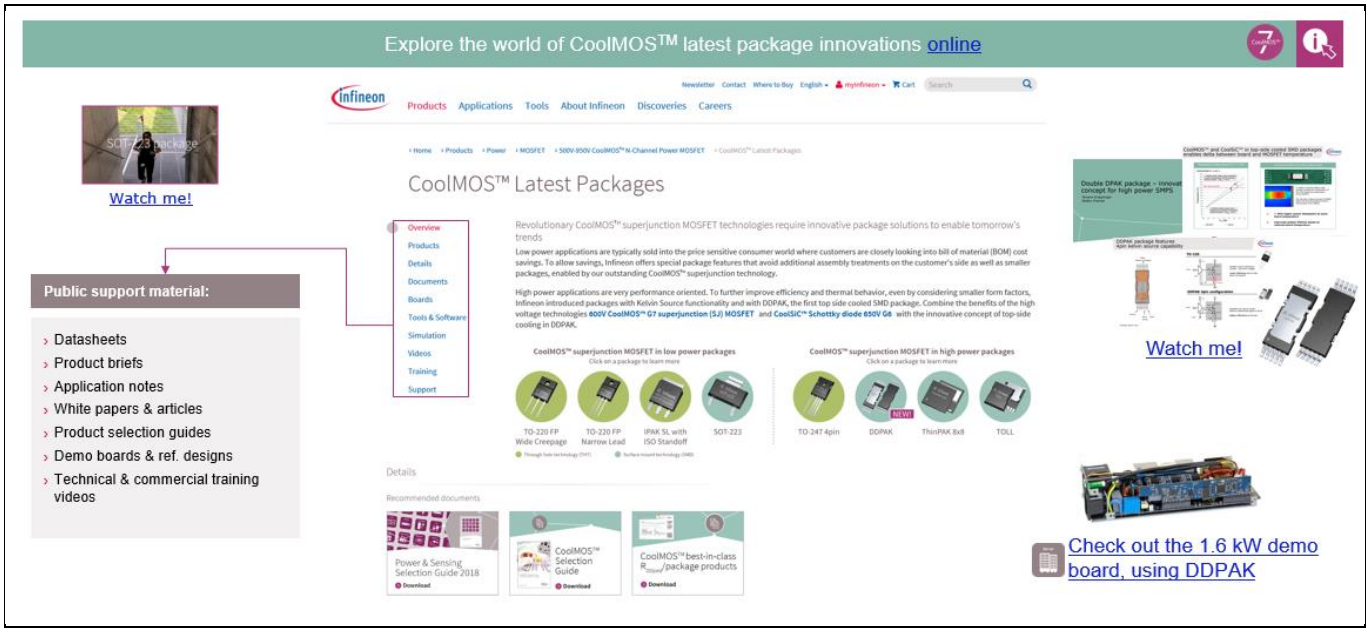


Figure 53 CoolMOS™ latest package innovations

In addition to all boards, colleterals, application notes and training, there will be more material on TSC packages launched later in 2021, giving hints for use of the TSC packages in the automotive area combined with further details on mounting techniques. Further isolation materials will be dicussed in a further application note entitled "**Innovative top-side cooled package solution for high-voltage applications**", and tests with different gap-fillers will be attached to several QDPAKs and afterward thermally analyzed.

Revision history

Document version	Date of release	Description of changes
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