Linear mode operation with high-voltage superjunction MOSFETs

Challenges with CoolMOS™ generation 7 devices in linear mode

About this document

Scope and purpose

This document is aimed to raise awareness that linear mode operation for high-voltage (HV) superjunction (SJ) MOSFETs (such as Infineon's CoolMOS™ – but not only) poses an inherent risk of device destruction.

Therefore, this document defines the term linear mode and highlights the risks with HV SJ MOSFETs.

Finally, it shows how SJ MOSFET devices can be used correctly in certain applications that are prone to linear mode operation best.

Intended audience

This document is intended for power supply designers and power electronic engineers.

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1 Introduction

The development of modern HV power MOSFETs has produced ultrafast switching and ultralow ohmic devices.

The latest Infineon CoolMOS™ generation 7 technology offers undisputed best-in-class $R_{DS(on)}$ in voltage classes ranging from 600 V up to 950 V. Infineon's technology leadership enables not only new and smaller packages (such as the **ThinPAK 5x6** or the **SOT-223**), but also CoolMOS™ products with much smaller $R_{DS(on)}$ values in existing packages.

Similar power semiconductors produced only a decade ago needed at least three times the area to achieve the same performance. In other words, the previous generations of power MOSFETs suffered from at least three times more $R_{DS(on)}$ than modern CoolMOS™ generation 7 chips (with the same chip area).

However, the advance of SJ MOSFET technology towards superfast switching comes with certain disadvantages. As much as modern HV SJ MOSFETs are appreciated for switching mode (SM) operation, they come with limitations that are undesirable for some applications.

Two characteristics are noteworthy:

First, the latest HV SJ MOSFETs experience a narrowing of the safe operating area (SOA) diagram. The reason for this area reduction is that today's state-of-the-art power MOSFETs utilize much smaller silicon die areas for a given on-channel resistance ($R_{DS(on)}$). Unfortunately, that also means the power-handling capabilities (P_{tot}) for a specific $R_{DS(on)}$ decrease, because the thermal resistance values (R_{th} and Z_{th}) increase with smaller chip areas. This is explained with the following formula:

$$R_{th} = \frac{l}{\lambda \cdot A}$$

… where l is the length of the material body, λ the thermal conductivity of the material and A the contact area for the heat transfer (chip size).

Consequently, the usable area in the SOA diagram gets smaller and smaller for modern power semiconductors (compared to previous SJ MOSFET generations with the same $R_{DS(on)}$ values).

Second, modern SJ MOSFETs offer substantially steeper transfer characteristics. This property enables much faster switching, because a small change in the gate-source voltage results in a much higher change in the drain-source current. This feature reduces the power losses in switched-mode power supplies (SMPS) substantially. Nonetheless, the high transconductance is counter-productive for applications that operate in linear mode. Typical applications that tend to operate in linear mode are hot-swap, inrush current limiters, linear voltage regulators, active DC-link discharge circuits and more.

*Note: The continuous development of new power MOSFET generations lead to a continuous decrease of the area-specific on-resistance ($R_{DS(on)}$ * A).*

2 Definition of switched-mode operating modes

Due to the superior switching performance and ultralow power losses, SJ MOSFETs are most commonly used as switching devices in SMPS. Their primary role is to turn-on and turn-off a load current, therefore acting primarily in two operating points: completely on (on-state or ohmic region) or completely off (off-mode or blocking mode).

Table 1 gives an overview of these two operating points and the respective voltage and current conditions in SM operations. The following observation is important: although the current through or the voltage across the MOSFET is high, the power dissipation (being the product of the voltage times the current) remains low to medium in these operating states.

Table 1 Overview of steady-state operating points in SM operation

State	V_{GS} conditions	Current through the device	Voltage across the device	Power dissipation of the MOSFET device
On	V_{GS} voltage is much higher than V_{th}	High	Low	Medium
Off	V_{GS} voltage is much below V_{th}	Very low leakage current	High	Very low

In order to turn-on or turn-off a MOSFET, the diagram in **Figure 1** has to be traversed from operating point off to on or from on to off respectively.

During this switching operation the MOSFET will be exposed to relatively high currents and relatively high voltages until the steady-state is reached again. The time needed to change between these states is defined as the switching time. During this switching time the power on the transistor can reach very high values. This is due to the HV across the switch and the significant current through the switch.

Table 2 summarizes the quantities during these transitions.

Note: Even if this instantaneous power is very high (i.e. several kilowatts) the MOSFET won't be harmed, because switching times remain reasonably small (the resulting energy is small).

In well-designed power supplies, the energy "lost" during this transition is relatively low. Nonetheless, modern power applications, such as power supplies for servers and telecoms, and as well automotive on-board-chargers, tend to reduce these switching losses as much as possible. One approach is therefore to switch the device as fast as possible. This will help to reduce the overlap of voltage and current, in order to reduce the switching losses in hard-switching applications. A more sophisticated approach is to deploy a technique called soft-switching. In this operating mode, the controller decides to turn-on the MOSFET in zero-voltage conditions after the energy stored in the parasitic output capacitance has been transferred to the load.

Table 2 Overview of transient events in SM operation

State	Gate-source voltage conditions	Current through the device	Voltage across the device	Power dissipation of the MOSFET device
Traversing from on to off	From high to low	Medium	Medium	High
traversing from off to on	From low to high	Medium	Medium	High

Figure 1 offers a graphical representation of the output characteristics of a MOSFET, with the most important operating points for SM operation.

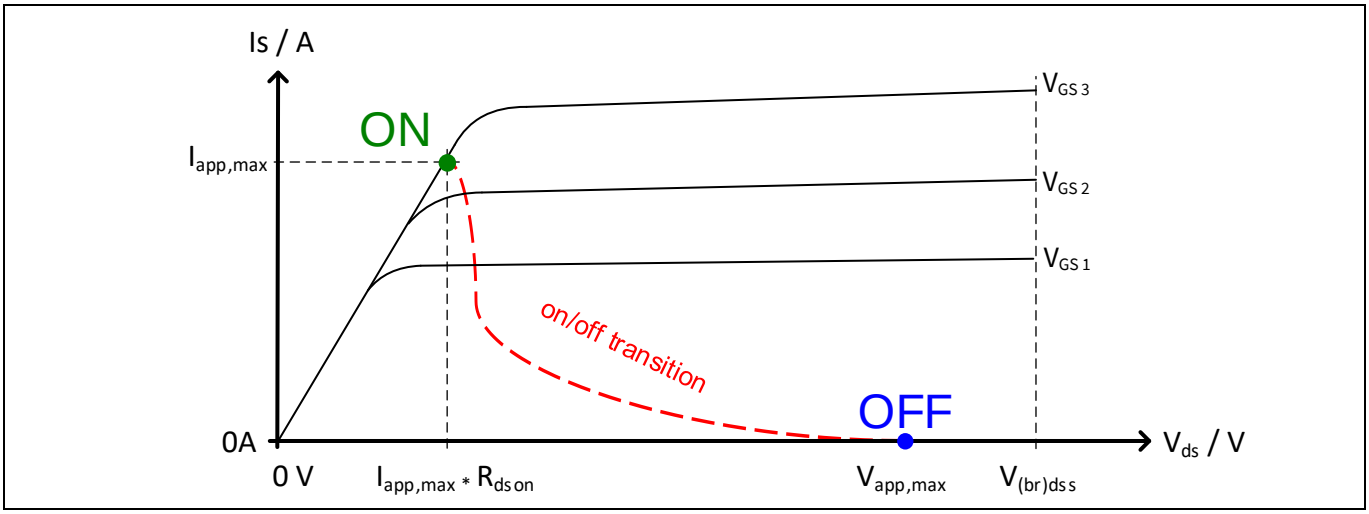

Figure 1 **Output characteristics of a power MOSFET with an indication of the two operating points in SM operation and an exemplary transition between them (red line)**

3 Definition of linear mode operation

After having defined SM operation in Chapter 2, this chapter aims to define linear mode operation.

Before doing so, it is worthwhile taking a closer look at the MOSFET characteristics, especially the output characteristics of a HV SJ MOSFET. **Figure 2** shows the output characteristics of the CoolMOS™ product **IPB60R180P7**. The plot could be divided into two parts: the ohmic region (marked in gray) and the saturation region (highlighted in yellow).

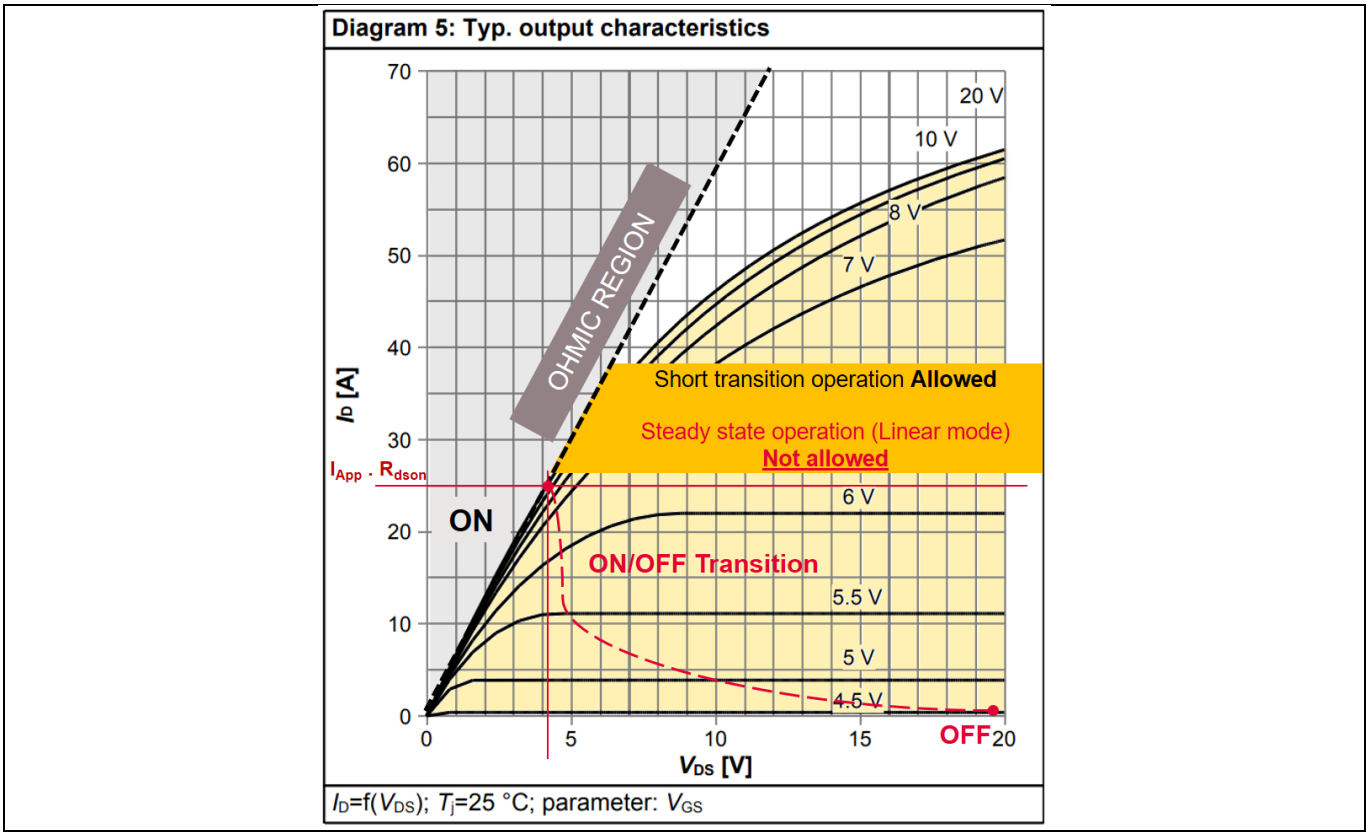

Figure 2 Typical output characteristics of CoolMOS™ IPB60R180P7: ohmic region (gray) and saturation region (yellow) [1]

In the ohmic region, the current through the MOSFET (I_D) is directly proportional to the drain-to-source voltage across the MOSFET (V_{DS}). The MOSFET behaves like a constant resistor ($R_{DS(on)}$) with a linear relation between current and voltage. Due to this “linear” behavior some people might refer to the operation in the ohmic region also as “linear operation of a MOSFET”. Nonetheless, this document refers to this operating mode purely as operation in the ohmic region. Linear mode in this document occurs in saturation mode.

The saturation region of a MOSFET is so called because the channel of a MOSFET is saturated with electrons. As a result, the current through the MOSFET will not increase even if the voltage across the MOSFET is increased. So, no matter how much you bias the FET, it will still produce around the same amount of current through it. You can control that current by modulating the gate-to-source voltage instead. In other words, the MOSFET acts like a constant current source, or a controllable resistor. In this operating mode the gate overdrive voltage (V_{GS}) acts as control quantity. By definition the control voltage (V_{GS}) is greater than the threshold voltage (V_{th}), but less than the V_{GS} voltage needed for full overdrive to reach the ohmic region (and thus a low $R_{DS(on)}$).

This operating mode is commonly known as linear mode. This operating point is characterized by high power dissipation on the MOSFET. The MOSFET is damaged by high voltage and current over a long period.

Furthermore, the term linear mode is used as defined here (explicitly in the saturation region of the MOSFET and not the ohmic region).

As mentioned previously, the MOSFET will not be harmed as long as the energy is relatively low (the traversing between the on and off states happens fast enough). Assuming that the traversing happens very slowly (or even comes to a complete stop in between the operating points), we are in linear mode operation.

Note: *Linear mode operation also occurs during "normal" SM operation – but only for a very short time, which will not harm the MOSFET.*

Linear mode is a common technique applied by low-voltage (LV) MOSFETs to regulate voltages. This technique is well known and has been used for decades throughout the industry, if the right devices are used and the gate voltage is controlled accordingly (see "Temperature stable point") in LV applications.

Nevertheless, for HV SJ MOSFETs, linear mode operation could be critical due to inherent differences in the device physics.

First of all, HV MOSFETs have to withstand a much higher electric field and therefore their physical structure is significantly different than LV MOSFETs.

Additionally, the transconductance of SJ MOSFETs is typically higher than the transconductance of their LV counterparts. Therefore, a potential linear mode operation of HV MOSFETs makes proper control of the gate voltage extremely difficult across all operating points and corner conditions. As a natural consequence, fatal destruction mechanisms like current crowding or compensation charge balance differences within the SJ HV MOSFETs cannot be avoided completely. Reliable operation of HV SJ MOSFETs in linear mode cannot be guaranteed over the intended lifetime!

As mentioned before, short transitions between on and off states of the MOSFET are inherent for MOSFETs that are correctly used in SM operations. During this transition, the power dissipated is typically very high. To understand the limits of the MOSFET in SM operation, the so-called SOA diagram of the datasheet can be used. The next chapter describes the SOA diagram in detail and highlights the limits of usage.

3.1 Safe operating area

The SOA diagram as it appears in the CoolMOS™ datasheets defines the operating limits of a MOSFET. It also gives information about the power dissipation the MOSFET can handle when it is operated in the saturation region.

Figure 3 shows the SOA of CoolMOS™ **IPB60R180P7**. Notice all the limitations and boundaries. Within this, there are more limitations for each individual pulse duration. As the lines on the inside show, they can either be calculated or measured.

The SOA diagram is useful for any application where the MOSFET is dissipating a large amount of power. Customers tend to use the SOA as an indicator of device robustness by comparing SOAs from different datasheets to see which parts can handle more power.

Infineon, as the technology leader in the SJ MOSFET area, has over the years developed many generations of MOSFETs with larger SOA limits, that are more prone to linear mode operation. For the latest CoolMOS™ generation 7 a more advanced SOA diagram has been implemented. We have introduced the thermal instability limit line on the SOA diagram as additional information for our customers.

Please note: Some older MOSFET technologies do not have this information in the SOA – and also, it is not considered on most competitor datasheets.

The SOA can be divided into five separate boundaries, covered in more detail below.

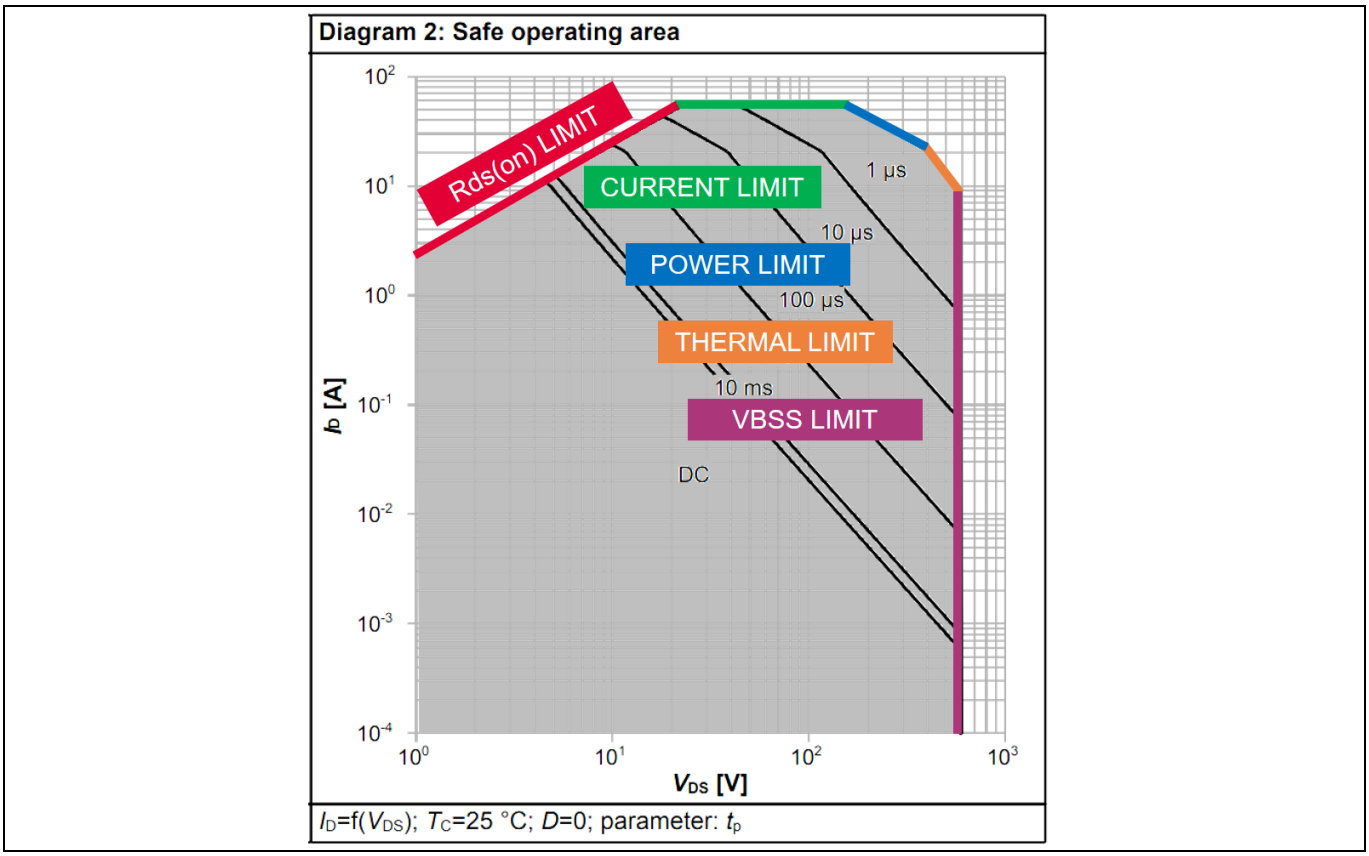

Figure 3 SOA diagram of CoolMOS™ IPB60R180P7 with the respective limits [1]

The first important boundary is the red line, which defines the $R_{DS(on)}$ limitation. This is where the amount of current that can be pushed through the device is limited by the on-resistance, at the maximum allowed junction temperature of the device. This line has a positive constant slope: every point on the line represents the same resistance defined according to Ohm's law.

The next limitation line is the current limitation, shown in green. The current-limit line is typically defined by the maximum current the weakest part of the MOSFET product can handle. Therefore, the amount of this current will be strongly package-dependent. Also, the die size will impact the current handling capability of the package, because it determines the bonding scheme (number of bond wires, bond wire diameter).

The third limitation, in blue, is the maximum power limitation line. This line has a constant negative slope because every point on this line represents the same constant power. So, on a logarithmic curve, this will have a negative slope.

Now, the fourth limitation, the thermal instability limitation, is where it becomes very important to actually measure the capability of the device. A MOSFET is considered to be thermally unstable if the power generated rises faster than the power dissipated overtemperature. To explore this concept of thermal instability, see Chapter 3.2 "Transfer characteristics and temperature stable point").

The fifth region highlighted in purple is the breakdown voltage limitation – simply the breakdown voltage of the MOSFET. The exemplary devices that act as the basis for the SOA in **Figure 3** offer a 600 V breakdown BVDSS, which is why this line has been imposed at 600 V only.

3.2 Transfer characteristics and temperature stable point

A very significant point for the MOSFET operation is the intersection of the transfer curves at different temperatures. This point is called temperature stable point (TSP) or zero temperature coefficient (ZTC). **Figure 4** shows the transfer characteristics of a SJ CoolMOS™ generation 7 MOSFET as an example (**IPB60R180P7**).

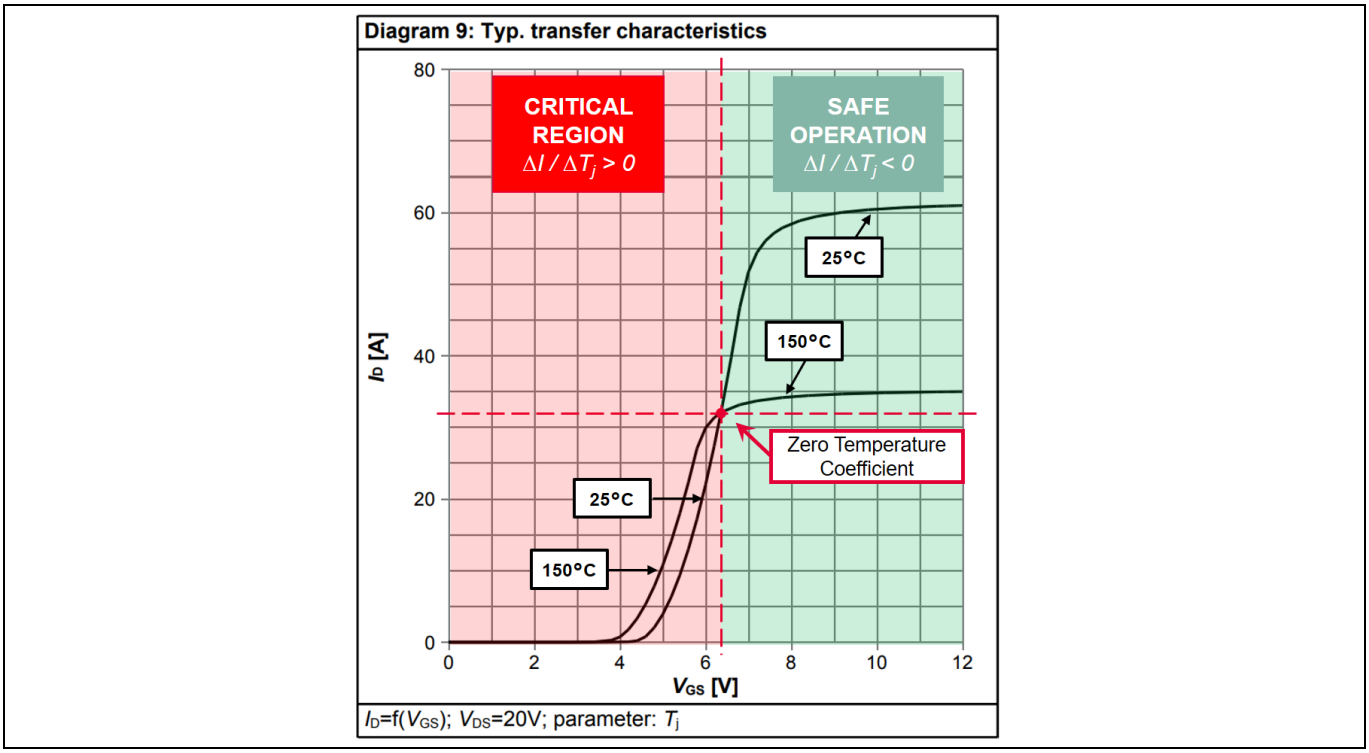

Figure 4 Transfer characteristics of CoolMOS™ IPB60R180P7: safe operation (green area) and critical region (red area) [1]

The point where the gain becomes independent of the temperature (ZTC) is indicated. As name indicates, this point marks the gate voltage level where the gain of the power MOSFET does not depend on the MOSFET's temperature.

If the gate voltage is higher than this point, the transconductance of the MOSFET will decrease. As a result, the device current will also be limited with rising temperature. This will reduce the conduction losses and subsequently the device temperature (negative feedback loop). This is the preferred operating point for safe operation of MOSFETs.

On the other hand, the effect is the opposite if the gate voltage is below the temperature stable point: the gain of the MOSFET will increase as the device temperature increases. This is positive feedback, which must be avoided in steady-state, since a higher transconductance will further increase the device current from drain to source, which will in turn increase the current through the MOSFET, the conduction losses and thus the device temperature even further. A thermal runaway of the device is likely to happen, which will lead to fatal destruction of the device!

To understand the origin of this limitation, it is necessary to consider the criteria for thermal instability.

A MOSFET is considered to be thermally unstable if the power generated rises faster than the power dissipated overtemperature [2]. As a consequence, the temperature of the system is not stable, and the system is not in thermal equilibrium, unlike for the maximum-power limit line [3].

$$V_{DS}.\frac{\Delta I}{\Delta T_J} > \frac{1}{Z_{thJC}(t_{pulse})}$$

The equation above defines the range where the MOSFET may encounter thermal instability. The term $(\frac{\Delta I}{\Delta T_J})$ is the *temperature coefficient*. Since V_{DS} is greater than 0 and $\frac{1}{Z_{thJC}(t_{pulse})}$ is greater than 0 thermal instability can occur only if the temperature coefficient of the drain-to-source current is positive.

To explore this concept of thermal instability on the CoolMOS™, we have to define the temperature coefficient, which is given as the change in current over the change in junction temperature of the device. So, if we look at the **Figure 4** transfer characteristics curve, usually Diagram 9 in the CoolMOS™ datasheet, it gives the drain-to-source current of the FET versus the increasing gate-to-source voltage of the FET at two different temperatures (usually 25°C and 150°C). Take as a reference the ZTC, where an increase in the junction temperature of the device yields no change in the current flowing through the device.

Now at points above the ZTC, as junction temperature increases from 25°C to 150°C, we see that the current actually decreases. So as the device heats up, the power dissipated through the device decreases. There's no fundamental risk of instability – you can still overheat the device (e.g., due to over-current) but there's no risk of thermal runaway.

Considering currents below the ZTC, we see the phenomenon where the junction temperature increases from, again, 25°C to 150°C, and the current running through the device increases, because the temperature coefficient is now greater than zero. And that increase in current can lead to an increase in $R_{DS(on)}$ and a further increase in temperature, which can in turn lead to more current, and a positive feedback loop, which leads to instability.

4 CoolMOS™ solution design guidelines

Typical applications that tend to operate in linear mode are hot-swap, inrush current limiters, linear voltage regulators, active DC-link discharge circuits and more.

4.1 Using CoolMOS™ CFD7A in active DC-link discharge applications for electric vehicles

We do not recommend using Automotive CoolMOS™ in linear mode in automotive applications [4] [5].

For applications that require active dissipation of energy (such as active DC-link discharge), we recommend using CoolMOS™ CFD7A to act as a control switch for a passive load, such as a power resistor. By doing so, linear mode operation of the MOSFET can be avoided. As a result, the power on the MOSFET is reduced significantly, as it only acts like a control switch while the discharge resistor handles the power dissipation.

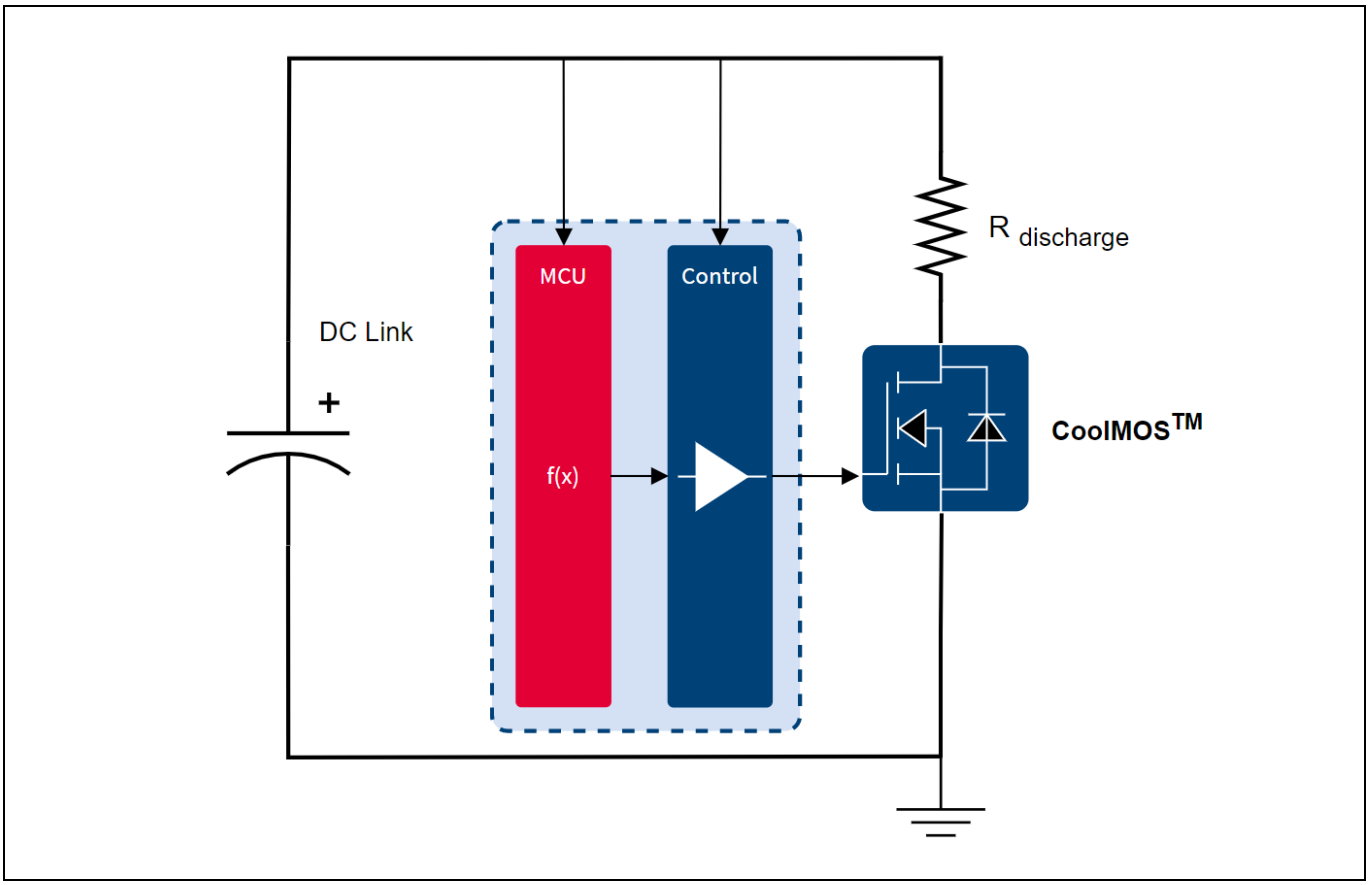

Figure 5 Principle of active DC-link discharge circuitry using CoolMOS™ as a control switch and a passive resistor for energy dissipation

Additionally, this concept offers the advantage of shaping the discharge current by PWM control: the duty cycle directly controls the discharge time and the average power on the resistor. Thus, different discharge scenarios can be implemented by software. Figures 6 and 7 show this concept implemented in simulation.

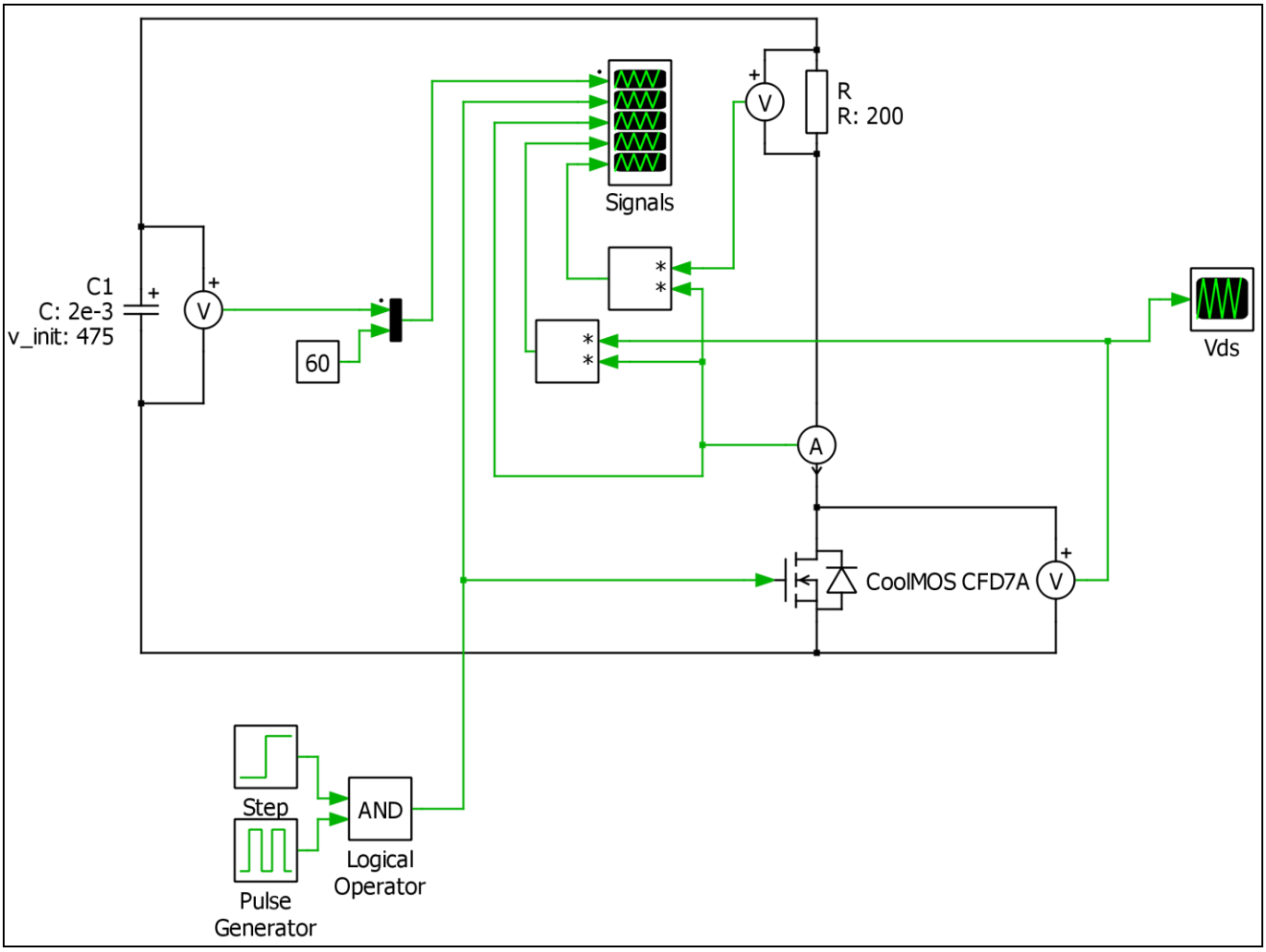

Figure 6 Principle of using PWM to control discharge behavior

In this scenario, the actual transition of the switching device proceeds, while the on/off levels of the gate signal are applied. Upon receiving a gate drive signal above the threshold, the device impedance has a maximum value while in the off-state and a minimum value in the on-state. With this method, the switching device passes for a short period through a transitional state (linear mode), in a way that the power dissipation at the MOSFET is significantly low so that the device is capable of dissipating the full charge from the DC-link capacitor. By maintaining this operation for a sufficient time, the DC-link capacitor can be very effectively discharged.

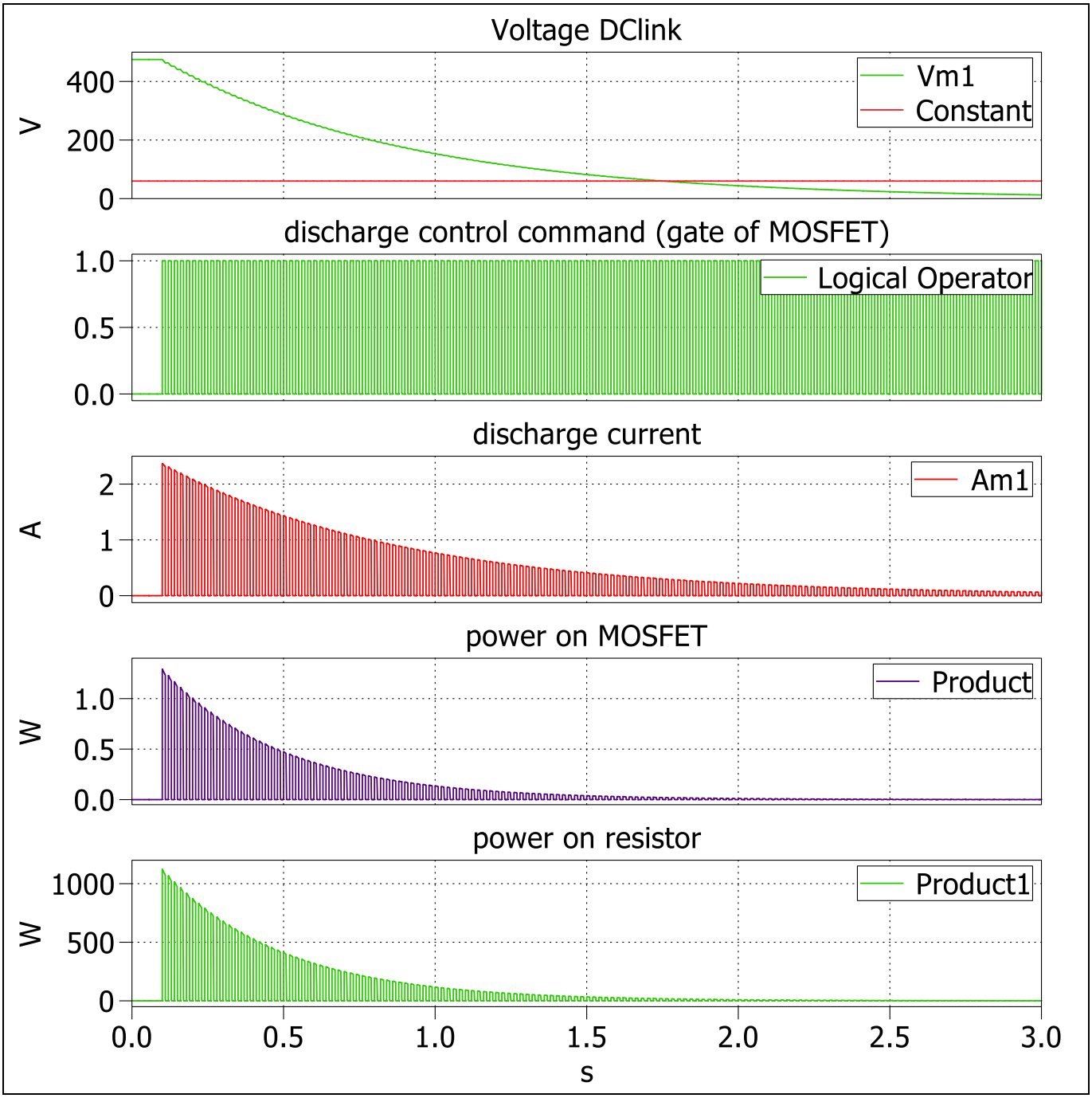

Figure 7 **Active DC-link discharge with PWM (D = 50 percent) helps the average power on the resistor**

5 Conclusion

The latest CoolMOS™ generation 7 series from Infineon offers outstanding performance and long-term reliability when used in SM operation where high efficiency is the ultimate goal. To judge the limits of the device in this operating state, please refer to the SOA diagrams provided on the individual datasheets.

For automotive applications, we do not recommend using Automotive HV SJ MOSFETs in linear mode. However, most linear-mode applications can be modified using SJ MOSFETs to become reliable and safe. Chapter 4.1 shows an example for active DC-link discharge applications.

6 References

[1] CoolMOS™ IPB60R180P7 datasheet: https://www.infineon.com/dgdl/Infineon-IPB60R180P7-DS-v02_01-EN.pdf?fileId=5546d4625ee5d4cd015f2a6b8e590481

[2] Infineon application note “Linear Mode Operation and Safe Operating Diagram of Power MOSFETs”: https://www.infineon.com/dgdl/Infineon-ApplicationNote_Linear_Mode_Operation_Safe_Operation_Diagram_MOSFETs-AN-v01_00-EN.pdf?fileId=db3a30433e30e4bf013e3646e9381200

[3] P. Spirito et al., “Thermal Instabilities in High Current Power MOS Devices: Experimental Evidence, Electro-Thermal Simulations and Analytical Modelling”, MIEL 2002, 23rd International Conference on Microelectronics, Vol. 1, May 12–15, 2002, pp. 23–30.

[4] CoolMOS™ CFD7A series overview: https://www.infineon.com/cfd7a

[5] Infineon application note “Automotive MOSFETs in Linear Applications: Thermal Instability”: https://www.infineon.com/dgdl/AutomotiveMOSFETsinLinearApplication-ThermalInstability.pdf?fileId=db3a304412b407950112b4188af12622

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