600 V CoolMOS™ S7 with temperature sense

About this document

Scope and purpose

This application note describes the functionality, target applications, and benefits of the new temperature sensing feature of Infineon's CoolMOS™ S7 family of products.

Intended audience

This document is intended for design engineers, technicians, and developers of electronic systems.

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1 Introduction

The CoolMOS™ S7T family of power MOSFETs from Infineon has added additional safety through temperature sensing. The embedded temperature sensor significantly enhances the accuracy of junction temperature sensing and robustness. The S7T family is designed to ensure easy and seamless implementation while allowing optimal utilization of both the power transistor and the system as a whole. The CoolMOS™ S7T family is released for industrial and automotive applications, featuring various package variants, which is shown in Section 1.1 below.

The following sections will give an overview on the portfolio and how to use the temperature sensing feature in an application.

1.1 Product portfolio

CoolMOS™ S7T is primarily intended for industrial applications, nevertheless, there are also products qualified for automotive applications available which can be found on Infineon's CoolMOS™ S7A webpage.

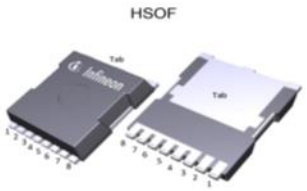
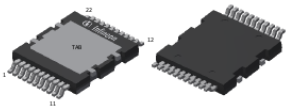
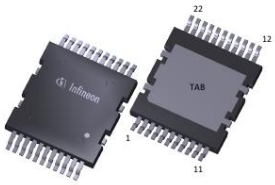
600 V CoolMOS™ S7T			
	TOLL	QDPAK	
$R_{DS(on),max}$ [mΩ]	HSOF 	PG-HDSOP-22 	PG-HDSOP-22 
65	IPT60T065S7		
40	IPT60T040S7		
22	IPT60T022S7	IPDQ60T022S7	IPQC60T022S7
17		IPDQ60T017S7	IPQC60T017S7
10		IPDQ60T010S7	IPQC60T010S7

Figure 1 CoolMOS™ S7T portfolio

Infineon's CoolMOS™ S7T portfolio had three products in the TO-leadless (TOLL) package, with an $R_{DS(on),max}$ of 22, 40, and 60 mΩ at a junction temperature (T_j) of 25°C and a rated blocking voltage of 600 V. This portfolio is now extended down to 10 mΩ in QDPAK package with both top-side and bottom-side cooling options. For further information, check the Infineon website.

1.2 Target applications

These products can be used in various applications with limited switching frequency requirements or solid-state operations (continuous conducting) with fast turn-off requirements during fault events.

1.2.1 Totem-pole PFC (slow-switching leg)

In totem-pole power factor correction (PFC), CoolMOS™ power MOSFETs can be used in the slow-switching leg, which is operated as a rectifier, and therefore, switching occurs only with the line frequency. There, the devices switch with a frequency of 50 or 60 Hz. This can be seen in Figure 2, which also shows the operating principle.

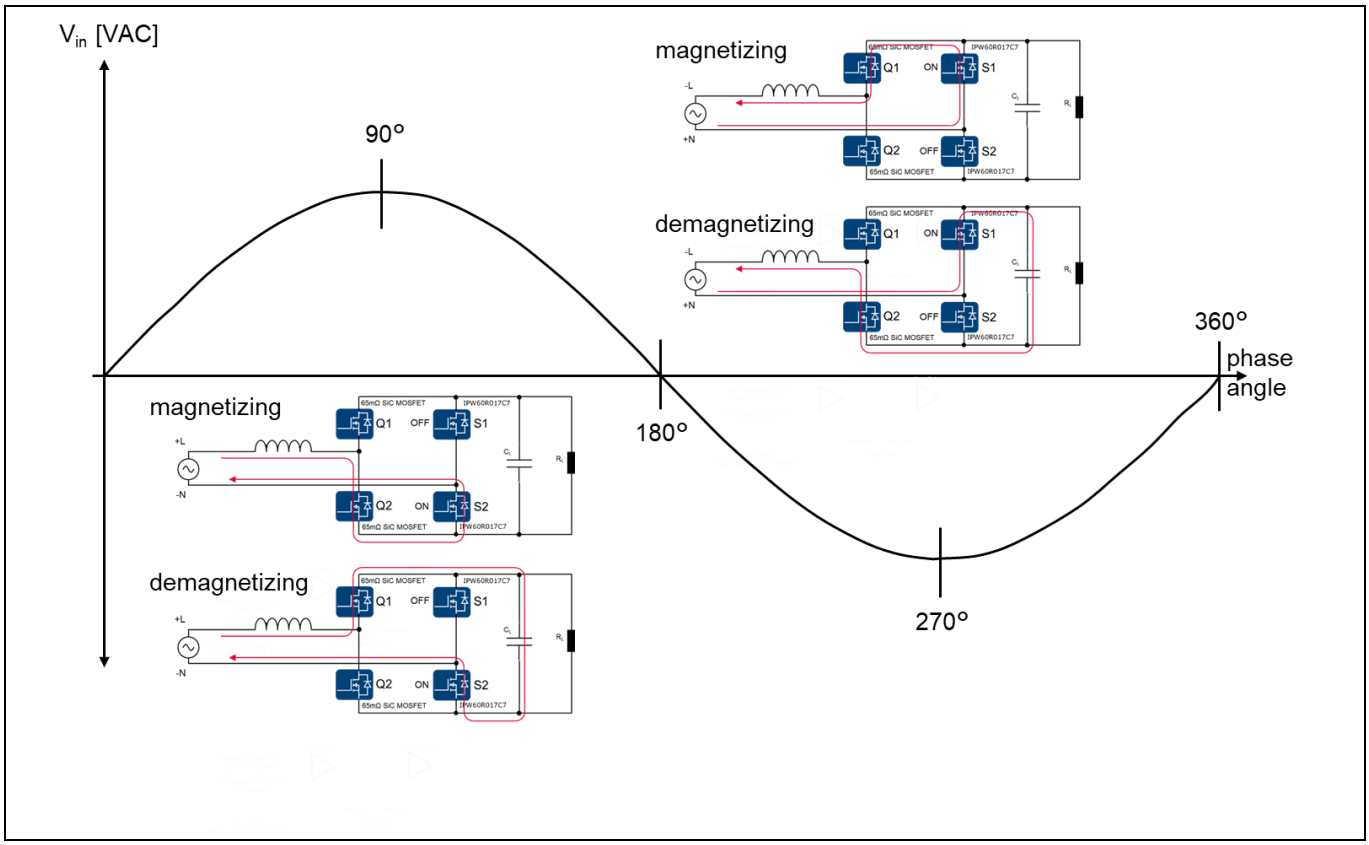


Figure 2 Block diagram and operating principle of the totem-pole PFC

As shown in the figure, S1 and S2, currently based on C7 and or S7, can be replaced with the new CoolMOS™ S7 family with temperature sensing. Additionally, S1 is only active during the positive half of the AC sinewave and S2 on the negative half of the sinewave. This means only one switch is turned on while the other one is completely turned off. In this application or topology, only the $R_{DS(on)}$ is relevant, not the switching behavior. Implementing temperature sensing can increase the reliability of the overall system.

1.2.2 Solid-state relay (SSR)

The most commonly used relays, from 110 V AC to 400 V AC and 300 V DC to 700 V DC, and the current range of 0 A to 16 A, are electromechanical relays (EMR). An EMR is an actuator device with electrically controlled physical moving parts. This is achieved by having an electromagnetic coil inside the relay, which produces a magnetic field that closes or opens the physical contacts of the relay. EMRs intrinsically enable galvanic isolation of the control and high-voltage circuits.

The main advantage an EMR is its affordability and very high power density. Power density is defined as a key performance indicator (KPI) of $\frac{V_{sw} \cdot I_{nominal}}{Volume}$. The disadvantages of an EMR include slow response times, high control power consumption, arcing between contacts, sensitivity to vibration and orientation, and acoustic switching noise. Mechanical contacts deteriorate over time, especially in applications requiring frequent switching events under biased (loaded) conditions. All these problems result in reliability and durability issues.

Compared to EMRs, solid-state relays (SSR) have no moving parts, providing the same power density and size as an EMR with improved durability. To gradually move from EMRs and adopt SSRs, Infineon introduces the new CoolMOS™ S7 family, which also increases safety through the new temperature sensing feature.

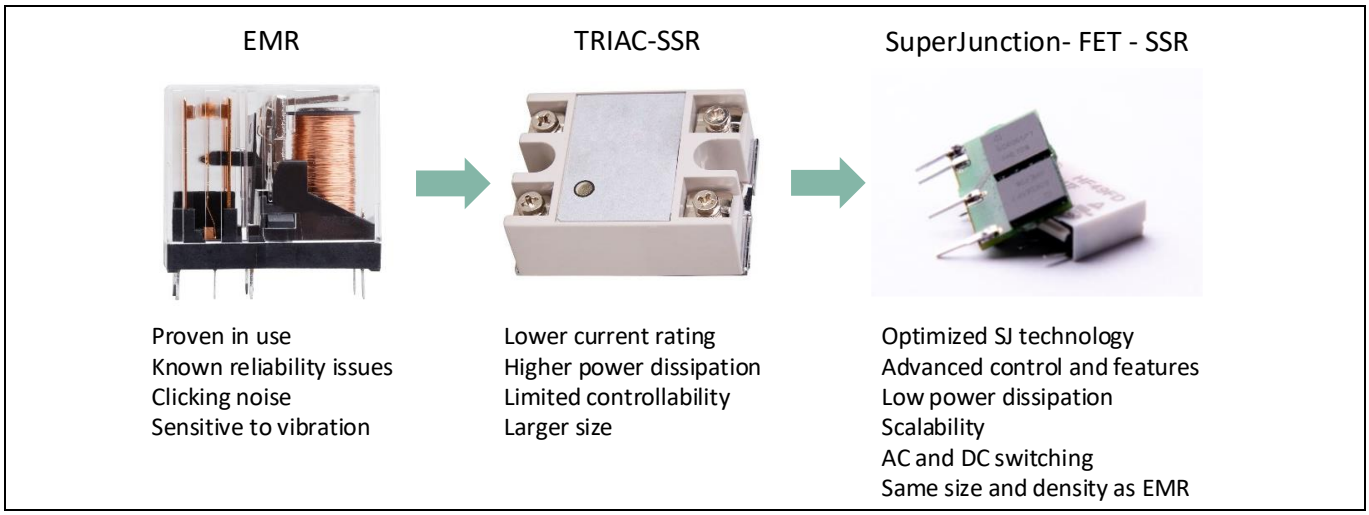


Figure 3 Looking to the future with superjunction FET SSRs

1.2.3 Solid-state circuit breaker (SSCB)

The solid-state circuit breaker is another target application where CoolMOS™ S7T can provide an additional safety feature, especially during overload operations. SSCBs combine all functions of a power distribution topology into a single device.

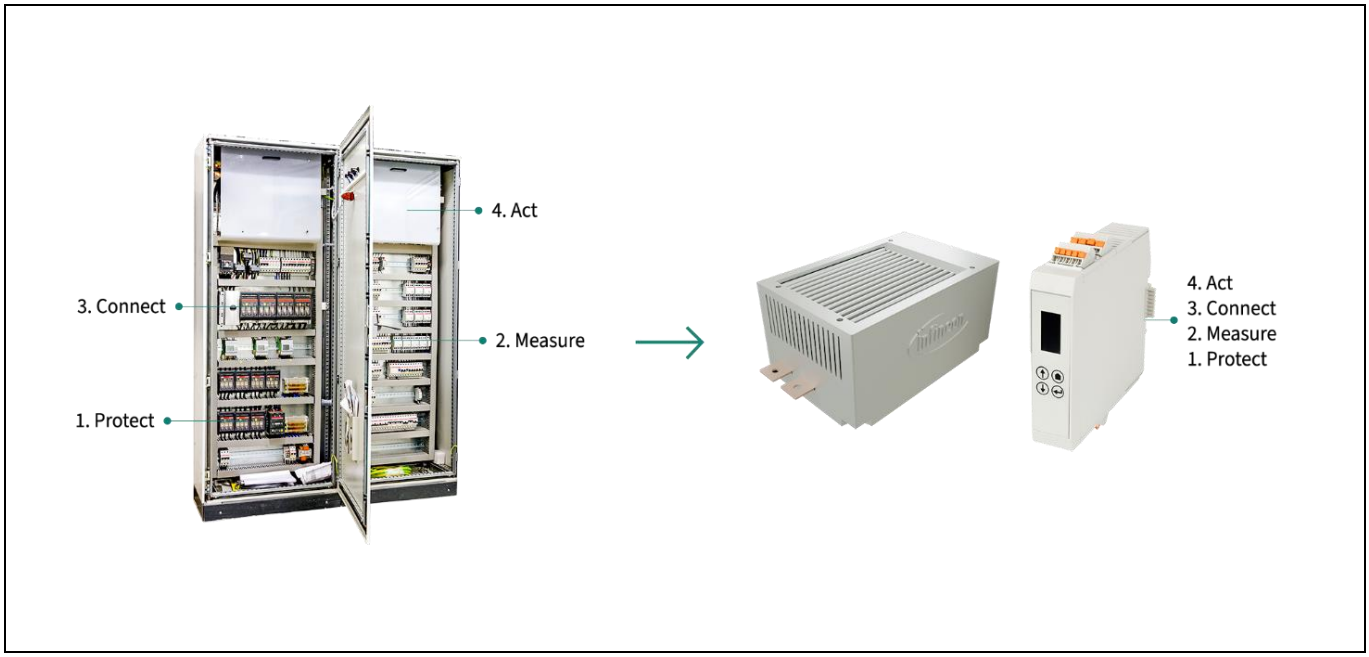


Figure 4 SSCBs combine all required functions in a single device

The combination of fast-switching devices in failure and SSCBs helps reduce the protection time from milliseconds to sub-microseconds. Additionally, it eliminates maintenance and manual diagnostics by providing wear- and arc-free operation and reduces space by removing the arcing chamber.

While these are the main target applications, the CoolMOS™ S7T family of MOSFETs can be used for numerous other applications.

2 Technical differences between CoolMOS™ S7 and S7T

2.1 Package and pin-out

In general, the package has the same outer dimensions and also the lead frame thickness stays completely the same as in CoolMOS™ S7. However, pin 2 for CoolMOS™ S7T in the TOLL package has been changed and is used for temperature sensing. No driver or kelvin source is available for this product anymore.

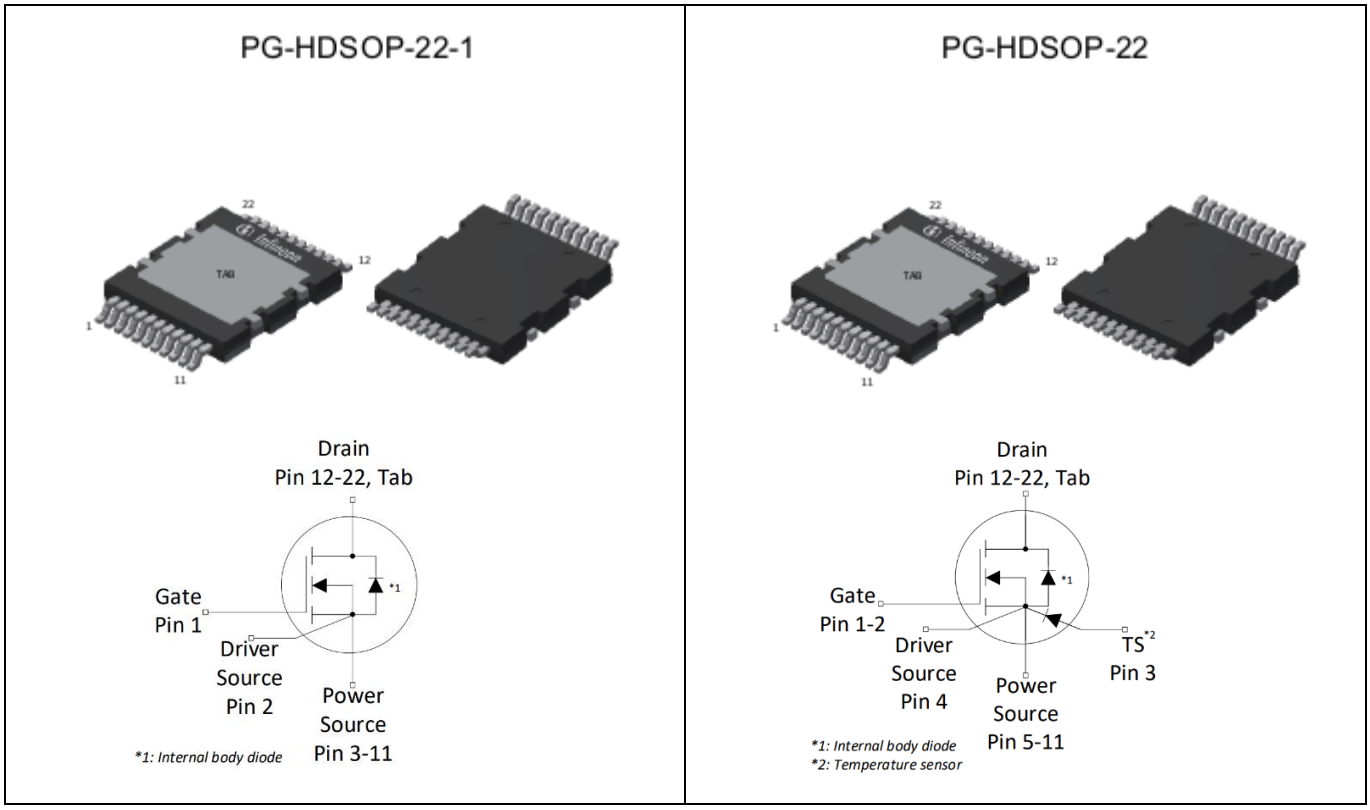


Figure 5 Package pin-out: CoolMOS™ S7 (left), CoolMOS™ S7T (right)

The pin-out for CoolMOS™ S7T in QDPAK is changed to allow both a TS and a driver or kelvin source (KS) pin as well as a gate sense or kelvin gate pin for in situ monitoring of the connection to the gate pin in the application.

2.2 Temperature sensor

Although switch designs typically include overtemperature protection, the temperature sensors are often located on the heatsink where the power semiconductors are mounted or connected, which provides good thermal protection. Since the R_{TH} chain from the junction to the sensor is typically very high, it results in significant latency between the thermal increase of the power semiconductor due to fault events. For S7T devices, the thermal sensor is placed as close to the active cells in the power semiconductor as possible, leading to reduced delay times (further described in Section 3.2). The location of the temperature sensor brings an additional safety feature to the overall system alongside the implementation of well-known thermal protection concepts.

The temperature sensor is simply a series connection of three diodes. Due to the linear temperature behavior of these diodes, their forward voltage (V_F) directly relates to a certain temperature these diodes have, provided they are biased with a current source.

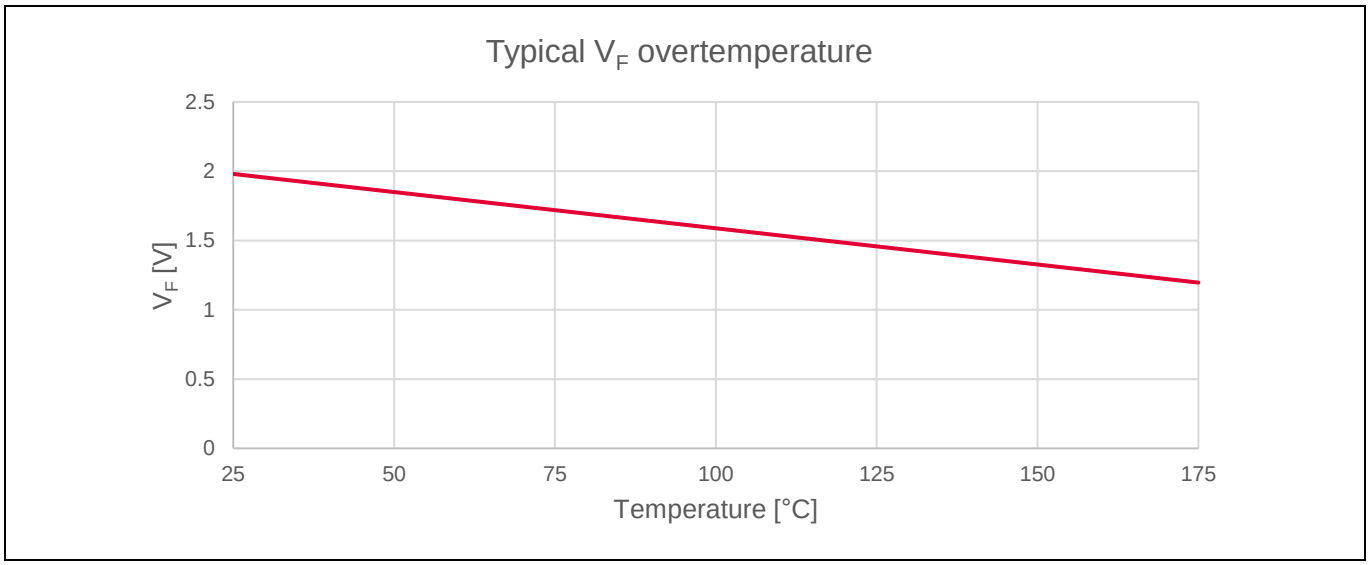


Figure 6 V_F overtemperature of the sensor diodes for a forward current of 200 µA

The sense current I_F for the above diagram is 200 µA, resulting in a V_F (of the diodes) = 1.9806 V for T_j = 25°C and V_F 1.1963 V for T_j = 175°C. This leads to a sensor forward voltage temperature coefficient (TC) of 5.2287 mV/K at I_F = 200 µA.

The design of the chip itself is completely carried over from the well-known CoolMOS™ S7, and the temperature sensor is also implemented near the gate pad.

3 Temperature readout

To understand how the temperature sensor works, a procedure for reading out information from the sensor is needed.

3.1 Procedure

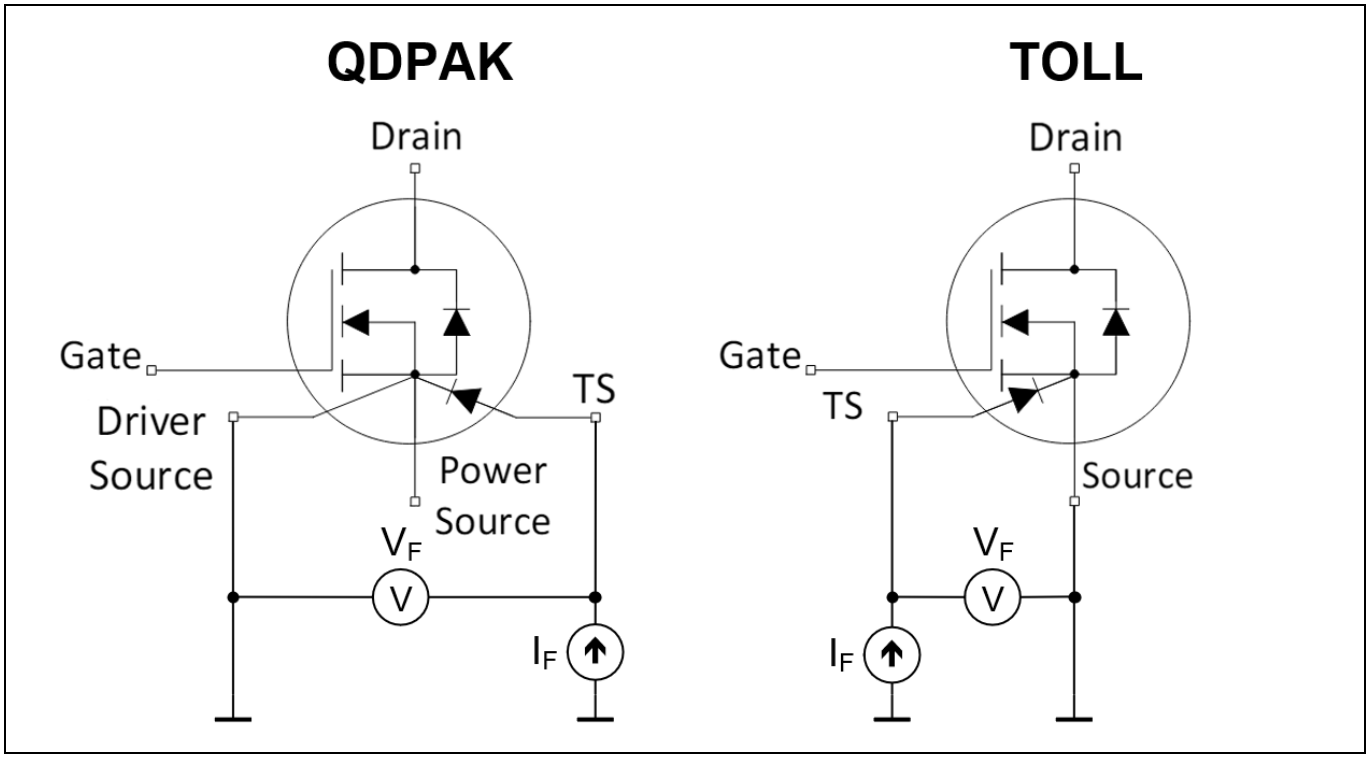


Figure 7 Simplified schematic for the temperature readout

As shown in Figure 7, it is necessary to force a current (I_F) through the temperature sensor. This current is stated in the corresponding product datasheets and is typically set to 200 µA. At the same time, the voltage from the temperature pin to source (V_F) can also be sensed.

Since CoolMOS™ S7T TOLL products no longer have a driver source, V_F sensing is also influenced by parasitic resistances such as the design, package, PCB, and drain current flowing. For QDPAK products, the V_F should be measured between the TS and the driver or kelvin source pin. It is recommended to place the V_F as close to the pins as possible or directly on them. The related datasheets of the S7T products represent the ideal connection without parasitics.

This means that the designer needs to know which I_D is flowing and what the parasitics are in the sensing loop. To provide an easier adaption, the available simulation models of the S7T TOLL products include the parasitics from the design and package resistances. Therefore, it is recommended to verify the resulting correlation of V_F and T_j of the customer system using a spice simulation. For QDPAK, this is not necessary as using the KS pin as reference for the read-out effectively removes the voltage drop caused by the parasitics, as shown in Figure 8.

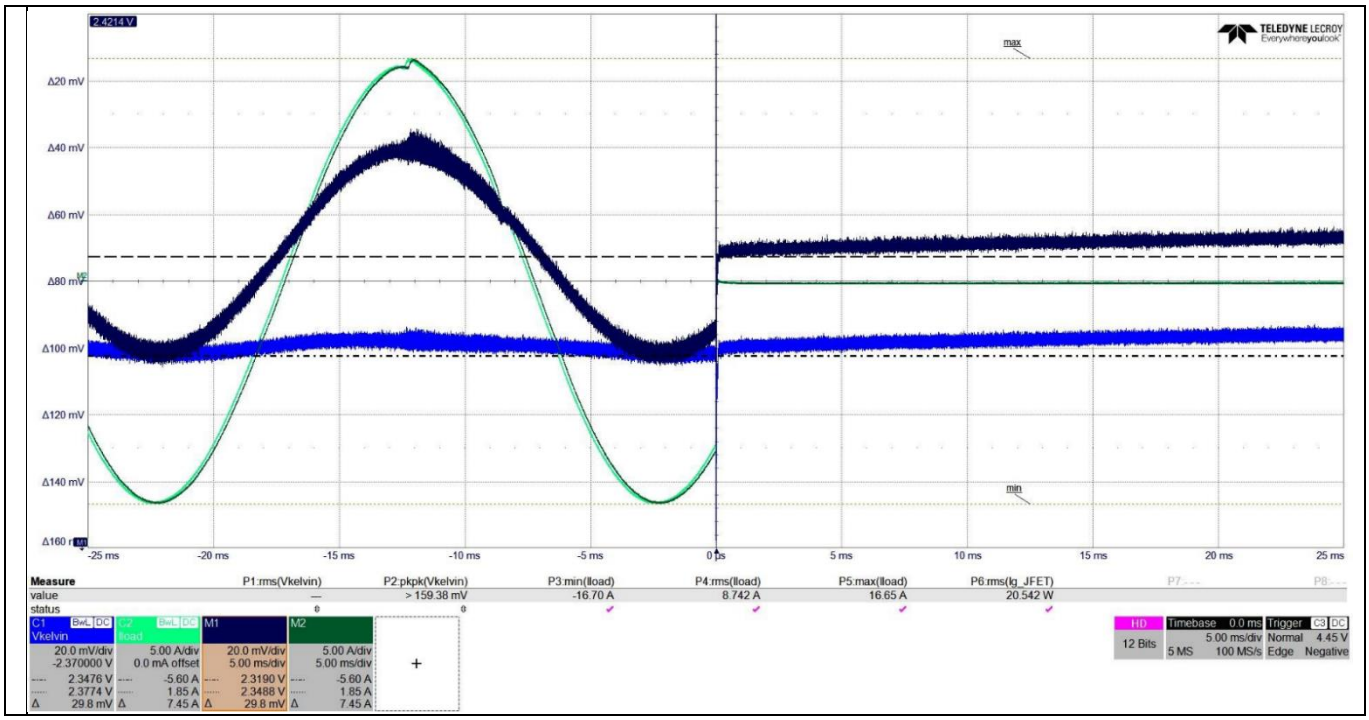


Figure 8 **Overtemperature shutdown of a TS device with temperature signal read-out between TS and power source (load current = dark green, TS signal = dark blue) and between TS and KS (load current = green, TS signal = blue)**

3.2 Hotspot to thermal sensor ΔT

Figure 9 shows how the temperature sense diodes are not directly at the center of the chip's active area; there is still a distance between the real hotspot at the center of the active area and the temperature sensing diodes. Hence, the designer needs to consider a delta of the temperature between the hotspot and temperature sensor.

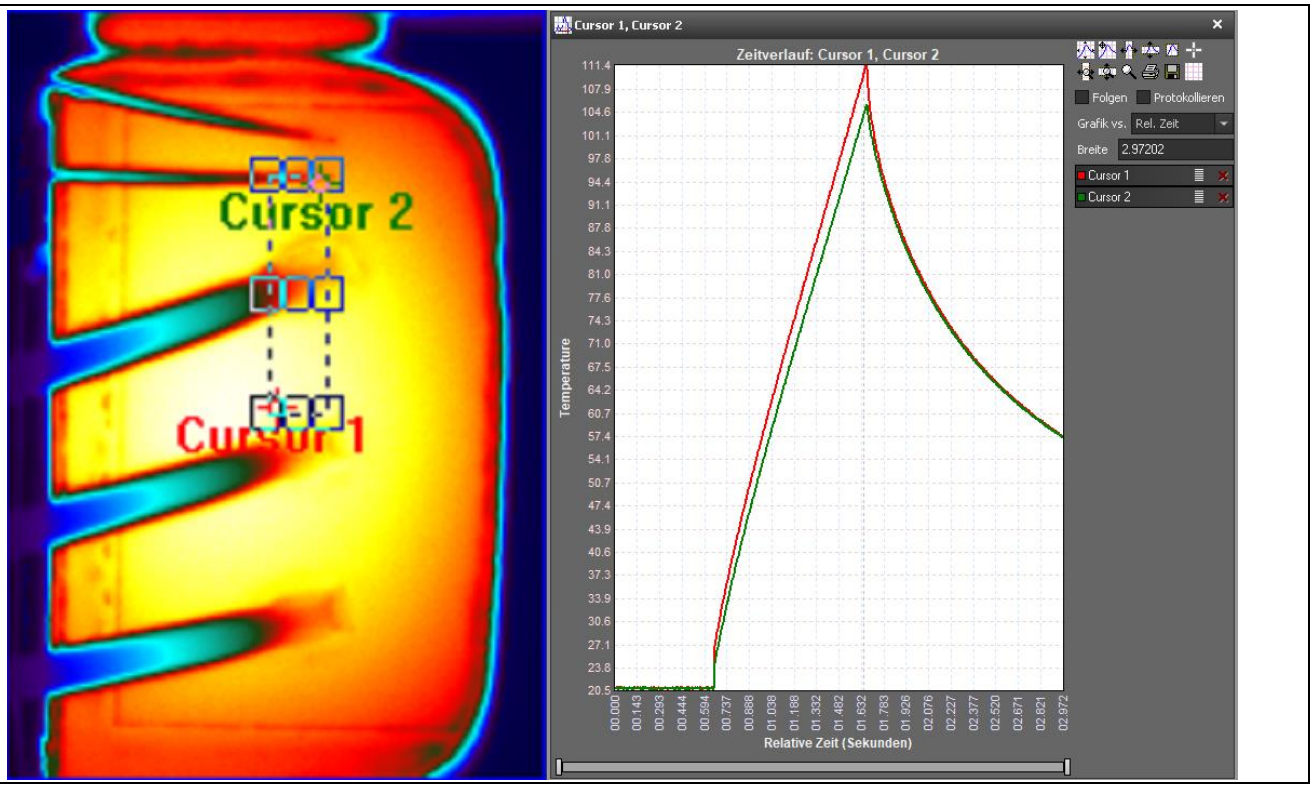


Figure 9 Delta between the hotspot and temperature sensor

Figure 9 (left) clearly shows the hottest point is located at **Cursor 1**, which is the center of the active area. **Cursor 2** is the location of the temperature sense diodes. In Figure 9(right), the red line corresponds to the temperature of the hotspot and the green line represents the temperature of the diode sensor. Due to the distance and the thermal impedance between these two locations, a delta temperature (ΔT = T_hotspot - T_sense) of ~5 K is present. As there is a thermal impedance, ΔT depends on the settling time, which means the delta is higher for shorter heat pulses compared to longer heat pulses. Figure 10 and Figure 11 show the behavior of the ΔT between hot spot and temperature sensor for each product.

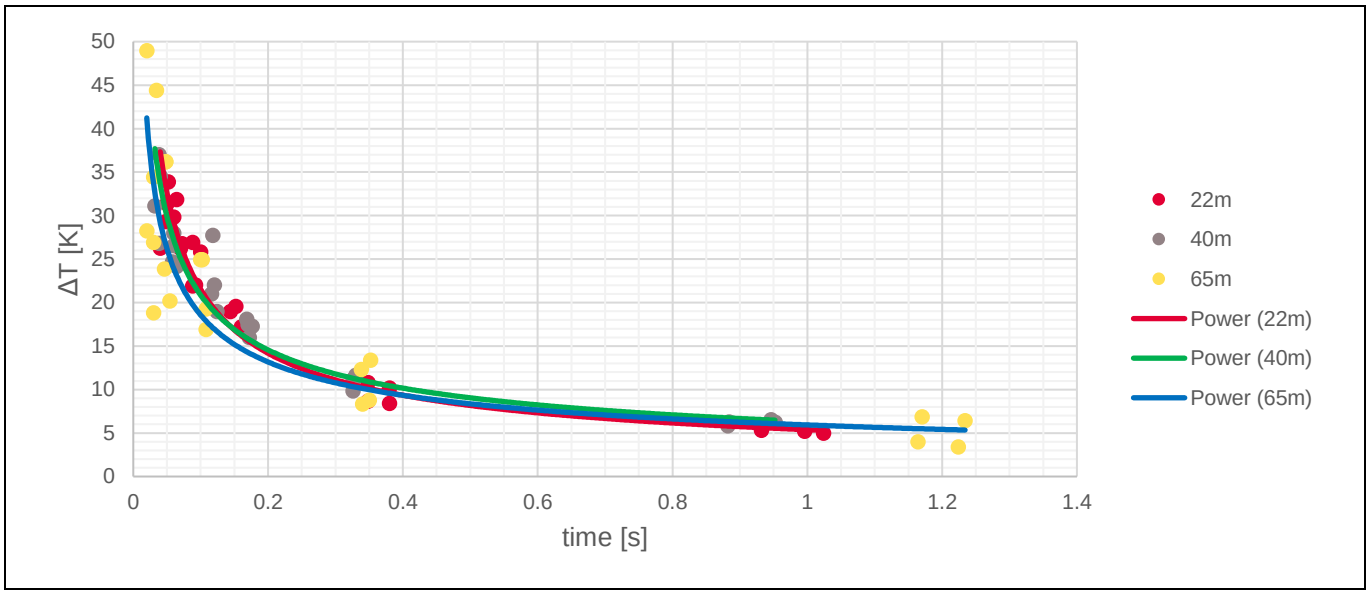


Figure 10 ΔT based on heat pulse for TOLL (22, 40, and 65 mΩ devices)

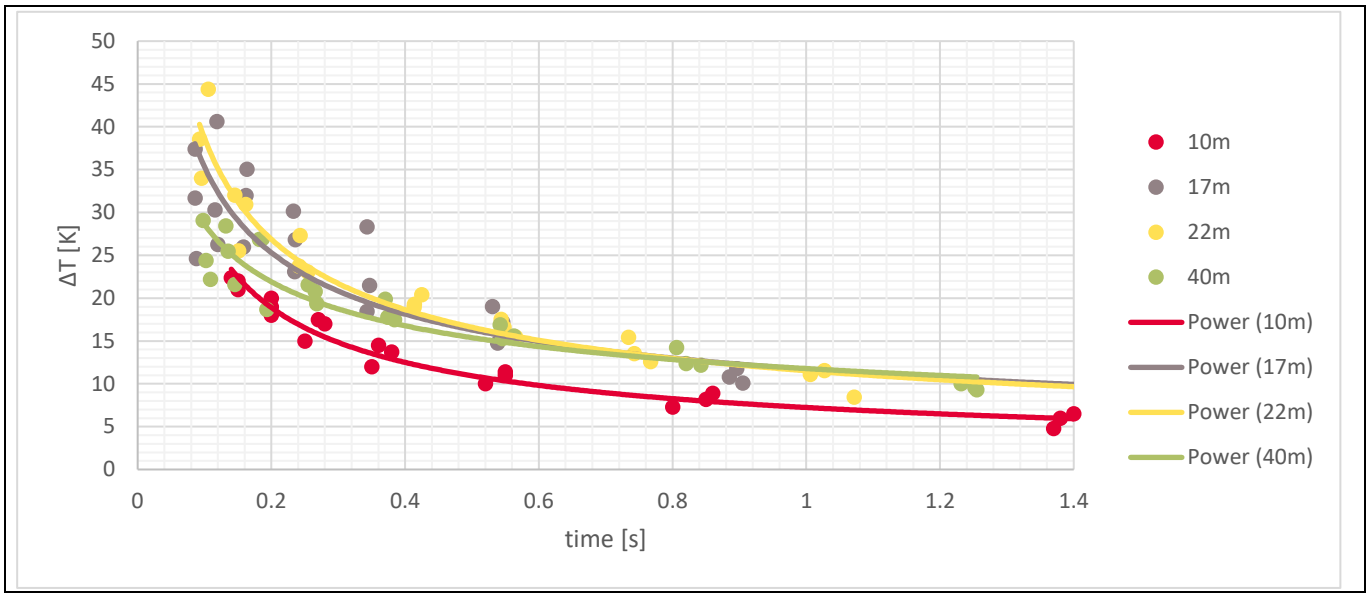


Figure 11 ΔT based on heat pulse for QDPAK (10, 17, 22, and 40mΩ devices)

The following delta temperatures can be extracted based on these diagrams.

Table 1 Delta temperature depending on heat pulse

Time	ΔT (TOLL)	ΔT (QDPAK)
< 50 ms	> 30 K	> 35 K
< 100 ms	> 20 K	> 30 K
< 400 ms	> 10 K	> 15 K
< 1 s	> 5 K	> 10 K
> 1 s	~5 K	~8 K

Notice how these time constants do not evolve with component aging and thus can be hardwired into the measurement setup to compensate for these differences.

Furthermore, ΔT can be explained over the power per mm² on the different dies. This is described in the following figures (from Figure 12 to Figure 18) for different $R_{DS(on)}$.

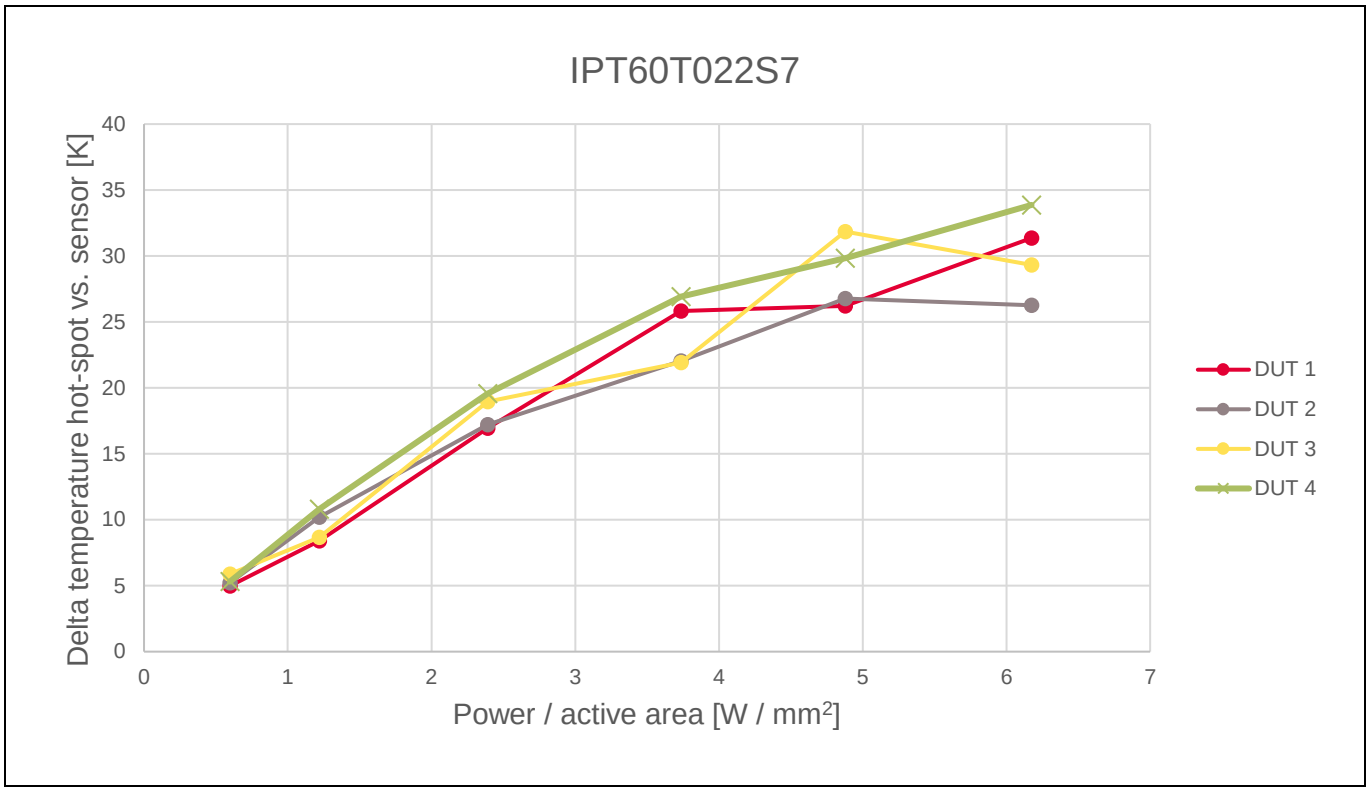


Figure 12 ΔT of hotspot vs. sensor over power per active area IPT60T022S7

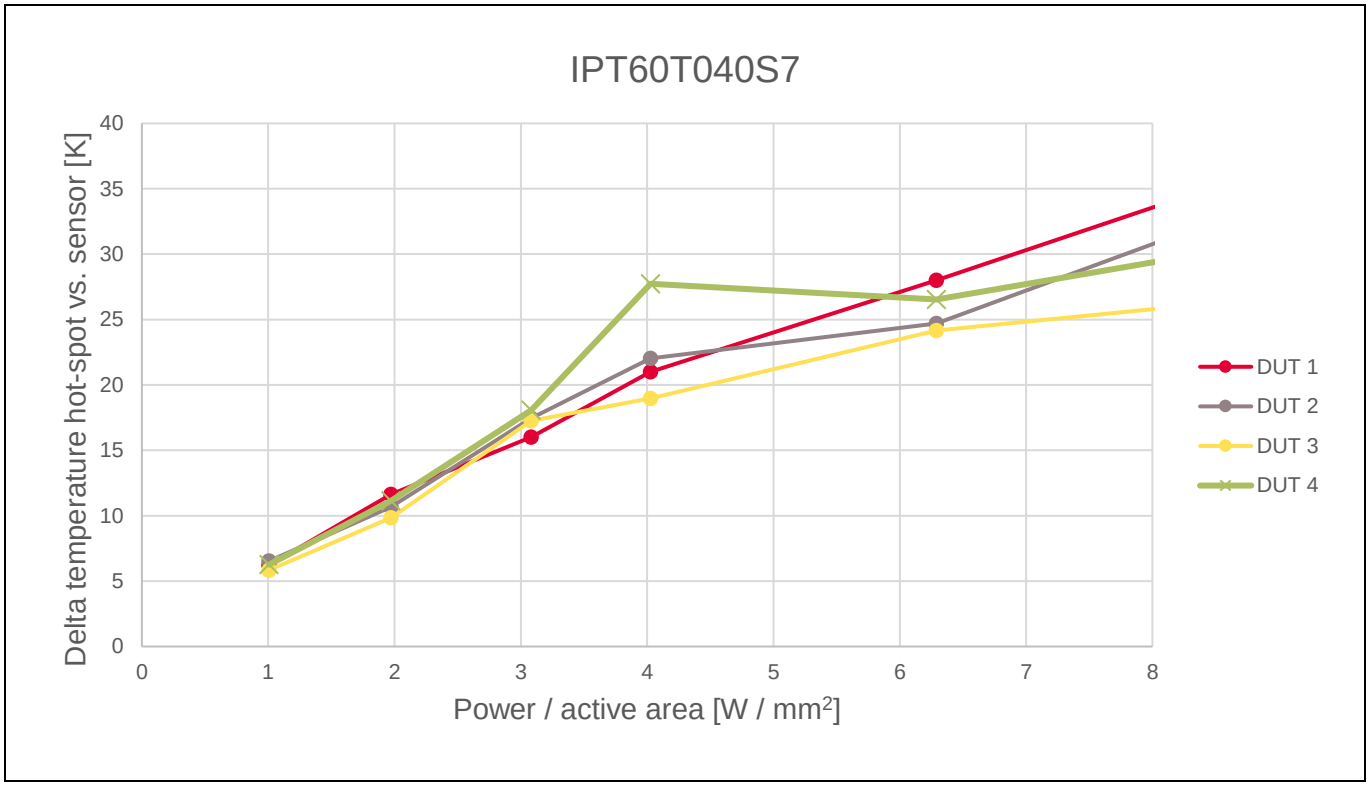


Figure 13 ΔT of hot-spot vs. sensor over power per active area IPT60T040S7

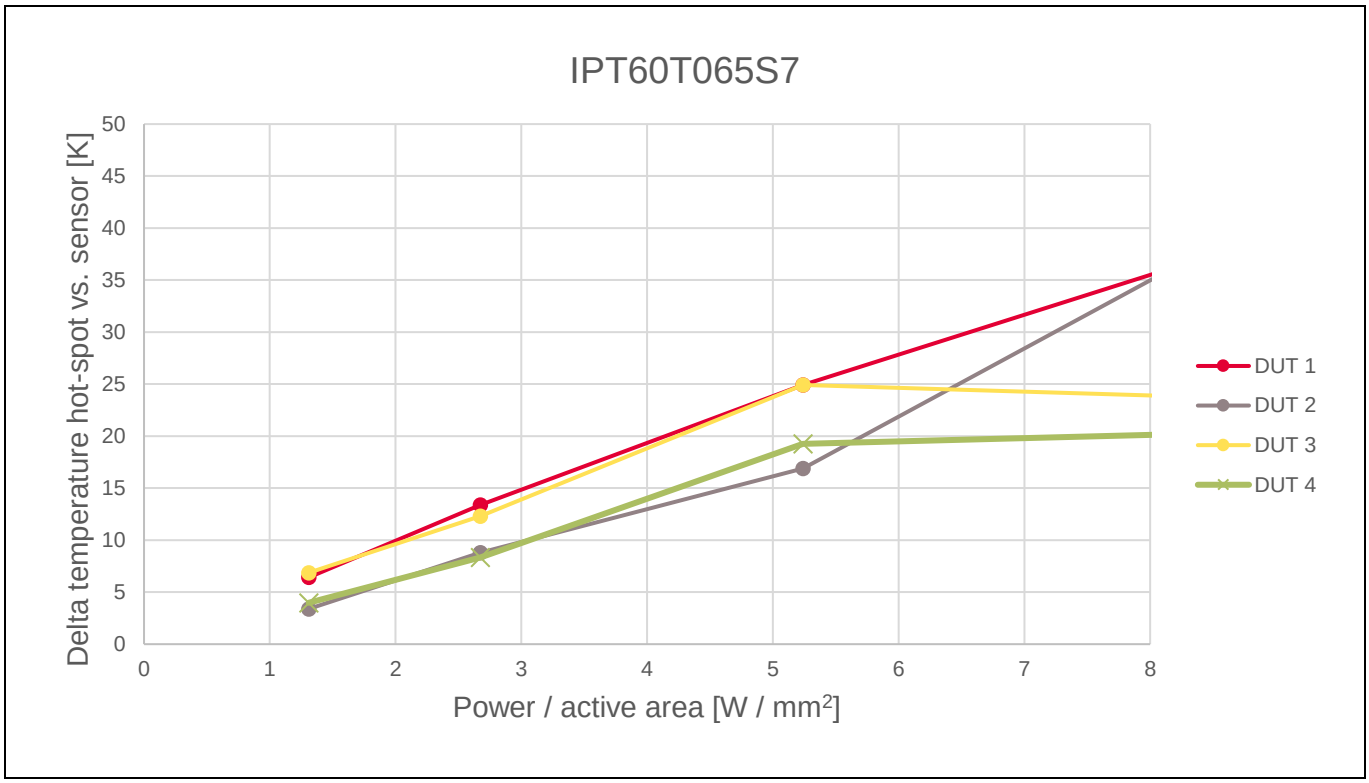


Figure 14 ΔT of hotspot vs. sensor over power per active area IPT60T065S7

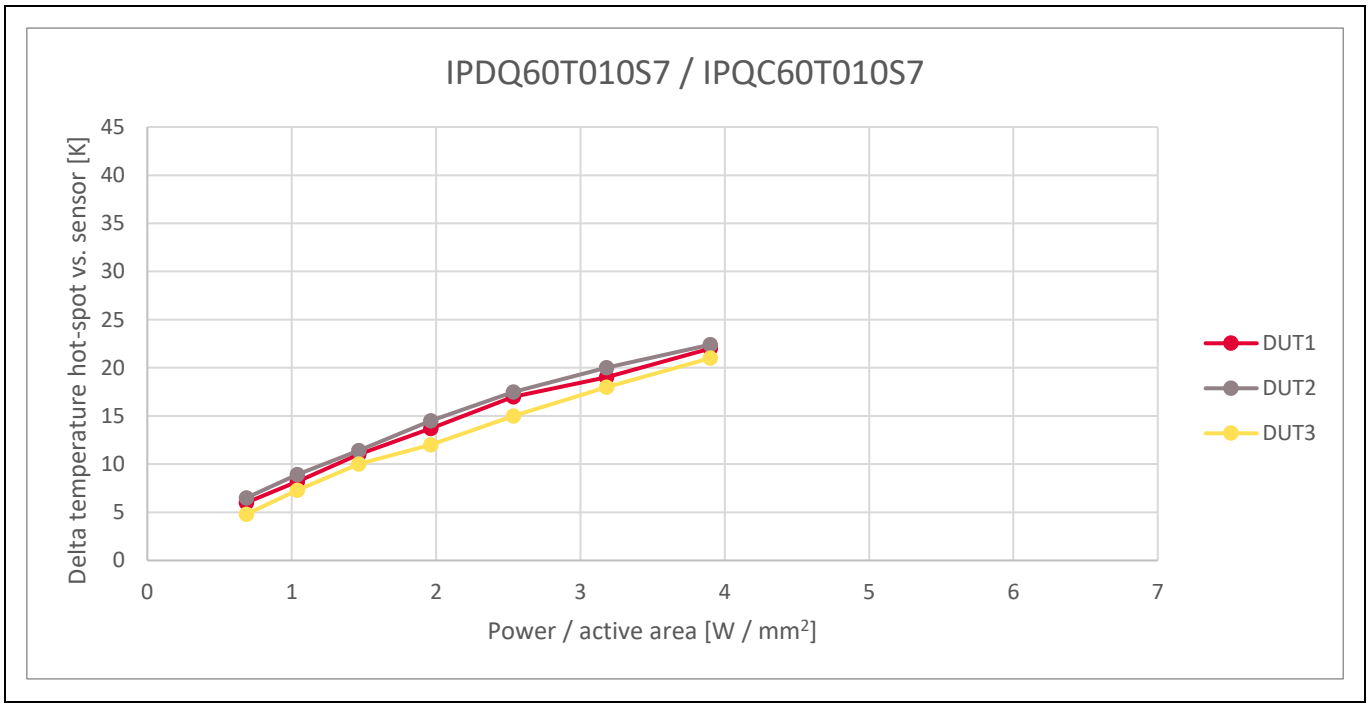


Figure 15 ΔT of hotspot vs. sensor over power per active area IPDQ60T010S7/IPQC60T010S7

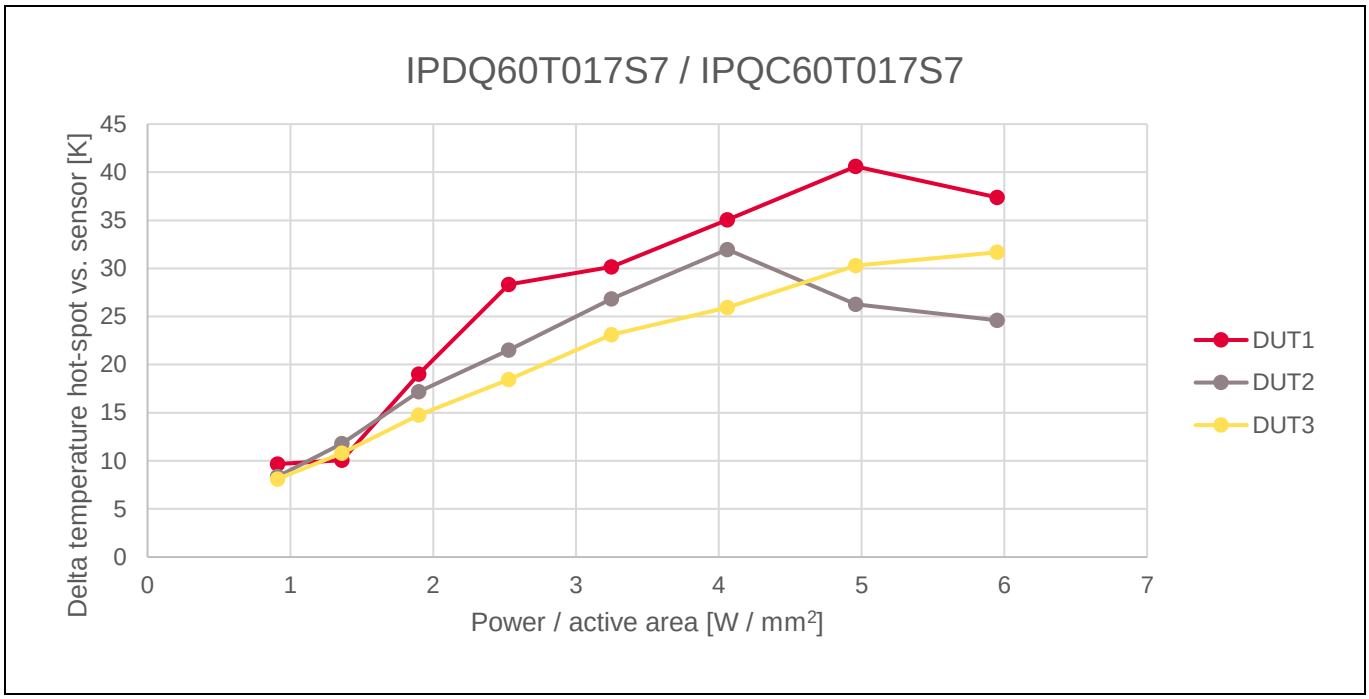


Figure 16 ΔT of hotspot vs. sensor over power per active area IPDQ60T017S7/IPQC60T017S7

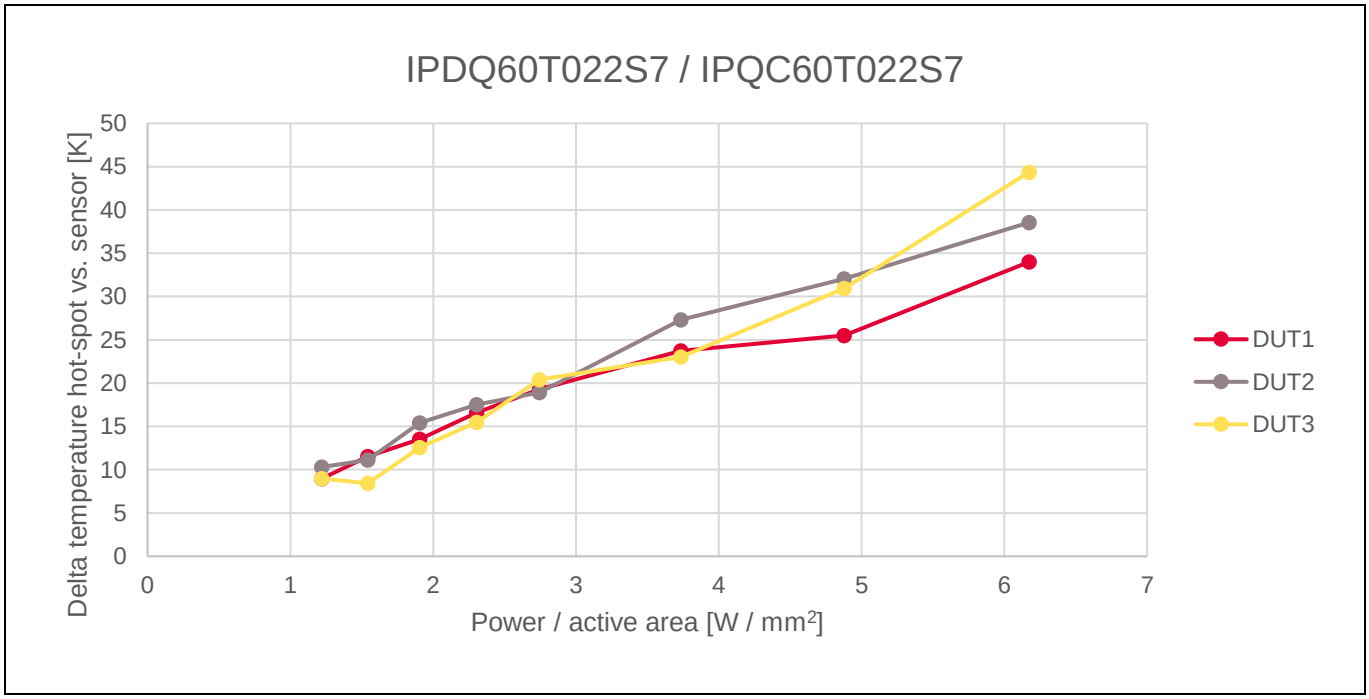


Figure 17 ΔT of hotspot vs. sensor over power per active area IPDQ60T022S7/IPQC60T022S7

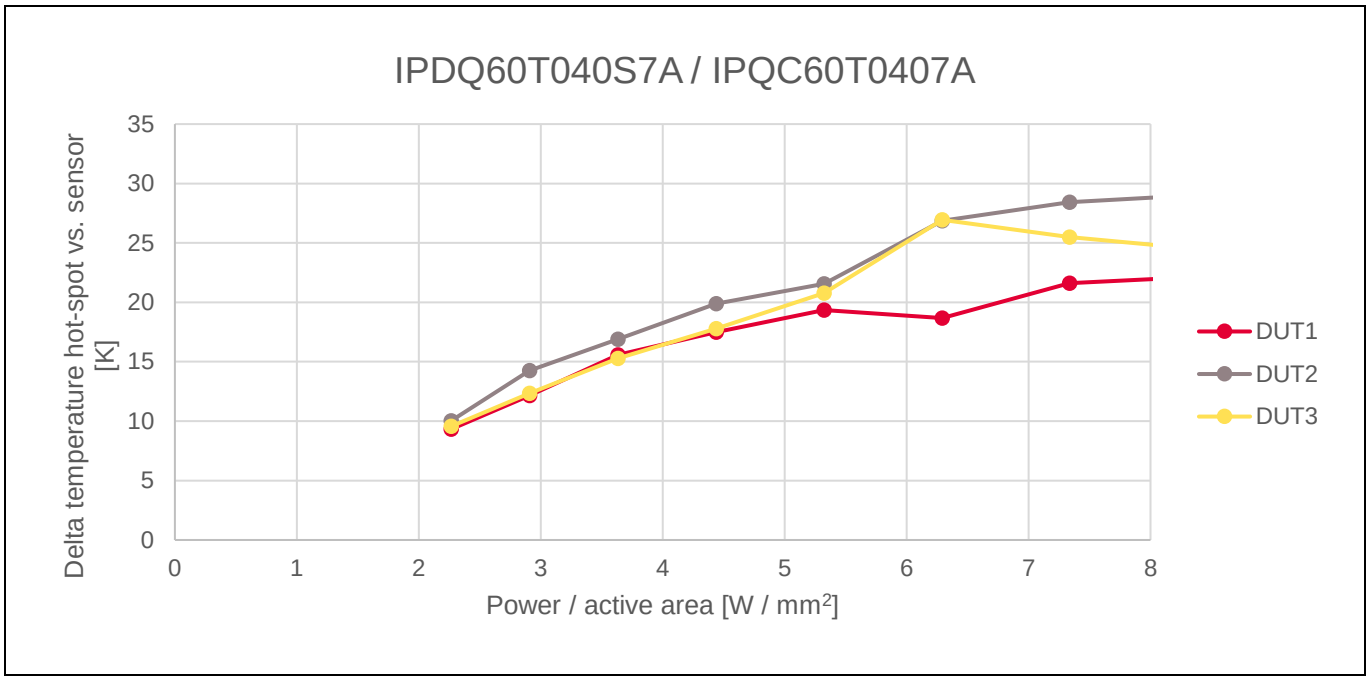


Figure 18 ΔT of hotspot vs. sensor over power per active area IPDQ60T040S7A/IPQC60T040S7A

As shown in Figure 12 to Figure 14, the higher the power per active area, the higher the difference is between the different DUTs. Nevertheless, the samples show excellent consistency and reproducibility in the typical operation range of 2-3 W/mm². Only IPT60T065S7 shows a delta in this range as well. This results from the solder differences from the package to the PCB (test board).

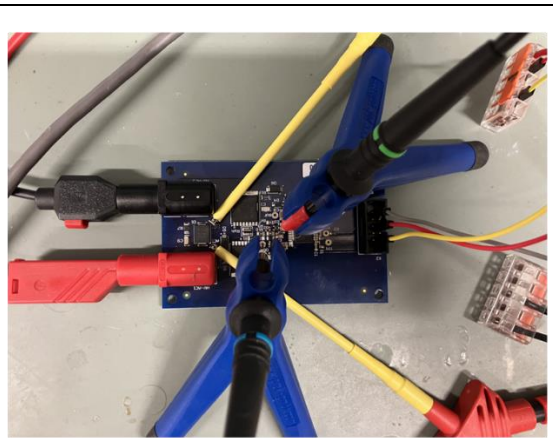
4 Application measurements

The next section shows application tests to verify the temperature sensing and product ruggedness.

4.1 Overtemperature test

This test aims to evaluate the functionality of the temperature sensor and its interaction with the gate driver to safely turn-off the devices. For this, Infineon's new gate driver iSSI30R12H is used.

The following figure shows the evaluation board and the corresponding block diagram.



– EVAL-iSSI30R12H evaluation board

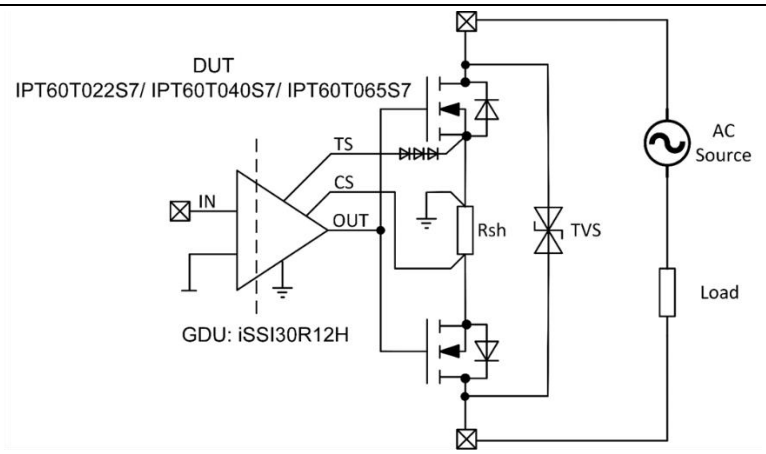


Figure 19 Overtemperature test setup

For this test, an AC signal is applied and the devices under test (DUTs) are turned on. The load forces a certain sinusoidal current to flow through the DUTs until the voltage on the TS pin reaches the defined threshold and the gate signal is removed (see Figure 20).

The load is chosen so that a slight overload condition is present, which constantly heats the device, leading to a constant drop in the measured forward voltage between the TS and ground pins over time.

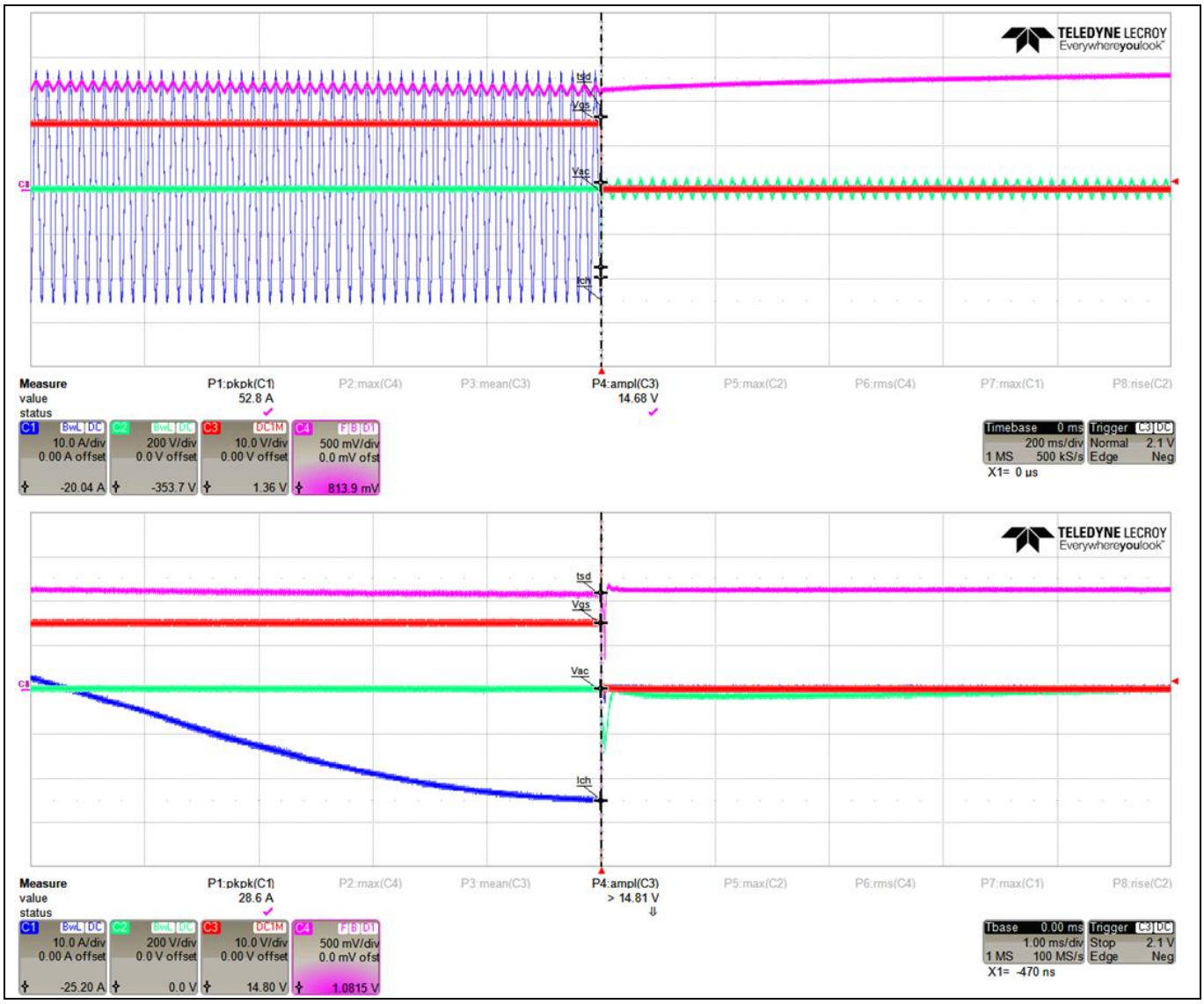


Figure 20 Waveforms overtemperature shutdown test (“magenta” TS pin voltage; “blue” drain current; “green” V_{DS}; “red” V_{GS})

Figure 20 clearly shows the shutdown of the current transfer and that the TS pin voltage is increasing as the devices are cooling down again. This test has been performed on several devices for all products and shows that temperature sensing works as an additional safety feature in all relevant applications.

4.2 Overcurrent test

This test aims to evaluate the current-switching capability of the new products. Particularly in solid-state applications, the drain current can achieve values close to the pulse current rating in the product datasheets. Therefore, it is crucial to verify if the devices are suitable for turning off these high currents safely. For this test, the earlier setup – except temperature sensing – is used. It has been performed on a number of samples for each product to ensure datasheet limits. The following figure shows this test.

As this is intended to test ruggedness, all samples have been tested up to the application requirement for solid-state solutions. For the use case described here, a 5 mΩ shunt is used and the current sense (CS) threshold limit between 185 mV and 215 mV is implemented. This leads to an overcurrent shutdown at ~40 A.

Even the lowest $R_{DS(on)}$ devices in the portfolio passed this test, which is shown in the following figure.

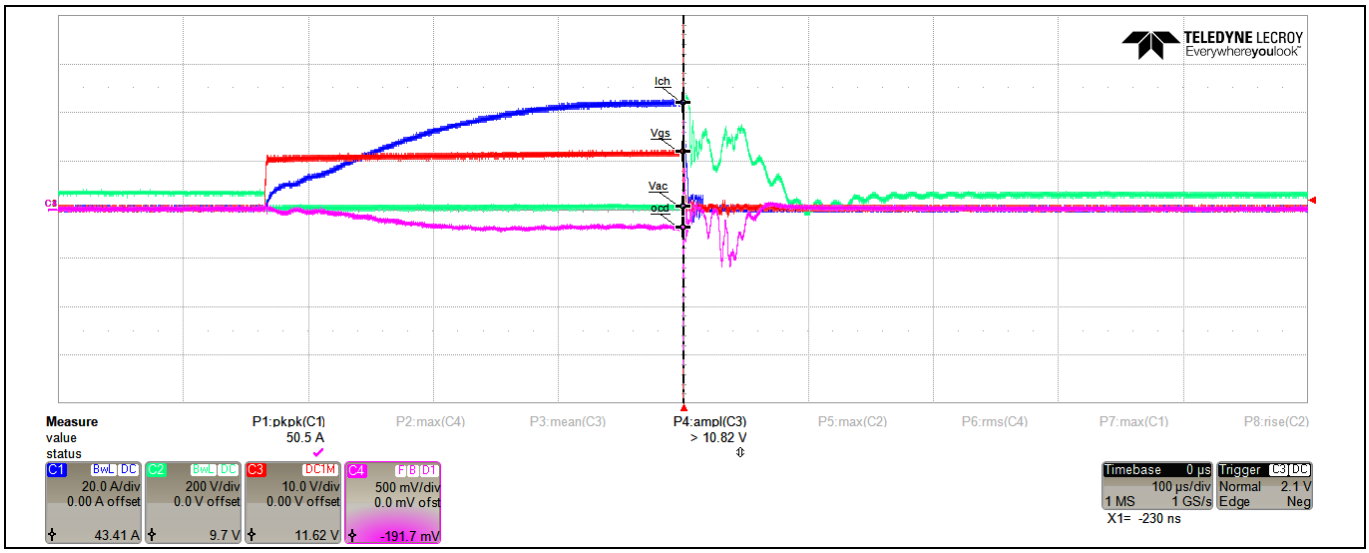


Figure 21 Overcurrent shutdown test waveforms (“magenta” CS voltage; “blue” drain current; “green” V_{DS}; “red” V_{GS})

During the high current turn-off, the devices can be seen being driven into an avalanche operation due to the inductance in the current path. During the design-in phase, it is necessary to stay below the rated avalanche characteristics. These characteristics are limited and can be found in the corresponding product datasheets.

4.3 AC-15 test

The AC-15 utilization category is described in IEC 60947-5-1 and considers a system with a nominal current of 2 A. The test uses a highly inductive load with a power factor of less than 0.3. A high inrush current, at least 10 times the nominal current, is conducting, as shown in the following figure.

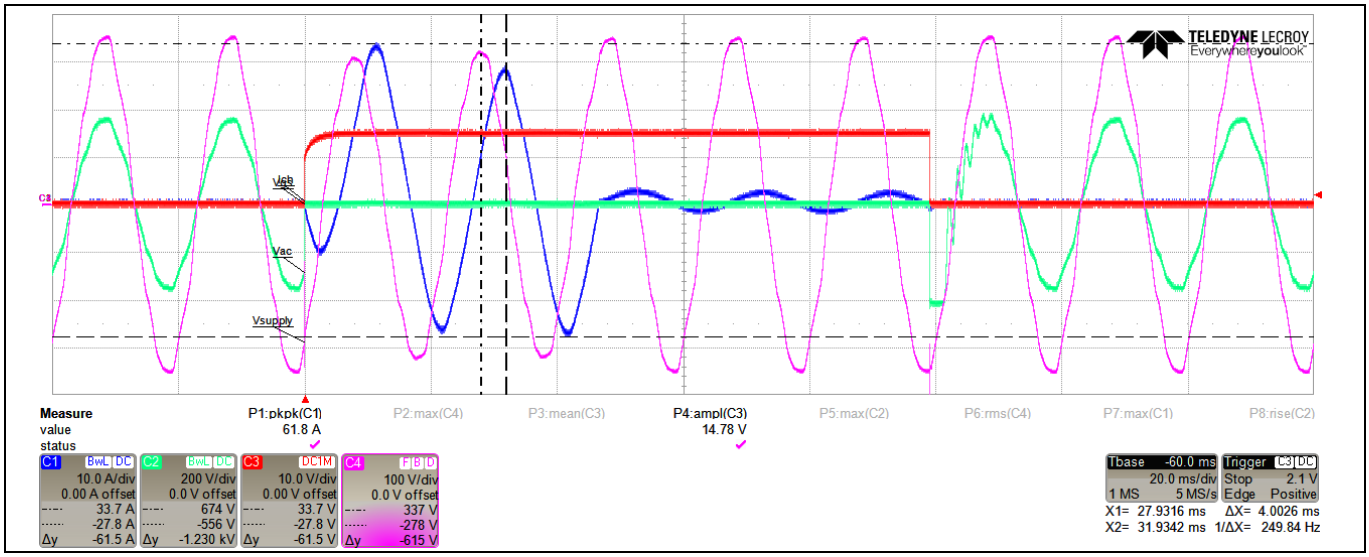


Figure 22 AC-15 test waveforms (“magenta” supply voltage; “blue” drain current; “green” V_{DS}; “red” V_{GS})

Figure 22 shows a peak inrush current of 33.7 A and a working peak current of 3.3 A. This test shows the functionality of these devices in a real application environment. All devices of all $R_{DS(on)}$ classes survived the AC-

15 test. The important safety element in this test is the TVS diode, which needs to be properly dimensioned, as a turn-off in the inrush current period can be critical and is generally recommended to use. The simplified block schematic is shown in the following figure.

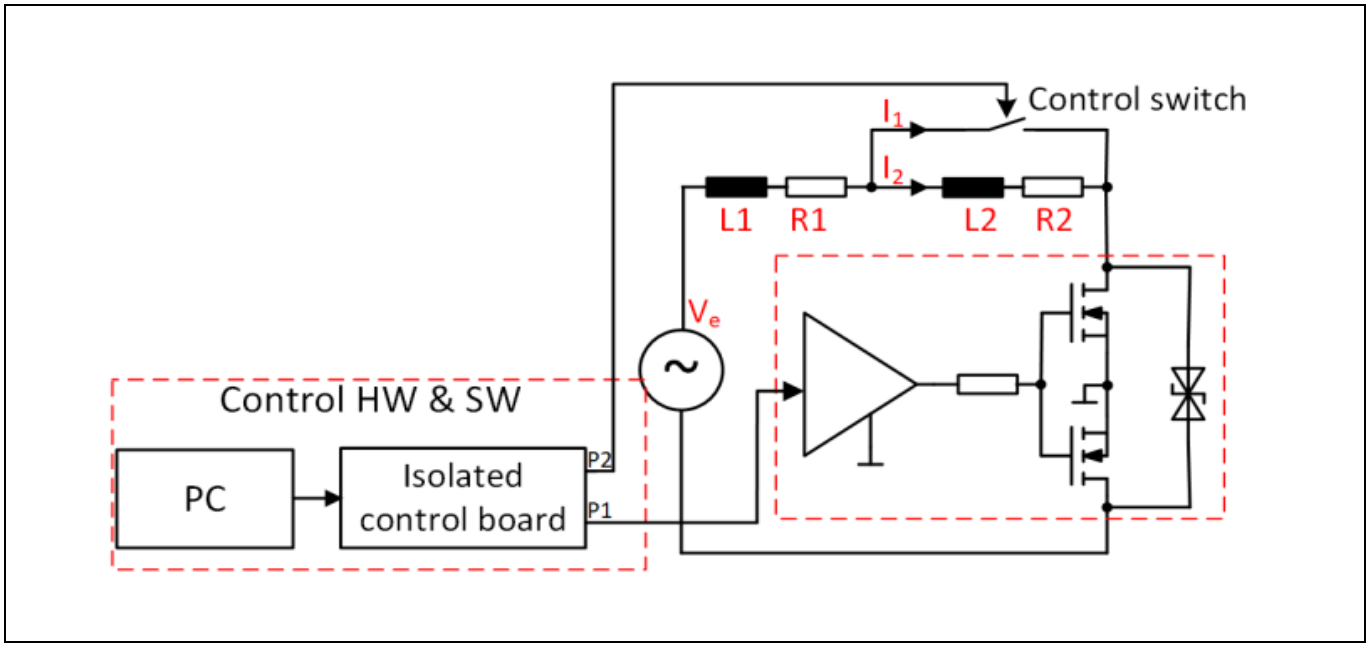


Figure 23 Block schematic of AC-15 test

5 Power cycling test

During a power cycle measurement, the DUT is heated up to a preset junction temperature of 150°C by running a constant load current through the device for a fixed time. The load pulse results in a T_j typically around the $T_{j,max}$ of the DUT. After heating up, the device is cooled down to the inlet temperature of the cooling block for a fixed time. This process is repeated until the device breaks due to the thermo-mechanical stress on the different internal materials, developing faults on the interfaces, starting from the device die attachment and wire bonds all the way to the PCB and heatsink.

As the power cycling standards are application-specific, the designer should qualify the devices based on their mission profiles and application behavior.

5.1 Test setup

To perform the measurements, the following test setup is used.

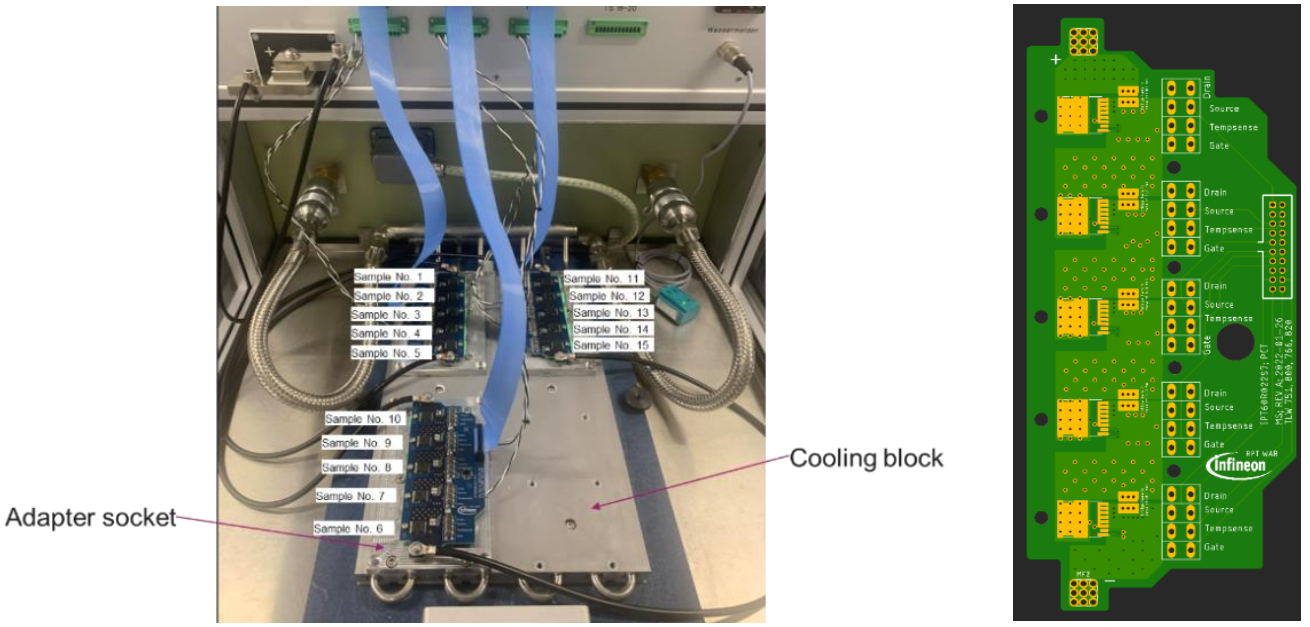


Figure 24 Test setup for power cycling test with a board for TOLL samples

The adapter PCBs contain the soldered DUTs and are supplied with the test current for heating up the samples. The samples are in a series connection. These PCBs are mounted on a cooling block, which has suitable adapter sockets to ensure a good cooling performance. Each PCB has five MOSFETs in the TOLL package, soldered in a series. The T_J is determined by measuring the calibrated temperature sense voltage of the DUT shortly after the load current is turned off. In the test setup shown in Figure 24, up to 15 samples can be measured at a time.

For devices in top-side cooling packages, the test boards are mounted upside down on the heat sink using a spring to ensure good thermal contact between the package case and the heat sink adapter. This means that for top-side-cooled devices, the heat does not need to go through the PCB and the board soldering. This significantly reduces the possibility of failure due to the degradation of the test PCB and soldering, as shown in Figure 25.

Due to the thermal stress inside the MOSFET die, the T_j and the voltage drop from drain to source change with the number of switching cycles. A modification in T_j also results in a modified thermal resistance chain from the junction to ambient (R_{thJA}). To make sure the device is still working without any thermal- stress-driven damage, the following criteria are set.

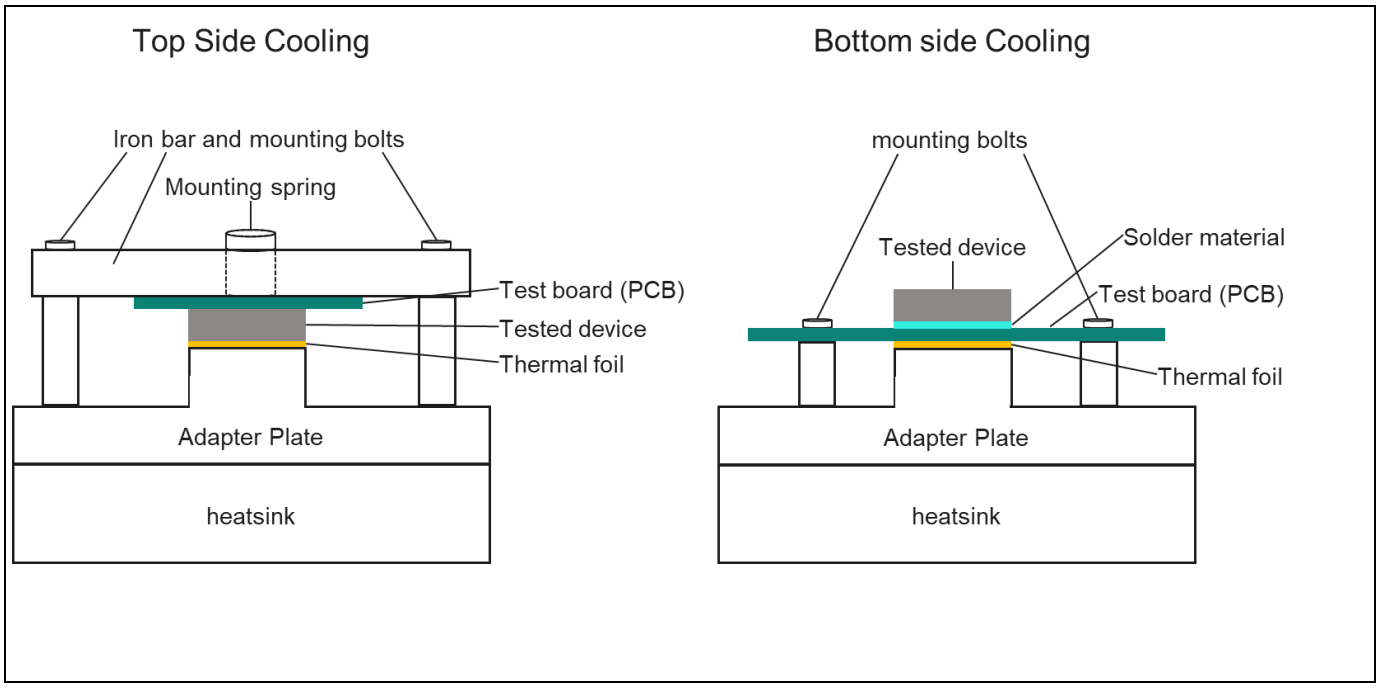


Figure 25 Test setup for power cycling: difference in thermal contact for packages with top-side and bottom-side cooling

The power cycling test promotes the deterioration of the interfaces that carry the heating current and conduct the heat away from the die. The former is monitored through the on-state voltage and the latter is monitored though the temperature difference between the junction and the heat sink.

For the test, the industry-standard end-of-life criteria for modules are adopted – the thermal resistance increases above 20 percent or a drain source voltage drop exceeds 5 percent of the initial value.

5.2 Test results

The result of this test for each product is shown the following tables. The cooling block has a constant temperature of 25°C.

Table 2 First failure after power cycling for TOLL products

Product	Stress current [A]	Average $T_{j,max}$ [°C]	First failure after [cycles]
IPT60T022S7	52	159	20,500
IPT60T040S7	36	156	32,900
IPT60T065S7	26	180	33,000

For TOLL products, all experiments had to be stopped due to the increased thermal resistance. The number of cycles to failure was unusually low for discrete devices. This prompted further investigation to identify the weak spot in the thermo-mechanical assembly of the devices.

Table 3 First failure after power cycling for QDPAK products

Product	Stress current [A]	Average $T_{j,max}$ [°C]	First failure after [cycles]
IPDQ60T010S7	121.5	155	160k
IPQC60T010S7	118	155	11k
IPDQ60T040S7	122	155	110k
IPQC60T040S7	47.3	155	45k

For QDPAK products, all experiments had to be stopped due to the increased thermal resistance. Overall, a significantly higher cycle time for a comparable stress compared to that of the TOLL products was observed. Therefore, a similar analysis to the TOLL products has been performed for the DUTs of QDPAK products.

5.3 Power cycling test strongly depending on solder interface from package to PCB or Cooling surface

After the power cycling test, the PCBs and DUTs were checked by an X-ray. For TOLL products, the X-ray images (shown in the following figure) indicate severe deterioration of the solder between the package and PCB , with extended voids from the PCB through-vias, mostly concentrated below the center of the device package.

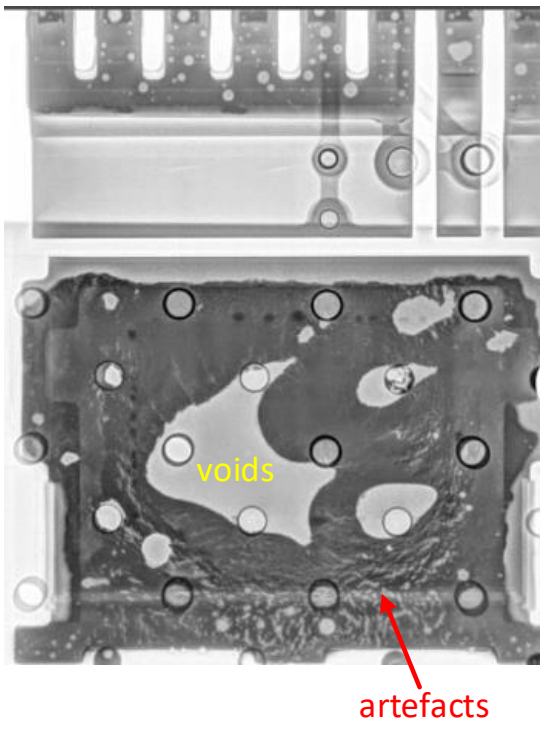


Figure 26 Artefacts in the solder between package and PCB for TOLL product

This was confirmed by a cross-section of the PCBs and DUTs, where an extended (virtually complete) delamination of the solder PCB or package layer is clearly visible. The state of the PCB solder is similar for all samples investigated.

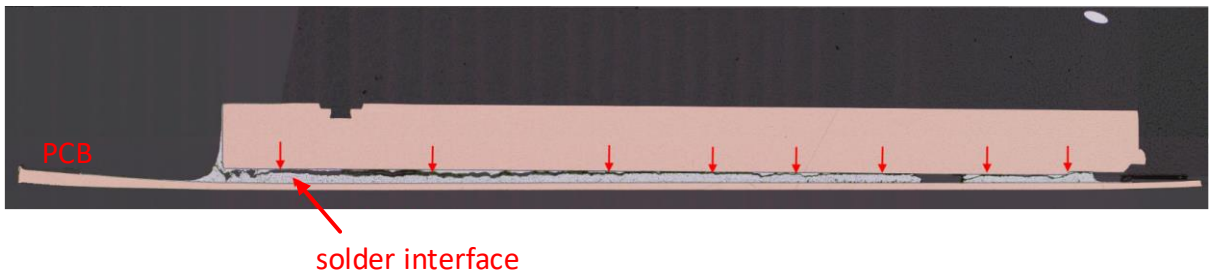


Figure 27 Cracks in solder interface between package and PCB for TOLL product

This degradation of the solder joint between the DUT and PCB is caused by different materials and their expansion coefficients. This adds stress, causing the final cracking of the interface material.

QDPAK TSC DUTs exhibited significantly higher cycles until failure. The X-ray images and ultrasound images indicated a damage to the bond wire. Unlike TOLL products, these products were directly connected to the cooling block of the setup, with their cooling bodies lacking any additional solder layer, as is necessary for the TOLL package. This has suppressed the failure mode observed for the TOLL products.

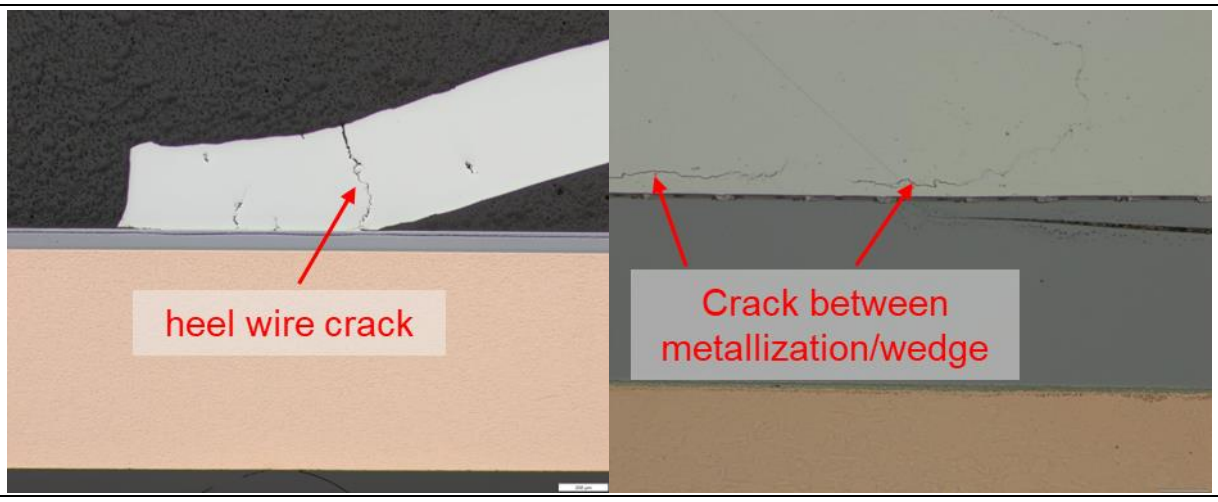


Figure 28 Cross-section of the source bond (left) and zooming in on the metallization/wedge interface for a failed IPDQ60T040S7 product

After the mechanical preparation of the samples, a heel wire crack and a beginning bond wire lift off could be detected. This is the standard failure mode expected while performing power cycling on this package.

Based on the investigation above and since all the failed DUTs of the TOLL products in the power cycling test showed artefacts in the solder connection, it is clear that the interface and the solder quality are key to achieving a high power cycle ruggedness.

If a greater power cycling ruggedness is required, it is recommended to:

- Use the blind vias below the solder pad of the package to avoid stress concentration
- Use solders with an increased resistance to metal fatigue
- Use soldering profiles that guarantee the absence of initial voids (known to promote crack inception and propagation)
- Use top-side cooled packages with a mechanical connection to the cooling body that is less prone to thermal stress compared to soldering, such as springs and screws

6 Summary

This application note explores the latest CoolMOS™ S7T family, which brings an additional protection feature – temperature sensing – that can increase safety in all target applications. It explains the differences between CoolMOS™ S7T and S7 families, including the replacement of the driver source pin with the temperature sense pin. It also discusses the delta temperature between the temperature sensor and the hotspot. Lastly, it demonstrates the application and ruggedness measurements, including how the solder joint degradation between the package and PCB is the main criteria for power cycling operations. All of this shows CoolMOS™ S7T is the ideal technology for various applications such as SSCBs, motor starters, µGrids, and power distribution units. In the near future, it will also extend to automotive applications such as eFuse and battery main switches.

Revision history

Document revision	Date	Description of changes
V 1.0	2023-11-24	Initial release
V 1.1	2024-07-01	Updated to latest released products
V 1.2	2024-07-29	Minor fixes

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