Migrating from XDP™ XDP710-002 to XDP711-001

About this document

Scope and purpose

This document provides a guide to migrate from XDP710-002 to XDP711-001 and highlighting the added features.

Intended audience

This document is intended for design engineers.

XDP™

XDP™ is a high-performance digital power controller designed to optimize the IC for the specific applications. They feature digital algorithms for high power efficiency and minimal standby power, digital parameter configuration for increased flexibility and lower development effort, and optimized bill of materials (BoM), making these controllers ideal for a range of applications such as:

- Telecom
- Datacenter and computing
- SMPS

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Safety precautions

Note: Please note the following warnings regarding the hazards associated with development systems.

Table 1 Safety precautions

	**Warning:** *The DC link potential of this board is up to 1000 VDC. When measuring voltage waveforms by oscilloscope, high voltage differential probes must be used. Failure to do so may result in personal injury or death.*
	**Warning***: The evaluation or reference board contains DC bus capacitors which take time to discharge after removal of the main supply. Before working on the drive system, wait five minutes for capacitors to discharge to safe voltage levels. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Warning:** *The evaluation or reference board is connected to the grid input during testing. Hence, high-voltage differential probes must be used when measuring voltage waveforms by oscilloscope. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Warning:** *Remove or disconnect power from the drive before you disconnect or reconnect wires, or perform maintenance work. Wait five minutes after removing power to discharge the bus capacitors. Do not attempt to service the drive until the bus capacitors have discharged to zero. Failure to do so may result in personal injury or death.*
	**Caution:** *The heat sink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.*
	**Caution:** *Only personnel familiar with the drive, power electronics and associated machinery should plan, install, commission and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.*
	**Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	**Caution:** *A drive that is incorrectly applied or installed can lead to component damage or reduction in product lifetime. Wiring or application errors such as undersizing the motor, supplying an incorrect or inadequate AC supply, or excessive ambient temperatures may result in system malfunction.*
	**Caution:** *The evaluation or reference board is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials that are unnecessary for system installation may result in overheating or abnormal operating conditions.*

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1 Introduction

The XDP™ XDP711-001 power controller is the latest addition to the XDP™ digital hot-swap family with several other new features and improvements compared to XDP710-002. These additional features require an update in the register map and effect the portability of XDP710-002 settings to XDP711-001. The following features have been added into XDP711-001:

- Hybrid mode to detect OUV fault either via FB pin or V_{OUT} telemetry
- Surge immunity feature
- AMON (IMON and PMON)
- VDS fault detection
- Increased power averaging
- Peaks and valley detection independent of averaging
- Configurable input overvoltage hysteresis
- Restart via GPIO pin
- Extended energy register

The following sections discuss the updated register map, explains the updated features, and outlines the hardware modifications required.

Table 2 Acronyms/abbreviations

Acronym	Description
AADM	Analog Assisted Digital mode
ACM	Analog Comparator mode
ADC	analog-to-digital converter
BW	bandwidth
DCM	Digital Comparator mode
FDM	Fully Digital mode
GND	Ground
OUC	output undercurrent
OUV	output undervoltage
POR	power on reset

2 PMBus commands comparison

Table 3 summarizes the differences in PMBus commands between XDP710-002 and XDP711-001.

Table 3 PMBus command structure differences between XDP710-002 and XDP711-001

PMBus command	Address	XDP710-002	XDP711-001
VOUT_UV_FAULT_LIMIT	0x44	Default value = 0x0000	Default value = 0x00E8
STATUS_MFR_SPECIFIC	0x80	Bits 7 – 4 are reserved	Introduced VDS_FAULT in bit 4, which indicates if a VDS fault has occurred
MFR_MODEL	0x9A	0x0000303137504458	0x0000313137504458
MFR_REVISION	0x9B	0x0001	0x0003
MODE	0x7F	Bit 7 is reserved FETs list is shown in Table 20	Introduced **FB_COMP_SEL** in bit 7 FETs list in **FET_SELECT** bit field has been updated according to Table 20
V_SNS_CFG	0xD4	Bits 14 – 10 are reserved	Introduced **VDS_FAULT_LIMIT** bits in position 14:13 and **VIN_OV_HYST** bits in position 12:10. Default value of the command is now 0x0428 since default value of **VIN_OV_HYST** is 0x1
I_SNS_OFFSET	0xD6	Bits 11 – 15 are reserved	**I_SOA_REG_OFFSET** is used to add an offset into the control loop to reduce the target regulation current at startup without effecting the telemetry
WATCHDOG_TMR	0xD8	Size of command is 8 bits	Size has been increased to 16 bits in order to introduce **SURGE_REC_WATCHDOG**[2:0] field in bits 10 – 8
GPO_CFG	0xDB	GPO2 can be configured as general purpose or CGDN by means of **GPO2_CFG** bit field	GPO2 can be configured as general purpose, CGDN, or RESTARTN by means of **GPO2_CFG** bit field
ENABLE_FAULTS, MASK_FAULTS, STATUS_FAULTS	0xDE, 0xDF, 0xE0	Bit 15 is reserved	Introduced VDS bit in position 15 to enable, mask, and monitor **VDS** fault. Default value of ENABLE_FAULTS and MASK_FAULTS is now 0xBEFF
RETRY	0xE7	Bit 14 is GATE_REC_EN	**SRG_PROT_EN** replaces **GATE_REC_EN** in bit position 14, which enables or disables the surge protection feature Default value of the register is now 0x3FBF
TELEMETRY_AVG	0xE9	Bits 11 – 10 are reserved P_TELEMETRY_AVG bit field is 3 bits	AMON_SEL has been introduced in position 11 and AMON_EN in

PMBus commands comparison

PMBus command	Address	XDP710-002	XDP711-001
			position 10. Command has been renamed as TELEMETRY_CFG. P_TELEMETRY_AVG has been enlarged to 4 bits
CONFIG_ID	0xFA	Non-existent	The CONFIG_ID command provides you the option to store an identification number in order to distinguish among the devices with different configurations in the system
READ_EIN_EXT	0xFB	Non-existent	For details, see Extended energy counter

3 XDP711-001 features

3.1 Hybrid mode setting for output undervoltage fault detection

When the device is operated in Digital Comparator Mode (DCM) i.e., no resistors are installed on the MODE pins, and MODE bit (Command code: **0xD1**, Command name: **MODE**, Bits: **MODE[6]**) is set high, the detection of OUV fault can be modified to be either analog based (i.e., via FB pin) or digital based (i.e., via VOUT telemetry).

This behavior can be selected via FB_COMP_SEL (Command code: **0xD1**, Command name: **MODE**, Bits: **FB_COMP_SEL[7]**) as described in Table 4.

Table 4 FB_COMP_SEL under command 0xD1: MODE

FB_COMP_SEL [7]	Description
0x0	OUV fault digital detection
0x1	OUV fault analog detection

Table 5 Output undervoltage fault detection method criteria

Mode Pins (MODE0 and MODE1)	MODE [6] under command 0xD1: MODE	FB_COMP_SEL [7] under command 0xD1: MODE	OUV fault detection criteria
Resistance to GND	x	x	ANALOG
Open	1: Digital Comparator Mode (DCM)	0	DIGITAL
Open	1: Digital Comparator Mode (DCM)	1	ANALOG
Open	0: Analog Comparator Mode (ACM)	x	ANALOG

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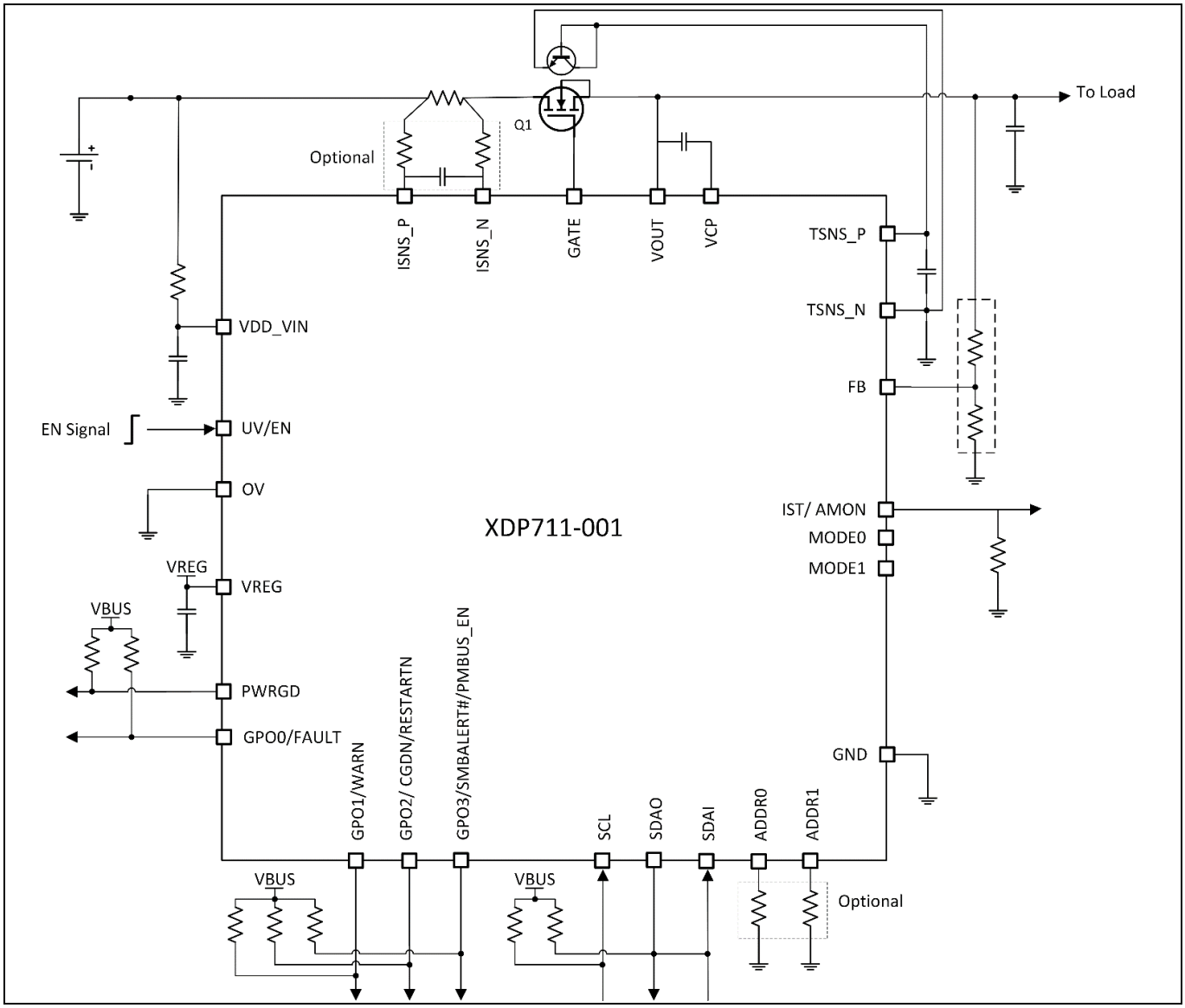


Figure 1 XDP711-001 Hybrid mode

3.2 Surge immunity protection

The surge immunity feature is added to XDP711-001 to protect the system from false tripping against the disturbances caused due to high input voltage transients. These high input voltage spikes, which are essentially fast dV/dt, result in high inrush current while charging the output capacitor on the positive peaks. This high inrush current is false detected as a short-circuit event and results in tripping of the system.

Figure 2 shows a typical scenario where the two rails have been supplied via the same 48 V backplane. In this case, the POWER_RAIL_1 experiences a short-circuit, which then gets isolated by the hot-swap controller.

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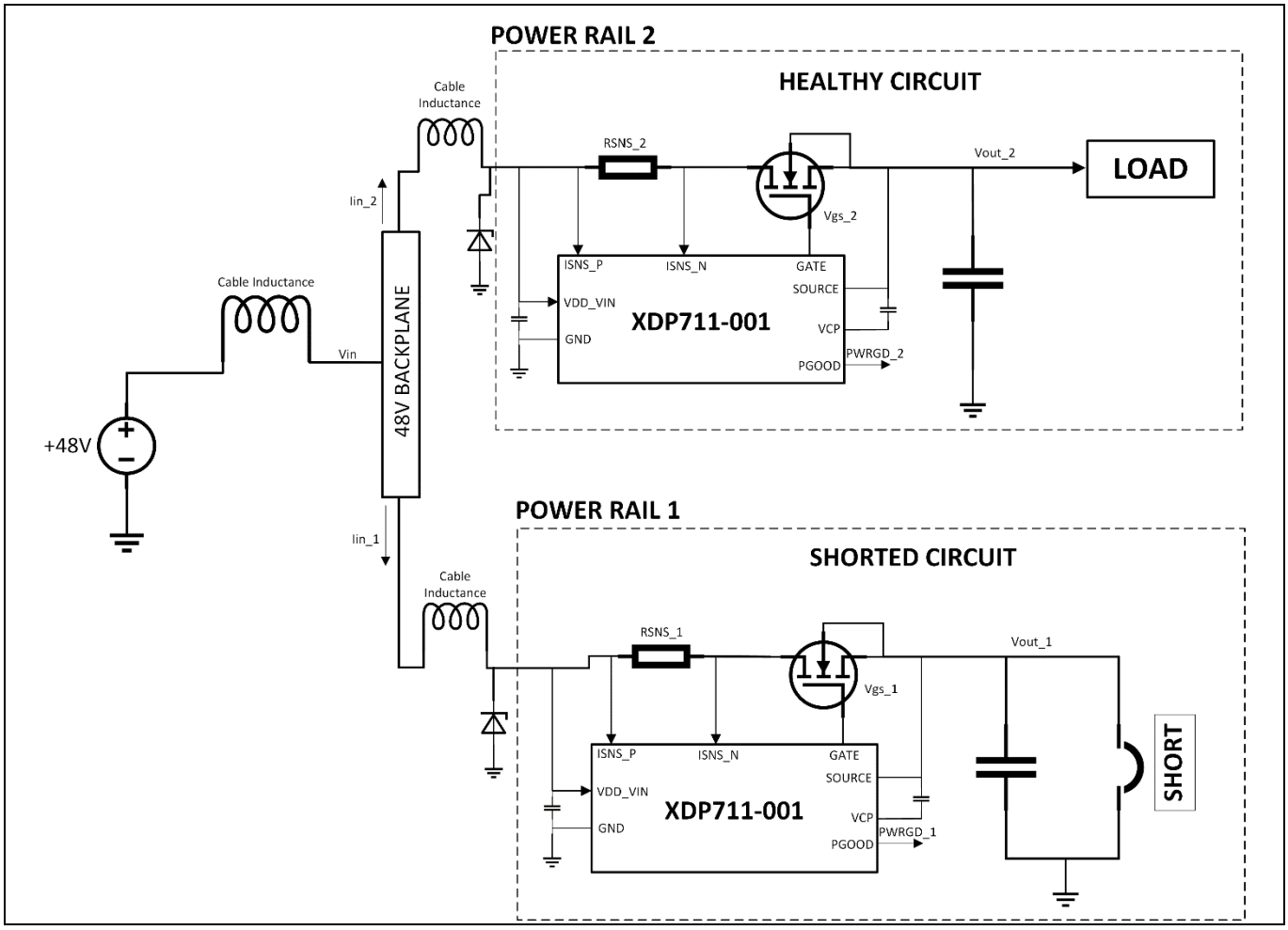


Figure 2 Typical application scenario of surge voltage generation

When the short-circuit event is isolated by the hot-swap controller, the gate is pulled down with a maximum pull-down strength of 1.5 A resulting in the current in the shorted rail to go from a high to a low value in a short period of time. This high di/dt of current induces a high input voltage spike due to cable inductance. The high dV/dt spike then results in charging the capacitor of the HEALTHY BUS (POWER_RAIL_2) and for a brief period of time, the current in POWER_RAIL_2 goes to a very high value, which gets detected as a short-circuit current and results in tripping the HEALTHY BUS. Figure 3 shows this scenario where the voltage spike induced a short-circuit in POWER_RAIL_1 trip the POWER_RAIL_2.

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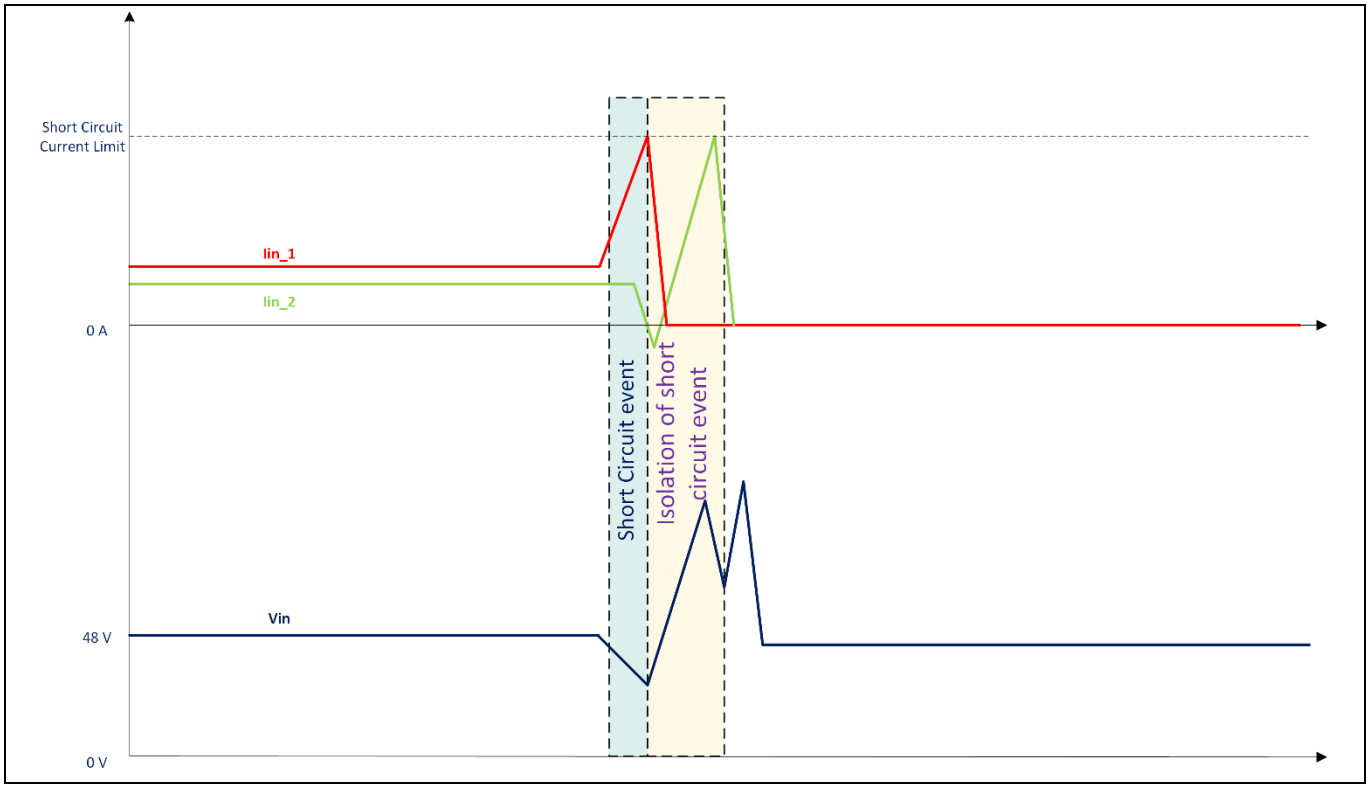


Figure 3 Tripping of POWER_RAIL_2 (HEALTHY BUS) due to short-circuit in POWER_RAIL_1

In XDP711-001, when the surge immunity feature is enabled (Command Code: **0xE7**, Command Name: **RETRY**, Bits: **SRG_PROT_EN [14]**) and upon detection of a surge, the controller follows the surge immunity protection procedure by going into SURGE, GREC1, and GREC2 states consecutively.

Table 6 SURGE_PROT_EN under command 0xE7: RETRY

SRG_PROT_EN[14]	Description
0x0 (0 bin)	Surge protection disabled
0x1 (1 bin)	Surge protection enabled

Note: This has replaced the GATE_FAST_RECOVERY feature of XDP710-002 in XDP711-001.

Surge detection

When the voltage on the current sense shunt measured at ISNS_x pins exceeds the programmed SOC fault level (Command code: **0xD5**, Command name: **I_SNS_CFG**, Bits: **SOC_FAULT_LIMIT [5:3]**), the **SOC_DG_TMR** (Command code: **0xE5**, Command name: **SOA_TMR**, Bits: **SOC_DG_TMR [10:9]**) starts running and the de-glitch timer is added to ignore the high frequency noise spikes. If the current stays above the SOC level for the programmed SOC_DG_TMR, then the controller enters into the **SURGE** state.

Note:

1. *If the surge immunity feature is disabled, the SOC fault is determined based on both SOC_DG_TMR and SOC_TMR (Command code: **0xE5**, Command name: **SOA_TMR**, Bits: **SOC_TMR [8:6]**) but when surge immunity is enabled then the SOC fault is determined only based on SOC_DG_TMR, the SOC_TMR is ignored.*

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2. *The power good signal is not de-asserted on the detection of a surge event.*

Surge state

After the SOC condition is detected, the controller enters into the SURGE state where the FET is pulled down using a strong 1.5 A pull-down current irrespective of what is configured in GATE_FAST_PD (Command code: **0xE6**, Command name: **TURN_OFF_CTRL**, Bits: **GATE_FAST_PD [0]**).

Note: 1.5 A is the maximum capability of the switch inside the controller. The pull-down strength can be adjusted by adding a resistor in the GATE or SOURCE path to the controller.

The gate is pulled low for 15 µs in this state and then enters into the GREC1 (GATE_RECOVERY_1) state. At this point, the SOC fault is not declared and the power good signal stays unchanged.

GREC1 state

In the GREC1 state, the programmed SURGE_REC_WATCHDOG_TMR (Command code: **0xD8**, Command name: **WATCHDOG_TMR**, Bits: **SURGE_REC_WD [10:8]**) shown in Table 7 starts and the gate voltage is ramped up with a 15 mA at V_{GS} = 0 V (calculation for gate charging current is shown in Equation 2) to bring the gate voltage above the FET's turn-on threshold. The controller stays in the GREC1 state until the following conditions are met to transition into the GREC2 (GATE_RECOVERY_2) state and the gate strong pull-up is stopped:

- The voltage drop across the current sense resistor reaches 12.5 mV level (if CS_RNG is 12.5 mV or 25 mV) or 25 mV level (if CS_RNG is 50 mV or 100 mV level)
- Or FET is fully enhanced i.e., V_{DS} < 1 V and V_{GS} > 7.8 V, happens when the FET current is very low (when output is already close to Vin and supplying no load current).

If SURGE_REC_WATCHDOG_TMR[2:0] expires before the above conditions are met, it triggers a WATCHDOG fault and transitions to FAULT state. This will de-assert the power good signal and assert the FAULT signal.

Table 7 SURGE_REC_WD under command 0xD8: WATCHDOG_TMR

SURGE_REC_WD[10:8]	Description
0x0 (000 bin)	Timer set by WATCHDOG (Command code: **0xD8**, Command name: **WATCHDOG_TMR**, Bits: **WATCHDOG[3:0]**)
0x1 (001 bin)	1 ms
0x2 (010 bin)	2 ms
0x3 (011 bin)	5 ms
0x4 (100 bin)	10 ms
0x5 (101 bin)	20 ms
0x6 (110 bin)	50 ms
0x7 (111 bin)	100 ms

Note: Ensure that the total gate charge from 0 V to the FETs gate threshold voltage ($V_{GS(th)}$) is around 20 µs. This is done to slow down the recovery of the gate voltage to avoid current spikes and have a controlled recovery. Thus, the total gate capacitance (C_{GATE_Total}) is calculated using Equation 1.

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$$C_{GATE_{Total}}(nF) = 20\mu s \times \frac{i\ (mA)}{V_{GS(th)}}$$

Equation 1 **C_{GATE_Total} calculations**

Where, i = gate charging current and is dependent on the gate to source voltage and is calculated by Equation 2:

$$\text{i} = i_{max}(mA) - \frac{(1.33 \times V_{GS(th)})}{2}$$

Equation 2 **Gate charging current calculation**

Where i_{max}= 15 mA

If C_{GATE_Total} is greater than the total FET gate capacitance (C_{FET}) then additional capacitor (C_{GS}) in between GATE and SOURCE is required which is calculated using Equation 3 and is shown in Equation 4:

$$C_{GS} = C_{GATE_Total} - C_{FET}$$

Equation 3 **C_{GS} calculation**

Where C_{FET} is the total FET's gate capacitance. In case FETs are placed in parallel, the capacitances must be summed as shown in Equation 4:

$$C_{FET} = n \times C_{iss}$$

Equation 4 **C_{FET} calculation**

This 15 mA of gate current is supplied by populating a capacitor between the pins VCP and VOUT as shown in Equation 3 and must be 10 times the total gate capacitance (C_{GATE_Total}) of the connected FETs as shown in Equation 5:

$$C_{VCP} = 10 \times C_{GATE_Total}$$

Equation 5 **C_{VCP} calculation**

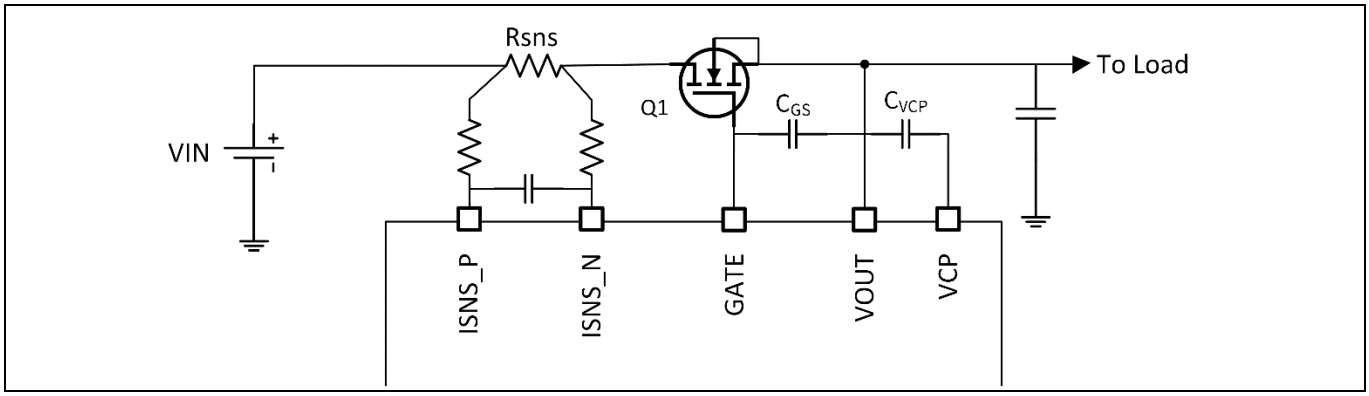


Figure 4 **Capacitor connections for surge immunity**

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Example:

- **FET:** ISC035N10NM5LF2
- **Number of FETs:** 4
- **$V_{GS(th)}$** = 3.1 V
- **FETs gate capacitance (C_{iss})** = 5500 pF

Using Equation 1, Equation 2, Equation 3, Equation 4, and Equation 5, the values of C_{GS} and C_{VCP} can be determined:

$$i = i_{max}(mA) - \frac{(1.33 \times V_{GS(th)})}{2} = 15\ mA - \frac{(1.33 \times 3.1V)}{2} = 12.93\ mA$$

$$C_{GATE_{Total}}(nF) = 20\ \mu s \times \frac{i\ (mA)}{V_{GS(th)}} = 20\ \mu s \times \frac{12.93\ mA}{3.1\ V} = 83.44\ nF$$

$$C_{FET} = n \times C_{iss} = 4 \times 5500\ pF = 22000\ pF = 22\ nF$$

$$C_{GS} = C_{GATE_Total} - C_{iss} = 83.44\ nF - 22\ nF = 61.44\ nF$$

$$C_{VCP} = 10 \times C_{FET} = 10 \times 83.44\ nF = 834.4\ nF$$

GREC2 state:

In GREC2 state, the controller enters into a regulation phase where the current is regulated at the programmed overcurrent level. If the current does not reach the OC level then the FET will be turned on without regulation. The output capacitor is charged continuously and when FET gets enhanced, i.e., V_{DS} < 1 V and V_{GS} > 7.8 V, then the controller transitions into ON state where the gate voltage continues rising to its maximum value and SURGE_REC_WATCHDOG_TMR is reset.

If at any point in GREC2 state the VDS voltage exceeds the 5.5 V level, the SOC fault is declared and the FET is turned off and fault response is based on the RETRY fault setting.

If the system fails to recover i.e., FET is not fully enhanced before the SURGE_REC_WATCHDOG_TMR expires, then the controller triggers a WATCHDOG fault and transitions to FAULT state. This will de-assert the power good signal and assert the FAULT signal.

*Note: Both SOC fault (Command code: **0xDE**, Command name: **ENABLE_FAULTS**, Bits: **SOC [4]**) and Surge Immunity Protection (Command Code: **0xE7**, Command Name: **RETRY**, Bits: **SRG_PROT_EN [14]**) needs to be enabled for the controller to follow the surge protection feature. If surge immunity protection feature is disabled, the controller follows the SOC fault procedure as is done in case of XDP710-002.*

Figure 5 shows the recovery process of POWER_RAIL_1 in the event of short-circuit when surge immunity protection is enabled. After the SOC_DG_TMR de-glitch, the SOC fault is detected and the system enters into the surge state by pulling the gate low with fast pull-down and stays in this state for 15 µs. Then, it enters into the GREC1 state where the SURGE_REC_WATCHDOG_TMR is initiated and the gate is ramped up with 15 mA at V_{GS} = 0 current source sourced from the capacitor placed between the VCP and SOURCE pin of the XDP711-001 controller. Once the voltage drop on the current sense resistor exceeds the 12.5 mV level for CS_RNG of 12.5 mV/25 mV or the level of 25 mV for CS_RNG of 50 mV/100 mV, it transitions into the GREC2 state. In the GREC2 state, VDS voltage is detected as greater than 5.5 V and the system enters into a FAULT state and declaring it as SOC FAULT and PWRGD signals is de-asserted.

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Figure 6 shows the recovery process of POWER_RAIL_2 in the event of surge induced from RAIL_1 when surge immunity protection is enabled. It follows the same steps as that of the POWER_RAIL_1 recovery but since this system is not shorted and VDS voltage stays below 5.5 V level in GREC2 state, the system successfully recovers before the SURGE_REC_WATCHDOG_TMR expires and the controller transitions to ON state without issuing any fault or de-asserting the PWRGD signal.

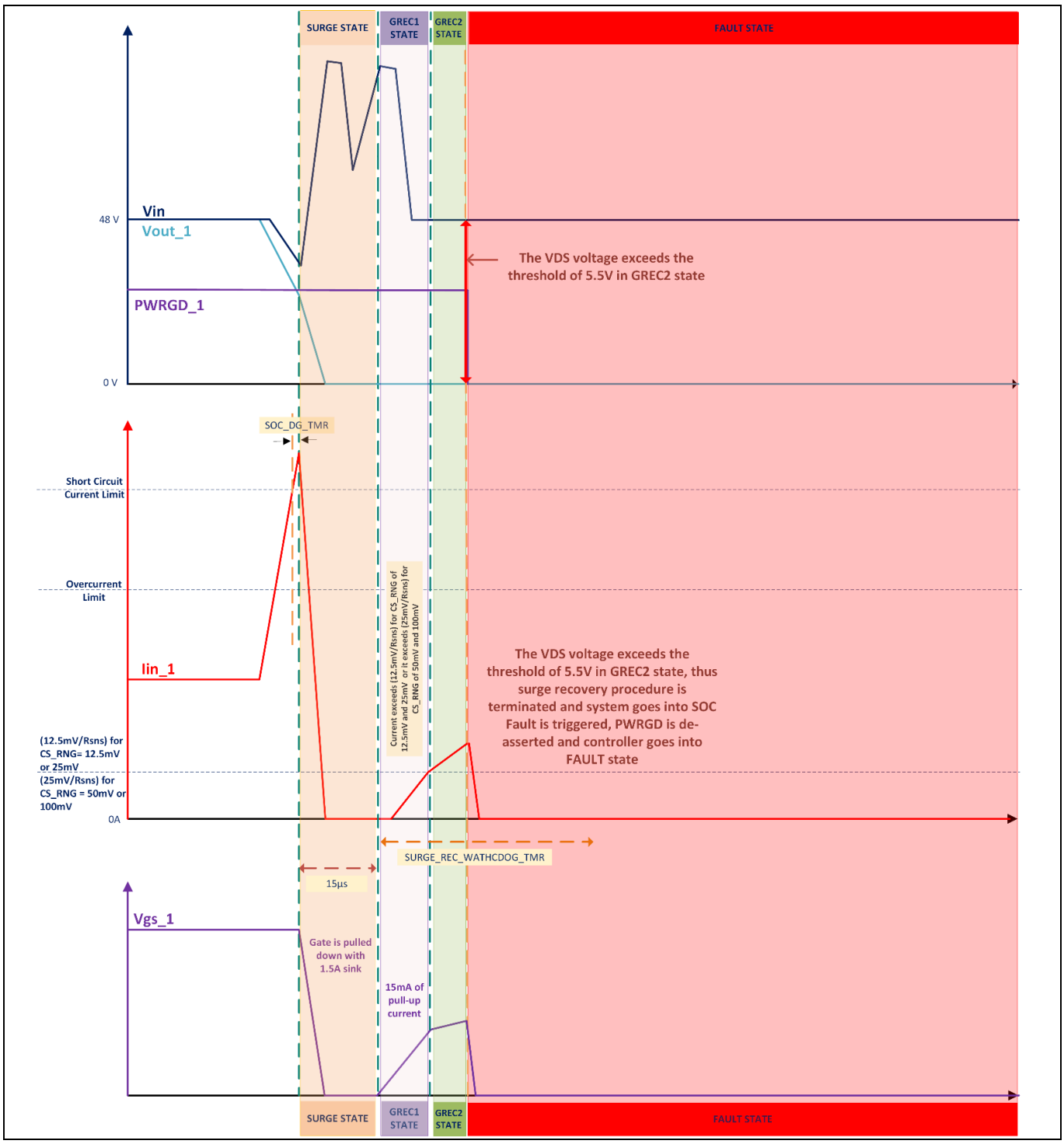


Figure 5 Surge recovery process for shorted POWER_RAIL_1

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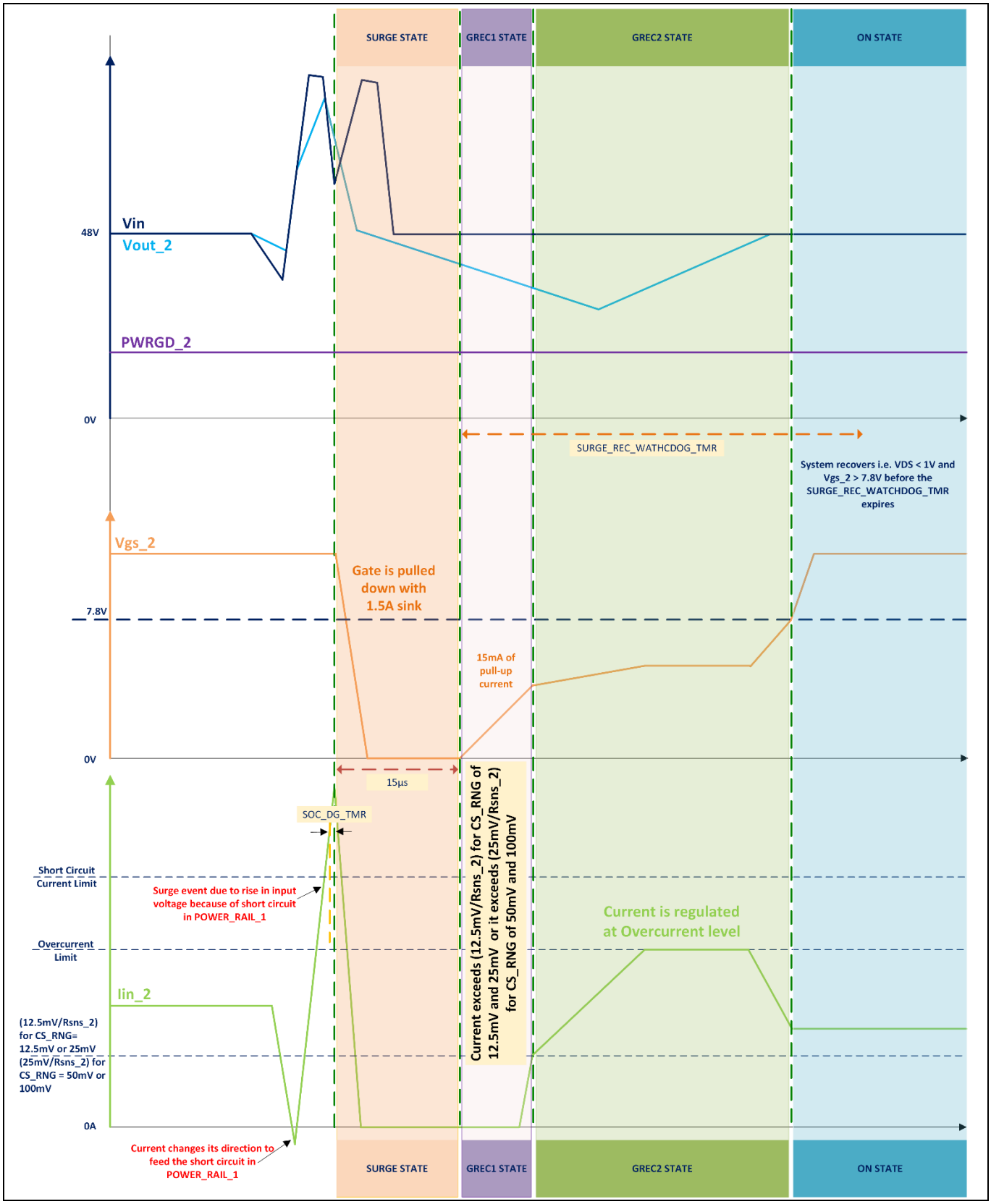


Figure 6 Surge recovery process for POWER_RAIL_2 tripped due to a voltage surge

3.2.1 Surge immunity design example

The surge immunity feature is tested on a 4kW design making use of 4x IPM018N10NM5LF2 FETs with 2.2 mF load capacitance and 50 mV CS_RNG. The overcurrent for this design is set to 100 A and the severe overcurrent level is set at 150 A with a 200 ns de-glitch.

The POWER RAIL 1 circuit is used to create a short circuit, which creates a surge in POWER RAIL 2 causing it to detect this surge as a short circuit. Then, by utilizing the surge immunity algorithm, the POWER RAIL 1 is recovered without any power interruption to downstream load. Figure 7 shows that the test setup to create a surge.

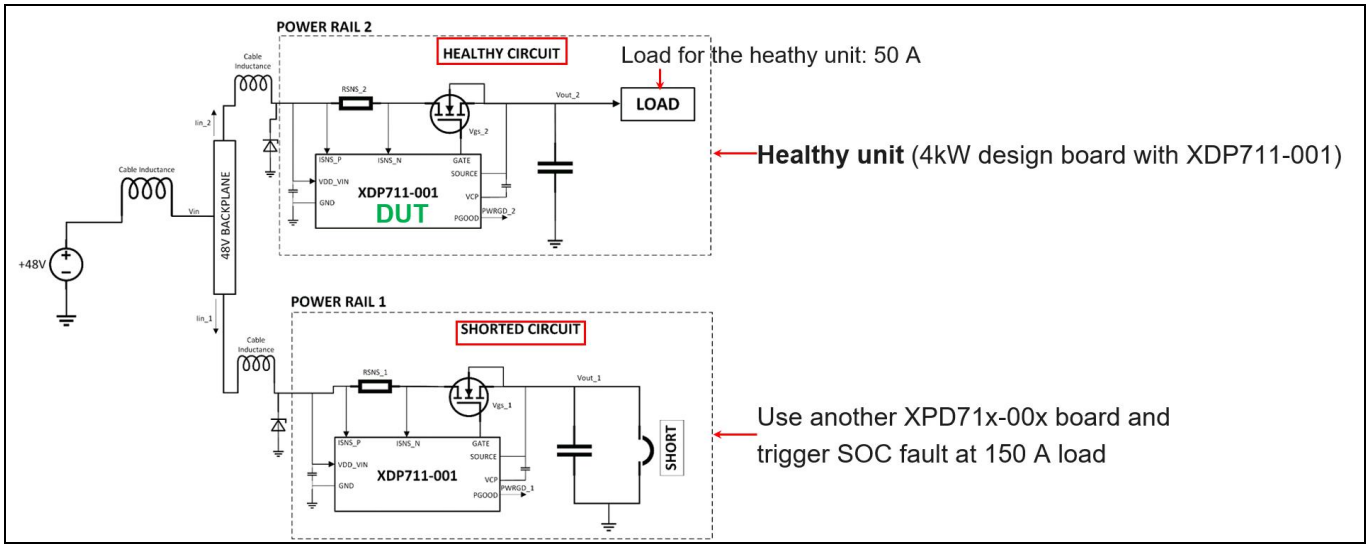


Figure 7 Surge immunity test setup

It can be observed from Figure 8 that after the POWER RAIL 2 is switched off, the input voltage sees a surge in the input voltage, which results in increasing the input current sensed turning off the GATE of the POWER RAIL 1 as it is detected as a short circuit. On close observation, it can be seen that PWRGD and FAULT signal remains high, which indicates that surge immunity procedure has been initiated.

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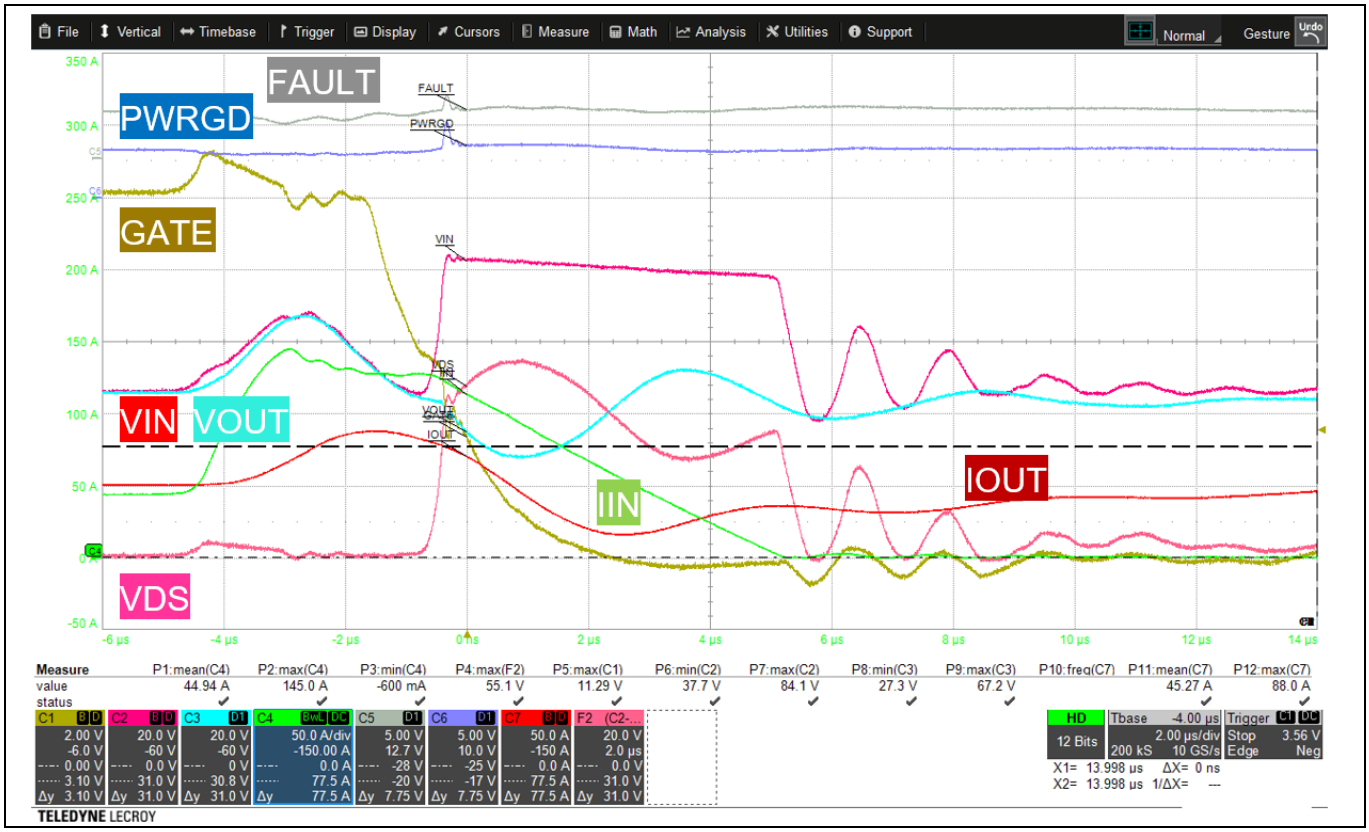


Figure 8 Voltage surge added to POWER RAIL 1

Figure 9, shows the first phase of surge immunity procedure where the GATE is pulled low for 15 µs and then, the startup sequence is initiated in GREC1 phase where is the GATE is pulled up to turn on the FET as fast as possible.

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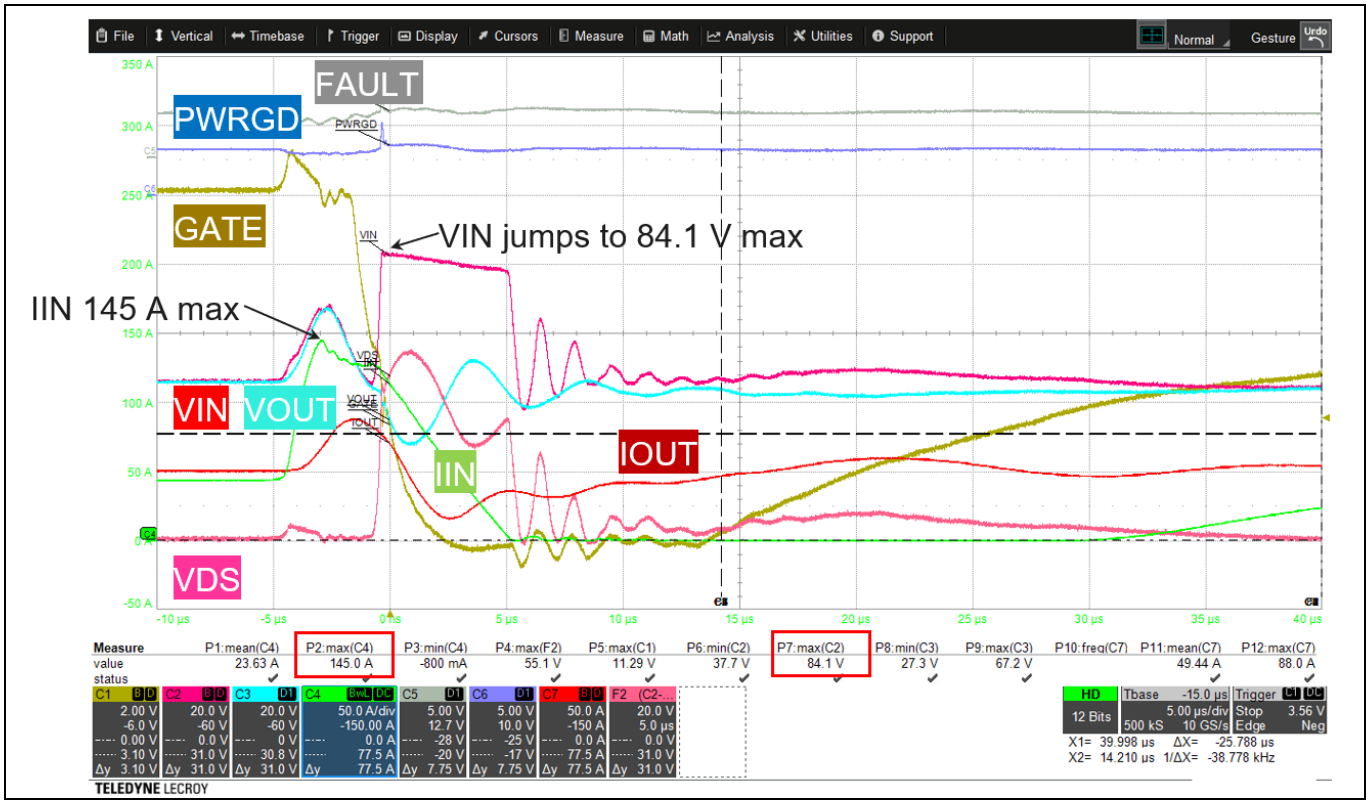


Figure 9 SURGE state

Figure 10 shows the surge recovery procedure; in this case, the input current stays below the 25 mV level i.e., 125 A, thus the GREC2 state is not achieved and recovery happens only in GREC1 state, and the gate is recovered to 7.8 V by utilizing the gate charge from the capacitor connected between VCP and VOUT pin and then, it utilizes internal charge pump of 248 µA to charge the gate all way up.

The recovery is achieved in less than 90 µs without the loss of voltage to output and without triggering the surge recovery watchdog timer, which is programmed to 2 Ms. The green waveform shows the input current during recovery and no high inrush current pulses can be observed during the recovery.

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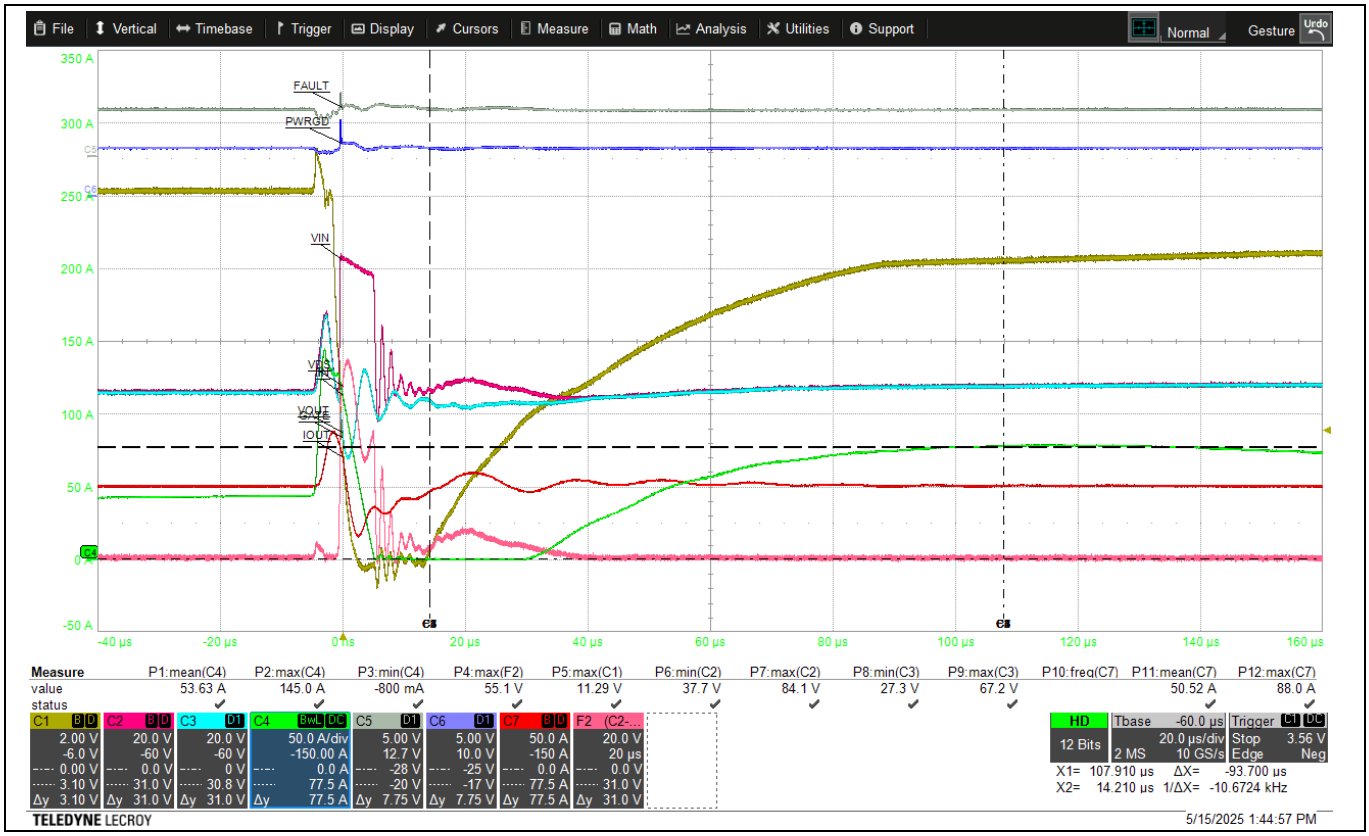


Figure 10 SURGE recovery state (GREC1)

Figure 11 shows the whole recovery process of the POWER RAIL 1 from the surge event and it can be observed that POWER RAIL 1 recovered without any interruption to the output.

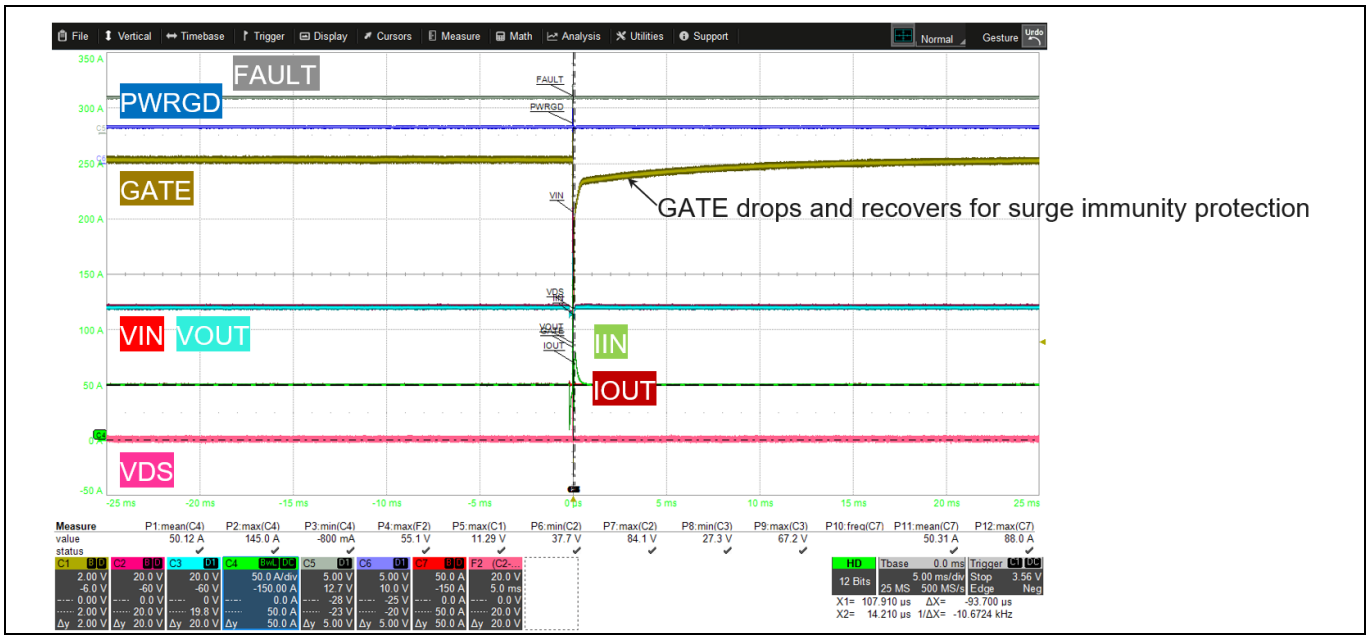


Figure 11 SURGE immunity

3.3 AMON (IMON and PMON)

In XDP711-001, analog monitoring and reporting (AMON) of FET current (IMON), or input power (PMON) signal can be output at the IST pin.

The AMON functionality can be enabled using AMON _EN (Command code: **0xE9**, Command name: **TELEMETRY_CFG,** Bits: **AMON_EN[10]**) and the desired IMON or PMON can be selected at the IST pin via AMON_SEL (Command code: **0xE9**, Command name: **TELEMETRY_CFG,** Bits: **AMON_SEL[11]**).

Table 8 AMON_EN under command 0xE9: TELEMETRY_CFG

AMON_EN (Bit: 10)	Description
0x0 (0 bin)	AMON is disabled
0x1 (1 bin)	AMON is enabled

Table 9 AMON_SEL under command 0xE9: TELEMETRY_CFG

AMON_SEL (Bit: 11)	Description
0x0 (0 bin)	Analog current is reported (IMON)
0x1 (1 bin)	Analog power is reported (PMON)

As shown in Figure 12, the information is taken from IOUT data path and PIN data output, which goes into a digital multiplexer (1), configurable by means of AMON_SEL. Output of the multiplexer then goes to an IDAC (2), which outputs a current level proportional to the corresponding current or power digital input at the IST pin. This current is converted to voltage by placing an external R_{AMON} resistor between the IST pin and GND.

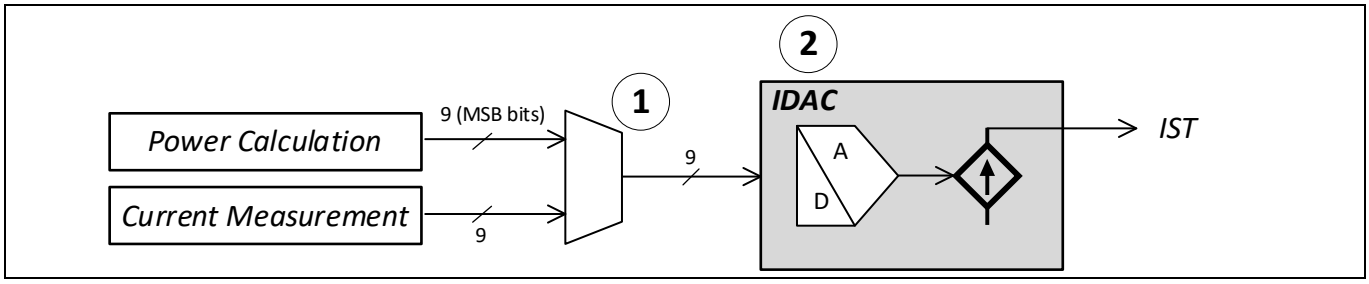


Figure 12 AMON generation

To reduce the noise, it is recommended to add an output RC low pass filter with a bandwidth (BW) of 80-100 kHz at the IST pin. C_{MON} can be calculated as per Equation 6.

$$C_{AMON}(nF) = \frac{1000}{2 \times \pi \times BW(kHz) \times R_{AMON}(k\Omega)}$$

Equation 6 C_{AMON} calculations

The maximum current that can be sourced out of the AMON pin is 2 mA, which corresponds to the maximum current or power that can be detected by the controller. Additionally, the functional maximum voltage that the AMON can sustain is 5.5 V. Hence, the resistor that will be used to translate the current to voltage needs to be sized accordingly.

Perform the following steps to calculate current from AMON pin when selected as IMON signal:

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1. Identify the CS_RNG (Command code: **0xD5**, Command name: **I_SNS_CFG,** Bits: **CS_RNG[7:6]**) as shown in Table 10

Table 10 CS_RNG under command 0xD5: I_SNS_CFG

CS_RNG[7:6]	Description
0x0 (00 bin)	12.5 mV
0x1 (01 bin)	25 mV
0x2 (10 bin)	50 mV
0x3 (11 bin)	100 mV

2. Note the value of Rsns that has been populated on the board or equivalent Rsns and call it as R_{eqv}
3. Calculate the gain of the IMON signal as follows:

$$G_{IMON} = \frac{2\ (in\ mA)}{\frac{CS_{RNG}(in\ mV)}{R_{eqv}(in\ m\Omega)}} \times R_{AMON}\ (in\ k\Omega)$$

Equation 7 G_{IMON} calculation

4. Calculate the final current as:

$$Current\ (A) = \frac{V_{IMON}}{G_{IMON}}$$

Equation 8 Current calculation from IMON signal

Consider the following example for calculation of current from IMON signal:

- CS_RNG = 25 mV
- R_{eqv} = 0.3 mΩ
- R_{AMON} = 2 kΩ
- V_{IMON} = 2.75 V

$$G_{IMON} = \frac{2\times0.3\times2}{25} = 0.048$$

$$Current\ (A) = \frac{2.75}{0.048} = 57.291\ A$$

Perform the following steps to calculate current from AMON pin when selected as PMON signal:

1. Identify the CS_RNG (Command code: **0xD5**, Command name: **I_SNS_CFG,** Bits: **CS_RNG[7:6]**) as shown in Table 10
2. Identify the VTLM_RNG (Command code: **0xD4**, Command name: **V_SNS_CFG,** Bits: **VTLM_RNG[1:0]**)

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Table 11 VTLM_RNG under command 0xD4: V_SNS_CFG

VTLM_RNG [1:0]	Description
0x0 (00 bin)	88 V
0x1 (01 bin)	44 V
0x2 (10 bin)	22 V

3. Note the value of Rsns that has been populated on the board or equivalent Rsns and call it as R_{eqv}
4. Calculate the gain of the PMON signal as follows:

$$G_{PMON} = \frac{2\ (in\ mA)}{\frac{CS_{RNG}(in\ mV)}{R_{eqv}(in\ m\Omega)} \times VTLM_RNG(in\ V)} \times\ R_{AMON}\ (in\ k\Omega)$$

Equation 9 G_{PMON} calculation

5. Calculate the final power as:

$$Power\ (W) = \frac{V_{PMON}}{G_{PMON}}$$

Equation 10 Power calculation from PMPN signal

Consider the following example for calculation of power from PMON signal:

- CS_RNG = 25 mV
- VTLM_RNG = 88 V
- R_{eqv} = 0.3 mΩ
- R_{AMON} = 2 kΩ
- V_{IMON} = 1.5 V

$$G_{PMON} = \frac{2 \times 0.3 \times 2}{25 \times 88} = 0.000545$$

$$Power\ (W) = \frac{1.5}{0.000545} = 2750W$$

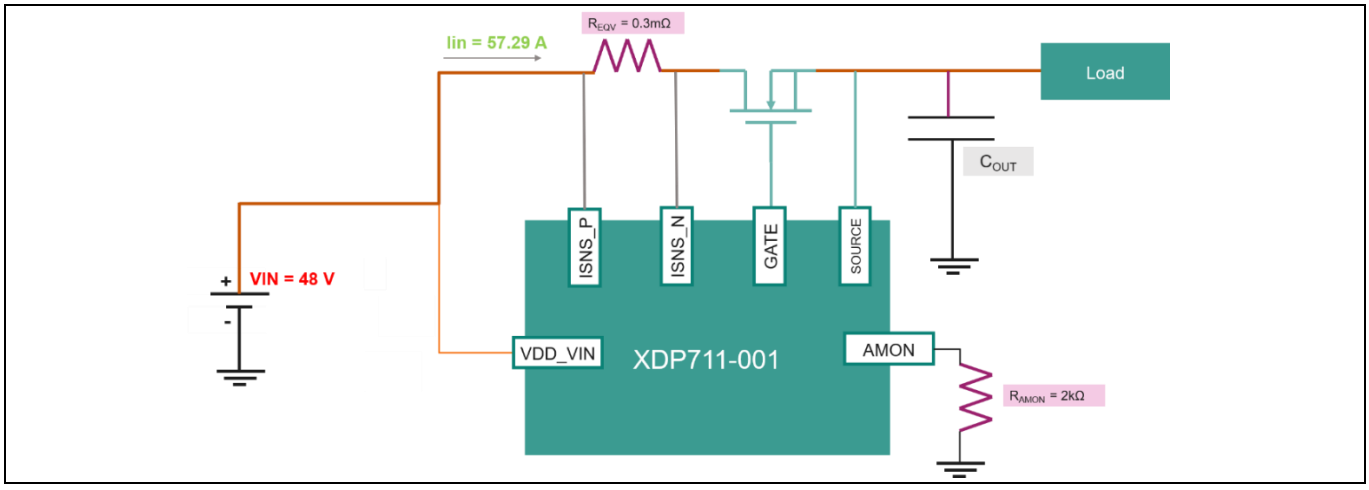


Figure 13 AMON pin connection example

3.4 Pre-charged output voltage (VDS) fault detection

VDS fault protection feature has been added to XDP711-001 to detect the pre-charged output due to shorted FET or some other factors in STANDBY state after the POR (power on reset) or after issuing a RESTART command.

VDS fault is enabled by VDS bit (Command code: **0xDE**, Command name: **ENABLE_FAULTS,** Bits: **VDS[15]**) and in STANDBY state, after EN_DG timer (Command code: **0xD8**, Command name: **WATCHDOG_TMR,** Bits: **EN_DG[7:4])** has expired for the first time after power-up. The VDS of the FET is measured digitally at pins VOUT and ISNS_P pin and, if it exceeds the limit programmed in VDS_FAULT_LIMIT (Command code: **0xD4**, Command name: **V_SNS_CFG,** Bits: **VTLM_RNG[1:0]**) and VOUT is greater than 2 V, the VDS fault is triggered and the controller goes to FAULT state, which keeps the FET off and asserts the FAULT or SMBALERT pins.

VDS fault is released as soon as the V_{DS} voltage of the FET goes below the same programmed VDS_FAULT_LIMIT or the voltage on the VOUT goes below 2. Especially in cases where the VIN is less than the programmed VDS_FAULT_LIMIT, the controller goes back into STANDBY state and if conditions allow, FET can be turned-on.

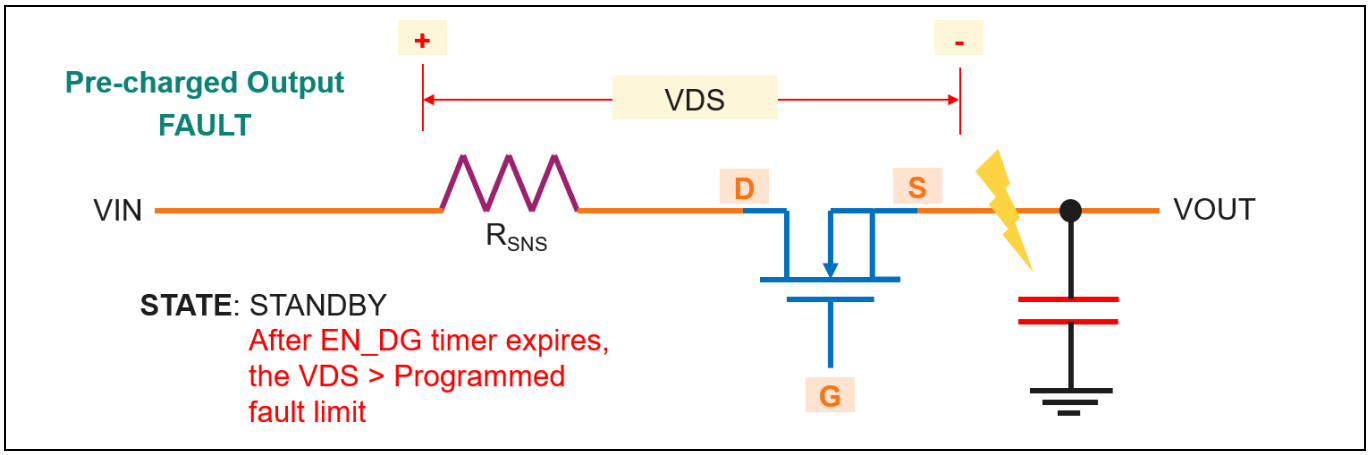


Figure 14 VDS fault detection

Table 12 VDS_FAULT_LIMIT under command 0xD4: V_SNS_CFG

VDS_FAULT_LIMIT [14:13]	VTLM_RNG		
	88 V	**44 V**	**22 V**
0x0 (00 bin)	10 V	5 V	2.5 V
0x1 (01 bin)	20 V	10 V	5 V
0x2 (10 bin)	30 V	15 V	7.5 V
0x3 (11 bin)	35 V	17.5 V	8.75 V

Note: VDS fault is detected only when entering into STANDBY state after a Power on Reset or after a RESTART event.

To ensure that the supply is stable when VDS is checked, it is recommended that the EN_DG timer has some value programmed other than ‘0’ when using VDS fault detection feature.

3.5 Adjustable power averaging up to three seconds

The maximum power averaging option available IN XDP710-002was up to 13.1072 ms. This has been improved in XDP711-001 to a maximum of 3.35 seconds. The averaging in power can be programmed via P_TELEMETRY_AVG (Command code: **0xE9**, Command name: **TELEMETRY_CFG,** Bits: **P_TELEMETRY_AVG[9:6]**). Table 13 shows the different power averaging options available in XDP711-001.

Table 13 P_TELEMETRY_AVG under command 0xE9: TELEMETRY_CFG

P_TELEMETRY_AVG[9:6]	No. of samples averaged	Power averaging time
0x0 (0000 bin)	1	102.4 µs
0x1 (0001 bin)	2	204.8 µs
0x2 (0010 bin)	4	409.6 µs
0x3 (0011 bin)	8	819.2 µs
0x4 (0100 bin)	16	1.64 ms
0x5 (0101 bin)	32	3.27 ms
0x6 (0110 bin)	64	6.55 ms
0x7 (0111 bin)	128	13.10 ms
0x8 (1000 bin)	256	26.21 ms
0x9 (1001 bin)	512	52.43 ms
0xA (1010 bin)	1024	104.86 ms
0xB (1011 bin)	2048	209.72 ms
0xC (1100 bin)	4096	419.43 ms
0xD (1101 bin)	8192	838.86 ms
0xE (1110 bin)	16384	1.677 s
0xF (1111 bin)	32768	3.35 s

Note: The power averaging effects the telemetry averaging of both READ_PIN (Command: 0x97) and READ_PIN_EXT (Command: 0xEE).

3.6 Telemetry peaks and valleys detection

In XDP710-002, the peak and valley of input current, input voltage, output voltage, and power are taken from the averaged telemetry data as shown in Figure 15.

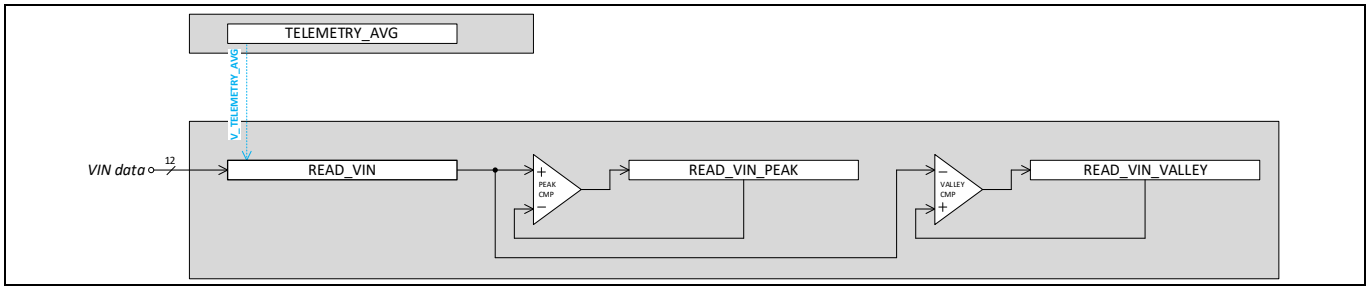


Figure 15 Peak and valley detection of VIN in XDP7x0-002 and XDP710-001

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In XD711-001, the peaks and valleys values are independent of averaging and are taken from the instantaneous data i.e., every 102.4 µs as shown in Figure 16.

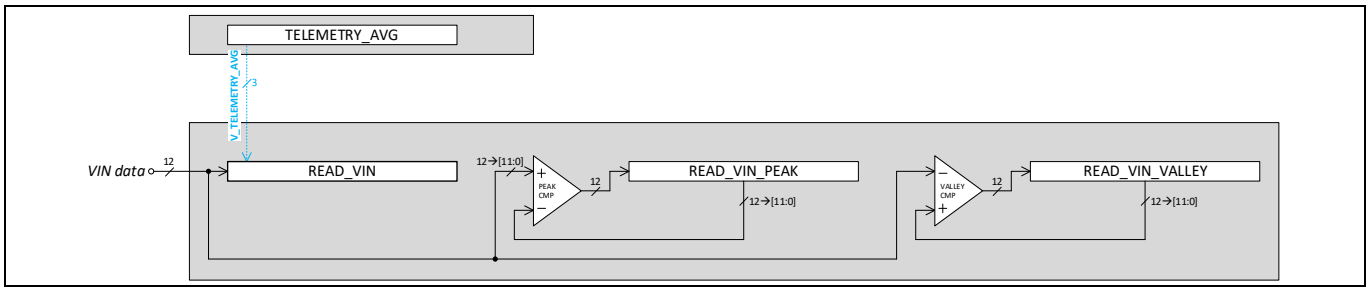


Figure 16 Peak and Valley detection of Vin in XDP711-001

3.7 Configurable input overvoltage hysteresis (VIN_OV_HYST)

In XDP711-001, the input overvoltage fault hysteresis is programmable via the register VIN_OV_HYST (Command code: **0xD4**, Command name: **V_SNS_CFG,** Bits: **VIN_OV_HYST[12:10]**) when input overvoltage fault detection is based on input voltage telemetry sensed at ISNS_P pin instead of OV pin. Table 14 shows the various available options for setting input overvoltage recovery hysterfesis based on different voltage sense range.

Table 14 VIN_OV_HYST under command 0xD4: V_SNS_CFG

VIN_OV_HYST[12:10]	VTLM_RNG		
	88 V	**44 V**	**22 V**
0x0 (000 bin)	1 V	0.5 V	0.25 V
0x1 (001 bin)	2 V	1 V	0.5 V
0x2 (010 bin)	3 V	1.5 V	0.75 V
0x3 (011 bin)	4 V	2 V	1 V
0x4 (100 bin)	5 V	2.5 V	1.25 V
0x5 (101 bin)	6 V	3 V	1.5 V
0x6 (110 bin)	7 V	3.5 V	1.75 V
0x7 (111 bin)	8 V	4 V	2 V

3.8 RESTARTN Pin

In XDP711-001, the restart feature can be triggered not only by RESTART (Command: 0xEC) PMBus command but can also by toggling the GPO2 pin (falling edge triggered) if configured as RESTARTN pin via register GPO2_CFG (Command code: 0xDB, Command name: GPO_CFG, Bits: GPO2_CFG[8:9]). Table 15 shows the required GPO2 settings to enable the restart feature on GPO2 pin.

Table 15 GPO2_CFG under command 0xDB: GPO_CFG

GPO2_CFG [6:7]	Description
0x0 (00 bin)	GPO2 functionality is disabled
0x1 (01 bin)	Pin reflects GPO2_ST [2] status
0x2 (10 bin)	Pin is configured as CGDN with pull-up resistor (input)
0x3 (11 bin)	Pin is configured as RESTARTN with pull-up resistor (input)

3.9 Extended energy counter

In XDP711-001, a new PMBus command READ_EIN_EXT (Command: **0xFB**) has been added, which is an extended version of READ_EIN (Command: **0xE6**). In the READ_EIN_EXT register, the power accumulator size has been extended from 24-bits to 40-bits as shown in Table 16. Since the energy counter reads the READ_PIN, which is a 16-bit value, the 24-bits of the rollover counter allows accumulation of a total of 16777215 ((2^24) -1) READ_PIN samples. Each sample is available after every 102.4 µs, thus power can be accumulated reliably over 28.6 minutes without the counter rolling over the maximum value.

Table 16 READ_EIN_EXT (Command: 0xFB)

Register	**READ_EIN_EXT**															
Offset	0xFB															
Address	0x0FB															
AsyncReset	0x0000000000000000															
Description	**The READ_EIN_EXT command returns the input energy reading in direct format.**															
Bit	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
Field	SAMPLE_COUNT...															
Bit	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
Field	...SAMPLE_COUNT								ROLLOVER_COUNT...							
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Field	...ROLLOVER_COUNT															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	ENERGY_COUNT															

Follow the procedure to calculate energy:

1. Read READ_EIN_EXT (Command: 0xFB) register at time t1 and extract the following values:

Table 17 Reading READ_EIN_EXT at t=t1 instance

READ_EIN_EXT[39:0]: ROLLOVER_COUNT [24:0] + ENERGY_COUNT[15:0]	**READ_EIN_EXT[63:40]: SAMPLE_COUNT[23:0]**
Accumulated_Power_t1	Sample_Counts_t1

2. Read another instance of READ_EIN_EXT register at timer t2 and extract the following values:

Table 18 Reading READ_EIN_EXT at t=t2 instance

READ_EIN_EXT[39:0]: ROLLOVER_COUNT [24:0] + ENERGY_COUNT[15:0]	**READ_EIN_EXT[63:40]: SAMPLE_COUNT[23:0]**
Accumulated_Power_t2	Sample_Counts_t2

Note: Ensure that the time difference between the time t2 and t1 is lower than 28.6 minutes, otherwise the calculated energy values will be junk values.

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3. Calculate the difference of sample counts to determine the accurate time differences between the two samples:

Code listing 1 Calculate time difference between two sample counts

```
If Sample_Counts_t2 is greater than Sample_Counts_t1 then:
Sample_Counts (t2-t1) = Sample_Counts_t2- Sample_Counts_t1

If Sample_Counts_t2 is less than Sample_Counts_t1 then:
                    Sample_Counts (t2-t1) = 0xFFFFFF + Sample_Counts_t2- Sample_Counts_t1
```

4. Calculate the difference of accumulated power counts to determine the accurate power accumulation between the two samples:

Code listing 2 Calculating accumulated power between two samples

```
If Accumulated_Power_t2 is greater than Accumulated_Power_t1 then:
Accumulated_Power (t2-t1) = Accumulated_Power_t2- Accumulated_Power_t1

If Accumulated_Power_t2 is less than Accumulated_Power_t1 then:
Accumulated_Power (t2-t1) = 0xFFFFFFFFFF + Accumulated_Power_t2- Accumulated_Power_t1
```

5. Convert the Sample_Counts into real world value using Equation 11.

$$Time\ elapsed\ between\ the\ samples = Sample_{Counts} \times 102.4 \times 10^{-6}\ \text{seconds}$$

Equation 11 Elapsed time calculation

6. Convert the accumulated power into real world value using Equation 12.

$$Energy = \frac{(Accumulated_{Power} \times 10^{(-r)} - b)}{m \times R_{sns_pop}(m\Omega)}\ Joules$$

Equation 12 Energy calculation equation

The m, r, and b values can be accessed from Table 19.

Note: The Rsns_pop is the equivalent shunt resistance populated on the board for current sensing.

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Table 19 READ_EIN_EXT coefficient values based on VLTM_RNG and CS_RNG

VTLM_RNG (V)	CS_RNG (mV)	m	b	r
88	12.5	10780	0	0
	25	5390	0	0
	50	26949	0	-1
	100	13474	0	-1
44	12.5	21559	0	0
	25	10780	0	0
	50	5390	0	0
	100	26949	0	-1
22	12.5	43120	0	0
	25	21559	0	0
	50	10780	0	0
	100	5390	0	0

3.10 SOA profiles updates

In XDP711-001, more SOA profiles have been added to support new FETs offered from Infineon and instead of having 10 ms SOA lines, Half DC SOA lines have been added for each FET to address the high-power designs.

When XDP711-001 is used for designs that have the maximum current setting greater than 83.33 A, the ratio of programmed Rsns and equivalent Rsns in the circuit is violated. In these designs, the R_{eqv} is always lower than the Rsns programmed and requires the scaling of the SOA profile accordingly. As an example, if the target current set in SOA profile is 2 A with Rsns_programmed is 0.3 mohm and CS_RNG = 25 mV but the Rsns_equv is 0.15 mohm, then the controller will regulate the current at 4 A instead of regulating at 2 A, which can destroy the FET. Hence, for these situations, special care should be taken to adjust the SOA profile accordingly and to address this issue, in XDP711-001 the half DC SOA profiles have been added.

Table 20 highlights the differences in the SOA profile options between XDP710-002 and XDP711-011.

Table 20 Differences in SOA profile options for XDP710-002 and XDP711-001 using FDM mode

FET_SELECT[5:0]	SOA Profile in XDP7xx-002	SOA Profile in XDP711-001
0x00 (00 0000 bin)	BSC027N10NS5ATMA1 – DC Line	BSC027N10NS5ATMA1 – DC Line
0x01 (00 0001 bin)	BSC035N10NS5ATMA1 – DC Line	**ISC022N10NM6– DC Line**
0x02 (00 0010 bin)	BSC040N10NS5ATMA1 - DC Line	**ISC027N10NM6– DC Line**
0x03 (00 0011 bin)	IPTG011N08NM5 - DC Line	IPTG011N08NM5 - DC Line
0x04 (00 0100 bin)	IPTC012N08NM5 - DC Line	IPTC012N08NM5 - DC Line
0x05 (00 0101 bin)	IPB017N10N5LFATMA1 – DC Line	IPB017N10N5LFATMA1 – DC Line
0x06 (00 0110 bin)	BSC093N15NS5 - DC Line	**ISC025N08NM5LF2– DC Line**
0x07 (00 0111 bin)	BSC074N15NS5 - DC Line	**ISC035N10NM5LF2– DC Line**
0x08 (00 1000 bin)	IPTG014N10NM5 - DC Line	IPTG014N10NM5 - DC Line
0x09 (00 1001 bin)	IPTC015N10NM5 - DC Line	IPTC015N10NM5 - DC Line
0x0A (00 1010 bin)	IPT015N10N5ATMA1 – DC Line	IPT015N10N5ATMA1 – DC Line

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FET_SELECT[5:0]	SOA Profile in XDP7xx-002	SOA Profile in XDP711-001
0x0B (00 1011 bin)	IPB017N10N5ATMA1 – DC Line	IPB017N10N5ATMA1 – DC Line
0x0C (00 1100 bin)	IPB018N10NM6 - DC Line	IPB018N10NM6 - DC Line
0x0D (00 1101 bin)	IPT013N08NM5LF - DC Line	**ISC030N10NM6– DC Line**
0x0E (00 1110 bin)	IPB020N10N5ATMA1 – DC Line	IPB020N10N5ATMA1 – DC Line
0x0F (00 1111 bin)	IPB020N10N5LFATMA1– DC Line	IPB020N10N5LFATMA1– DC Line
0x10 (01 0000 bin)	IPB027N10N5ATMA1 – DC Line	IPB027N10N5ATMA1 – DC Line
0x11 (01 0001 bin)	IPB032N10N5ATMA1 – DC Line	IPB032N10N5ATMA1 – DC Line
0x12 (01 0010 bin)	IPB033N10N5LFATMA1 – DC Line	IPB033N10N5LFATMA1 – DC Line
0x13 (01 0011 bin)	IPB072N15N3 – DC Line	IPB072N15N3 – DC Line
0x14 (01 0100 bin)	IPB042N10N3 – DC Line	IPB042N10N3 – DC Line
0x15 (01 0101 bin)	IPT016N10NM5LF – DC Line	**Reserved**
0x16 (01 0110 bin)	Reserved	**IQD020N10NM5CG– DC Line**
0x17 (01 0111 bin)	Reserved	**BSC035N10NS5ATMA1 – DC Line**
0x18 (01 1000 bin)	Reserved	**BSC040N10NS5ATMA1 - DC Line**
0x19 (01 1001 bin)	Reserved	**BSC093N15NS5 - DC Line**
0x1A (01 1010 bin)	Reserved	**BSC074N15NS5 - DC Line**
0x1B (01 1011 bin)	Reserved	**LF1FET1 - DC Line**
0x1C (01 1100 bin)	Reserved	**LF2FET2 - DC Line**
0x1D (01 1101 bin)	Reserved	Reserved
0x1E (01 1110 bin)	Reserved	Reserved
0x1F (01 1111 bin)	Reserved	Reserved
0x20 (10 0000 bin)	BSC027N10NS5ATMA1 – 10 ms line	**BSC027N10NS5ATMA1 – 1/2 DC Line**
0x21 (10 0001 bin)	BSC035N10NS5ATMA1 – 10 ms line	**ISC022N10NM6– 1/2 DC Line**
0x22 (10 0010 bin)	BSC040N10NS5ATMA1 – 10 ms line	**ISC027N10NM6– 1/2 DC Line**
0x23 (10 0011 bin)	IPTG011N08NM5 – 10 ms line	**IPTG011N08NM5 - 1/2 DC Line**
0x24 (10 0100 bin)	IPTC012N08NM5 – 10 ms line	**IPTC012N08NM5 - 1/2 DC Line**
0x25 (10 0101 bin)	IPB017N10N5LFATMA1 – 10 ms line	**IPB017N10N5LFATMA1 – 1/2 DC Line**
0x26 (10 0110 bin)	BSC093N15NS5 – 10 ms line	**ISC025N08NM5LF2– 1/2 DC Line**
0x27 (10 0111 bin)	BSC074N15NS5 – 10 ms line	**ISC035N10NM5LF2– 1/2 DC Line**
0x28 (10 1000 bin)	IPTG014N10NM5 – 10 ms line	**IPTG014N10NM5 - 1/2 DC Line**
0x29 (10 1001 bin)	IPTC015N10NM5 – 10 ms line	**IPTC015N10NM5 - 1/2 DC Line**
0x2A (10 1010 bin)	IPT015N10N5ATMA1 – 10 ms line	**IPT015N10N5ATMA1 – 1/2 DC Line**
0x2B (10 1011 bin)	IPB017N10N5ATMA1 – 10 ms line	**IPB017N10N5ATMA1 – 1/2 DC Line**
0x2C (10 1100 bin)	IPB018N10NM6 – 10 ms line	**IPB018N10NM6 - 1/2 DC Line**
0x2D (10 1101 bin)	IPT013N08NM5LF – 10 ms line	**ISC030N10NM6– 1/2 DC Line**
0x2E (10 1110 bin)	IPB020N10N5ATMA1 – 10 ms line	**IPB020N10N5ATMA1 – 1/2 DC Line**
0x2F (10 1111 bin)	IPB020N10N5LFATMA1– 10 ms line	**IPB020N10N5LFATMA1– 1/2 DC Line**
0x30 (11 0000 bin)	IPB027N10N5ATMA1 – 10 ms line	**IPB027N10N5ATMA1 – 1/2 DC Line**
0x31 (11 0001 bin)	IPB032N10N5ATMA1 – 10 ms line	**IPB032N10N5ATMA1 – 1/2 DC Line**

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FET_SELECT[5:0]	SOA Profile in XDP7xx-002	SOA Profile in XDP711-001
0x32 (11 0010 bin)	IPB033N10N5LFATMA1 – 10 ms line	**IPB033N10N5LFATMA1 – 1/2 DC Line**
0x33 (11 0011 bin)	IPB072N15N3 – 10 ms line	**IPB072N15N3 – 1/2 DC Line**
0x34 (11 0100 bin)	IPB042N10N3 – 10 ms line	**IPB042N10N3 – 1/2 DC Line**
0x35 (11 0101 bin)	IPT016N10NM5LF – 10 ms line	**Reserved**
0x36 (11 0110 bin)	Reserved	**IQD020N10NM5CG– 1/2 DC Line**
0x37 (11 0111 bin)	Reserved	**BSC035N10NS5ATMA1 – 1/2 DC Line**
0x38 (11 1000 bin)	Reserved	**BSC040N10NS5ATMA1 - 1/2 DC Line**
0x39 (11 1001 bin)	Reserved	**BSC093N15NS5 - 1/2 DC Line**
0x3A (11 1010 bin)	Reserved	**BSC074N15NS5 - 1/2 DC Line**
0x3B (11 1011 bin)	Reserved	**LF1FET1 - 1/2 DC Line**
0x3C (11 1100 bin)	Reserved	**LF2FET2 - 1/2 DC Line**
0x3D (11 1101 bin)	Reserved	Reserved
0x3E (11 1110 bin)	Reserved	Reserved
0x3F (11 1111 bin)	SOA OTP (User Defined SOA)	SOA OTP (User Defined SOA)

If AADM mode is selected, then Table 21 shows the differences in XDP710-002 and XDP711-001 on the selection of pre-defined SOA profiles using MODE pins. While porting the design from XDP710-002 to XDP711-001 utilizing AADM mode, care should be taken to select the correct resistors for corresponding SOA profiles.

XDP711-001 features

Table 21 Differences in SOA profile options for XDP710-002 and XDP711-001 using AADM mode

MODE1 pin voltage	MODE0 pin voltage	SOA Profiles in XDP710-002	SOA Profiles in XDP711-001
GND (MODE1<0.8 V)	GND (MODE0<0.8 V)	BSC027N10NS5	BSC027N10NS5
GND (MODE1≥2.4 V)	12 kΩm (0.8 V≤MODE0<1.6 V)	BSC035N10NS5	**ISC022N10NM6**
GND (MODE1≥2.4 V)	20 kΩ (1.6 V≤MODE0<2.4 V)	BSC040N10NS5	**ISC027N10NM6**
GND (MODE1≥2.4 V)	Open (MODE0≥2.4 V)	IPTG011N08NM5	IPTG011N08NM5
12 kΩ (0.8 V≤MODE1<1.6 V)	GND (MODE0<0.8 V)	IPTC012N08NM5	IPTC012N08NM5
12 kΩ (0.8 V≤MODE1<1.6 V)	12 kΩ (0.8 V≤MODE0<1.6 V)	IPB017N10N5LF	IPB017N10N5LF
12 kΩ (0.8 V≤MODE1<1.6 V)	20 kΩ (1.6 V≤MODE0<2.4 V)	BSC093N15NS5	**ISC025N08NM5LF2**
12 kΩ (0.8 V≤MODE1<1.6 V)	Open (MODE0≥2.4 V)	BSC074N15NS5	**ISC035N10NM5LF2**
20 kΩ (1.6 V≤MODE1<2.4 V)	GND (MODE0<0.8 V)	IPTG014N10NM5	IPTG014N10NM5
20 kΩ (1.6 V≤MODE1<2.4 V)	12 kΩ (0.8 V≤MODE0<1.6 V)	IPTC015N10NM5	IPTC015N10NM5
20 kΩ (1.6 V≤MODE1<2.4 V)	20 kΩ (1.6 V≤MODE0<2.4 V)	IPT015N10N5	IPT015N10N5
20 kΩ (1.6 V≤MODE1<2.4 V)	Open (MODE0≥2.4 V)	IPB017N10N5	IPB017N10N5
Open (MODE1≥2.4 V)	GND (MODE0<0.8 V)	IPB018N10NM6	IPB018N10NM6
Open (MODE1≥2.4 V)	12 kΩ (0.8 V≤MODE0<1.6 V)	IPT013N08NM5LF	**ISC030N10NM6**
Open (MODE1≥2.4 V)	20 kΩ (1.6 V≤MODE0<2.4 V)	IPB020N10N5	IPB020N10N5
Open (MODE1≥2.4 V)	Open (MODE0≥2.4 V)	SOA Profile selected via MODE command	SOA Profile selected via MODE command

3.11 User-specific configuration ID storage register

In XDP711-001, a new 1-byte register CONFIG_ID accessed using PMBus command CONFIG_ID (Command: **0xFA**) has been added to allow user to store their desired information. This can be used to store the configuration ID to quickly identify the configuration that is been stored into the controller.

3.12 Warning activations

The differences in warnings activation between XDP710-002 and XDP711-001 are highlighted in bold in the following table:

Table 22 Warning activation in XDP711-001

Warning name	State of controller														
	POR_INIT	READ_OTP	READ_PINS	ANA_EN	CHK_FET	STANDBY	INIT_SOA_REG	ON	I_REG	SURGE	GREC1	GREC2	FAULT	WAIT_10S	MEM_FAULT/ LATCH_OFF
VGSL	–	–	–	–	–	–	–	X	–	–	–	–	–	–	–
OT	–	–	–	–	–	X	X	X	X	X	X	X	X	–	–
TSD	–	–	–	–	–	X	X	X	X	X	X	X	X	–	–
UV	–	–	–	–	–	X	X	X	X	X	X	X	X	–	–
OV	–	–	–	–	–	X	X	X	X	X	X	X	X	–	–
OOV	–	–	–	–	–	X	X	X	X	X	X	X	X	–	–
OUV	–	–	–	–	–	–	–	X	X	X	X	X	–	–	–
SOAR	–	–	–	–	–	–	–	X	X	–	–	–	–	–	–

XDP711-001 features

Warning name	State of controller														
	POR_INIT	READ_OTP	READ_PINS	ANA_EN	CHK_FET	STANDBY	INIT_SOA_REG	ON	I_REG	SURGE	GREC1	GREC2	FAULT	WAIT_10S	MEM_FAULT/ LATCH_OFF
OUC	–	–	–	–	–	–	–	X	X	–	–	–	–	–	–
OOC	–	–	–	–	–	**X**	**X**	X	X	X	X	X	–	–	–
INeg	–	–	–	–	–	–	--	X	X	–	–	–	–	–	–
OP	–	–	–	–	–	**X**	X	X	X	X	X	X	–	–	–
COM	–	–	–	–	X	X	X	X	X	X	X	X	X	X	X

4 Hardware changes required in XDP711-001

In XDP711-001, the following hardware changes are necessary to port the design from XDP710-002:

- The Pin 25 (SOURCE) and Pin 24 (VOUT) functionality have been combined into a single Pin 25 (VOUT). Hence, both the sensing of output voltage and the connection of SOURCE node of the MOSEFT is done via the same pin
- Pin 24 is now utilized for populating a charge pump capacitor in between Pin 24 (VCP) and Pin 25 (VOUT) for utilizing the surge immunity feature. Even if this feature is not used, it is recommended to leave a footprint for a capacitor
- Capacitor footprint is required between Pin 26 (GATE) and Pin 25 (VOUT). This is required when the surge immunity feature is utilized and the calculations of this capacitor is explained in Section 3.2 via Equation 2, Equation 3, and Equation 4
- A resistor to GND and a capacitor to GND is required on Pin 19 (AMON) if AMON feature has been utilized. The resistor is required for converting the current to voltage for interfacing it with ADC for reading analog current or power, the capacitor is required to reduce the noise
- The input voltage range of XDP711-001 has been updated to a voltage range of 7 V to 80 V while for XDP710-002, from 5 V to 80 V

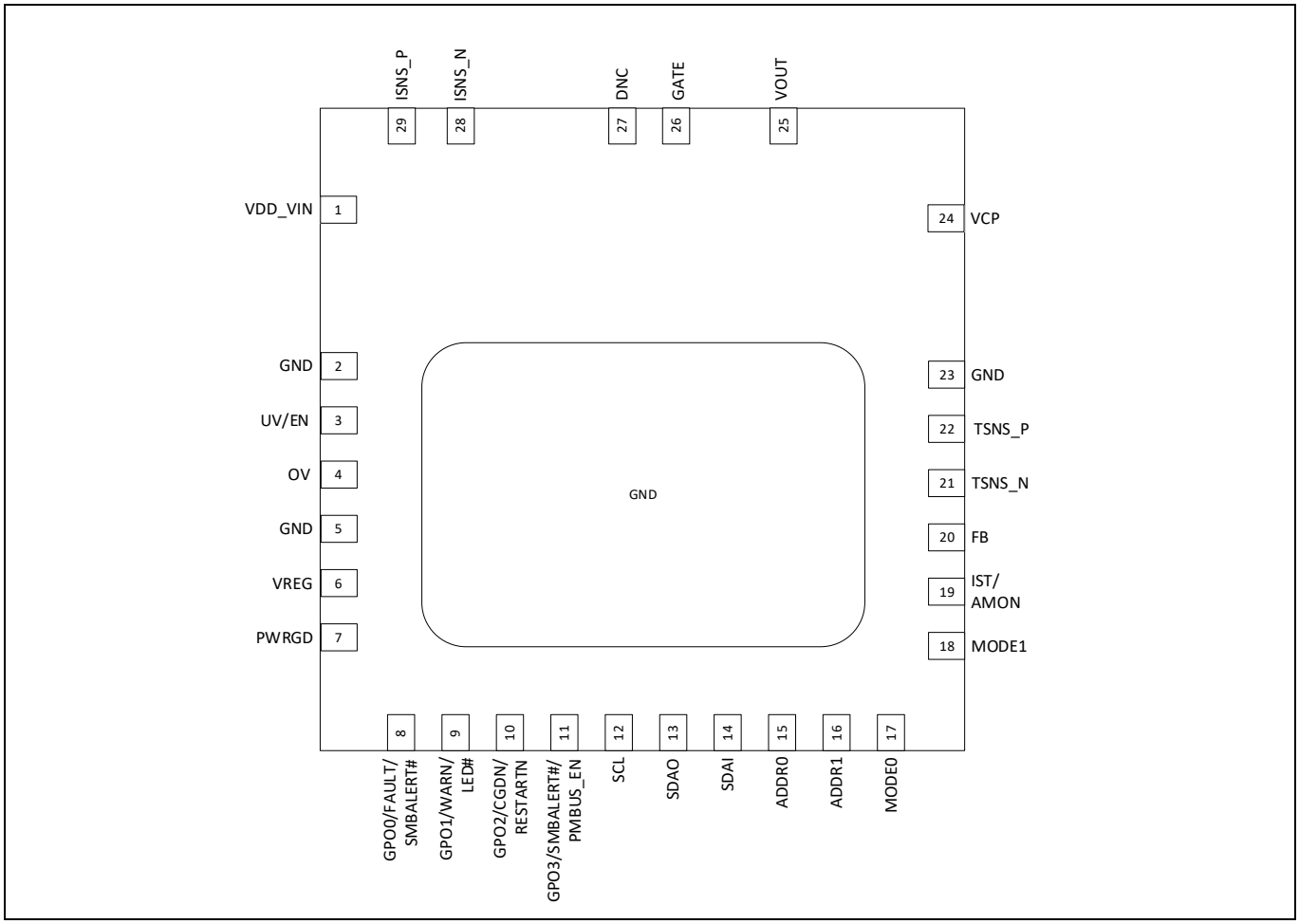


Figure 17 XDP711-001 pinout

5 PCB layout guidelines and schematics

5.1 VCP pin layout

Figure 18 displays the schematics of the gate driver for XDP711-001. GATE is connected to the gate pins of all power MOSFETs through some resistors, while V_{OUT} is connected to the source pins. VCP is the voltage reservoir capacitor pin for the integrated charge pump and needs to be connected an external capacitor (C2) from this pin to V_{OUT} pin. Table 15 shows the recommended PCB layout guidelines.

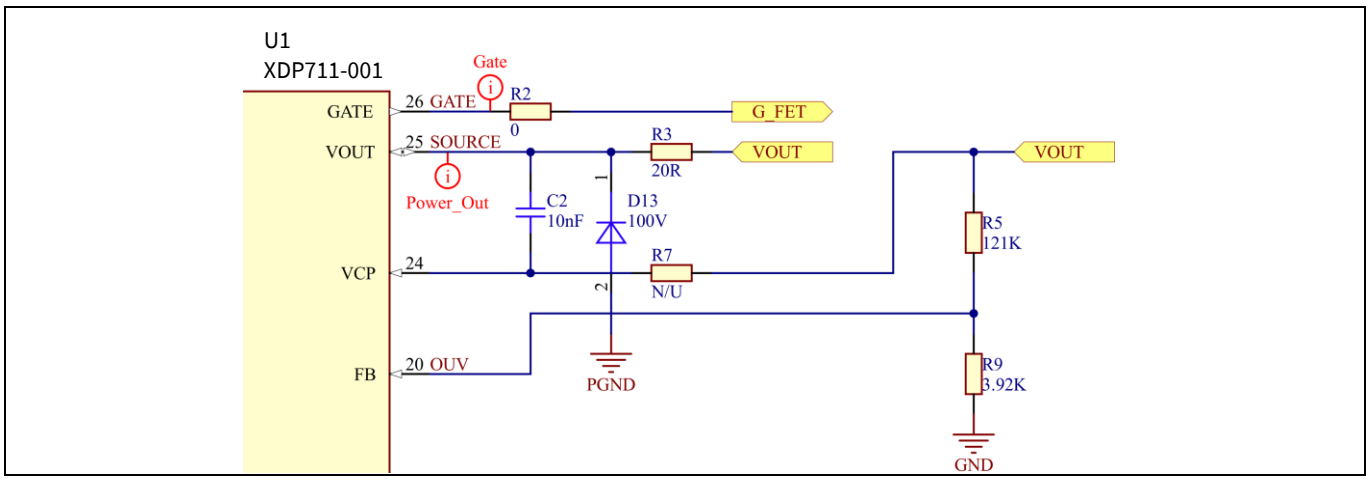


Figure 18 Schematics of gate driver for XDP711-001

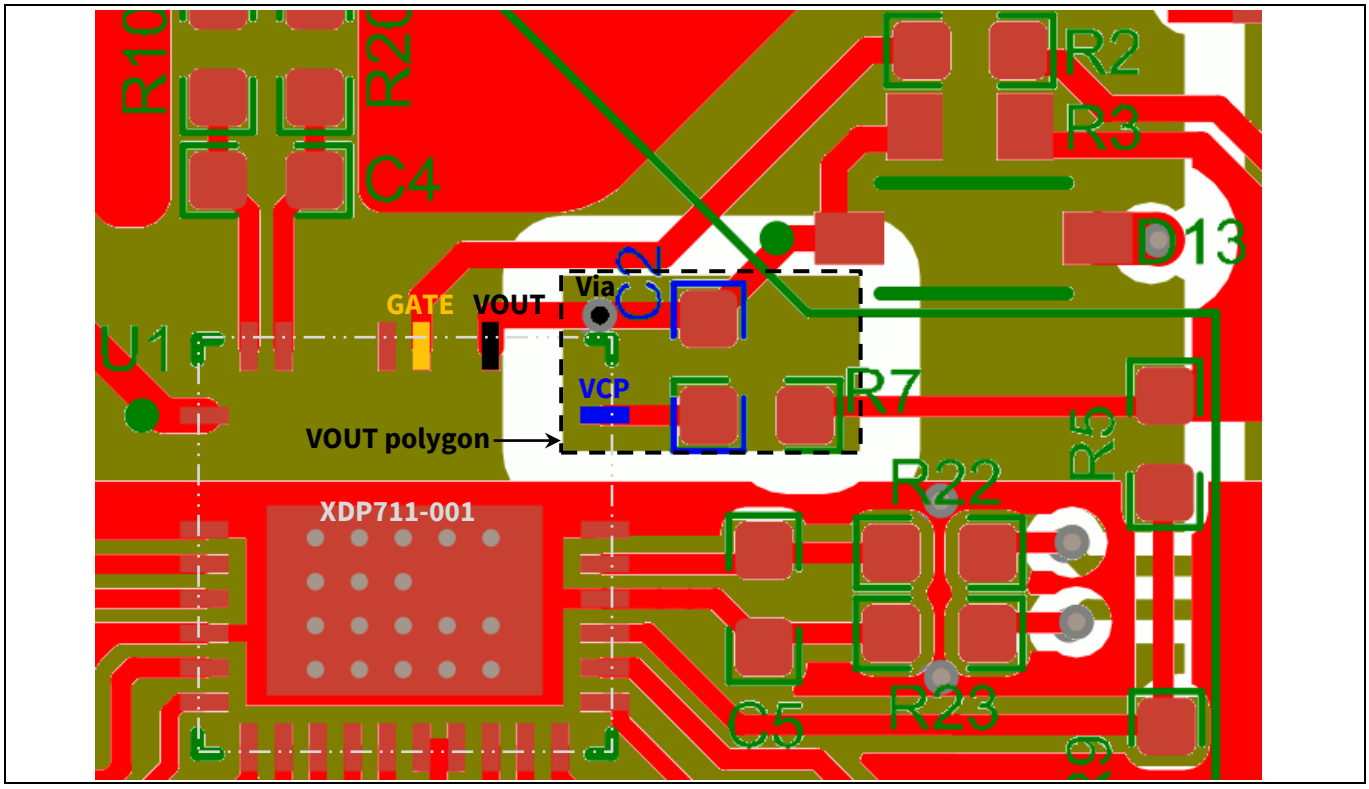


Figure 19 PCB top layer (red) on middle layer 2 (green)

PCB layout guidelines and schematics

The recommended PCB layout guidelines are:

- Put the VCP capacitor (C2) as close as possible to the VCP pin
- **Important**: Put a VOUT polygon on the adjacent layer (Middle Layer 2 in this example) under the VCP pin and the VCP capacitor pad. A V_{OUT} via (or a few vias) connects the V_{OUT} polygon to the V_{OUT} signal
- Minimize the copper area of VCP pad, VCP trace, and the pad(s) connected to VCP pin. In this example, the capacitor (C2) and resistor (R7) pads of VCP signal is shared by a single pad as C2 and R7 will not be installed at the same time

6 Design compatible with both XDP710-002 and XDP711-001

To have the design compatible with both the parts, it is advisable to have a footprint for a capacitor and a resistor in between Pin 24 and Pin 25. As shown in Figure 20, components C2 and R7 are added.

For the different use cases, following components needs to be populated:

- **XDP710-002:** Populate R7 and de-populate C11 and C2
- **XDP711-001 (without surge immunity feature):** Populate C2 (can be left open) and de-populate R7 and C11
- **XDP711-001 (with surge immunity feature):** Populate C2 and C11 and de-populate R7

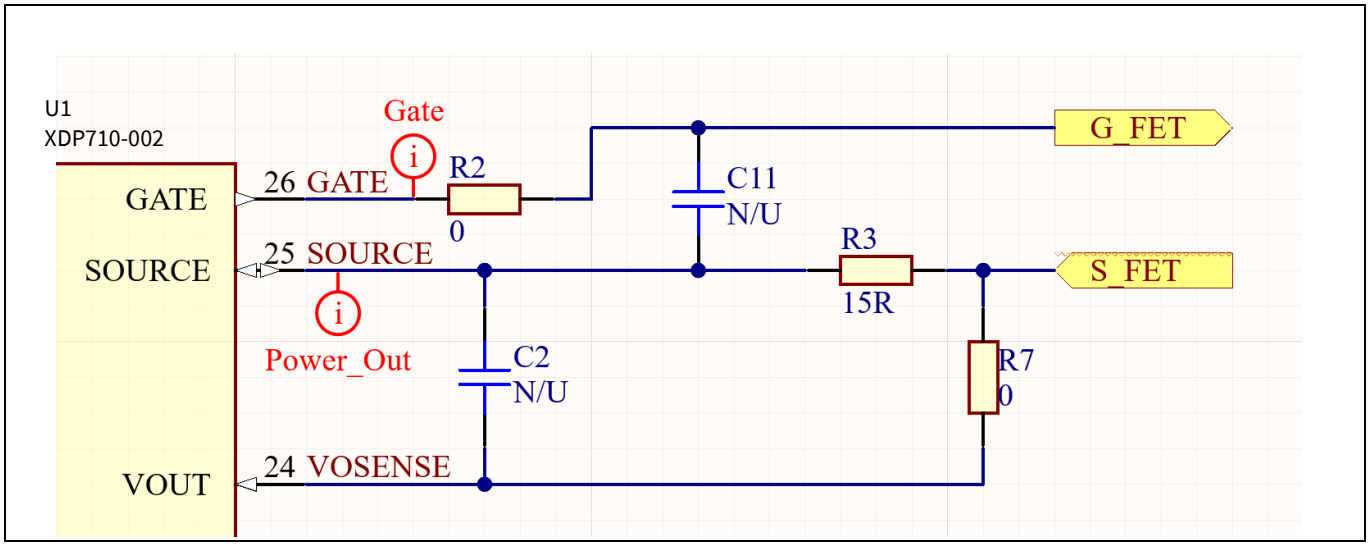


Figure 20 Schematics of Pin 24 and Pin 25 connection for XDP710-002 and XDP711-001

7 Detection algorithm for XDP711-001

Perform the following procedure to identify the XDP711-001 on the PMBus:

1. Identify the manufacturer of the controller by reading the PMBus command 0x99 (command name: **MFR_ID**, Length: **3 bytes**). The data **0x004649** corresponds to Infineon Technologies
2. Block read the PMBus command 0x9A (command name: **MFR_MODEL**, Length: **16 bytes**). The data **0x0000313137504458** corresponds to the detection of a device as XDP711
3. Block read the PMBus command 0x9B (command name: **MFR_REVISION**, Length: **4 bytes**). The data **0x0003** corresponds to detection of REVISION 3 hence the device as XDP711-001

8 Summary

The steps outlined in this document are necessary to have a design ported easily from XDP710-002 to XDP711-001. The XDP Design GUI also provides a **Config File Converter Tool** to convert the XDP710-002 configuration file to XDP711-001 configuration file to have an identical design as that of XDP710-002 and then, the required settings can be modified to utilize the enhanced features of XDP711-001.

References

[1] Infineon Technologies AG: *XDP710-002 hot-swap controller datasheet;* Available online

[2] Infineon Technologies AG: *XDP700-002 hot-swap controller datasheet*; Available online

[3] Infineon Technologies AG: *XDP711-001 hot-swap controller datasheet*; Available online

Revision history

Document revision	Date	Description of changes
V 1.0	2025-06-27	Initial release

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