

Managing Transients in Control IC Driven Power Stages

About this document

Scope and purpose

The scope of this document is to discuss the management of transients in control IC driven power stages, specifically focusing on the effects of parasitic elements on the bridge circuit and the control IC. The purpose is to provide guidelines and recommendations for minimizing the impact of parasitics, avoid latch-up, and ensure reliable operation of the control IC and power stage.

Intended audience

The intended audiences for this document are design engineers, technicians, and developers of electronic systems.

Table of contents

Table of contents

About this document.....	1
Table of contents.....	2
1 Control IC Product Range	3
2 Parasitic Elements of The Bridge Circuit	4
3 VS Undershoot: Cause.....	5
4 VS Undershoot: Effects On the Control IC	6
5 Avoiding Latch-Up.....	7
6 Monitor And Verify	9
6.1 Measurements to verify undershoot severity.....	9
7 General Recommendations	10
7.1 Minimize the parasitics of figure 1	10
7.2 Reduce control IC exposure	10
7.3 Improve local decoupling	10
8 Boosting VS Undershoot Immunity.....	12
9 APPENDIX 1: IR2110 Parasitic Diode Structure	14
References.....	15
Revision history.....	16
Disclaimer.....	17

1 Control IC Product Range

International Rectifier (now acquired by Infineon) offers a broad range of control ICs from single channel to complete three-phase bridge drivers. All types employ high-integrity level shifting techniques to simplify control of power transistors from logic circuits. Our latest products further enhance this capability to drive power switches relatively displaced by up to 1200V.

As leading edge performance demands switching more current at ever higher speeds, the unwanted effects of parasitics are magnified and warrant heightened attention. The aim here is to locate their source, quantify the immunity of the IC against a potentially troublesome effect and finally, show how to maximize the margin between the two.

Parasitic Elements of The Bridge Circuit

2 Parasitic Elements of The Bridge Circuit

The circuit shown in figure 1 depicts a typical application in which two power MOSFETs are driven by a control IC in a half bridge configuration. Unwanted inductance in the power circuit from die bonding in the transistors, pinning and PCB tracks are lumped together and arbitrarily labeled LS1,2 and LD1,2.

Further parasitics will exist in the gate drive circuit and these should also be considered during circuit layout but for now, we will focus on the bridge itself as the highest currents and di/dt will occur here. During switching, rapidly changing bridge current induces voltage transients across all parasitics shown. Left unchecked, these transients may couple into other circuits causing noise problems, increased switch dissipation or even IC damage in extreme cases.

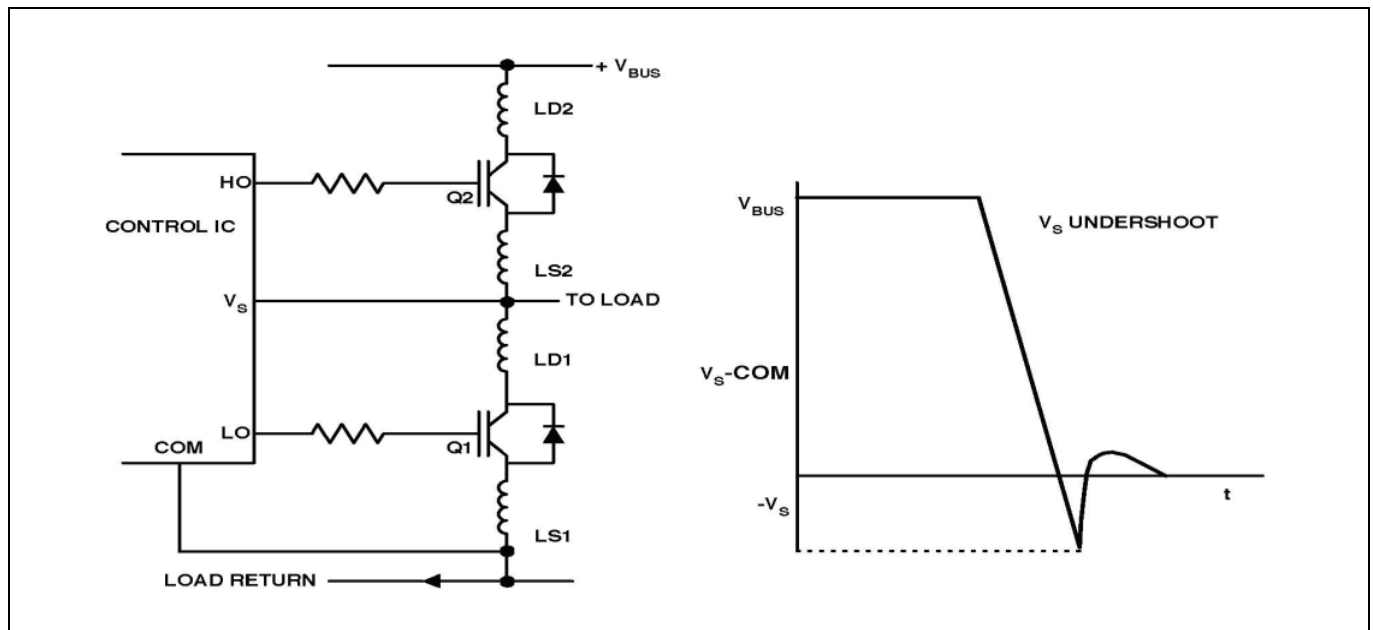


Figure 1 Parasitic Elements of the Half Bridge

3 VS Undershoot: Cause

Of the problems caused by parasitics, one of the main issues for control ICs is a tendency for the VS node to undershoot ground following switching events. Conversely, overshoot does not generally cause a problem due to the high differential voltage capability of Infineon's proven HVIC and Silicon on Insulator (SOI) process.

With inductive loading of the bridge, high side transistor turn-off causes load current to suddenly flow in the low side free-wheeling diode. On top of the 'slack' from diode turn-on delay and forward voltage drop, stray inductance $LS1+LD1$ contribute to undershoot of the Vs node beyond-ground, as shown in the graph of figure 1. If the load circuit does not totally self-commutate in the dead-time (both transistors off) VS undershoot or ringing may occur when the low side device is hard switched.

4 VS Undershoot: Effects On the Control IC

Infineon control ICs are guaranteed completely immune to VS undershoot of at least 5V (as high as 100V for SOI parts), measured with respect to COM. If undershoot exceeds this level, the high side output will temporarily latch in its current state. Provided VS remains within absolute maximum limits the IC will not suffer damage, however the high-side output buffer will not respond to input transitions while undershoot persists beyond 5V. This mode should be noted but proves trivial in most applications, as the high-side is not usually required to change state immediately following a switching event.

Avoiding Latch-Up

5 Avoiding Latch-Up

The parasitic diode structure for a typical control IC (developed with HVIC process) is shown in appendix 1 (a SOI part has less parasitic structure due to the oxide layer). As with any CMOS device, driving any of these diodes into forward conduction or reverse breakdown may cause parasitic SCR latch-up. The ultimate outcome of latchup often defies prediction and can range from temporary erratic operation to total device failure.

The control IC may also be damaged indirectly by a chain of events following initial overstress. By way of example, latch-up could conceivably result in both output drivers assuming a high state, causing cross-conduction followed by switch failure and finally catastrophic damage to the IC. This failure mode should be considered a possible root cause if power transistors and/or control IC are destroyed in the application.

The following theoretical extremes can be used to help explain the relationship between excessive V_S undershoot and the resulting latch-up mechanism.

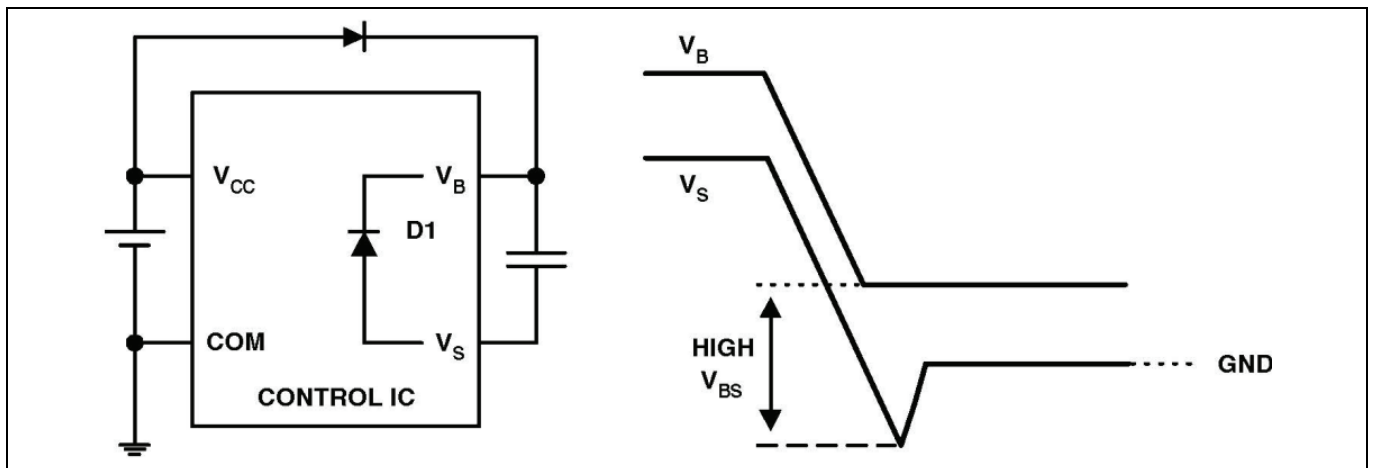


Figure 2 Case 1: Ideal Bootstrap Circuit

In the first case an 'ideal bootstrap' circuit is used in which V_{CC} is driven from a zero-ohm supply with an ideal diode feeding V_B . Undershoot now sums with V_{CC} causing the bootstrap capacitor to overcharge as shown in figure 2. By way of example, if $V_{CC} = 15V$ then V_S undershoot in excess of 10V forces the floating supply above 25V, risking breakdown in diode D1 and subsequent latchup. Suppose now that the bootstrap supply is replaced with the ideal floating supply of figure 3 such that V_{BS} is fixed under all circumstances. Note that using a low impedance auxiliary supply in place of a bootstrap circuit can approach this situation.

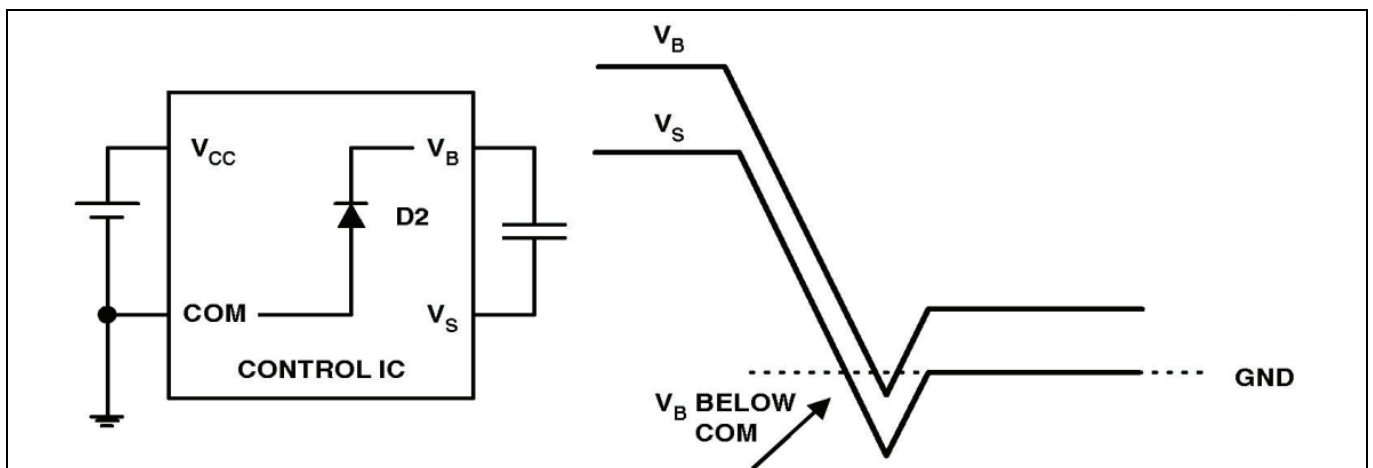


Figure 3 Case 2: Ideal Floating Supply

Avoiding Latch-Up

This time, latch-up risk appears if V_S undershoot exceeds V_{BS} , since parasitic diode D2 will ultimately enter conduction.

A practical circuit is likely to fall somewhere between these two extremes, resulting in both a small increase of V_{BS} and some V_B droop below V_{CC} as depicted by Figure 4.

Exactly which of the two extremes is prevalent can be checked as follows.

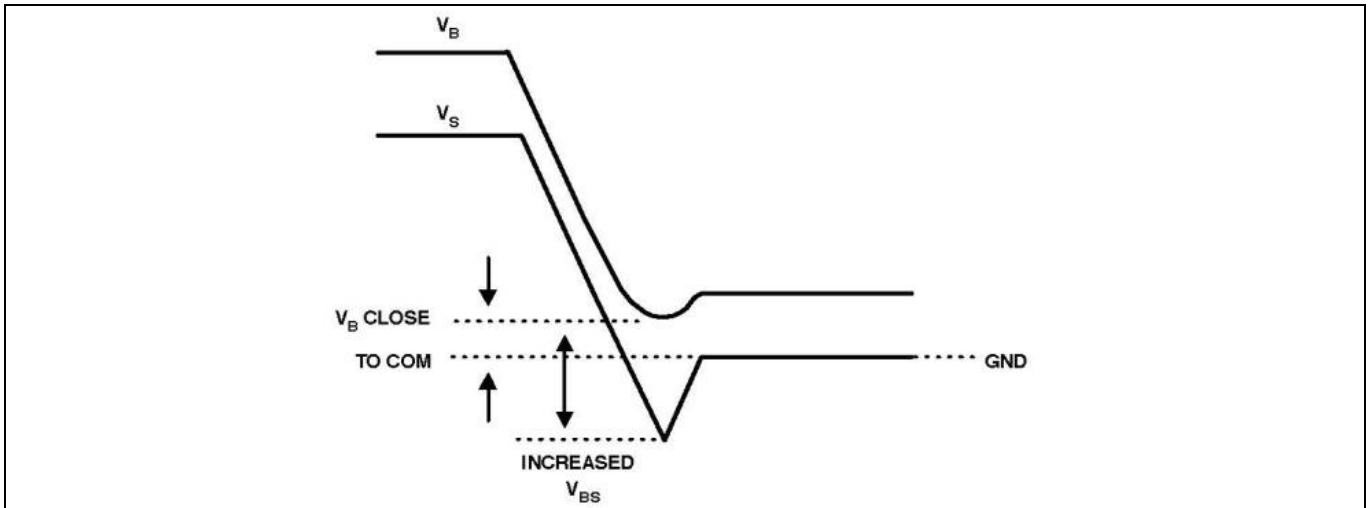


Figure 4 Typical Response

6 Monitor And Verify

The signals listed below should be observed both in normal operation and during high-stress events such as short circuit or over current shutdown, when di/dt is highest. Readings should always be taken directly across IC pins as shown in figure 5, so that contributions from parasitics in the drive coupling are included in the measurement.

6.1 Measurements to verify undershoot severity

1. High side offset with respect to common; V_S - COM
2. The floating supply; V_B - V_S

Most bridge circuits employ a bus of several hundred volts which means selecting an insensitive Y-axis scale to prevent distortion from saturation of the input amplifier. This can make the comparatively small V_S undershoot difficult to quantify.

For best resolution, check your oscilloscope manual and then select the highest useable sensitivity level.

For the second measurement, the signal of interest is permanently superimposed on the changing bridge voltage. The oscilloscope may be floated with a transformer, but this method is discouraged because capacitive loading can alter circuit performance and sometimes mask underlying problems by inadvertently reducing dv/dt .

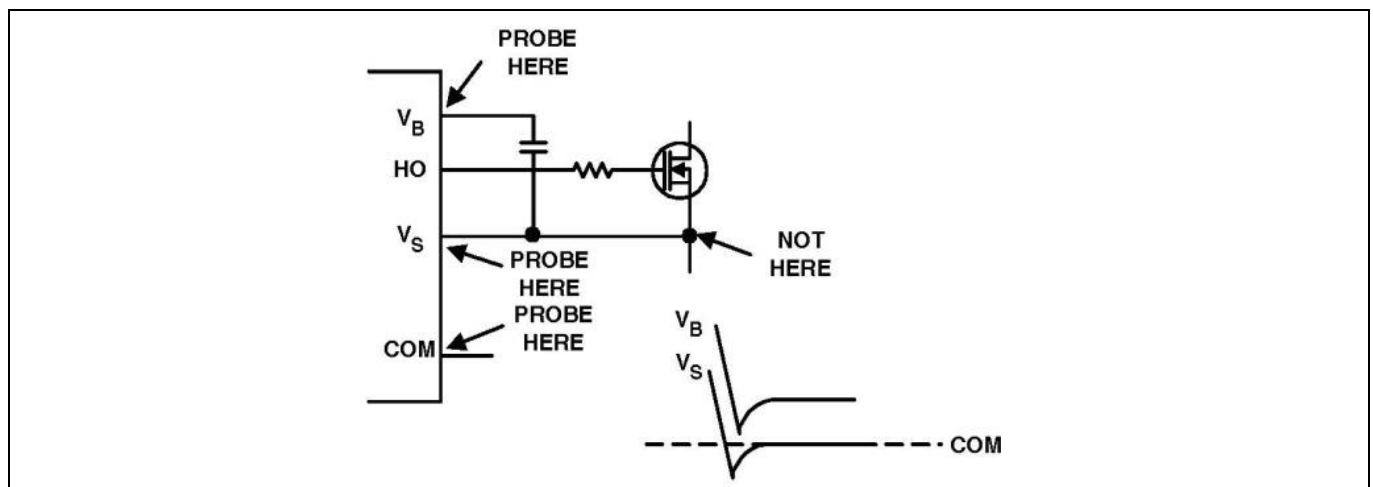


Figure 5 Measurement Points

A high-bandwidth differential voltage probe (or an isolated differential-input oscilloscope) can give good results here, allowing other ground referenced signals to be viewed at the same time. However, be aware of propagation delay mismatch between differential and conventional probes when comparing relative event times.

Always measure the noise floor prior to making measurements. Common-mode noise on high side referenced signals (V_B , HO) can be observed by joining probe tip and ground lead directly to the V_S node.

Do not assume that 'low-side' referenced signals are free from common-mode noise. Measure the noise floor by joining probe tip and ground lead together at the COM node.

General Recommendations

7 General Recommendations

The following guidelines represent good practice in control IC circuits and warrant attention regardless of the observed latch-up safety margin.

7.1 Minimize the parasitics of figure 1

- 1a. Use thick, direct tracks between switches with no loops or deviation.
- 1b. Avoid interconnect links. These can add significant inductance.
- 1c. Reduce the effect of lead-inductance by lowering package height above the PCB.
- 1d. Consider co-locating both power switches to reduce track lengths.

7.2 Reduce control IC exposure

- 2a. Connect VS and COM as shown in figure 6.
- 2b. Minimize parasitics in the gate drive circuit by using short, direct tracks.
- 2c. Locate the control IC as close as possible to the power switches.

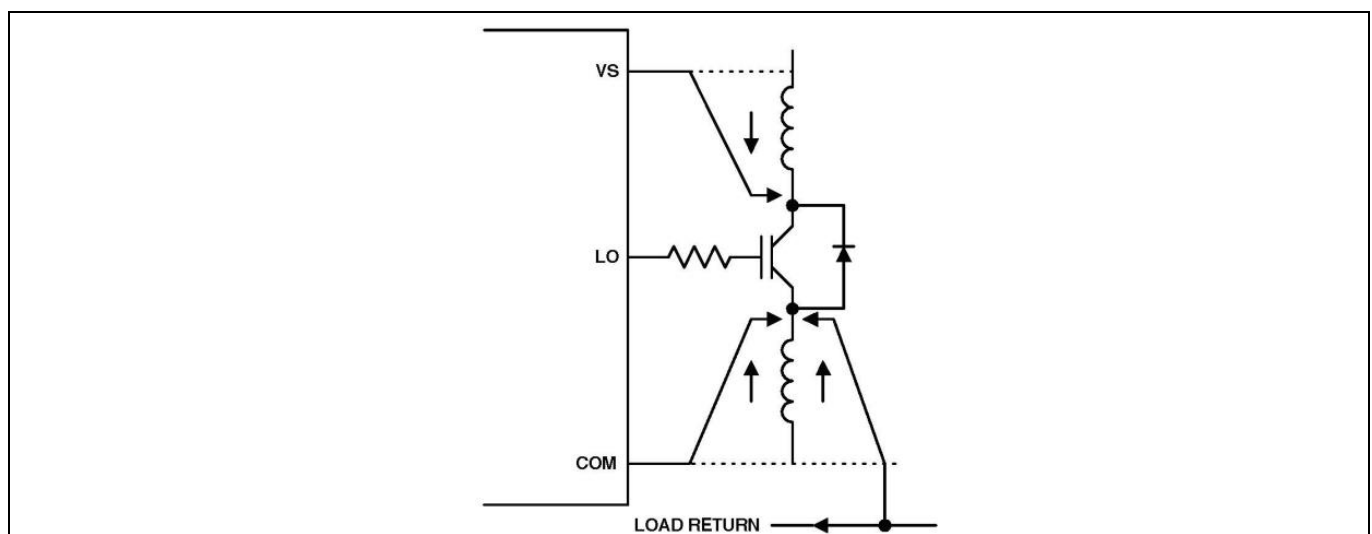


Figure 6 Bypass Parasitics

7.3 Improve local decoupling

- 3a. Increase the bootstrap capacitor (C_b) value using at least one low-ESR capacitor. This will reduce overcharging from severe V_s undershoot. See Design Tip DT98-2 for more information.
- 3b. Use a second low-ESR capacitor from V_{cc} to COM. As this capacitor supports both the low-side output buffer and bootstrap recharge, we recommend a value at least ten times higher than C_b .
- 3c. Connect decoupling capacitors directly across appropriate pins as shown in figure 7.
- 3d. If a resistor is needed in series with the bootstrap diode, verify that V_B does not fall below COM, especially during start-up and extremes of frequency and duty cycle.

General Recommendations

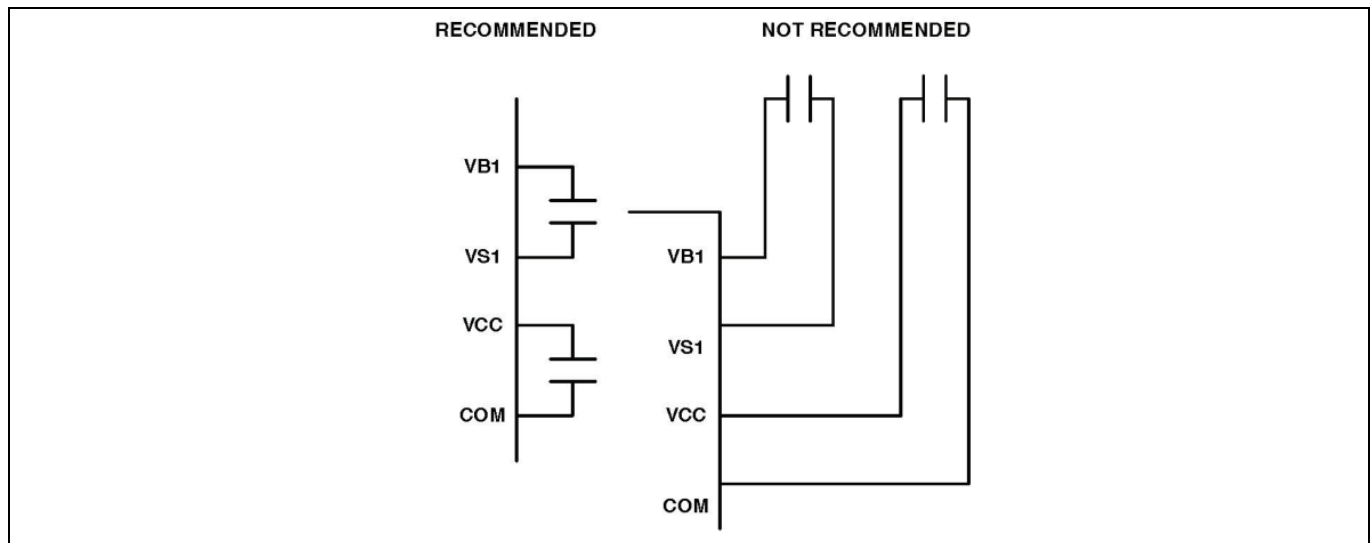


Figure 7 Decoupling Capacitor Location

Granted proper application of the above guidelines, the effects of VS undershoot will be minimized at source. If the level of undershoot is still considered too high, then some reduction of dv/dt may be necessary.

External snubbing and/or increasing gate drive resistance may be used to trade efficiency for lower switching rate. If the system will not tolerate this, then fast anti-parallel clamping diodes may be considered appropriate. HEXFRED diodes are ideal for this purpose.

Boosting VS Undershoot Immunity

8 Boosting VS Undershoot Immunity

If the key signals measured fall within specified limits under worst case conditions, then no further action should be necessary. However, in very noisy environments, where V_s undershoot remains excessive despite the measures above, then further steps may be taken to increase control IC tolerance. We recommend two different methods for improving undershoot immunity.

Method A:

A resistor between the V_s pin and the bridge center may be used to limit the current flow into the V_s pin during undershoot. This method is viable for resistor values of around 5 Ohms or less. Since the bootstrap capacitor charges through this resistor, as shown in figure 8, inadvertent shootthrough may occur at start-up if the value is too high. If there is a series gate resistor, this should be reduced in value so the net gate resistance of both high and low side transistors remains equal.

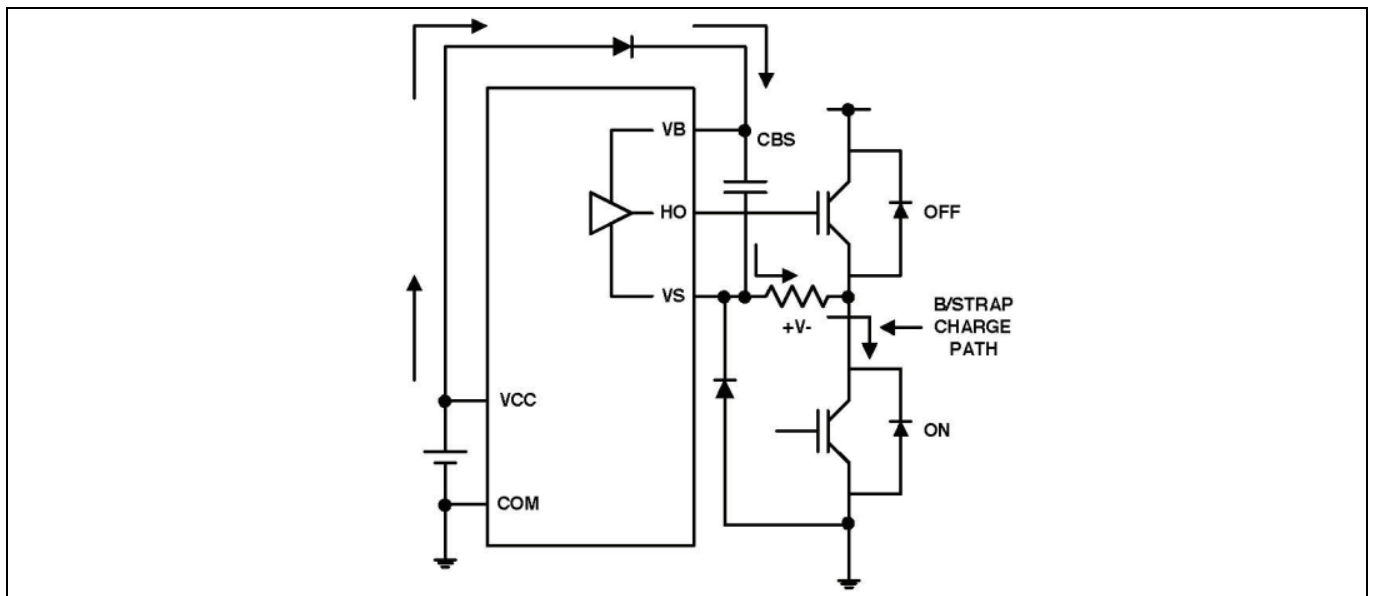


Figure 8 Boosting Immunity Method A

Method B:

By way of an alternative approach, we also recommend the insertion of a single resistor between COM and the low side source or emitter as depicted by figure 9. Since the boot strap capacitor is not charged through the resistor, this method grants flexibility to choose a higher resistance and afford greater protection to the control IC.

A resistor in this location has the effect of limiting peak current flow in the 600V diode D2 shown in figure 3. Again, drive symmetry requires that the total resistance in both gate drive circuits be equal, so the low-side gate resistor should be slightly reduced to accomplish this.

Boosting VS Undershoot Immunity

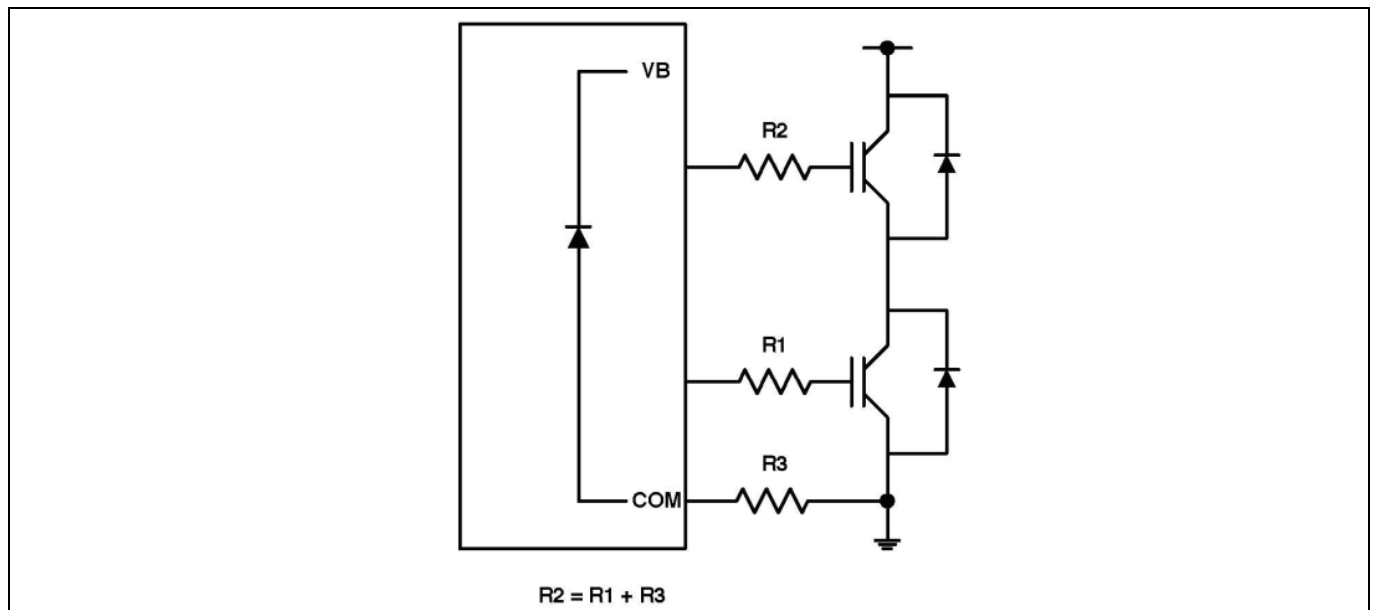


Figure 9 Boosting Immunity Method B

Note:

When using control ICs which do not have a separate logic ground, i.e. those which share COM for both input and out put ground references, either of the two methods discussed may be applied. However, care should be taken to ensure that logic inputs fall within the permitted levels.

APPENDIX 1: IR2110 Parasitic Diode Structure

9 APPENDIX 1: IR2110 Parasitic Diode Structure

The parasitic diode structure of the IR2110 control IC is shown in Figure 10. This is, in essence, a pictorial representation of our Absolute Maximum Ratings table.

The IR2110 has separate logic and output supply rails, however, these rails are combined in some control IC types due to pinning restrictions.

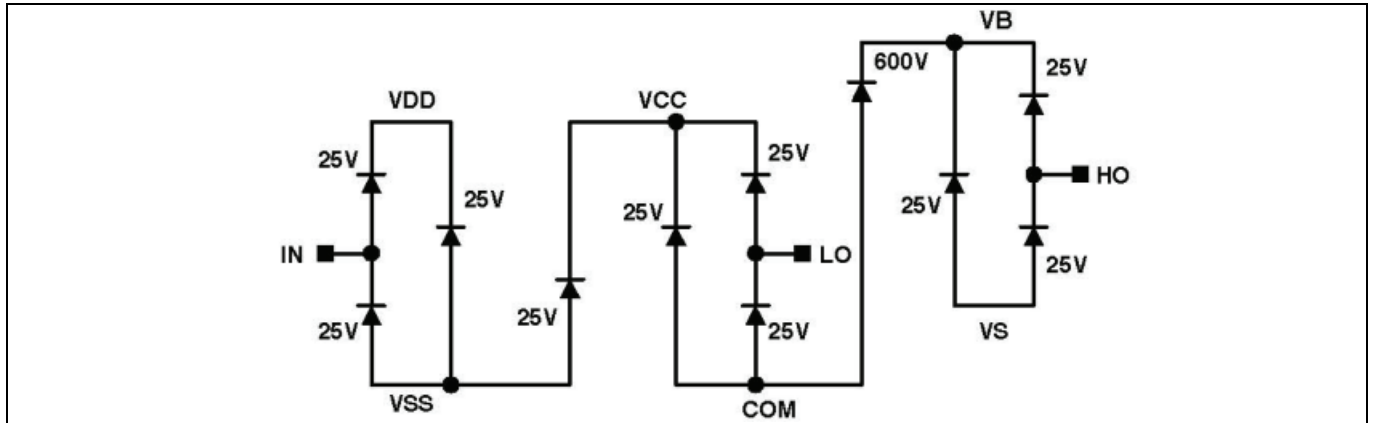


Figure 10 IR2110 Parasitic Diode Structure

References

References

- [1] IR2110 datasheet: https://www.infineon.com/dgdl/Infineon-IR2110-DataSheet-v01_00-EN.pdf?fileId=5546d462533600a4015355c80333167e
- [2] Gate driver reference page: <https://www.infineon.com/cms/en/product/power/gate-driver-ics/>

Revision history

Revision history

Document revision	Date	Description of changes
Revision 1.00		Initial Version
Revision 1.01	2024-11-20	Document Template Change

Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

Edition 2024-11-20

Published by

Infineon Technologies AG

81726 Munich, Germany

**© 2024 Infineon Technologies AG.
All Rights Reserved.**

Do you have a question about this document?

Email: erratum@infineon.com

Document reference

Important notice

The information contained in this application note is given as a hint for the implementation of the product only and shall in no event be regarded as a description or warranty of a certain functionality, condition or quality of the product. Before implementation of the product, the recipient of this application note must verify any function and other technical information given herein in the real application. Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind (including without limitation warranties of non-infringement of intellectual property rights of any third party) with respect to any and all information given in this application note.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

Warnings

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.