Design of 200 W boost PFC plus HB LLC resonant converter with IR1155, IRS27952 and IR11688

Application note

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About this document

Scope and purpose

The purpose of this document is to provide a comprehensive functional description of and guide to using the DEMO_200W_12VDC two-stage PFC + LLC resonant converter evaluation board based on the following ICs: IR1155S, IRS27952, IRS11688 and ICE5QR0680AG. The following document describes its operation and covers technical aspects essential to the design process, including calculation of external component values, MOSFET selection and PCB layout optimization, as well as additional protection circuitry. Test results and waveforms are also included.

Intended audience

Power supply design engineers, applications engineers, students.

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1 Introduction

The DEMO_200W_12VDC_LLC evaluation board is an off-line isolated power supply designed to provide a 12 V DC output up to amaximum load of 16 A operating from a 50/60 Hz AC-line input voltage between 85 and 265 V AC. The output of this evaluation board is protected against over-load and short-circuit. An over-voltage protection circuit is also included to limit the output voltage. At light loads. This application note gives a detailed description of a 192 W (12 V/16 A) two-stage isolated constant voltage regulated PFC boost plus resonant LLC half-bridge SMPS evaluation board with synchronous rectification based on the IR1155, IRS27952 and IR11688 controllers. Detailed test results and operating waveforms are provided. The board meets an average efficiency of at least 89 percent to meet the European Code of Conduct (EU COC) and US Department of Energy (US DOE) standards for 25 percent, 50 percent, 75 percent and 100 percent loads.

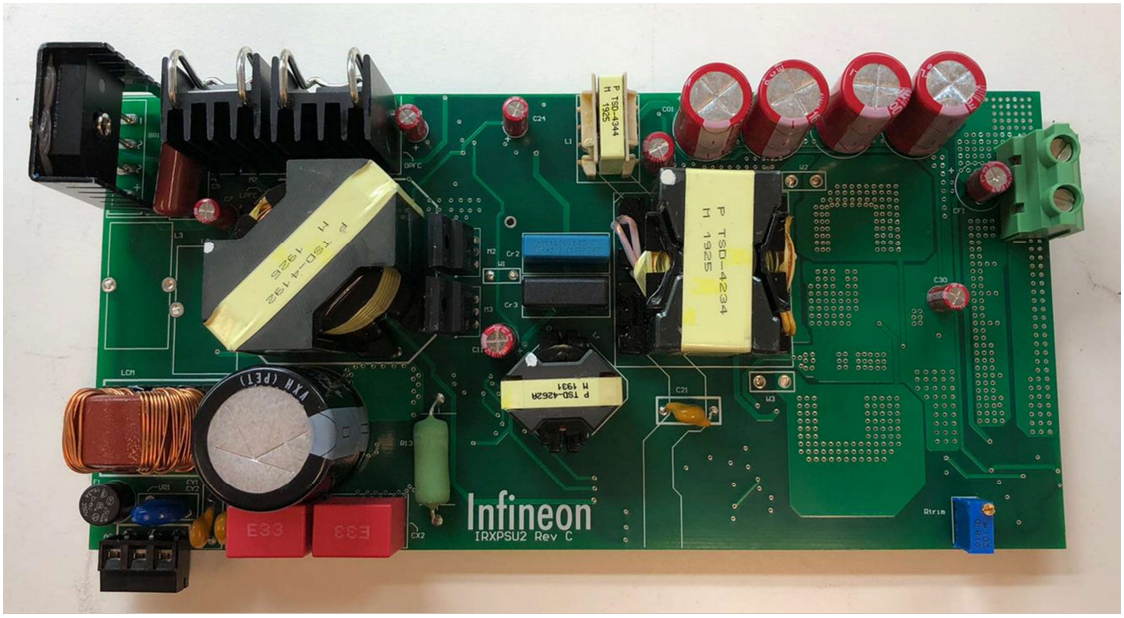


Figure 1 DEMO_200W_12VDC_LLC two-stage PFC boost + LLC resonant converter demo board (top view)

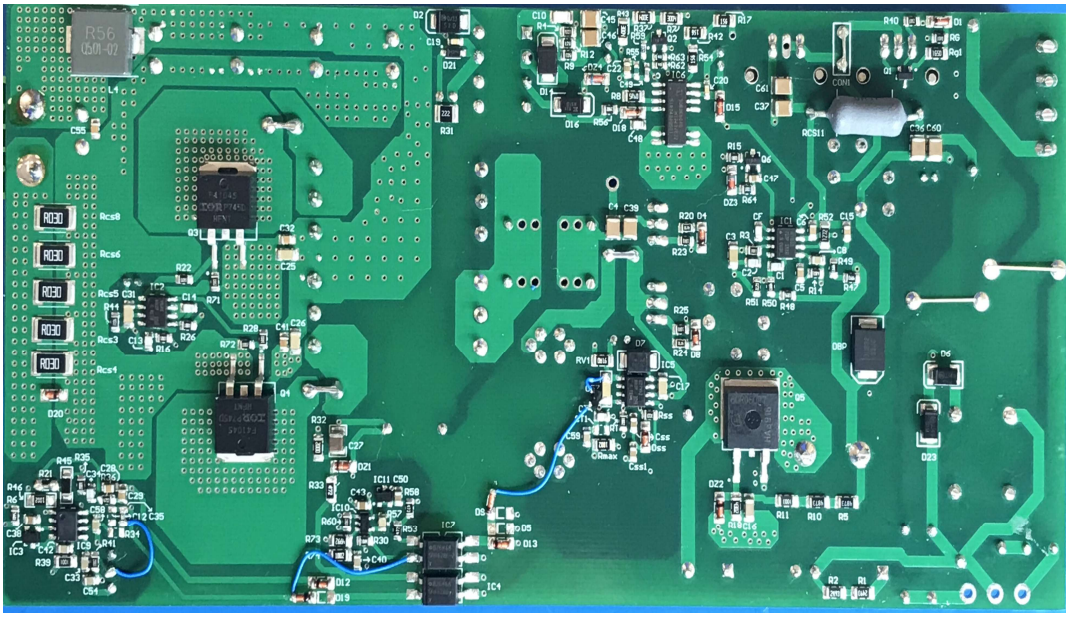


Figure 2 **DEMO_200W_12VDC_LLC two-stage PFC boost + LLC resonant converter demo board (bottom view)**

2 Evaluation board specifications

Input and output at normal operation

- AC input voltage 85 to 265 V_{RMS} (55 to 65 Hz)
- Output voltage 12 V
- Output current 16 A
- Maximum output continuous power 192 W
- PF greater than 0.9 at maximum load, 85 V AC to 265 V AC input voltage
- Total Harmonic Distortion (iTHD) less than 20 percent at maximum load, to 265 V_{RMS} input voltage
- Average four-point efficiency greater than 89 percent at 120 and 230 V_{RMS} input voltage
- Start-up time to reach the secondary nominal output voltage during full-load condition at 120 and 230 V_{RMS} input voltage less than 300 ms

Protection features

- Output Over-Voltage Protection (OVP) at V_{OUT} less than or equal to 16 V
- Over-Current Protection (OCP) at 19 A, hiccup mode
- Short-Circuit Protection (SCP), hiccup mode
- Brown-out protection, shut-down at 60 to 65 V_{RMS}, start-up at 75 to 80 V_{RMS} AC input voltages

No-load operation

- Burst mode during no-load condition
- Maximum power loss during no-load condition is 1 W at 120 and 230 V_{RMS} input voltage

Maximum component temperature

In an ambient temperature of 30°C, the maximum allowed component temperatures are as follows:

- Resistors less than 100°C
- Ceramic capacitors, film capacitors and electrolytic capacitors less than 100°C
- PFC, Flyback, LLC transformers less than 100°C
- MOSFET transistors and diodes less than 100°C
- ICs less than 100°C

Dimensions of evaluation board

Maximum width 7.66 inches (194.7 mm), maximum length 3.66 inches (93.04 mm).

WARNING!

The board should be tested only by qualified engineers and technicians.

3 Schematics

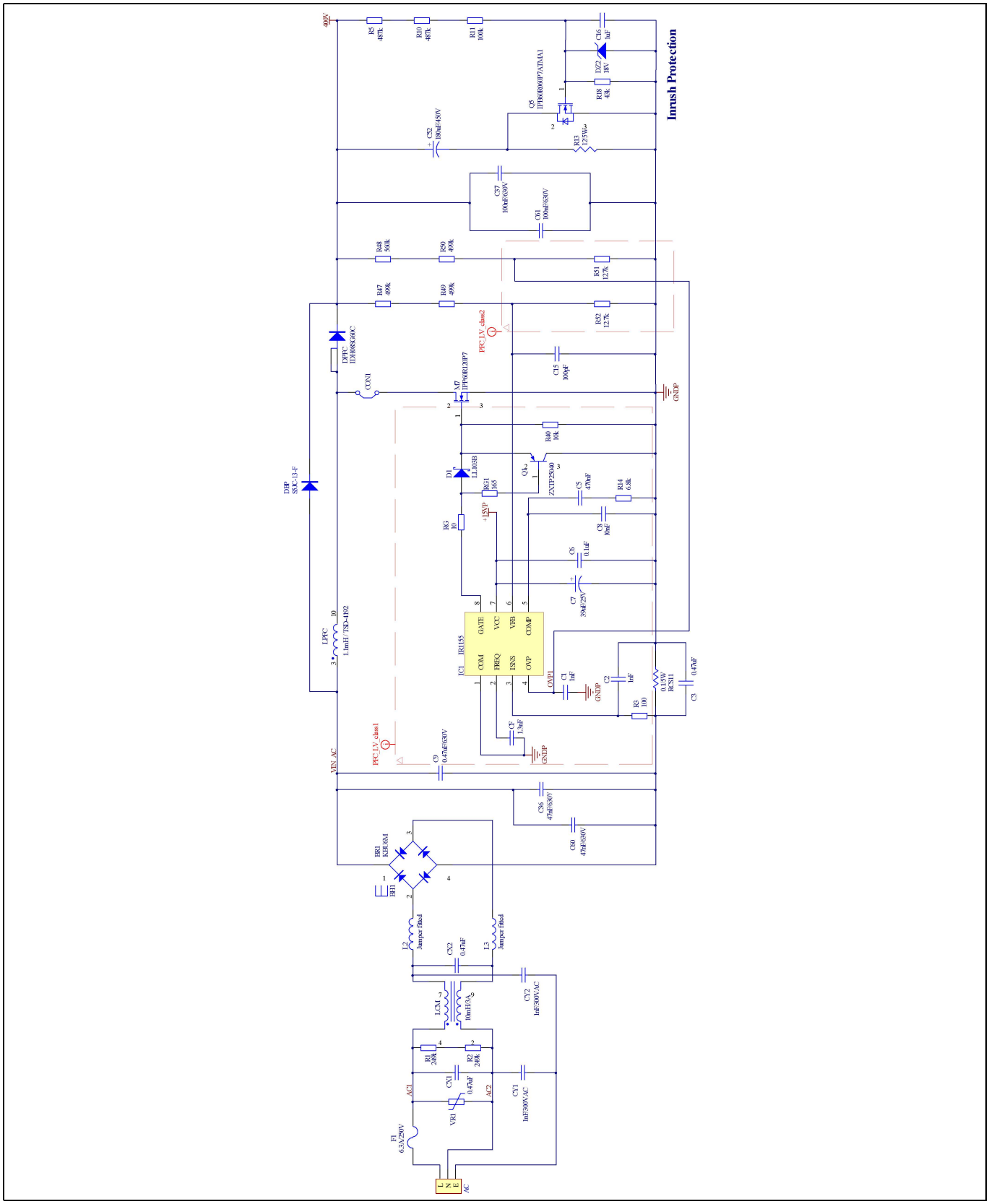


Figure 3 Front-end PFC boost converter

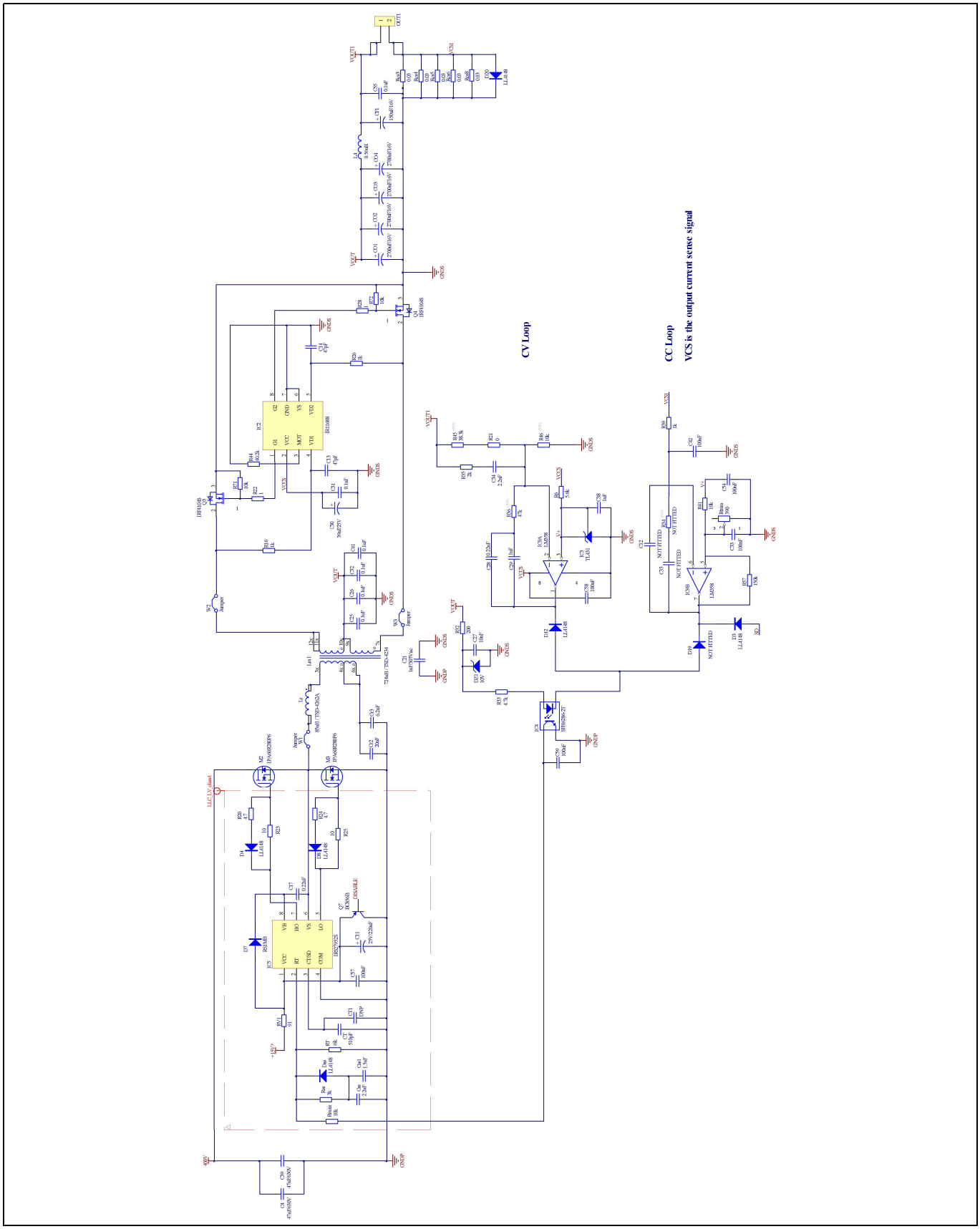


Figure 4 Second-stage LLC resonant converter

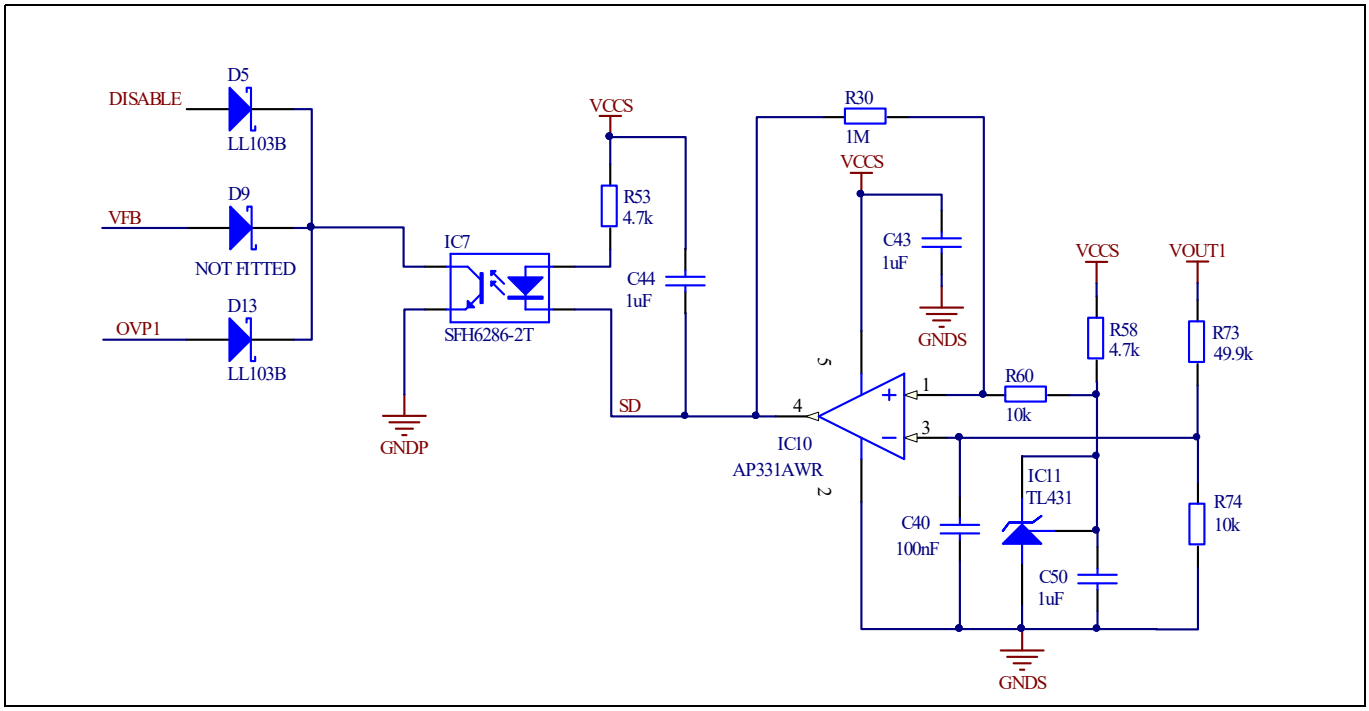


Figure 5 Burst mode and over-voltage protection circuit of LLC

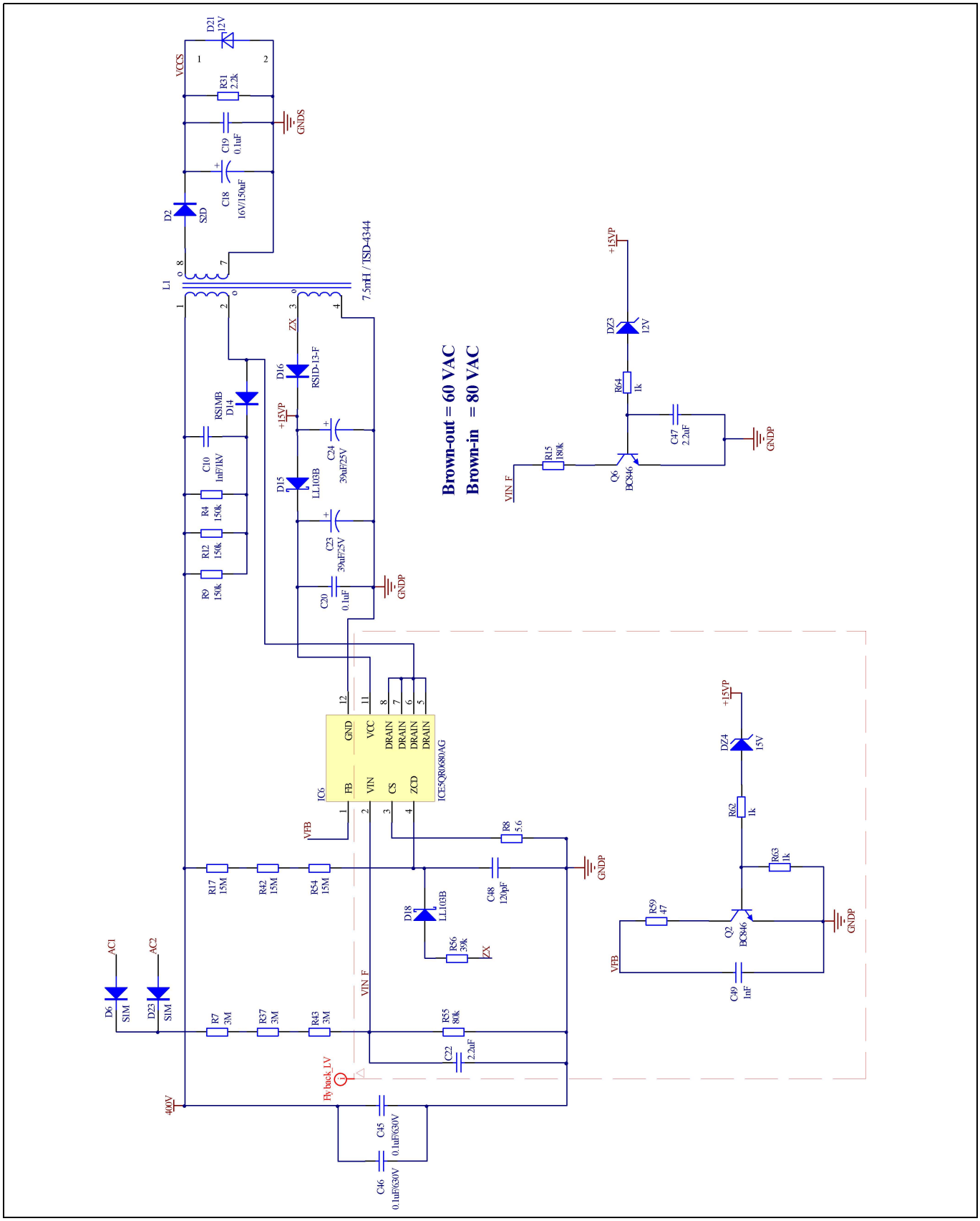


Figure 6 Auxiliary flyback power supply

4 PFC section

DEMO_200W_12VDC_LLC is a two-stage topology power converter demo board based on a PFC boost pre-regulator followed by a half-bridge LLC resonant converter. It provides a constant voltage output of 12 V over a wide AC-line voltage input range with high power factor and low total harmonic distortion of the line input current (iTHD). The evaluation board has a 12 V DC output up to 16 A and AC-line input voltage range between 85 and 265 V AC 50/60 Hz.

Many electronic appliances incorporate Switch Mode Power Supplies (SMPS), which traditionally include capacitive line filtering circuitry followed by a bridge rectifier and bulk capacitor to provide a DC bus voltage to supply a DC-DC converter. Without PFC circuitry such an SMPS draws a high peak current at the voltage peak and almost no current over the remainder of the cycle, resulting in a typical power factor of around 0.5 containing high THD. Low power factor leads to the circulation of RMS current greater than that necessary to perform the required work. This excess current flows in the conductors, forcing utility companies to oversize their distribution networks. In some countries the utility companies charge their end users in the event that the annual amount of reactive power exceeds a certain value [4]. PFC circuitry is often added to enable the appliance to draw an almost sinusoidal current from the AC-line with negligible phase shift that has very low harmonic distortion. This provides the best possible load for the power transmission grid so that power may be supplied without additional conduction losses in transmission lines or burden on transformers and generators.

Power factor consists of two distinct components – distortion and phase displacement [4].

1) *Displacement factor* (k_{ϕ}): This is the phase difference between input voltage and current (V AC and I_{AC}), which is defined as *cosine phi* (cos ϕ).

2) *Distortion factor* (k_d): This parameter quantifies the degree of distortion of the AC input current. A sinusoidal signal is composed purely of fundamental frequency with no harmonic content.

$$\text{Power Factor (PF)} = \frac{I_{1,rms}}{I_{rms}} \text{Cos}\phi = k_d \cdot k_{\phi}$$

Where k_{ϕ} = cos ϕ is called the displacement factor where ϕ represents the displacement angle between voltage and current fundamentals, and $k_d = \frac{I_{1,rms}}{I_{rms}}$ is called the distortion factor. $I_{1,rms}$ is the RMS amplitude of the fundamental and I_{rms} is the total RMS value of the complete current signal. THD of the current is often referred to as iTHD to differentiate it from the voltage THD. The line voltage should remain sinusoidal.[1]

PFC shapes the input current of the power supply, causing it to be in synchronization with the mains voltage. In an ideal PFC circuit the input current follows the input voltage as in a purely resistive load with no input current harmonics [6]. Although active PFC may be achieved with several topologies, the boost converter (Figure 7) is the most popular solution for the following reasons:

- The input current of the boost converter is continuous, as opposed to the discontinuous input current of the buck, buck-boost or flyback topologies. The continuous input current is much easier to filter, which is a major advantage of this topology because any additional filtering needed at the converter input would increase cost and reduce the power factor due to capacitive loading of the line. A discontinuous input current waveform would also increase EMI, requiring further filtering.
- A buck converter is not suitable, because when the input voltage falls below the output voltage, no power can be transferred, creating a drop-out period depending on the output voltage, which inevitably results in low power factor and high iTHD.

[1] Power factor and iTHD measurements should be carried out using a pure sinewave AC source, otherwise voltage distortion would produce inaccurate results.

- The buck-boost converter produces an output which is negative and not preferred. The input current is not continuous, and additionally the MOSFET has high voltage stress ($V_{in} + V_o$).
- The flyback converter is able provide isolation, though this is usually done in the DC-DC stage and is therefore unnecessary in the PFC stage. It also has a discontinuous input current and requires more components and larger magnetics, leading to a higher Bill of Materials (BOM) cost. The front-end stage in this demo board is a PFC boost converter topology, which operates in Continuous Conduction Mode (CCM) using average current mode control.

4.1 PFC modes of operation

The different operating modes are briefly described as follows: Continuous Conduction Mode (CCM), Discontinuous Conduction Mode (DCM) and Critical Conduction Mode (CrCM).[1] Figure 8 illustrates the boost inductor current waveforms and the average input current in the three operating modes. DCM operation may appear to be simpler than CrCM, since it can operate at constant switching frequency; however, it has a higher peak input current than CrCM, which in turn has a higher peak than CCM. DCM is therefore less efficient and also requires the most filtering.

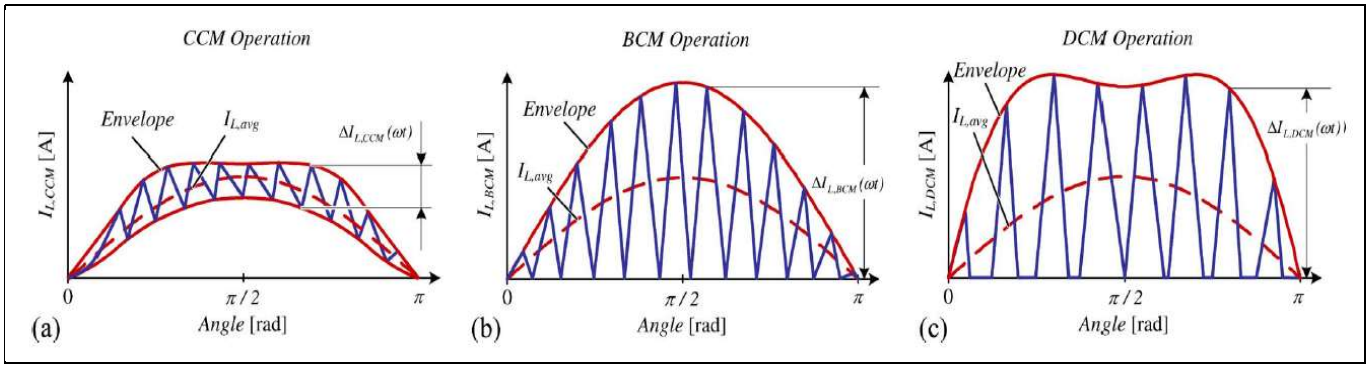


Figure 7 Boost inductor current for different operating modes: (a) CCM, (b) CrCM, (c) DCM [7]

In CrCM, the inductor current is forced to operate at the boundary between CCM and DCM. CrCM generally uses constant on-time control in which the switching frequency changes during the AC-line cycle. Each new switching cycle begins when the energy stored in the inductor has been fully transferred to the output, therefore the off-time varies during the AC-line cycle, becoming longer at the peak [8]. The reset time for the inductor varies, causing the frequency to adjust in order to maintain the boundary mode operation. CrCM requires the controller to sense the inductor current zero crossing in order to trigger the start of the next switching cycle. The inductor current ripple (or the peak current) in CrCM is twice the average value, which increases the MOSFET RMS currents and turn-off current. However, since every switching cycle starts at zero current and usually with ZVS operation, turn-on loss of the MOSFET is eliminated. Also, since the output diode turns off at zero current, reverse recovery losses and EMI are eliminated as well. On balance the high input ripple current and its impact on the input EMI filter tends to eliminate the benefit of CrCM mode for higher-power designs unless interleaved stages are used to reduce the input HF current ripple, which can enable a highly efficient design but at substantially higher cost [6]. The main differences between CCM and CrCM relate to the current ripple profile and switching frequency, which affect RMS current, switching power losses and the filter design.

CCM operation requires a higher inductor value compared to CrCM; however, the core loss and the winding loss are lower due to the lower peak and RMS currents. In the case of CCM PFC, the inductor current ripple is typically designed to be 20 to 40 percent of the average input current.

[1] Critical conduction mode is sometimes referred to in the literature as “boundary” mode (BCM or BM) or “transition” mode (TM).

This has several advantages:

- Peak current is lower and the RMS current factor with a trapezoidal waveform is reduced compared to a triangular waveform, thereby reducing conduction losses.
- Turn-off losses are lower due to switch-off at lower peak current.
- The HF ripple current, which needs to be smoothed by the input EMI filter, is much lower in amplitude.

On the other hand, CCM encounters the turn-on losses in the MOSFET, which can be exacerbated by the output diode reverse recovery loss due to reverse recovery charge Qrr. For this reason ultra-fast recovery silicon diodes or silicon carbide Schottky diodes with extremely low Qrr are necessary for CCM mode. In conclusion, for low-power applications the CrCM boost PFC converter has the advantage of power saving and improving power density up to 100 to 150 W. Above this range CCM starts to become a better option for medium- to high-power applications.

5 IR1155S functional overview

The µPFC IR1155S PFC IC is based on Infineon's proprietary One Cycle Control (OCC) technique, which provides high power factor, low THD and an excellent DC bus regulation while enabling reduction of component count, PCB area and design time when compared to traditional solutions. The IR1155S is a fixed-frequency PFC IC designed to operate in CCM with average current mode control. It incorporates programmable switching frequency, programmable soft-start, micro-power start-up current, and user-initiated micro-power sleep mode for compliance with standby energy standards with ultra-low bias currents for sensing pins. The switching frequency can be set from 48 kHz to 200 kHz. In addition it includes dedicated OVP, cycle-by-cycle peak current limit, Open-Loop Protection (OLP) and V_{CC} Under Voltage Lock-Out (UVLO).

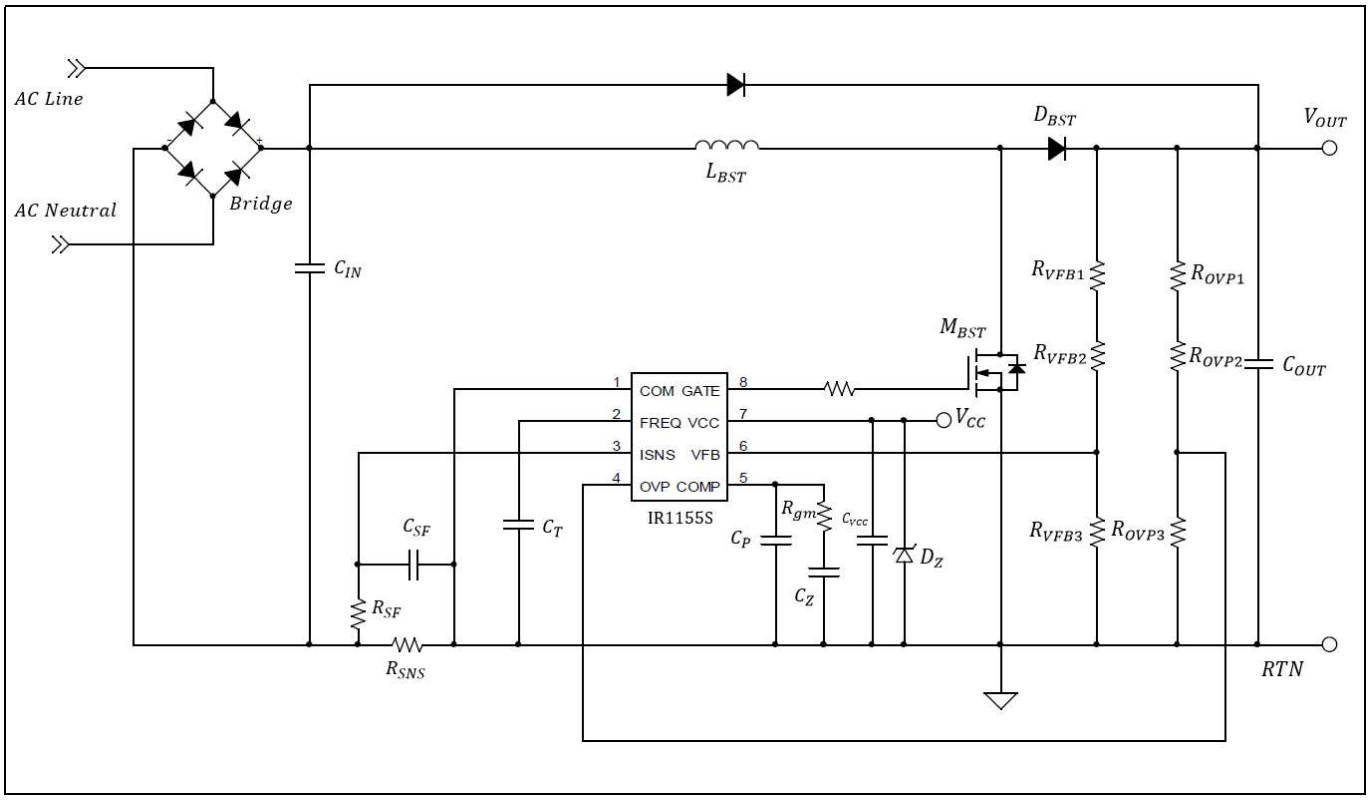
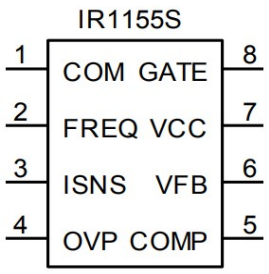


Figure 8 IR1155-based PFC boost converter

The diagram above shows the system application diagram of the IR1155S-based PFC converter. There are three input pins – VFB, COMP and ISNS – which provide the necessary signals to achieve PFC and maintain output voltage regulation. The functions of the above-mentioned inputs are as follows:

- VFB – provides DC output bus voltage feedback sensing for voltage regulation
- COMP – used for compensating the voltage feedback loop to set the correct transient response characteristics
- ISNS – provides sensing of the inductor current, which is used to determine the PFC switching duty cycle

Essentially, there are two control loops in the control algorithm: a slow outer voltage loop whose function is to maintain output voltage regulation, and a fast inner current loop whose function is to determine the instantaneous duty cycle for each switching cycle. The current-shaping function, i.e. PFC, is achieved primarily by the current loop. The voltage loop is responsible only for controlling the magnitude of the input current in order to maintain DC bus voltage regulation.



Pin	Name	Description
1	***COM***	Ground
2	***FREQ***	Frequency set
3	***ISNS***	Current sense
4	***OVP***	Output over-voltage detect/enable
5	***COMP***	Voltage loop compensation
6	***VFB***	Output voltage sense
7	***VCC***	IC supply voltage
8	***GATE***	Gate drive output

Figure 9 IR1155S pin assignments

5.1 Key features of the IR1155S

1. *Programmable oscillator*

The switching frequency of IR1155S is programmed by a capacitor (CT) connected from the FREQ pin to the IC ground. The switching frequency can be set in the range of 48 to 200 kHz with capacitor values ranging from 430 pF to 2 nF. A 200 µA constant current source $I_{(OSC(CHG))}$ is used to charge the capacitor voltage from $V_{(OSC(VAL))}$ (2 V typical) to $V_{(OSC(PK))}$ (4 V typical). Once the voltage at CT reaches the 4 V threshold, the charging current is disconnected and a 6.6 mA discharging current source $I_{(OSC(CHG))}$ is activated to discharge CT. When the voltage is discharged to 2 V, the discharging current is discontinued and the charging current source will be turned on again. In this way a sawtooth waveform is produced at the FREQ pin, as shown in figure 9. The rising slope of the sawtooth defines the maximum duty cycle of the GATE output, which is shown in figure 10. In the system the actual duty for each switching cycle is determined by the OCC modulator and may vary from minimum 0 percent to maximum 96~99 percent. The relationship between CT and the switching frequency is outlined in figure 11.

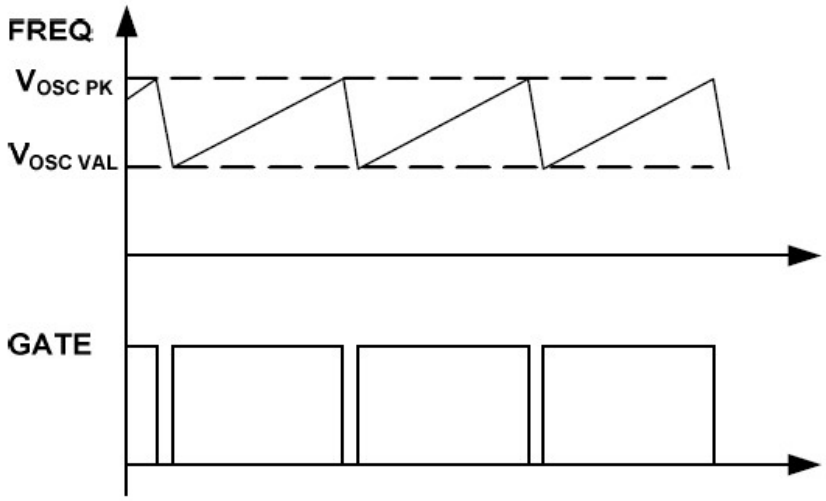


Figure 10 FREQ and GATE pin waveforms

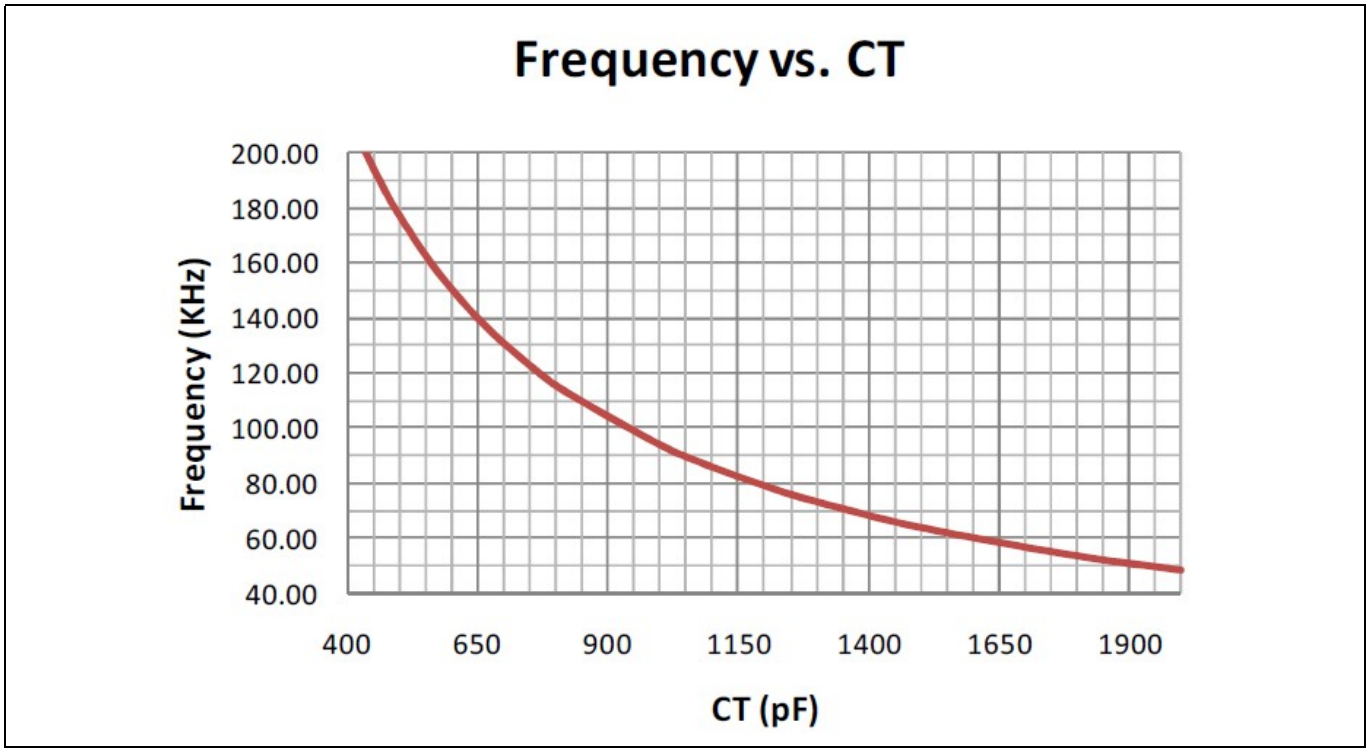


Figure 11 IR1155S programmable switching frequency

Using an external capacitor to set the frequency improves the oscillator noise immunity and also provides the option to synchronize the IR1155S to an external clock pulse. In this case, the clock should be a narrow pulse with 1~5 percent duty cycle. The duty cycle of the sync pulse defines the dead-time of the GATE output such that 1 percent sync duty-cycle results in 99 percent maximum PFC GATE output. For this reason, a smaller sync duty cycle is preferred to achieve lower THD. However, it is necessary for the minimum clock pulse to be longer than 100 ns to guarantee reliable operation. The amplitude of the sync signal should be higher than $V_{OSC(PK)}$.

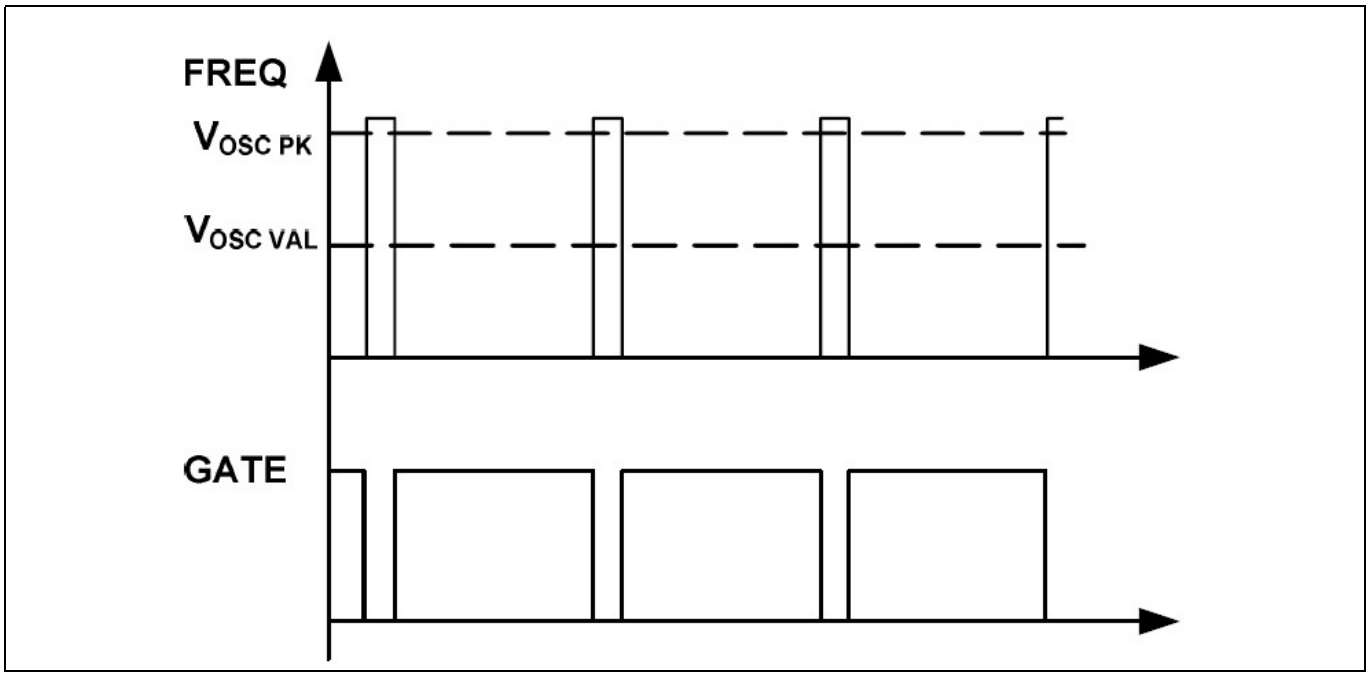


Figure 12 Synchronizing the IR1155S with an external signal

2. *Programmable soft-start*

The IR1155S facilitates programmability of the system soft-start time, allowing the designer freedom to choose the converter start-up time appropriate for the application. The soft-start time is defined as the time required for the V_{COMP} voltage to charge through its entire dynamic range, i.e. from 0 V to $V_{COMP, EFF}$. As a result, the soft-start time is dependent on the component values selected for compensation of the voltage loop at the COMP pin, primarily the CZ capacitor. As V_{COMP} voltage rises gradually, the IR1155S allows a higher and higher RMS current into the PFC converter. This controlled increase of the input current serves to reduce system component stress during start-up. During soft-start the controller is capable of full duty-cycle modulation (from zero to MAX DUTY), based on the instantaneous I_{SNS} signal from system Current Sense (CS) input. Furthermore, the IR1155S internal logic ensures that the soft-start capacitor is discharged when the IC enters sleep or standby mode in order to facilitate soft-start on restart.

3. *User-initiated micro-power sleep mode*

The IR1155S has an ENABLE function embedded in the OVP/EN pin. When this pin voltage is actively pulled below V_{SLEEP} threshold, the IC is pushed into sleep mode, where the current consumption is less than 200 µA even when V_{CC} is above the $V_{CC(ON)}$ threshold. The system designer can use an external logic-level signal to access the ENABLE feature, since the V_{SLEEP} threshold is so low. The IR1155S internal logic ensures that V_{COMP} is discharged before the IC enters sleep mode in order to enable soft-start on resumption of operation.

4. *Over-Voltage Protection (OVP)*

The OVP pin is a dedicated pin for OVP that also safeguards the system if there is a break in the VFB feedback loop due to the resistor divider becoming disconnected. An over-voltage fault is triggered when the OVP pin voltage exceeds the V_{OVP} threshold of 106.5 percent of V_{REF}. The IR1155S gate drive is immediately set low. The over-voltage fault is removed and gate drive re-enabled only when both pin voltages are below the $V_{OVP(RST)}$ threshold of 102.2 percent of V_{REF}. The OVP level can be programmed through an external resistor divider.

5. *Open-Loop Protection (OLP)*

The OLP ensures that the IC is restrained in standby mode if the VFB pin voltage has not exceeded or has dropped below the V_{OLP} threshold of 19 percent of V_{REF}. In standby mode, all internal circuitry of the IC remains biased, the gate drive is disabled and current consumption is in the low milliamp range. During start-up, if for some reason the voltage feedback loop is open, the IR1155S will remain in standby and not start, thus avoiding a potentially catastrophic failure.

6. *Cycle-by-cycle peak current limit protection (IPK LIMIT)*

The cycle-by-cycle peak current limit is triggered when the V_{ISNS} pin voltage exceeds the $V_{ISNS(PK)}$ threshold of -0.77 V (in magnitude). When this condition is encountered, the IC gate drive is immediately disabled and held in that state until the I_{SNS} pin voltage falls below $V_{ISNS(PK)}$. Even though the IR1155S operates based on average current mode control, the input to the peak current limit comparator is decoupled from the averaging circuit, thus enabling instantaneous cycle-by-cycle protection for peak current limitation.

7. V_{CC} UVLO

In the event that the voltage at the V_{CC} pin should drop below the V_{CC} UVLO turn-off threshold $V_{CC(UVLO)}$, the IC enters UVLO mode, the gate drive is terminated and the turn-on threshold $V_{CC(ON)}$ must again be exceeded in order to re-start the process. In UVLO mode, the current consumption is less than 175 µA.

6 PFC boost stage dimensioning

Table 1 PFC converter specifications

AC input voltage	85 to 264 V_{RMS}
Input line frequency	47 to 63 Hz
Nominal DC output voltage	400 V
Maximum output power	210 W
Power factor	0.99 at 120 V_{RMS}/210 W 0.99 at 230 V_{RMS}/210 W
Minimum output hold-up time	20 ms
Maximum soft-start time	40 ms
Switching frequency	70 kHz
Over-voltage protection	440 V

1. *Peak input current*

It is necessary to determine the maximum input currents (RMS and peak) from the specifications in table 1 before proceeding with detailed design of the PFC boost converter. The maximum input current condition occurs at the highest load and lowest line input voltage (210 W at 85 V AC). Assuming a nominal efficiency of 93 percent, the maximum input power can be determined:

$$P_{IN(MAX)} = \frac{P_{o(MAX)}}{\eta_{MIN}} = \frac{210\ W}{0.93} = 225.81\ W \quad [1]$$

From this, the maximum RMS AC-line current is then calculated:

$$I_{IN(RMS)\ MAX} = \frac{P_{o(MAX)}}{PF.\eta_{MIN}.V_{IN(RMS)MIN}} = \frac{210\ W}{0.99\ .0.93\ .85\ V} = 2.66\ A \quad [2]$$

The selection of the semiconductor components (bridge rectifier, boost switch and boost diode) is based on $I_{IN(RMS)MAX}$.

Assuming a pure sinusoidal input, the maximum peak AC-line current can then be calculated:

$$I_{IN(PK)\ MAX} = \frac{\sqrt{2}P_{IN(MAX)}}{V_{IN(RMS)MIN}} = \frac{\sqrt{2}\ .225.81\ W}{85\ V} = 3.76\ A \quad [3]$$

2. *Boost inductance*

The IR1155S is an average current mode controller. An on-chip RC filter is sized to effectively filter the boost inductor current ripple to generate a clean average current signal for sensing. The averaging function in the IC can accommodate a maximum limit of 40 percent inductor current ripple factor at maximum input current. The inductance has to be sized so that the ripple current factor is not more than 40 percent at maximum input current condition (at the peak of AC sinusoid).
This is because:

- Higher ripple current factors would interfere with the average current mode operation of the OCC algorithm in the IR1155S, leading to duty-cycle instabilities and pulse skipping, resulting in current distortion and sometimes even audible noise.

- Power devices are stressed with higher ripple currents, as the peak inductor current ($I_{L(PK)MAX}$) increases proportionately. In this calculation, an inductor current ripple factor of 25 percent is selected. The ripple current at the peak of the AC sinusoid at maximum input current is:

$$\Delta I_L = 0.25 \cdot I_{IN(PK)MAX} = 0.25\ .\ 3.757A = 0.939\ A \quad [4]$$

And, the peak inductor current is:

$$I_{\mathrm{L(PK)}\ MAX} = I_{IN(PK)MAX} + \frac{\Delta I_L}{2} = 3.757\ A + \frac{0.939\ \mathrm{A}}{2} = 4.227\ A \quad [5]$$

In order to determine the boost inductance, the power switching duty cycle at the peak of AC sinusoid (at lowest input line of 85 V AC) is required.

$$V_{IN(PK)MIN} = \sqrt{2}\ .V_{IN(RMS)MIN} = \sqrt{2} \cdot 85\mathrm{V} = 120.21\ \mathrm{V} \quad [6]$$

Based on the boost converter voltage conversion ratio:

$$D = \frac{(V_O - V_{IN(PK)MIN})}{V_O} = \frac{(395-120.21)}{395} = 0.717 \quad [7]$$

The boost inductance is then given by:

$$L_{BOOST} = \frac{V_{IN(PK)MIN}\ .D}{F_{SW}\ .\Delta I_L} = \frac{120.21\ V\ .\ 0.717}{70k\ .\ 0.939A} = 1.165\ mH \quad [8]$$

A value of 1.2 mH is selected for L_{BOOST} for this converter.

3. High-frequency input capacitor

The purpose of the High-Frequency (HF) capacitor is to supply the HF component of the inductor current (the ripple component) via the shortest possible loop. This has the advantage of acting like an EMI filter since it minimizes the HF current requirement from the AC-line. Typically a HF film capacitor with low ESL and high-voltage rating (630 V) is used.

HF input capacitor design is essentially a trade-off between:

- Sizing it sufficiently to minimize the noise injected back into the AC-line
- Making it small enough to avoid line current zero-crossing distortion (flattening)

The HF input capacitor is determined as follows:

$$C_{IN} = k_{\Delta I_L} \cdot \frac{I_{IN(RMS)MAX}}{2.\pi.F_{SW}\ .r.V_{IN(RMS)MIN}} \quad [9]$$

Where:

$k_{\Delta I_L}$ = inductor current ripple factor of 20 percent, as mentioned earlier
r = maximum HF input voltage ripple factor ($\Delta V_{IN}/V_{IN}$), assumed 6 percent

$$C_{IN} = k_{\Delta I_L} \cdot \frac{I_{IN(RMS)MAX}}{2.\pi.F_{SW}\ .r.V_{IN(RMS)MIN}} = 0.25 . \frac{2.662}{2.\pi.70k.6\%.85} = 296.7nF$$

A standard 330 nF, 630 V capacitor is selected for C_{IN} for this converter.

4. Output capacitor (C_{OUT})

Output capacitor sizing is based on the hold-up time requirement. For 20 ms hold-up time and minimum output voltage of 300 V the output capacitance is first calculated:

$$C_{OUT(MIN)} = \frac{2 \cdot P_O \cdot \Delta t}{{V_O}^2 - {V_{O(MIN)}}^2} = \frac{2.210.0.02}{395^2 - 350^2} = 250.6\ \mu F \quad [10]$$

Minimum capacitor value must be de-rated for capacitor tolerance (20 percent) to guarantee the minimum hold-up time.

$$C_{OUT} = \frac{C_{OUT(MIN)}}{1 - \Delta C_{TOL}} = \frac{250.6 \cdot 10^{-6}}{1 - 20\%} = 313\ \mu F \quad [11]$$

Based on the board testing done in the lab, a standard 180 μF, 450 V capacitor was sufficient for 20 ms hold-up time. RMS capacitor rating is:

$$I_{Crms} = I_{out} \cdot \sqrt{\frac{16 \cdot V_{out}}{3 \cdot \pi \cdot V_{acmin(dc)}} - 1} = 1.138\ A \quad [12]$$

7 IR1155S control circuit design

7.1 CS resistor (ISNS pin)

The IR1155S incorporates two levels of current limiting:

1. A “soft” current limit, which limits the duty cycle and causes the DC bus voltage to fold back, i.e. droop
2. A cycle-by-cycle “peak” current limit feature, which immediately terminates the current gate drive pulse once the ISNS pin voltage exceeds the $V_{ISNS(PK)}$ soft current limit

The COMP pin voltage is directly proportional to the RMS input current into the PFC converter, i.e. V_{COMP} is higher at higher RMS current. Clearly its magnitude is highest at maximum load P_{MAX} and minimum AC input voltage, $V_{IN(MIN)}$. The dynamic range of V_{COMP} is defined by $V_{COMP(EFF)}$ stated in the IR1155S datasheet. Once the V_{COMP} signal reaches $V_{COMP(EFF)}$ any system requirement causing an additional increase in current will cause the IC to respond by limiting the duty cycle and thereby causing the output voltage to drop. This is called “soft” current limit protection. The selection of R_{SNS} must ensure that soft current limit is not encountered at any of the allowable line and load conditions.

1. R_{SNS} calculation

The determination of R_{SNS} is performed at the system condition when the inductor current is highest at lowest input line ($V_{IN(MIN)}$) and highest load (P_{MAX}). The inductor current is highest at the peak of the AC sinusoid. The duty cycle required at the peak of AC sinusoid at $V_{IN(MIN)}$ = 85 V AC in order to regulate V_{OUT} = 388 V is:

$$D_{PEAK} = \frac{(V_O - \sqrt{2}V_{IN(RMS)MIN})}{V_O} = \frac{(395 - \sqrt{2}\cdot 85)}{395} = 0.696 \quad [13]$$

R_{SNS} selection should guarantee that:

i. PFC algorithm can deliver this duty cycle at the peak of AC sinusoid at $V_{IN(MIN)}$ and P_{MAX} condition
ii. Soft current limit is encountered whenever there is a further increase in demand for current while operating at $V_{IN(MIN)}$ and P_{MAX} condition. To do this, V_{ISNS} is calculated below:

$$V_{ISNS(MAX)} = \frac{V_{COMP(EFF)MIN}\cdot(1-D)}{g_{DC}} = \frac{4.6V\cdot(1-0.696)}{3.1} = 0.452\ V \quad [14]$$

Note: If the calculated $V_{ISNS(MAX)}$ is higher than the cycle-by-cycle peak over-current limit threshold of the IC, the $V_{ISNS(PK)}$ value should be used to determine R_{SNS}. In this example, $V_{ISNS(MAX)}$ is lower than the minimum $V_{ISNS(PK)}$ value specified in the datasheet (0.69 V), thus 0.47 V is used for R_{SNS} calculation.

Next the peak inductor current at maximum peak AC-line current, de-rated with an over-load factor (KOVL of 5 percent), is calculated.

$$I_{IN(PK)OVL} = I_{L(PK)MAX}.(1 + K_{OVL}) = 4.227\ .(1 + 0.05) = 4.438\ A \quad [15]$$

From this maximum current level and the required voltage on the CS pin, the maximum resistor value that can be used for the PFC converter is determined.

$$R_{SNS} = \frac{V_{SNS(MAX)}}{I_{IN(PK)OVL}} = \frac{0.452}{4.438} = 0.102\ \Omega \quad [16]$$

It is noted that even although IR1155S operates in average current mode it is still safer to use the peak inductor current for CS resistor design to guarantee avoidance of premature fold-back.

Power dissipation in the resistor is now calculated based on worst case RMS input current at minimum input voltage:

$$P_{RS} = I^2_{IN(RMS)MAX}.R_s = 2.662^2.0.102 = 0.721\,W \quad [17]$$

A standard 0.1 Ω/3 W resistor is selected for R_{SNS}, keeping in mind the inrush current at the initial turn-on of the power supply.

2. *Peak current limit*

The cycle-by-cycle peak current limit is reached when the V_{ISNS} pin voltage exceeds $V_{ISNS(PK)}$. For the PFC converter this limit is encountered whenever the inductor current exceeds the following:

$$I_{PK_LMT} = \frac{|-0.77|}{0.1} = 7.549\,A \quad [18]$$

It is clear that even though the IR1155S operates based on average current mode control, the input to the peak current limit comparator is decoupled from the averaging circuit, thus enabling instantaneous cycle-by-cycle protection for peak over-current.

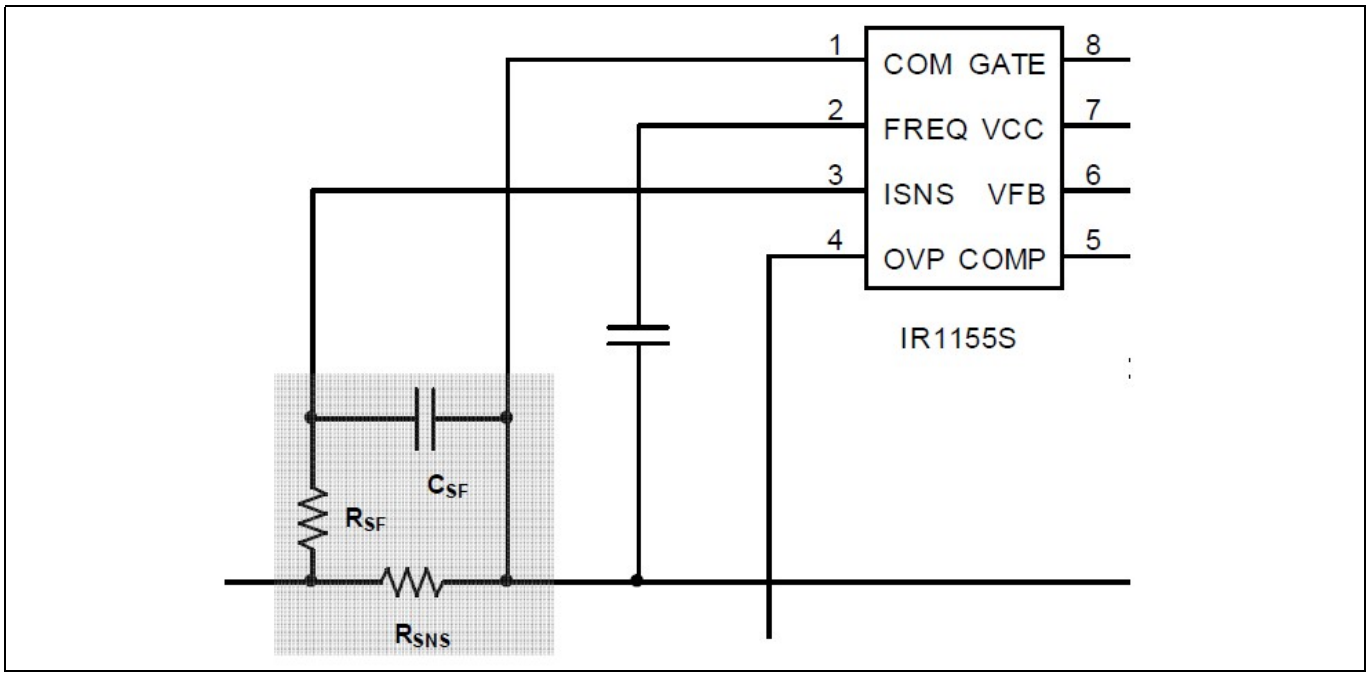


Figure 13 CS resistor and filtering

The CS signal is detected at the I_{SNS} pin of the IC using a current-limiting series resistor, R_{SF}. An external RC filtering for the I_{SNS} pin can be realized (though not necessarily for IR1155S) by adding a filter capacitor C_{SF} between the I_{SNS} pin and COM, as shown in figure 13. A corner frequency around 1 to 1.5 MHz will offer a safe compromise in terms of filtering, while maintaining the integrity of the CS signal for cycle-by-cycle peak OCP.

$$F_{PSF} = \frac{1}{2\cdot\pi\cdot R_{SF}.C_{SF}} \quad [19]$$

With R_{SF} = 100 Ω, we can use C_{SF} = 1 nF to obtain a cross-over frequency of 1.6 MHz. The input impedance of the CS amplifier is approximately 25 kΩ. The R_{SF} resistor will form a divider with this 25 kΩ resistor. For R_{SF} = 100 Ω it is noted that the accuracy of the CS voltage signal communicated to the IC is more than 99.5 percent.

3. *Output regulation voltage divider (VFB pin)*

The output regulation voltage of the PFC converter is set by voltage divider at the VFB pin (R_{FB1}, R_{FB2} and R_{FB3}). The total impedance of this divider network must be high enough to reduce power dissipation but low enough to keep the feedback voltage error (due to finite bias currents into the voltage error amplifier, which is less than 0.2 µA) negligible. Around 2 MΩ is an acceptable value for the total resistor divider impedance. A standard 499 kΩ, 1 percent tolerance resistor is selected for R_{FB1} and R_{FB2} for this converter. Then, R_{FB3} is determined based on error amplifier $V_{REF(TYP)}$ = 5 V and V_{OUT} = 388 V converter specification:

$$R_{FB3} = V_{REF}.\frac{(R_{FB1}+R_{FB})}{(V_{OUT}-V_{REF})} = 5.\frac{(499\,k+499\,k)}{(395-5)} = 12.79\ k\Omega \quad [20]$$

A standard resistor, R_{FB3} = 13.0 kΩ, 1 percent tolerance, is selected for this converter.

Power dissipation of divider resistors is given by the following.

$$P_{R_{FB1}} = P_{R_{FB}} = \frac{(V_O-V_{REF})^2}{2.(R_{FB1}+R_{FB2})} = \frac{(395-5)^2}{2(499\,k+499\,k)} = 76\ mW \quad [21]$$

4. *Dedicated OVP divider (OVP/EN pin)*

The IR1155S features a dedicated over-voltage sensing input pin (OVP/EN). The user can use the same resistor divider as calculated earlier with FB control. This will give a fixed OVP level, which is 106.5 percent of regulated output voltage. If a different over-voltage level is desired, a separated OVP resistor divider can be calculated. Here is an example:

A 499 kΩ, 1 percent tolerance resistor is selected for R_{OVP1} and R_{OVP2} for this converter. The OVP threshold is 420 V:

$$R_{OVP3} = \frac{1.065\,.V_{REF}.(R_{OVP1}+R_{OVP2})}{(V_{OV}-1.065.V_{REF})} = 1.065\frac{5\cdot(499k+487k)}{(420-1.065\,.5)} = 12.66\ k\Omega \quad [22]$$

The OVP reset point can be calculated:

$$V_{OVPREST} = \frac{1.022\,.V_{OV}}{1.065} = 1.022.\frac{420}{1.065} = 403.04\ V \quad [23]$$

5. *Timing capacitor (FREQ pin)*

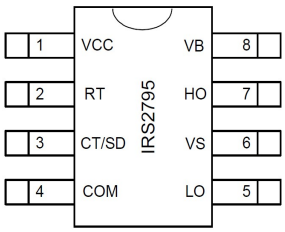
The timing capacitor C_T can be obtained per the following formula:

$$C_T = \frac{\left(\frac{1}{F_{SW}}-0.45\mu s\right).0.194mA}{2V} = \frac{\left(\frac{1}{70k}-0.45\ \mu s\right).0.194\ mA}{2} = 1.34\ nF \quad [24]$$

For 70 kHz target switching frequency, C_T is calculated as 1.34 nF. A standard 1.3 nF capacitor will be used, and it programs the switching frequency to 70 kHz.

8 IRS27952 functional overview

The IRS27952 is a self-oscillating half-bridge driver IC for resonant half-bridge DC-DC converter applications for use up to 600 V. It has a fixed 50 percent duty cycle (minus the dead-time) and very wide operating frequency range able to operate up to 500 kHz. The frequency can be adjusted between two set boundaries via an opto-isolator feedback circuit. The frequency range is programmed by external components connected to the RT and CT[1] pins, allowing flexibility to set the minimum and maximum operating frequencies as well as the frequency sweep at power-up for the soft-start function. The dead-time is also adjustable, determined by the CT capacitor. Programmable dead-time is essential to enable the designer to optimize the system with the minimum body-diode conduction time in M2 and M3 for higher efficiency under full load, while maintaining ZVS under a no-load condition. The IRS27952 also offers OCP using the on-state resistance of the low-side MOSFET sensed at the VS pin with a nominal threshold of 3 V. The gate drive outputs can be disabled by externally pulling the voltage at the CT pin below its enable voltage threshold. In this condition the IC enters sleep mode, in which minimal power is consumed. However great care must be taken when connecting any additional protection circuitry to the CT pin. Only an open-collector type comparator is suitable with defined fully on and off states. This is because any small leakage currents present at the CT node affect the operation of the oscillator and cause unstable operation and possible MOSFET failure.



Pin	Name	Description
1	***VCC***	Supply voltage
2	***RT***	Oscillator timing resistor
3	***CT/SD***	Oscillator timing capacitor/shut-down
4	***COM***	Ground
5	***LO***	Low-side gate drive
6	***VS***	High-side gate drive return/HV CS
7	***HO***	High-side gate drive
8	***VB***	High-side floating supply voltage

Figure 14 IRS27952 pin assignment

[1] CT refers to the capacitor connected to the CT/SD pin of the IRS27952 (see figure 14), not to be confused with CT of the IR1155 referred to in the previous section.

9 LLC resonant half-bridge converter operation

The increasing popularity of the LLC resonant converter in its half-bridge implementation is due to its high-efficiency, low switching noise and ability to achieve high power density. This topology is also the most attractive topology for front-end DC bus conversion. It utilizes the magnetizing inductance of the transformer to construct a complex resonant tank with buck and boost transfer characteristics in the soft-switching region. The typical power stage schematic for this topology is shown below:

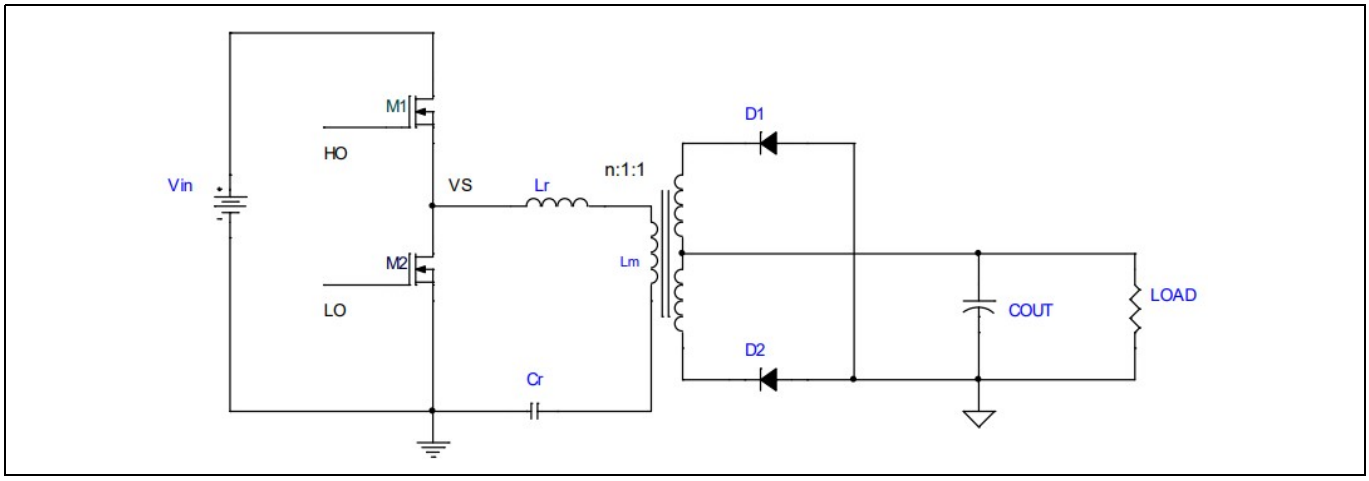


Figure 15 LLC resonant half-bridge converter basic elements

Devices M1 and M2 operate at 50 percent duty cycle, and the output voltage is regulated by varying the switching frequency of the converter. The converter has two resonant frequencies: a lower resonant frequency (given by L_m, L_r, C_r and the load), and a fixed higher-series resonant frequency F_{r1} (given by L_r and C_r only). The two bridge devices M1 and M2 can be soft-switched for the entire load range by operating the converter under inductive load mode (ZVS region). It can be either above or below the resonant frequency F_{r1}.

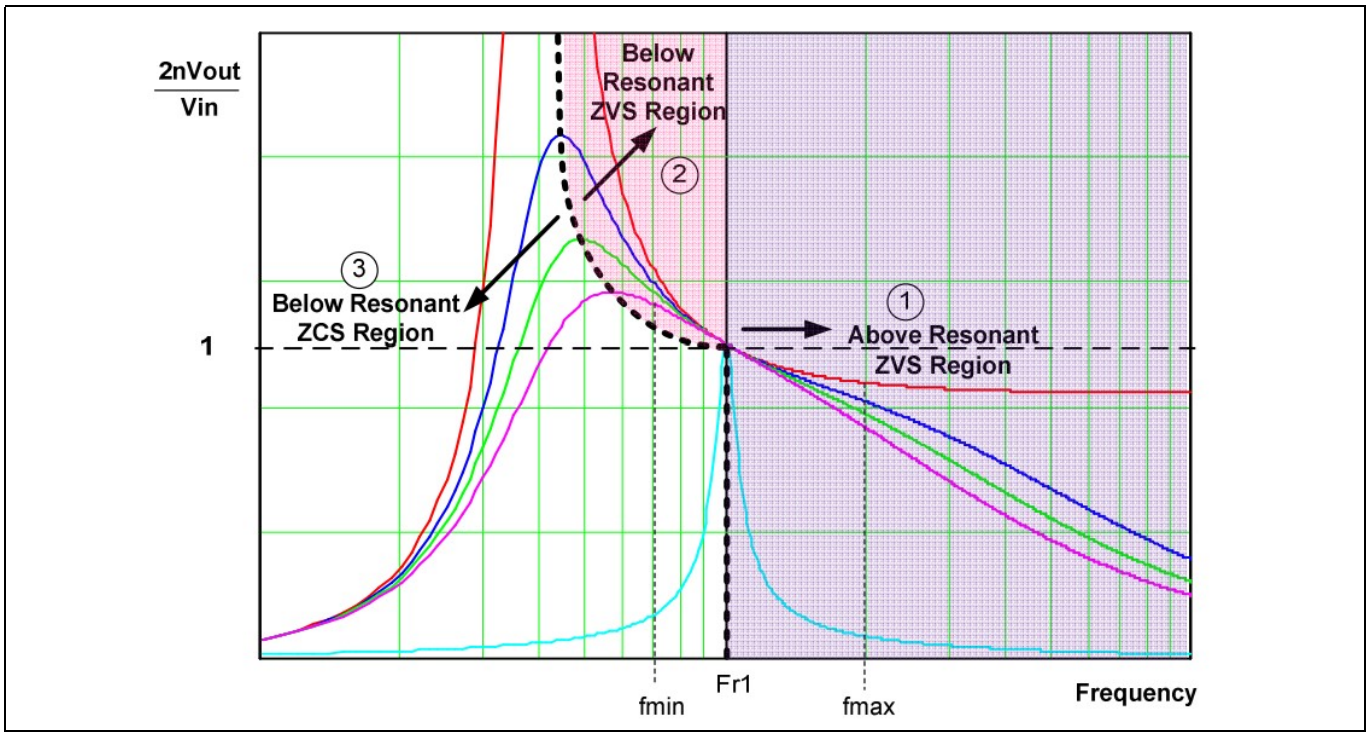


Figure 16 Frequency response of a typical LLC resonant converter

The characteristics of an LLC resonant converter can be divided into three regions based on the three different modes of operation. The first region is for a switching frequency above the resonant frequency F_{r1}:

$$F_{r1} = \frac{1}{2.\pi.\sqrt{L_r .C_r}} \quad [25]$$

In region 1 of figure 16 (the purple shaded area) the switching frequency is higher than resonant frequency F_{r1}. The converter operation is very similar to a series resonant converter. Here L_m does not resonate with the resonant capacitor C_r; it is clamped by the output voltage and acts as the load of the series resonant tank. This is the inductive load region and the converter is always under ZVS operation regardless of the load condition.

In region 2 (the pink shaded area) the switching frequency is higher than the lower resonant frequency but lower than F_{r1}. The lower resonant frequency varies with load so the boundary (the dotted line of the load gain curve) of region 2 and region 3 traces the peaks of the family of load vs. gain curves. In this complex region the LLC resonant operation can be divided into two time intervals; in the first time interval L_r resonates with C_r and L_m and is clamped by the output voltage. When the current in the resonant inductor L_r resonates back to the same level as the magnetizing current, L_m and C_r stop resonating. L_m now participates in the resonant operation and the second time interval begins. During this time interval the dominant resonant components become C_r and L_m in series with L_r. The ZVS operation in region 2 is guaranteed by operating the converter to the right side of the load gain curve. For a switching frequency below resonant frequency F_{r1} operation could fall in either region 2 or region 3 depending on the load condition.

The waveforms in figures 17, 18, 19 and 20 show the behavior of the system in each of the operating regions.

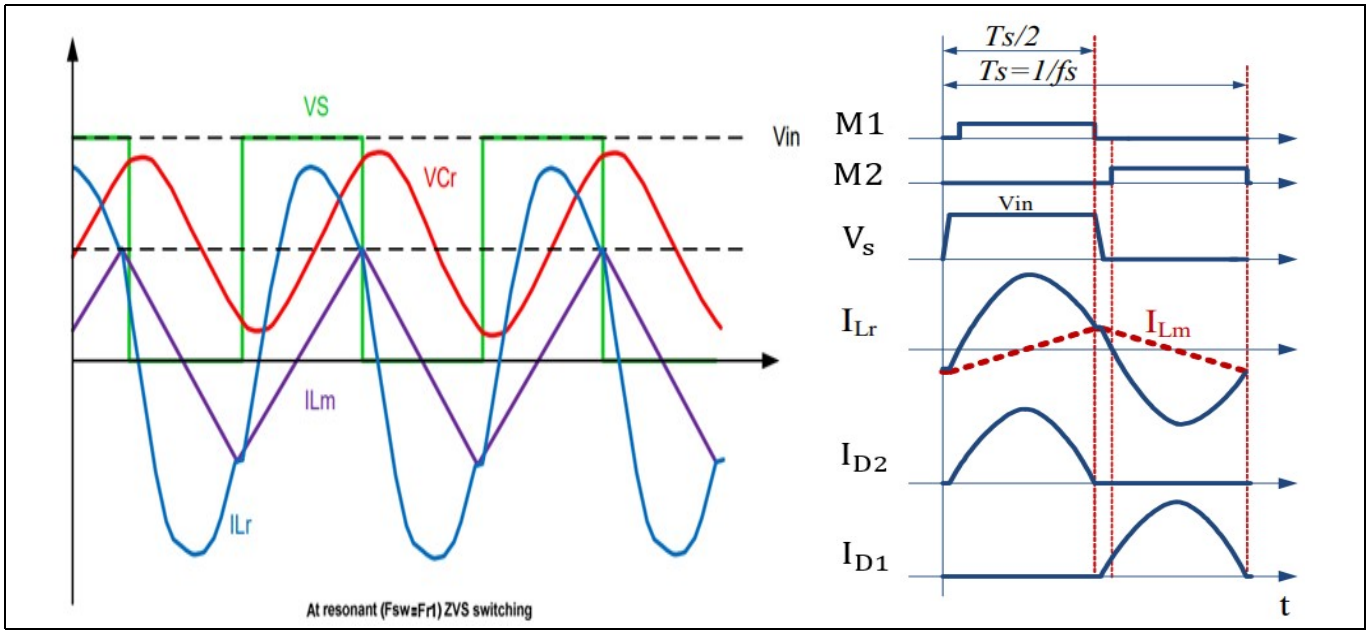


Figure 17 Operating waveforms at resonance with ZVS

When operating at resonance ($F_{sw} = F_{r1}$), each half switching cycle ($T_s/2$) contains a complete power delivery. During the first time interval $T_s/2$, L_r resonates with C_r and L_m is clamped by the output voltage and acts as the load of the series resonant tank. When the current in the resonant inductor L_r resonates back to the same level as the magnetizing current L_m, the L_r and the C_r stop resonating and L_m now participates in the resonant operation and the second time interval begins. During this time interval the dominant resonant components are C_r and L_m in series with L_r. At this time, the rectifier current in the secondary side of the transformer reaches zero. At this point the resonant tank has unity gain with optimum efficiency, and therefore the transformer turns ratio is designed such that the converter operates at this point at nominal input and output voltages.

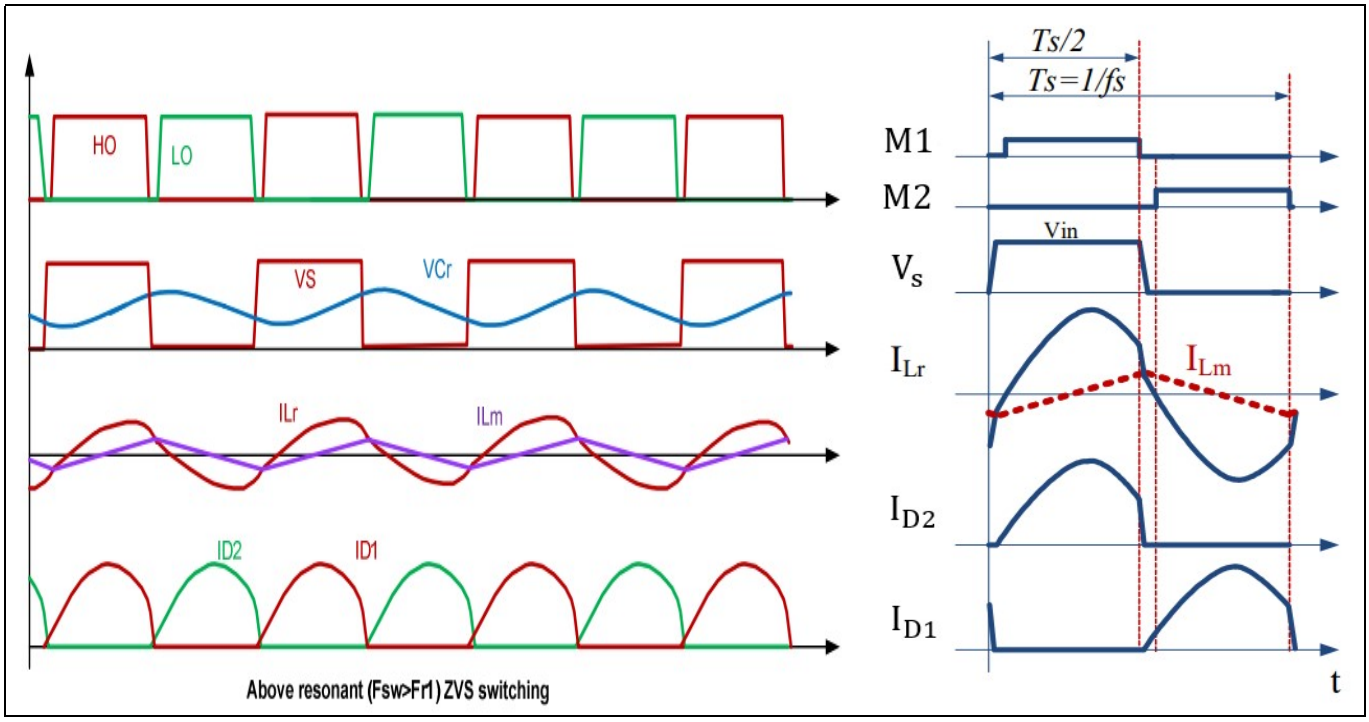


Figure 18 Operating waveforms above resonance with ZVS

Figure 18 shows the operation above the resonant frequency. Each half of the switching cycle contains a partial power delivery since the resonant half-cycle is not completed and is interrupted by the start of the other half of the switching cycle. The primary-side MOSFETs have therefore increased turn-off losses and secondary rectifier diodes are subject to hard commutation [3]. The converter operates in this mode at higher input voltage where a step-down gain or buck operation is required.

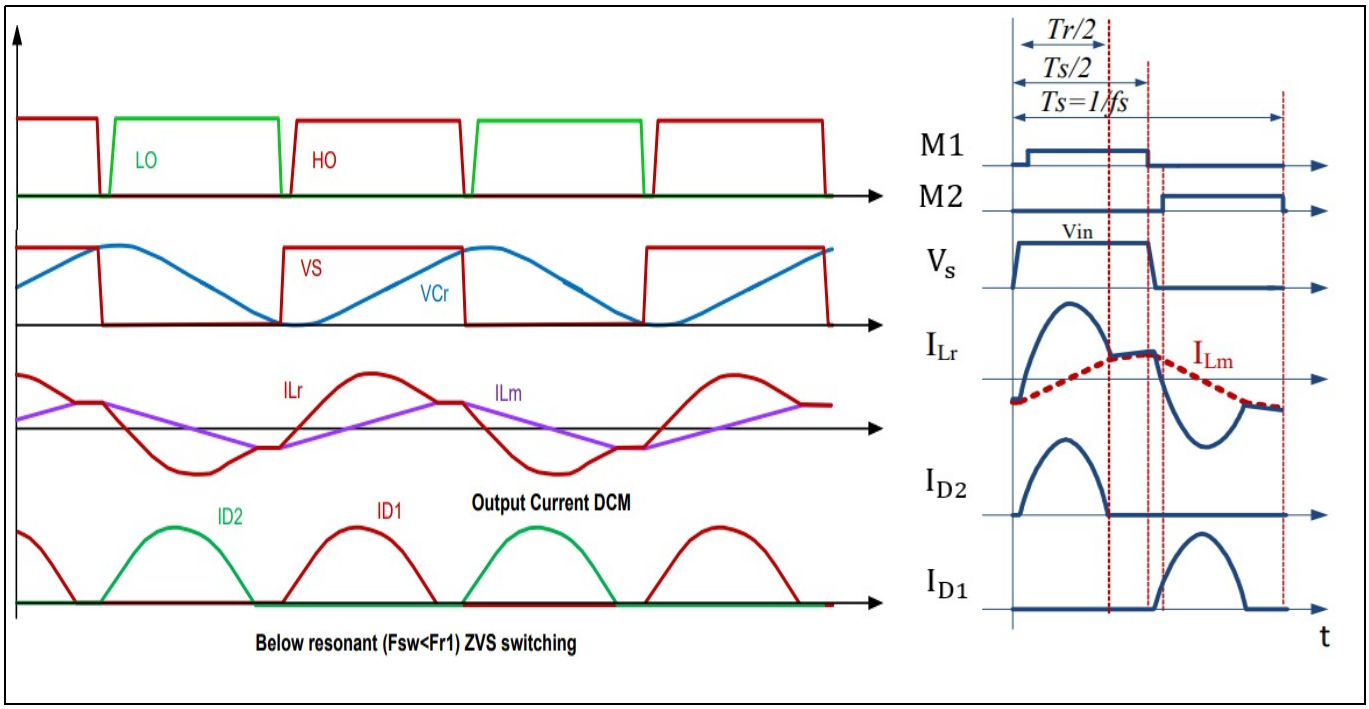


Figure 19 Operating waveforms below resonance with ZVS

Operating below resonance, each half of the switching cycle contains a power delivery operation. At the time when the resonant half-cycle has completed and resonant inductor current I_{Lr} reaches the magnetizing current, the freewheeling operation starts and carries on to the end of the switching half-cycle. The primary side now sees increased conduction losses due to the circulating energy. The converter operates in this mode at lower input voltage, where a step-up gain or boost operation is required. The waveforms shown in figure 19 indicate that the secondary rectifier diode currents transition from CCM to DCM when the switching frequency changes from above resonant ZVS to below resonant ZVS due to increasing load. The ripple voltage on the resonant capacitor C_r also increases in the below-resonant ZVS mode.

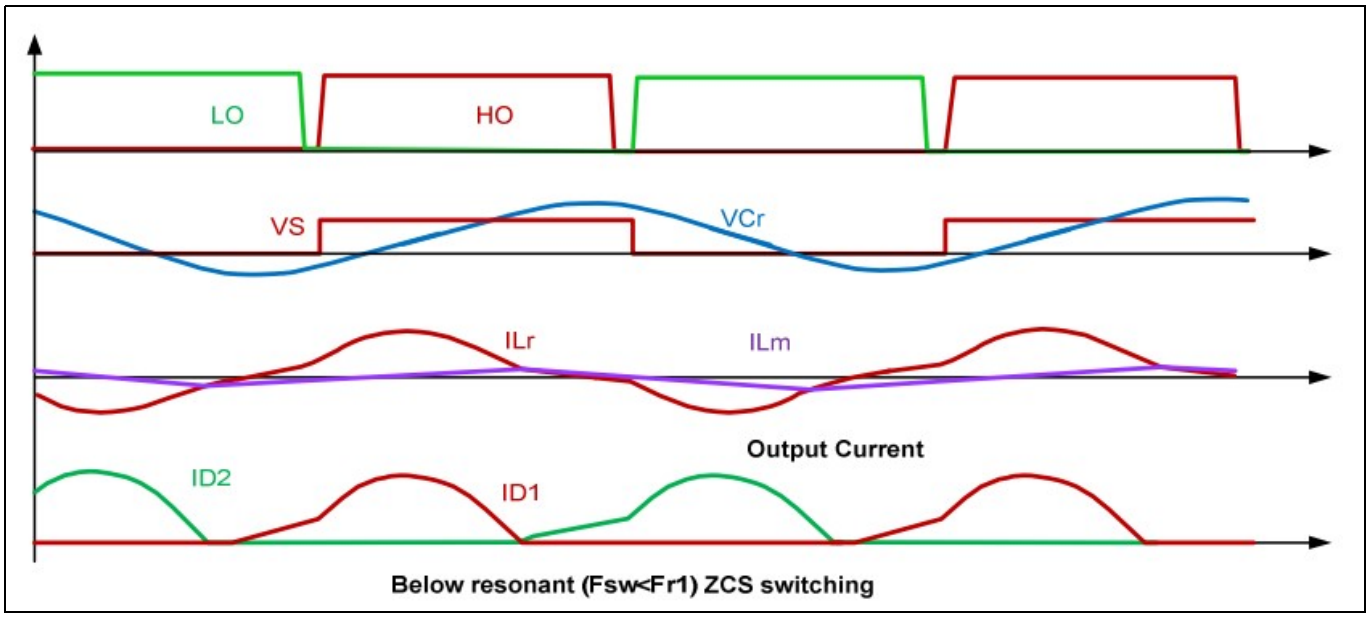


Figure 20 Operating waveforms below resonance with ZCS

In the ZCS region (F_{sw} less than F_{r1}), the LLC resonant converter operates in capacitive mode, and M1 and M2 are hard switching with high switching losses. For this reason ZCS operation should always be avoided.

9.1 Important points to consider when designing an LLC converter

1) As k (L_m/L_r ratio) increases, I_{Lm} decreases, Q decreases, voltage stress on C_r ($V_{cr(pk-pk)}$) is reduced, dead-time increases, no/light-load current decreases, light-load efficiency increases and frequency range increases.
2) Increasing k causes the gain peak to drop so the voltage regulation range is reduced because the frequency span increases.
3) Keeping the values of L_m and C_r unchanged and decreasing L_r reduces the gain.
4) When the switching frequency is lower than the resonant frequency, behavior is more like a parallel resonant converter with higher gain but with higher circulating currents (peak and RMS currents are higher). The conduction losses in the half-bridge MOSFETs and transformer are therefore higher. On the secondary side the synchronous rectifier MOSFETs will have ZVS turn-on and ZCS turn-off.
5) When the switching frequency is higher than the resonant frequency, the primary peak and RMS currents in the tank are lower. However, on the secondary side the rectifier MOSFET turns off with non-zero current, resulting in hard switching, so the reverse recovery (Q_{rr}) of the MOSFET shows up as a large ringing spike on the V_{DS} waveform.

For wide voltage range, narrow switching frequency is needed, which means lower k ratio and lower L_r/C_r. Efficiency versus voltage regulation range is a trade-off.

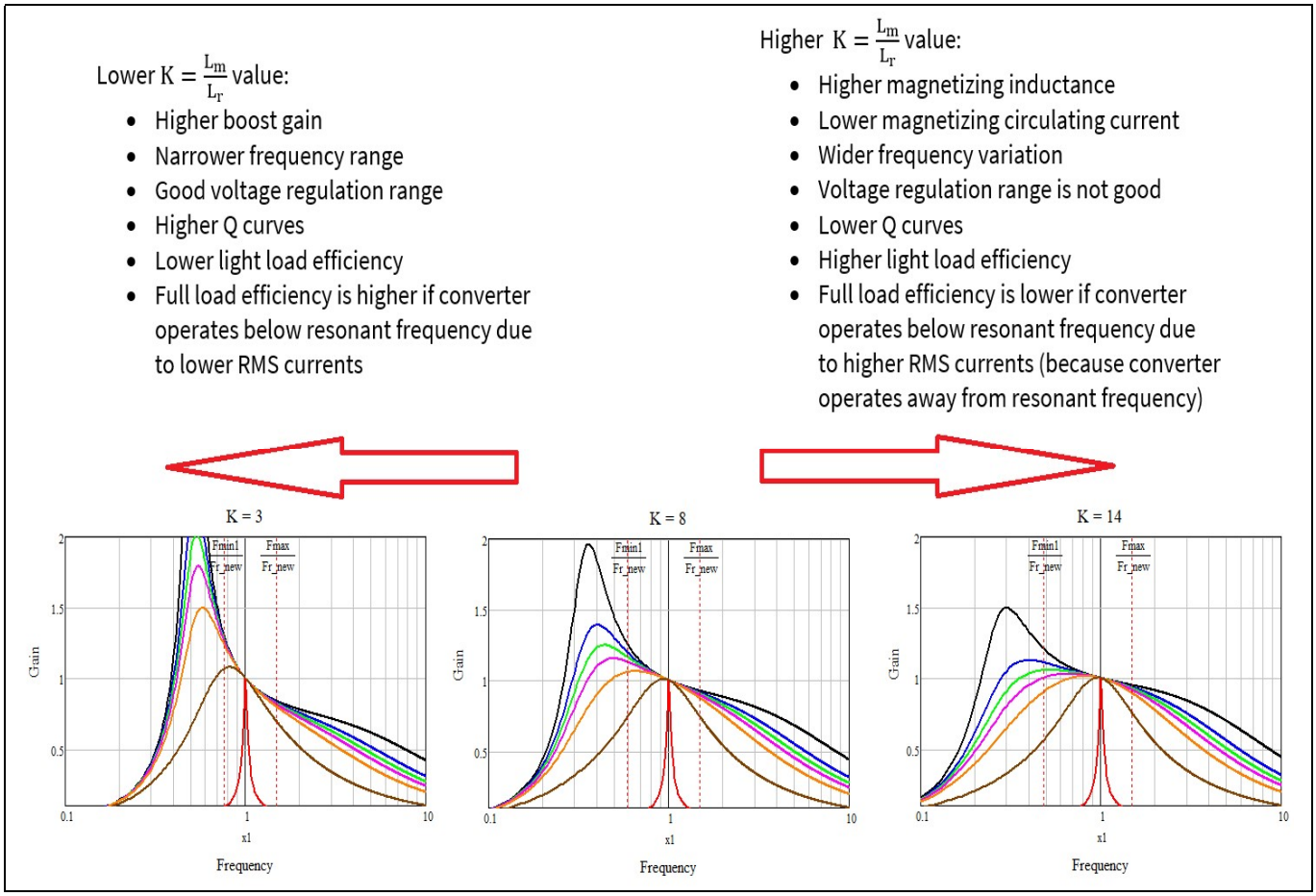


Figure 21 Gain curves for different values of k

A study by Infineon[1] compared a 600 W LLC design for k = 6 and k = 13. Both converters were operating below the resonant frequency. The light-load efficiency was higher, with k = 13 due to lower magnetizing current, but the full-load RMS current was higher, which translated to a lower efficiency at full load. Full-load RMS currents are higher because the frequency range is wider, with k = 13 and converter operating away from resonant frequency. With k = 6, the full-load RMS current is lower, therefore efficiency is higher at full load than with k = 13. This is because the frequency range is narrower and the converter operates close to the resonant frequency. The light-load efficiency with k = 6 was lower than k = 13 due to high circulating currents in the resonant tank.

9.2 First Harmonic Approximation (FHA)

To design the LLC resonant half-bridge resonant converter, the First Harmonic Approximation (FHA) is used to obtain an equivalent circuit. All the components are referenced to the primary side to simplify the analysis. The load is equated to a resistor R_{ac}, which is situated in parallel with transformer primary inductance L_m.

The equivalent AC resistor is given by:

$$R_{ac} = \frac{8n^2}{\pi^2} R_{Load} \quad [26]$$

[1] Study carried out by Jon Hancock and Mladen Ivankovic

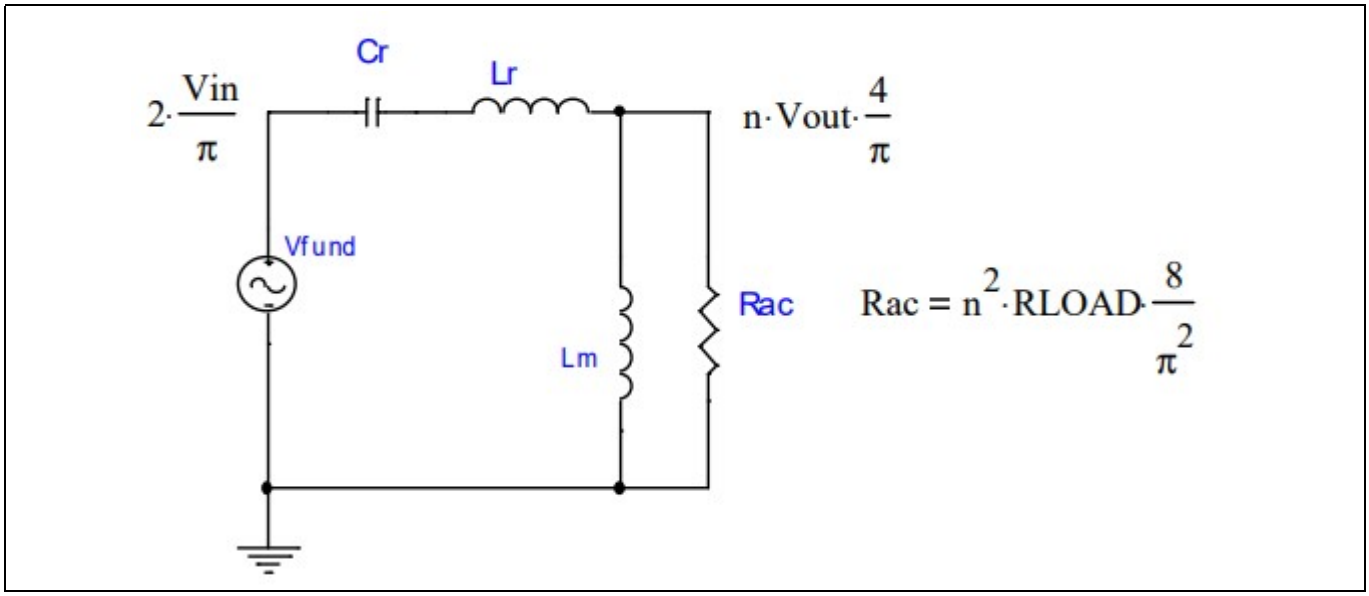


Figure 22 FHA equivalent circuit

The transfer ratio of the equivalent circuit can be obtained as follows:

$$M = \left| \frac{\frac{j.\omega.L_m.R_{ac}}{j.\omega.L_m+R_{ac}}}{j.\omega.L_r+\frac{1}{j.\omega.C_r}+\frac{j.\omega.L_m.R_{ac}}{j.\omega.L_m+R_{ac}}} \right| \quad [27]$$

M can be broken down as follows:

$F_{r1} = \frac{1}{2\pi\sqrt{L_r C_r}}$ Resonant frequency

$x = \frac{F_{s\omega}}{F_{r1}}$ Normalized switching frequency

$k = \frac{L_m}{L_r}$ Ratio of magnetizing inductance to resonant inductance

$R_{ac} = \frac{8 \cdot n^2 \cdot R_{load}}{\pi^2}$ Reflected load resistance

$n = \frac{N_p}{N_s}$ Turns ratio

$Q = \frac{2.\pi \cdot F_{r1}.Lr}{R_{ac}} = \frac{1}{2.\pi \cdot F_{r1}.Cr.R_{ac}}$ Quality factor

$$M = \left| \frac{1}{1+\frac{1}{k}.\left(1-\frac{1}{x^2}\right)+j.Q.\left(x-\frac{1}{x}\right)} \right|$$

Or

$$M = \frac{1}{\sqrt{\left[1+\frac{1}{k}.\left(1-\frac{1}{x^2}\right)\right]^2+\left[Q.\left(x-\frac{1}{x}\right)\right]^2}} \quad [28]$$

The conversion ratio of output voltage V_{OUT} to input voltage V_{IN} is given by:

$$\frac{V_{out}}{V_{in}} = \frac{M}{2 .n} \quad [29]$$

Design calculations for the DEMO_200W_12VDC_LLC HB resonant DC-DC stage have been made using MathCAD 15 software, which will be listed in the following pages.

Code Listing 1

Design of LLC Resonant Half-Bridge

Input Parameters:

Input Voltage:

Vinmin := 350V Vinnom := 397V Vinmax := 420V

Output Voltage:

Vo := 12V Vf := 0.5V Vf with sync rec may be lower

Output Current

Io := 16A

Po := Vo·Io = 192 W

Define target operation freq range:
resonant frequency (Fr), and max frequency (Fmax)

Fr := 100kHz Fmax := 150kHz

Calculate transformer turns-ratio n per maximum input voltage

Load resistance

$$RL := \frac{Vo}{Io} = 0.75\,\Omega$$

Mmin, Mnom, Mmax are the gains

$$Mmin := \frac{(Vo + Vf)}{Vinmax} = 0.03$$

$$Mnom := \frac{(Vo + Vf)}{Vinnom} = 0.031$$

$$Mmax := \frac{(Vo + Vf)}{Vinmin} = 0.036$$

$$xmax := \frac{Fmax}{Fr} = 1.5$$

Code Listing 2

Turns ratio calculation

$$n_cal := \left[\frac{Vinnom}{2\cdot(Vo + Vf)}\right] = 15.88$$

Select a convenient value for n:

$n := 16$

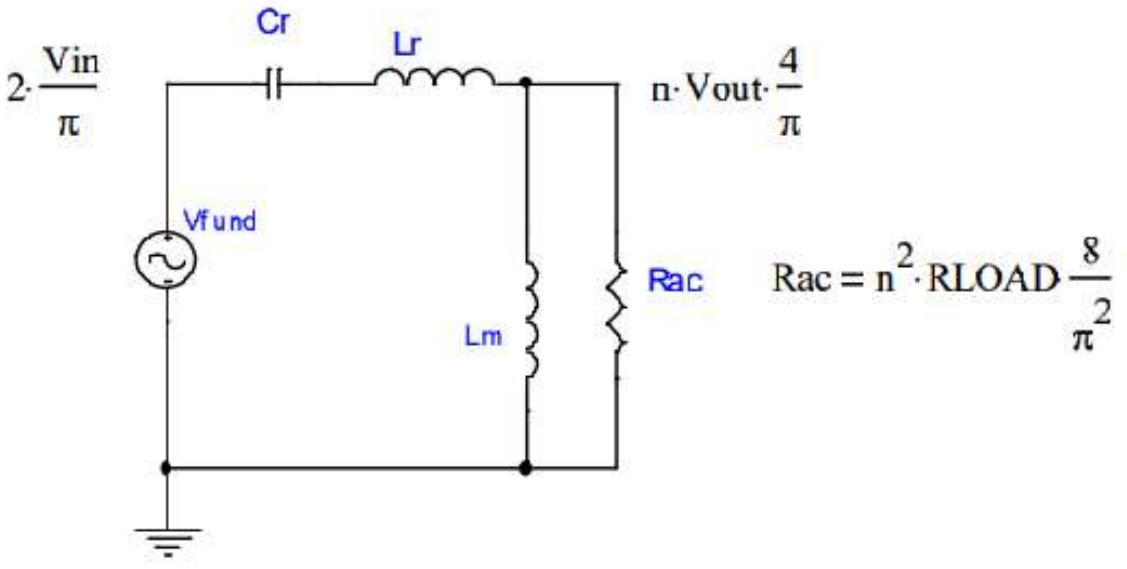
Choose the ratio of transformer magnetizing inductance Lm and leakage inductance Lr : k = Lm/Lr

Smaller *k* value gives steeper Gain curve, especially at the below resonant ZVS region.
The output voltage is more sensitive to frequency variation with smaller *k* factor.
Suggested *k* range: 4~10

$k := 8$

Lp is the measured primary inductance
Lp=Lm+Lr.

Calculate the max. Q value, Qmax1, to stay in the ZVS region at min. Vin and max. load:



Code Listing 3

Transfer ratio of the equivalent circuit can be obtained as following:

The power stage gain is:

$$\text{The } M(x,k,Q)=\frac{1}{\sqrt{\left[1+\frac{1}{k}\cdot\left(1-\frac{1}{x^2}\right)\right]^2+Q^2\cdot\left(x-\frac{1}{x}\right)^2}}$$

To keep the converter working in soft switching mode, the operating point should always lie in the ZVS region as shown in gain curve. The ZVS-ZCS boundary line is defined by the phase angle of Zin, Φ(Zin)= 0 (the boundary condition between capacitive and inductive load), i.e. the imaginary part of Zin is zero. With this condition we can calculate the maximum Q, which enables the converter to remain in ZVS. The maximum Q occurs at the minimum input voltage and the maximum load.

Input impedance:

$$Zin = Zr\left|\frac{k^2\cdot x^2\cdot Q}{1+k^2\cdot x^2\cdot Q^2}+j\left(x-\frac{1}{x}+\frac{x\cdot k}{1+k^2\cdot x^2\cdot Q^2}\right)\right|$$

The definition of k, x and Q:

k = Lm/Lr
x = Fsw/Fr1

$$Fr1=\frac{1}{2\pi\sqrt{Lr\cdot Cr}} \qquad Q=\frac{\sqrt{\frac{Lr}{Cr}}}{Rac}$$

Calculate Qmax to remain in ZVS operation at maximum load and minimum input voltage.
The ZVS-ZCS boarderline is defined by Im(Z(in))=0, thus:

$$Qmax := \frac{1}{k}\cdot\frac{1}{2\cdot n\cdot Mmax}\cdot\sqrt{\frac{(2\cdot n\cdot Mmax)^2}{(2\cdot n\cdot Mmax)^2-1}}+k = 0.383$$

Code Listing 4

Calculate the effective load resistance:

$$Rac := \frac{8}{\pi^2}\cdot n^2 \cdot RL = 155.629\,\Omega$$

Set value for Q:

$$Q := Qmax = 0.383$$

Calculate the value xmin the converter will work at, at min. input voltage and max. load:

The minimum switching frequency occurs at the maximum load and minimum input voltage with the previously calculated maximum Qmax. As Qmax is defined by Im(Zin) = 0,

$$\left[x - \frac{1}{x} + \left(x \cdot \frac{k}{1 + k^2 \cdot x^2 \cdot Qmax^2}\right) = 0\right]$$

Fmin is calculated as :

$$xmin := \sqrt{\frac{1}{1 + k \cdot \left[1 - \frac{1}{(2 \cdot n \cdot Mmax)^2}\right]}} = 0.59$$

$$Fmin := xmin \cdot Fr = 58.977 \cdot kHz$$

Calculate the characteristic impedance of the tank circuits and all component values:

$$Zr := Rac \cdot Q = 59.617\,\Omega$$

$$Cr_cal := \frac{1}{2 \cdot \pi \cdot Fr \cdot Zr} = 2.67 \times 10^{-8}\,F$$

$$Lr_cal := \frac{Zr}{2 \cdot \pi \cdot Fr} = 9.488 \times 10^{-5}\,H$$

Code Listing 5

Select a standard value for Cr

$Cr := 26.2nF$ Composed of 20nF paralleled with 6.2nF

Recalculate Fr1 and Lr

$$Fr1 := \frac{1}{2\cdot(\pi\cdot Cr\cdot Zr)} = 101.893\cdot kHz$$

$$Lr_est := \frac{Zr}{2\cdot\pi\cdot Fr1} = 9.312\times 10^{-5}\,H$$

$$Lm_est := k\cdot Lr_est = 7.45\times 10^{-4}\,H$$

The above resonant frequency of 102 kHz corresponds to Lm = 745uH and Lr = 93uH

Magnetics vendor may not provide exact values as shown by the calculation above, in such cases adjust "k" and "Cr" values to match the magnetics vendor values for Lm and Lr

The LLC transformer (Lm) and resonant inductor (Lr) available with us are :
Lm = 724uH and Lr = 90uH

Back calculate with the available transformer (Lm) and inductor (Lr) values

$Vinmin = 350\,V$

$$Mmax1 := \frac{(Vo + Vf)}{Vinmin} = 0.036$$ $Rac = 155.629\,\Omega$

$n = 16$

$Lm1 := 724\cdot 10^{-6}\,H$

$Lr1 := 90\mu H$

$Cr1 := Cr = 2.62\times 10^{-8}\,F$

$$k1 := \frac{Lm1}{Lr1} = 8.044$$

Code Listing 6

$$Q1 := \frac{1}{k1}\cdot\frac{1}{2\cdot n\cdot Mmax1}\cdot\sqrt{\frac{(2\cdot n\cdot Mmax1)^2}{(2\cdot n\cdot Mmax1)^2-1}} + k1 = 0.382$$

$$Zr1 := Rac\cdot Q1 = 59.395\,\Omega$$

With the current Lm = 724uH and Lr= 90uH values, the new resonant frequency is

$$Fr_new := \frac{Zr1}{(2\cdot\pi\cdot Lr1)} = 105.034\cdot kHz$$

$$xmin1 := \sqrt{\frac{1}{1 + k1\cdot\left[1 - \frac{1}{(2\cdot n\cdot Mmax1)^2}\right]}} = 0.589$$

Minimum frequency is

$$Fmin1 := xmin1\cdot Fr_new = 61.834\cdot kHz$$

Primary and Secondary Peak, RMS currents

I1 is the current where the resonant current in Lr meets the magnetizing current in Lm.
This is also the point where Cr and Lr finish resonance for the first half-period of Fr1.
At this point, there is no more energy delivered to the load and the output diodes are off.
The Cr starts to resonate with Lr + Lm until the switching MOSFETs change states.
I1 can be calculated as:

$$Lm1 = 7.24\times10^{-4}\,H \qquad Fr_new = 105.034\cdot kHz$$

$$I1 := n\cdot\frac{Vo}{2\cdot Lm1\cdot 2\cdot Fr_new} = 0.631\,A$$

$$Fmin1 = 61.834\cdot kHz \qquad Fr_new = 105.034\cdot kHz \qquad Fmax = 150\cdot kHz$$

$$Io = 16\,A$$

Code Listing 7

$$Ipri_pk := \sqrt{\left(Io \cdot \frac{\pi}{2 \cdot n}\right)^2 + I1^2} = 1.693\,A$$

$$Ispk := Io \cdot \frac{\pi}{2} = 25.133\,A$$

$$Iprms := \frac{Ipri_pk}{\sqrt{2}} = 1.197\,A \qquad Isrms := Io \cdot \frac{\pi}{4} = 12.566\,A$$

Plot the power stage transfer function per Lr, Lm, Cr, Rac :

$$M(x1, k1, Q1) := \left| \frac{1}{\sqrt{\left[1 + \frac{1}{k1} \cdot \left(1 - \frac{1}{x1^2}\right)\right]^2 + Q1^2 \cdot \left(x1 - \frac{1}{x1}\right)^2}} \right|$$

$x1 := 0.1, 0.11 .. 10$ $\quad k1 = 8.044$ $\quad Q1 = 0.382$ $\quad n = 16$

$Vinmin = 350\,V$ $\quad Vinnom = 397\,V$ $\quad Vinmax = 420\,V$ $\quad Vf = 0.5\,V$

$$min_gain := 2 \cdot n \cdot \frac{(Vo + Vf)}{Vinmax} = 0.952$$

$$m_nom := 2 \cdot n \cdot \frac{(Vo + Vf)}{Vinnom} = 1.008$$

$$max_gain := 2 \cdot n \cdot \frac{(Vo + Vf)}{Vinmin} = 1.143$$

$Fmin1 = 61.834 \cdot kHz$ $\quad Fr_new = 105.034 \cdot kHz$ $\quad Fmax = 150 \cdot kHz$

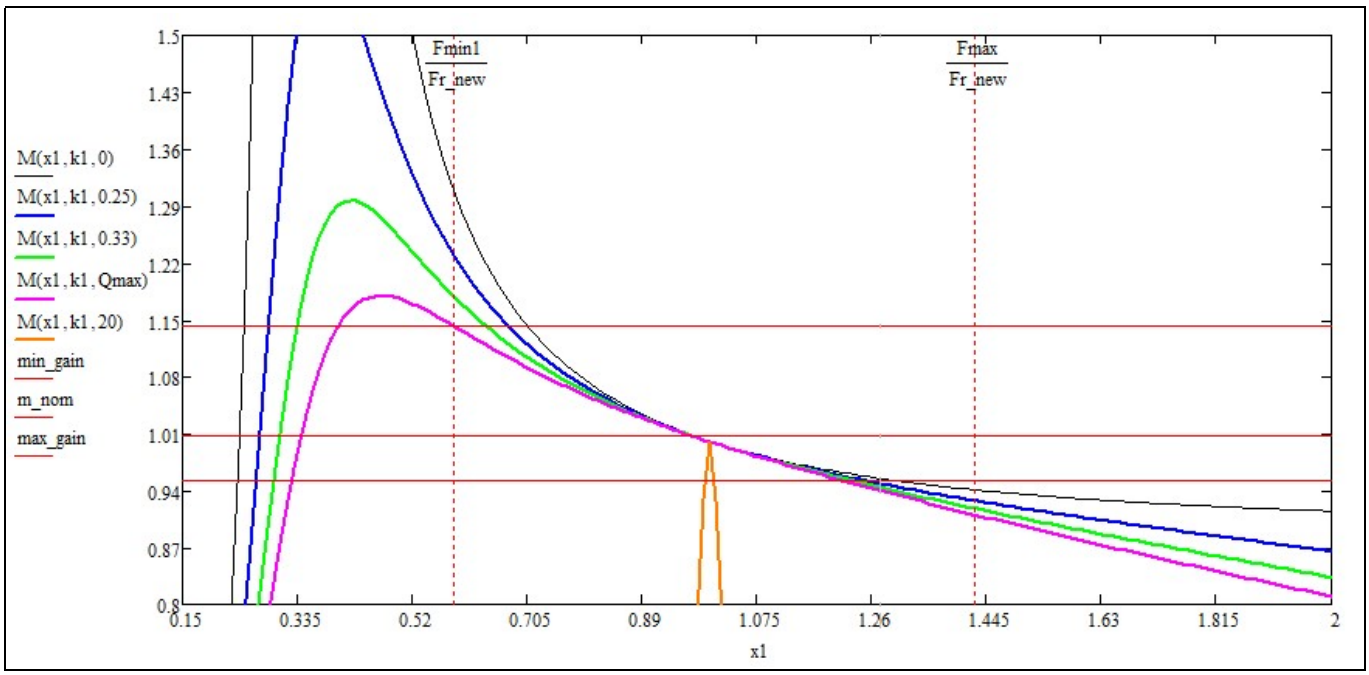


Figure 23 Curves of gain against frequency

The above graph is based on FHA. It shows the variation of the gain versus the frequency. The pink curve corresponds to the full-load condition ($Q = Q_{max} = 0.383$). In order to design the LLC tank components for optimized operation over an input PFC voltage variation of 350 V up to 420 V, it is necessary to make sure the no-load (Q = 0, black) and the full-load ($Q = Q_{max}$, purple) curves intersect the minimum gain (min_gain = 0.952), nominal gain (m_nom = 1.008) and the maximum gain (max_gain = 1.143) shown on the vertical axis, within the frequency boundaries.

9.3 Dead-time calculations

Code Listing 8

What happens during the dead time ?

$n = 16$

$Lm1 = 7.24 \times 10^{-4}\,H$

$Lr1 = 9 \times 10^{-5}\,H$

$Cr1 = 2.62 \times 10^{-8}\,F$

IPP60R280P6 MOSFET parameters:

$Rdson := 280 \cdot 10^{-3}\,\Omega$ $factor := 1.76$ $Fmax = 150 \cdot kHz$

Co_er is the energy related capacitance when Vds is rising from 0 to 400V:

$Co_er := 44pF$ $Vds := 400V$

$$Idoff_min := 2 \cdot \frac{\sqrt{2}}{\pi} \cdot n \cdot \frac{Vo}{2 \cdot \pi \cdot Fmax \cdot Lm1} = 0.253\,A$$

$Ceq := 2 \cdot Co_er = 8.8 \times 10^{-11}\,F$

First Condition Inductive energy > Capacitive energy

$$\frac{1}{2} \cdot (Lm1 + Lr1) \cdot Idoff_min^2 = 2.612 \times 10^{-5}\,J \qquad \frac{1}{2} \cdot Ceq \cdot Vinmax^2 = 7.762 \times 10^{-6}\,J$$

$26\mu J > 7.7\mu J$

Second Condition Deadtime > Time required to charge/discharge the total cap

Co_tr is the time related capaitance when Vds is rising from 0 to 400V

Crss_eff can be taken as 1/2 or 1/3 of Crss

$Co_tr := 182pF$ $Crss_eff := 2.5pF$ $Cwell := 5pF$

$CHB := 2Co_tr + Crss_eff + Cwell = 3.715 \times 10^{-10}\,F$

Code Listing 9

No load current is calculated as

$Lm1 = 7.24 \times 10^{-4}\,H$ $Lr1 = 9 \times 10^{-5}\,H$ $Vo = 12\,V$ $Fmax = 150\cdot kHz$

$$I_noload := n\cdot\frac{Vo}{[4\cdot Fmax\cdot(Lm1 + Lr1)]} = 0.393\,A$$

Time needed to discharge the Coss of the half bridge MOSFETs

$$time_needed := CHB\cdot\frac{Vinmax}{I_noload} = 3.969 \times 10^{-7}\,s$$

Calculation of the deadtime
(Ref: International Rectifier AN-1160 application note)

Rdown : IRS2795(1,2) gate driver effective pull down resistance (6Ω)
Rg :is the external MOSFET gate drive resistor
Rgfet: MOSFET gate input resistance

IC - Rdown: $Rdown := 6\Omega$

Rgfet-internal of MOSFET: $Rgfet := 5.5\Omega$

External gate resistance $Rg := 10\Omega$

Gate Source voltage $Vgs := 15V$

IPP60R280P6 plateau voltage from the datasheet:

Vm is Vplateau of the mosfet $Vm := 6.1V$

IPP60R280P6 gate charge values:

$Qg := 25.5nC$ $Qgd := 9.5nC$ $Qgs := 7nC$

$$Cgeq := \left(\frac{Qg - Qgd - Qgs}{Vgs - Vm}\right) = 1.011 \times 10^{-9}\,F$$

$Vgsth := 4V$ $Vcc := 15V$

$Rtotal := Rdown + Rg + Rgfet = 21.5\,\Omega$

$$t1 := -Rtotal\cdot Cgeq\cdot\ln\left(\frac{Vgsth}{Vcc}\right) = 2.874 \times 10^{-8}\,s$$

Code Listing 10

$$Tch := CHB \cdot \frac{Vinmax}{I_noload} = 3.969 \times 10^{-7}\,s$$

$$Tdeadtime := Tch + t1 + 50ns = 4.756 \times 10^{-7}\,s$$

$$new_Tdeadtime := Tdeadtime = 4.756 \times 10^{-7}\,s$$

Calculate RT and CT capacitor for IRS27952 Half bridge LLC IC

$$Ct := \frac{\left(\frac{new_Tdeadtime}{1s} \cdot 10^{-3} - 40 \cdot 10^{-12}\right)}{0.85} = 5.125 \times 10^{-10}$$

CT capacitor should be equal or bigger than the calculated value for ZVS operation:

$new_Ct := 510pF$ We chose 510pF which is a standard value

Calculate the actual dead-time per the selected CT value:

$$tdt := (0.85 \cdot new_Ct + 40pF) \cdot 2\frac{V}{2mA} = 4.735 \times 10^{-7}\,s$$

$Fmin1 = 61.834 \cdot kHz$

Calculate RT per the minimum switching frequency Fmin and CT:

$$Rt := \frac{1}{\left(2 \cdot Fmin1 \cdot tdt \cdot 10^{-3}\right)} - 1000 = 1.608 \times 10^{4}\ \Omega$$

RT resistor should be smaller than the calculated value to keep ZVS operation

Select RT= 16k $new_Rt := 16k\Omega$

Code Listing 11

Calculate Rmax based on the maximum switching frequency Fmax, C_T, and R_T:

$$Req := \frac{1}{(2 \cdot Fmax \cdot tdt \cdot 10^{-3})} - 1000 = 6.04 \times 10^{3} \quad \Omega$$

$$Rmax := \frac{new_Rt}{1\Omega} \cdot \frac{Req}{\left(\frac{new_Rt}{1\Omega} - Req\right)} = 9.702 \times 10^{3} \quad \Omega$$

Select Rmax= 10k $\quad Rmax_chosen := 10 \cdot 10^{3} \quad \Omega$

Calculate Softstart- Rss and Css and Startup Frequency

Calculate Rss with the desired soft-start frequency

$Fss := 300kHz$

$Tss := 30ms$

Deadtime $\quad tdt = 4.735 \times 10^{-7}\ s$

$new_Rt = 1.6 \times 10^{4}\ \Omega$

$$Rsseq := \frac{1}{(2 \cdot Fss \cdot tdt \cdot 10^{-3})} - 1000 = 2.52 \times 10^{3} \quad \Omega$$

$$Rss := \frac{new_Rt}{1\Omega} \cdot \frac{Rsseq}{\left(\frac{new_Rt}{1\Omega} - Rsseq\right)} = 2.991 \times 10^{3} \quad \Omega$$

$Rss_chosen := 3k\Omega$

$$Css := \frac{Tss}{(3 \cdot Rss_chosen)} = 3.333 \times 10^{-6}\ F$$

$Css_Chosen := 3.7\mu F$

$Tss_recalculated := 3 \cdot Rss_chosen \cdot Css_Chosen = 0.033\ s$

Code Listing 12

Final LLC component values

$Lm1 = 7.24 \times 10^{-4} H$

$Lr1 = 9 \times 10^{-5} H$

$Cr1 = 2.62 \times 10^{-8} F$

$new_Rt = 1.6 \times 10^{4} \Omega$ 16kΩ

$new_Ct = 5.1 \times 10^{-10} F$ 510pF

$Rmax_chosen = 1 \times 10^{4}$ 10kΩ

$Rss_chosen = 3 \times 10^{3} \Omega$ 3kΩ

$Css_Chosen = 3.7 \times 10^{-6} F$ 3.3µF

$Fmin1 = 61.834 \cdot kHz$

$Fr_new = 105.034 \cdot kHz$

$Fmax = 150 \cdot kHz$

9.4 OVP circuit (hiccup mode operation)

The following circuit has been used to implement the light/open-load burst mode operation of the LLC resonant converter. Under light-load conditions the LLC resonant converter voltage feedback loop attempts to drive the switching frequency higher to prevent the output voltage rising above the target level. However, as frequency increases a point is reached at which ZVS operation is no longer possible. In a hard switching scenario the half-bridge MOSFETs would begin to suffer high switching losses leading to over-heating. To avoid this, the maximum permitted switching frequency is set below the ZVS region upper boundary. However, to prevent output voltage at light load from exceeding an acceptable level, it now becomes necessary to introduce hiccup mode over-voltage protection, which enables the converter to operate in short bursts..

The following circuit reduces system standby power by disabling the PFC section and the LLC section through an opto-isolator (IC7), which provides pull-down through three Schottky diodes connected to its collector. The open-collector output of IC10 transitions low when the converter output voltage rises above a defined level providing current to the diode of IC7. The comparator circuit includes a resistor (R30) to provide hysteresis so that when the output capacitors discharge sufficiently the circuit will deactivate. In this way burst mode operation is implemented with controllable on and off periods to maintain the correct output voltage at light load or in an open circuit.

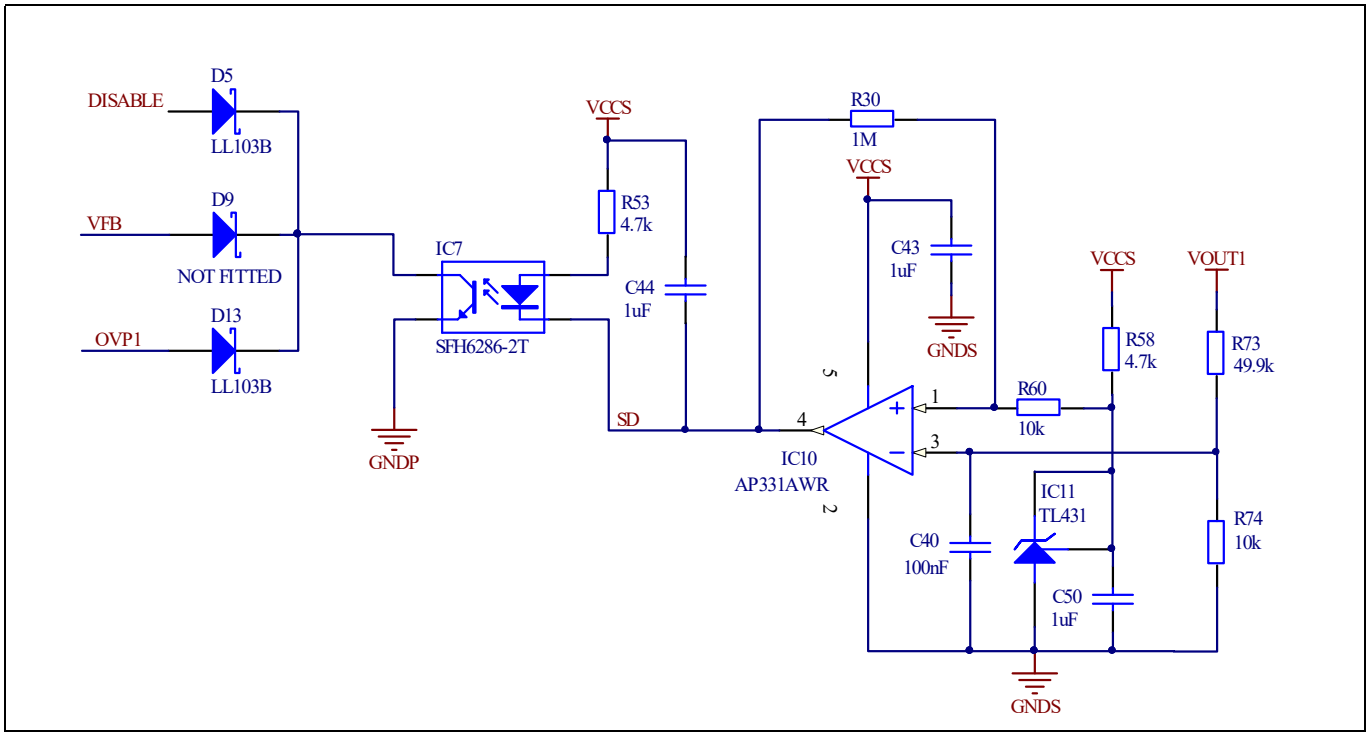


Figure 24 OVP circuit for the IRS27952-based LLC resonant converter

9.5 Over-current protection

Over-current protection is implemented with the following high output current detection circuit. IC9 and IC10 are supplied form the auxiliary power supply so that they are able to continue functioning when the output is shorted.

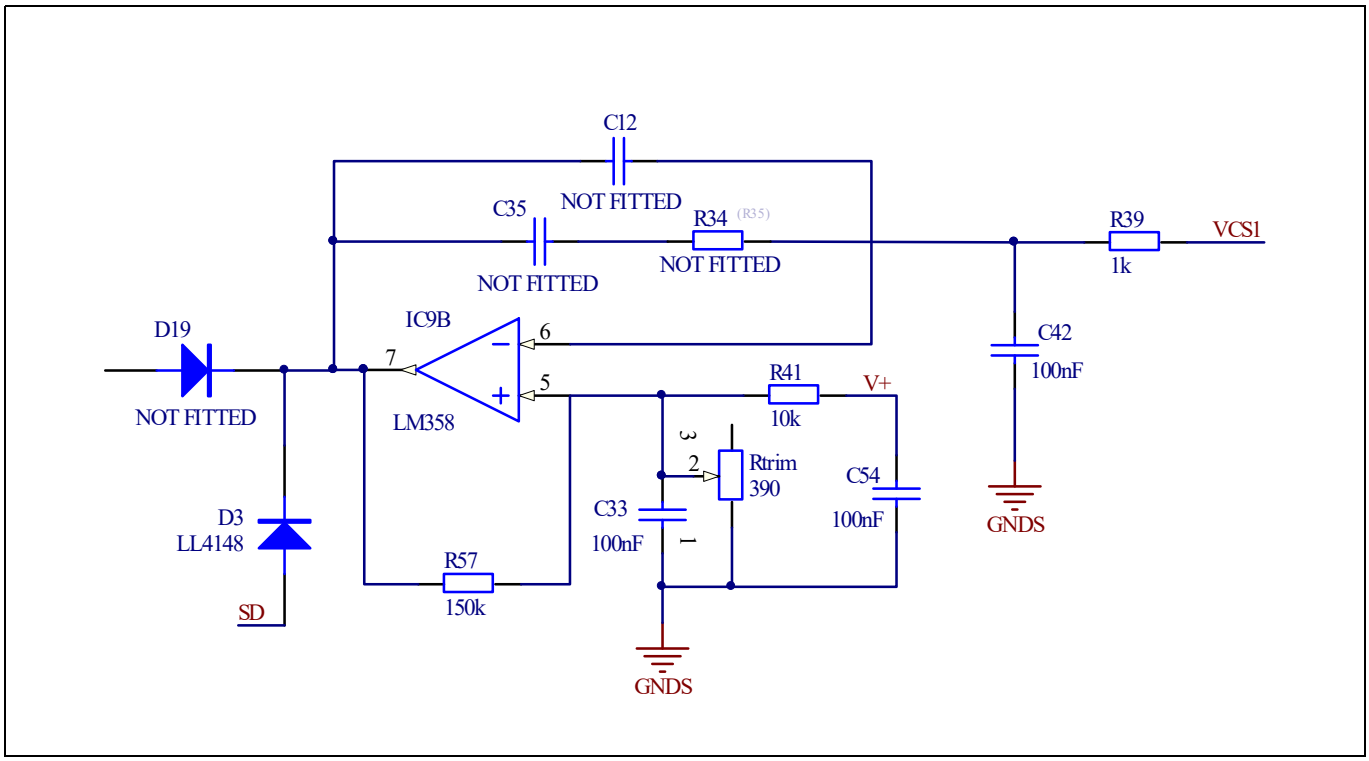


Figure 25 OCP circuit for the IRS27952-based LLC resonant converter

The circuit based around IC9B provides over-current protection sensed through the output current shunt resistors Rcs3, 4, 5, 6 and 8. The threshold is set by adjusting Rtrim, which is set to trigger protection in the 18 to 19 A range. When the output current exceeds this limit, the output of IC9B transitions low causing conduction through the diode of opto-isolator IC4 through D19 if D19 is installed. Since IC4 is used for both voltage and current feedback, D19 and D12 may be used to OR the outputs from IC9a (voltage feedback) and IC9b (over-current detection) so that either may cause the switching frequency to be increased to reduce output power as IC4 pulls down on the RT input of IC5 through Rmax. In this implementation the over-current protection circuit utilizes IC9B as a comparator with hysteresis provided by R57 and connected to IC7 through D3 providing ORing with the open-collector output of IC10[1]. Hiccup-mode protection is provided through D5, which is connected to the base of Q7. This causes C11 supplying VCC to IC5 to discharge to a voltage below the UVLO negative threshold[2]. IC5 then ceases to oscillate so that power transfer is interrupted. The PFC section is also disabled during this time through D13. The output current then falls and Q7 is released as the output of IC9B transitions positive again so that C11 is able to re-charge back up to the UVLO positive threshold of IC5. This cycle repeats until the overload condition is removed from the output.

[1] This circuit has been modified from a current feedback loop controlling the switching frequency to a hiccup mode protection scheme. This is why C12, C35 and R34 have been removed and R57 has been added.

[2] D9 has been removed from the circuit as it was found that small leakage currents through this diode can affect the operation of the oscillator of IC5.

9.6 Short-circuit protection

As mentioned earlier, the IRS27952 includes a high current shut-down function, which uses the on-state resistance of the low-side MOSFET sensed at the VS pin with a nominal threshold of 3 V that triggers a latched shut-down of the gate drive outputs.
However, it cannot be guaranteed that the primary tank circuit during an output short circuit will be high enough to trigger this protection mechanism. Furthermore, the tank current would need to reach a peak in the region of 10 A to trigger this protection. In this design the over-current protection scheme described in the previous section also provides short-circuit protection therefore the system would enter hiccup mode befre ever triggering protection previously described, which is considered to be a safer and more reliable approach.

10 IRS11688 functional overview

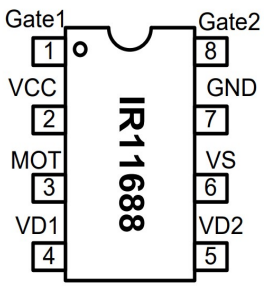
The IRS11688 Synchronous Rectifier (SR) control IC drives a pair of N-channel power MOSFETs, forming the rectifying output stage of a resonant half-bridge converter. The drain-to-source voltage of each SR MOSFET is directly sensed to determine the level of conducted current so that the MOSFET can be turned on and off in close proximity to the zero current transition. Built-in shoot-through protection logic prevents both channels from ever being able to turn on at the same time. Internal blanking, reverse current protection and double pulse suppression enable reliable operation in all operating modes.

The IRS11688 precisely controls switching on and off of the synchronous MOSFETs, thereby bypassing their body diodes during the secondary conduction phases to emulate the rectifying action of a dual-diode rectifier while eliminating the majority of conduction losses. The MOSFET drain-to-source voltages are sensed at millivolt levels to determine the magnitude and polarity of the drain current so that the IRS11688 can switch the gates on and off appropriately. The high-voltage input structure allows the IRS11688 to withstand up to 200 V from direct connection to each drain pin. The IRS11688-based smart Synchronous Rectifier (SR) offers significant efficiency improvement in resonant converters over the full load range. Replacement of a Schottky diode output rectifier with the IRS11688, combined with a pair of correctly selected high-performance MOSFETs, provides significantly reduced power dissipation.

The IRS11688 is able to operate from wide V_{CC} supply voltage ranging from 4.75 V to 20 V, enabling it to be supplied from the output in a 5 V system without the need for an auxiliary transformer winding. A logic-level MOSFET is required for low output (low V_{CC}) voltage applications. A built-in arming and triggering mechanism allows correct switching on and off of the SR MOSFET under all system conditions, offering improved system reliability over a basic self-driven SR scheme or earlier generations of SR controller.

In addition, the IRS11688 enters a power-saving mode if neither VD sensing input detects a transition for more than an internally defined waiting time (typically 500 µs). In this mode supply current reduces to a few hundreds of micro amps, reducing quiescent power consumption and improving system standby and light-load efficiency.

The IRS11688 is available in a SO-8 package. The pin-out is shown below:



Pin	Name	Description
1	***GATE1***	Gate drive output 1
2	***VCC***	Supply voltage
3	***MOT***	Minimum on-time program input
4	***VD1***	SR MOSFET 1 drain voltage sense
5	***VD2***	SR MOSFET 2 drain voltage sense
6	***VS***	SR MOSFET source voltage sense
7	***GND***	Analog and power ground
8	***GATE2***	Gate drive output 2

Figure 26 IRS11688 pin assignments

The operating waveforms shown in figure 28 show one side of the split secondary dual MOSFET SR. During period T1 there is no current in this branch of the secondary. The T2 phase begins when the corresponding primary switch is turned on and energy is transferred through the transformer to be delivered to the load through the output rectifier circuit. At this point the conduction phase of the branch SR MOSFET is initiated and current starts flowing through its body diode to produce a negative V_{DS} voltage. The body diode has a much higher voltage drop than the turn-on threshold V_{TH2}, causing the IR11688 to drive the gate of the SR MOSFET on to bypass it. When the MOSFET is turned on the instantaneous sensed voltage reduces to $I \cdot R_{DS(on)}$. This voltage

level, being much lower than body diode forward voltage drop, is sensitive to parasitic ringing generated by the transformer leakage inductance and MOSFET output capacitance. To avoid false triggering and resulting premature gate turn-off, a blanking period (MOT) is set that disables V_{TH1} triggering for a minimum period of time set by an external resistor. This avoids premature turn-off from occurring shortly after turn-on, by maintaining the MOSFET on for a minimum amount of time regardless of ringing transitions.

Once the SR MOSFET has been turned on, it remains on until the rectified current decays to a level where V_{DS} falls to the regulation threshold V_{THR}. At this point the gate drive pull-up is switched off and the gate drive output remains in a high impedance state with a weak pull-down to slowly discharge the gate voltage. The MOSFET channel resistance increases as gate voltage drops, moving toward the linear region of operation and thereby maintaining the negative V_{DS} voltage drop, more negative than the turn-off threshold V_{TH1}. The discharge circuit is maintained to keep V_{DS} voltage regulated around V_{THR} as current falls, thereby extending the MOSFET conduction period and enabling light-load operation.

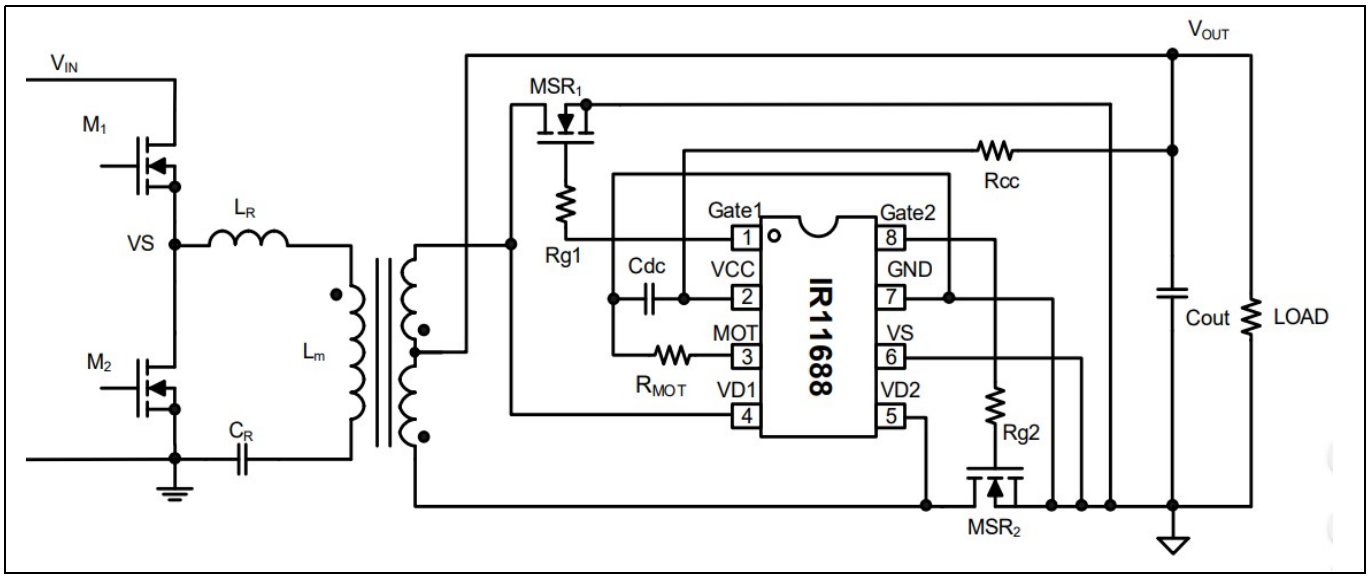


Figure 27 Typical schematic of a resonant half-bridge converter with IR11688 SR controller

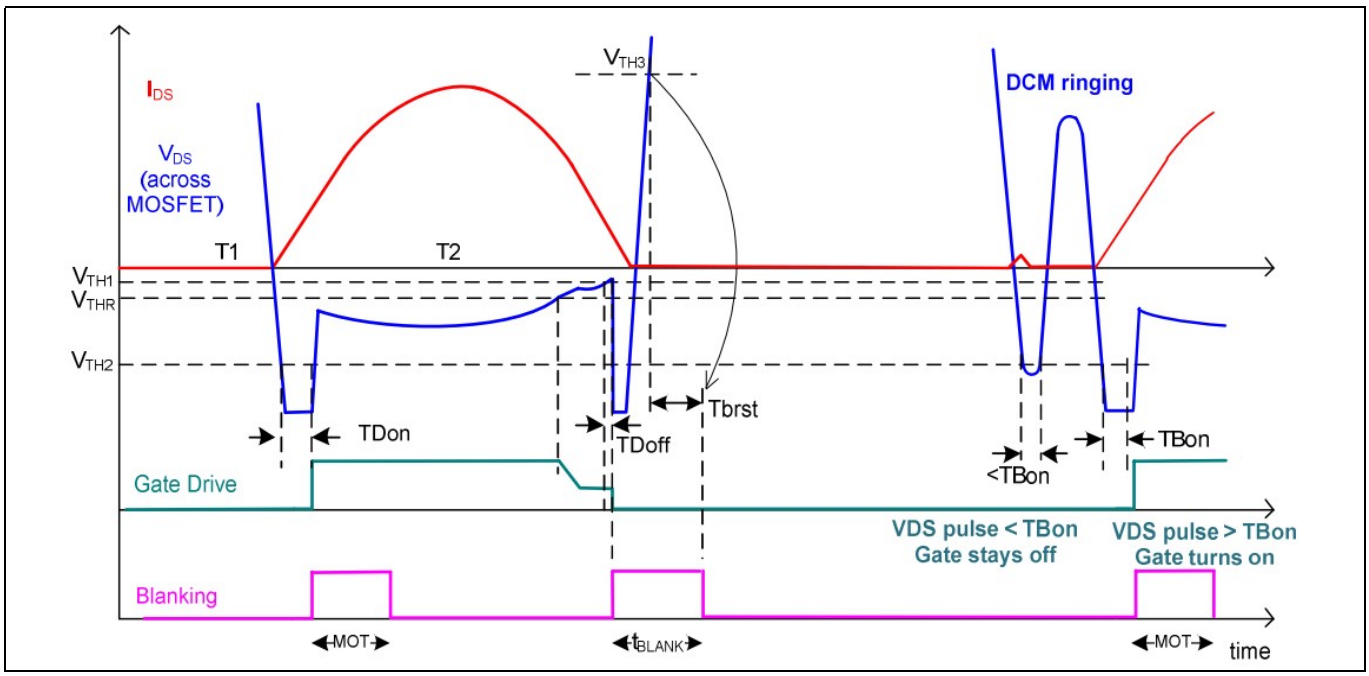


Figure 28 Typical operating waveform of the IR11688

Eventually, as the MOSFET channel current reduces further toward zero, the V_{DS} voltage crosses threshold V_{TH1} and the IR11688 turns the gate off. The gate drive regulation function is illustrated in figure 29:

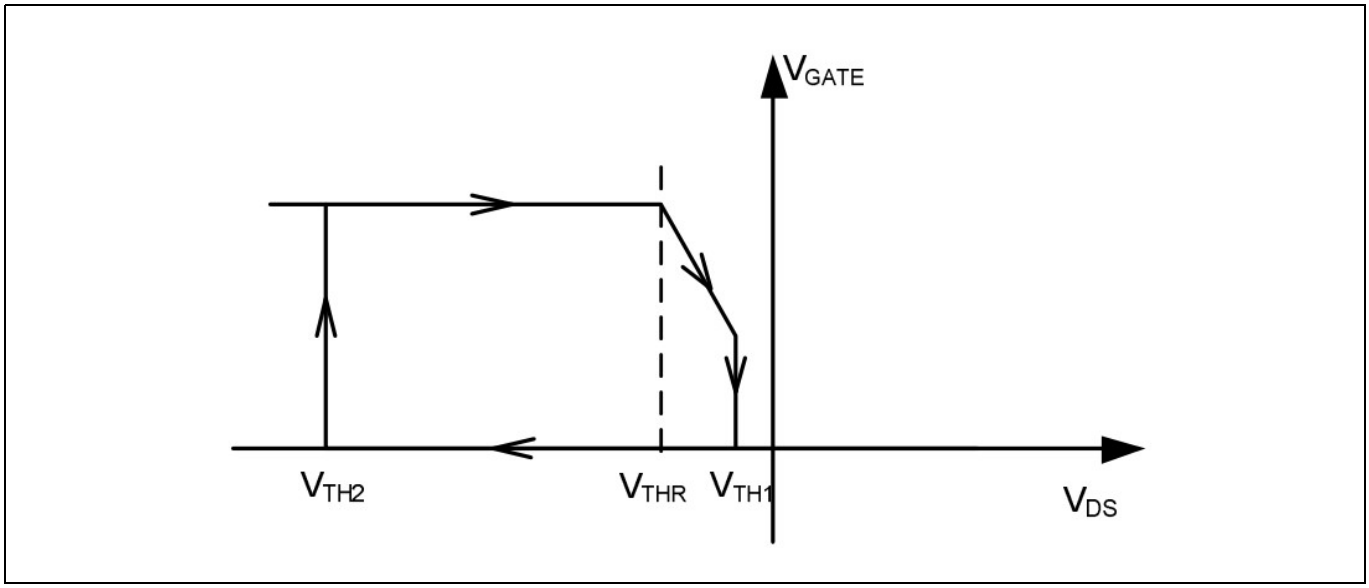


Figure 29 IR11688 voltage sensing thresholds

When the IR11688 turns the gate off, current again starts flowing through the body diode, which causes the V_{DS} voltage to make a sharp negative transition. Depending on the amount of residual current, V_{DS} may once again exceed the turn-on threshold V_{TH2}. For this reason re-triggering is disabled after the gate drive has been switched off until the controller has re-armed. The re-arming sequence requires V_{DS} to cross the positive V_{TH3} threshold and remain above it for a period denoted as t_{BRST}. If this does not occur the gate drive will remain low for a period of t_{BLANK}, after which time re-arming will occur automatically, to achieve high system efficiency combined with low standby loss. As mentioned, the IR11688 incorporates a programmable minimum on-time (MOT) to provide flexibility when using the IR11688 in various applications operating at different switching frequencies. The MOT function effectively sets the shut-down point at light load. During normal operation, the designer sets the minimum on-time to be shorter than the secondary conduction period. At progressively lighter loads, the conduction period reduces until it is eventually shorter than the MOT. If the IR11688 detects no voltage drop signifying no SR drain current, the MOT protection function causes the gate drive to be disabled for the next cycle. This MOT protection operates whether or not the SR gate drive is on, that is if conduction is through the drain-source channel or the body diode. In this way the IR11688 does not drive the gate at light loads and therefore consumes minimal power, improving system efficiency.

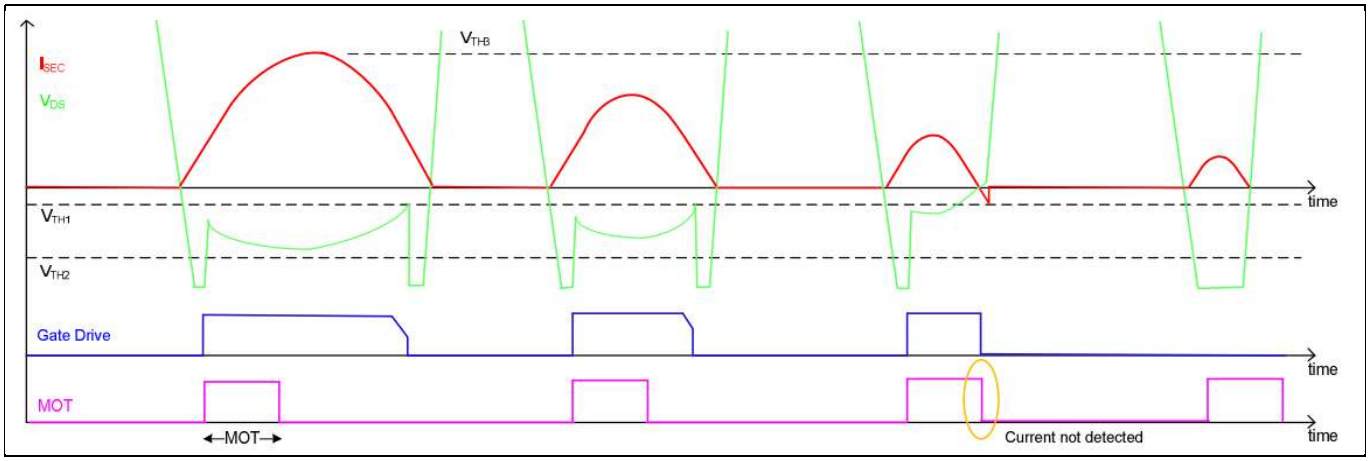


Figure 30 MOT protection as load decreases

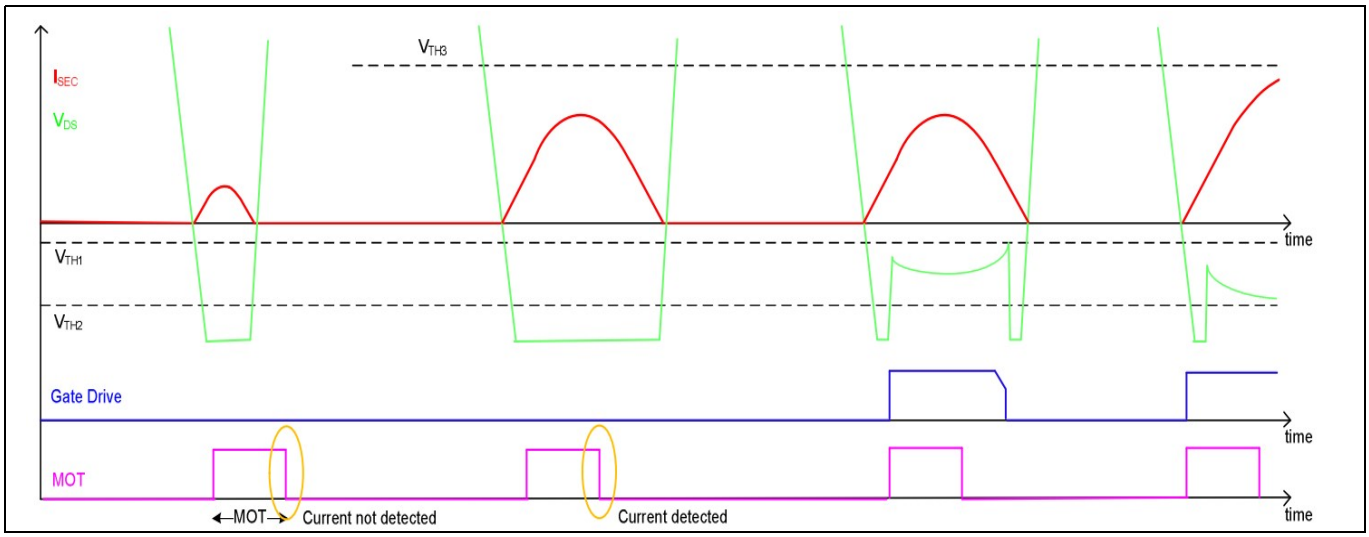


Figure 31 Gate drive resuming as load increases

The IR11688 includes a turn-on leading-edge blanking function to prevent misfiring that could be triggered by high frequency ringing in DCM operation. In DCM the drain voltage of the SR MOSFET can resonate when secondary current transitions in each half-cycle. This V_{DS} ringing, as shown in figure 28, could drop below zero volts under certain conditions, such as higher body diode voltage drop or longer body diode reverse recovery. To avoid false triggering by negative ringing, the IR11688 only triggers if V_{DS} is lower than V_{TH2} and longer than blanking time T_{bon}. Therefore, in the case of a short spike or ringing the IR11688 will not switch on the MOSFET gate and the internal MOT timer will not be initiated, preventing a false trigger event and resulting shoot-through current. In a regular conduction cycle V_{DS} remains lower than V_{TH2} for more than T_{bon}, and so the gate turns on after T_{bon} expires. The total turn-on delay T_{don} is the sum of T_{bon} blanking time and the propagation delay of the internal comparator. The turn-on delay T_{don} and the MOT time limit the minimum conduction time of the secondary rectifiers, and hence the maximum switching frequency of the converter with which it can effectively operate.

10.1 MOT resistor calculation

The MOT is linear in relation to the resistor value R_{MOT}. The following formula can be used to determine the required value:

$$R_{MOT} = 5.10^{10} \cdot t_{MOT} \quad [30]$$

The value of R_{MOT} should not be lower than the minimum recommended on the datasheet. On this board a standard value of 40.2 kΩ is used at the MOT pin of the IC. This value gives a minimum on-time of 800 ns.

11 ICE5QR0680AG functional overview

For low output power applications, the flyback converter is the most widely used topology when galvanic isolation and/or multiple output are required, because it has a low system cost and is easy to design. It is used as an auxiliary “housekeeping” power supply for higher-power applications (e.g. air-conditioners, PC power, server power, industrial SMPS, etc.).

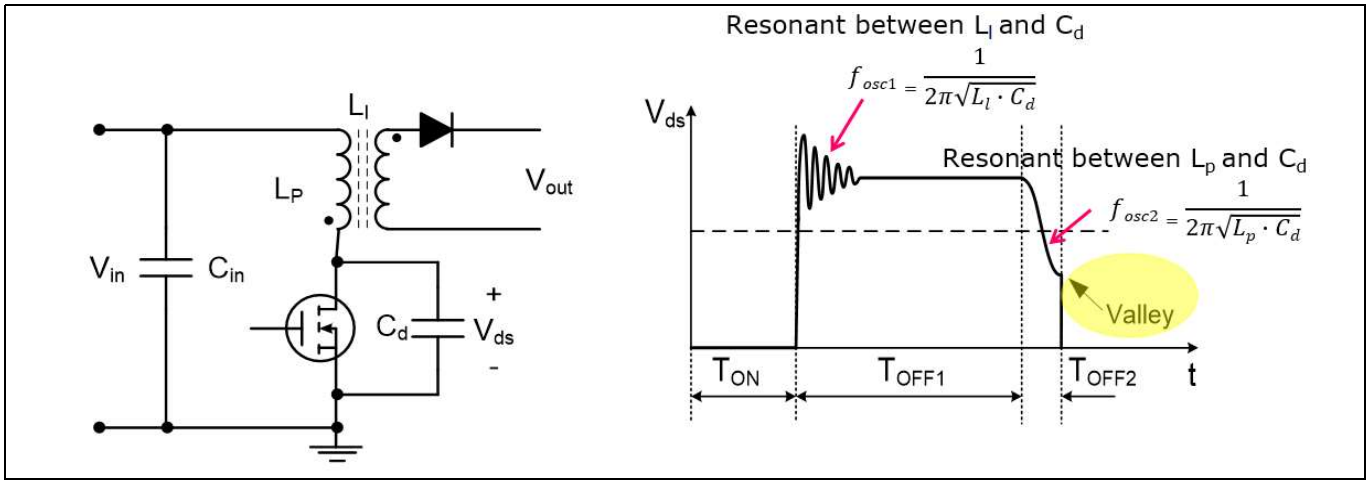


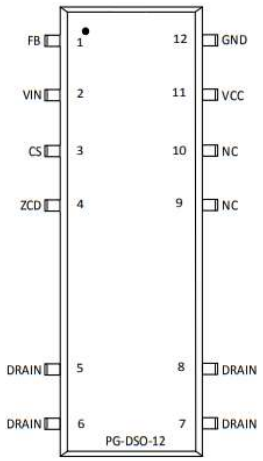
Figure 32 QR flyback converter

11.1 Quasi-Resonant (QR) flyback converter operation

When the primary MOSFET is turned on in the flyback converter the current through the primary side of the transformer begins to ramp up and energy is stored in the transformer core air gap. When the MOSFET turns off, the energy stored in the gap is transferred to the secondary side of the flyback converter. The flyback transformer leakage inductance (L_l) also has some energy stored in it, which does not get transferred to the secondary. Instead this energy transfers to the combined drain-to-source capacitance seen at the MOSFET C_d, which consists of the MOSFET C_{oss}, the transformer parasitic capacitance, trace capacitances and any other capacitance that may be present at the drain node. An LC ringing occurs with the period set by the C_d resonating with the leakage inductance L_l.

The QR flyback converter operates with a variable switching frequency in DCM such that the MOSFET is turned on at the one of the valleys of the LC ringing. In doing so, the benefits include lower switching losses, higher average efficiency and lower EMI. Valley skipping is used to maintain a lower switching frequency.

To control the peak voltage of the MOSFET drain ringing at switch-off an external capacitance can be added in parallel to the drain source of the MOSFET. In the DEMO_200W_12VDC_LLC design, an auxiliary power supply for providing isolated bias supplies to the primary- and secondary-side circuitry of the converter is realized using the ICE5QR0680AG, which includes an integrated MOSFET and controller in a single package. This IC senses the DC bus input voltage, the zero crossing of the flyback transformer current (ZCD), the feedback voltage employing internal logic to supervise the valley switching operation. On this board, primary-side voltage feedback has been used to avoid the additional cost of isolated feedback circuitry.



Pin Definitions and Functions

Pin		Symbol	Function
DIP-7	DSO-12		
1	1	FB	**Feedback & Burst entry/exit control** **FB** pin combines the functions of feedback control, selectable burst entry/exit control and overload/open loop protection.
2	2	VIN	**Input Line OVP & Brownout** **VIN** pin is connected to the bus via resistor divider (see Figure 1) to sense the line voltage. This pin combines the functions of input Line OVP, Brownout and minimum ZC count setting for low and high line.
3	3	CS	**Current Sense** The **CS** pin is connected to the shunt resistor for the primary current sensing externally and to the PWM signal generator block for switch-off determination (together with the feedback voltage) internally. Moreover, CS pin short to ground protection is sensed by this pin.
4	4	ZCD	**Zero Crossing Detection** **ZCD** pin combines the functions of start up, zero crossing detection and output over voltage protection. During the start up, it is used to provide a voltage level to the gate of power switch CoolMOS™ to charge V_{CC} capacitor.
5	5, 6, 7, 8	DRAIN	**Drain** The **DRAIN** pin is connected to the drain of the integrated CoolMOS™.
7	11	VCC	**VCC(Positive Voltage Supply)** The **VCC** pin is the positive voltage supply to the IC. The operating range is between V_{VCC_OFF} and V_{VCC_OVP}.
8	12	GND	**Ground** The **GND** pin is the common ground of the CoolSET™.
-	9, 10	NC	Not connected.

Figure 33 ICE5QR068AG pin assignment and description

MathCAD design calculations for the auxiliary flyback supply are listed as follows:

Code Listing 13

Input and Output Specifications of Flyback Power Supply

$Vdcmin := 100V$ $Vdcmax := 430V$

$Vo1 := 10V$ $Vaux := 15V$ $\eta := 0.9$

$Vf1 := 0.7V$ $Vf2 := 0.7V$ $Fsw := 40kHz$

$Io1 := 0.3A$ $Iaux := 0.1A$ $Cds := 24pF$

$Po := Vo1 \cdot Io1 = 3\,W$

$$Pin := \frac{Po}{\eta} = 3.333\,W$$

Transformer Design

$Fsw = 4 \times 10^{4}\,kHz$ Switching frequency

$Vr := 90V$ Reflected voltage

$$Dmax := \frac{Vr}{Vr + Vdcmin} = 0.474$$

Flyback transformer inductance

$$Lp_est := \frac{1}{\left[\left[\frac{1}{Vdcmin}\cdot\sqrt{(2\cdot Fsw\cdot Pin)}\cdot\left(\frac{Vdcmin}{Vr}+1\right)\right]+\left(\pi\cdot Fsw\cdot\sqrt{Cds}\right)\right]^{2}} = 7.539\times10^{-3}\,H$$

$Lp := 7.5\cdot10^{-3}H$

$$Iavg := \frac{Pin}{Vdcmin\cdot Dmax} = 0.07\,A \qquad \Delta I := Vdcmin\cdot\frac{Dmax}{Lp\cdot Fsw} = 0.158\,A$$

Code Listing 14

Primary inductance peak current

$$Ipmax := Iavg + \frac{\Delta I}{2} = 0.149\,A$$

Primary and secondary RMS currents

$$Iprms := \sqrt{\left[3 \cdot Iavg^2 + \left(\frac{\Delta I}{2}\right)^2\right] \cdot \frac{Dmax}{3}} = 0.058\,A$$

$$Isrms := Iprms \cdot \sqrt{\frac{1 - Dmax}{Dmax} \cdot \frac{Vr}{Vo1 + Vf1}} = 0.512\,A$$

Transformer core used

EE 16/8/5

Number of primary turns	Np = 187
Number of secondary turns	Ns = 22
Number of auxiliary turns	Naux = 33

11.2 Brown-out protection

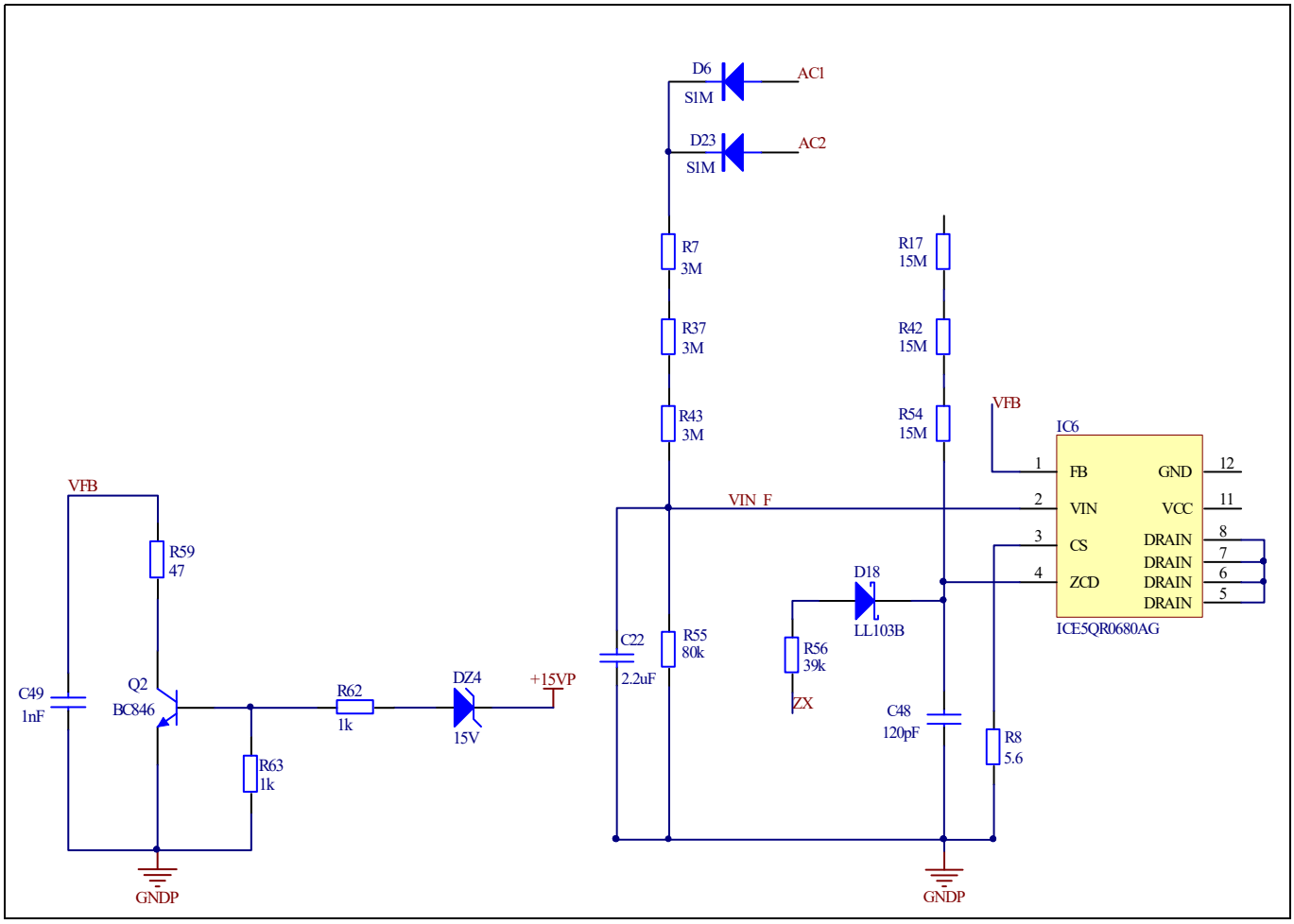


Figure 34 Brown-out protection circuit

The ICE5QR0680 includes a built-in brown-out protection function. The input DC bus voltage is detected at the VIN pin of the IC through a resistor divider. If the voltage at the VIN pin goes below the brown-out threshold of 0.4 V (typical), the IC shuts down, turning back on when this voltage again rises above the brown-in threshold of 0.66 V (typical). Since the auxiliary supply provides the bias voltages to all of the other control ICs this protection is able to shut down the entire system in the event of a brown-out.

With R55 = 80 kΩ, shut-down normally happens when the input falls below around 45 V_{RMS} for the IC to start up at 75 V_{RMS} as desired in this system. However, for this design the brown-out and brown-in thresholds of the ICE5QR0680 are too far apart to meet the specification requirements. To get around this an additional circuit shown in figure 34 increases the brown-out threshold by connecting R15 (180 kΩ) in parallel with R55 after start-up, thereby altering the voltage divider ratio so that the IC shuts down at around 65 V_{RMS} and restarts at 80 V_{RMS}.

12 Bill of Materials (BOM)

Designator	Quantity	Part Number	Manufacturer	Value/Rating
AC	1	0395433103	Molex	Terminal block/Black/3 position/Top entry/5mm/PCB
BH1	1	ATS-PCBT1079	Advanced Thermal Solutions Inc	HEATSINK/ TO-220/VERT/BLACK
BR1	1	KBU6M	GeneSiC Semiconductor	BRIDGE RECT/1PHASE/ 1 kV/6 A/KBU
C1, C2	2	885012007040	Wurth Electronics Inc	1 nF/25 V/0805/5%
C3	1	CC1206KKX7R9BB474	Yageo	0.47 µF/50 V/X7R/1206/10%
C4, C36, C39, C60	4	C1210C473KBRAC7800	Kemet	47 nF/630 V/1210/X7R/10%
C5	1	C0805C474J3RACAUTO	Kemet	0.47 µF/25 V/X7R/0805/5%
C6, C32, C41, C55	4	C0805C104J5RACTU	Kemet	0.1 µF/50 V/0805/ X7R/10%
C7, C23, C24, C30	4	860080472001	Wurth Electronics Inc	39 µF/25 V/RADIAL/20%/105°C
C8	1	08053C103JAT2A	AVX	10 nF/25 V/0805/X7R
C9	1	ECW-FD2J474J	Panasonic Electronic Components	0.47 µF/630 V/5%
C10	1	CC1206JKNPOCBN102	Yageo	1 nF/1 kV/NPO/1206
C11	1	860010473011	Wurth Electronics Inc	220 µF/25 V/RADIAL/20%
C12	0	08053C104JAT2A	AVX	0.1 µF/25 V/0805/5%
C35	0	CC0805JKX7R9BB224	Yageo	0.22 µF/50 V/0805/X7R
C13, C14	2	08051A470FAT2A	AVX	47 pF/100 V/0805/NP0
C15	1	885012207054	Wurth Electronics Inc.	100 pF/25 V/0805/X7R
C16	1	CC1206JKX7R9BB105	Yageo	1 µF/50 V/1206/X7R
C17	1	CC1206JKX7R9BB224	Yageo	0.22 µF/50 V/1206/ X7R
C18	1	860160373013	Wurth Electronics Inc	150 µF/16 V/20%
C19, C20	2	06035C104JAZ2A	AVX	0.1 µF/50 V/0603/ X7R
C21	1	VY2102M29Y5VS63V7	Vishay BC Components	1 nF/300VAC/Y5V/RADIAL
C22, C47, Css	3	CL21B225KAFNFNE	Samsung Electro-Mechanics	2.2 µF/25 V/0805/X7R
C25, C26, C31	3	CC1206KRX7R9BB104	Yageo	0.1 µF/50 V/1206/ X7R
C27	1	UMK325C7106MM-T	Taiyo Yuden	10 µF/50 V/1210/ X7S
C28	1	CC0805JKX7R9BB224	Yageo	0.22 µF/50 V/0805/ X7R

C29, C38, C43, C44, C50	5	08053C105JAT2A	AVX	1 µF/25 V/0805/X7R
C33, C40, C42, C54, C58, C59	6	08053C104JAT2A	AVX	0.1 µF/25 V/0805/5%
C34	1	08053A222FAT2A	AVX	2.2 nF/25 V/0805/NP0
C37, C61	2	C1210C104KBRAC7800	Kemet	100 nF/630 V/1210/X7R
C45, C46	2	C1210C104KBRAC7800	Kemet	100 nF/630 V/1210/X7R
C48	1	CC0805GRNPO9BN121	Yageo	120 pF/50 V/0805/NPO
C49	1	CL10C102JB8NNNC	Samsung Electro-Mechanics	1 nF/50 V/0603/C0G/NP0
C52	1	450VXH180MEFCSN25X30	Rubycon	180 µF/450 V
C57	1	CC1206KRX7R9BB104	Yageo	0.1 µF/50 V/1206/X7R
CF	1	C0805C132J5GAC7800	Kemet	1.3 nF/50 V/0805/5%
CF1	1	860160373013	Wurth Electronics Inc	150 µF/16 V/20%
CO1, CO2, CO3, CO4	4	860080378025	Wurth Electronics Inc	2700 µF/16 V/3Arms
CON1	1			
Cr2	1	BFC238330203	Vishay BC Components	0.02 µF/1 kVDC/RADIAL/5%
Cr3	1	B32672L1622J000	Epcos/TDK	6.2 nF/1.6 kVDC/RADIAL/5%
Css1	1	CL21B155KAFNNNE	Samsung Electro-Mechanics	1.5 µF/25 V/0805/X7R
CT	1	C0805C511J5HACAUTO	Kemet	510 pF/50 V/0805
CT1	1			
CX1, CX2	2	890334024005	Wurth Electronics Inc	0.47 µF/310 VAC/X2
CY1, CY2	2	VY2102M29Y5VS63V7	Vishay	1 nF/300 VAC/Y
D1, D5, D13, D15, D18	5	LL103B-GS08	Vishay	Schottky/30 V/200 mA/SOD80
D2	1	S2D	ON Semiconductor	200 V/2 A/SMB
D3, D4, D8, D12, D20, Dss	6	FDLL4148	ON Semiconductor	100 V/0.2 A/MINIMELF
D6, D23	2	S1M	ON Semiconductor	1 kV/1 A/SMA
D7	1	RS1MB-13-F	Diodes Inc	1000 V/1 A
D9	1	FDLL4148	ON Semiconductor	100 V/0.2 A/MINIMELF
D19	1	LL103B-GS08	Vishay	Schottky/30 V/200 mA/SOD80
D14	1	RS1MB-13-F	Diodes Inc	1000 V/1 A/SMB
D16	1	RS1D-13-F	Diodes Inc	200 V/1 A/SMA
D21	1	MMSZ5242BT1G	ON Semiconductor	Zener/12 V/500 mW/SOD123
DBP	1	S5JC-13-F	Diodes Inc	600 V/5 A/SMC
DPFC	1	IDH08SG60C	Infineon Technologies	600 V/8 A Fast Recovery

DZ1	1	BZT55C10-GS08	Vishay	10 V/0.5 W/MINIMELF
DZ2	1	BZV55-C18,135	Nexperia USA Inc	Zener/18 V/500 mW/SOD80C
DZ3	1	TZMB12-GS18	Vishay Semiconductor Diodes Division	Zener/12 V/500 mW/SOD80
DZ4	1	TZMB15-GS08	Vishay Semiconductor Diodes Division	Zener/15 V/500 mW/SOD80
F1	1	MRT 6.3-BULK	Bel Fuse Inc.	250 V/6.3 A/ Slow Fuse
HS1, HS2	2	WA-T220-101E	Ohmite	HEATSINK AND CLIP FOR TO-220 BLK
HS3	1	ATS-PCBT1079	Advanced Thermal Solutions Inc.	HEATSINK TO-220 VERT BLACK
IC1	1	IR1155S	Infineon Technologies	PFC Controller IC
IC2	1	IR11688	Infineon Technologies	Synchronous rectifier IC
IC3, IC11	2	ZTL431AFTA	Diodes Inc	IC, Voltage Reference, SOT23-3
IC4, IC7	2	SFH6286-2T	Vishay	Opto-isolator, 5.3kV
IC5	1	IRS27952	Infineon Technologies	600 V HB driver IC
IC6	1	ICE5QR0680AG	Infineon Technologies	Aux flyback controller IC
IC9	1	LM358MX	TI	1 MHz operational amplifier
IC10	1	AP331AWRG-7	Diodes Inc	Comparator, SOT23-5
L1	1	TSD-4344	Premier Magnetics	7.5 mH
L2, L3	2	7447071	Wurth Electronics Inc.	470 µH/3 A/110 mΩ/TH
L4	1	SCIH1040HC-R56M	Signal Transformer	0.56 µH/40 A/200 kHz/SMD
LCM	1	744824310	Wurth Electronics Inc	10 mH/3 A
Lm1	1	TSD-4234	Premier Magnetics	724 µH
LPFC	1	TSD-4192	Premier Magnetics	1.1 mH
Lr	1	TSD-4262A	Premier Magnetics	85 µH
M2, M3	2	IPA60R280P6	Infineon Technologies	600 V/8.8 A/TO-220
M7	1	IPP60R120P7	Infineon Technologies	600 V/16 A/TO-220
OUT1	1	1714971	Phoenix Contact	Terminal block/2 positions/Side entry/9.53mm/PCB
Q1	1	ZXTP25040DFHTA	Diodes Inc	PNP/40 V/3 A/SOT23-3
Q2, Q6	2	BC846BLT1G	ON Semiconductor	NPN/65 V/0.1 A/SOT23-3
Q3, Q4	2	IRF4104SPBF	Infineon Technologies	40 V/5.5 mΩ/D2PAK
Q5	1	IPB60R060P7ATMA1	Infineon Technologies	650 V/60 mΩ/D2PAK

Q7	1	BC856B-7-F	Diodes Inc	PNP/65 V/0.1 A/SOT23-3
R1, R2	2	RC1206FR-07249KL	Yageo	249 kΩ/0.25 W/1206/5%
R3	1	CR0805-FX-1000ELF	Stackpole Electronics Inc.	100Ω/0.25 W/0805/1%
R4, R9, R12, R57	4	CRG0805F150K, RNCP0805FTD150K0	Stackpole Electronics Inc., TE Connectivity Passive Product	150 kΩ/0.25 W/0805/1%
R5, R10	2	CRCW1206487KFKEA	Vishay Dale	487 kΩ/0.25 W/1206/1%
R6	1	RMCF0805FT5K60	Stackpole Electronics Inc.	5.6 kΩ/0.125 W/0805/1%
R7, R37, R43	3	RC1206FR-073ML	Yageo	3 MΩ/0.25 W/1206/1%
R8	1	RMCF1206FT5R60	Stackpole Electronics Inc	5.6 Ω/0.25 W/1206/1%
R11	1	CRGCQ1206F100K	TE Connectivity Passive Product	100 kΩ/0.25 W/1206/1%
R13	1	AC05AT0001209JAC00	Vishay Beyschlag	12 Ω/5 W
R14	1	RC0805FR-076K8L	Yageo	6.8 kΩ/0.125 W/0805/5%
R15	1	RC0805FR-07180KL	Yageo	180 kΩ/0.125 W/0805/1%
R16, R26, R64	3	RC0805FR-071KL	Yageo	1 kΩ/0.125 W/0805/1%
R17, R42, R54	3	RMCF1206JT15M0	Stackpole Electronics Inc.	15 MΩ/0.25 W/1206/5%
R18	1	RC1206FR-0743KL	Yageo	43 kΩ/0.25 W/1206/1%
R20, R24	2	RNCP0805FTD4R70	Stackpole Electronics Inc.	4.7 Ω/0.25 W/0805/1%
R21	1	RMCF1206ZT0R00	Stackpole Electronics Inc	0 Ω/0.25 W/1206
R22, R28	2	RMCF0805FT1R00	Stackpole Electronics Inc.	1 Ω/0.25 W/0805/1%
R23, R25, RG	3	RNCP0805FTD10R0	Stackpole Electronics Inc	10 Ω/0.25 W/0805/1%
R30	1	RMCF1206FT1M00	Stackpole Electronics Inc	1 MΩ/0.125 W/0805/1%
R31	1	CRCW12102K20JNEAHP	Vishay Dale	2.2 kΩ/0.75 W/1210/5%
R32	1	RC1206FR-07200RL	Yageo	200 Ω/0.25 W/1206/1%
R33	1	RC1206FR-074K7L	Yageo	4.7 kΩ/0.25 W/1206/1%
R34	1	CRG0805F3K3	TE Connectivity Passive Product	3.3 kΩ/0.125 W/0805/1%
R35	1	RC0805FR-072KL	Yageo	2 kΩ/0.125 W/0805/1%
R36	1	CRGCQ0805F47K	TE Connectivity Passive Product	47 kΩ/0.125 W/0805/1%
R39	1	CRG1206F1K0	TE Connectivity Passive Product	1 kΩ/0.25 W/1206/1%
R40, R41, R60, R71, R72	5	RNCP0805FTD10K0	Stackpole Electronics Inc	10 kΩ/0.25 W/0805/1%,

R46	1	RC1206FR-0710KL	Yageo	10 kΩ/0.25 W/1206/1%
R44	1	RC0805FR-0740K2L	Yageo	40.2 kΩ/0.25 W/0805/1%
R45	1	CRCW120638K3FKEA	Vishay Dale	38.3 kΩ/0.25 W/1206/ 1%
R47, R49, R50	3	RC0805FR-07499KL	Yageo	499 kΩ/0.125 W/0805/1%
R48	1	RC0805FR-07560KL	Yageo	560 kΩ/0.125 W/0805/1%
R51	1	RC0805FR-0712K7L	Yageo	12.7 kΩ/0.125 W/0805/1%
R52	1	RC1206FR-0712K7L	Yageo	12.7 kΩ/0.25 W/1206/1%
R53, R58	2	RC0805JR-074K7L	Yageo	4.7 kΩ/0.125 W/0805/5%
R55	1	PTN0603E8002BST1	Vishay Thin Film	80 kΩ/0.15 W/0603/0.1%
R56	1	RMCF0805FT39K0	Stackpole Electronics Inc	39 kΩ/0.125 W/0805/1%
R59	1	ERJ-3GEYJ470V	Panasonic Electronic Components	47 Ω /0.1 W/0603/5%
R62, R63	2	RMCF0603FT1K00	Stackpole Electronics Inc.	1 kΩ/0.1 W/0603/1%
R73	1	RC1206FR-0749K9L	Yageo	49.9 kΩ/0.25 W/1206/1%
R74, Rmax	2	RNCP1206FTD10K0	Stackpole Electronics Inc	10 kΩ/0.5 W/1206/1%
Rcs3, Rcs4, Rcs5, Rcs6, Rcs8	5	RL2512FK-070R03L	Yageo	0.03 Ω/1 W/2512/1%
RCS11	1	UB5C-0R1F1	Riedon	0.1 Ω/5 W
RG1	1	RC1206FR-07165RL	Yageo	165 Ω/0.25 W/1206/1%
Rss	1	CRG0805F3K0	TE Connectivity Passive Product	3 kΩ/0.125 W/0805/1%
RT	1	RC0805FR-0716KL	Yageo	16 kΩ/0.125 W/0805/1%
Rtrim	1	3296W-1-103LF	Bourns Inc	TRIMMER/10 kΩ/0.5 W/PC PIN/TOP
RV1	1	RC1206FR-0791RL	Yageo	91 Ω/0.25 W/1206/1%
TH1, TH2	2	HF115AC-0.0055-AC-54	Bergquist	Thermal pad
VR1	1	B72210S2321K101	Epcos/TDK	510 V/3.5 kA
W1	1			Jumper
W2	2			Jumper

13 PCB layout

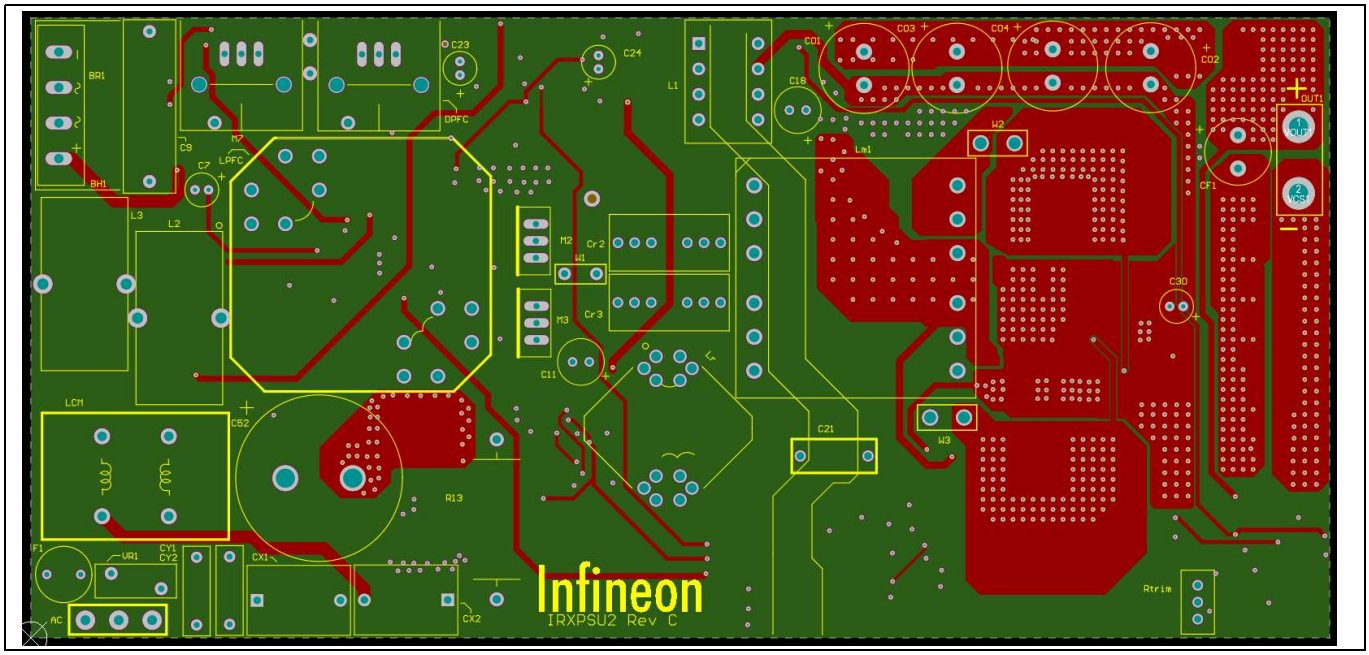


Figure 35 PCB top-side components and traces (first layer)

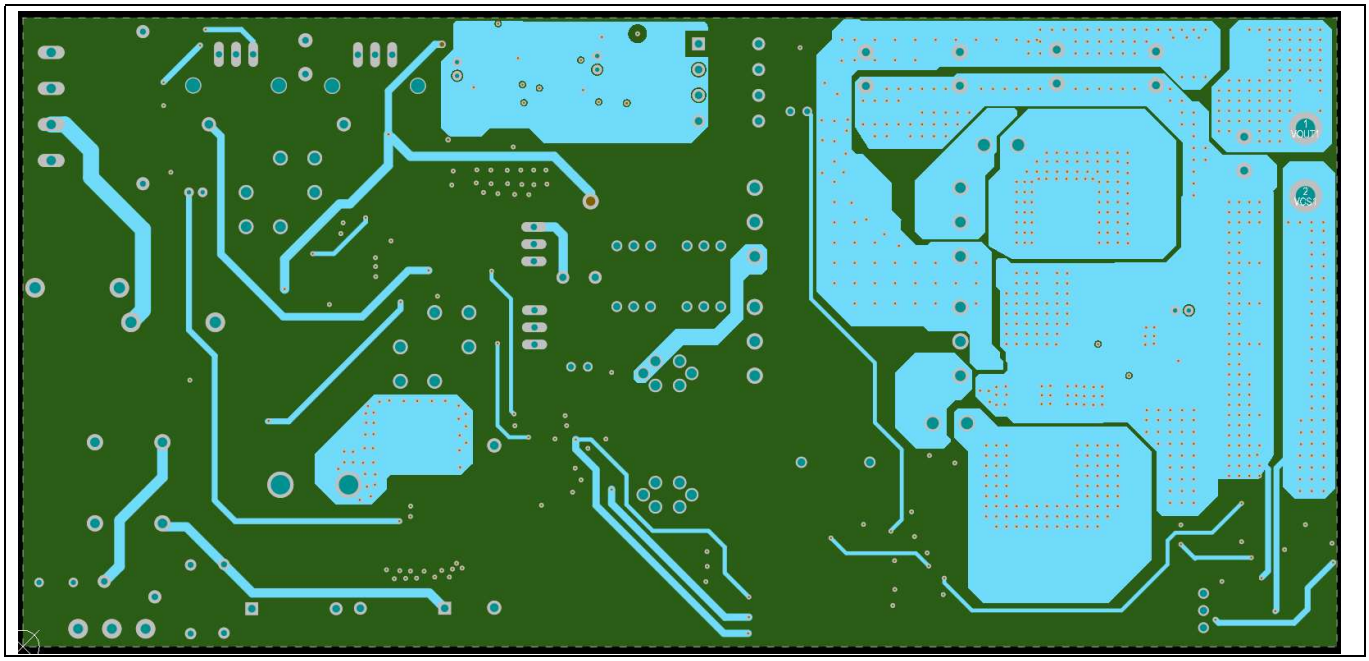


Figure 36 PCB second layer (internal)

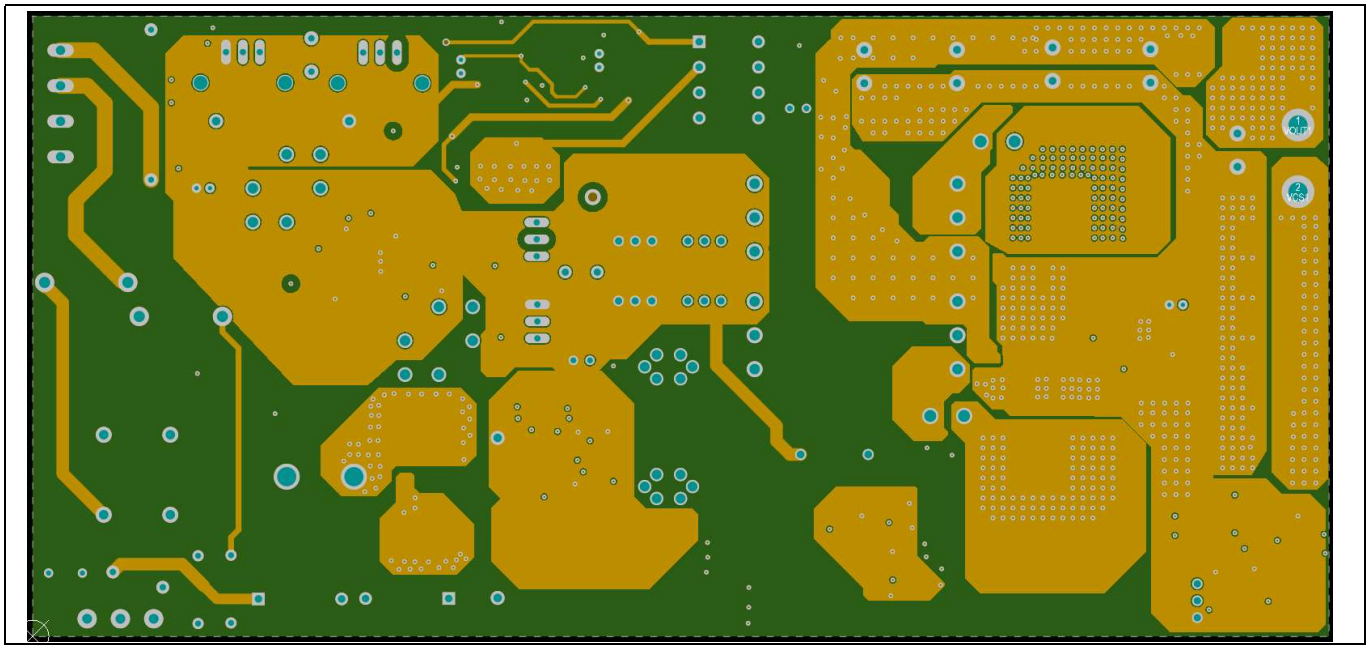


Figure 37 PCB third layer (internal)

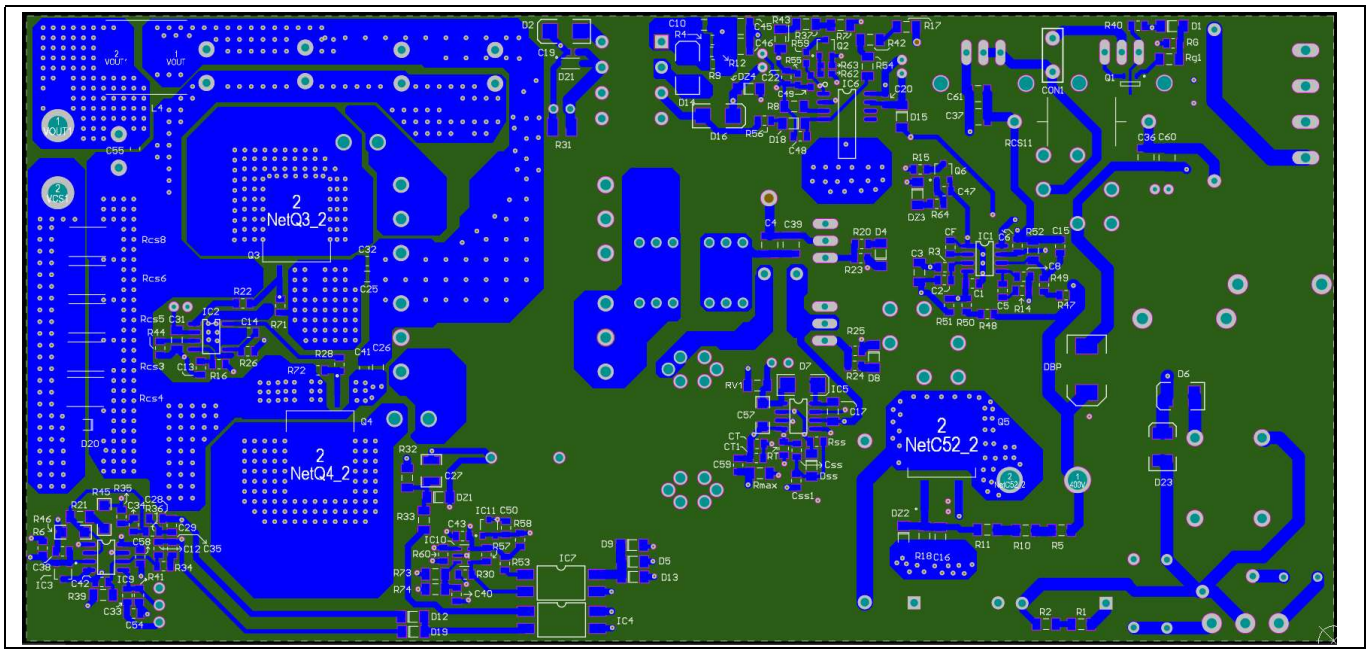


Figure 38 PCB bottom-side components and traces (fourth layer)

Note
Some modifications were made to the original PCB layout shown in the above figures. These modifications can be seen in can be seen in figure 2. The circuit modifications are reflected in the schematics.

13.1 PCB layout guidelines for system optimization

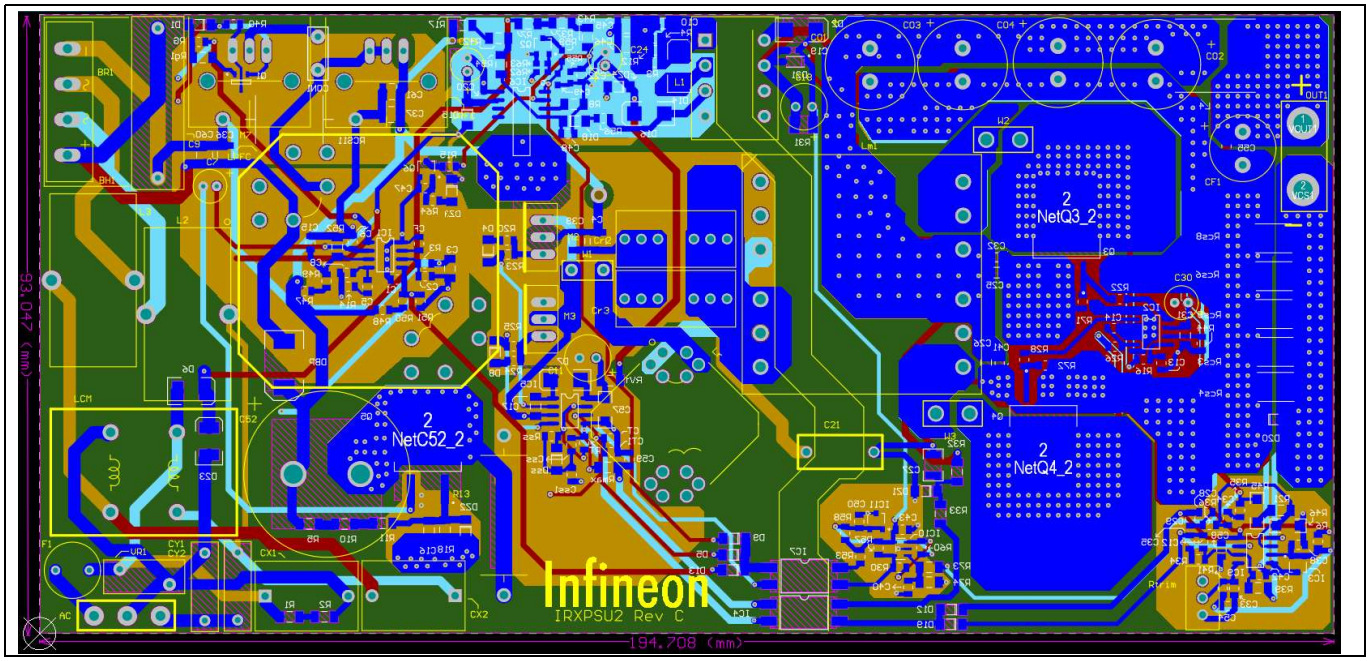


Figure 39 Complete board layout

The primary HF current loop on the left side of the board originates from HF capacitor C9 connecting first to the PFC inductor (LPFC). The other side of the PFC inductor winding is connected to the drain of the MOSFET (M7) and the CS resistor (RCS11). The other end of the CS is connected to the return of the C9 capacitor. To minimize EMI, this HF loop is kept as small as possible. In order to minimize the loop inductance, the return path is kept right beneath the top layer through layer 2.

The second PFC HF current loop originates from C9, LPFC, C37 and RCS11. The other end of the CS resistor R11 returns directly back to C9 through the shortest possible trace, providing the tightest HF current loop. The layout techniques described minimize EMI emitted by the PFC pre-converter stage as far as possible.

For the second-stage LLC resonant converter, the same rules apply – the HF switching loop C39, M2, Lr, Lm and Cr2 should be kept as small as possible. This is the first HF AC loop. The second HF AC loop is formed by M3, Lr, Lm and Cr2. Therefore, in order to keep the layout as tight as possible, these HF AC loop components are placed close to each other thereby minimizing the loop area, and this translates to lower EMI. The LLC half-bridge resonant converter is quite advantageous when it comes to EMI due to the sinusoidal shape of the tank current. With the second stage being a soft-switched topology it is fairly easy to meet conducted emission standards in comparison to the hard-switched topologies.

Aside from EMI considerations it is also extremely important to design the PCB so that PFC and LLC controller ICs are able to operate correctly without suffering from potential interference caused by noise or incorrect grounding. It is also essential that decoupling capacitors C6, C20 and C31 are located right next to IC1, IC5 and IC2 with direct connections to the VCC and COM/0 V pins.

As in all switching power supplies, the signal and power grounds must be kept separate and join together only at the star points or single-point connections, which are at the negative side of the HF capacitor C9 for the PFC section and C39 for the half-bridge LLC section. All the noise-sensitive components at the FREQ, VFB inputs of IC1 (IR1155S) and RT, CT inputs of IC5 (IRS27952) need to be located close to the ICs with short connections to the signal grounds.

On the secondary side of the HB-LLC stage, the MOSFETs are driven by the SR IC IR11688. A decoupling capacitor C31 is located as close as possible to the IC supply pins. The return path is directly beneath the IC on the second layer to keep the loop inductance as small as possible. The HF AC loop on the secondary side of the HB-LLC stage is formed by C25, CO1 and Q4. The other HF AC loop is C25, CO1 and Q3. In order to keep the loops as small as possible, it is preferable to use ceramic capacitors C25, C26, C32 and C41 to close the AC loops and keep the return path right beneath the capacitors and MOSFETs. The current at high frequencies should always follow the path of least impedance to minimize noise. Every signal has a return and as the signal harmonics get higher in frequency, it becomes more important for the return paths to be placed directly under the signal paths, thus leading to field cancelation and reduction of inductance. This is where the concept of ground plane comes into the picture. The ground plane also aids thermal management, as it couples some of the heat to the other side of the PCB, and the ground plane can capacitively link to noisy traces above it, causing reduction in overall noise and EMI [10].

For the flyback power supply, the first loop is formed by C45, transformer pins 1 and 2, the IC drain and R8. The second loop is on the secondary side formed by the transformer pins 8 and 7, D2 and C18 capacitor. These two loops should be kept as small as possible.

14 Transformer and inductor specifications

14.1 PCB inductor

TABLE 1: ELECTRICAL SPECIFICATIONS AT 25 °C

PARAMETER	SPEC LIMITS MIN.	TYP.	MAX.	UNITS
INDUCTANCE: V=250mVrms, F=10kHz 3-10	1.0	1.165	1.3	mH
TURNS RATIO: V=250mVrms, F=10kHz 3-10 : 4-9	---	11.44 : 1	---	±3%
HIPOT: 60Hz at 5mA for 1 second PRIMARY TO SECONDARY	500	---	---	Vrms
PRIMARY TO CORE	500	---	---	Vrms

FIGURE 1: SCHEMATIC DIAGRAM

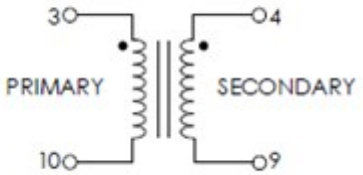
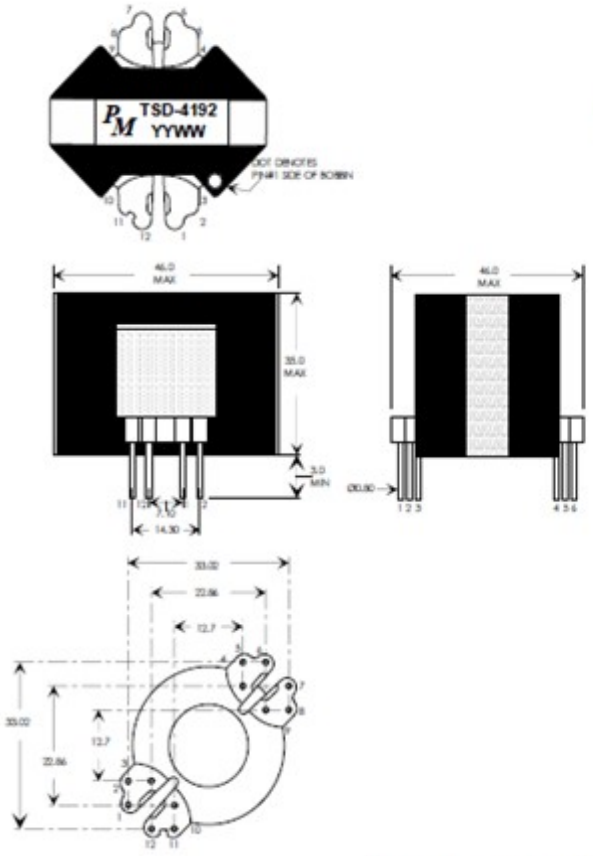


FIGURE 2: PHYSICAL DIMENSIONS IN mm



NOTES:
1) All materials comply with Insulation System Class B.
2) All units comply with the requirements of EU RoHS Directive.
3) All materials per Premier Magnetics UL file #E177139.

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UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN mm
DIMENSIONAL TOLERANCES ARE:
DECIMALS ANGLES
.X ± .4 ± 0° 30'
.XX ± .30
DO NOT SCALE DRAWING

PFC INDUCTOR CONTROL DRAWING	
PREMIER P/N: TSD-4192	REVISION: 05/22/18
ENGR: RISHA PADILLA	REF: 200W, 200V @ 0.5A
APPROVED: PETER PHAM	SHEET: 1 OF 1

Figure 40 PFC boost inductor

14.1 LLC transformer

TABLE 1: ELECTRICAL SPECIFICATIONS AT 25°C

PARAMETER	SPEC LIMITS MIN	TYP	MAX	UNITS
INDUCTANCE 100mV$_{RMS}$, 10kHz L (4-3)	650	724	795	µH
LEAKAGE INDUCTANCE 100mV$_{RMS}$, 100kHz, short 7,9,10,12 LL (4-3)	---	---	5.5	µH
DC RESISTANCE DCR (4-3) DCR (7-9) DCR (10-12)	--- --- ---	--- --- ---	126 1.4 1.4	mΩ mΩ mΩ
TURN RATIO 100mV$_{RMS}$, 10kHz (4-3):(7-9) (4-3):(10-12)	--- ---	16:1 16:1	--- ---	±3% ±3%
HIPOT 60Hz, 5mA MAX, ramp 0.5s, dwell 1s 4 TO 9,10	3,000	---	---	V$_{RMS}$

FIGURE 1: SCHEMATIC

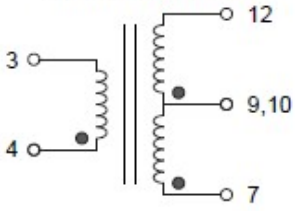
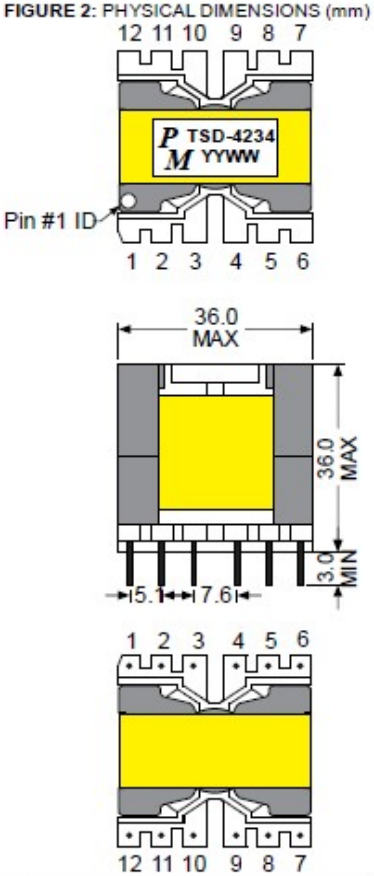


FIGURE 2: PHYSICAL DIMENSIONS (mm)



Notes:
1) Design to comply with the requirements of UL, IEC and CSA Insulation System Class B.
2) All units comply with the requirements of REACH regulation.
3) All units comply with the requirements of EU RoHS Directive.
4) All materials per Premier Magnetics UL file #E177139.

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DIMENSION UNIT mm.
TOLERANCES:
DECIMALS ANGLES
.X ± 0.5 ± 0° 30'
.XX ± 0.3
DRAWING NOT TO SCALE

TRANSFORMER CONTROL DRAWING	
PREMIER P/N: TSD-4234	REVISION: 07/26/18
ENGR: ANDRES ARIAS	REF:
APPROVED: PETER PHAM	SHEET: 1 OF 1

Figure 41 Half-bridge LLC resonant transformer

14.2 Resonant inductor

TABLE 1: ELECTRICAL SPECIFICATIONS AT 25 °C

PARAMETER	SPEC LIMITS MIN.	TYP.	MAX.	UNITS
INDUCTANCE: V=250mVrms, F=10kHz 1,2 - 11,12	76	85	94	µH
DCR: 1,2 - 11,12	---	---	45	mΩ

FIGURE 1: SCHEMATIC DIAGRAM

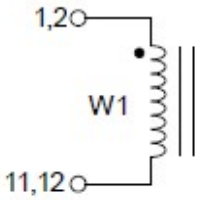
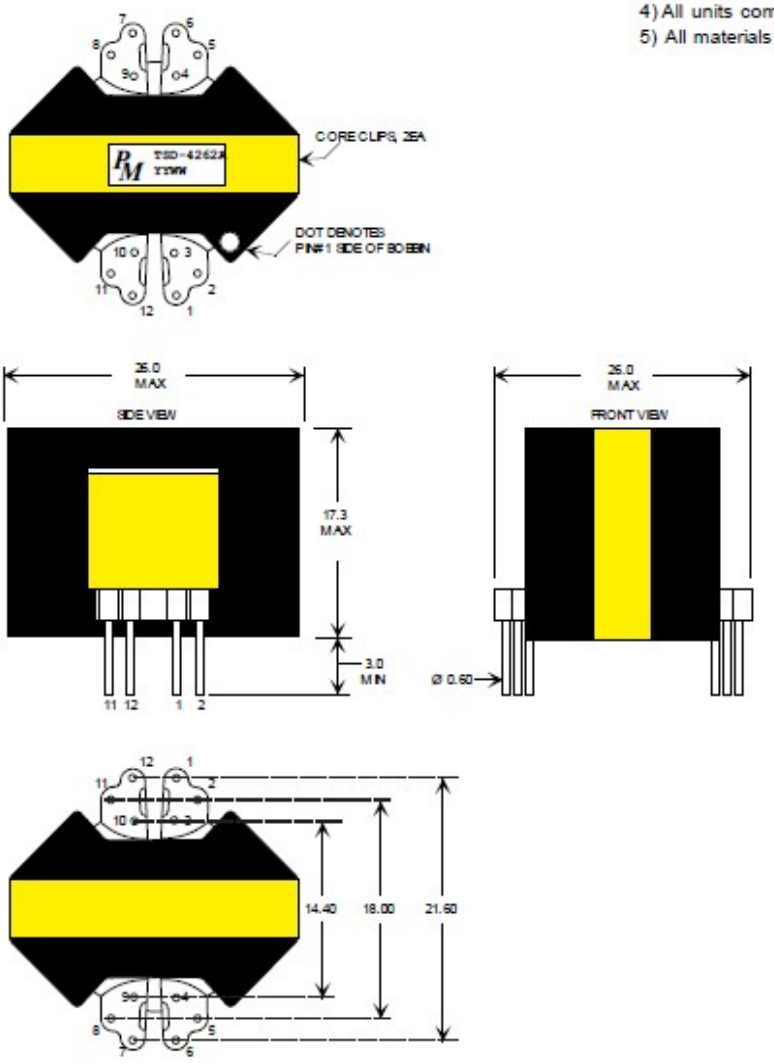


FIGURE 2: PHYSICAL DIMENSIONS IN mm

Notes:
1) Design to comply with the requirements of UL/CSA/IEC 60950-1.
2) All materials comply with Insulation System Class B.
3) All units comply with the requirements of EU RoHS Directive.
4) All units comply with the requirements of REACH Regulation.
5) All materials per Premier Magnetics UL file #E177139.



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DIMENSIONS ARE IN mm
DIMENSIONAL TOLERANCES ARE:
DECIMALS ANGLES
X ± .4 ±0° 30'
XX ± .30
DO NOT SCALE DRAWING

INDUCTOR CONTROL DRAWING	
PREMIER P/N: TSD-4262A	REVISION: 01/23/19
ENGR: RISHA PADILLA	REF:
APPROVED: PETER PHAM	SHEET: 1 OF 1

Figure 42 LLC resonant inductor

14.3 Flyback transformer (coupled inductor)

TABLE 1: ELECTRICAL SPECIFICATIONS AT 25 °C

PARAMETER	SPEC LIMITS MIN.	TYP.	MAX.	UNITS
INDUCTANCE: V=0.250Vrms, F=40kHz 2-1	6.75	7.50	8.25	mH
TURNS RATIO: V=0.250Vrms, F=40kHz 2-1 : 3-4	---	5.67 : 1	---	±3%
2-1 : 8-7	---	8.50 : 1	---	±3%
HIPOT: 60Hz at 5mA for 1 second PINS 2,3 TO PIN 8	3000	---	---	Vrms

FIGURE 1: SCHEMATIC DIAGRAM

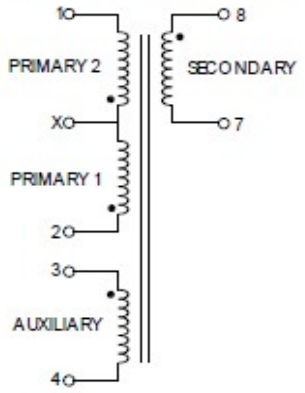
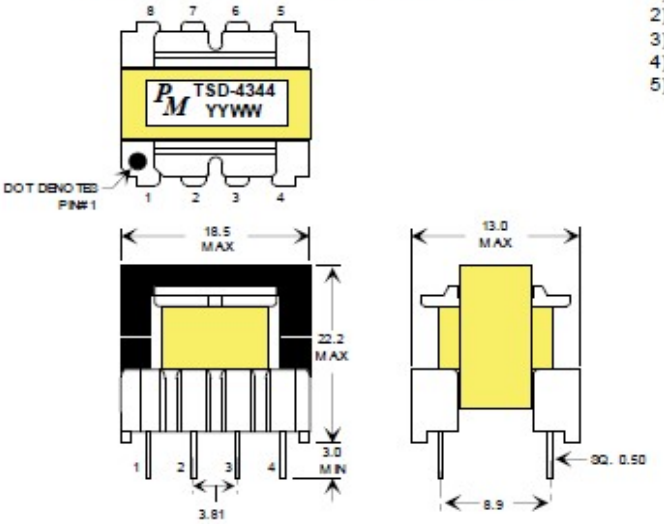


FIGURE 2: PHYSICAL DIMENSIONS IN mm



NOTES:
1) Design to comply with the requirements of UL 60950-1.
2) All materials comply with Insulation System Class B.
3) All units comply with the requirements of EU RoHS Directive.
4) All units comply with the requirements of REACH Regulation.
5) All materials per Premier Magnetics UL file #E177139.

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UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN mm
DIMENSIONAL TOLERANCES ARE:
DECIMALS ANGLES
X ± .4 ±0° 30'
XX ± .30
DO NOT SCALE DRAWING

TRANSFORMER CONTROL DRAWING	
PREMIER P/N: TSD-4344	REVISION: 01/30/19
ENGR: RISHA PADILLA	REF: IRXPSU2
APPROVED: PETER PHAM	SHEET: 1 OF 1

Figure 43 Flyback transformer

15 Test results

15.1 Operation under different line and load conditions

Table 2 Input 120 V $AC_{(RMS)}$

P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	PF	iTHD (%)	Efficiency (%)
15.94	12	1	12	0.912	13.7	75.28
28.57	12	2	24	0.961	14	84.00
40.77	11.99	3	35.97	0.982	6.4	88.23
53.8	11.99	4	47.96	0.985	7.94	89.14
66.58	11.99	5	59.95	0.989	7.5	90.04
79.18	11.97	6	71.82	0.992	6.77	90.70
91.98	11.96	7	83.72	0.993	6.572	91.02
104.71	11.96	8	95.68	0.995	6.65	91.38
117.32	11.95	9	107.55	0.995	3.45	91.67
130.3	11.93	10	119.3	0.996	3.083	91.56
143.25	11.92	11	131.12	0.996	3.09	91.53
156.35	11.91	12	142.92	0.997	3.087	91.41
169.6	11.9	13	154.7	0.997	2.7	91.21
182.84	11.89	14	166.46	0.997	2.8	91.04
196.31	11.89	15	178.35	0.997	2.77	90.85
209.8	11.88	16	190.08	0.998	2.77	90.60

Table 3 Input 230V $AC_{(RMS)}$

P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	PF	iTHD (%)	Efficiency (%)
15.942	12	1	12	0.544	14.25	75.27
28.29	12	2	24	0.74	10	84.84
40.88	11.99	3	35.97	0.836	9.57	87.99
52.98	11.99	4	47.96	0.889	9.89	90.52
65.32	11.99	5	59.95	0.923	9.84	91.78
77.77	11.98	6	71.88	0.939	9.56	92.43
90.43	11.97	7	83.79	0.951	9.76	92.66
102.9	11.96	8	95.68	0.96	9.55	92.98
115.39	11.95	9	107.55	0.967	8.34	93.21
128.12	11.93	10	119.3	0.973	6.2	93.12
140.97	11.92	11	131.12	0.977	3.66	93.01
153.83	11.91	12	142.92	0.979	3	92.91
166.74	11.9	13	154.7	0.981	2.76	92.78
179.79	11.89	14	166.46	0.982	2.80	92.59
192.9	11.89	15	178.35	0.984	2.77	92.46
205.9	11.88	16	190.08	0.986	2.61	92.32

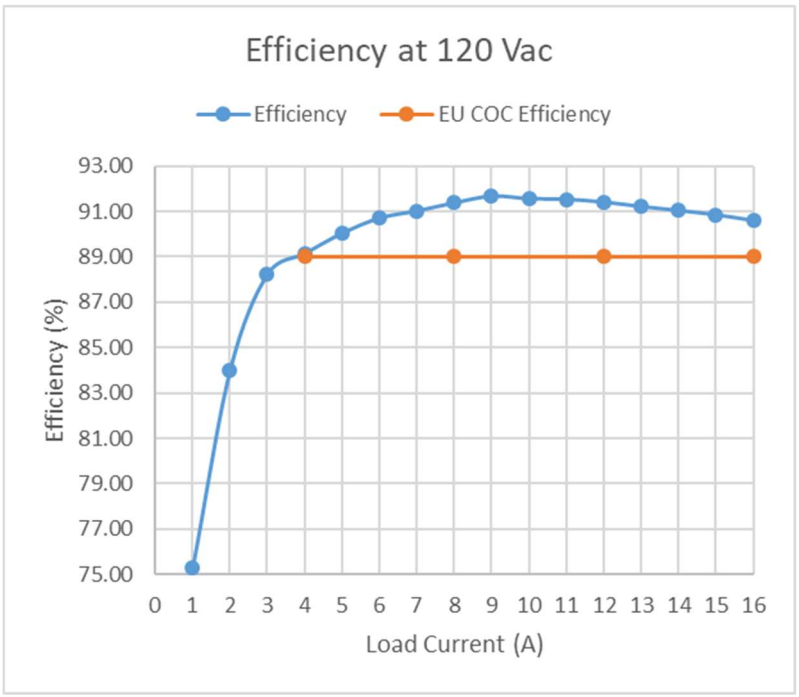


Figure 44 Efficiency at 120 V AC_{RMS} input

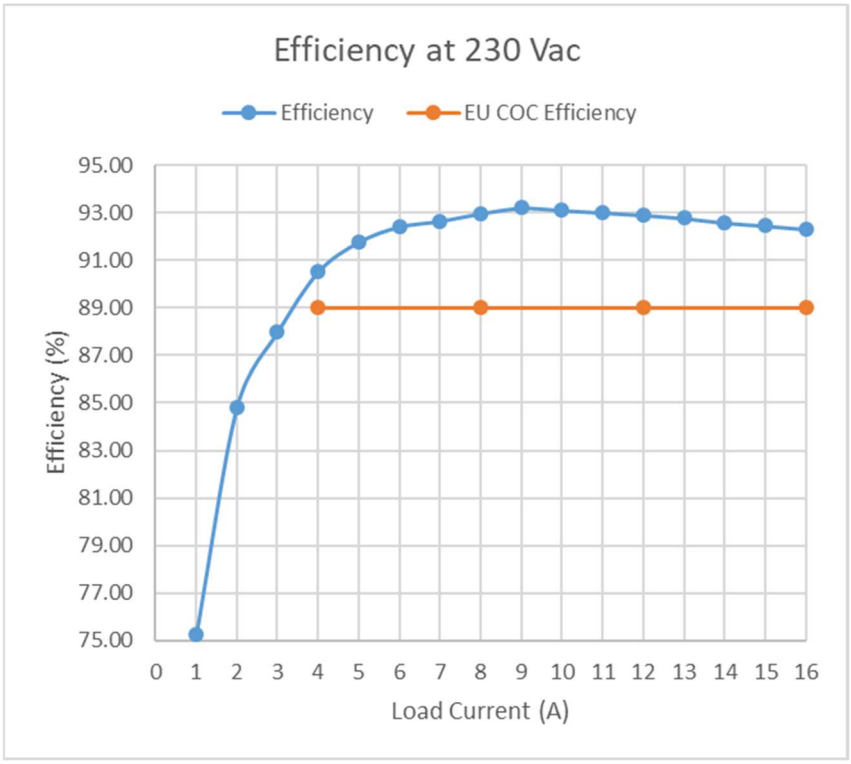


Figure 45 Efficiency at 230 V AC_{RMS} input

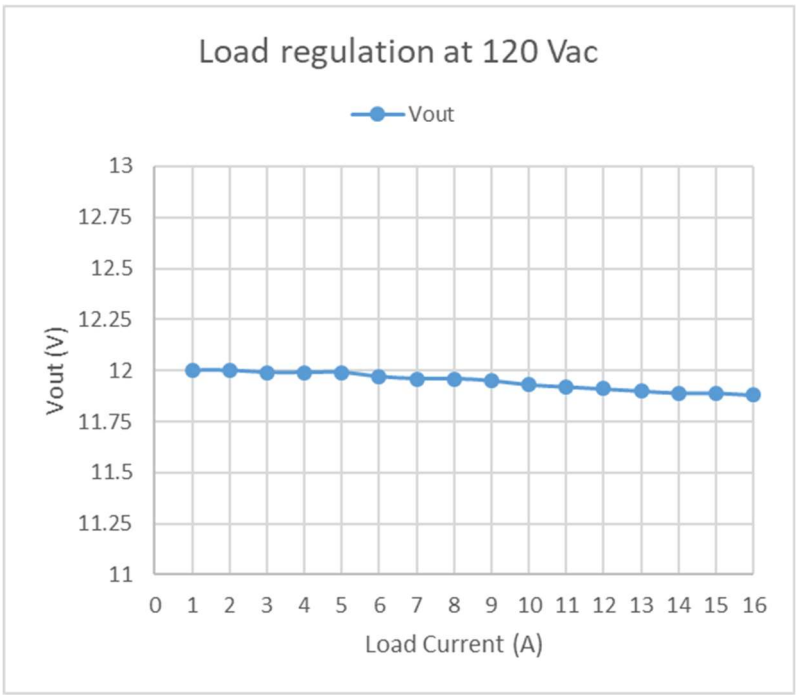


Figure 46 Load regulation at 120 V AC_{RMS} input

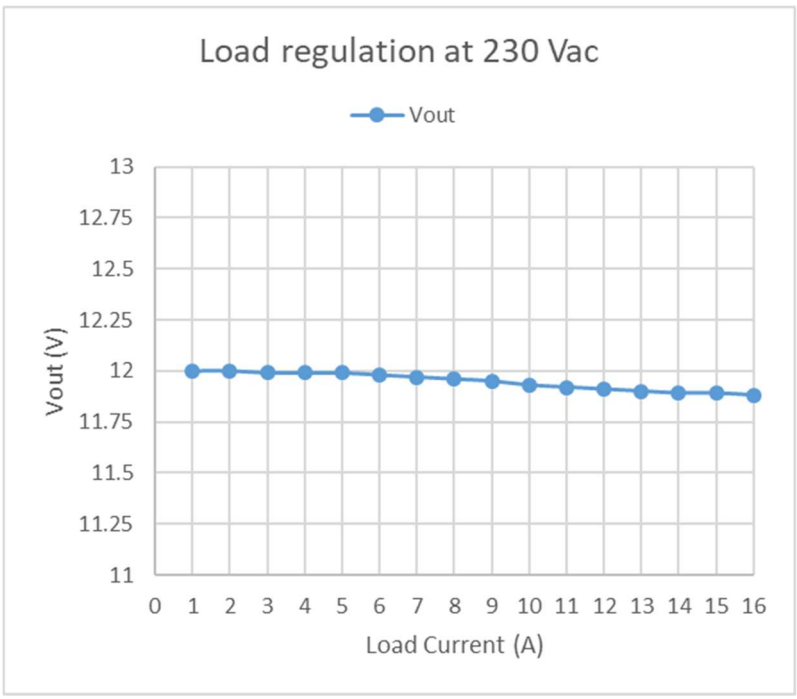


Figure 47 Load regulation at 230 V AC_{RMS} input

15.2 Power factor and input current harmonics (iTHD)

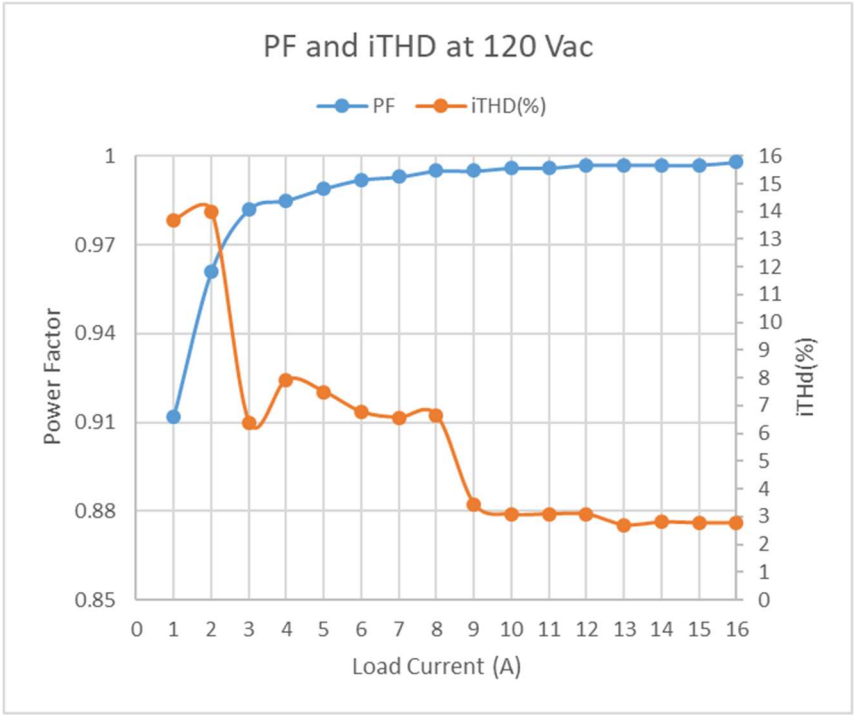


Figure 48 Power factor and iTHD at 120 V AC_{RMS} input

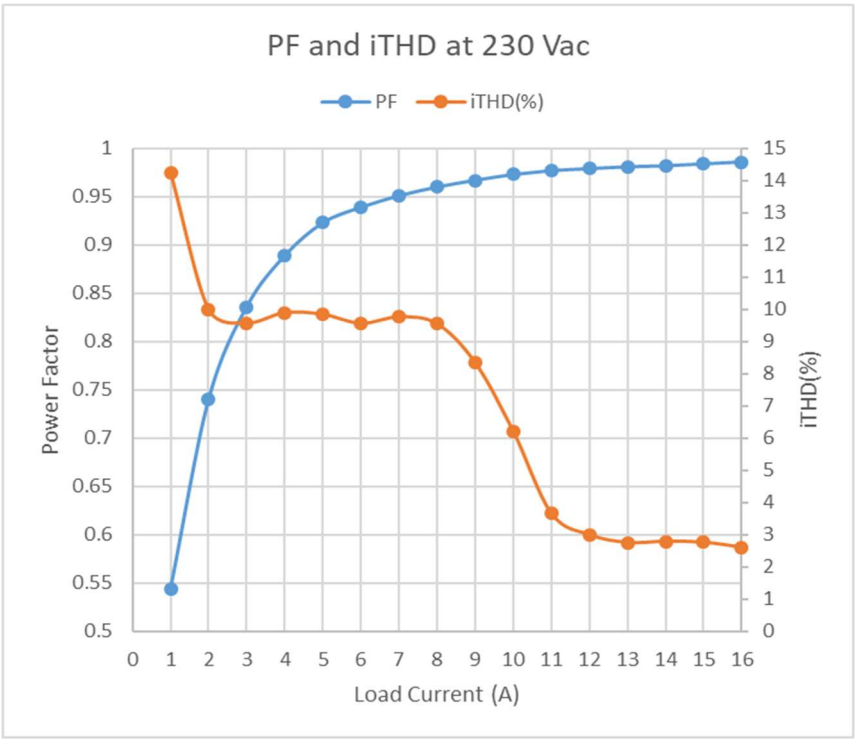
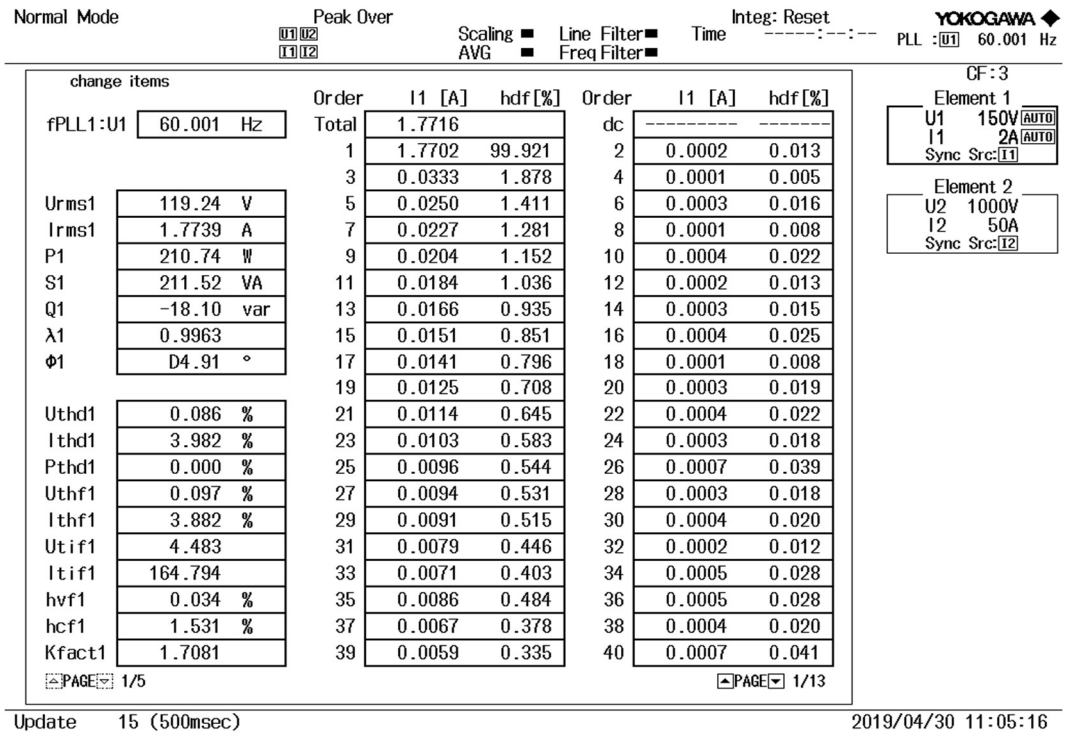


Figure 49 Power factor and iTHD at 230 V AC_{RMS} input

An international standard, the IEC 1000-3-2 (EN 61000-3-2), defines the rules for the current distortion affecting mains-powered devices. This standard does not discuss the power factor directly, but fixes current harmonic limits [4].

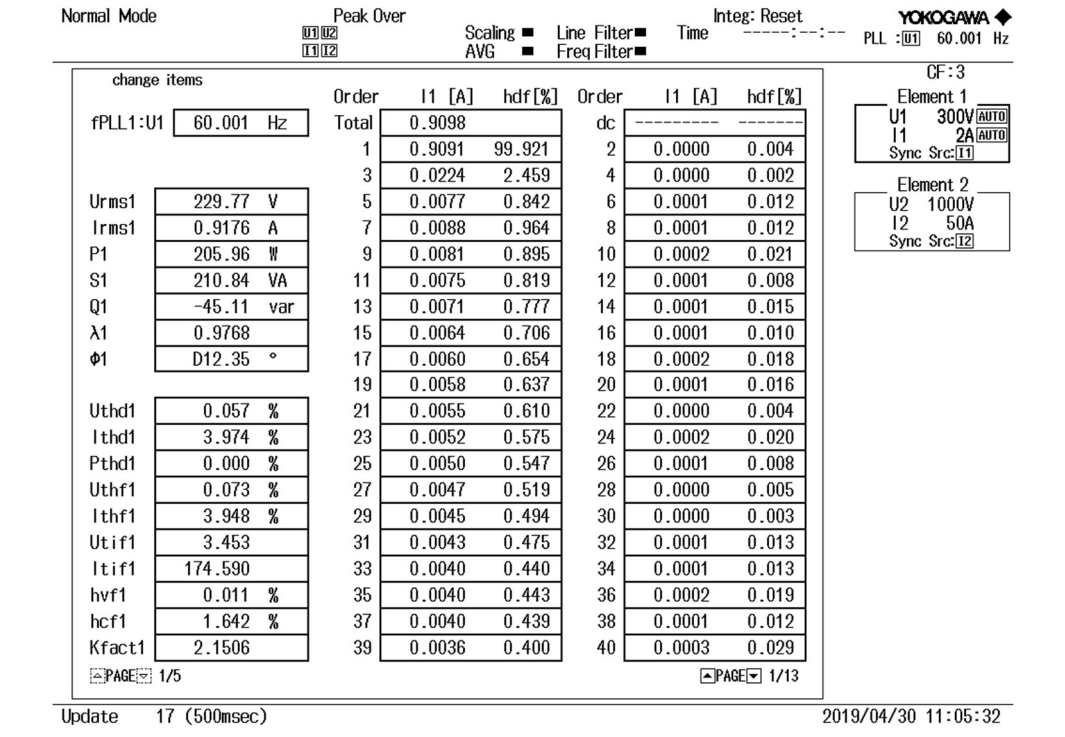
Table 4 EN61000-3-2 class D limits for system power greater than 75 W

	Harmonics limits class D according EN 61000-3-2 for system power greater than 75 W and less than 600 W	
	Harmonics order n	**mA_{RMS}/W**
Requirements	3	3.4
	5	1.9
	7	1.0
	9	0.5
	11	0.35
	13	0.296
	15 less than or equal to n less than or equal to 39	3.85/n



Order	I1 [A]	hdf[%]	Order	I1 [A]	hdf[%]
Total	1.7716		dc	---------	-------
1	1.7702	99.921	2	0.0002	0.013
3	0.0333	1.878	4	0.0001	0.005
5	0.0250	1.411	6	0.0003	0.016
7	0.0227	1.281	8	0.0001	0.008
9	0.0204	1.152	10	0.0004	0.022
11	0.0184	1.036	12	0.0002	0.013
13	0.0166	0.935	14	0.0003	0.015
15	0.0151	0.851	16	0.0004	0.025
17	0.0141	0.796	18	0.0001	0.008
19	0.0125	0.708	20	0.0003	0.019
21	0.0114	0.645	22	0.0004	0.022
23	0.0103	0.583	24	0.0003	0.018
25	0.0096	0.544	26	0.0007	0.039
27	0.0094	0.531	28	0.0003	0.018
29	0.0091	0.515	30	0.0004	0.020
31	0.0079	0.446	32	0.0002	0.012
33	0.0071	0.403	34	0.0005	0.028
35	0.0086	0.484	36	0.0005	0.028
37	0.0067	0.378	38	0.0004	0.020
39	0.0059	0.335	40	0.0007	0.041

Figure 50 Power analyzer read-out at 120 V AC_{RMS} input with 16 A load



Order	I1 [A]	hdf[%]	Order	I1 [A]	hdf[%]
Total	0.9098		dc	---------	-------
1	0.9091	99.921	2	0.0000	0.004
3	0.0224	2.459	4	0.0000	0.002
5	0.0077	0.842	6	0.0001	0.012
7	0.0088	0.964	8	0.0001	0.012
9	0.0081	0.895	10	0.0002	0.021
11	0.0075	0.819	12	0.0001	0.008
13	0.0071	0.777	14	0.0001	0.015
15	0.0064	0.706	16	0.0001	0.010
17	0.0060	0.654	18	0.0002	0.018
19	0.0058	0.637	20	0.0001	0.016
21	0.0055	0.610	22	0.0000	0.004
23	0.0052	0.575	24	0.0002	0.020
25	0.0050	0.547	26	0.0001	0.008
27	0.0047	0.519	28	0.0000	0.005
29	0.0045	0.494	30	0.0000	0.003
31	0.0043	0.475	32	0.0001	0.013
33	0.0040	0.440	34	0.0001	0.013
35	0.0040	0.443	36	0.0002	0.019
37	0.0040	0.439	38	0.0001	0.012
39	0.0036	0.400	40	0.0003	0.029

Figure 51 Power analyzer read-out at 230 V AC_{RMS} input with 16 A load

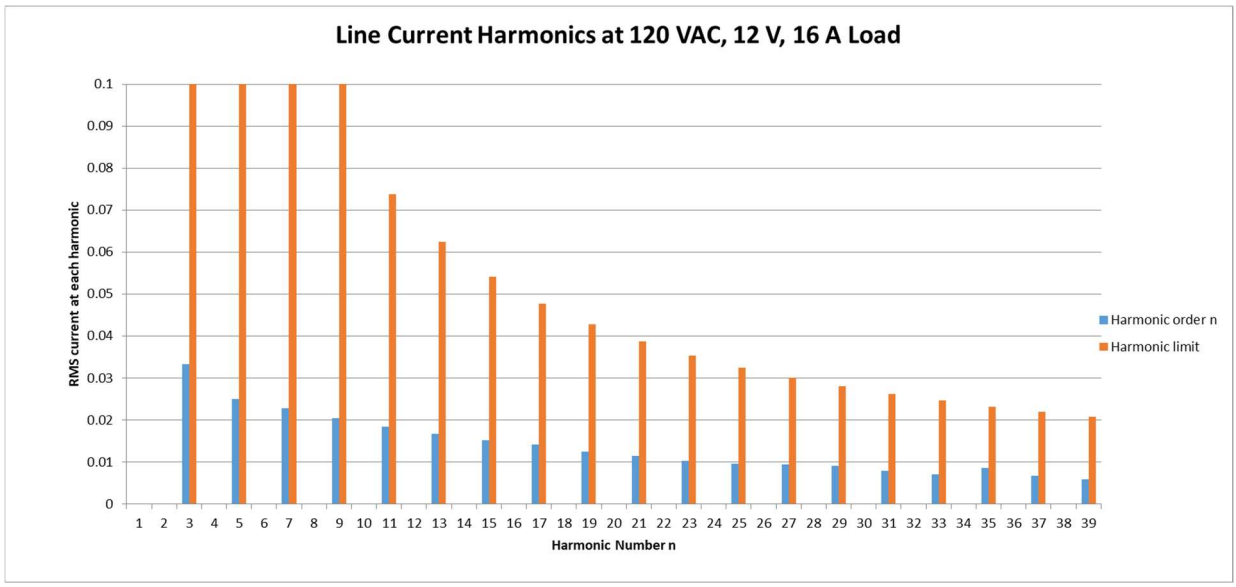


Figure 52 Input current harmonics compared with class D limits at 120 V AC_{RMS} input with 16 A load

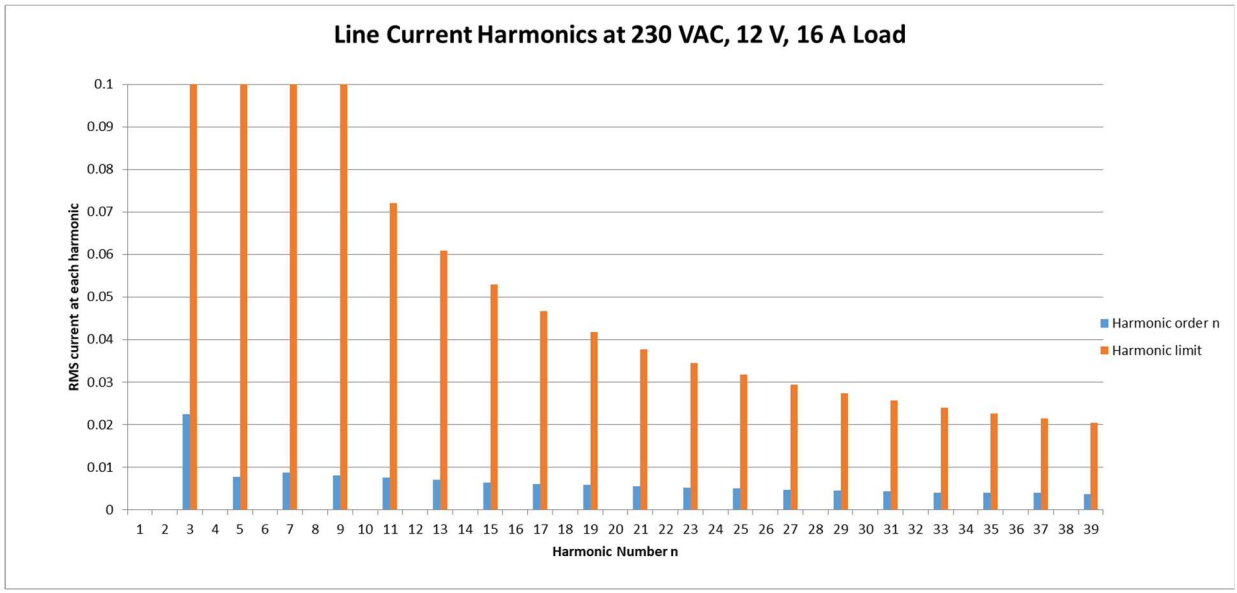


Figure 53 Input current harmonics compared with class D limits at 230 V AC_{RMS} input with 16 A load

It is shown that the input current harmonics at full load are well within the class D limits of standard EN 61000-3-2 at both nominal input voltages.

15.1 Operating waveforms

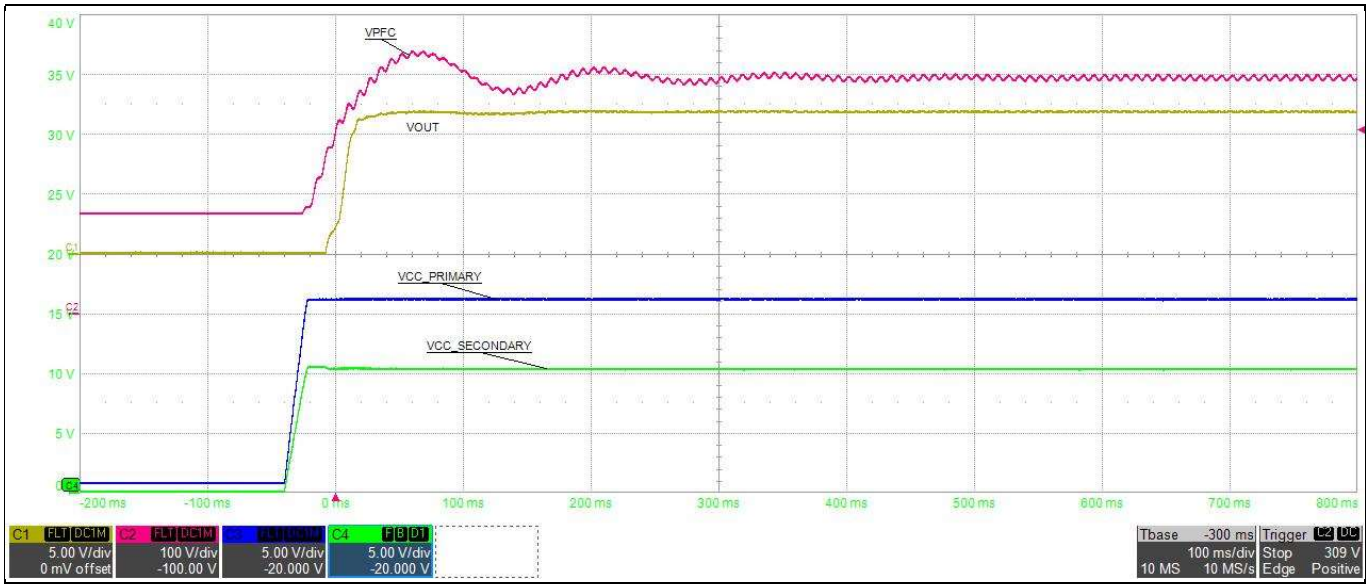


Figure 54 **120 V AC_{RMS} start-up at 100 percent load: output voltage V_{OUT} (yellow), V_{CC} primary (blue), V_{PFC} (red), V_{CC} secondary (green)**

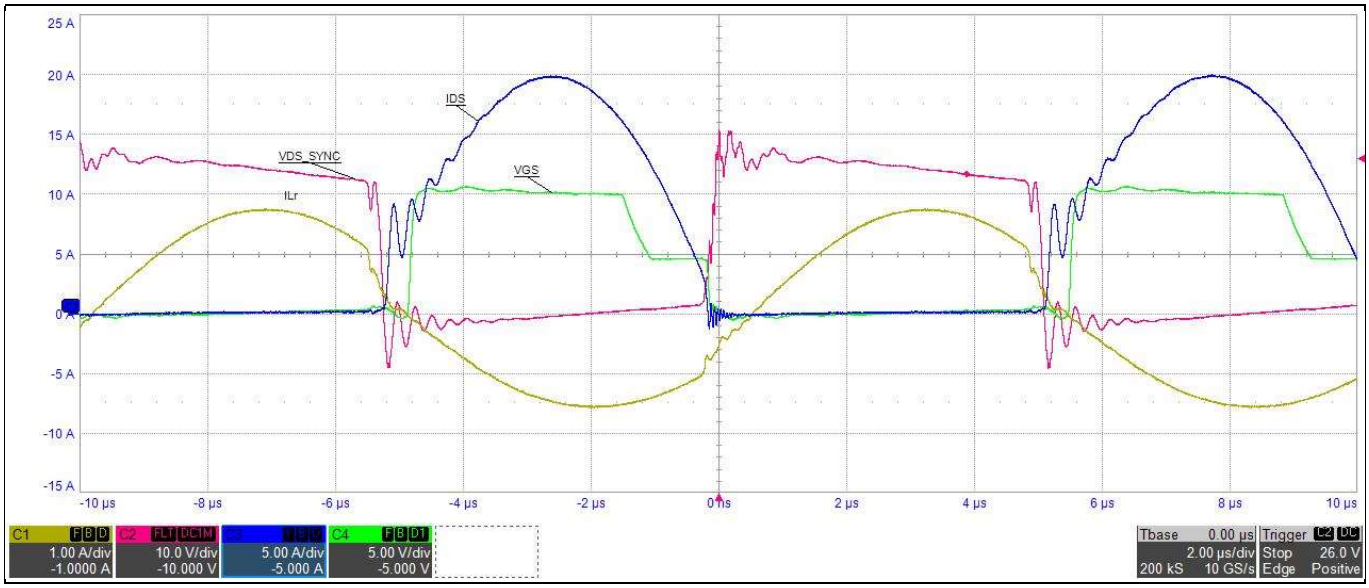


Figure 55 **Steady-state operation at 100 percent load: resonant inductor current (yellow), V_{DS} of synchronous MOSFET (red), V_{GS} gate (green), I_{DS} of synchronous MOSFET (blue)**

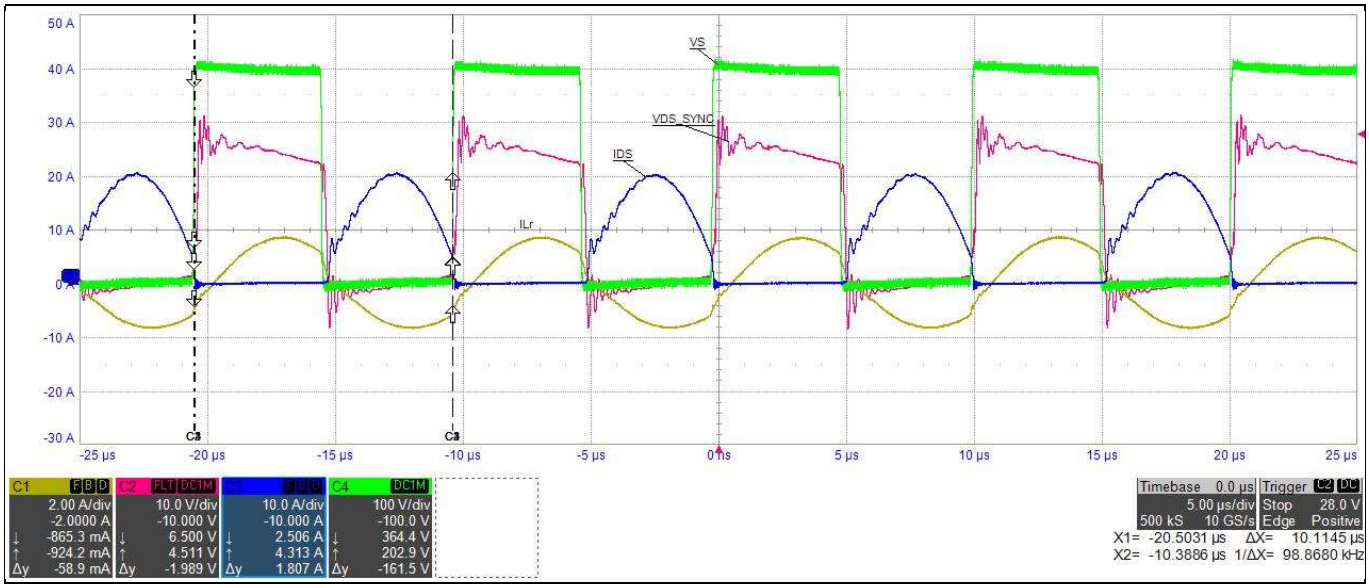


Figure 56 **Steady-state operation at 100 percent load: resonant inductor current (yellow), V_{DS} of synchronous MOSFET (red), switch node of half-bridge VS (green), I_{DS} (blue)**

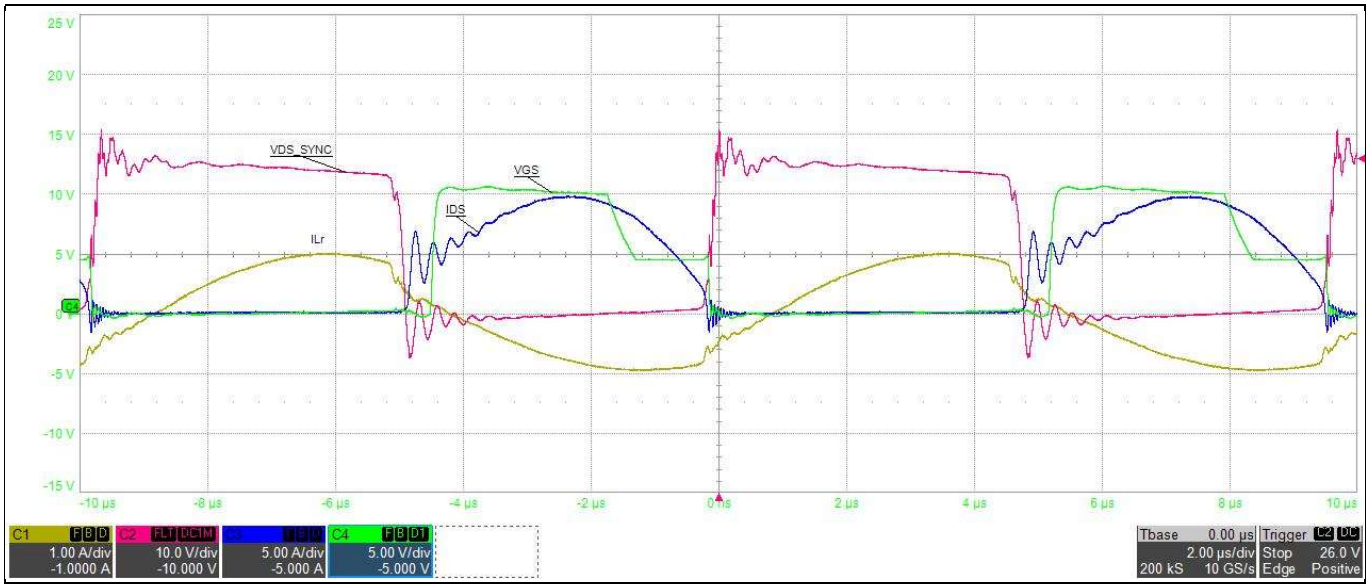


Figure 57 **Steady-state operation at 50 percent load: resonant inductor current (yellow), V_{DS} of synchronous MOSFET (red), V_{GS} gate (green), I_{DS} (blue)**

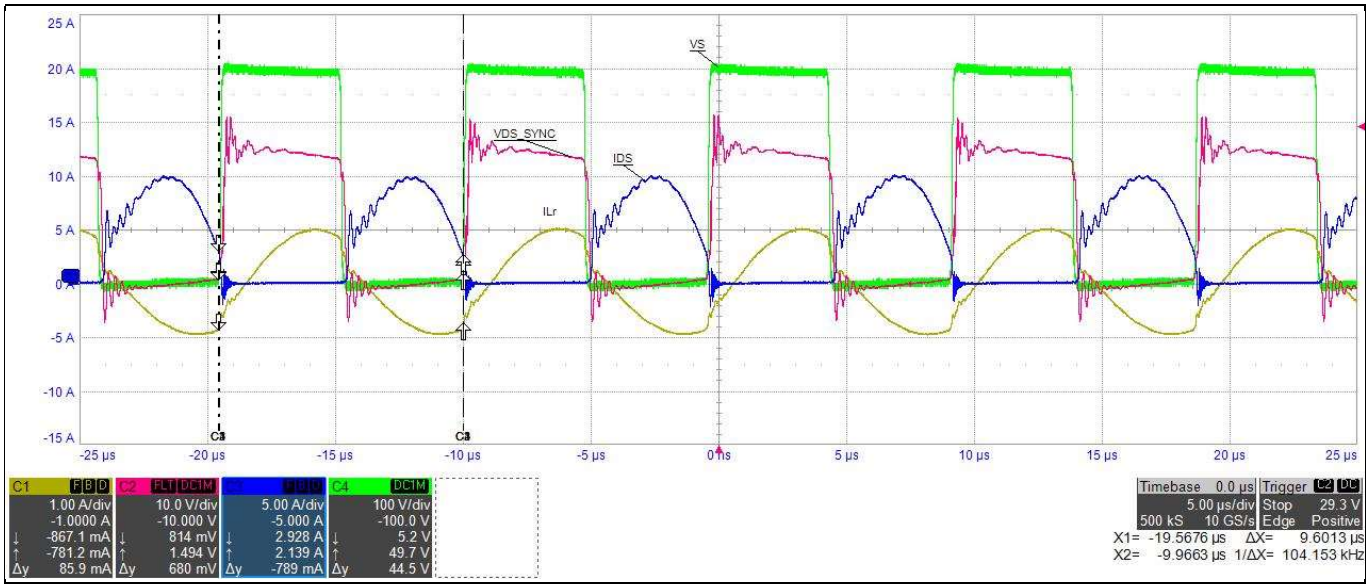


Figure 58 **Steady-state operation at 50 percent load: resonant inductor current (yellow), V_{DS} of synchronous MOSFET (red), switch node of half-bridge VS (green), I_{DS} (blue)**

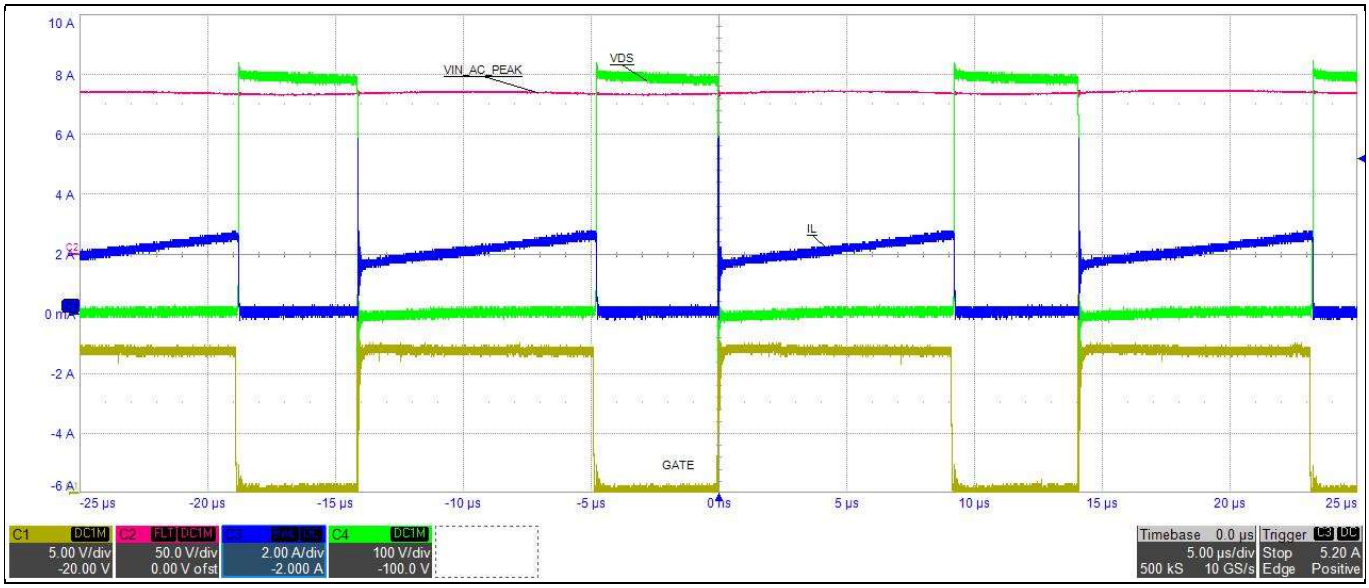


Figure 59 **Steady-state waveform at 120 V AC_{RMS} peak 100 percent load: PFC inductor current (blue), input V AC peak (red), PFC MOSFET drain (green), PFC MOSFET gate (yellow)**

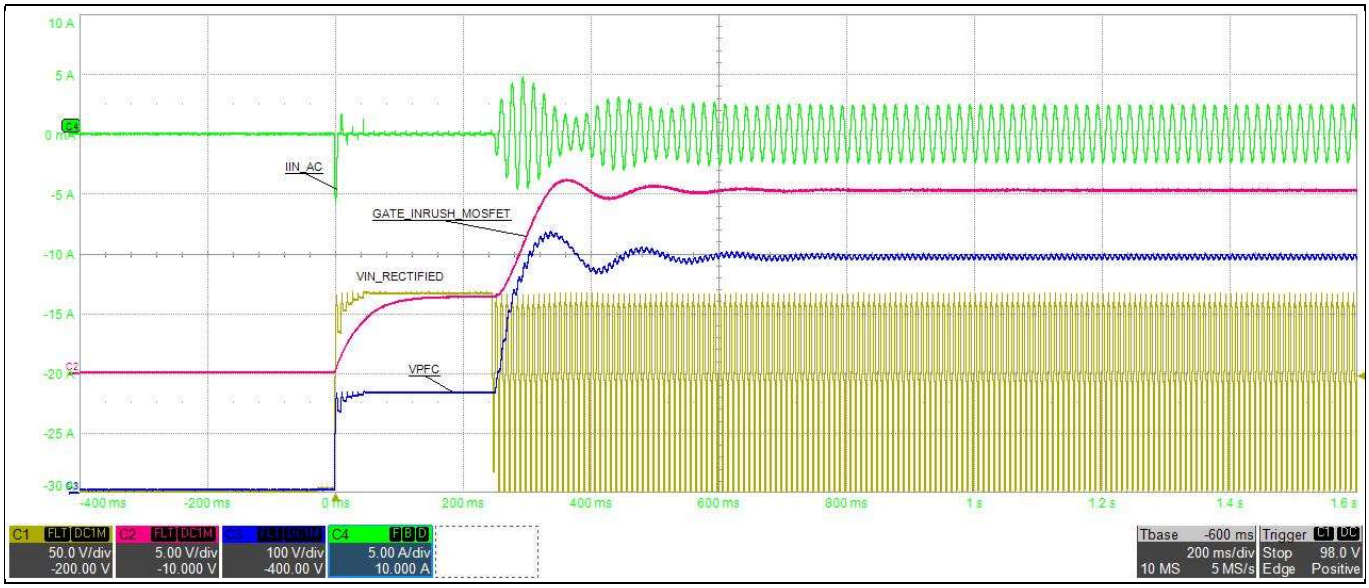


Figure 60 **120 V AC_{RMS} start-up at 100 percent load: input line current (green), gate of inrush MOSFET (red), PFC voltage (blue), input AC rectified voltage (yellow)**

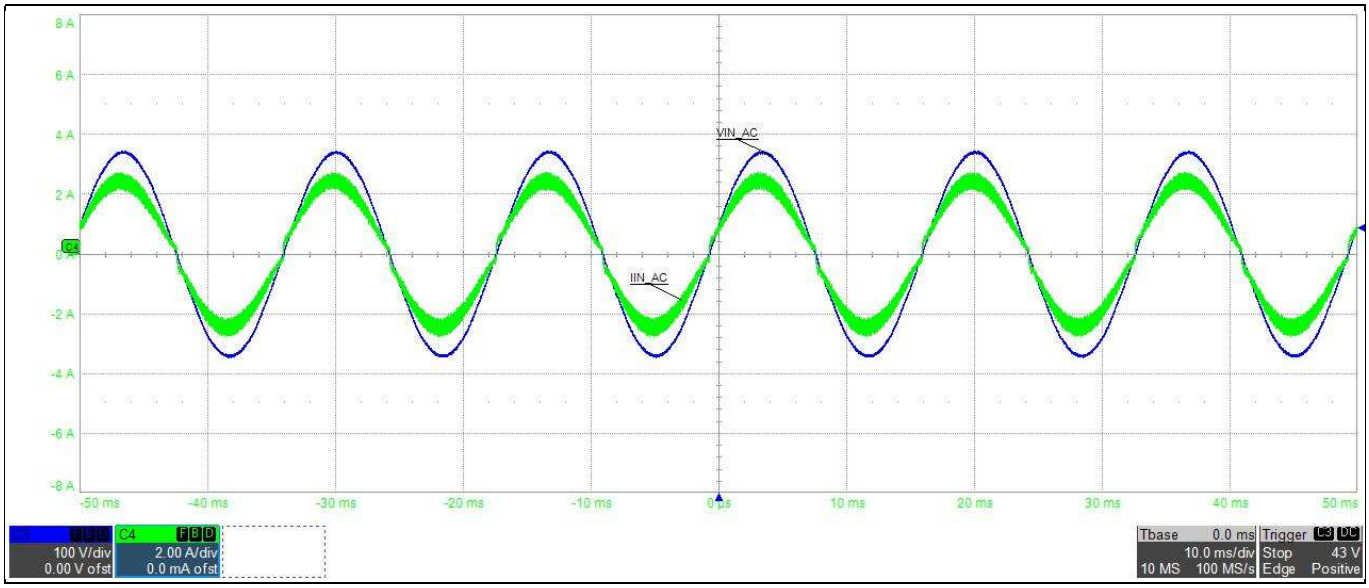


Figure 61 **Steady-state waveform at 120 V AC_{RMS} 100 percent load: input AC voltage (blue), input AC current (green)**

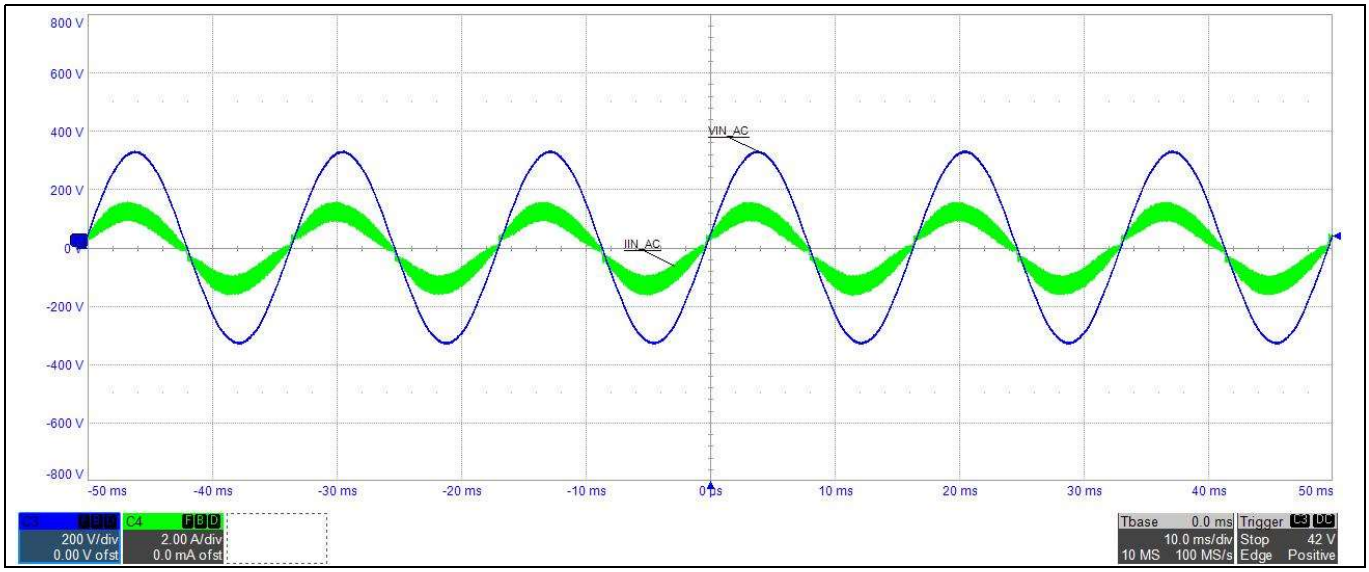


Figure 62 **Steady-state waveform at 230 V AC_{RMS} 100 percent load: input AC voltage (blue), input AC current (green)**

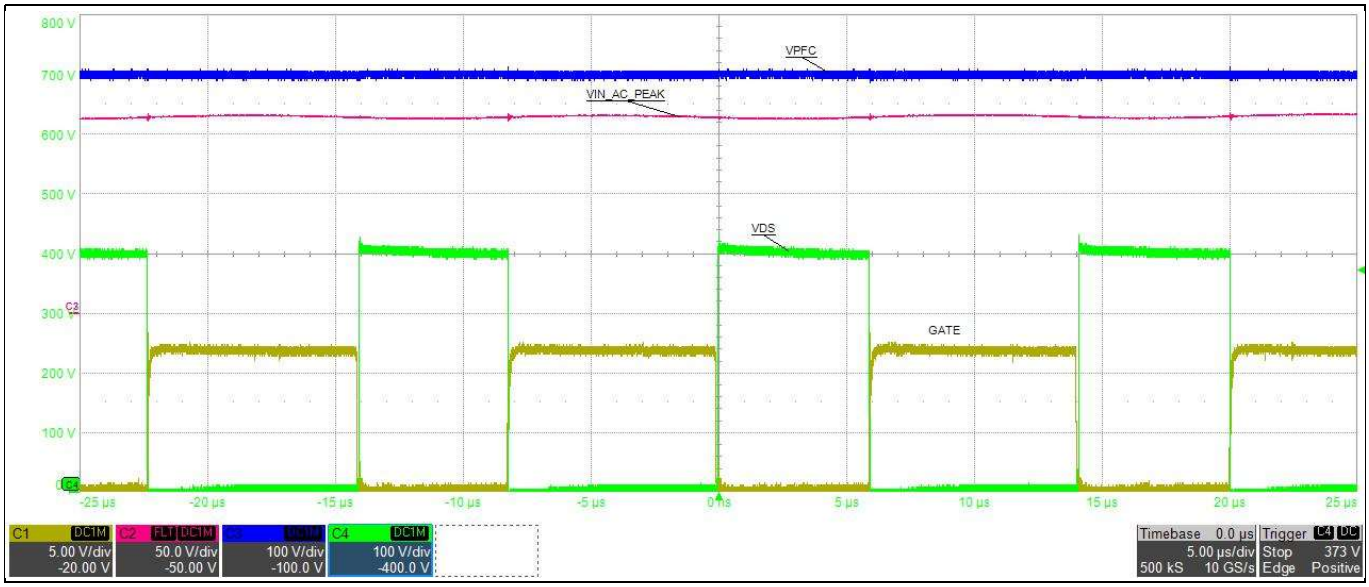


Figure 63 **Steady-state waveform at 120 V AC_{RMS} peak 100 percent load: PFC output voltage (blue), Input V AC peak (red), MOSFET V_{DS} (green), MOSFET gate (yellow)**

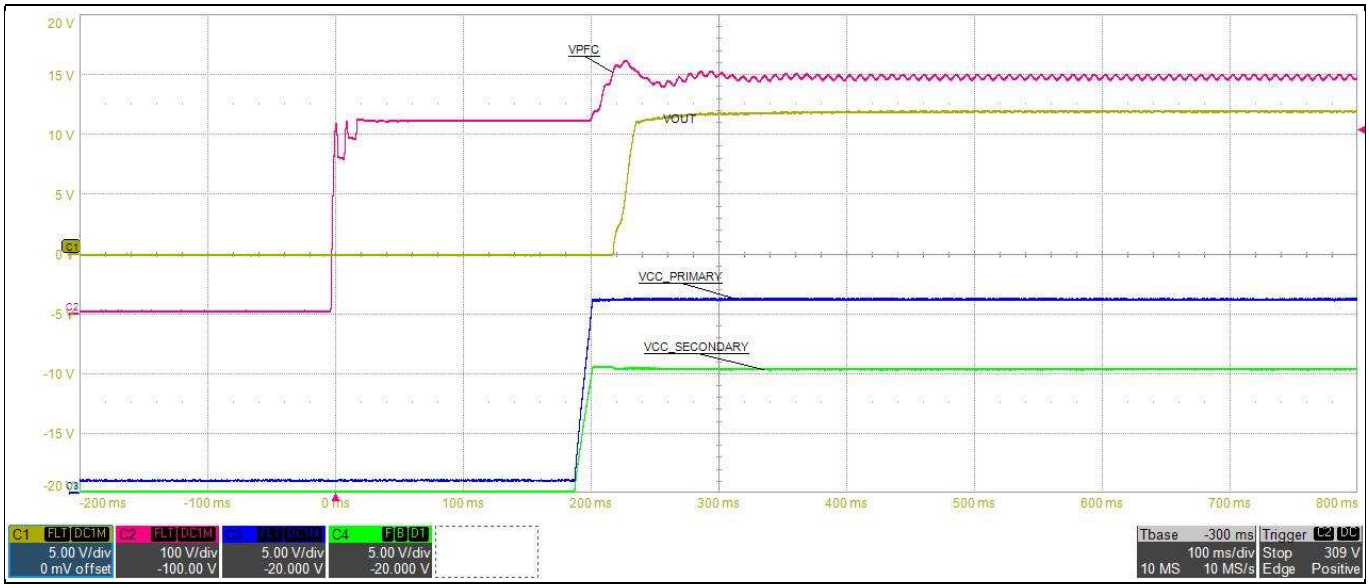


Figure 64 **Start-up at 230 V AC_{RMS} 100 percent load: PFC voltage (red), output voltage (yellow), primary V_{CC} (blue), secondary V_{CC} (green)**

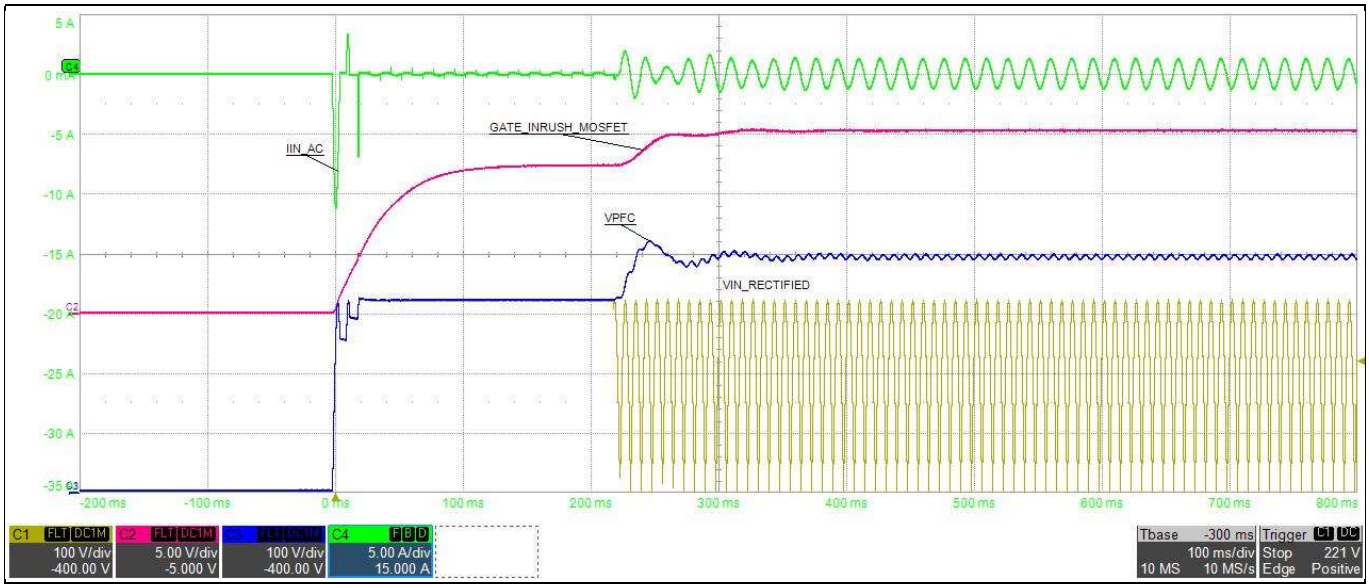


Figure 65 **Start-up at 230 V AC_{RMS} 100 percent load: input AC current (green), gate of inrush MOSFET (red), rectified input AC voltage (yellow)**

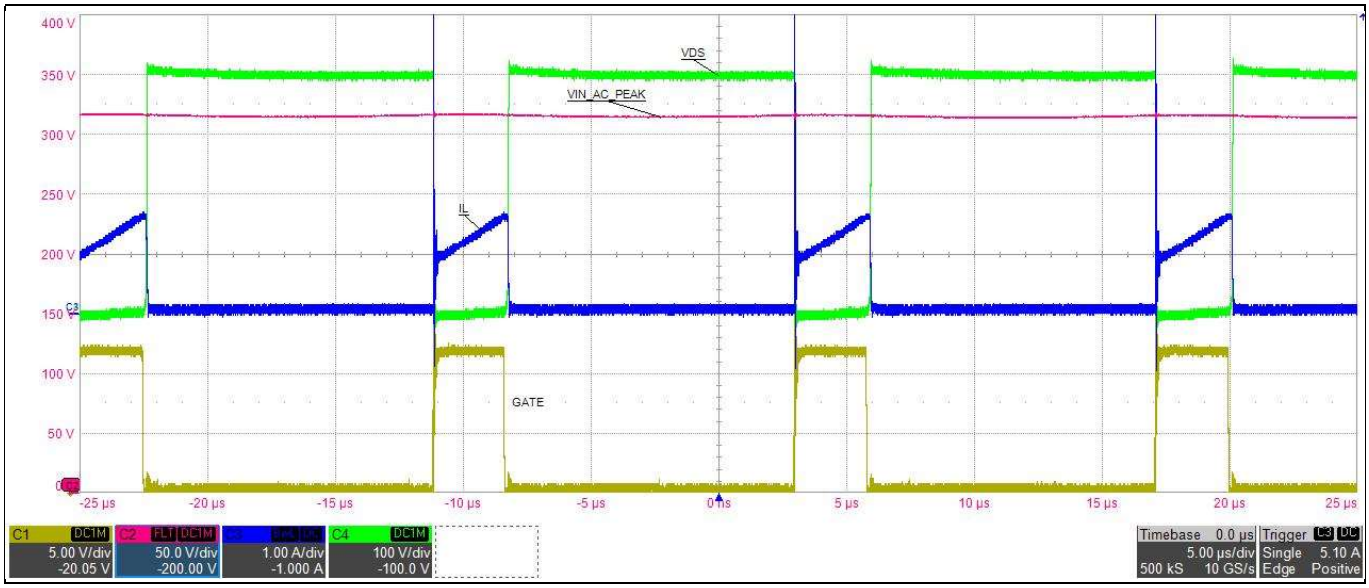


Figure 66 **Steady-state waveform at 230 V AC_{RMS} peak 100 percent load: input AC peak voltage (red), PFC MOSFET V_{DS} (green), PFC inductor current (blue), PFC MOSFET gate (yellow)**

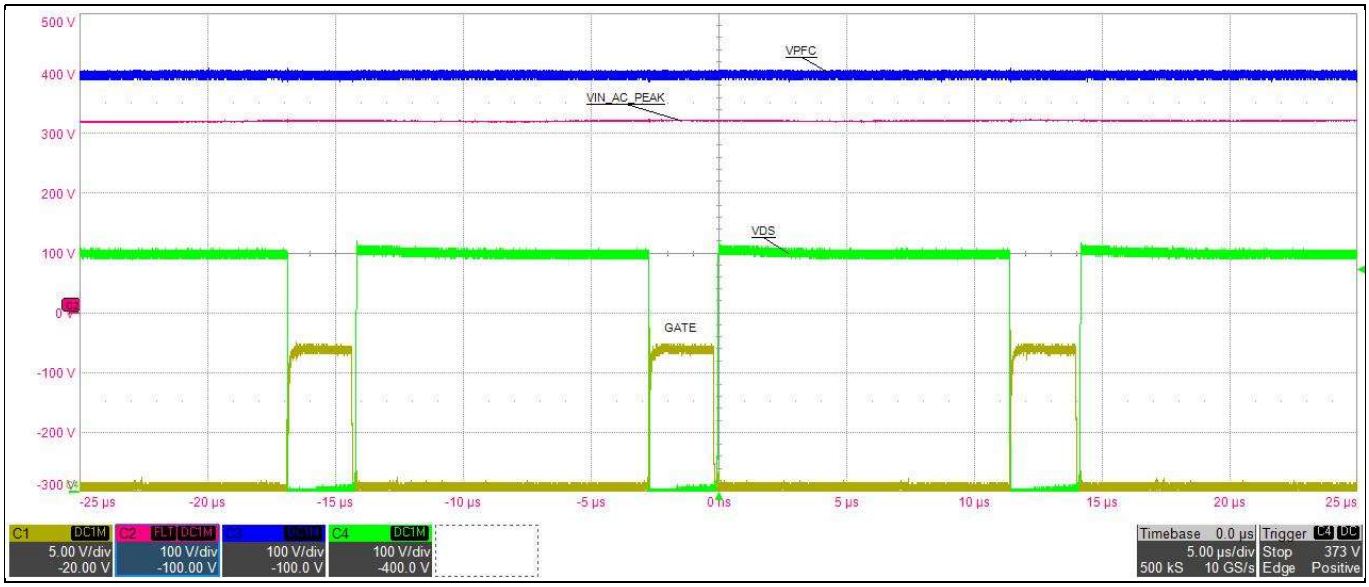


Figure 67 **Steady-state waveform at 230 V AC_{RMS} peak 100 percent load: PFC output voltage (blue), input V AC peak (red), PFC MOSFET drain (green), PFC MOSFET gate (yellow)**

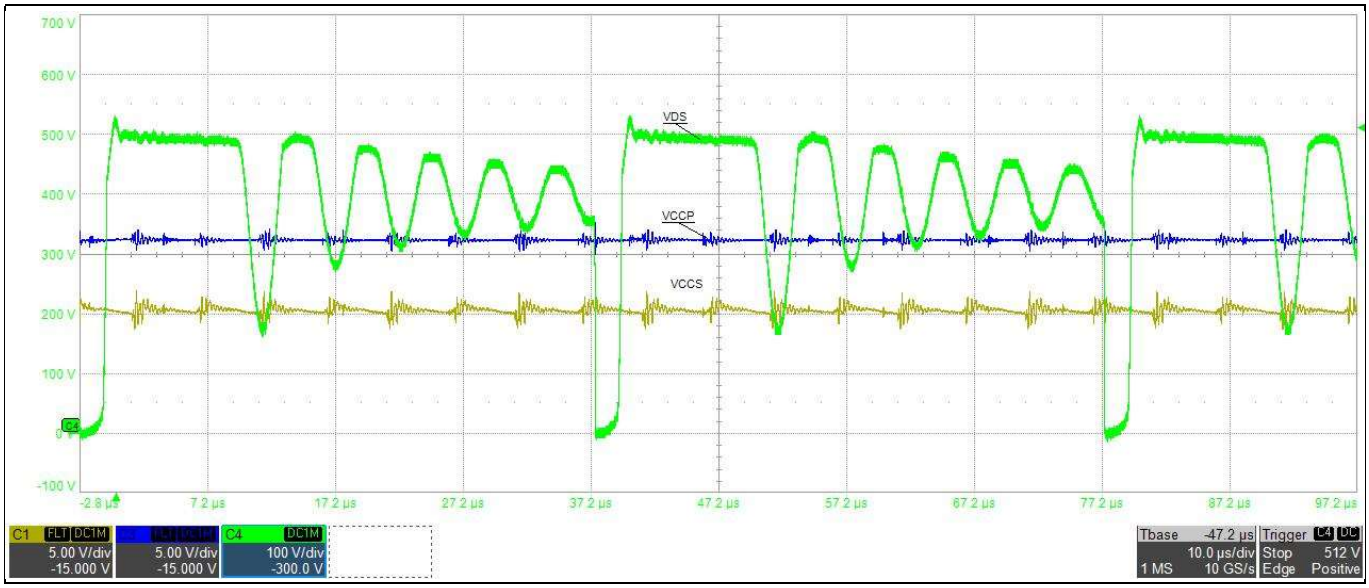


Figure 68 **Steady-state waveform of flyback: drain voltage (green), primary V_{CC} voltage (blue), secondary V_{CC} voltage (yellow)**

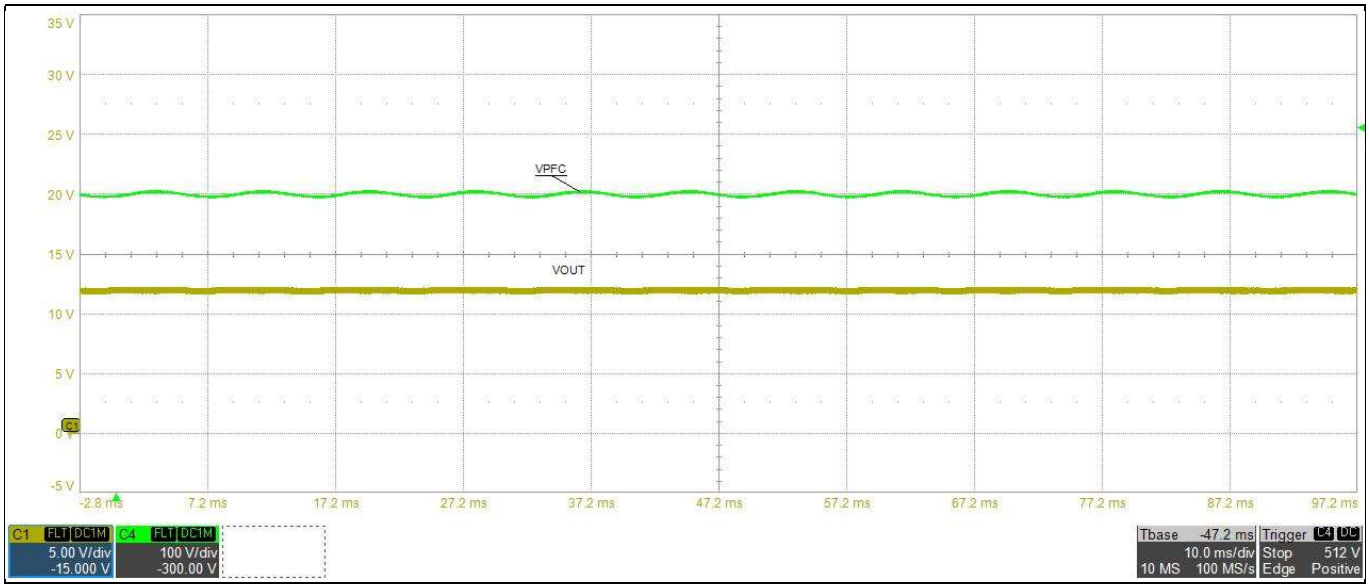


Figure 69 **Steady-state waveform: output voltage V_{OUT} (yellow), PFC voltage (green)**

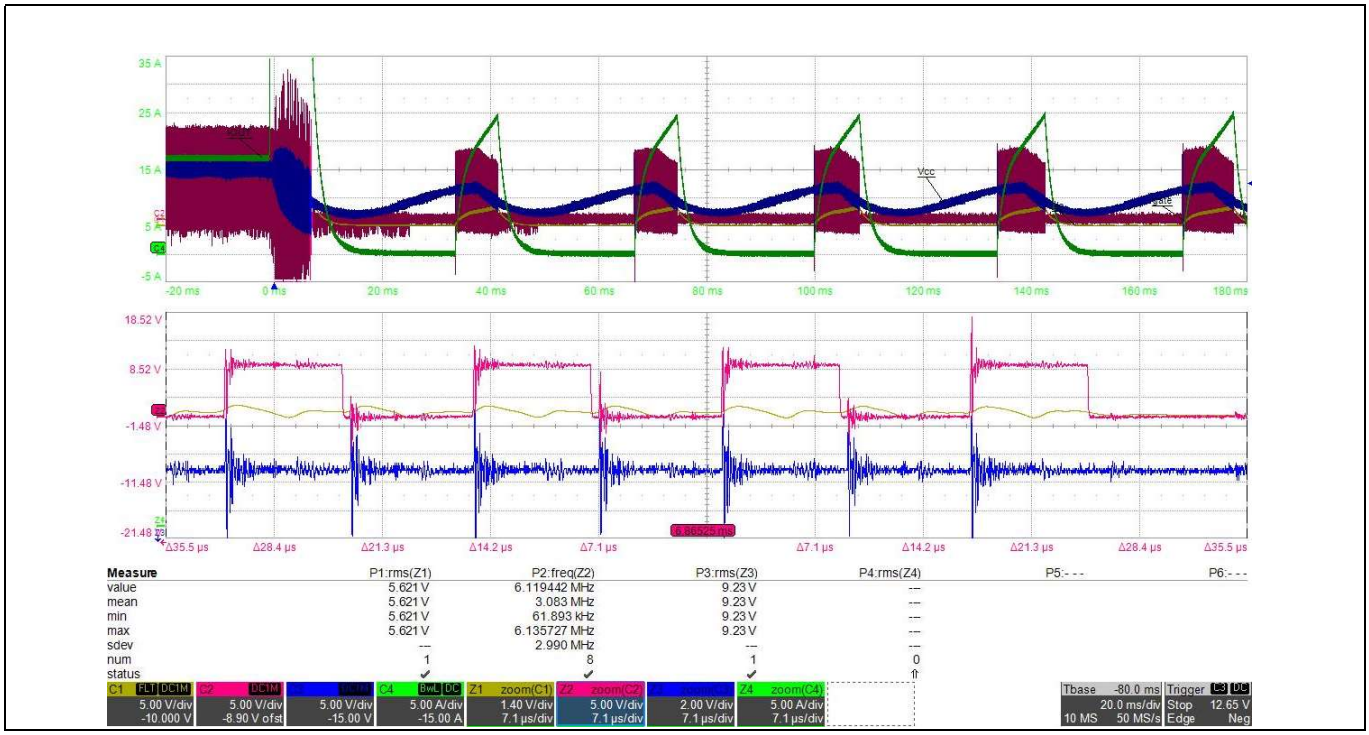


Figure 70 **Short-circuit waveform: output voltage V_{OUT} (yellow), output current I_{OUT} (green), half-bridge low-side MOSFET gate (red), V_{CC} supply to IC5 (blue)**

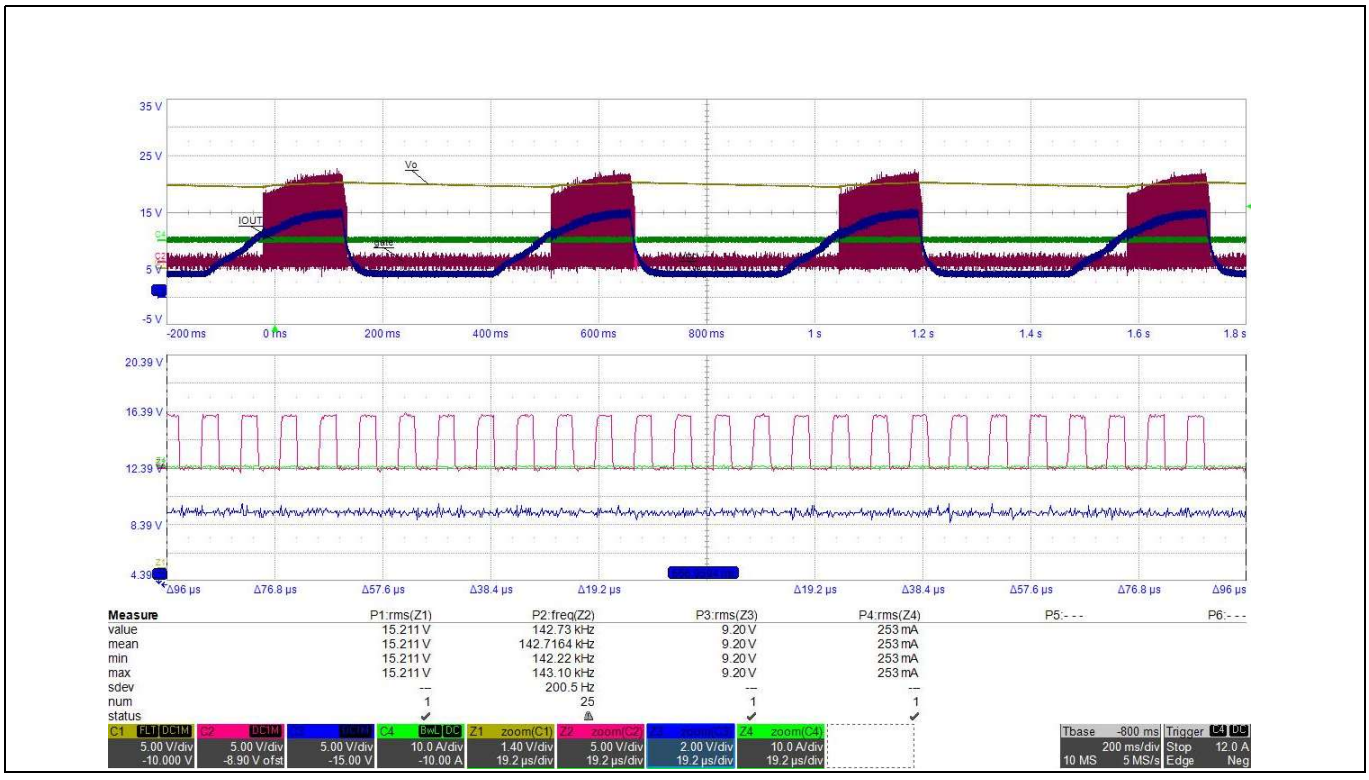


Figure 71 **No-load waveform: output voltage V_{OUT} (yellow), current I_{OUT} (green), half-bridge low-side MOSFET gate (red), V_{CC} supply to IC5 (blue)**

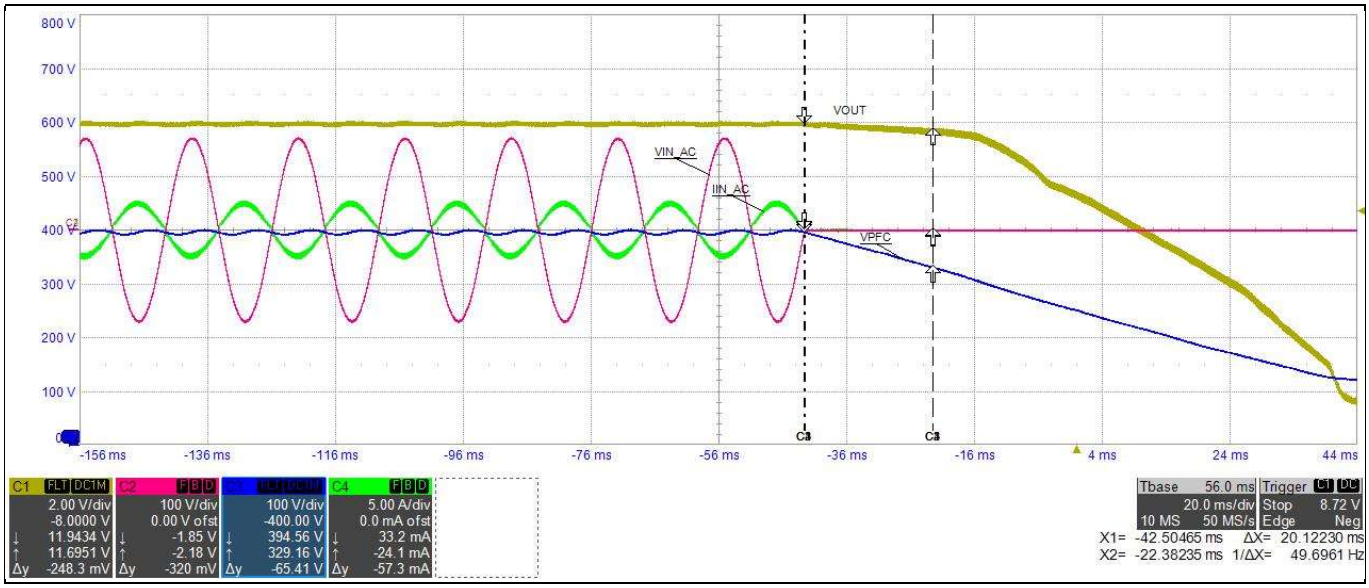


Figure 72 **Hold-up time at 120 V AC_{RMS} 100 percent load: output voltage (yellow), input AC voltage (red), input AC current (green), PFC voltage (blue)**

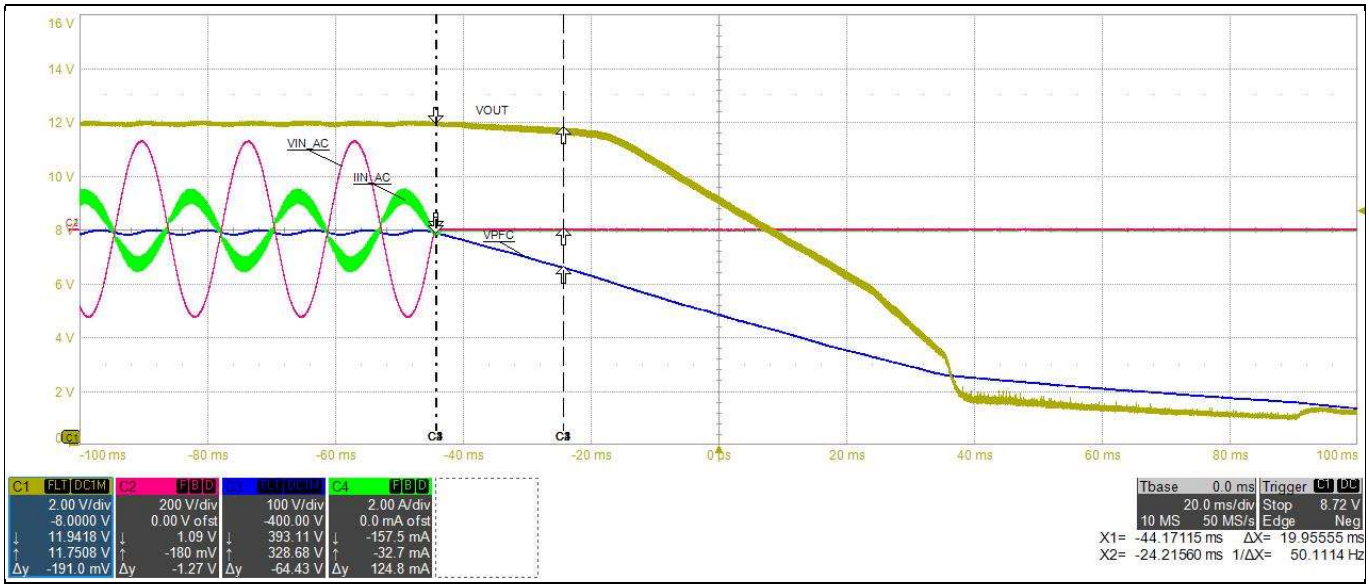


Figure 73 **Hold-up time at 230 V AC_{RMS} 100 percent load: output voltage (yellow), input AC voltage (red), input AC current (green), PFC voltage (blue)**

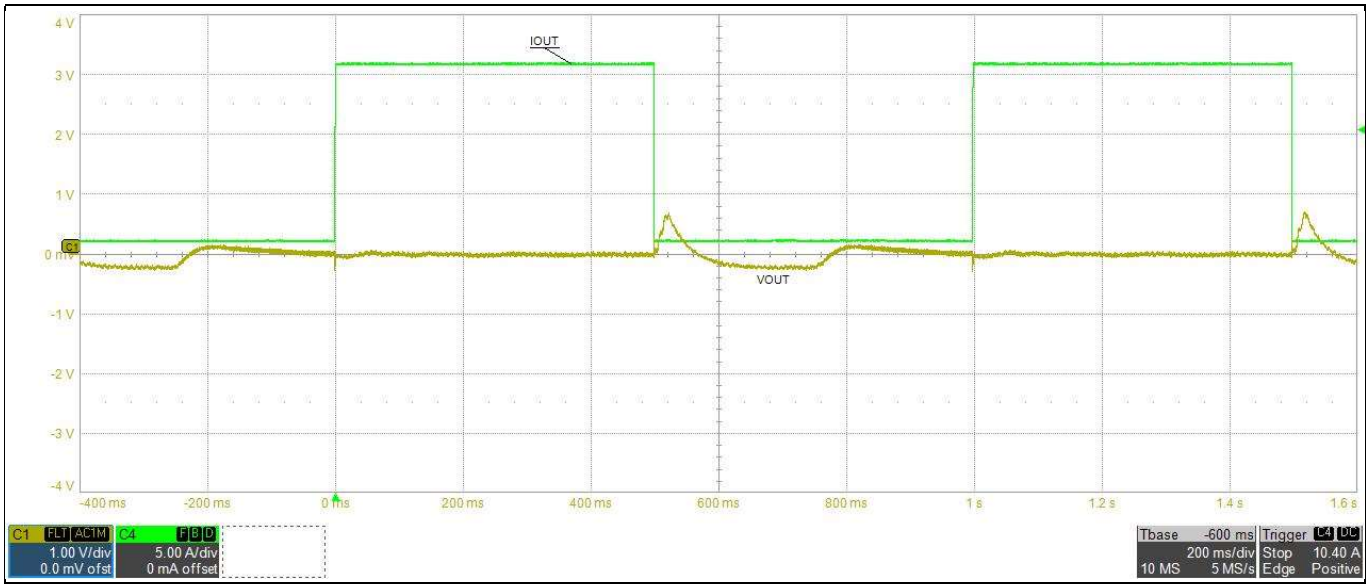


Figure 74 **Transient performance at 0.5 Hz (1 A to 16 A load variation): output current (green), output voltage (yellow)**

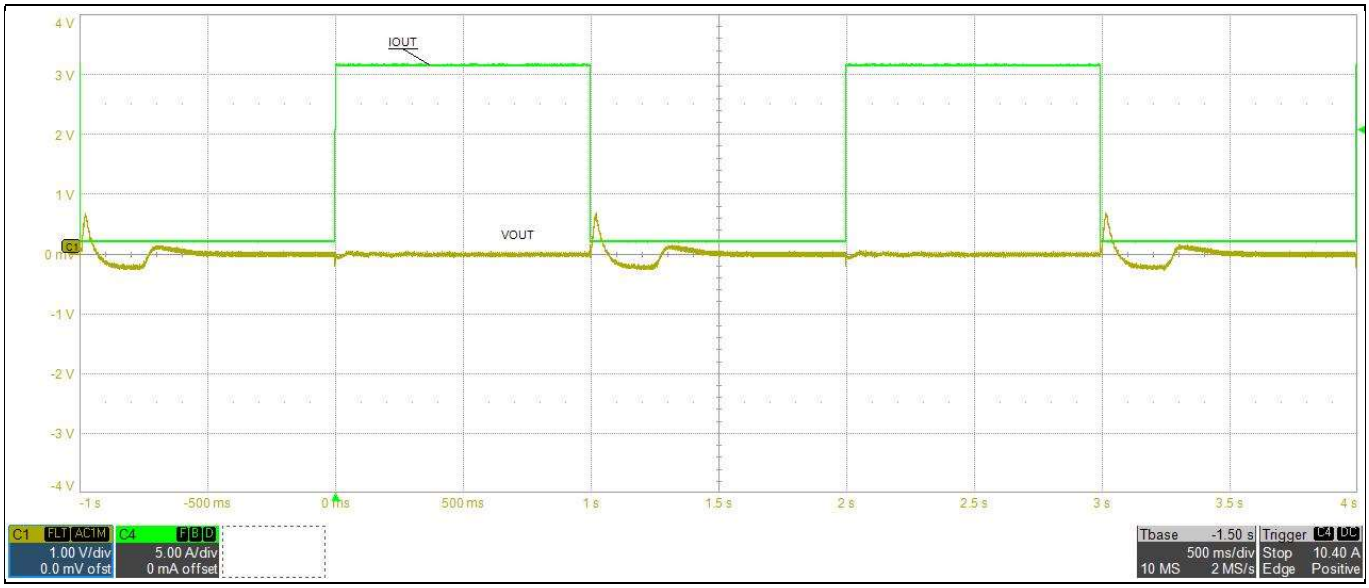


Figure 75 **Transient performance at 1 Hz (1 A to 16 A load variation): output current (green), output voltage (yellow)**

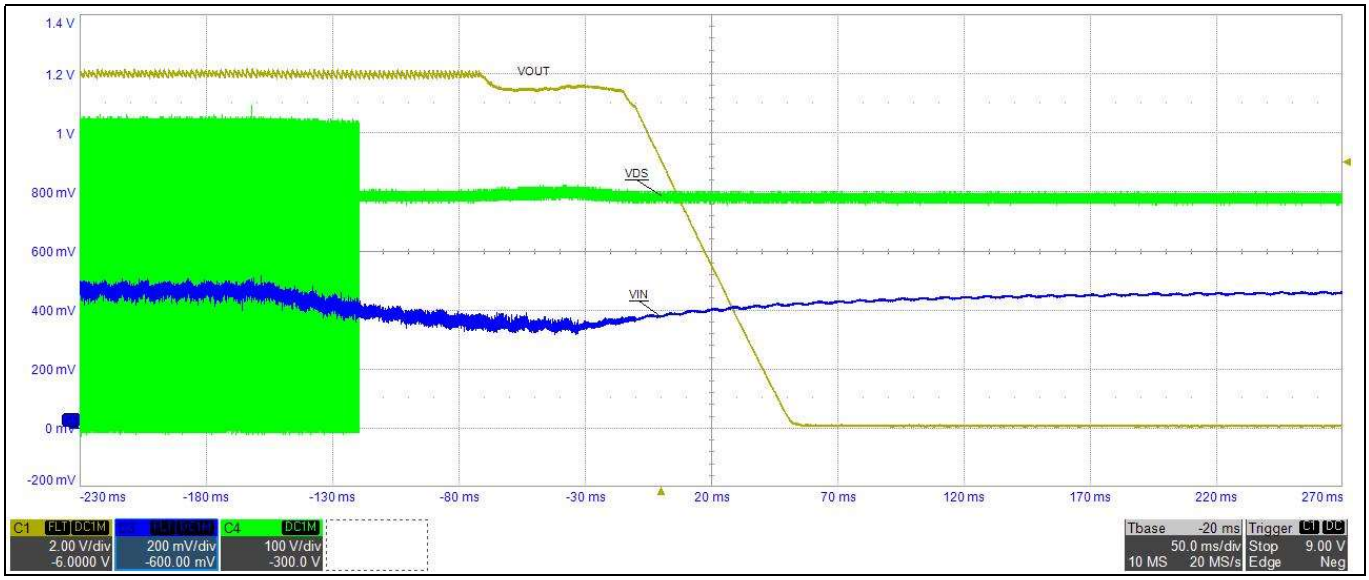


Figure 76 **Brown-out condition at 60 V AC_{RMS}: output voltage V_{OUT} (yellow), flyback drain V_{DS} (green), ICE5QR0680AG V_{IN} pin (blue)**

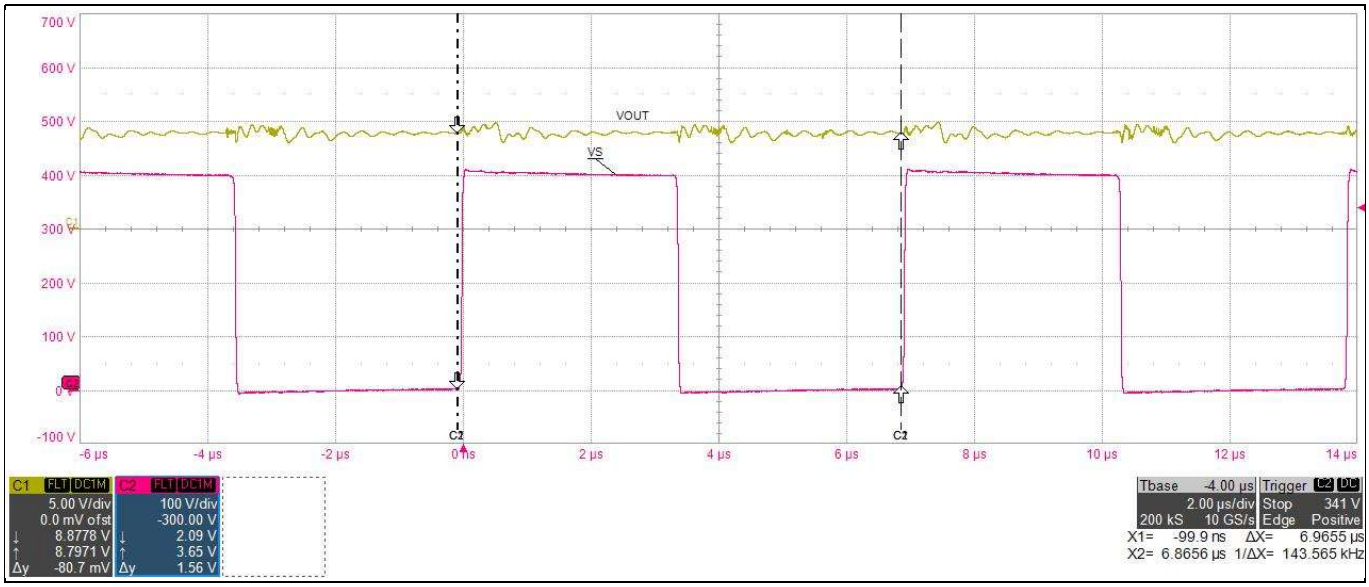


Figure 77 **Current limit at 120 V AC_{RMS}, 19 A (V_{OUT}: 8.5 V, frequency: 143.5 kHz): output voltage V_{OUT} (yellow), half-bridge V_s (red)**

15.2 Closed-loop frequency response

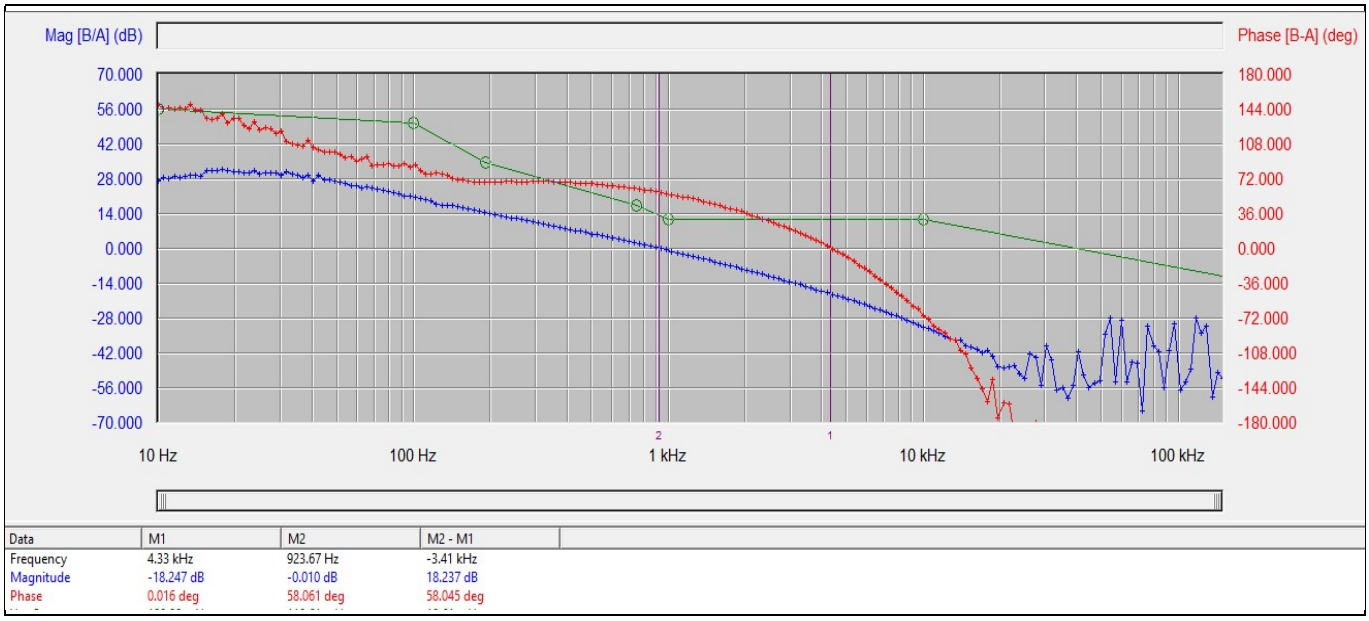


Figure 78 Gain margin and phase margin at 120 V AC_{RMS}: PM = 58 degrees, GM = 18 dB, crossover frequency = 923 Hz

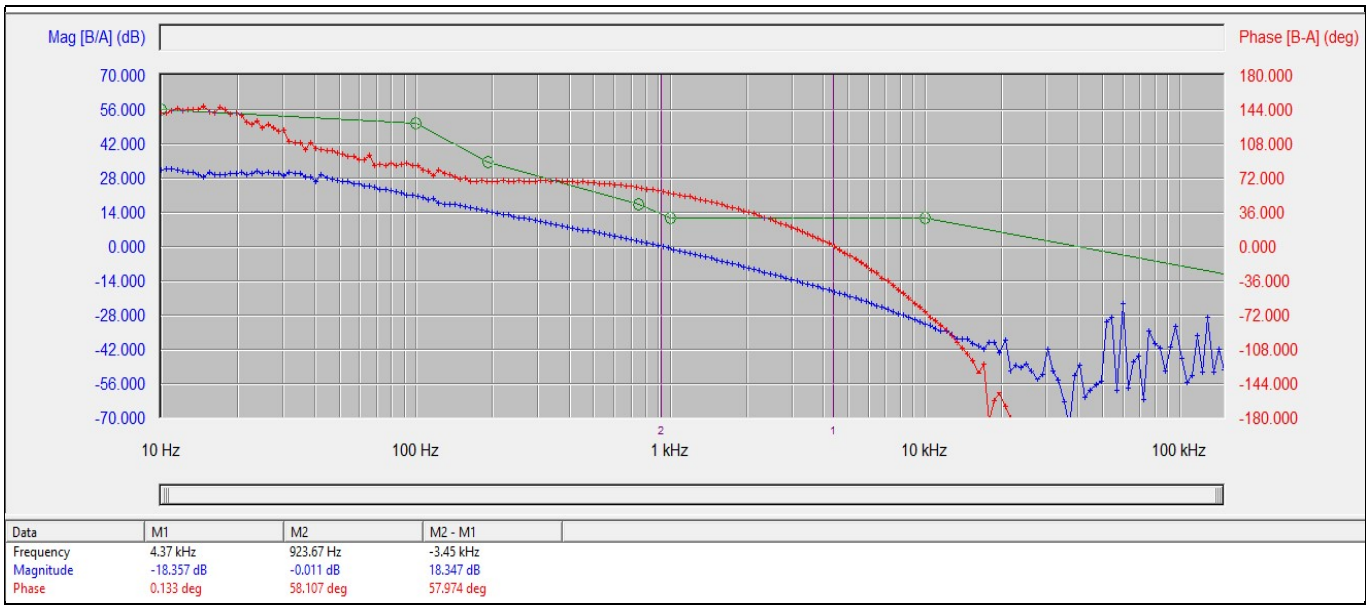


Figure 79 Gain margin and phase margin at 230 V AC_{RMS}: PM = 58 degrees, GM = 18 dB, crossover frequency = 924 Hz

15.3 Thermal performance under normal operating conditions

Thermal images captured under conditions of 120 V AC input, 12 V/16 A load (after 1 hour of operation):

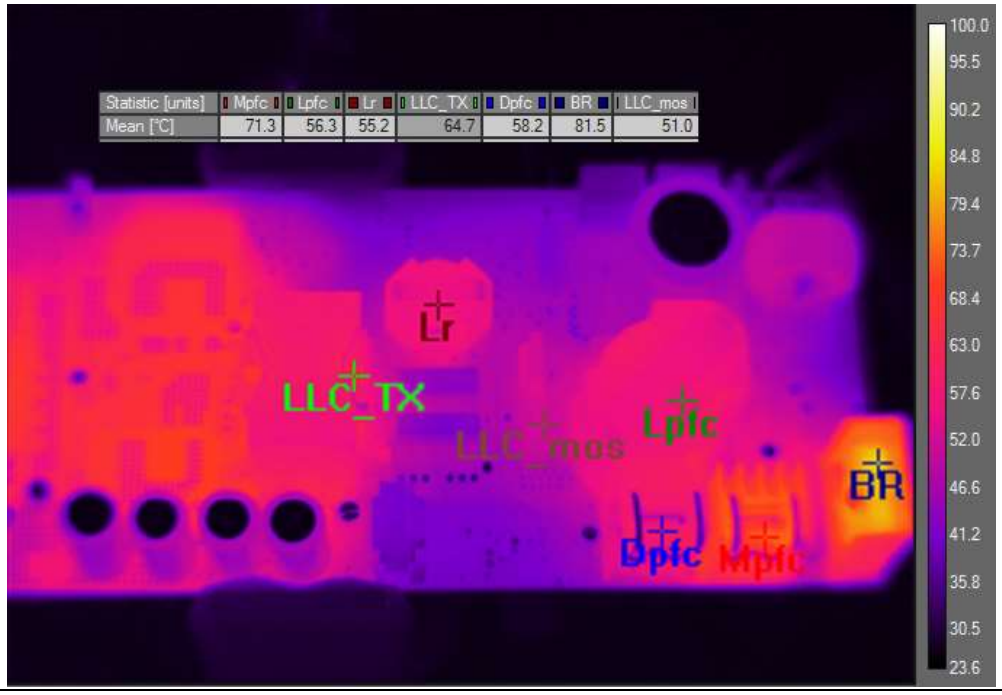


Figure 80 Top-side thermal image

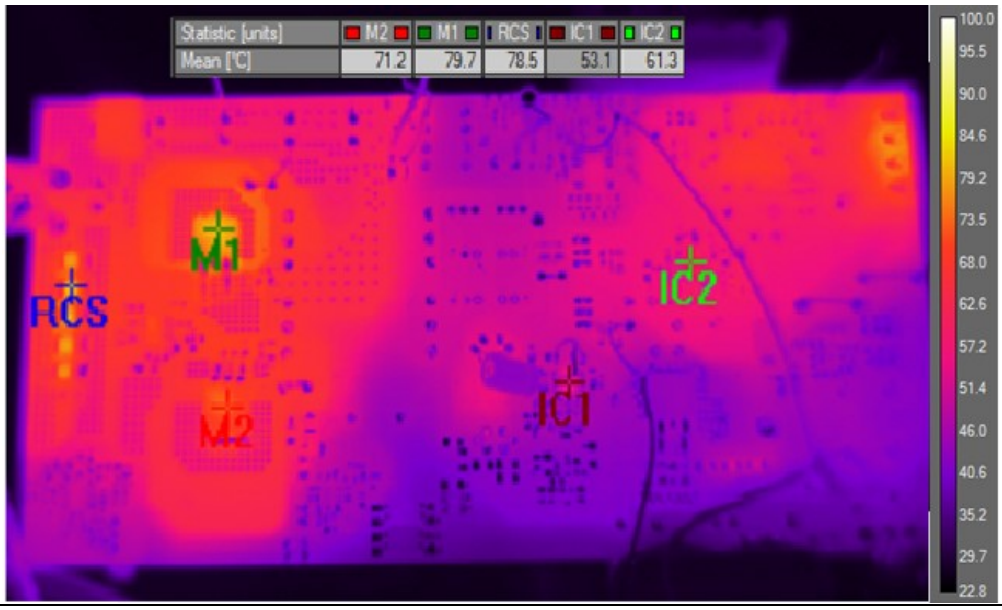


Figure 81 Bottom-side thermal image

Thermal images captured under conditions of 230 V AC_{RMS} input, 12 V/16 A load (after 1 hour of operation):

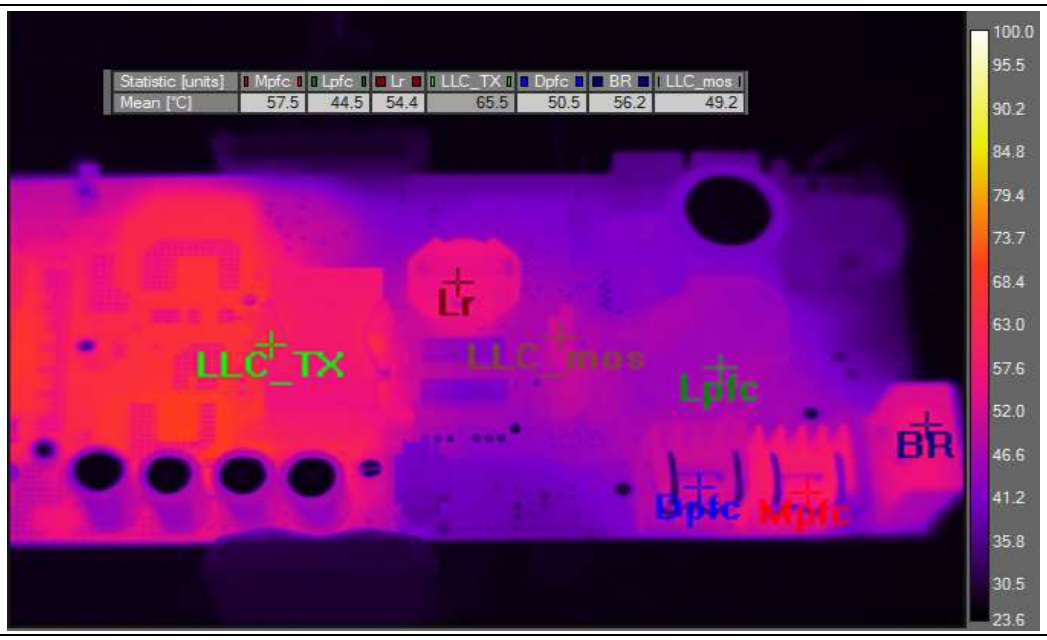


Figure 82 Top-side thermal image

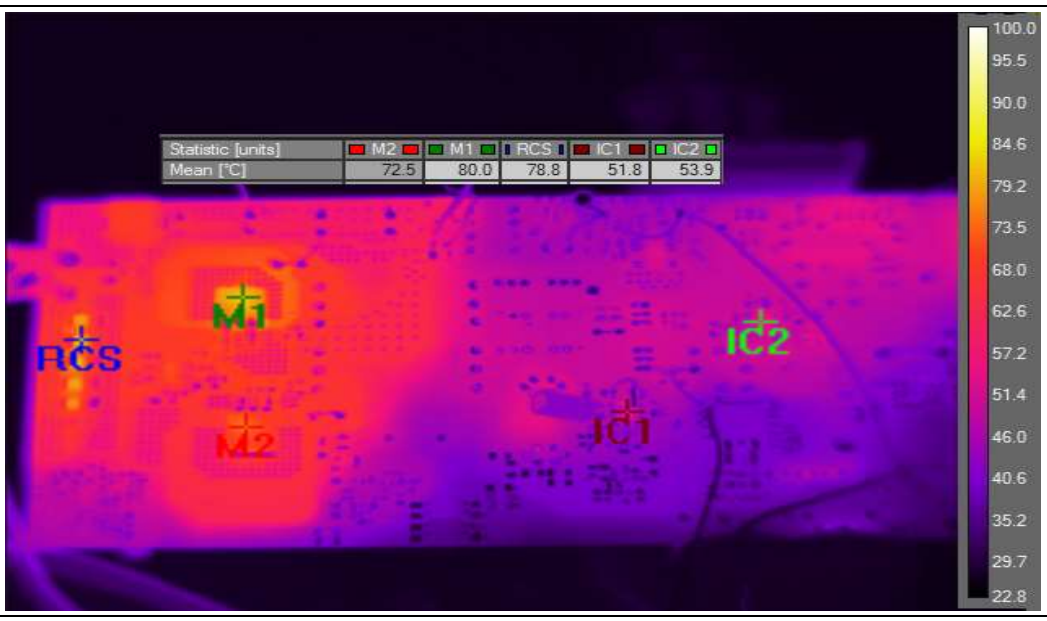


Figure 83 Bottom-side thermal image

15.4 Conducted EMI

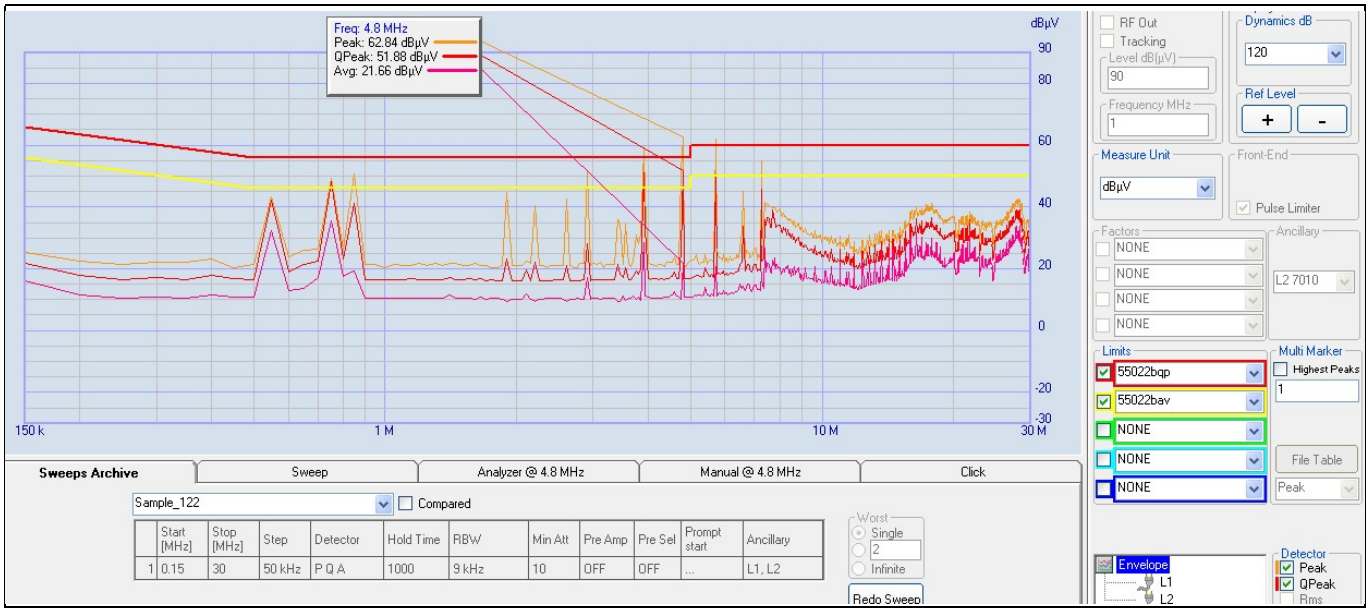


Figure 84 Conducted emissions at 120 V AC_{RMS} with 100 percent load

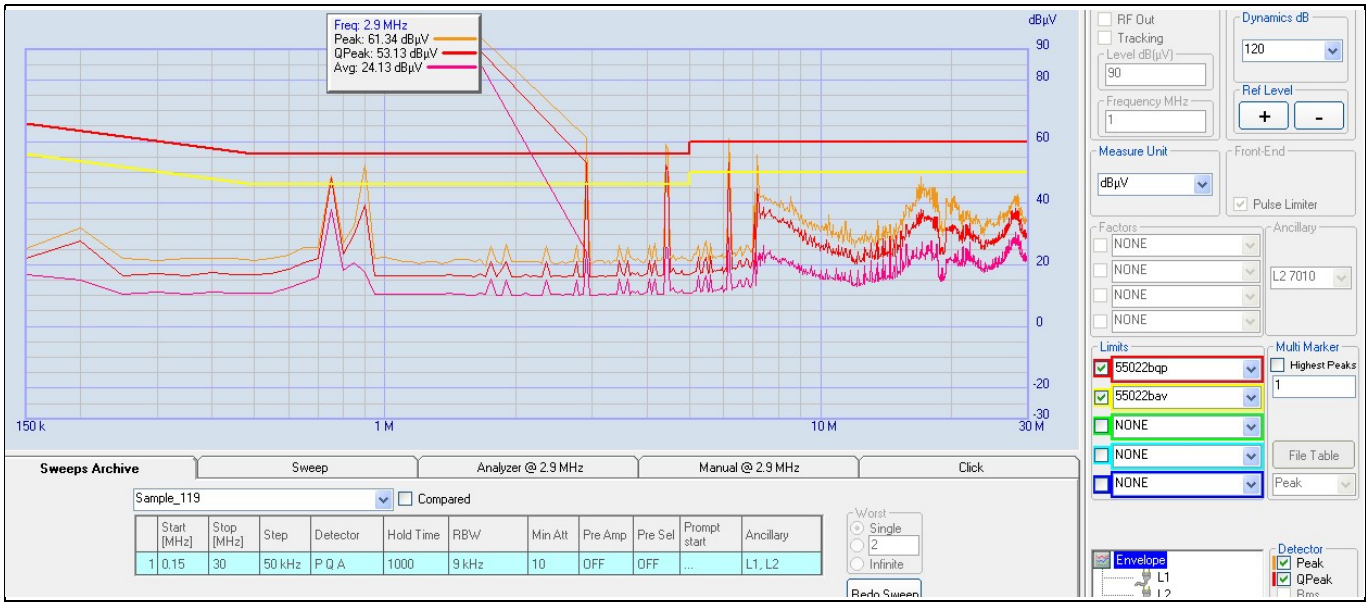


Figure 85 Conducted emissions at 230 V AC_{RMS} with 100 percent load

The limit lines in the above figures represent EN 55022 class B limits for the quasi-peak in red and average in yellow. Frequency sweep measurements are shown in red for quasi-peak and pink for average. The results provided here are from pre-compliance tests only. These were not carried out at a certified test lab. For compliance with the standard the traces must remain below their respective limit lines for both quasi-peak and average measurements, as shown in the table below.

Tests were carried out using a 16 A load. EMI emissions are very dependent on the board layout; please refer to section 13.1.

Table 5 EN 55022 class B limits for conducted EMI

CISPR22 class B conducted EMI limits		
Frequency emission (MHz)	**Quasi-peak**	**Average**
0.15 to 0.50	66 to 56*	56 to 46*
0.50 to 5.00	56	46
5.00 to 30.0	60	50
FCC part 15 class B conducted EMI limits		
Frequency emission (MHz)	**Quasi-peak**	**Average**
0.15 to 0.50	66 to 56*	56 to 46*
0.50 to 5.00	56	46
5.00 to 30.0	60	50
*Decreases with logarithm of the frequency		

Note
Infineon Technologies does not guarantee compliance with any EMI standard.

16 Conclusion

The DEMO_200W_12VDC_LLC evaluation board demonstrates a robust, cost-competitive two-stage PFC plus LLC half-bridge power supply design successfully implemented with the PFC stage controlled by the IR1155S and the LLC half-bridge resonant converter controlled by the IRS27952.

It has been shown that the IR1155 operating in CCM provides a very high power factor with low-line current THD over the input range. The LLC resonant half-bridge converter secondary-side feedback circuit demonstrates a very tight voltage regulation over a wide load range. Accuracy of regulation over the output current range remains within +/-1 percent of the nominal output over the input line voltage range. The high current shut down protection function of the IRS27952 VS pin has not been implemented in this design to protect againt output short circuit. This was replaced by a hiccup mode protection scheme, which operates by pulling the VCC supply voltage below the UVLO threshold. The original design of this demo board has been modified to implement this protection. This was found to be more reliable than using the CT pin shut down function.

Transient response and stability of the converter have been verified using step response and measurement of the gain/phase margin using the frequency response analyzer AP300. The converter is very stable, with a bandwidth of 924 Hz and gain margin of 18 dB, with a near-ideal phase margin of 58 degrees. The excellent performance of the SR IC IR11688 has also been demonstrated. The QR flyback bias power supply based around the ICE5QR0680AG provides faster start-up response over the input voltage range with additional brown-out protection for the whole system.

The start-up time of the power supply over the input voltage range is less than 300 ms measured at 115 V AC_{RMS} and 230 V AC_{RMS} line inputs. The component temperatures on the board remain less than 85°C under all line and load conditions.

Test results show that the design specifications have been met.

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Revision history

Document version	Date of release	Description of changes
1.0	7/22/2019	First release
2.0	12/5/2019	Modifications to over-load protection, updates schematics and waveforms
2.2	2/12/2020	Updates to bill of materials

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