Isolated gate driver IC with a configurable isolated bias supply for GaN HEMTs

KIT_1EDB_AUX_GaN

About this document

Scope and purpose

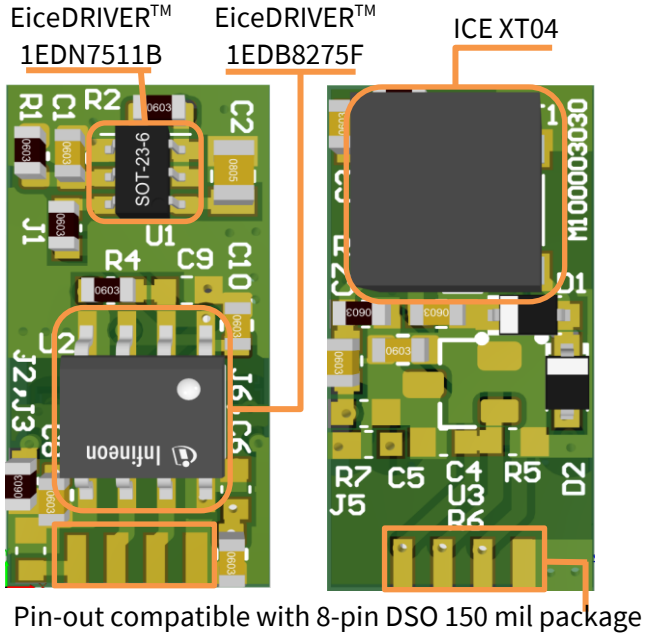
KIT_1EDB_AUX_GaN is a complete driving solution for gallium nitride (GaN) HEMTs that includes an isolated single-channel gate driver IC (**EiceDRIVER™ 1EDB8275F**) and a configurable isolated bias supply enabled by a simple single-channel non-isolated gate driver IC (**EiceDRIVER™ 1EDN7511B**).

The board is pin-out compatible with the EiceDRIVER™ 1EDB8275F itself and with equivalent drivers in the industry-standard 150 mil DSO-8 package. Therefore, it is an easy plug-in solution in designs that already include those isolated gate driver ICs and allows testing the EiceDRIVER™ 1EDB8275F in combination with an isolated bias supply; one potential replacement scenario is for example when bootstrap is originally used in the design but cannot be used due to the modulation scheme or topology change. The board can be easily configured by jumpers for unipolar or bipolar driving; bipolar driving can be beneficial to prevent the “first pulse” issue at start-up or in burst mode.

The board allows driving of GaN HEMTs with several unipolar or bipolar gate-to-source voltages that can be configured by means of resistor R1. High common-mode transient immunity (CMTI) is also ensured thanks to the very low input-to-output capacitance (3 pF) of the XT04 transformer and the high robustness of EiceDRIVER™ 1EDB8275F (more than 300 V/ns).

Intended audience

This document targets power electronic engineers and designers who are interested in a configurable isolated bias supply for their GaN design featuring compactness, high efficiency, good regulation and attractive cost.



V_{pos} [1]	V_{neg} [1, 2]	V_{CCI}	R1
+7 V	-4 V	12 V	5.1 kΩ
+9 V	-5 V	15 V	3.9 kΩ
+8 V	-6 V	15 V	4.3 kΩ
+5 V [3]	-4 V [3]	10 V	7.5 kΩ

[1] Positive and negative voltages are unregulated, see Section 3.1 for more details
[2] If unipolar supply is selected, only V_{pos} is applied
[3] Positive rail regulation, important for Schottky gate GaN HEMTs, is possible by enabling the on-board TL432 (U3)

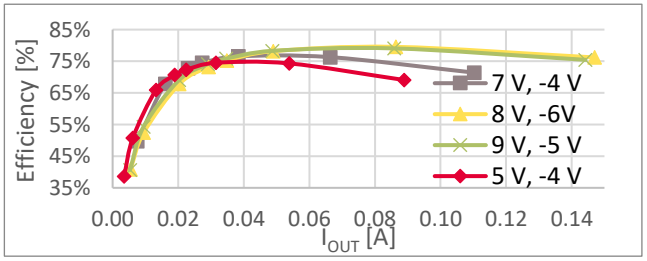


Figure 1 Overview of KIT_1EDB_AUX_GaN

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1 Requirements for driving GaN HEMTs

One challenge of GaN switch technologies is the low (around 1 V) gate voltage threshold $V_{(GS)th}$ that makes the device prone to induced return-on. It is well-known that in a half-bridge configuration, during hard-switching turn-on of either the low-side or high-side GaN power switch, the high dV/dt of the switching node induces a Miller current; this current flows through the C_{GS} and C_{GD} gate capacitances of the complementary device and pulls up its gate-to-source voltage. This induced voltage at the gate must be kept below the $V_{(GS)th}$ gate threshold voltage to avoid extra losses or severe return-on. An example is provided in **Figure 2**; it refers to a hard-switching turn-on transition at 14 A of Infineon's **CoolGaN™ IGLD60R070D1** in the EVAL_2EDB_HB_GaN (see **[1]**) platform during reverse double pulse test.

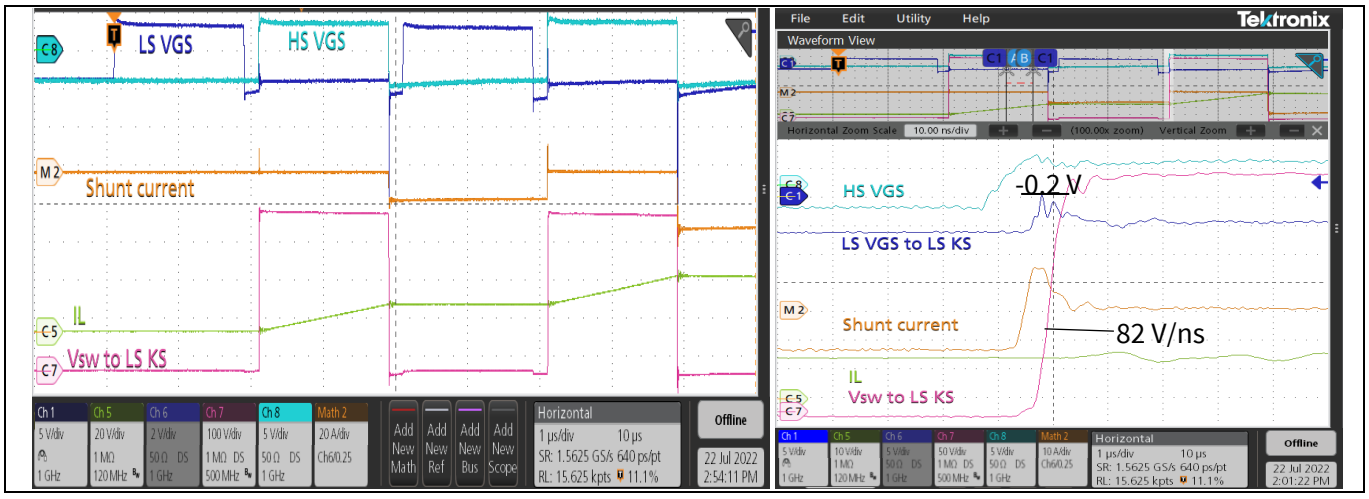

Figure 2 Induced gate-to-source voltage during hard-switching of the complementary switch

In this condition the low-side gate-to-source voltage (blue) is pulled up by around 6 V. Therefore, to introduce some margin from the gate voltage threshold and prevent return-on, it is mandatory to consider a negative gate-to-source voltage during OFF-state. For Infineon's CoolGaN™ GIT HEMTs, this can be achieved by using a coupling capacitance (C_c) on the gate able to store charge during the ON-state and consequently pull down the V_{GS} during the OFF-state; this mechanism benefits of the integrated gate clamping structure of Infineon CoolGaN™ GIT HEMT. For more basic information on CoolGaN™ driving, please refer to **[2]**.

However, this mechanism does not cover "first pulse" scenarios, when there has been no activity for prolonged time (e.g., start-up, recovery, burst-mode) and therefore the coupling capacitor is discharged. In this situation, at the point in time when one GaN HEMT starts switching, the other will show a 0 V $V_{GS,off}$; **Figure 3** shows an example.

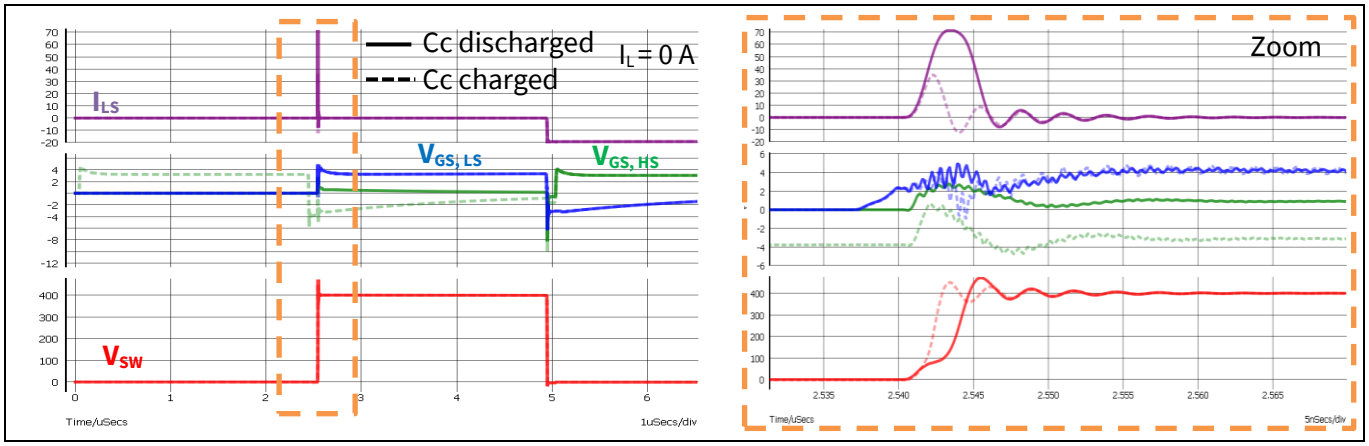

Figure 3 First pulse issue – visualization with unipolar V_{GS} = 9 V, C_c = 3.3 nF charged or discharged

Requirements for driving GaN HEMTs

The dotted line clearly represents a “first pulse” issue caused by the discharged gate coupling capacitance; the return-on is visible in the green gate-to-source voltage level (above the threshold), in the distorted switching node shape and in the increased charge. To prevent the “first pulse” issue, a bipolar bias supply driving approach can be considered; in this case, when the coupling capacitor is discharged, the gate-to-source voltage in the OFF-state would still be given by the negative bias voltage. However, it must be pointed out that this fixed negative voltage increases the reverse conduction losses during the dead time, therefore its applicability and the evaluation of pros and cons is left to the user.

KIT_1EDB_AUX_GaN enables both unipolar and bipolar driving and by default is configured for bipolar driving with V_{pos} = 7 V, V_{neg} = -4 V. The V_{GS} measurements shown in this application note relate to driving the of Infineon’s CoolGaN™ IGLD60R070D1 with 2.2 nF gate coupling capacitor (C_c) and 470 Ω static resistance (R_{ss}).

2 Board description

2.1 Schematic and general description

The schematic of KIT_1EDB_AUX_GaN is shown in **Figure 4**.

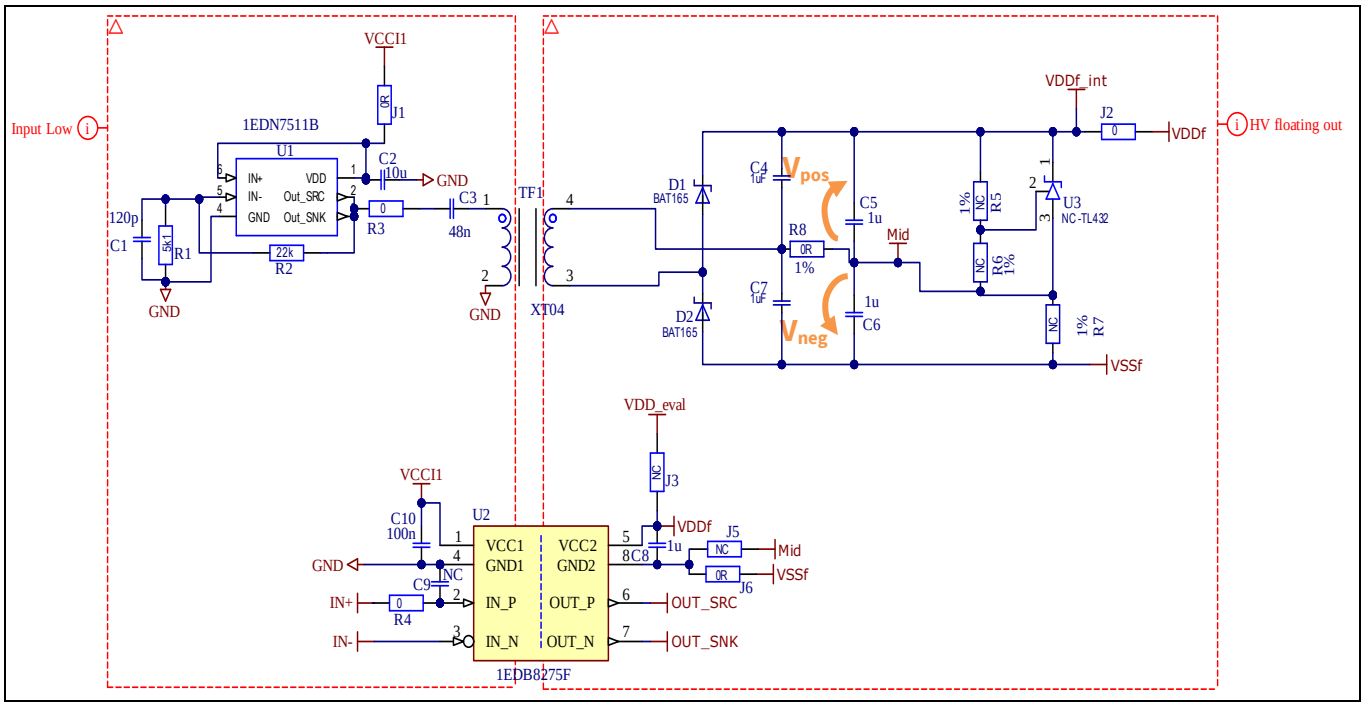

Figure 4 KIT_1EDB_AUX_GaN schematic

The board includes the EiceDRIVER™ 1EDB8275F, a single-channel isolated gate driver IC featuring 3 kV_{RMS} input-to-output isolation thanks to Infineon's coreless transformer (CT) technology. This driver is optimized to drive high-side GaN devices and can be used in combination with **EiceDRIVER™ 1EDN8550B** for low-side driving as described in Section 6.4 of **[3]** and **[4]**.

The circuit on the top side of the schematic is the bias supply that operates as an isolated DC-DC converter and provides the floating supply to the secondary side of EiceDRIVER™ 1EDB8275F; bipolar driving is enabled by opening the jumper J5 and closing J6 (gate driver GND2 connected to VSSf); vice versa for unipolar driving (gate driver GND2 connected to Mid).

The board operates with a single supply voltage (V_{CCI1}), which supplies both the EiceDRIVER™ 1EDB8275F primary side and the isolated DC-DC converter.

The operating voltages of the bias supply are shown in **Figure 5** for ease of understanding.

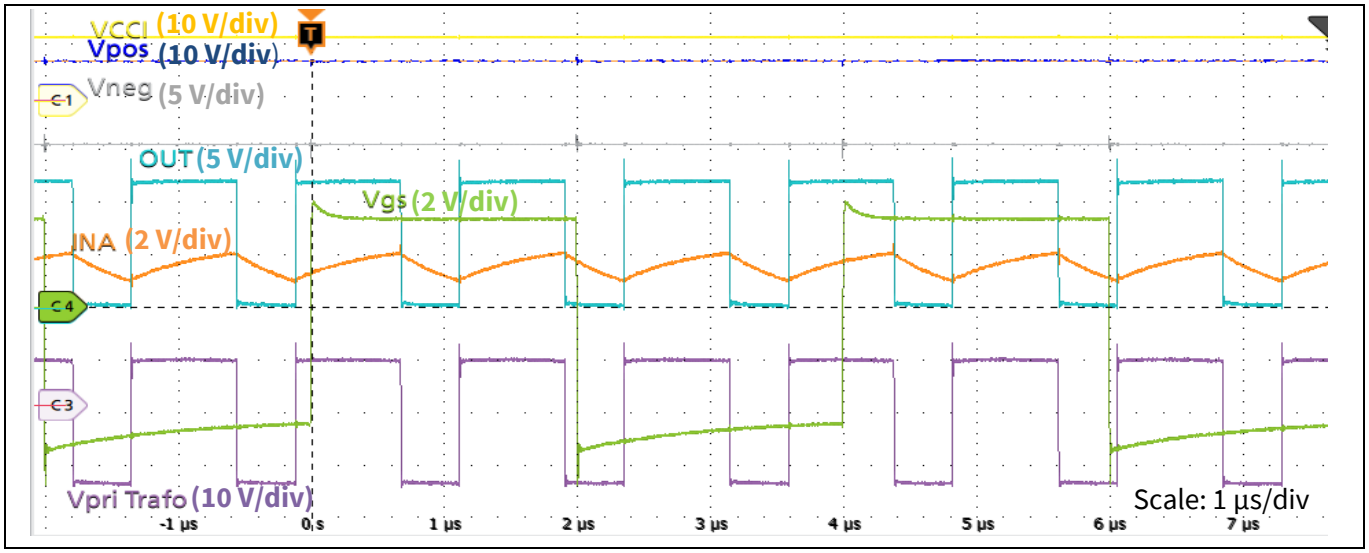

Figure 5 Operating waveform of the bias supply for the default configuration with V_{CCI} = 12 V and V_{pos} = 7 V, V_{neg} = -4 V driving Infineon CoolGaN™ at 250 kHz

The V_{CCI} voltage (12 V by default) is shaped by the EiceDRIVER™ 1EDN7511B in a two-level waveform (see blue, OUT) with levels V_{CCI}, 0 V; the frequency and duty-cycle are set via feedback components C1, R1, R2 to 812 kHz and 64 percent duty-cycle (see Appendix **5** for dimensioning details). With a 1:1 ratio, the XT04 transformer is only responsible for galvanic isolation and therefore the signal on the transformer's secondary side still shows an amplitude equal to almost V_{CCI}. This voltage is rectified by D1 and D2 Schottky diodes and with 64 percent duty-cycle the capacitors C5 and C6 charge respectively to 64 percent and 38 percent of the total secondary voltage (V_{CCI} minus 1 V typical drop). The voltages on C5 and C6 represent the positive and negative bipolar bias supplies, respectively.

2.2 Bias supply ring oscillator concept

The bias supply circuit is based on the **EiceDRIVER™ 1EDN7511B**, a single-channel non-isolated gate driver IC. The output is used as feedback to the inverting input (IN-) to create a "ring oscillator".

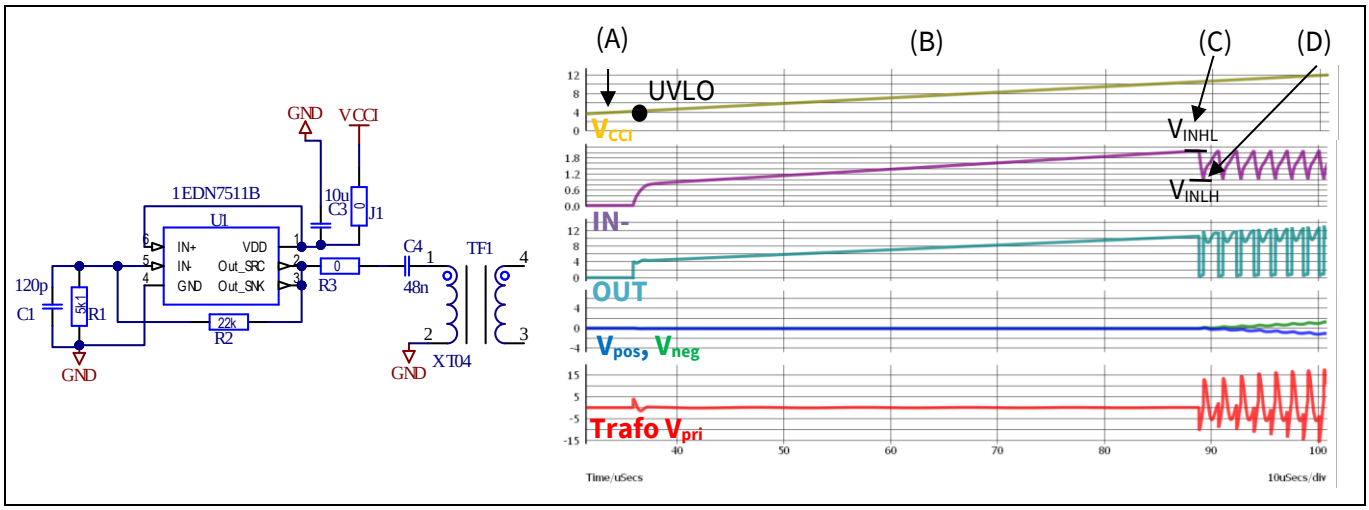

Figure 6 Ring oscillator concept and start-up

The ring oscillator behavior of the circuit is explained by referring to the start-up behavior shown in **Figure 6**:

(A) When the supply V_{CCI} is below the 4 V undervoltage lockout (UVLO) level of the EiceDRIVER™ 1EDN7511B, the output is actively held low by the driver.

(B) When the supply reaches the UVLO, the driver wakes up; being the non-inverting input, IN+ connected to the supply and the inverting input IN- connected to ground (since C1 is discharged), the output goes high. At the same time, high OUT starts to charge C1 via the resistive feedback path; IN- increases.

(C) When IN- reaches the driver input high threshold (V_{INH} = 2.1 V), the EiceDRIVER™ 1EDN7511B drives the output low after one propagation delay period (19 ns typ.). At the same time, IN- starts to discharge on the parallel R1//R2.

(D) When IN- reaches the driver low input threshold (V_{INHL} = 1.2 V), the EiceDRIVER™ 1EDN7511B drives the output high and the oscillation is then established.

2.3 Dimensioning of the bipolar split V_{pos}/V_{neg}

The bipolar V_{pos}/V_{neg} can be obtained by simply tuning the duty-cycle of the driver output signal (OUT) via the oscillator feedback resistors R1 and R2. As a rule of thumb, for tuning duty-cycle and frequency:

- Always consider the core saturation limit of the transformer (6 V-µs for XT04). This limit must not be exceeded in the charging and discharging phase. Therefore, please select the switching frequency accurately.
- Duty-cycle only depends on R1 and R2. To reduce the duty-cycle, increase R1 and reduce R2, and vice versa to increase it.
- For a fixed R_p = R1//R2, the switching frequency can be increased by reducing C1, and vice versa to reduce it.

Please refer to Appendix **5** for the detailed formulas.

Table 1 shows the dimensioning for different bipolar splits; by default, Conf. A is considered. Relevant data such as voltage regulation and efficiency for the different configurations can be found in Section **3**.

Table 1 Recommended dimensioning for different bipolar voltage levels

Conf.	V_{pos} [1]	V_{neg} [1]	V_{CCI}	R1, R2, C1
A	+7 V	-4 V	12 V	5.1 kΩ, 22 kΩ, 120 pF
B	+9 V	-5 V	15 V	3.9 kΩ, 22 kΩ, 120 pF
C	+8 V	-6 V	15 V	4.3 kΩ, 22 kΩ, 120 pF
D[2]	+5 V	-4 V	10 V	7.5 kΩ, 22 kΩ, 120 pF

[1] Positive and negative rails are unregulated since Infineon's CoolGaN™ GIT HEMTs have a robust gate based on ohmic contact; see Section **3.1.1** for the behavior with the current load.
[2] This configuration is suitable for driving GaN HEMTs from other suppliers based on Schottky gate; it is additionally recommended to consider regulation of the positive voltage rail by enabling the on-board TL432 and related resistors.

2.4 Use-case example and mounting

The board is intended to replace a single-channel isolated gate driver IC on a main board, as shown in **Figure 7**. With 2.8 mm thickness, the KIT_1EDB_AUX_GaN can be directly soldered into the 8-pin DSO 150 mil footprint, with the shortest possible connection to the main board; this is important for the connection to the gate resistor in order to minimize the gate loop towards the GaN HEMT. Alternatively, proper connectors with 1.27 mm pitch could also be used.

Bipolar or unipolar driving can be enabled by means of J5, J6 jumpers as shown in **Figure 7**.

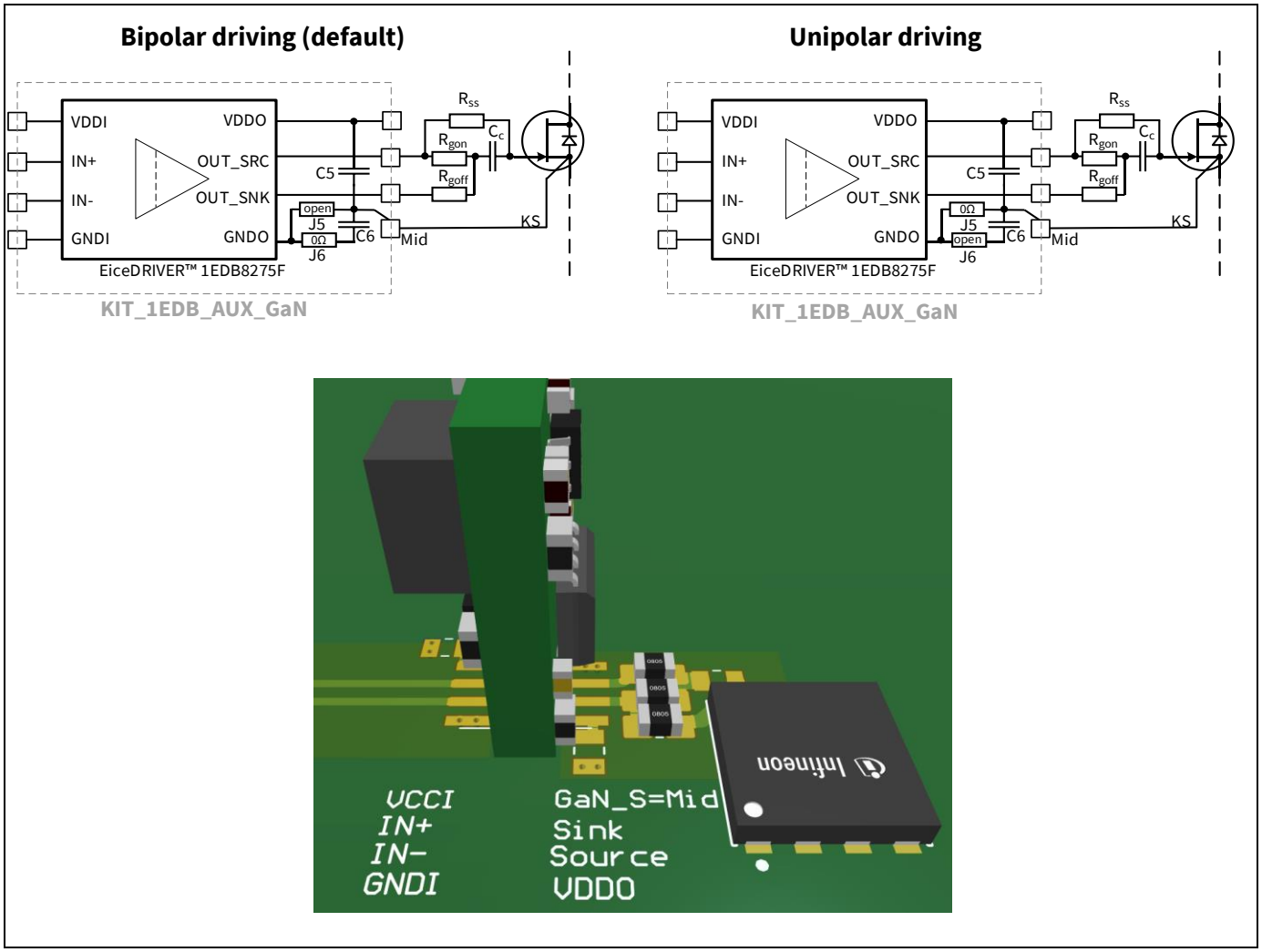

Figure 7 Mounting of KIT_1EDB_AUX_GaN on a main board

3 Measurement results

3.1 Output voltage regulation

The positive and negative voltage rails are unregulated, therefore they change with the current load I_{OUT} that depends on the switching frequency and on the selected GaN HEMT (by means of its charge).

Additionally, an inaccuracy on the V_{CCI} input voltage is also reflected in the value of V_{pos} and V_{neg}. Those two aspects are investigated in the next two subsections, where the output voltage regulation with load or inaccurate V_{CCI} are shown.

3.1.1 Output voltage regulation with load

Figure 8 shows the behavior of the bias supply output voltages V_{pos} and V_{neg} with different loads. The characterization is performed on the bias supply circuit alone by removing the EiceDRIVER™ 1EDB8275F and simply using resistors as loads. The voltages are measured with a 6½ digit multimeter.

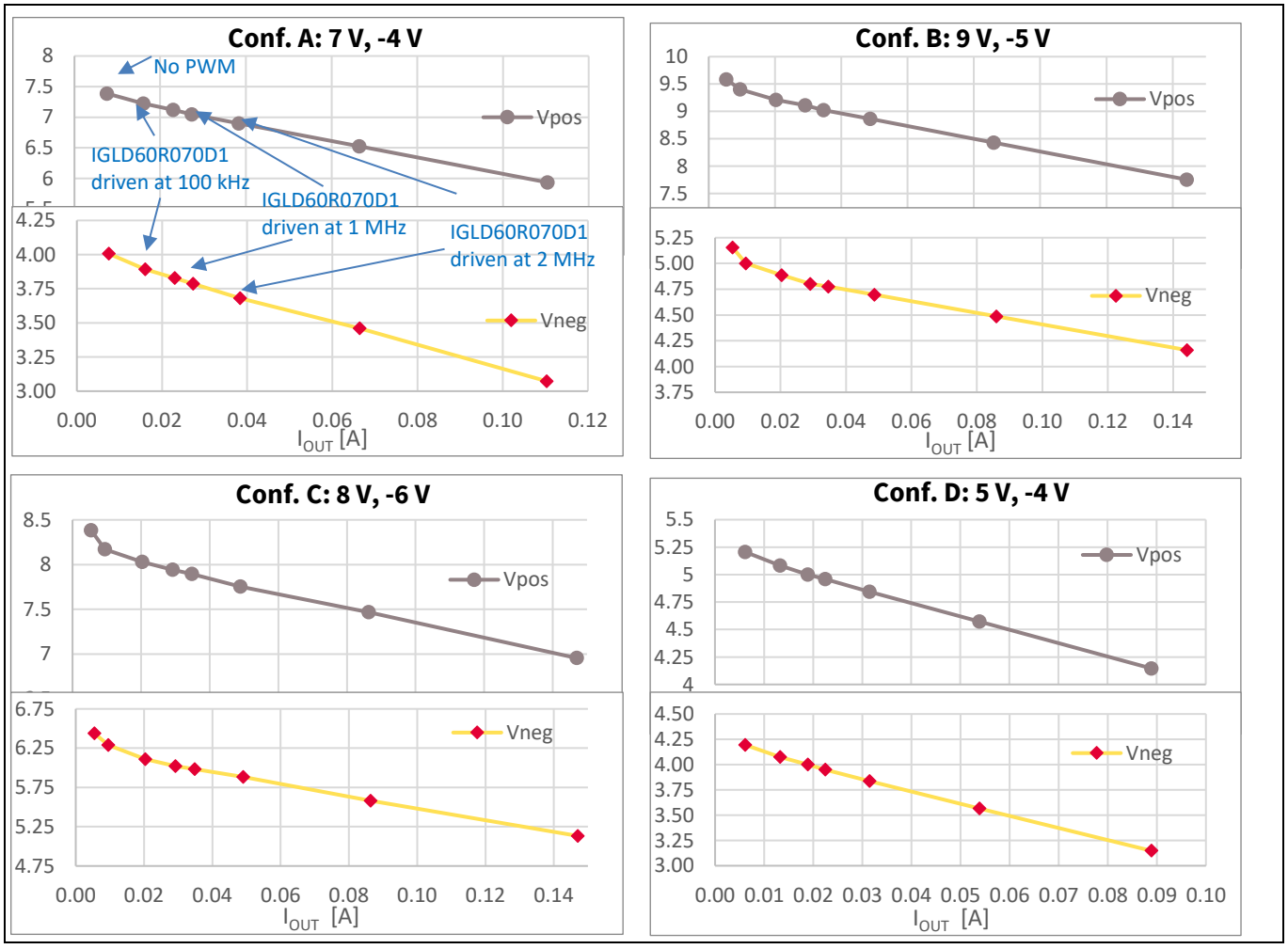

Figure 8 Bias supply output voltage V_{pos}, V_{neg} over output current load I_{OUT}

For Infineon's CoolGaN™ GaN HEMT that is a current-controlled switch, a limited variation of the positive rail voltage is not leading to a significant impact on the R_{DSON}. The variation of the negative rail over frequency instead could lead to first-pulse issues in case the negative voltage is not enough to prevent V_{GS} to reach the threshold. However, **Figure 10** shows that this voltage variation with the load is acceptable being limited to only few hundred of mV in typical use-cases.

Figure 9 also shows the bias supply output voltage behavior with different input currents. This is just a different view of **Figure 8**, and is provided for convenience because when driving a GaN device with KIT_1EDB_AUX_GaN, the user can more easily read I_{IN} from the DC power supply providing V_{CCI}. Here the I_{IN} mapping has been provided for Conf. A when driving Infineon's CoolGaN™ IGLD60R070D1 as an example.

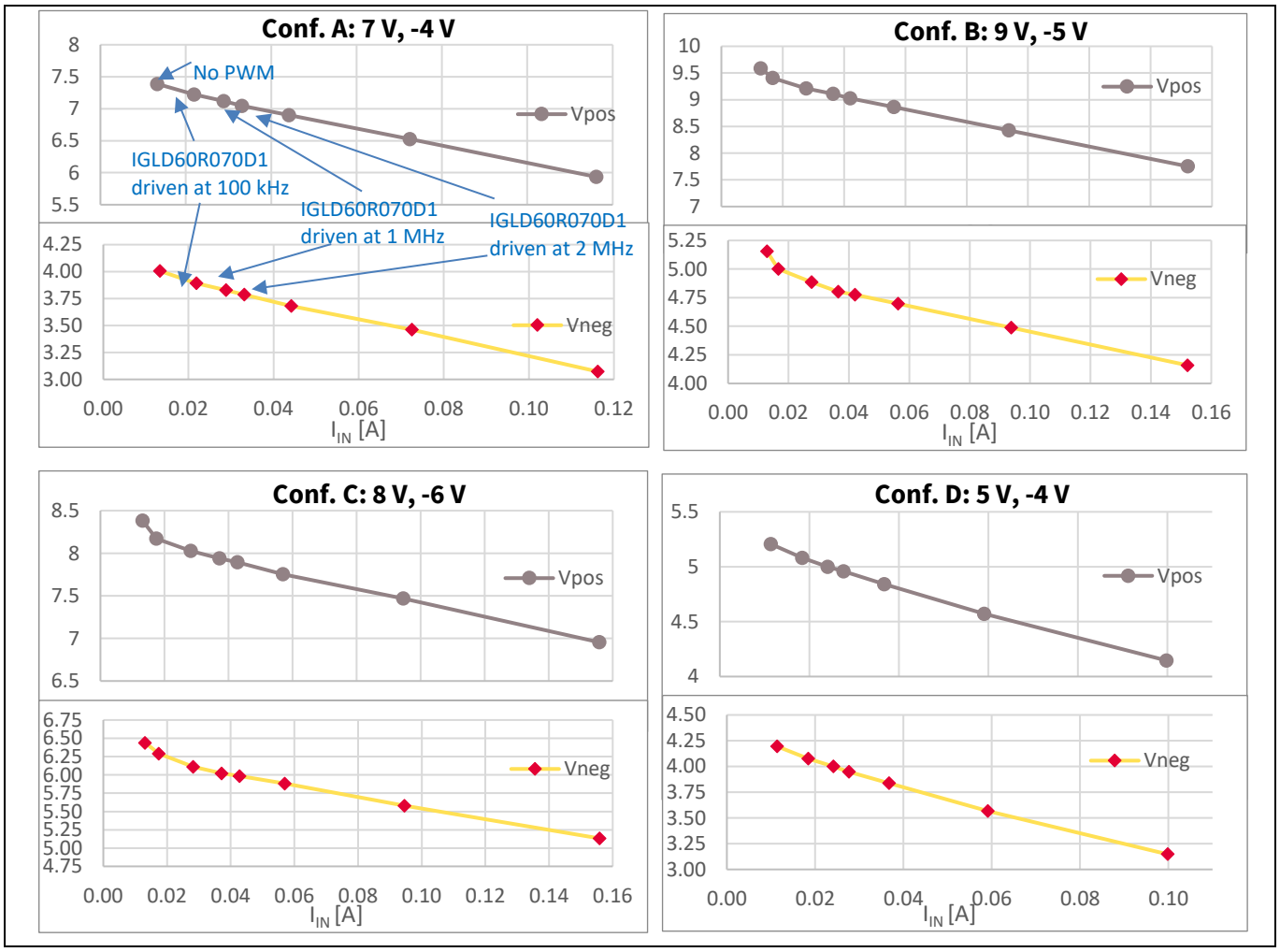

Figure 9 Bias supply output voltage V_{pos}, V_{neg} over input current I_{IN}

3.1.2 Output voltage regulation with input supply voltage V_{CCI}

The input supply voltage of the isolated DC-DC converter will have a certain inaccuracy that should be considered when looking at the output voltage regulation. **Figure 10**, **Figure 11**, **Figure 12** and **Figure 13** show the output voltage regulation for the different configurations considering a typical 5 percent accuracy.

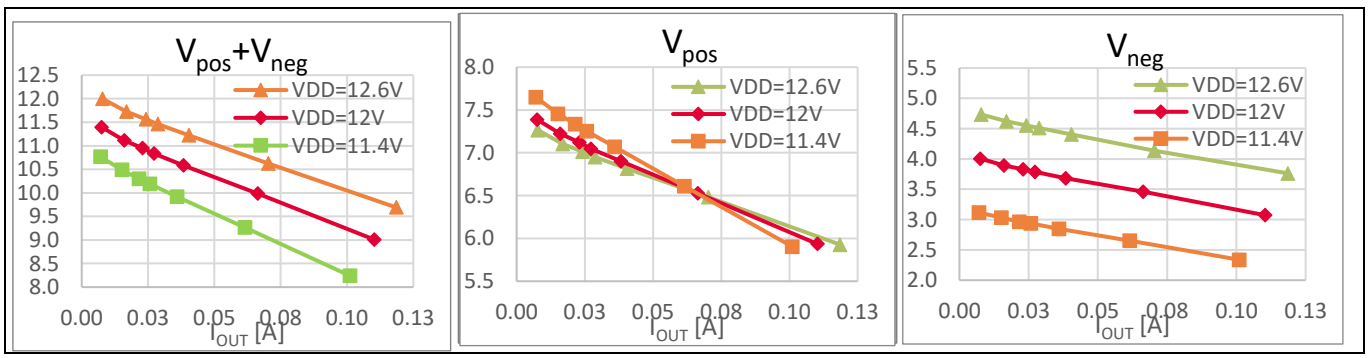

Figure 10 Regulation over output current with 5 percent inaccurate V_{CCI} voltage for Conf. A (7 V, -4 V)

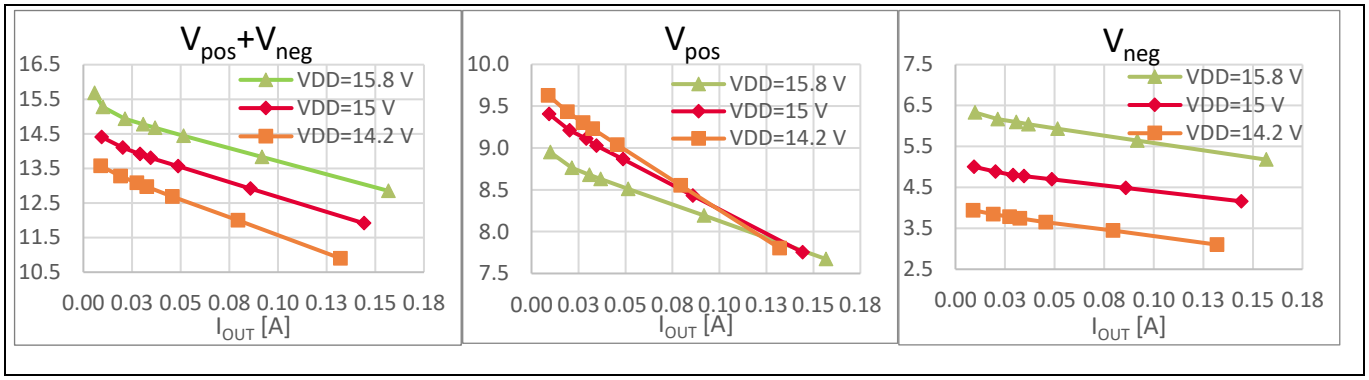

Figure 11 Regulation over output current with 5 percent inaccurate V_{CCI} voltage for Conf. B (9 V, -5 V)

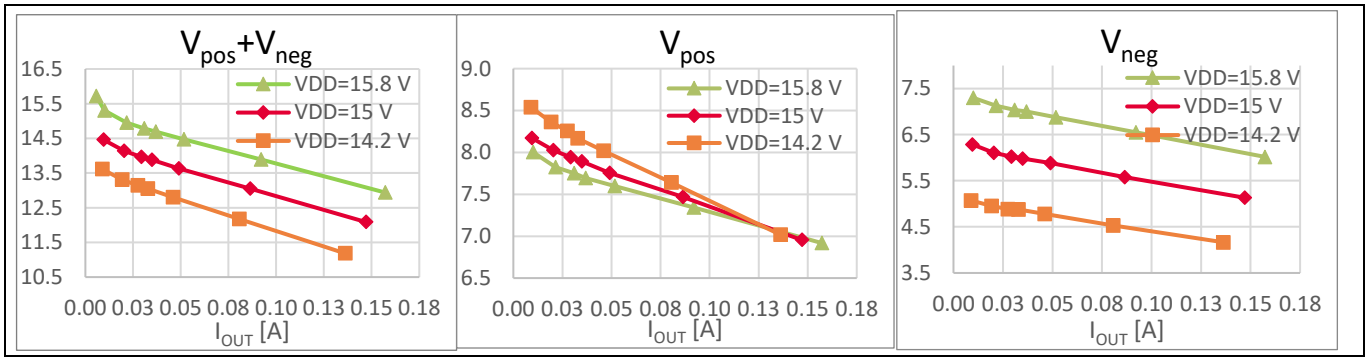

Figure 12 Regulation over output current with 5 percent inaccurate V_{CCI} voltage for Conf. C (8 V, -6 V)

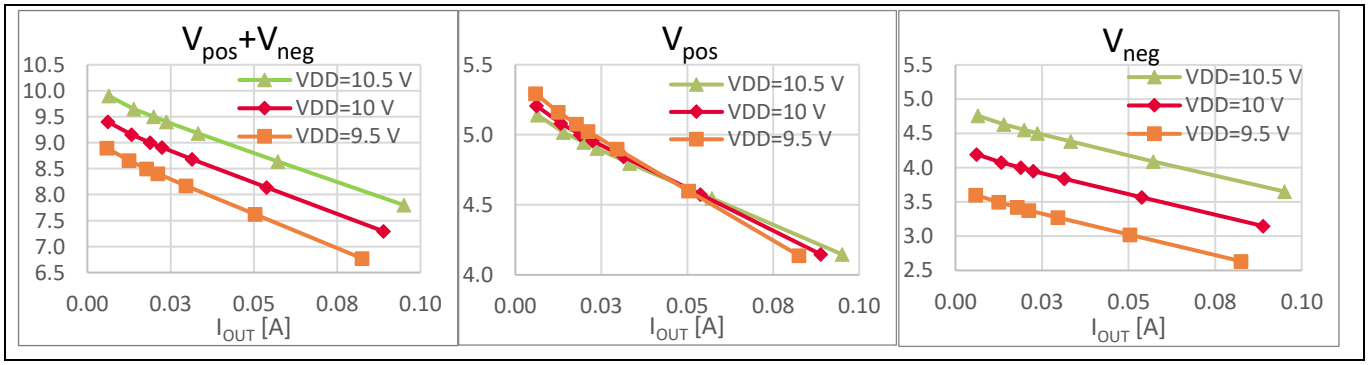

Figure 13 Regulation over output current with 5 percent inaccurate V_{CCI} voltage for Conf. D (5 V, -4 V)

3.2 Efficiency

Figure 14 shows the efficiency for Conf. A, B, C and D over output power and input supply voltage V_{CCI}. As shown previously for the output voltage regulation, the efficiency is measured with the bias supply circuit alone without the EiceDRIVER™ 1EDB8275F; simple resistors have been used as load for the bias supply. 0.1 Ω shunts are used for input and output current measurement, and a 6½ digit multimeter is used to measure the voltages.

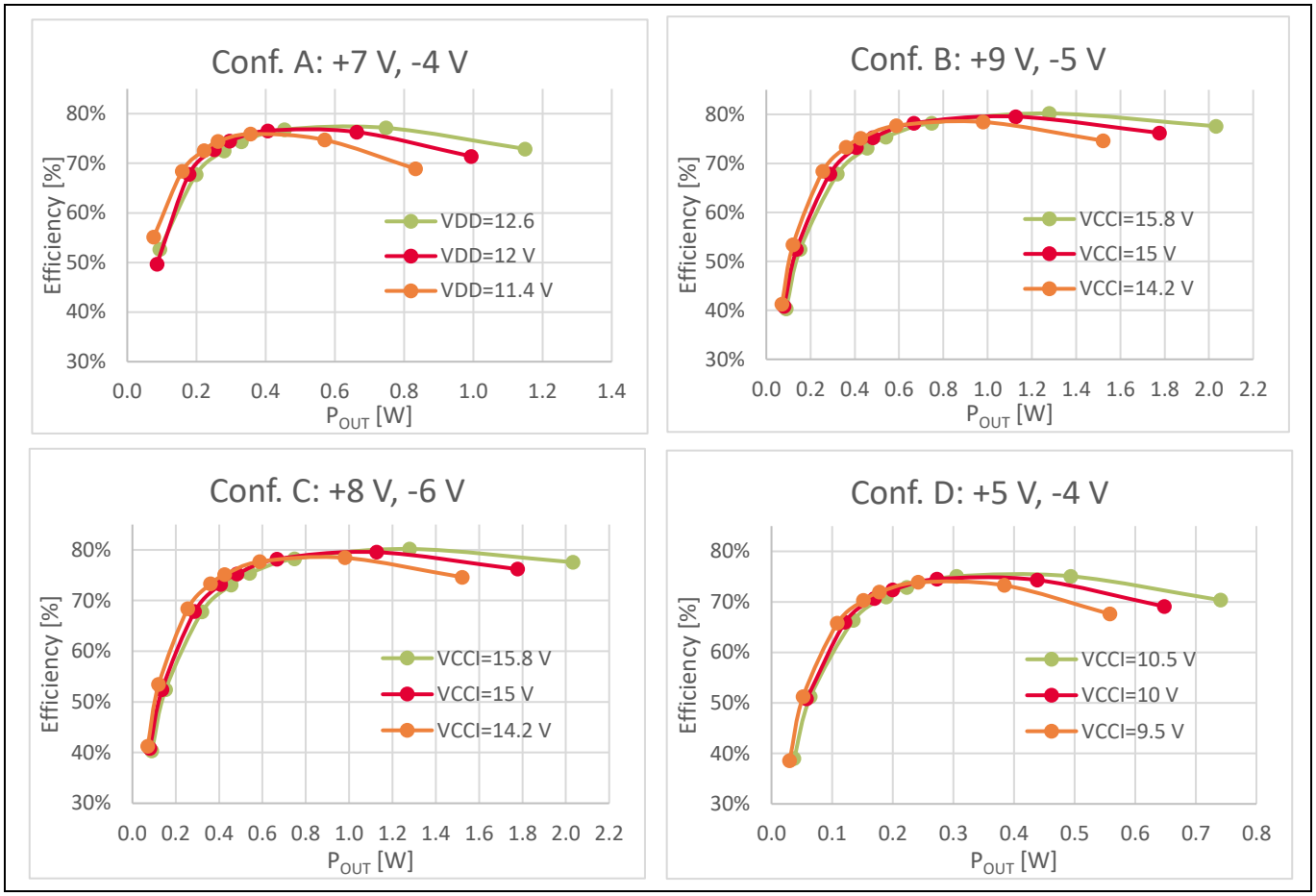

Figure 14 Efficiency over output power for inaccurate 5 percent V_{CCI}

A different view with the efficiency over output current and input current is provided in **Figure 15**.

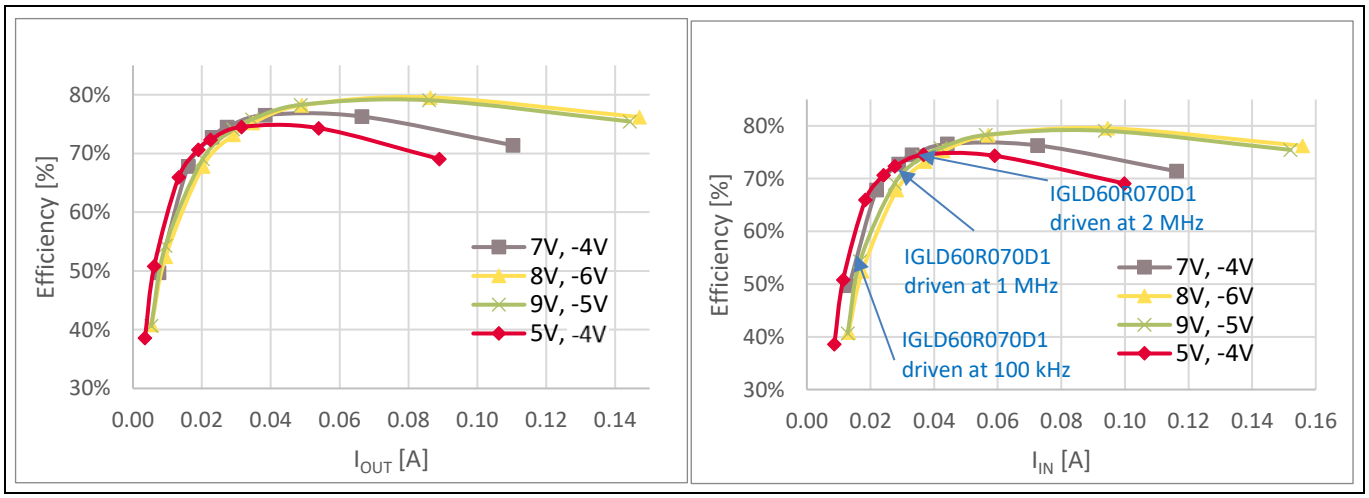

Figure 15 Efficiency at nominal V_{CCI} over output current (left) and input current (right)

The efficiency graph over input current in particular allows easy reading for the user, who can simply read I_{IN} from the DC power supply while providing V_{CCI}; here the I_{IN} mapping has been provided for Conf. A when driving Infineon's CoolGaN™ IGLD60R070D1 at different frequencies as an example.

3.3 Operating waveforms

The operating waveforms for the bias supply in Conf. A, B, C, D are shown in **Figure 16**. The bias supply switching frequency (see C3, V_{trafo}) varies from one configuration to the other because of the different V_{CCI} and R1, but it always fulfills the 6 V-µs transformer saturation limit. The duty-cycle also varies with V_{pos}, V_{neg} ratio.

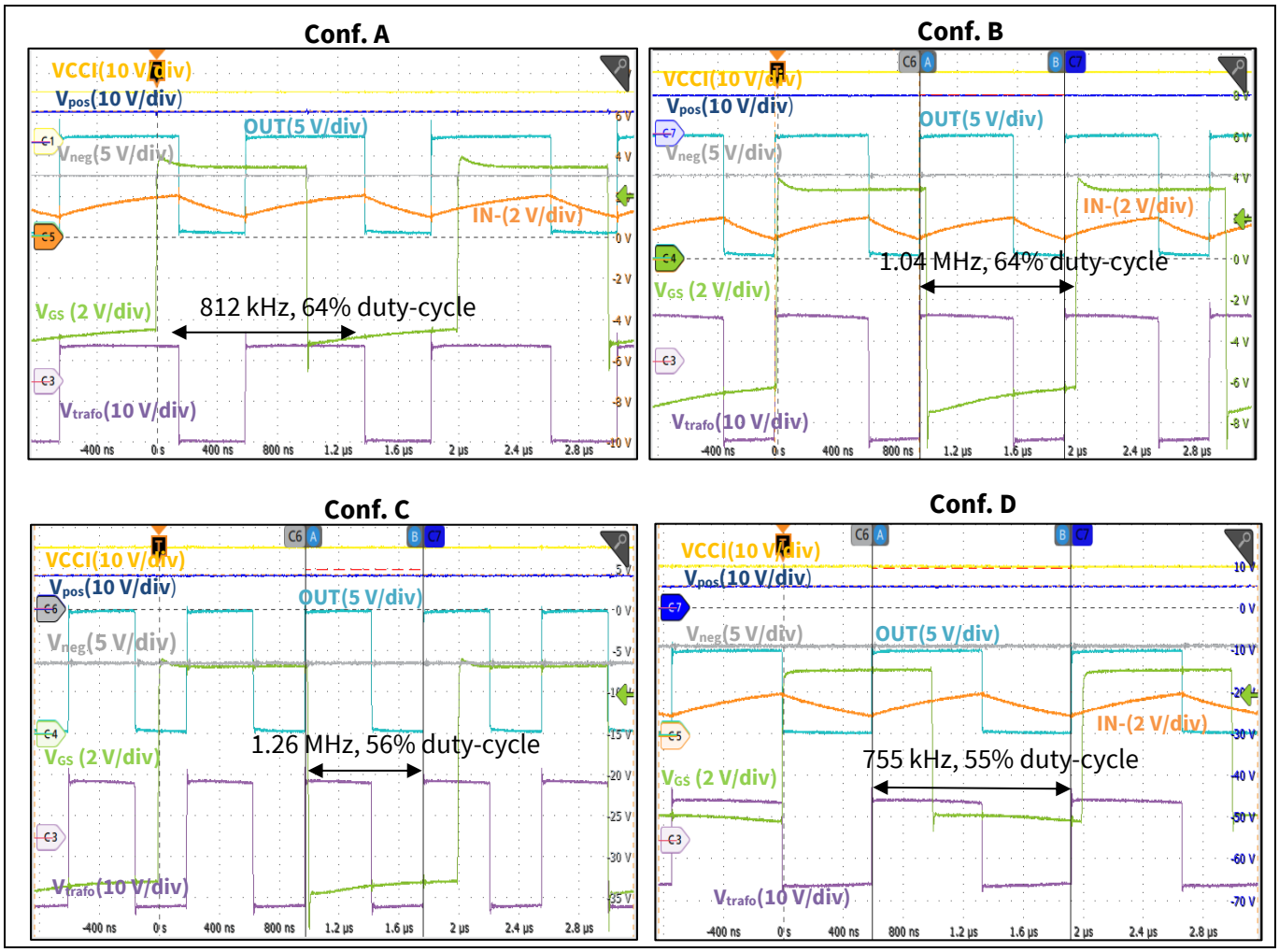

Figure 16 Bias supply operating waveform for Conf. A, B, C, D

In this example KIT_1EDB_AUX_GaN drives one Infineon CoolGaN™ IGLD60R070D1 at 500 kHz; selected coupling gate capacitor C_c is 2.2 nF and static resistance R_{ss} is 470 Ω. The gate-to-source voltage (green, C4) in the OFF-state has an exponential decaying shape with an offset given by the negative bias voltage V_{neg}; the exponential decaying shape instead depends on the charge stored in the coupling capacitor. The value of $V_{GS,OFF}$ at the beginning of turn-off fulfills formula (1):

$$V_{GS,OFF} = -V_{neg} - \frac{C_C\,(V_{pos}-V_F)-Q_{Geq}}{C_C+C_{GS}} \quad (1)$$

with Q_{Geq} denoting an equivalent application-specific gate charge, i.e., Q_{Geq} ~ Q_{GS} for hard-switching and Q_{Geq} ~ Q_{GS} for soft-switching transitions.

3.4 Start-up behavior

The power supply is designed to work at nominal V_{CCI}; however, when the input supply is ramping up and down (e.g., start-up, shutdown) the bias supply could work in an unwanted condition. The isolated DC-DC converter

must be able to leave this operating mode safely. **Figure 17** and **Figure 18** show a start-up of the board with, respectively, a fast and slow V_{CCI} ramp when driving Infineon's CoolGaN™ IGLD60R070D1 at 2 MHz; high load is the most critical case to look at.

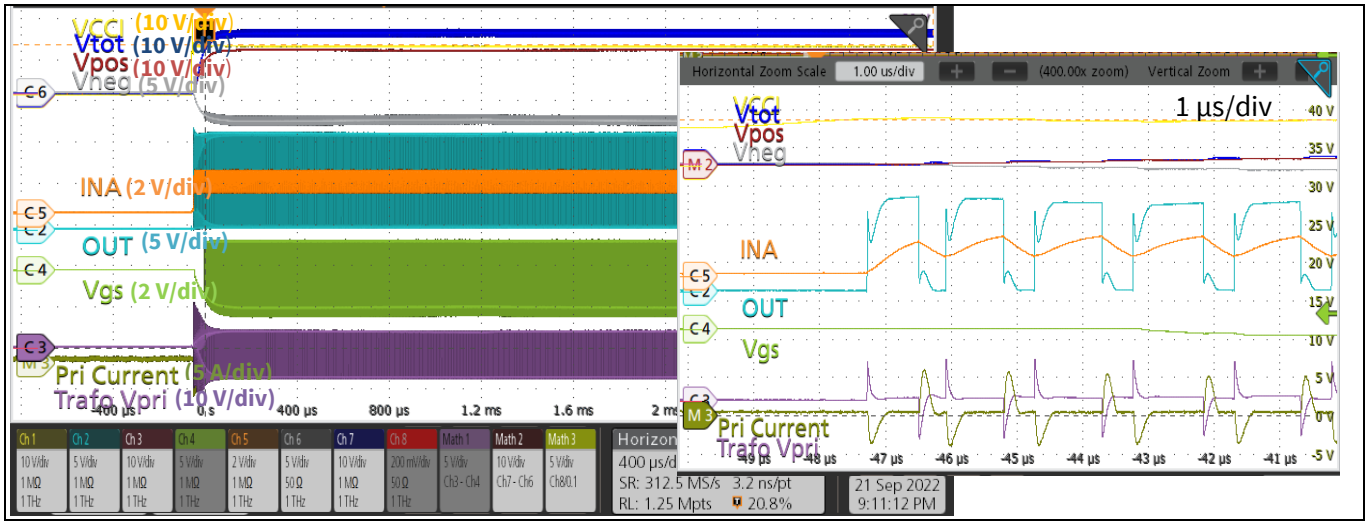

Figure 17 Fast start-up driving Infineon's CoolGaN™ IGLD60R070D1 at 2 MHz in Conf. A

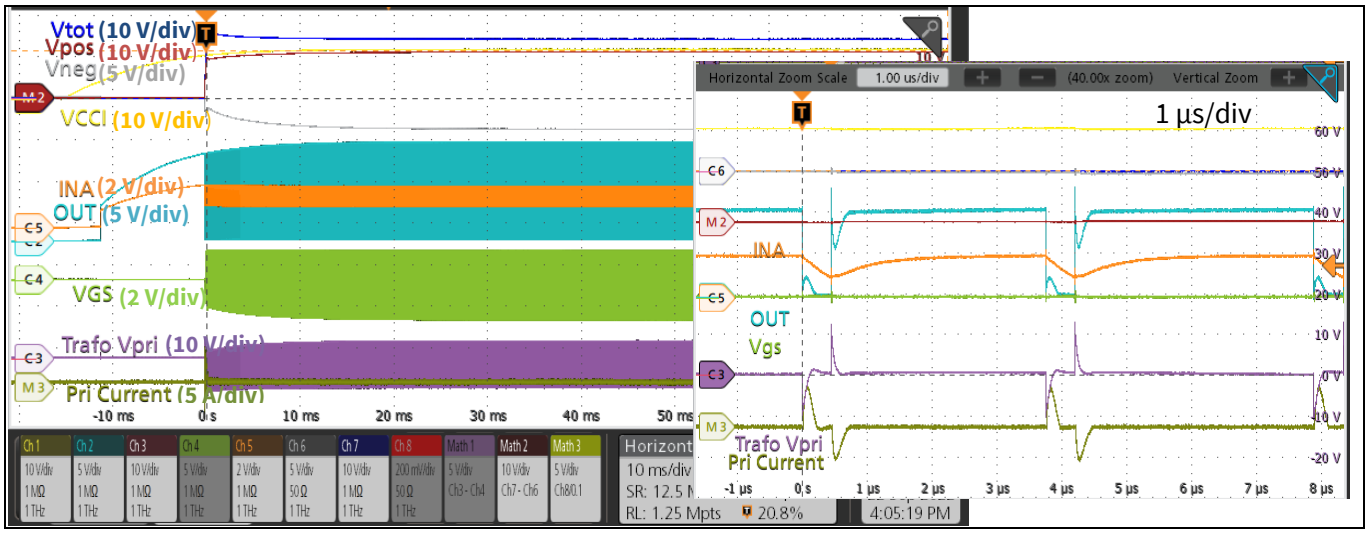

Figure 18 Slow start-up driving Infineon's CoolGaN™ IGLD60R070D1 at 2 MHz in Conf. A

During start-up, high current (see M3, dark green) flows in the bias supply when the output capacitors are still discharged. This current should be contained to avoid overheating of EiceDRIVER™ 1EDN7511B and potential saturation of the transformer. This is possible by placing a limited resistor R3 or reducing the coupling capacitor C3. In this design a relatively small value for C3 (48 nF) has been selected; this way, in high-current events (start-up, output short-circuits), this capacitor completely charges and discharges at any cycle, thus limiting the time-duration of the current and the voltage stress on the transformer (see zooms). The 48 nF selection has been dictated especially from the necessity to avoid prolonged transformer saturation in output short-circuit events.

In addition, it should be checked that the -10 V static rating of Infineon's CoolGaN™ GIT HEMT and GaN switches from other suppliers is fulfilled. This design does not experience significant overshoot and undershoot of positive and negative rails.

3.5 Shutdown behavior

Figure 19, **Figure 20**, **Figure 21** show three shutdown scenarios: the input voltage V_{CCI} is turned off via the DC voltage generator (with its internal impedance), the input voltage is disconnected to emulate a “sudden open” and finally V_{CCI} is short-circuited. For shutdown the more critical condition is the light-load, because the bias supply takes longer to discharge its output capacitors and then stays longer in this condition.

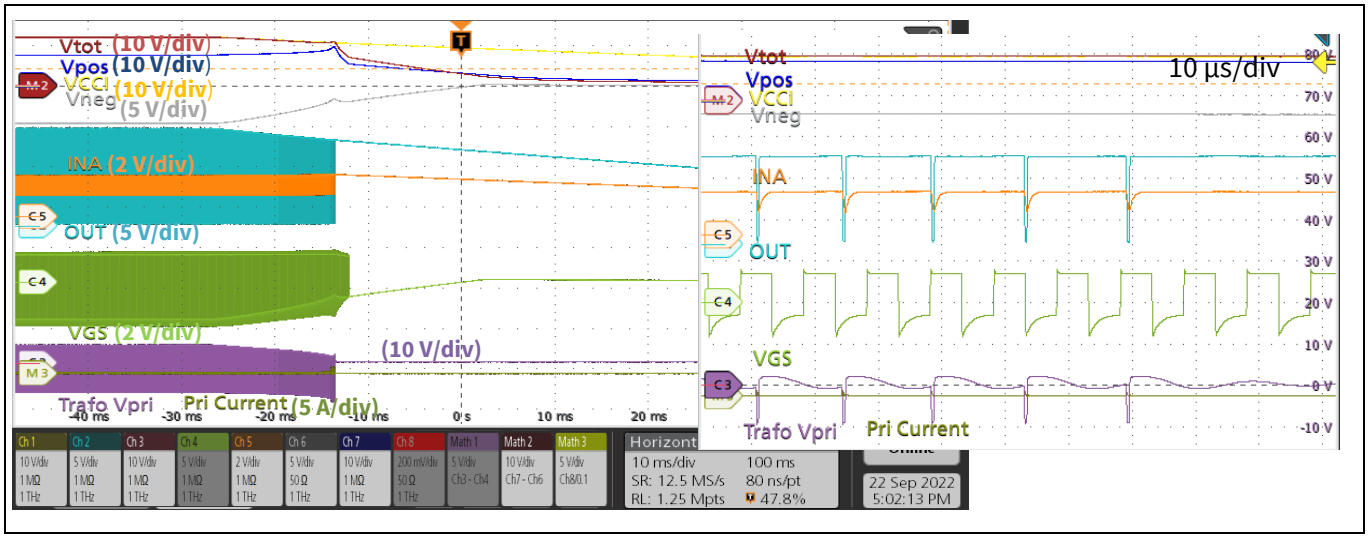

Figure 19 Shutdown via V_{CCI} OFF driving Infineon’s CoolGaN™ IGLD60R070D1 at 100 kHz in Conf. A

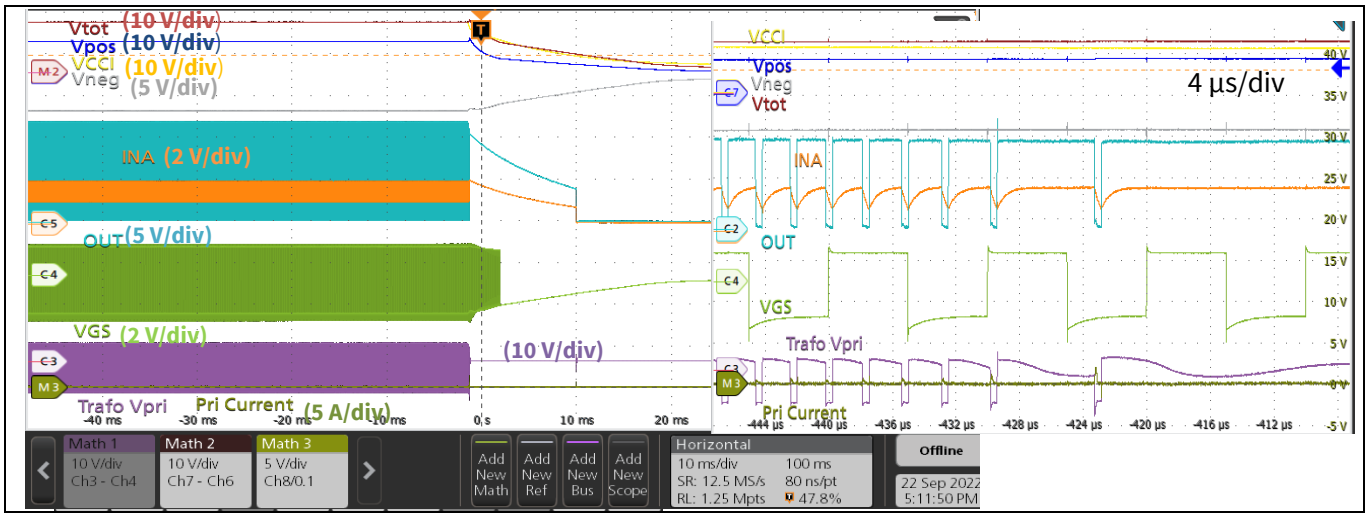

Figure 20 Shutdown via V_{CCI} open driving Infineon’s CoolGaN™ IGLD60R070D1 at 100 kHz in Conf. A

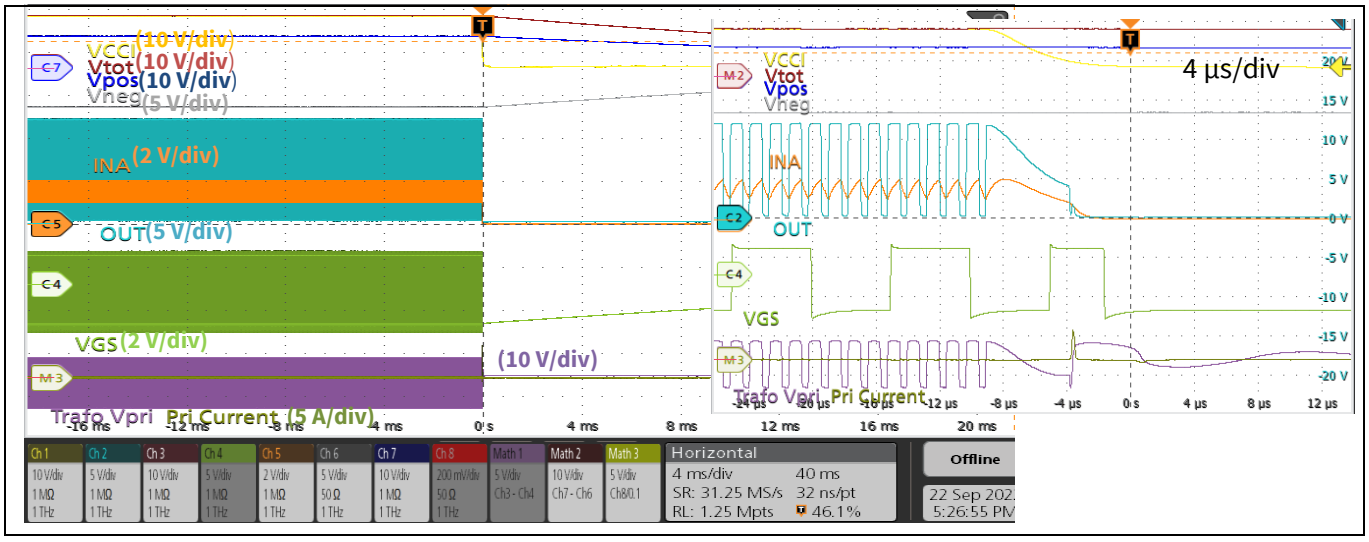

Figure 21 Shutdown via V_{CCI} short driving Infineon's CoolGaN™ IGLD60R070D1 at 100 kHz in Conf. A

3.6 Output short-circuit

In case of failure in the power stage, the GaN HEMT gate-to-source and the EiceDRIVER™ 1EDB8275F output stage itself could show a very low impedance towards the bias supply leading to an increased load current; the bias supply circuit has to survive this special condition.

Figure 22, **Figure 23** and **Figure 24** show what happens on the bias supply when its output (V_{tot}, V_{pos} and V_{neg} respectively) is short-circuited. The bias supply circuit is robust to short-circuit in these stress conditions without showing a prolonged saturation of the main transformer or ICs failure. As mentioned already in Section **3.4**, this is enabled by the selection of 48 nF for the capacitor C3, that is acting as a current limiter.

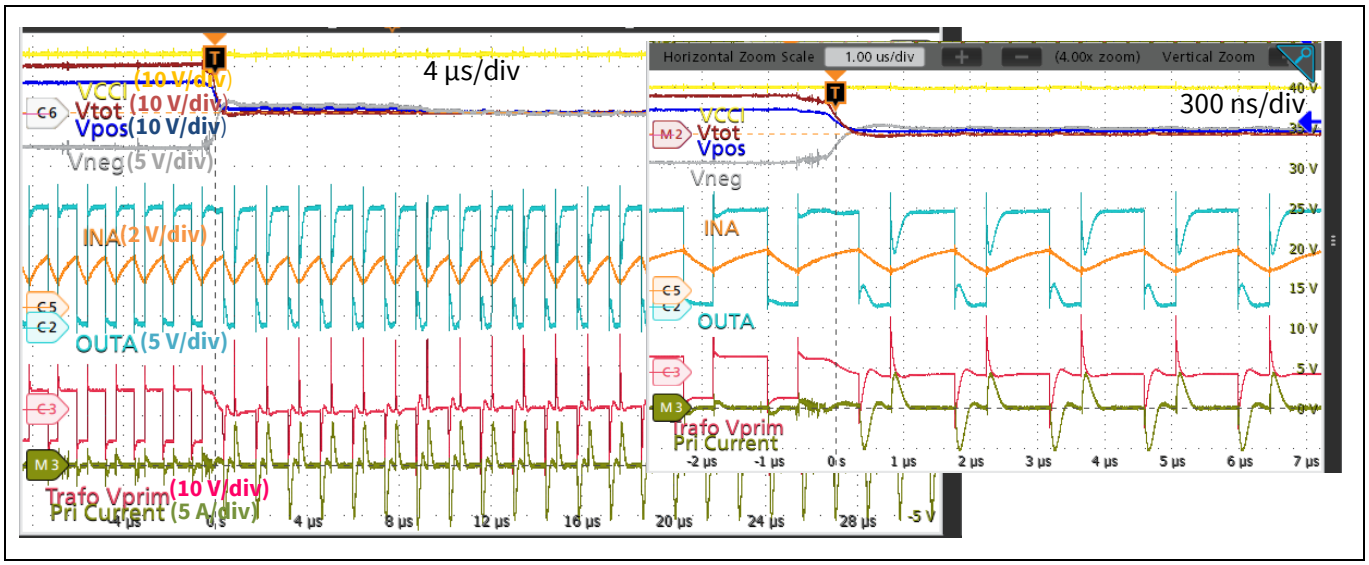

Figure 22 Output short-circuit on bias supply output V_{tot} (detail on the right-hand side)

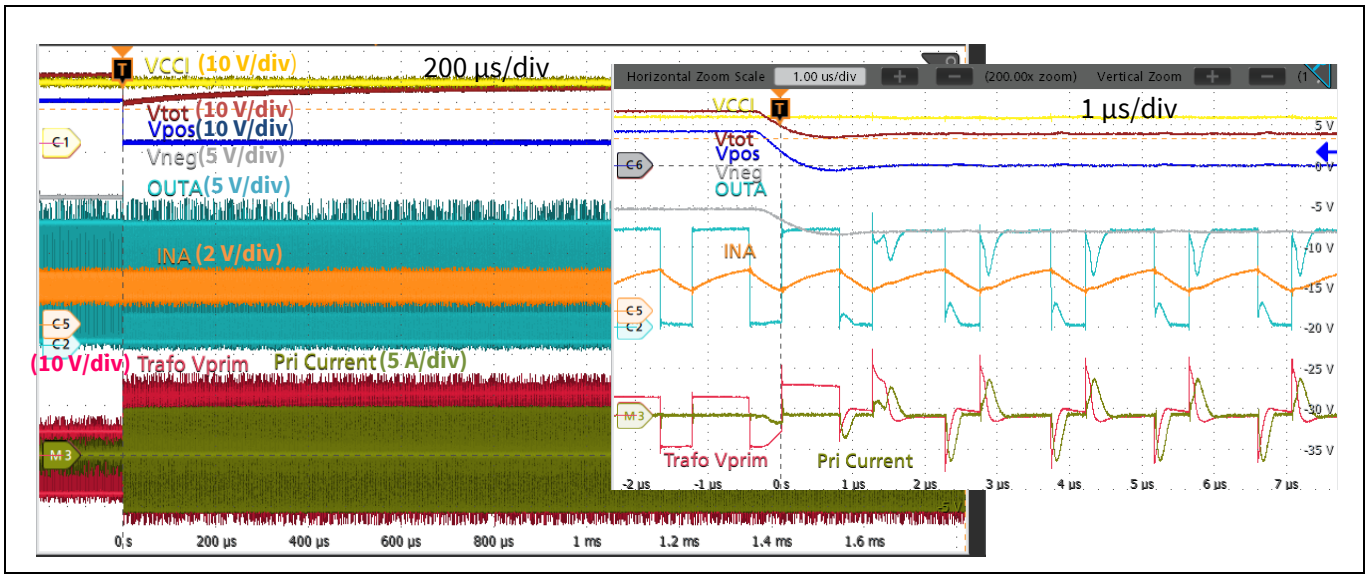

Figure 23 Output short-circuit on bias supply output V_{pos} (detail on the right-hand side)

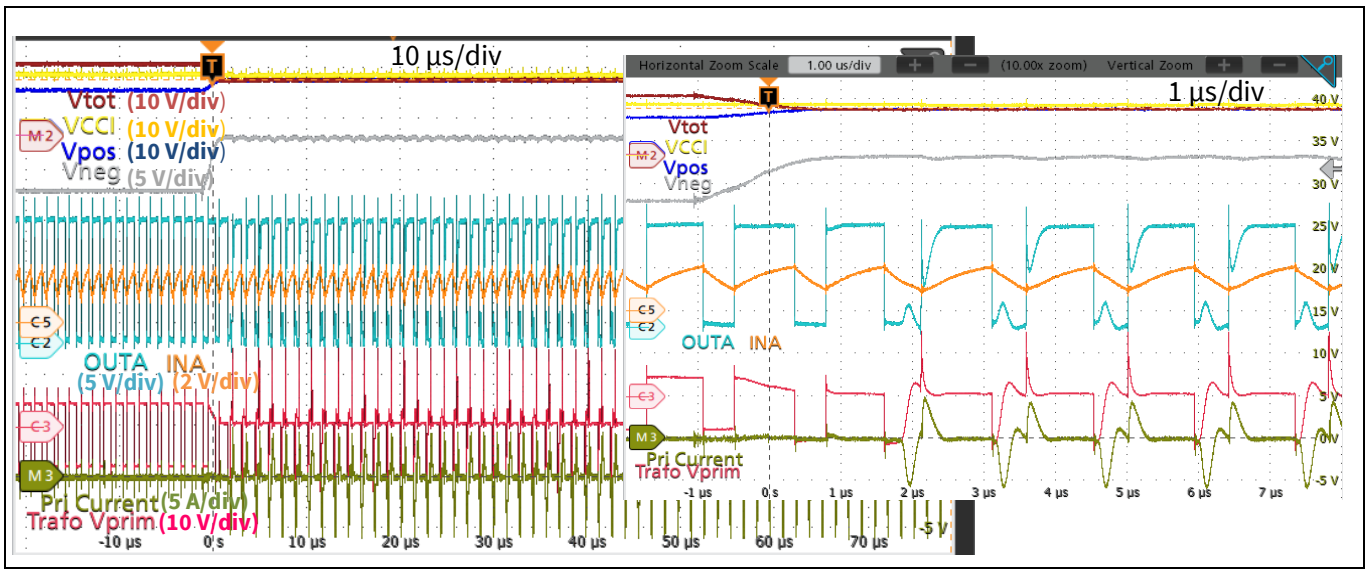

Figure 24 Output short-circuit on auxiliary supply output V_{neg} (detail on the right-hand side)

3.7 Operation at high voltage and high CMTI

The CMTI robustness of the bias supply circuit has been checked in the EVAL_2EDB_HB_GaN evaluation board. This board includes the same bias supply, with the only difference in this case being that the EiceDRIVER™ 1EDN7511B drives two transformers to provide the isolated voltage supplies to both the low-side and the high-side gate driver ICs.

Figure 25, as an example, shows the results of the double pulse and confirms operation up to 150 V/ns. More waveforms, at different test modes (double pulse, buck-mode, boost-mode) and different frequencies (100 kHz to 2 MHz) can be found in application note **[1]**.

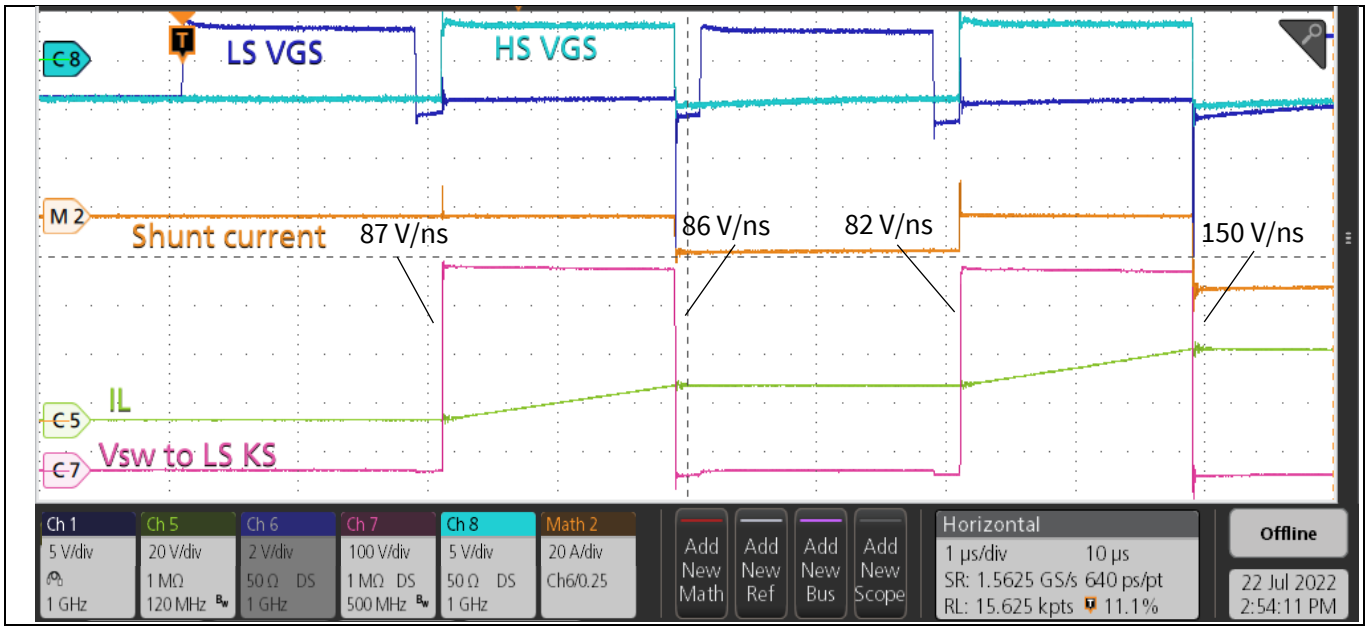

Figure 25 **Bias supply shows more than 150 V/ns CMTI capability – example of reverse double pulse in the evaluation board EVAL_2EDB_HB_GaN**

4 Layout

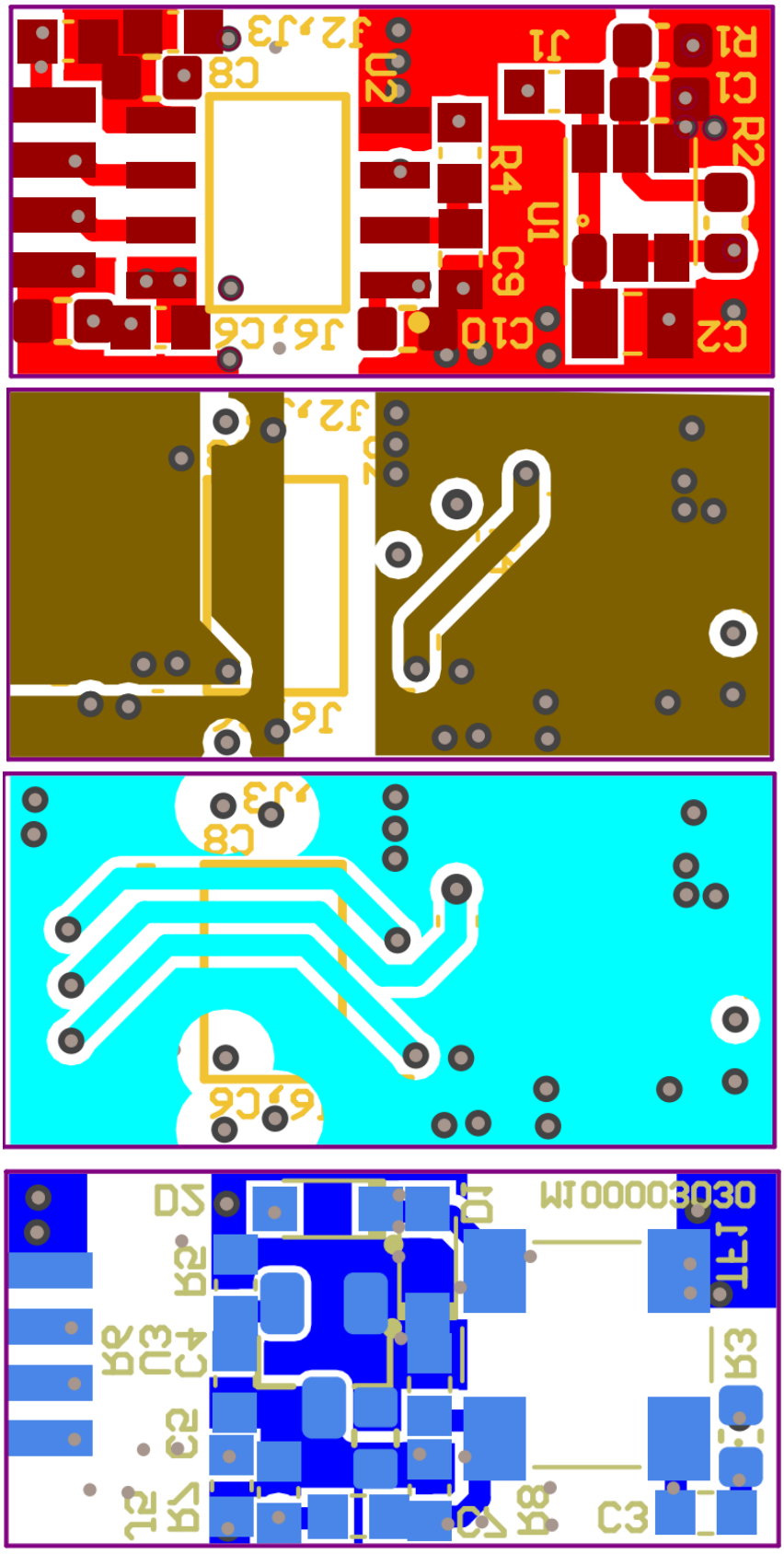

Figure 26 Layout, from top to bottom: top layer, mid-layer1, mid-layer2, bottom layer

#	Name	Material	Type	Weight	Thickness	Dk	Df
	Top Overlay		Overlay				
	Top Solder	Solder Resist	Solder Mask		0.01016mm	3.5	
1	Top Layer		Signal	1oz	0.035mm		
	Dielectric 1	FR-4	Dielectric		0.32004mm	4.8	
2	Mid-Layer 1		Signal	1oz	0.035mm		
	Dielectric2	FR-4	Dielectric		2mm	4.8	
3	Mid-Layer 2		Signal	1oz	0.035mm		
	Dielectric3	FR-4	Dielectric		0.32004mm	4.8	
4	Bottom Layer		Signal	1oz	0.035mm		
	Bottom Solder	Solder Resist	Solder Mask		0.01016mm	3.5	
	Bottom Overlay		Overlay				

Figure 27 Layer stackup

5 Appendix A

The ring oscillator behavior has been described in Section **2.2**. Clearly the duty-cycle and the frequency of the OUT signal can be tuned by acting on the charging and discharging phase of INA (IN- pin of the EiceDRIVER™ 1EDN7511B), as illustrated in **Figure 28**.

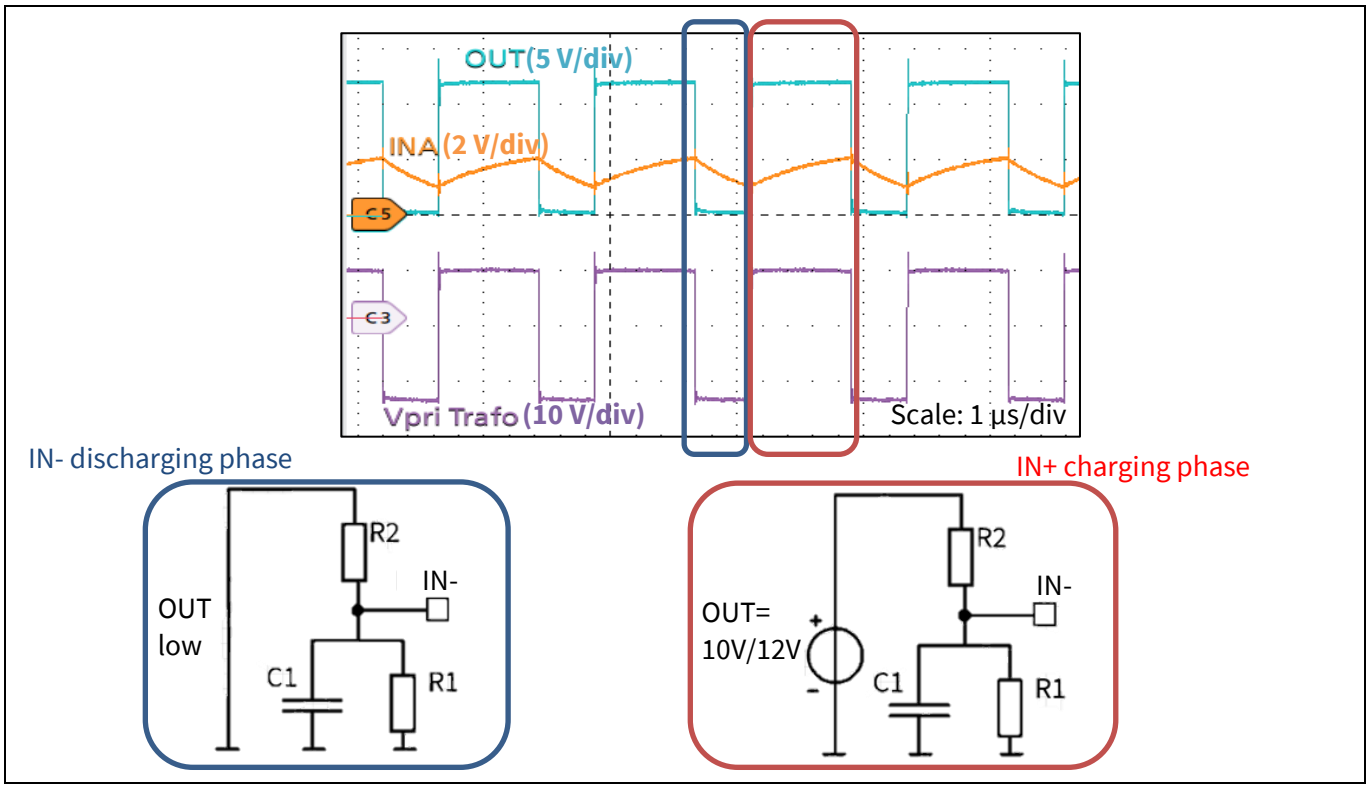

Figure 28 IN- charging and discharging mechanisms

Please follow the dimensioning steps described below.

1. Calculate the duty-cycle D according to formula (4):

$$D \cong \frac{V_{pos}}{V_{CCI} - 1V} \quad (4)$$

Where 1 V is a typical voltage drop expected on the bias supply output.

Example: for V_{pos}= 7 V, V_{neg}= -4 V from V_{CCI} = 12 V → D = 64 percent

2. Calculate the minimum t_{on}, t_{off} (minimum switching period) allowed from the core-saturation limit of the selected transformer (6 V-µs for XT04). The minimum period T_{min} can be selected according to formula (5) with some margin:

$$T_{min} = \frac{t_{off,max}}{D} = \frac{6\ V\mu s}{V_{neg} * D} \quad (5)$$

Example: for V_{pos}= 7 V, V_{neg}= -4 V and D = 64 percent → T_{min} = 2.34 µs → f_{sw} = 427 kHz → $f_{selected}$ = 812 kHz with margin

3. Fix the value of C1 in the range of 100 pF to 1 nF.

Example: Selected 120 pF

4. Calculate R_p = R1//R2 from equation (6):

$$R_p = \frac{1.35 * t_{OFF}}{C1} = \frac{1.35 * (1 - D)}{f_{selected} * C1} \quad (6)$$

Example: With $f_{selected}$ = 812 kHz and D = 64 percent → R_p = 4.99 kΩ

5. Calculate R2 from equation (7).

$$V_{INH} = e^{-\frac{0.57\,D}{1-D}} (V_{INL} - \frac{R_p}{R2} V_{CCI}) + \frac{R_p}{R2} V_{CCI} \quad (7)$$

Where V_{INH} = 2.1 V, V_{INL} = 1 V is the input voltage threshold of the driver.

Example: With R_p = 4.99 kΩ → R2 = 22 kΩ according to the dimensioning in **Figure 4**.

6. Make sure that the selected values fulfill equation (8):

$$V_{IN-} = \frac{R_1}{R_1 + R_2} V_{DD} > V_{INHL} \quad (8)$$

This is necessary to ensure that the oscillation takes place.

Complete derivation of equation (6)

Equation (7) is derived from IN- discharging phase as per equation (9):

$$V_{IN-}(t) = V_{IN-}(t_0) e^{-\frac{t}{R_P C1}} \quad (9)$$

At the end of the discharging phase for t = t_{off}:

$$V_{IN-}(t_{OFF}) = V_{INL} = V_{INH}\, e^{-\frac{t_{off}}{R_P C1}} \rightarrow R_p = \frac{-t_{OFF}}{C1} * \frac{1}{\ln \frac{V_{INL}}{V_{INH}}} \quad (10)$$

Complete derivation of equation (7)

Equation (7) is derived from the IN- charging phase. From Kirchhoff laws:

$$i = \frac{V_{IN-}}{R1} + C_1 \frac{dV_{IN-}}{dt}$$
$$V_{IN-} = V_{CCI} - R_2 * i \quad (11)$$

This leads to the following first-order differential equation:

$$\frac{dV_{IN-}}{dt} + \frac{1}{R_P C_1} V_{IN-} = \frac{V_{CCI}}{R_2 C_1} \quad (12)$$

Equation (12) has the following resolution:

$$V_{IN-}(t) = e^{-\frac{t}{R_P C1}} \left[V_{INL} - \frac{R_P}{R_2} V_{DD}\right] + \frac{R_P}{R_2} V_{CCI} \quad (13)$$

At the end of the charging phase for t = t_{ON}:

$$V_{IN-}(t_{ON}) = V_{INH} = e^{-\frac{t_{ON}}{R_P C1}} \left[V_{INL} - \frac{R_P}{R_2} V_{CCI}\right] + \frac{R_P}{R_2} V_{CCI} \quad (14)$$

By including (10) in (14), equation (7) can be derived.

References

[1] C. Matrisciano, " Half-bridge evaluation board designed with CoolGaN™ GIT HEMTs and EiceDRIVER™ 2EDB8259Y. EVAL_2EDB_HB_GaN", Infineon Technologies AG, Application Note **AN_2210_PL21_2211_151906**, 2022.

[2] B. Zojer, "Driving 600 V CoolGaN™ high electron mobility transistors", Infineon Technologies AG, Application Note **AN_201702_PL52_012**, 2018.

[3] D. Varajao, B. Zojer, "**Gate drive solutions for CoolGaN™ GIT HEMT**: Exploiting the full potential of GaN", Infineon Technologies AG, Whitepaper B152-I1089-V1-7600-EU-EC, 2021.

[4] D. Varajao, T. Ferianz, V. Zhang, and C. Matrisciano, "Driving GaN HEMT High-Voltage Half-Bridge with a Single-Channel Non-Isolated Gate Driver with Truly Differential Inputs", PCIM Europe 2020; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany, 2020, pp. 1-8.

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