Isolated -48 V to 50 V converter for telecom applications

Digitally controlled 750 W FB-FB power supply using XDPP1140

About this document

Scope and purpose

This application note provides the reference design and performance of an isolated -48 V to 50 V digital power supply using XDPP1140. The topology is full-bridge primary with full-bridge rectification (FB-FB).

XDPP1140-100B is the enhanced version of digital controller XDPP1100-Q024. The key improvements include:

- High performance feed-forward with high digital resolution
- More accurate input voltage telemetry
- Wider range for transformer turns ratio
- Higher speed current sensing
- Flexible burst mode operation
- Flux balancing

Intended audience

This document is intended for application engineers and designers who uses the telecom power modules

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Glossary

Table 1 Definitions of acronyms, symbols, and terms

Acronym, symbol or term	Definition
ADC	Analog-to-digital converter
DE	Diode emulation
DMM	Digital multimeter
FB	Full-bridge
FF	Feed-forward
FTR	Fast transient response
FW	Firmware
LSB	Least significant bit
NTC	Negative temperature coefficient
N_p	Transformer primary-side number of turns
N_s	Transformer secondary-side number of turns
PID	Proportional-integral-derivative filter
PWM	Pulse width modulation
RAM	Random-access memory
SR	Synchronous rectification/synchronous rectifier
TS	Telemetry sense
VMC	Voltage mode control
VRS	Rectification voltage sense
V_{IN}	Input voltage
V_{DS}	MOSFET drain to source voltage
V_{OUT}	Output voltage
V_{RECT}	Transformer secondary rectified voltage

1 Introduction

28 V and 50 V are the two typical voltages used in telecommunication equipment such as base stations, including 5G networks. Isolated FB-FB converter is the industry typical topology for these applications.

Infineon Evaluation Board EVAL_XDPP1140_FBFB_50V aims to address this application requirement. Compared to the previous design detailed in [1], this new design utilizes the Infineon XDPTM XDPP1140-100B digital power controller that takes the design to the next level. It offers configuration flexibility and exceptional performance. FW patch is no longer required for transformer turns ratio with Ns:Np higher than 1; telemetry sense ADC has increased input voltage range; feed-forward hardware has been redesigned to deliver better resolution and reduces output voltage ripple; burst mode support is added for light-load efficiency improvement.

This evaluation board has an input voltage range of -36 V to -60 V DC. The nominal output voltage is 50 V, with a maximum output current of 15 A, corresponding to a maximum output power of 750 W.

The simplified schematic and block diagram for this converter is shown in Figure 1. It consists of full-bridge topology with full-bridge synchronous rectification, and active clamp circuits. The functionally isolated (coreless transformer technology) gate driver EiceDRIVER™ 2EDF7275K is used for driving all MOSFETs. On the primary-side, 80 V power MOSFETs in a SuperSO8 package from the latest OptiMOS™ 6th generation are used. For the secondary-side full-bridge, the 3:5 transformer step-up ratio dictates the need for 150 V rated devices, and OptiMOS™ 5 150 V serve as SRs in this application.

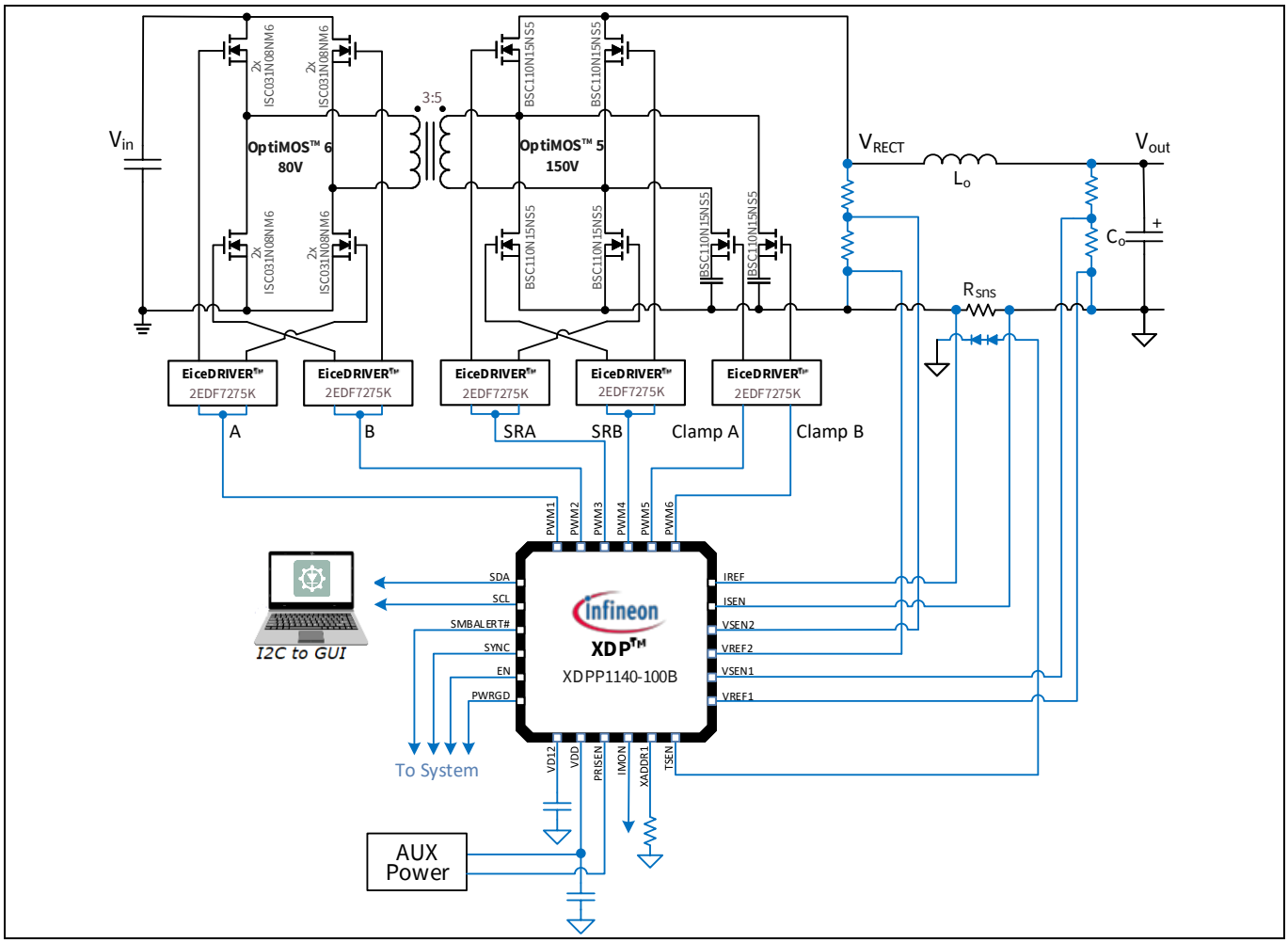


Figure 1 Block diagram of the Infineon EVAL_XDPP1140_FBFB_50V

Compared to [1], major hardware changes are:

- The new digital power controller XDPP1140-100B is used instead of XDPP1100-Q024
- Current sensing: a common mode voltage of 1.2 V is required for XDPP1140
- Temperature sensing: NTC resistor is replaced by two diodes connected in series
- Board size: increase from standard quarter brick to 89 mm x 65 mm (3.5 in x 2.54 in) as a standalone unit, which includes all connectors, bulk capacitors, enable/disable switch, test points, I2C programming headers, etc.

1.1 Board specifications

The specifications for the EVAL_XDPP1140_FBFB_50V isolated DC-DC converter are given in Table 2 at T_a = 25°C, V_{OUT} = 50 V unless otherwise specified.

Table 2 Specifications

Parameter	Symbol	Values			Unit	Note/test condition
		Min.	Typ.	Max.		
Operating input voltage	V_{IN}	-36	-48	-60	V	–
Input current RMS value	$I_{in,RMS}$	–	16.4 21.9	–	A	V_{IN} = -48 V, P_{out} = 750 W V_{IN} = -36 V, P_{out} = 750 W
Start-up voltage threshold	$V_{IN(on)}$	-35	–	–	V	–
Minimum operating voltage after start-up	$V_{IN(off)}$	–	–	-34	V	–
Output voltage set-point	$V_{OUT,nom}$	25	50	55	V	Adjustable setpoint
Output current	I_{out}	–	–	15	A	–
Output power	P_{out}	–	–	750	W	v_{air} = 4 m/s
Efficiency	η	–	95.8	–	%	V_{IN} = -48 V, P_{out} = 750 W
Power dissipation	P_{diss}	–	32.4	37	W	V_{IN} = -48 V, P_{out} = 750 W
Output voltage ripple (peak-to-peak)	$V_{OUT,ac(pp)}$	–	130 300	200	mV	Continuous switching burst mode
Output voltage set-point tolerance	$\sigma V_{OUT,nom}$	-1	–	+1	%	–
Output voltage regulation (load)	$\Delta V_{OUT(load)}$	–	–	100	mV	V_{IN} = -48 V, 0-100% of $I_{out,max}$
Output voltage regulation (line)	$\Delta V_{OUT(line)}$	–	–	100	mV	V_{IN} = -60…-36 V, I_{out} = 15 A
Dynamic load response - Output voltage deviation - Settling time	 $\Delta V_{OUT(tr,load)}$ $t_{tr(load)}$	–	–	 ±500 80	 mV µs	 V_{IN} = -48 V, 25% to 75% of $I_{out,max}$ at 2 A/µs
Switching frequency	f_{sw}	–	140	–	kHz	–
Airflow velocity	v_{air}	–	800 4	–	LFM m/s	–
Operating temperature (ambient)	T_a	-40	–	+50	°C	–
Functional isolation voltage	V_{iso}	–	1500	–	V	–

1.2 Schematics

The main power schematic is shown in Figure 2, and the control, auxiliary circuit, and test points schematic is shown in Figure 3.

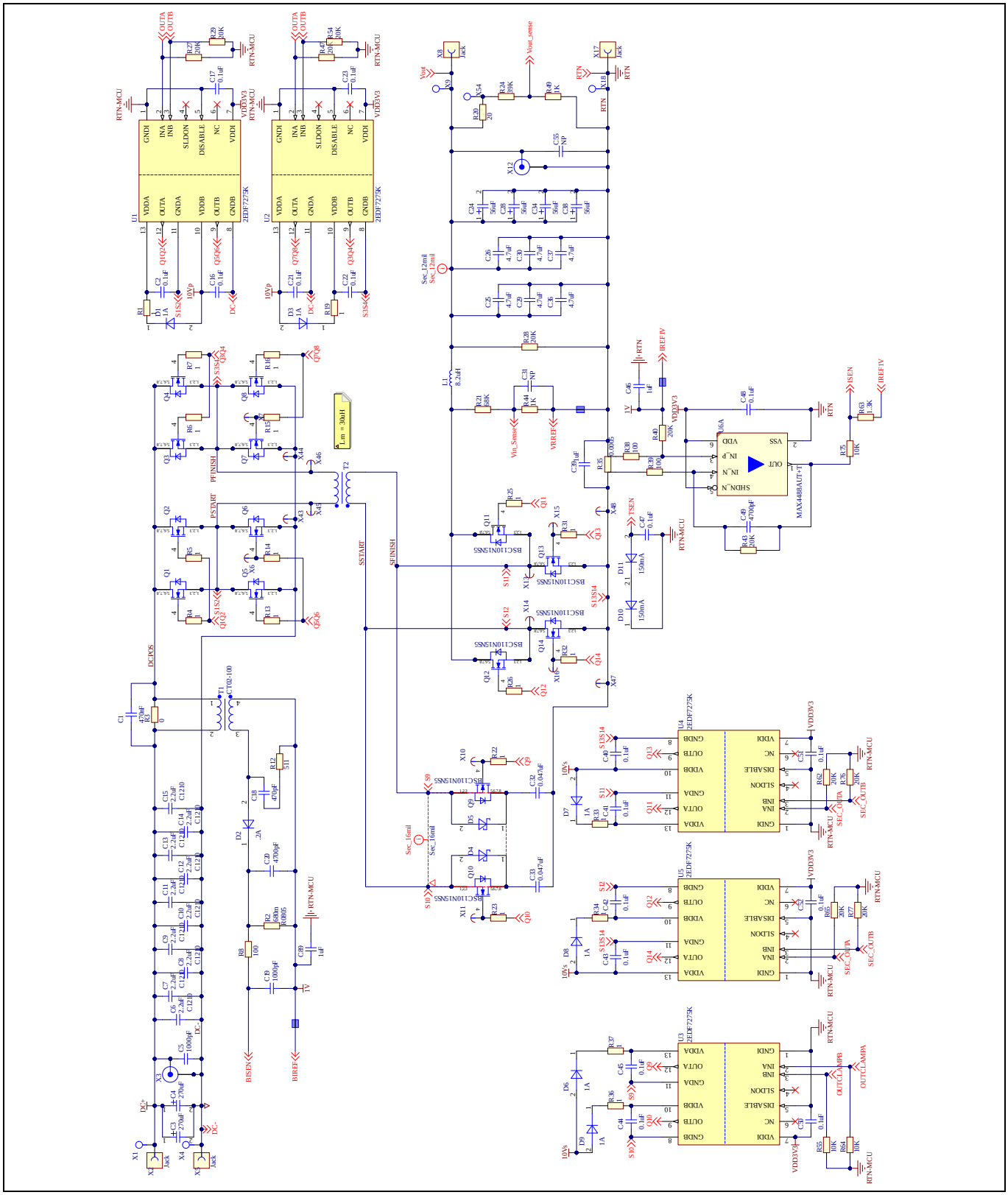


Figure 2 Main power schematic

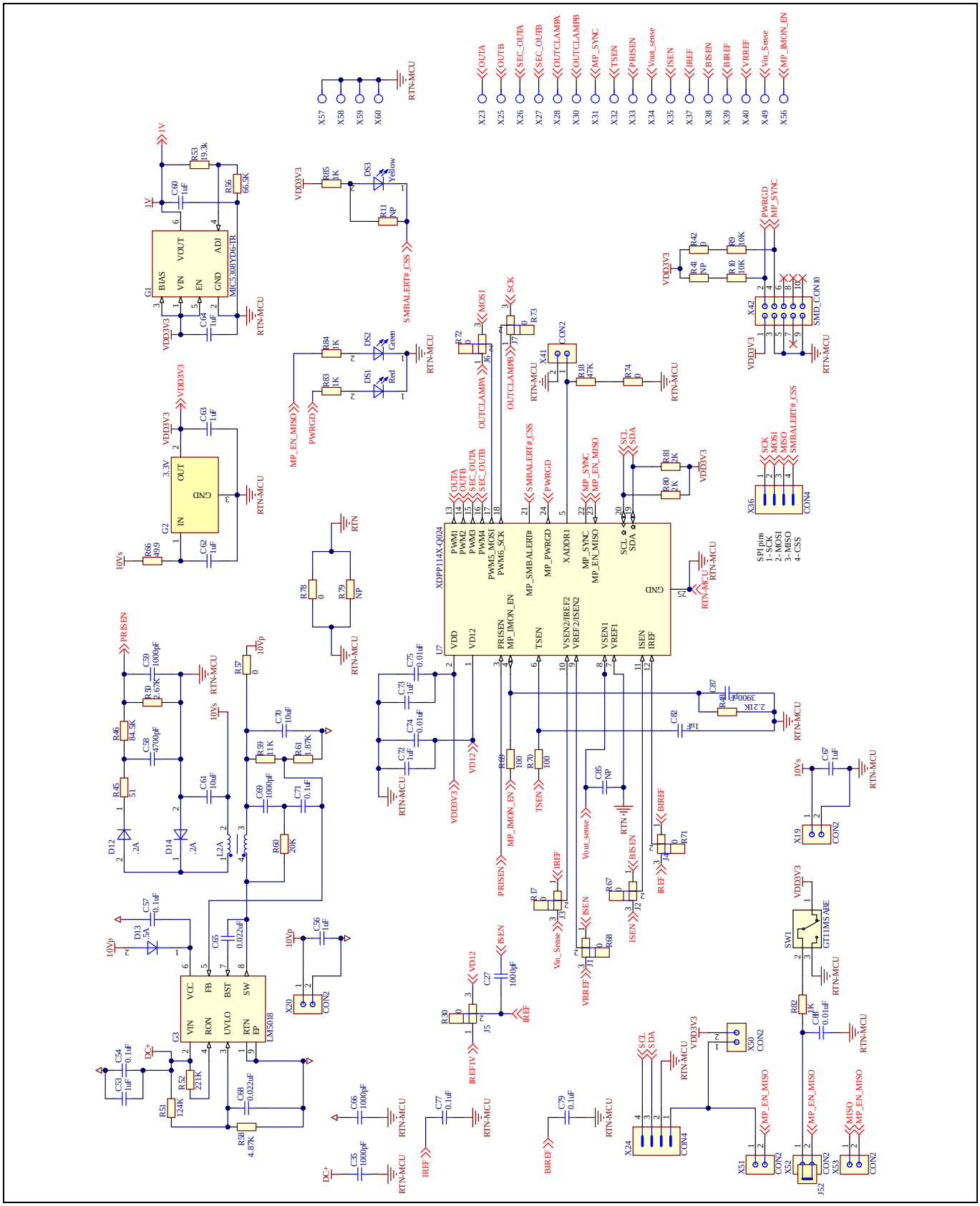


Figure 3 Control and auxiliary circuit schematic

2 XDPP1140 configuration

2.1 Topology and transformer turns ratio

Previously with XDPP1100, the PMBus command MFR_TRANSFORMER_SCALE (Ns:Np) is clamped to 0.999 maximum. As a result, the transformer turns ratio, n = Np:Ns is always greater than 1. This limits the application to a step-down style. For applications that need output voltage higher than the input voltage, a FW patch is required to correct the transformer turns ratio for input voltage telemetry and input feedforward. With the XDPP1140, step-up turns ratios are also allowed as the Ns:Np can be set up to 3.99994. Therefore, the configuration is straightforward, and no patch is necessary.

In this reference design, the turns ratio is 3:5. MFR_TRANSFORMER_SCALE is set to 1.667.

2.2 Input voltage sensing

There are two identical voltage sensing channels (VSEN1 and VSEN2) in XDPP1140, offering the flexibility of selecting either for input/output voltage sensing by configuring register **vsen_select**. While in XDPP1100, VSEN can only be used for output voltage sensing, and VRSEN is only for input voltage sensing.

VSEN and PRISEN are the two options for input voltage sensing. When using VSEN for input voltage sensing, XDPP1140 also supports direct sense and rectification voltage sense (VRS). Rectification voltage sense is used in isolated topologies, where the secondary side bridge rectifier switching node voltage (V_{RECT}) is measured, and with the PWM timing information, input voltage is calculated using the transformer turns ratio. PRISEN measures the input voltage through a secondary winding of the auxiliary power supply, using telemetry sense (TS) ADC. A brief comparison of these two sensing options is shown in Table 3. VSEN is faster, more accurate, but when rectification voltage is used, it only works when OPERATION is ON and MOSFETs are switching. When using VSEN, the register **vrs_voltage_init** needs to be set to an expected initial input voltage that is higher than VIN_ON. If input voltage telemetry is required in OFF state, PRISEN should be used. In this case, it is possible to use a FW patch to switch to VSEN after the converter turns on. VSEN also supports same cycle measurement. When enabled, the measurement result can be available before the current PWM falling edge, allowing faster feed forward response.

Table 3 VSEN vs. PRISEN

	ADC	Sample rate [MSps]	Resolution [mV]	Range [V]
VSEN1/VSEN2	11 bit	100	1.25	0 to 2.1
PRISEN (TS ADC)	10 bit	0.926 (shared with other channels)	2.344	0 to 2.4

In this design, VSEN is used for input voltage sense. From the schematic in Figure 2, the resistor divider R44 and R21 ratio is 0.01449. Correction terms such as resistive and SR diode voltage drops can also be configured, to account for differences in measured V_{RECT} voltage at different load current. The relevant registers and PMBus commands can be configured as shown in Table 4.

Table 4 Configuration for input voltage telemetry using VSEN

Register/PMBus command	Value	Comment
vsen_select	0	VSEN1= V_{OUT}, VSEN2=V_{IN} or V_{RECT}
tlm_vin_src_sel	0	VSEN selected by vsen_select
vsen_vrect_mode	0	V_{RECT} mode
vrs_cmp_wdt_thr	10	V_{RECT} comparator watchdog timeout threshold

Register/PMBus command	Value	Comment
vrs_cmp_ref_sel	0	VRS comparator threshold. Set to 500 mV
vsp_vrs_cnt_num_avg	0	Number of samples in VRS deadtime measurement. Set to 4
vrs_delta_vsum_sel	0	VRS ADC fast and slow low-pass filter output delta selection threshold. Set to 8-ADC codes
vrs_bypass_slow_lpf	0	VRS slow filter not bypassed
vrs_bypass_fast_lpf	0	VRS fast filter not bypassed
vrs_track_start_thr	22	V_{RECT} tracking start time threshold. Set to 220 ns
vrs_min_pw	0	Minimum V_{RECT} pulse width
vrs_same_cycle_en	0	Same cycle mode disabled
vrs_meas_start_thr	0	Not used (same cycle mode disabled)
vrect_div_2_sel	1	Bridge topologies
MFR_VRECT_SCALE	0.0143	Resistor divider ratio
MFR_TRANSFORMER_SCALE	1.667	Transformer turns ratio Ns:Np
vrs_voltage _init	59	Initial voltage for VSEN after sense resistor divider. Set to 1.18 V
tlm_vrect_rcorr	14	Resistive correction term. Set to 54 mΩ
tlm_vrect_voffset	0	Voltage offset correction
tlm_vrect_sr_diode	0	Voltage correction term when SR FETs are off. Set to 480 mV

The option to use PRISEN is also available in this design. As shown in Figure 3, the secondary winding of the auxiliary supply is connected to PRISEN pin of XDPP1140 through resistor divider R46 and R50. Telemetry is computed using linear estimation configured by two register values: **vin_pwl_slope** and **vin_trim** as V_{IN} = ADC × vin_pwl_slope + vin_trim. Since the resistor divider ratio is 2.67 / (84.5 + 2.67) = 0.03063, **vin_pwl_slope** can be calculated as:

$$\text{vin\_pwl\_slope} = \frac{2.4 \times 2^4}{scale} = \frac{38.4}{0.03063} = 1253$$

Equation 1

To get accurate telemetry, further tuning is usually needed. In addition, PRISEN voltage tends to have load dependency of the auxiliary supply. That means, the settings of these two registers will be different depending on whether the operation is on or off. If desired, it is possible to use a FW patch to automatically apply the correct set of register values to get the most accurate telemetry using PRISEN. The example configuration for PRISEN is listed in Table 5.

Table 5 Configuration for input voltage telemetry using PRISEN

Register	Value	Comment
tlm_vin_src_sel	2	PRISEN
vin_pwl_slope	1263	When operation is off
vin_trim	29	When operation is off
vin_pwl_slope	1290	When operation is on
vin_trim	5	When operation is on

2.3 Feed-forward

The voltage mode control (VMC) generally has a slower input transient response compared to the current mode control. Feed-forward is a technique for the VMC that greatly improves line transient responses. It works by computing the ideal duty cycle based on input and output voltages, and then add the PID output together for pulse width modulation (PWM) module. Its effectiveness depends on the input voltage sensing accuracy and speed. On the other hand, in the actual implementation, digital resolution, quantization, and algorithmic errors could adversely affect the output voltage ripple. The XDPP1140 incorporates a new method in the feed-forward hardware implementation that improves the computation resolution and reduces output voltage ripple. In addition, a configurable dead band is added when computing the feed forward term. If the difference between consecutive samples is smaller than the dead band, the feed forward will continue to use previous value of V_{IN}. The dead band could reduce jittering that caused by switching noise in the voltage sensing path.

The block diagram of the feed forward of XDPP1140 is shown in Figure 4.

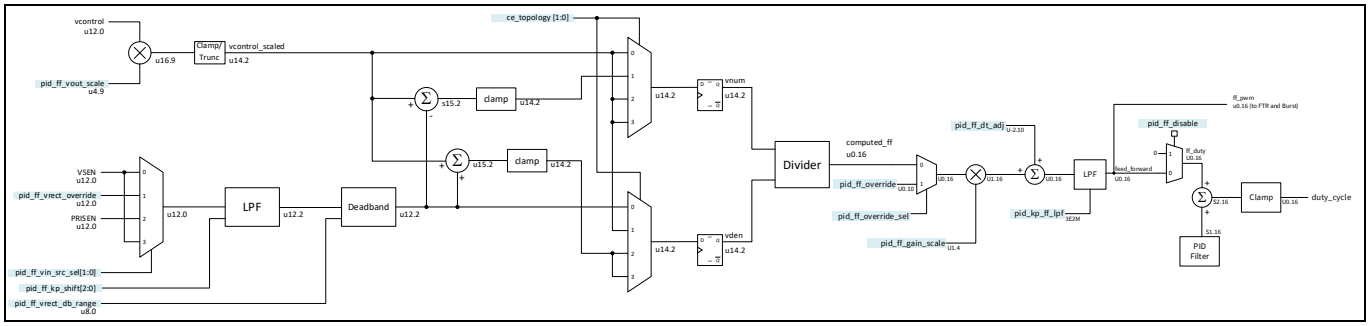


Figure 4 Feed-forward block diagram

The registers that are highlighted in light blue are accessible.

The **pid_ff_vin_src_sel** is similar to the pid0_ff_vrect_sel in the XDPP1100. It defines the input voltage source for feedforward. There are two options for input voltage sensing: VSEN and PRISEN, and the configuration is independent of telemetry. This allows different input voltage sensing methods for telemetry and feed-forward. Since sample rate and resolution of input voltage in feed-forward will directly affect the output voltage ripple, VSEN is selected in this design. If needed, same-cycle V_{RECT} update can be enabled to achieve even faster response (**vrs_same_cycle_en**).

The **pid_ff_kp_shift** is a low pass filter applies to the PID FF input voltage sense. It could config the filter bandwidth from 63 kHz to 7958 kHz or can be bypassed for faster response.

The **pid_vrect_db_range** sets the dead band to the input voltage sensing portion to ignore noise. Resolution is 1.25 mV at the sense pin. A setting of '0' disables the dead band feature.

The **pid_ff_disable** is used to enable or disable the feedforward. When disabled, the FF output is forced to '0' for the loop compensation. However, the feedforward duty cycle is still computed for the fast transient response (FTR) and burst mode even with the feedforward disabled. This is necessary when the PID accumulator is frozen in the FTR and burst mode. This register should not be changed while converter is in regulation.

The **pid_ff_gain_scale** is used to apply a gain between 0 to 1.9375 to the computed FF term with resolution 0.0625. The typical setting is 16 that corresponds to a gain of 1.0.

The **pid_ff_dt_adj** is used to adjust PID FF duty-cycle to compensate PWM dead-time.

The **pid_kp_ff_lpf** is PID FF low pass filter coefficient. The computed FF term is passed through a low pass filter before being used by the PID as part of the duty cycle calculation. This parameter sets the bandwidth of this filter. A setting of '0' bypasses the filter. The actual bandwidth can be computed from the filter coefficient as follows. The exponent and mantissa are taken form the corresponding bits of the register.

$$exp = \text{pid\_kp\_ff\_lpf[4:2]}, man = \text{pid\_kp\_ff\_lpf[1:0]}$$

$$kfp = \begin{cases} man \times 2^{-10}, & exp = 0 \\ (4 + man) \times 2^{exp-1} \times 2^{-10}, & exp > 0 \end{cases}$$

$$BW = \frac{kfp}{1 - kfp} \times \frac{50}{2\pi} \text{ [MHz]}$$

Equation 2

For example, for **pid_kp_ff_lpf** = 12, exp = 3, man = 0.

$$kfp = 4 \times 2^{3-1} \times 2^{-10} = 0.015625$$

$$BW = \frac{0.015625}{1 - 0.015625} \times \frac{50}{2\pi} = 0.126 \text{ [MHz]}$$

Equation 3

The **pid_ff_vout_scale** is conversion factor of output voltage scaling for use in the feed-forward function. This parameter is computed automatically by the built-in FW and requires no manual computation. However, after changing **pid_ff_vin_src_sel** config in RAM, it is required to re-write PMBus command VOUT_SCALE_LOOP for FW to refresh the **pid_ff_vout_scale** value. This is common during board evaluation that different input voltage sources are verified for FF.

The following registers and PMBus commands are configured.

Table 6 Configuration for feed-forward

Register	Value	Comment
pid_ff_vin_src_sel	0	VSEN selected by vsen_select (see Table 4)
pid_ff_disable	0	FF enabled
pid_ff_dt_adj	0	FF adjustment for dead-time
pid_ff_kp_shift	1	FF V_{RECT} low pass filter bandwidth. Set to 7958 kHz
pid_ff_gain_scale	16	FF gain is 1.0
pid_kp_ff_lpf	12	FF low pass filter coefficient. Set to 126 kHz
pid_vrect_db_range	2	2.5 mV dead band applied to V_{RECT}
vrs_same_cycle_en	0	Same cycle mode disabled
ce0_topology	0	FB topology

2.4 Output current sensing

The XDPP1140 requires a common-mode voltage at ISEN and IREF pins, typically 1.2 V. There is only one gain mode. The LSB of current sense ADC is 1 mV, and therefore the calculation of MFR_IOUT_APC is changed to:

$$\text{MFR\_IOUT\_APC} = 1\ \text{mV}/R_{sense,\text{eq}}$$

Equation 4

In this design, current sense resistor is 0.5 mΩ; the amplifier gain is 200; and the resistor divider is 10 kΩ and 1.3 kΩ. Rsense,eq can be calculated as:

$$R_{sense,\text{eq}} = 0.5\ \text{m}\Omega \times 200 \times {}^{1.3}/_{(10+1.3)} = 11.5\ \text{m}\Omega$$

Equation 5

The offset can be adjusted using PMBus command IOUT_CAL_OFFSET. In addition, a new register **isp0_offset_range** is added, allowing user to change the zero-code location of the current sense ADC. This is useful when asymmetric ADC range is needed.

Due to heavy filtering, even though the sense resistor is in the path of inductor current, the signal at ISEN pin is DC. Therefore, no current estimator is used, as shown in Table 7.

Table 7 Configuration for output current sensing

Register/PMBus command	Value	Comment
MFR_IOUT_APC	0.09131	Corrected based on measurement
IOUT_CAL_OFFSET	0	-
isp0_offset_range	0	No offset, symmetric ADC
ce0_ktrack_off	5	1.00, no estimation
ce0_ktrack_on	5	1.00, no estimation

2.5 Burst mode

The XDPP1140 offers two methods for improving light load efficiency: diode emulation (DE) mode and burst mode. One of these two methods can be selected, and automatically activated by FW when the output current is below a certain threshold. DE mode turns off SR switches, therefore, emulating the diode behavior. Burst mode turns off all switches when output voltage reaches regulation and turns only primary switches back on for a few pulses when the output voltage drops below an error threshold. The SR switches remain off in burst mode in FB-FB topology.

Bench testing shows that burst mode is more effective. Therefore, it will be the focus of this application note. Figure 5 shows some key waveforms for burst mode operation.

First of all, burst mode is enabled by setting PMBus command POWER_MODE = 0x08. After entering burst mode, there are burst OFF and burst ON time intervals.

When entering burst mode, the controller turns off PWM, waiting for the output voltage to drop to threshold **pid_burst_mode_err_thr** and starts burst ON.

The burst ON interval starts when output voltage error is larger than **pid_burst_mode_err_thr**. This error voltage is defined as (V_{target} – V_{sense}). The V_{target} is converter target regulated output voltage scaled per VOUT_SCALE_LOOP by output resistor divider. The V_{sense} is the instantaneous voltage sensed at VSEN pin. Only primary PWM turns on during burst ON interval. The duty cycle is determined by feed-forward duty cycle, regardless of the status of **pid_ff_disable**. The number of burst pulses is defined by **pid_burst_reps**.

The burst entry and exit conditions are defined as follows:

Entry condition:

- Output current is lower than threshold defined by **pid_burst_mode_ith**; and
- Enough time has passed before last burst exit defined by **burst_mode_holdoff_time** (can be disabled by setting to 0).

Exit conditions:

- Output current is above threshold defined by **burst_exit_ithr** and enabled by **burst_exit_ithr_en**; or
- Burst OFF interval is below half of the switching cycle; or
- Output voltage error is above FTR threshold **pid_verr_entry_thrs** (can be disabled by setting to 0). This feature should be disabled for full-bridge topology due to errata bug #9. For more details, see the errata sheet.

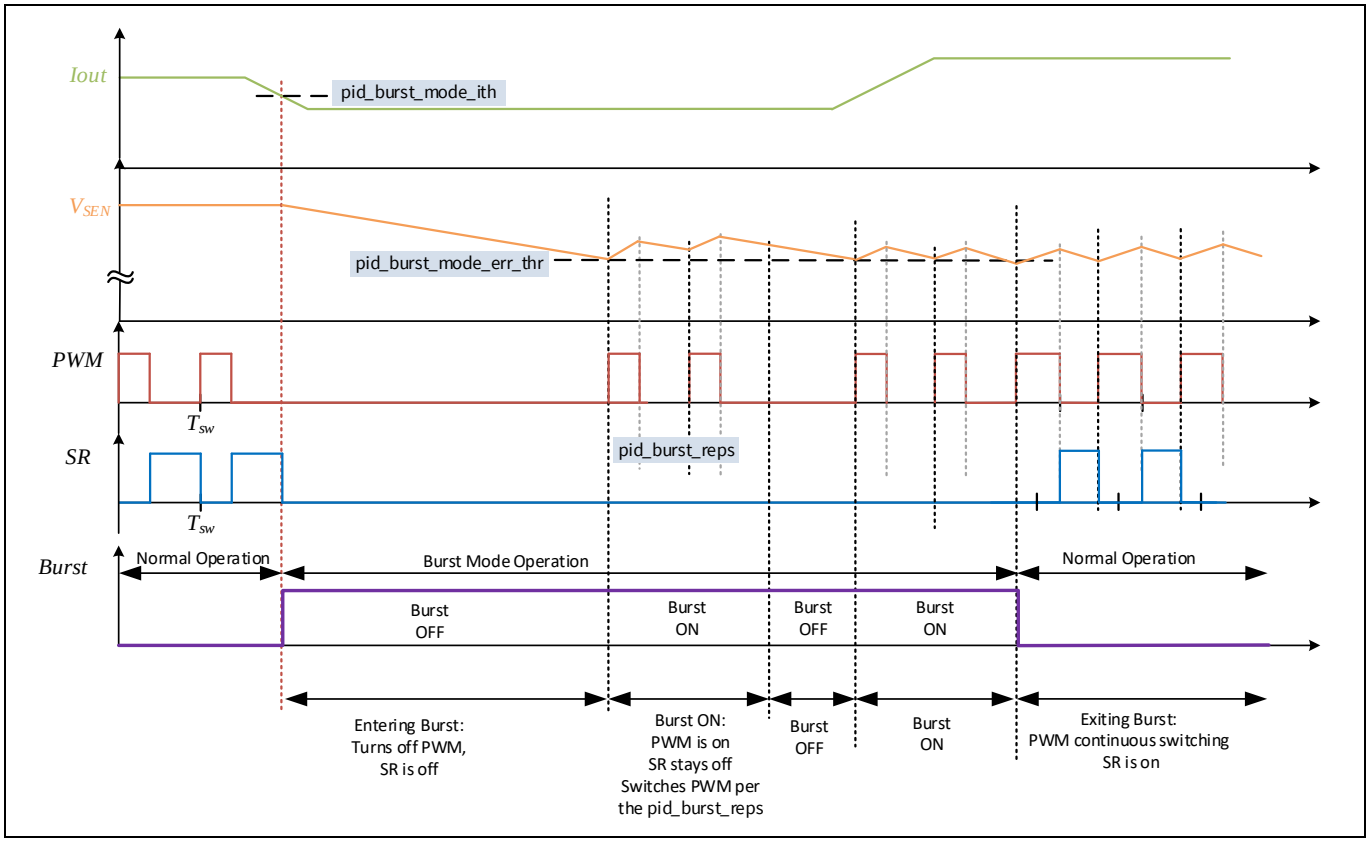


Figure 5 Example waveforms in burst mode

Under very light load, output voltage drops very slowly and the burst OFF time can be extended. As a result, the bootstrap capacitor for the gate driver could be over discharged. In this case, the first few pulses will charge the bootstrap capacitor, and high-side MOSFETs will stay off. The XDPP1140 introduces a mechanism to automatically increase the number of burst pulses based on the previous burst OFF time. For every interval

defined by **burst_rep_inc_time**, the number of burst pulses is increased by 1. The maximum increase of the number of pulses is defined by **burst_rep_inc_max**.

Due to the nature of pulsating current and long OFF time, the burst mode can affect the current telemetry. A different low pass filter, usually lower bandwidth compared to normal operation, can be used to improve the current telemetry, set by **tlm_kfp_iout_burst**.

Typical steps to configure burst mode:

1. Determine maximum output voltage error Verr in burst mode, ripple and load current threshold for burst mode entry. The valley of output voltage ripple is set by register **pid_burst_mode_err_thr**, and the peak of output voltage ripple is determined by **pid_burst_reps**. For example, if the allowed minimum output voltage is 49.5 V, then the error voltage Verr is 0.5 V.

$$\text{pid\_burst\_mode\_err\_thr} = V_{err} \times \text{VOUT\_SCALE\_LOOP}/1.25\,\text{mV}$$
$$= 0.5\,\text{V} \times 0.025/1.25\,\text{mV} = 10$$

Equation 6

2. Determine peak output voltage in burst mode. This is set by **pid_burst_reps**. For each burst pulse, output voltage rises by a fixed amount △Vo. This rise can be estimated by using total output capacitance Co, inductor Lo, transformer turns ratio Ns/Np, duty cycle D, switching frequency fs, input voltage V_{IN} and output voltage V_{OUT}. For example, considering 48 V input and 50 V output, Ns/Np of 1.667, D of 0.625, fs of 140 kHz, 250 µF for Co and 8.2 µH for Lo, the contribution to △Vo from each burst pulse can be estimated as:

$$\Delta V_o \approx 2 \times \frac{1}{C_o}\int i_{C_o}\mathrm{dt} = 2 \times \frac{1}{C_o} \times \frac{1}{2}\, i_{L_o,\mathrm{pk}} T_s = \frac{D\left(V_{in}\frac{N_S}{N_p} - V_o\right)}{C_o L_o f_s^2} = 0.47\,\text{V}$$

Equation 7

This rough estimation assumes 0 A load current and small output voltage ripple. The factor of 2 comes from the full-bridge configuration. Typically, a small value for **pid_burst_reps** yields good results. Too large value could cause too much energy being delivered to the output capacitors, resulting in over-voltage conditions. For this design, **pid_burst_reps** is set to 2 (3 burst cycles).

3. Configure the load current threshold for burst mode: entry threshold using register **pid_burst_mode_ith** and exit threshold using **burst_exit_ithr**. It is recommended to have some hysteresis between entry and exit thresholds. In this design, entry is set to 2 A and exit is 2.5 A.
4. Configure the auto increase of burst cycles. Depending on the gate driver and MOSFET selections, this can be estimated or determined from waveform measurement. Typically, if **pid_burst_reps** is very low, for example, 0 or 1, enabling auto increase can help improve performance. In this design, however, this feature is disabled.
5. Determine if burst hold off is required. In some applications, it may be desirable to prevent entering burst for a period after exiting. This is set by register **burst_mode_holdoff_time**.

Table 8 Configuration for burst mode

Register/PMBus command	Value	Comment
POWER_MODE	0x08	Maximum efficiency; burst mode
pid_burst_mode_err_thr	10	Error voltage at VSEN. Set to 12.5 mV
pid_burst_mode_ith	16	Burst mode entry current threshold. Set to 2 A
pid_burst_reps	2	Number of cycles in each burst. Set to 3
burst_rep_inc_time	0	Disable auto increase of burst cycles
burst_rep_inc_max	0	Disable auto increase of burst cycles
burst_mode_holdoff_time	0	No hold off time between burst exit and entry
burst_exit_ithr_en	1	Enable burst exit based on current threshold
burst_exit_ithr	5	Burst mode exit current threshold. Set to 2.5 A
pid_verr_entry_thrs	0	Disable burst exit based on FTR threshold
tlm_kfp_iout_burst	16	Burst mode current telemetry low pass filter

3 Experimental verification

An image of the test setup is shown Figure 6.

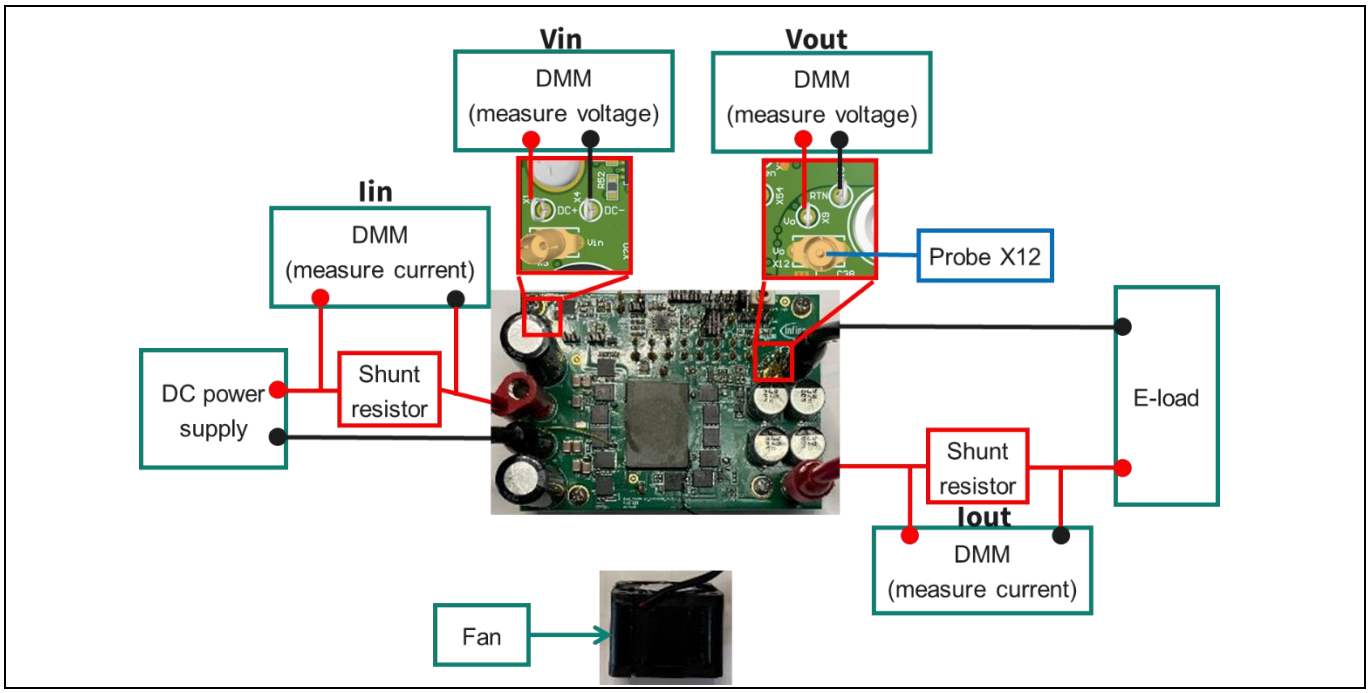


Figure 6 Test setup diagram: the reference design, power supply, load, and measurement connections

Necessary connections to operate the board:

- Connect the main power supply (-36 V to -60 V DC) to input connectors X2 (DC+) and X5 (DC-) with banana plugs
- Connect the electronic load to output connectors X8 (V_{OUT}) and X17 (RTN) with banana plugs
- A fan placed about 1cm from the bottom edge of the board supplying about 3 m/s airflow
- Enable switch in the 'ON' position, as shown in Figure 7.

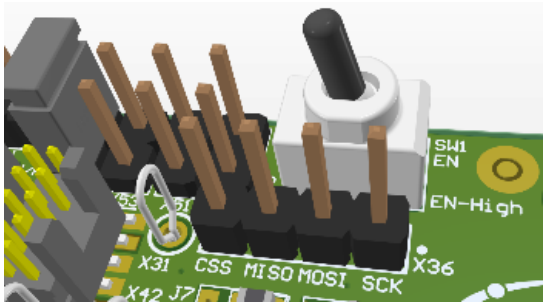


Figure 7 Enable switch located on the top edge of the board in 'ON' position

Optional connections for measurement:

- Input voltage measurement DMM to X1(DC+) and X4(DC-)
- Output voltage measurement DMM to X9(Vo) and X18(RTN)
- Input and output current measurement using shut resistors

- Oscilloscope probe to test point jack **X12** for output voltage ripple measurement.

3.1 Operation waveforms

3.1.1 Steady-state operation

Continuous switching waveforms for different operation conditions are shown in Figure 8.

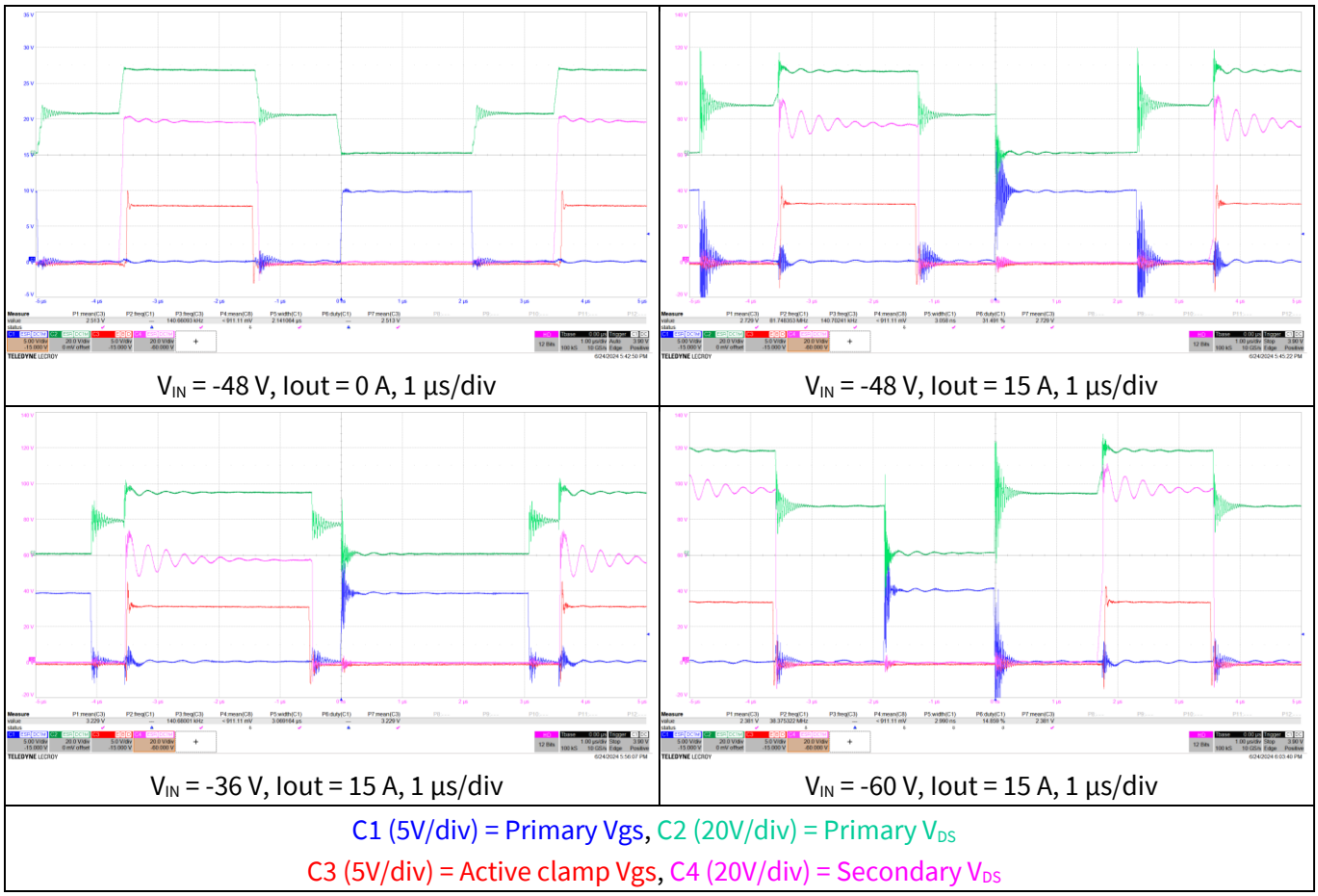
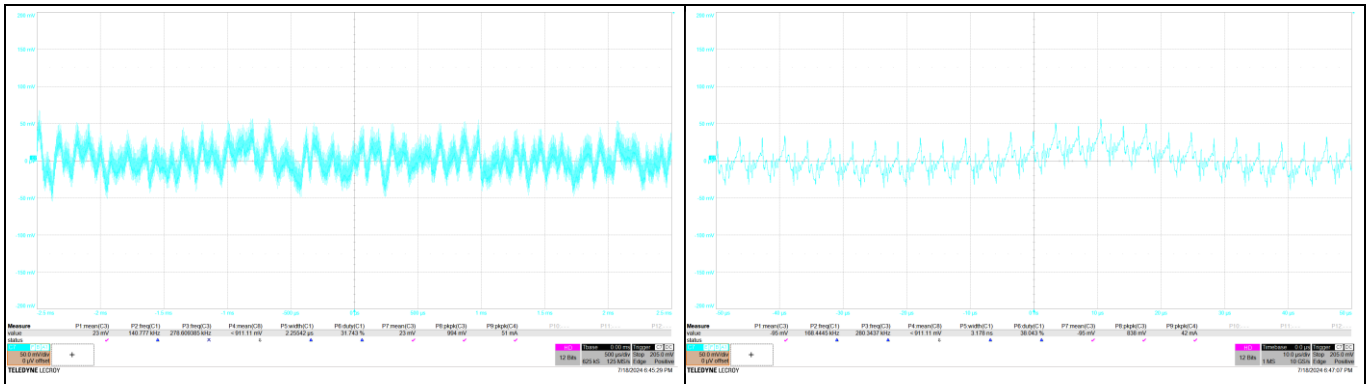


Figure 8 Stead-state switching waveforms

3.1.2 Output voltage ripple

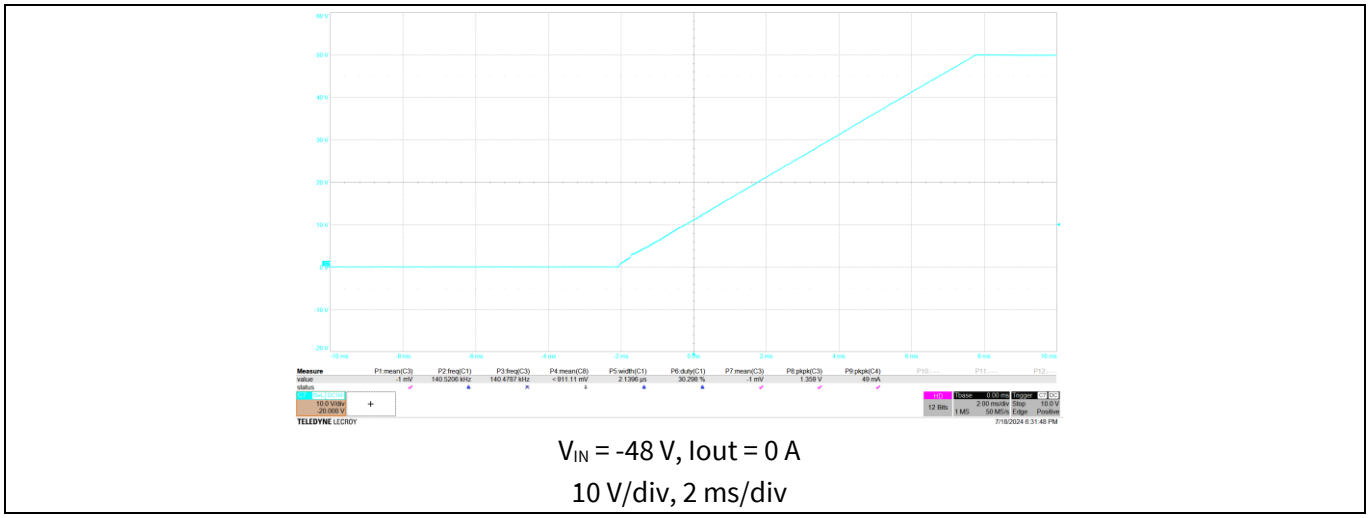


V_{IN} = -48 V, V_{OUT} = 50 V, Iout = 15 A
50 mV/div, 500 µs/div

V_{IN} = -48 V, V_{OUT} = 50 V, Iout = 15 A
50 mV/div, 10 µs/div

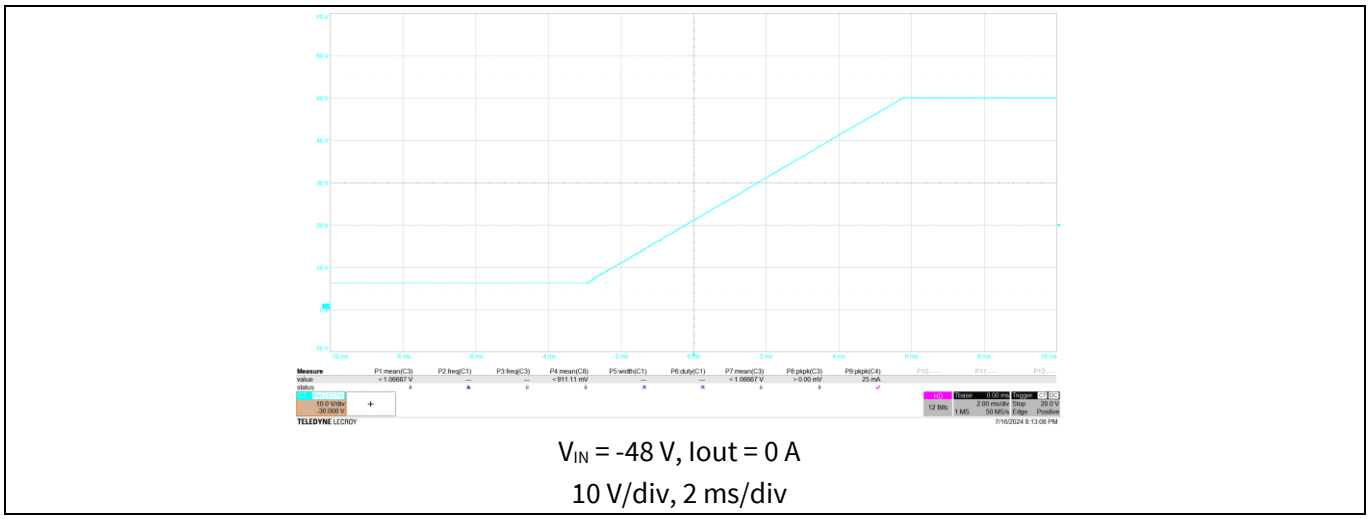
Figure 9 Output voltage ripple

3.1.3 Start up



V_{IN} = -48 V, Iout = 0 A
10 V/div, 2 ms/div

Figure 10 Start up waveform from 0 V_{OUT}



V_{IN} = -48 V, Iout = 0 A
10 V/div, 2 ms/div

Figure 11 Start up with pre-bias of 7 V

3.1.4 Burst mode

From the configurations in Section 2.5, the output voltage error in burst mode is set to 0.5 V, and burst cycles is set to 3. Figure 12 shows the output voltage and one primary PWM waveforms for two different load conditions: 0.2 A and 0.5 A. As expected, the minimum V_{OUT} is 49.5 V. The output voltage ripple is around 0.4 V.

To demonstrate the effect of burst cycles on output voltage ripple, similar waveforms are measured at 0.5 A output, with burst cycles set to 2 and 5, as shown in Figure 13. A small burst cycle results in less voltage ripple, while a large burst cycle could cause output to exceed regulation voltage, especially at very light-load conditions (0 A, for example).

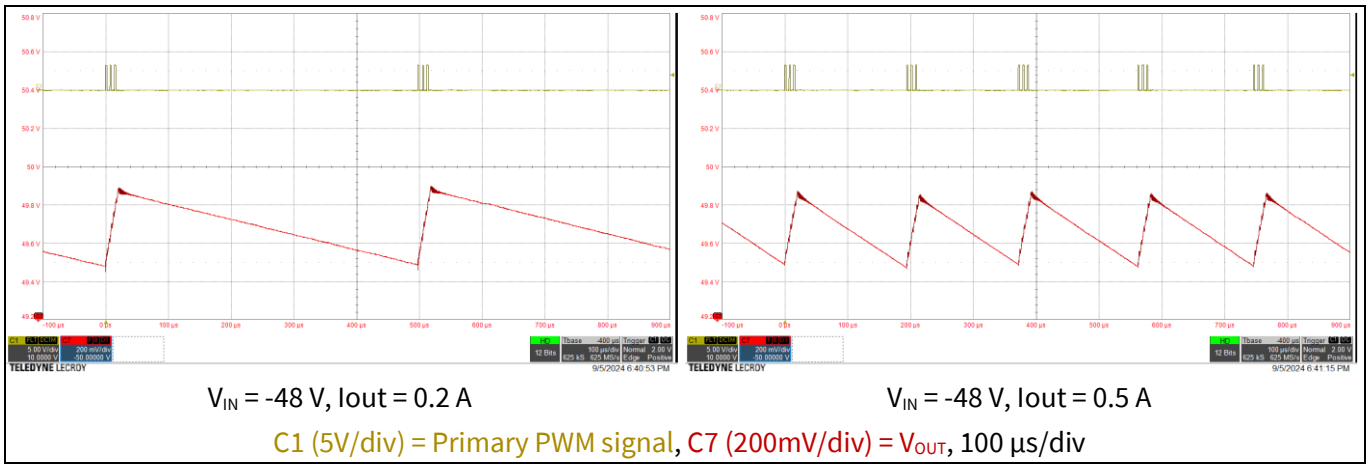


Figure 12 Burst mode waveform at light load

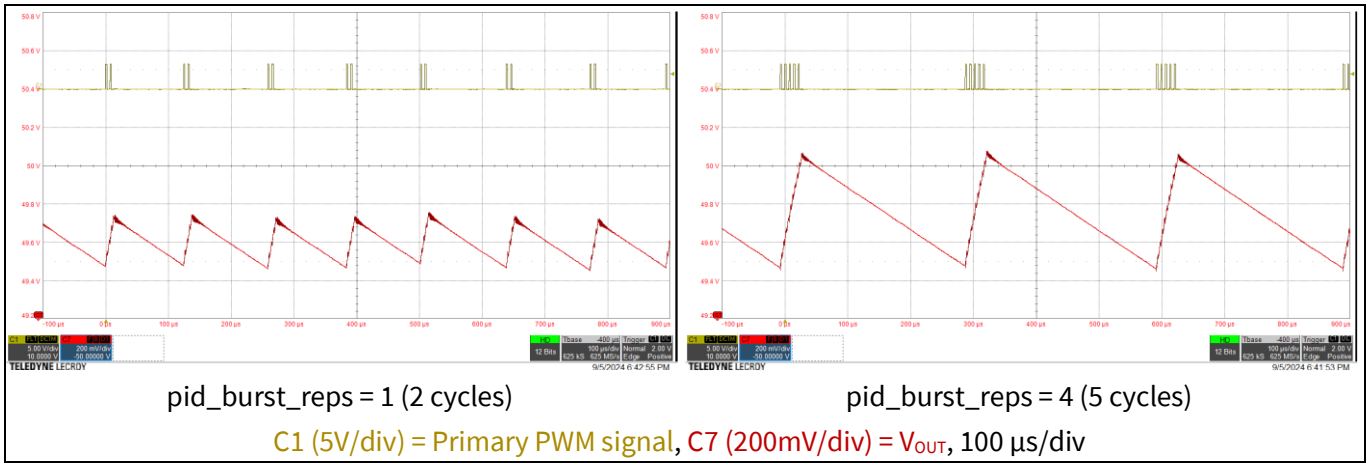
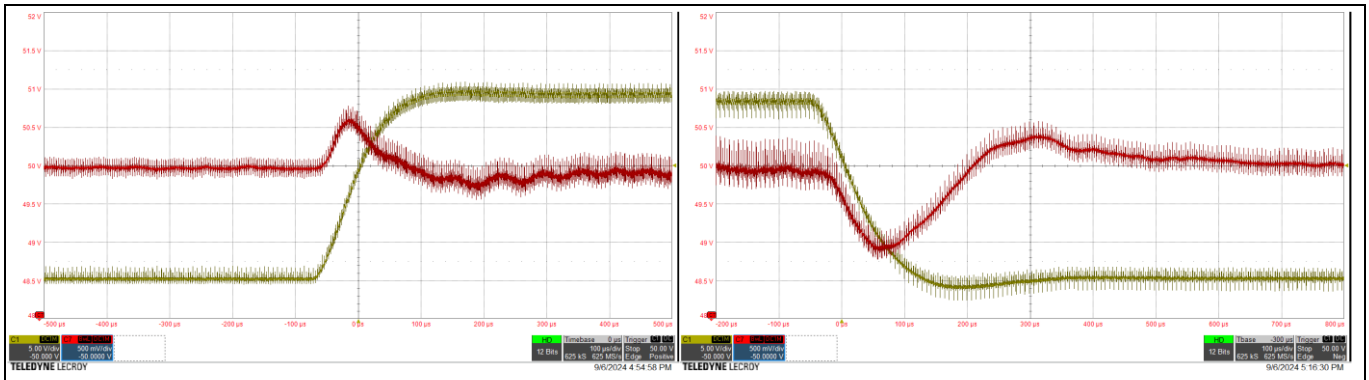


Figure 13 Burst mode waveform at 0.5 A output current

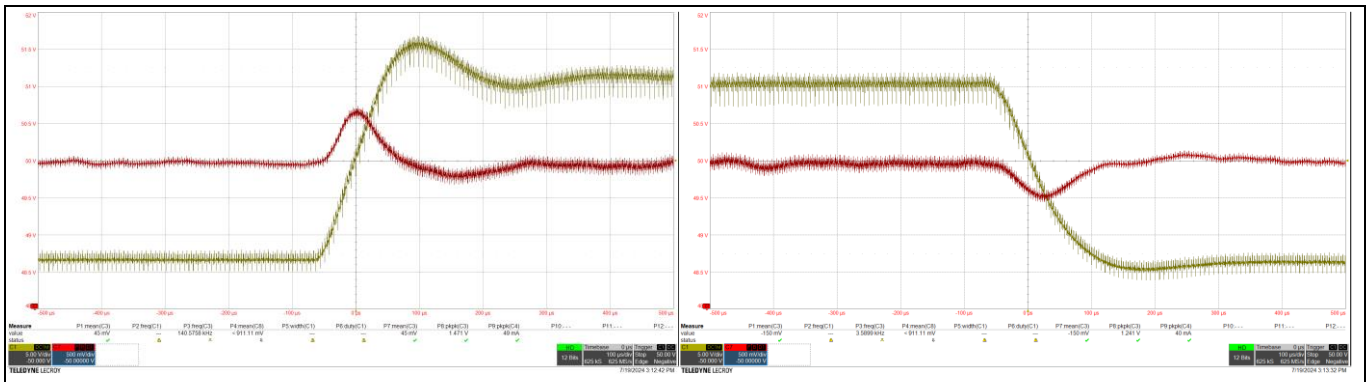
3.1.5 Line transients

The input voltages for line transients are -36 V/-60 V, with slew rate of 0.25 V/µs, at maximum load current 15 A. Negative voltages are measured as positive with the oscilloscope to avoid grounding complications. The waveforms using PRISEN and VSEN are shown in Figure 14 and Figure 15, respectively. For high to low line transient, the peak output voltage error using VSEN is about half of that using PRISEN. If same cycle response is enabled by setting **vrs_same_cycle_en** to 1, even smaller error is achieved in Figure 16.



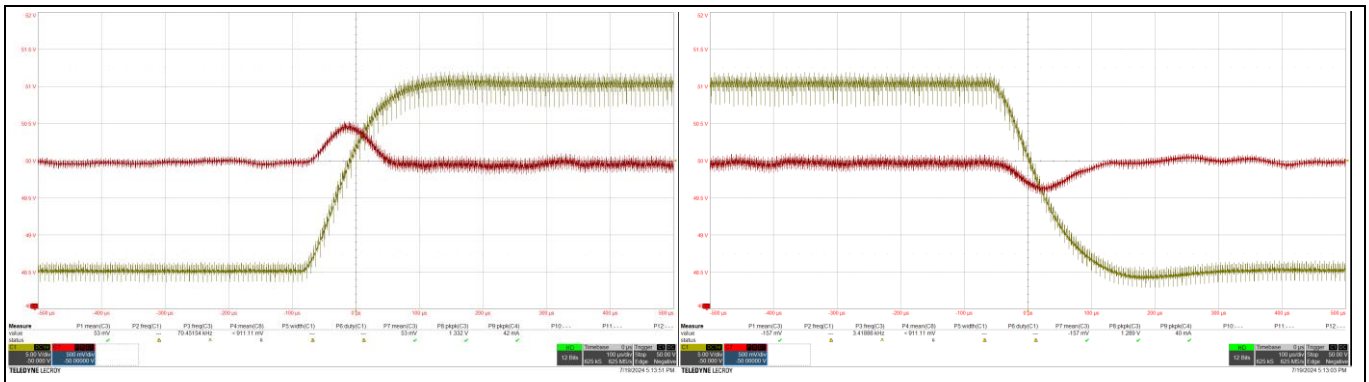
V_{IN} = -36 V / -60 V / -36 V, dV_{IN}/dt = 0.25 V/µs, Iout = 15 A
C1 (5 V/div) = Input voltage
C7 (500 mV/div) = Output voltage

Figure 14 Line transient waveform using PRISEN



V_{IN} = -36 V / -60 V / -36 V, dV_{IN}/dt = 0.25 V/µs, Iout = 15 A
C1 (5 V/div) = Input voltage
C7 (500 mV/div) = Output voltage

Figure 15 Line transient waveform using VSEN

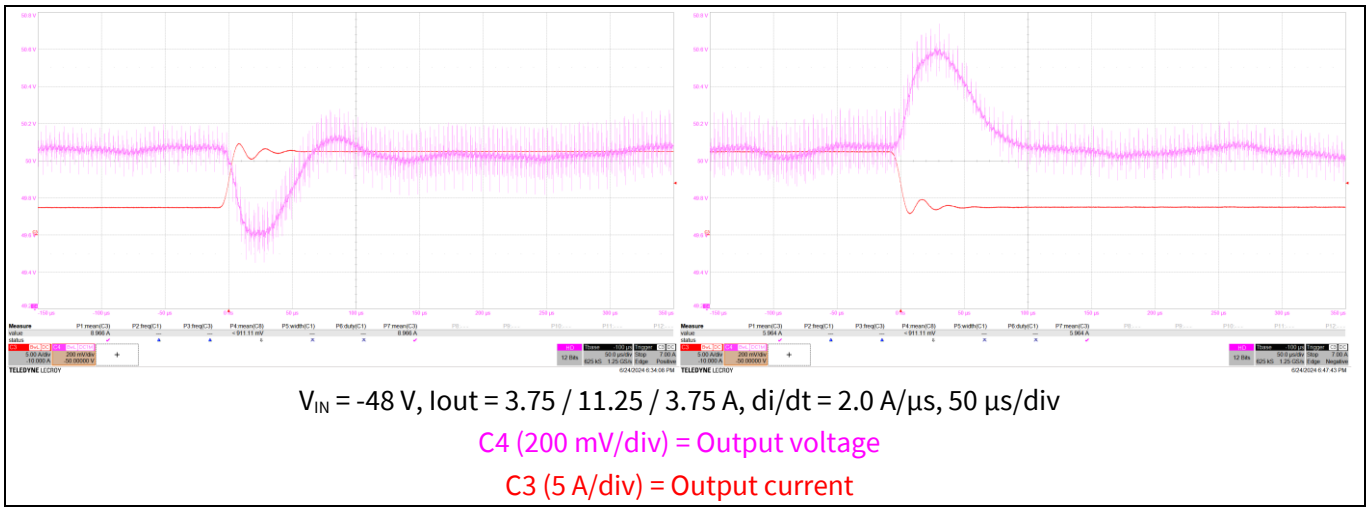


V_{IN} = -36 V / -60 V / -36 V, dV_{IN}/dt = 0.25 V/µs, Iout = 15 A, 100 µs/div
C1 (5 V/div) = Input voltage
C7 (500 mV/div) = Output voltage

Figure 16 Line transient waveform using VSEN with same cycle enabled

3.1.6 Load transients

Input voltage is fixed at -48 V, and output voltage is set to 50 V. The load current is programmed to step between 25% and 75% fullload, corresponding to 3.75 A and 11.25 A. Current slew rate is 2 A/µs. The output voltage and output current waveforms are shown in Figure 17.



V_{IN} = -48 V, Iout = 3.75 / 11.25 / 3.75 A, di/dt = 2.0 A/µs, 50 µs/div
C4 (200 mV/div) = Output voltage
C3 (5 A/div) = Output current

Figure 17 Load transient waveforms

3.2 Efficiency

In normal operating mode (continues switching), efficiencies are captured at about 4 m/s (800 LFM) air flow, and with a dwell time of 5 minutes. The results are given in Table 9 and Figure 18. With burst mode enabled, the loss reduction is shown in Figure 19.

Table 9 Measured efficiency at 50 V output voltage

Output current (A)	-36 V input	-48 V input	-60 V input
1	88.74%	83.50%	79.79%
2	93.48%	90.51%	88.54%
3	95.27%	92.69%	91.32%
4	96.00%	93.51%	91.54%
5	96.50%	94.14%	92.39%
6	96.77%	94.72%	93.16%
7	96.89%	95.19%	93.70%
8	96.92%	95.30%	94.10%
9	96.86%	95.48%	94.39%
10	96.84%	95.60%	94.57%
11	96.76%	95.63%	94.68%
12	96.65%	95.97%	94.74%
13	96.53%	95.94%	94.74%
14	96.39%	95.88%	94.69%
15	96.19%	95.85%	94.66%

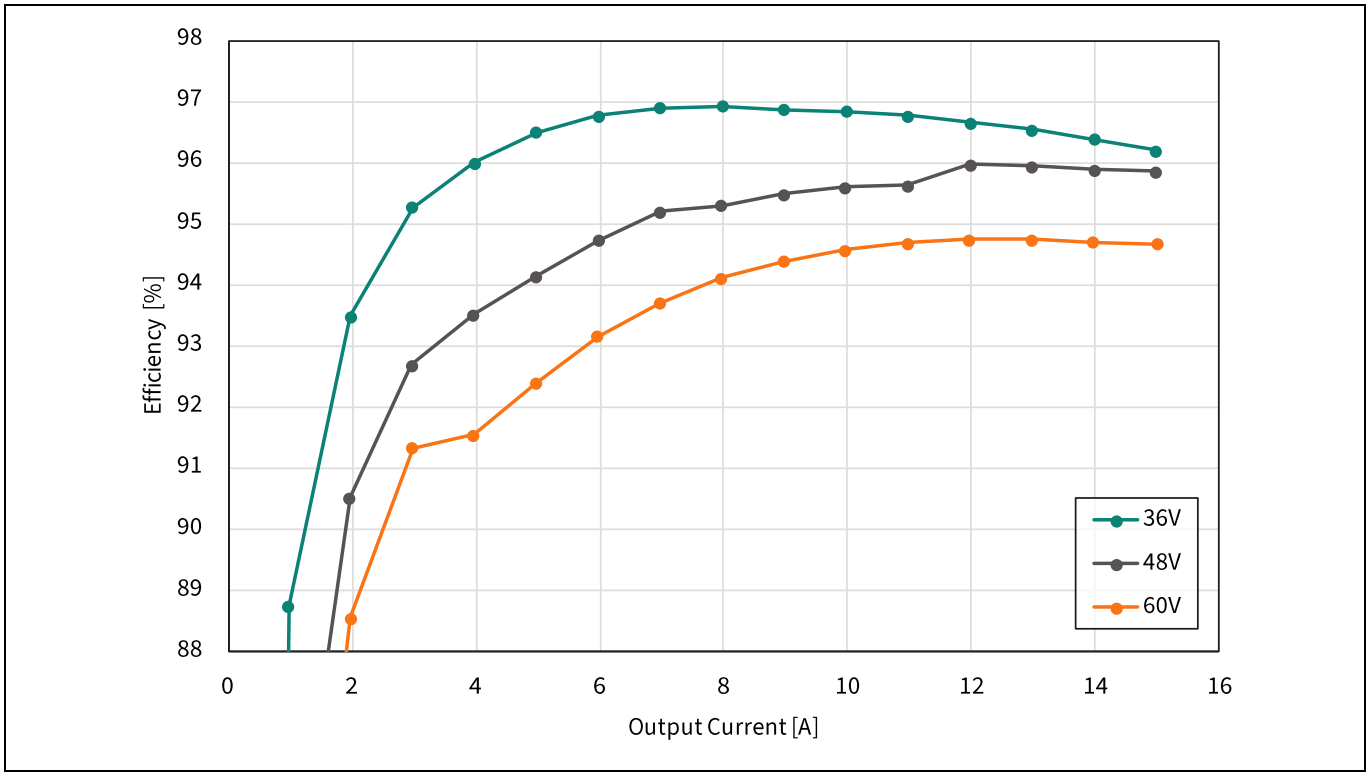


Figure 18 Measured efficiency at 50 V output voltage for different input voltages across load range

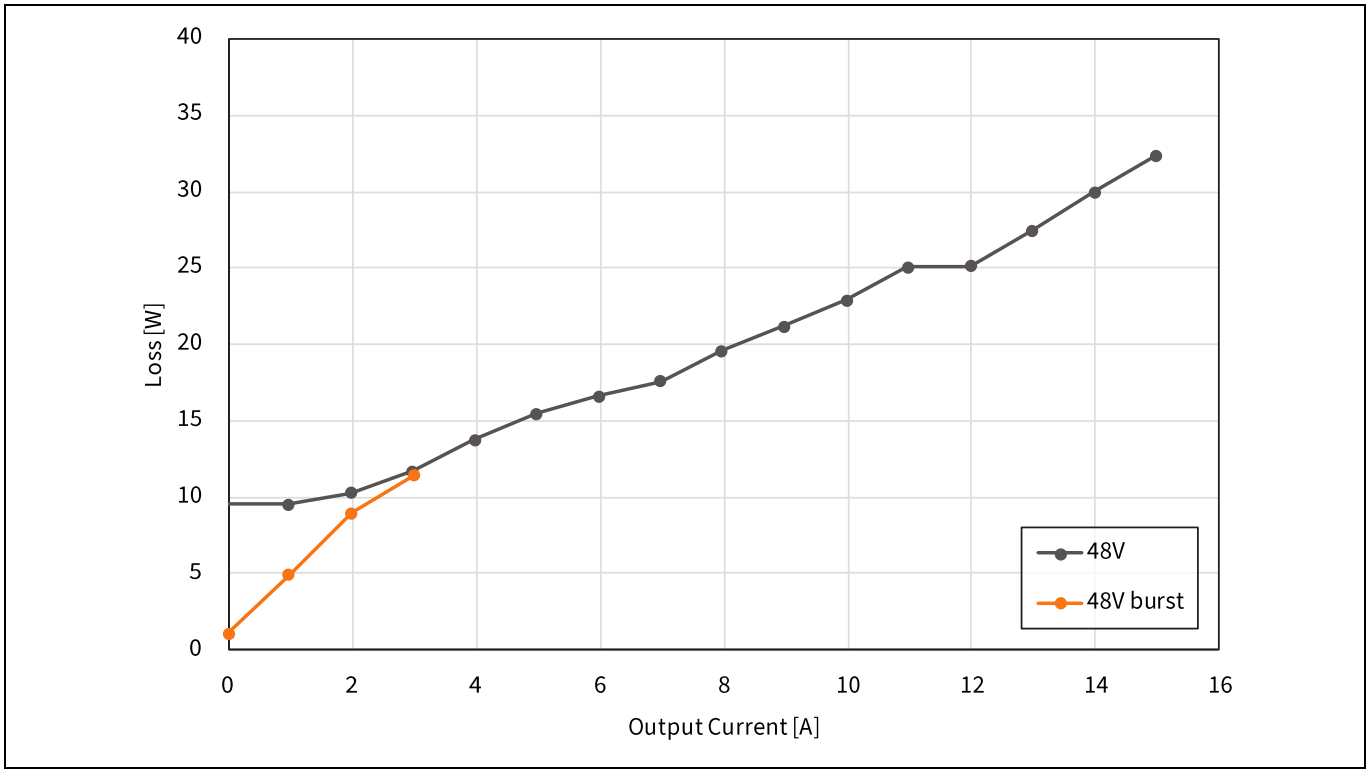


Figure 19 Light-load improvement using burst mode

3.3 Thermal performance

Thermal images are recorded using a FLIR A700, while regulating V_{OUT} = 50 V with 15 A output current, at three different input voltages. The airflow is about 4 m/s (800 LFM).

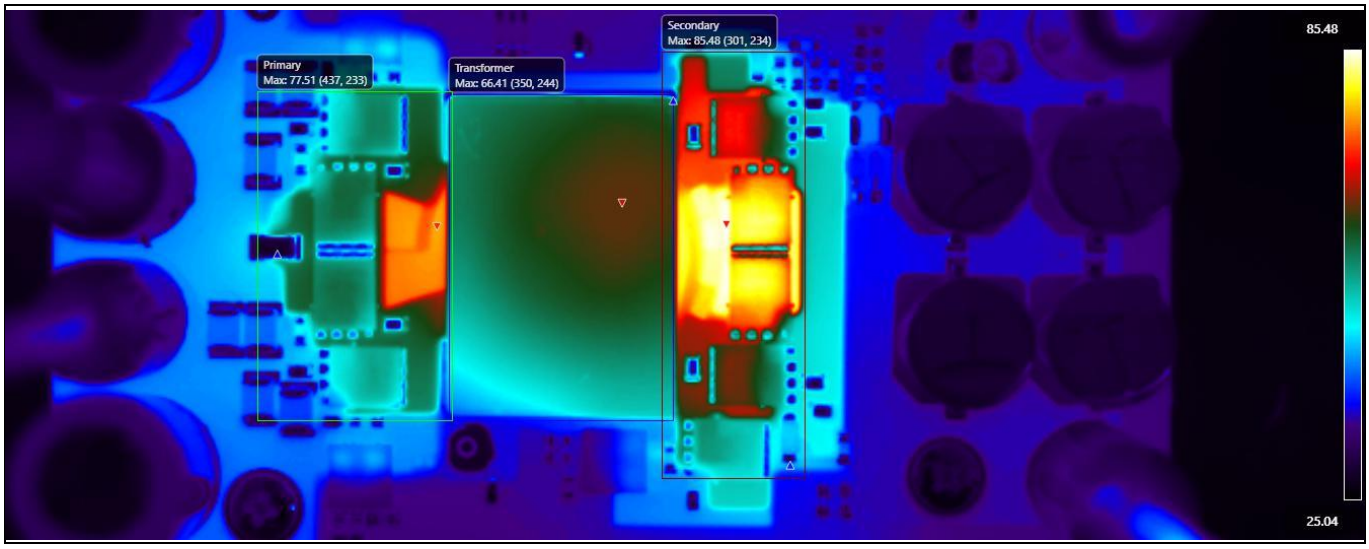


Figure 20 Thermal image for V_{IN} = -36 V

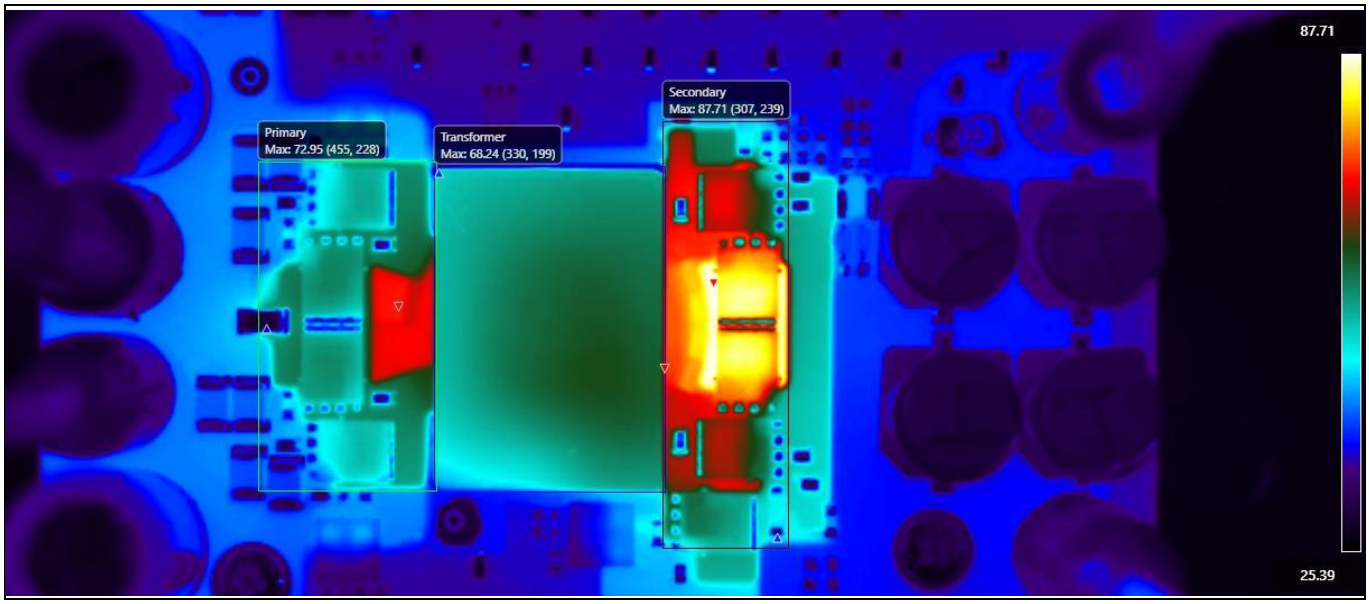


Figure 21 Thermal image for V_{IN} = -48 V

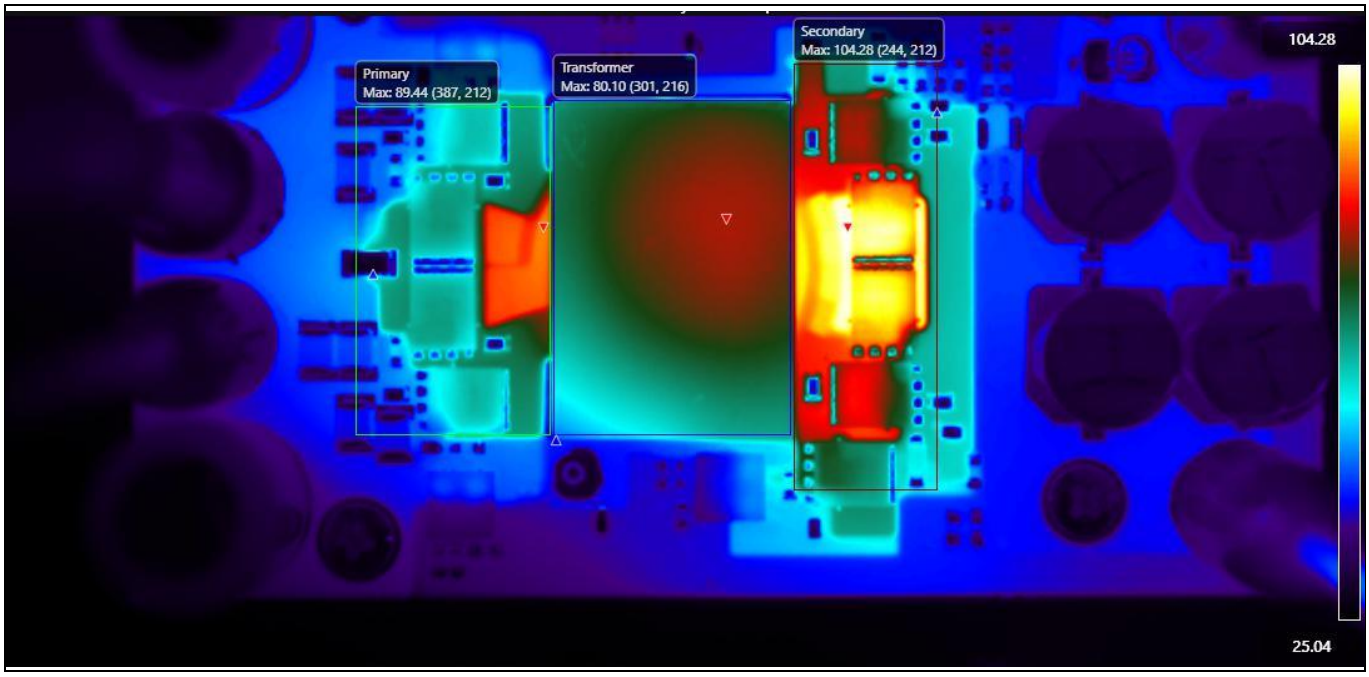


Figure 22 Thermal image for V_{IN} = -60 V

References

[1] Infineon Technologies AG. *AN230508: 750 W FB-FB quarter-brick DC-DC converter for RFPA applications*. Available online.

Revision history

Document revision	Date	Description of changes
Revision 1.00	2024-11-08	Initial release

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