ICL8105 - Digital Flyback Controller IC

.dp digital power 2.0

ICL8105 Design Guide

Design Guide

About this document

Scope and purpose

This document is a step-by-step guide for designing high-performance single-stage digital flyback AC-DC converter using the Infineon ICL8105 controller for LED lighting applications. The document also describes parameter handling for typical use cases using the Infineon .dp vision tool for the Infineon ICL8105.

Intended audience

This document is intended for anyone wishing to design high-performance single-stage digital flyback AC-DC converter for LED lighting based on the ICL8105.

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1 Introduction

1.1 Product Highlights

- High primary side-controlled output current accuracy (line/load regulation typical within +/- 3%)
- High power quality (typical power factor > 0.99 and total harmonic distrortion < 10%)
- Efficiency (up to 91%)
- Parameter configurability using graphic user interface .dp vision.
- Low-power standby mode
- Wide input voltage range
- Wide output voltage range
- Support for isolated 0 – 10 V dimming; no extra ICs required.



1.2 Features

- Single-stage flyback with power factor correction (PFC) and high-precision primary side-controlled constant current output
- Excellent line and load regulation capabilities
- Universal AC (85 – 305 V~) and/or DC input voltage
- Wide output voltage range
- Integrated 600 V startup cell
- Low Bill Of Materials (BOM)
- Intelligent thermal management
- Configurable parameters, e.g. adjustable voltage/current ranges, protection modes or gate driver slope for reduced EMI

1.3 Application

- Electronic control gear (ECG) for LED luminaires (5 W to 80 W)

1.4 Description

The ICL8105 is a configurable single-stage flyback controller with power factor correction (PFC), delivering a constant output current. The IC is available in a DSO-8 package and supports a wide feature set, requiring only a minimum of external components. A digital engine offers the possibility to configure operational parameters and protection modes, which helps to ease the design phase and allows a reduced number of HW variants in production. Accurate primary side output current control is implemented to eliminate the need for secondary side feedback circuitry.

1.5 Pin Configuration and Description

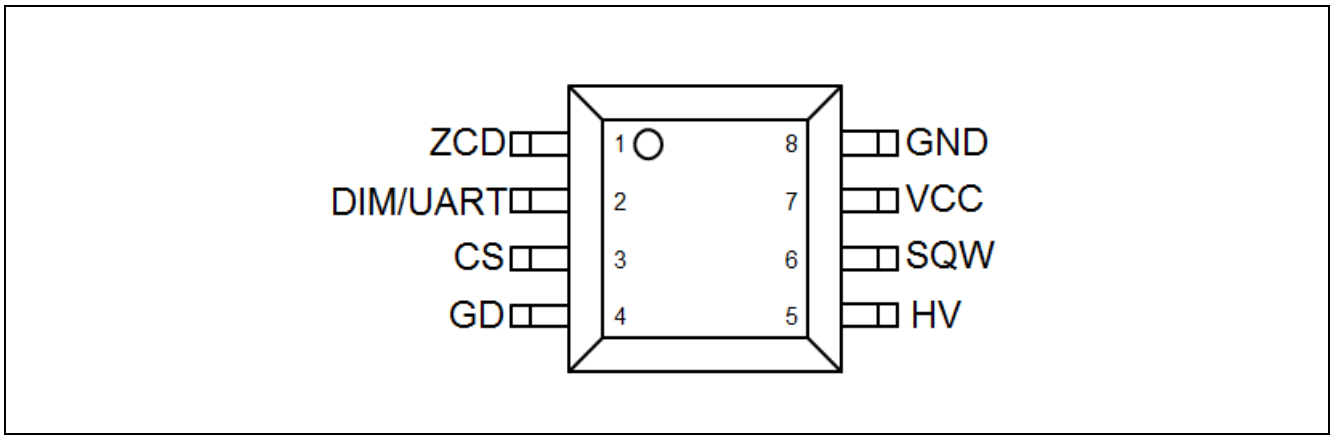


Figure 1 Pin Configuration

Table 1 Pin Definitions and Functions

Symbol	Pin	Type	Function
ZCD	1	I	**Zero crossing detection** The ZCD pin is connected to an auxiliary winding for zero crossing detection and sampled positive and negative voltage sensing.
DIM/UART	2	I/O	**Dimming / UART input** The DIM/UART pin is used as dimming input. During startup the pin is sensed for the UART interface to support configuration.
CS	3	I	**Current sense** The CS pin is connected to an external shunt resistor and the source of the power MOSFET.
GD	4	O	**Gate driver output** Output for directly driving a power MOSFET.
HV	5	I	**High-voltage input** The HV pin is connected to the rectified input voltage via an external resistor. An internal 600 V HV startup cell is used to initially charge VCC.
SQW	6	O	**Square wave generator output** The SQW pin provides a square wave signal for dimming. The signal is turned off for non-dimmed applications.
VCC	7	I	**Voltage supply** IC power supply.
GND	8	—	**Power and signal ground**

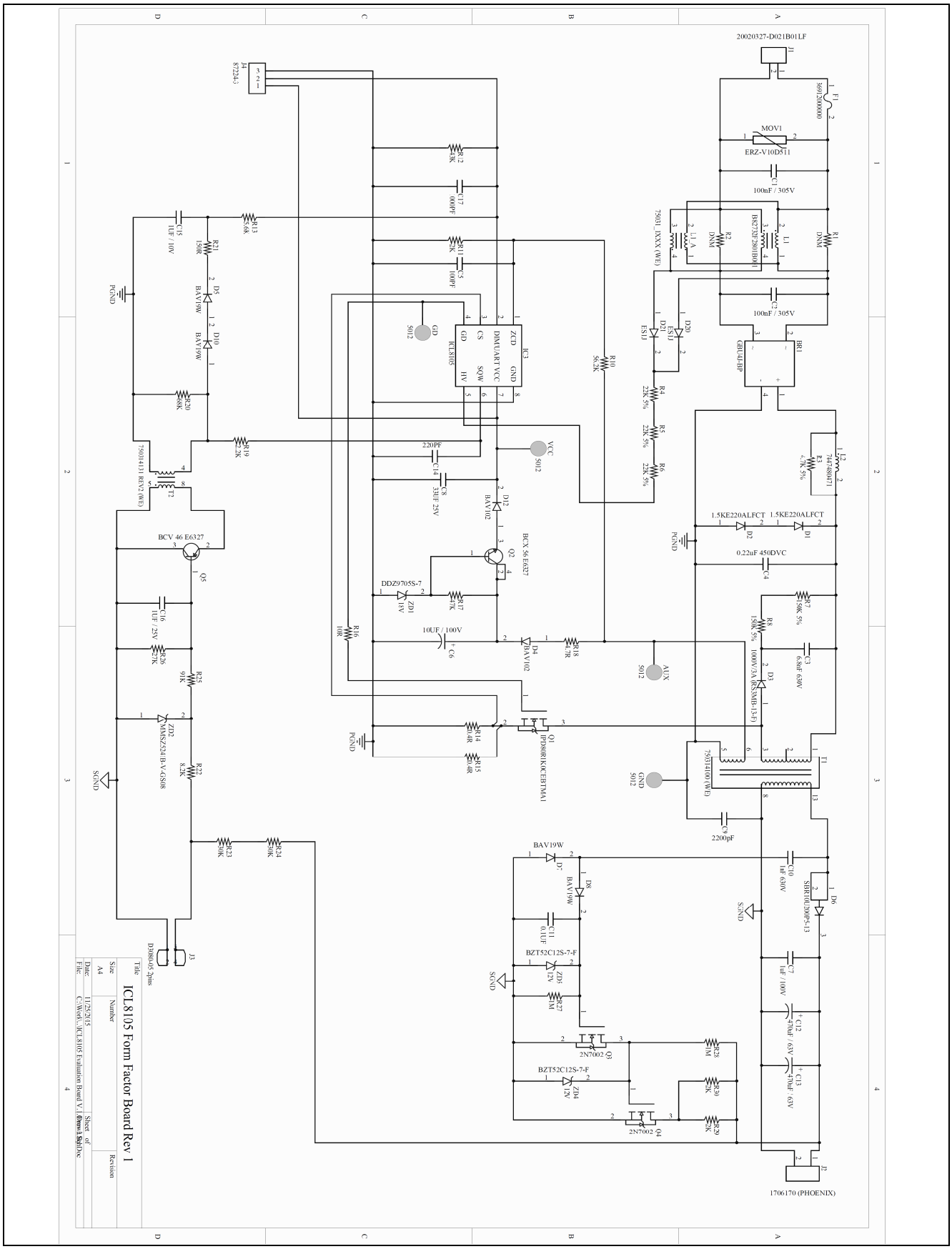


Figure 2 Schematic of a Typical Application Circuit

2.2 Designing an ECG

The ICL8105 is a digital AC/DC flyback controller with power factor correction (PFC). The PFC function enables a rectified sinusoidal input current waveform with a typical power factor (PF) > 0.99 and total harmonic distortion (THD) < 10% for a wide range of operating conditions.

The ICL8105 provides primary-side constant output current control that avoids the secondary-side control feedback loop circuitry usually needed in isolated power converters. This approach supports a low part count that is necessary to build up the application.

The ICL8105 uses a configurable multi-mode operation to select the best mode of operation for every operation condition. The multi-mode operation will automatically switch between quasi-resonant mode (QRM), discontinuous mode (DCM) and active burst mode (ABM).

In addition, the ICL8105 supports 0 - 10V dimming functionality with no additional microcontroller. Digital and RF interfaces can be supported by a microcontroller using a digital-to-analog converter.

Table 2 lists the system specification for an example design of a 40 W ECG.

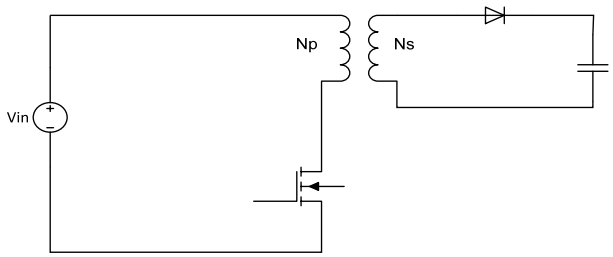
Table 2 System Specification

Parameter	Symbol	Value	Unit
Nominal input voltage	V_{in}	90 – 265	V~
Input overvoltage	$V_{in,OV}$	305	V~
Output power	P_o	40	W
Output voltage	V_{out}	15 – 45	V
Output overvoltage threshold	$V_{out,OV}$	50	V
Output current	$I_{out,set}$	880	mA
Efficiency	η	> 80	%
Minimum switching frequency	$f_{sw,min}$	30	kHz
Power factor		> 0.9	
THD		< 15	%
MOSFET maximum drain-source voltage	V_{DS}	800	V

2.3 Designing the Flyback Transformer

In flyback converters, the transformer stores energy during the forward cycle and transfers it to the secondary side in the flyback cycle. Current flows in either the primary or secondary winding, but not in both at the same time. Flyback transformer design is a somewhat iterative process, due to the number of variables involved, but it is not difficult, and with a little experience can become a quick and simple process.

First step, we shall set our reflected voltage, $V_{reflected}$ for our transformer design; the higher the $V_{reflected}$, the better the PF and THD. On the other hand, we need to consider the maximum voltage across the MOSFET for robust design.



$$V_{DS} = V_{in} + V_{reflected} \quad (1)$$

Where:

V_{DS} is the voltage across the MOSFET
V_{in} is the input voltage
$V_{reflected}$ is the output voltage reflected to the primary winding during flyback

Using an 800 V MOSFET and given a 30% margin for robust design, at worst case maximum input voltage = 305 V~:

$$V_{reflected} = V_{DS} - V_{in,max} \quad (2)$$

$$V_{reflected} = 0.7 * 800\ \text{V} - \sqrt{2} * 305\ \text{V} = 130\ \text{V}$$

Next, we shall calculate the maximum duty cycle, D_{max} which happens at lowest input voltage, $V_{inmin_{pk}}$

$$V_{inmin_{pk}} = \sqrt{2} * V_{in,\min} = \sqrt{2} * 85 = 120\ V$$

$$D_{max} = \frac{V_{reflected}}{V_{inmin_{pk}} + V_{reflected}} \quad (3)$$

$$D_{max} = \frac{130}{120 + 130} = 0.52$$

We will then calculate the peak current $I_{p,pk}$flowing thru the primary inductance of the transformer.

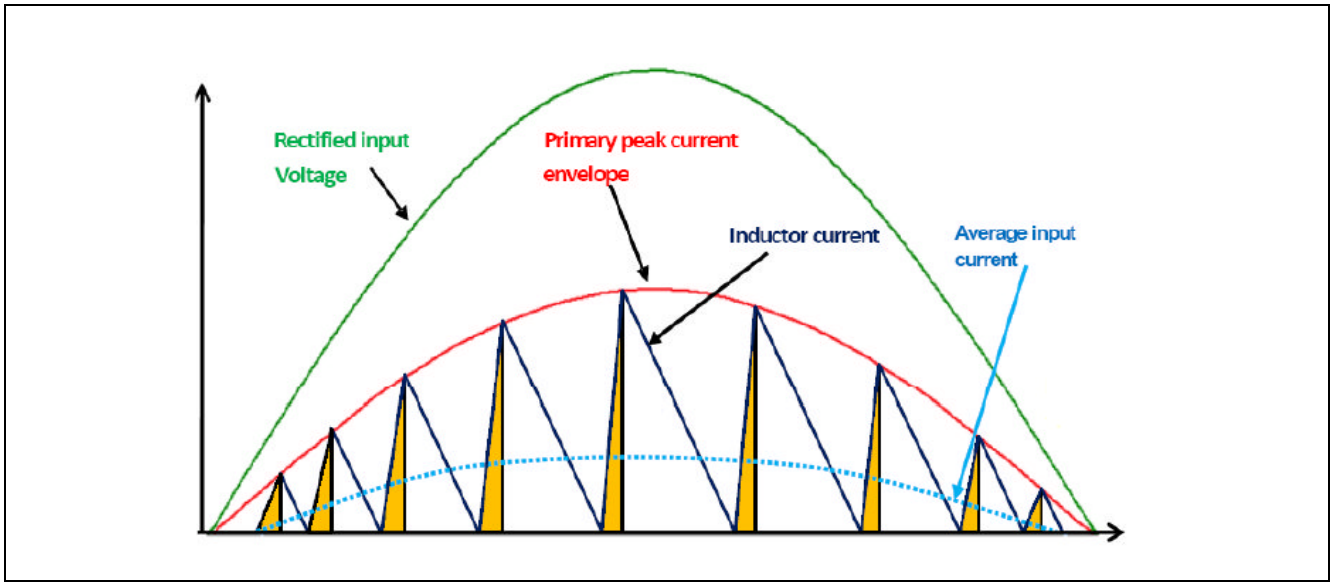


Figure 3 Current Waveform

$$P_{out} = \eta * I * V * PF \quad (4)$$

The maximum peak line current occurs at the lowest input voltage @ full load:

$$I_{inmax} = \frac{P_{out}}{\eta * V_{in,min} * PF} \quad (5)$$

$$I_{inmax} = \frac{40}{0.8 * 85 * 0.9}$$

$$I_{inmax} = 0.65 \text{ A}$$

Then, $I_{inmax_{pk}} = \sqrt{2} * I_{inmax}$

$$I_{inmax_{pk}} = 0.92 \text{ A}$$

$$I_{p,pk} = (k)\frac{2 * I_{inmax_{pk}}}{D_{max}} \quad (6)$$

K is a factor ≥ 1 that reflects the deviation from sinusoidal input current. Here k is approximated chosen to be equal to 1 since our input current is very close to sinusoidal shaped at low mains input.

Then, $I_{p,pk} = \frac{2 * 0.92\ A}{0.52} = 3.54$ A

Hardware Design

Choosing the minimum switching frequency $f_{sw,min}$ as 30 KHz
The transformer primary inductance L_p is calculated by:

$$L_p = \frac{D_{max} * V_{inmin_{pk}}}{I_{p,pk} * f_{sw,min}} \quad (7)$$

$$L_p = \frac{0.52 * 120}{3.54 * 30 * 10^3}$$

$L_p = 588$ µH
For a good design, we set

$$V_{reflected} = \left(V_{out} * \frac{N_p}{N_s}\right) \quad (8)$$

$$130\ \text{V} = \left(45\ \text{V} * \frac{N_p}{N_s}\right)$$

$$\frac{N_p}{N_s} \cong 3$$

The next step is to calculate the number of turns for the required inductance. Using

$$N_p = \frac{L_p * I_{p,pk}}{B_{sat} * A_e} \quad (9)$$

Where:

L_p is the primary inductance
N_p is the number of turns on the primary winding
$I_{pri_{pk}}$ is the peak current on the primary winding
B_{sat} is the flux density in Tesla (typically 0.35T should be chosen for flyback converters)
A_e is the effective area of the transformer core; using PQ20/20, from the datasheet, Ae = 65 x 10^{-6}m^2

$$N_p = \frac{588 * 10^{-6} * 3.54}{0.35 * 65 * 10^{-6}} \cong 90 \text{ turns}$$

Using $\frac{N_p}{N_s} = 3$, we calculated N_s = 30 turns

The voltage obtained from the bias winding has to be high enough to support the IC V_{cc} during the worst case condition, i.e. when the output voltage is at a minimum during full dimming. The IC will restart at a V_{cc} of 6 V. To have some margin, $V_{CC,min}$ = 10 V was chosen:

$$N_a = N_s * \frac{V_{cc,min}}{V_{out,min}} = 30 * \frac{10\ \text{V}}{10\ \text{V}} = 30 \text{ turns}$$

Please note that the transformer design is an iterative process, i.e. based on above calculated transformer specification, we will construct the transformer and tested it out to check the performance. Based on the tested result, we will re-design the transformer to get the optimize result that we desire.

After a few rounds of re-design, the final transformer specification for this system is as follows:

Transformer primary inductance L_p = 540 µH
Number of primary winding turns, N_p = 66 turns
Number of secondary winding turns, N_s = 17 turns
Number of auxillary winding turns, N_a = 17 turns

2.4 Selecting the MOSFET

As we have selected an 800 V-rated MOSFET, the next step is to calculate the maximum peak current. It can be calculated using the peak current $I_{inmax_{pk}}$ calculated in equation (2).

The actual peak current $I_{p,pk}$ on the primary winding was calculated in the above section,
$I_{p,pk} = 3.54$ A

With respect to the Infineon Power Management Selectionguide [4] the CoolMOS™ transistor SPD06N80C3 (800 V, 6 A, $R_{DS(on)}$ = 0.9 Ω) is chosen in consideration of the margins.

Attention: ***To protect the MOSFET against component or soldering failures (e.g. pin GD open), a 10k resistor between MOSFET gate and MOSFET source is recommended.***

2.5 Selecting the Snubber Circuit

In flyback converters, resonance between transformer leakage inductance and parasitic capacitance causes excessively high voltage surges that cause damage to the MOSFET during turn-off. This voltage surge must be suppressed by a snubber circuit as shown in **Figure 4**.

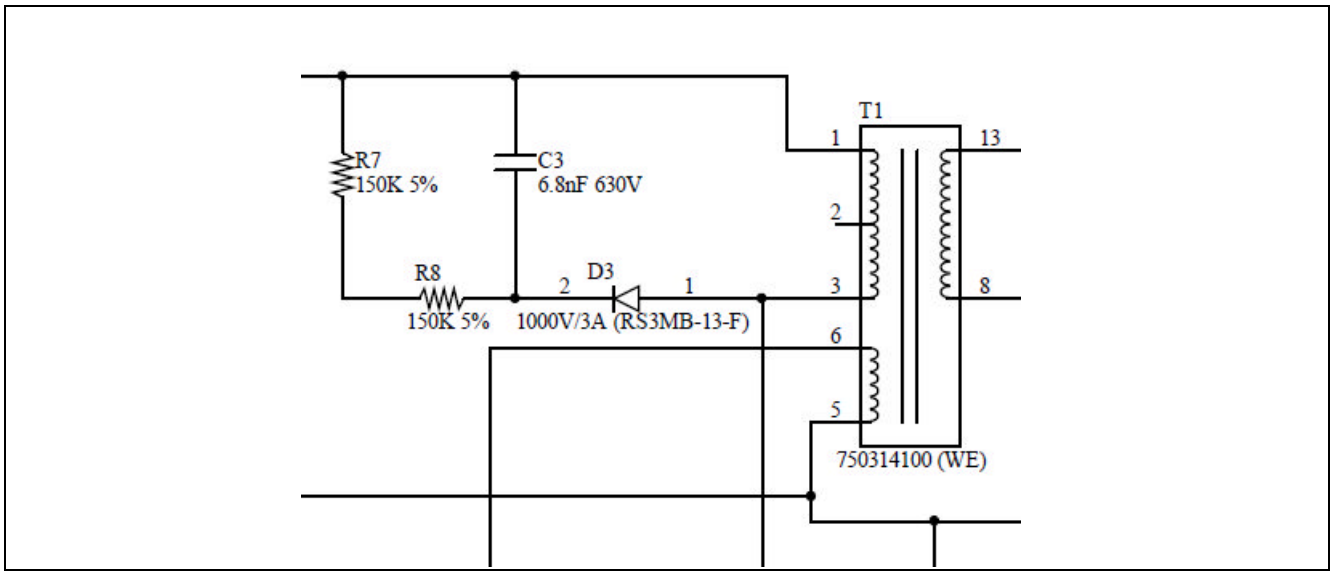


Figure 4 Snubber Circuit

2.6 Selecting the Input Capacitor

The input capacitance C4 in **Figure 5** is used to improve EMI performance of the system. However, it has direct impact on PF and THD as well. To improve the PF and/or THD, an enhanced PFC feature is available to compensate for the effects of the input capacitance to optimize the PF and/or THD (see **Section 3.1.6**).

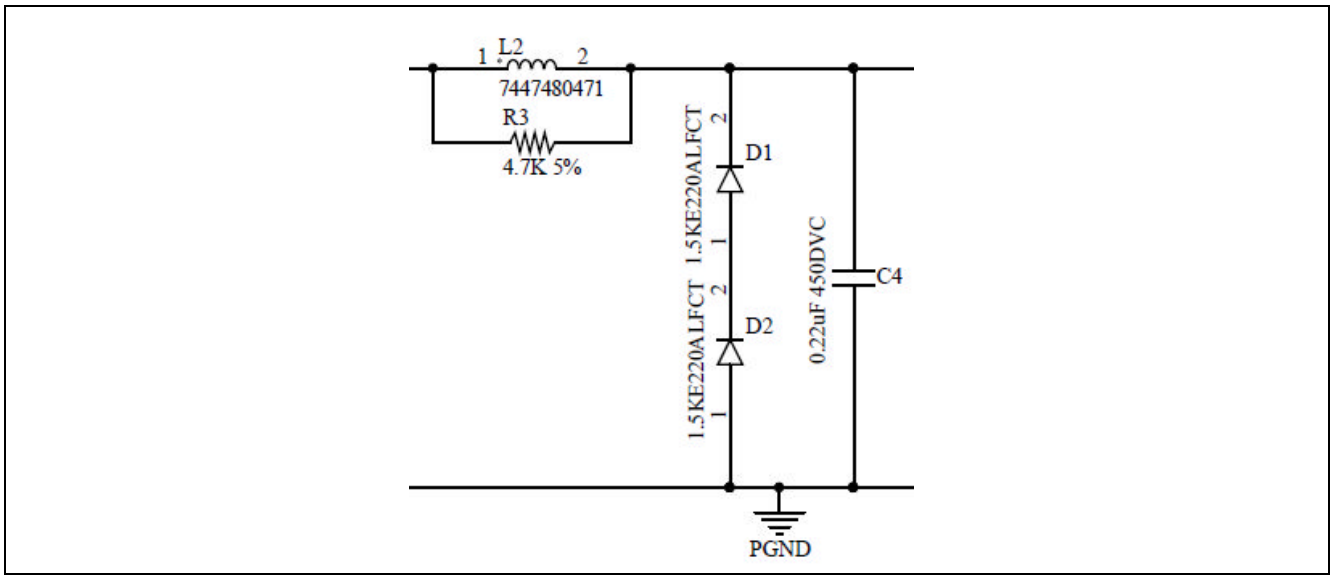


Figure 5 Input Capacitor

2.7 Selecting the Secondary Rectifier Diode

The secondary rectifier diode has to be selected to withstand the maximum reverse voltage and to be able to carry the forward peak current.
The maximum reverse voltage of the secondary rectifier diode can be calculated by:

$$Vr_{max} = V_{out,OV} + \frac{Ns}{Np} * V_{in,OV} \quad (9)$$

$$Vr_{max} = 50 + \frac{30}{90} * \sqrt{2} * 305 = 194\ \text{V}$$

The forward peak current of the secondary rectifier diode can be calculated by:

$$Ir_{pk} = \frac{2}{1-\text{DIin(max)}_{\text{pk}}} * Iout \quad (10)$$

$$Ir_{pk} = \frac{2}{1-0.52} * 880\ \text{mA} = 3.67\ \text{A}$$

Therefore, the SBR10U200PS (200 V/10 A) is chosen in consideration of the margins.

2.8 Selecting the Output Capacitor

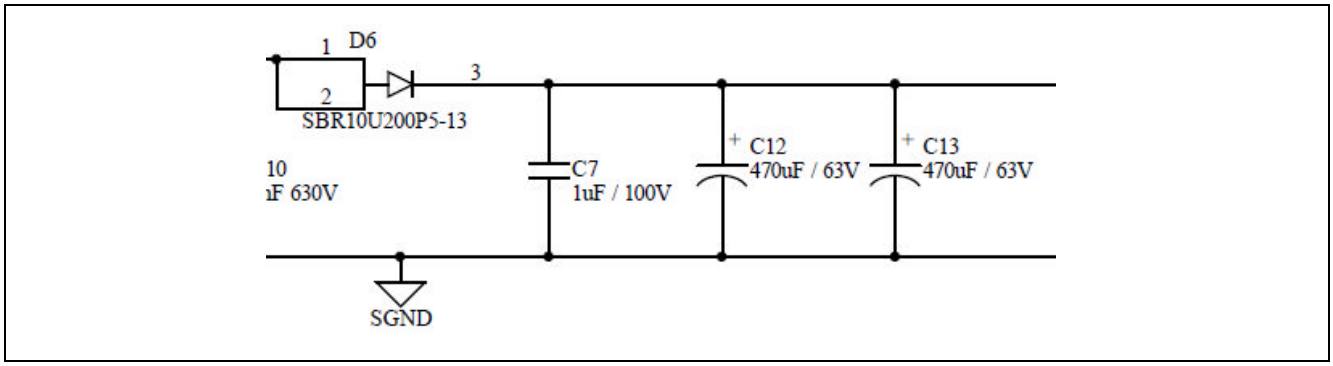


Figure 6 Output Capacitor

Output capacitance will need to be selected carefully in order to meet the LED ripple current. It represents a trade-off between LED ripple current and BOM cost that the designer has to choose. In addition, the capacitor has to be able to handle the ripple current through it. As a rule of thumb, the total output capacitors should be able to handle at least 2.5 times the max LED DC current at maximum temperature.

2.9 Selecting the High-Voltage Input Resistor

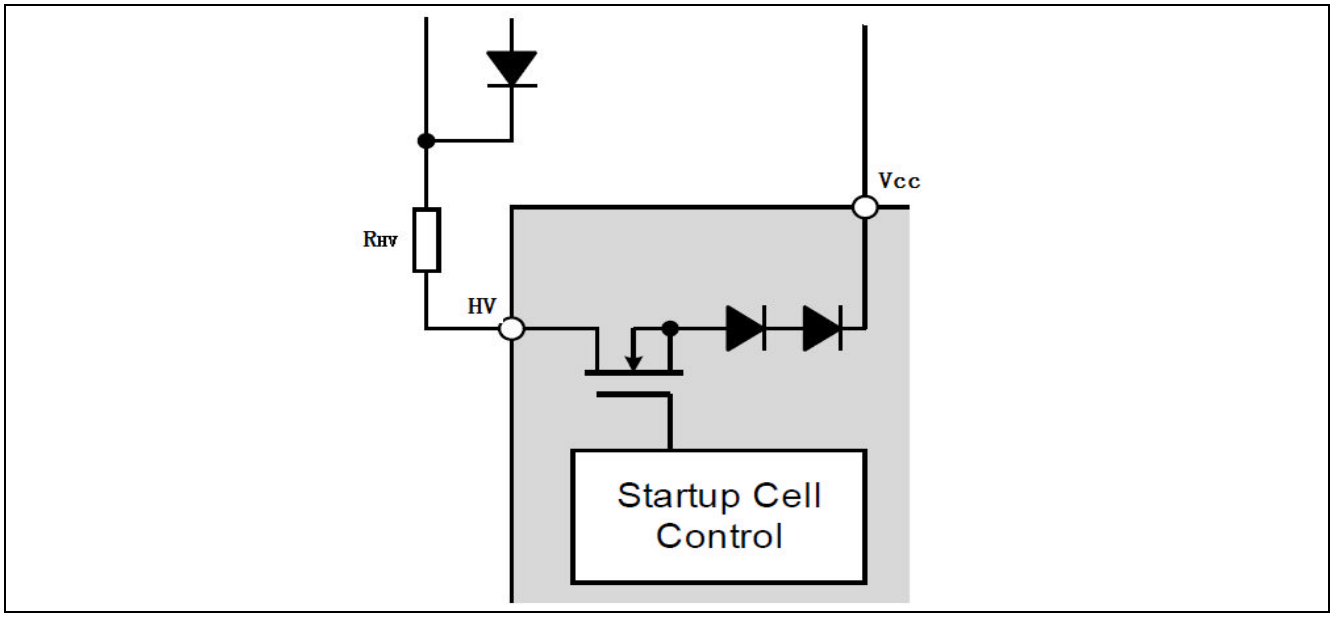


Figure 7 HV Resistor

To limit the HV current, R_{HV} must be:

$$R_{HV} > \frac{\sqrt{2}\,V_{in,OV}}{I_{HVmax}}$$

where

$V_{in,OV}$ is the input overvoltage threshold

I_{HVmax} : 9.6 mA (refer to the IC datasheet)

$R_{HV} > \frac{\sqrt{2}*305}{9.6*10^{-3}}\ \Omega = 44.93\ k\Omega$

The selection of this resistor allows a trade-off between power consumption and time-to-light.

To have some margin, R_{HV} = 66 kΩ was chosen.

Attention: ***To maintain the high input voltage and to lower the risk of component failure, this resistance must be splitted into minimum two 1206 resistors (Vin(rms)<277ac) or minimum three 1206 resistors (Vin(rms)<305Vac).***

2.10 Selecting the Current Sensing (CS)

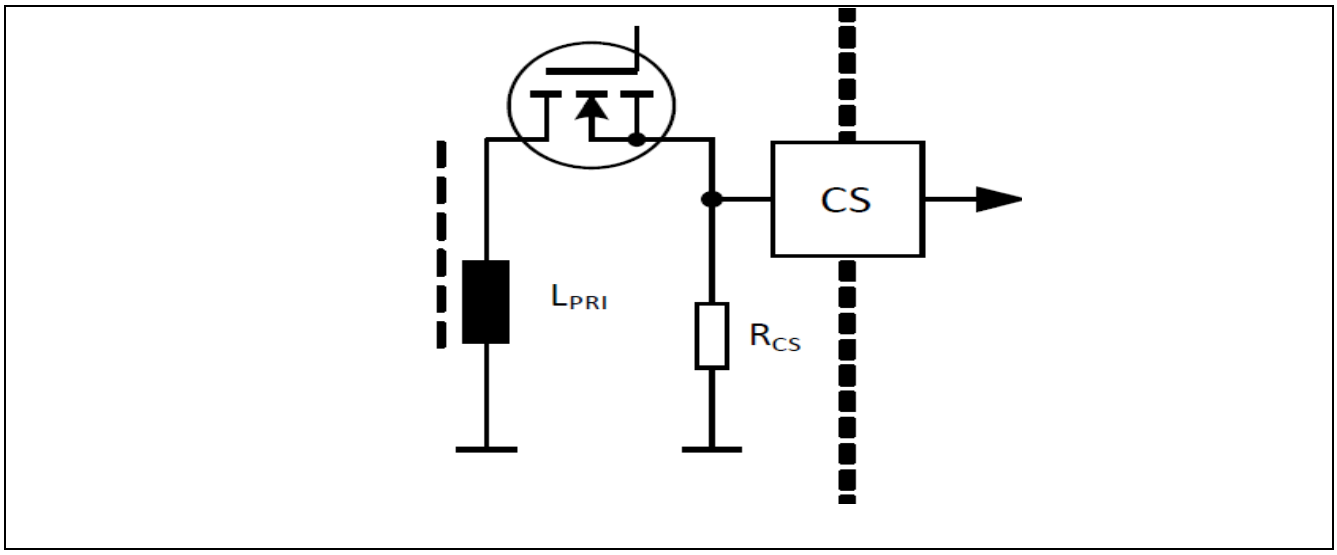


Figure 8 CS Resistor

The primary input peak current is determined by sensing the sampled signal V_{CS} at the CS pin. The output current I_{out} will then be calculated based on the output diode conduction time and the switching period. The recommended operating voltage range at the CS pin is 0 V to 1.2 V. Thus, R_{CS} must be lower than $1.2/I_{OCP1}$.

I_{OCP1} is the switching cycle-by-cycle primary current limit in the flyback transformer design (which we have caluculated to be $I_{p,pk} = 3.54$ A = I_{OCP1})

$R_{CS} < \frac{1.2\ V}{I_{OCP1}}$

$R_{CS} < \frac{1.2}{3.54}\ \Omega = 0.34\ \Omega$

The sense resistor was chosen to be R_{CS} = 0.2 Ω for better power consumption.

2.11 Selecting the Zero Crossing Detection (ZCD) Resistors

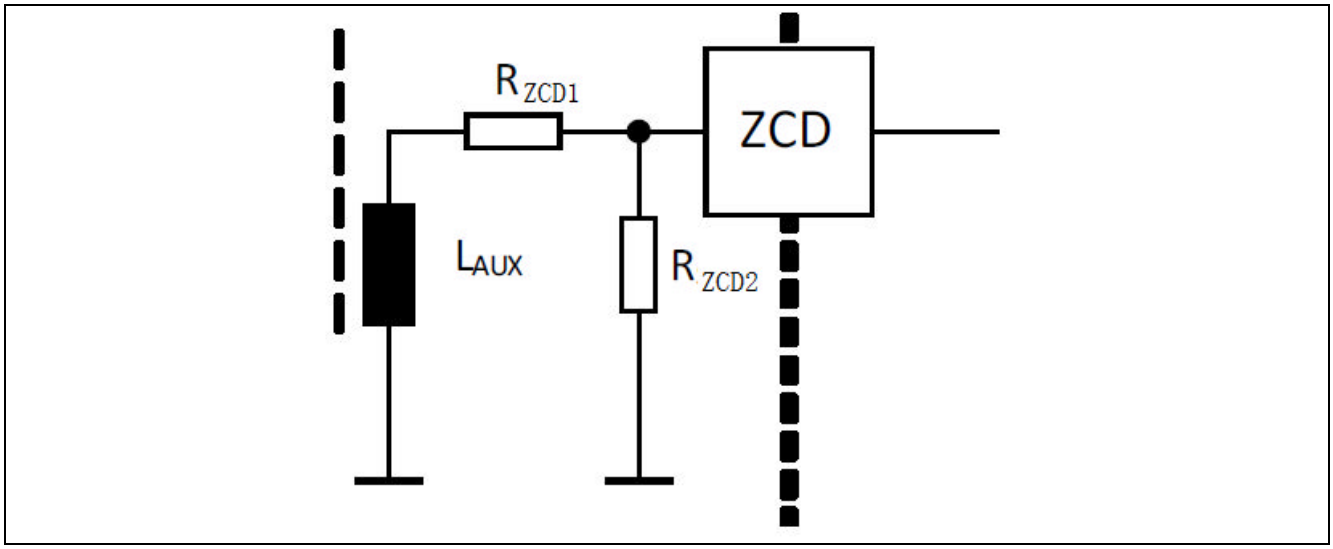


Figure 9 ZCD Resistors

To ensure that the maximum input and output voltages can be measured,

$$R_{ZCD1} > \left(\frac{\sqrt{2}\,V_{in,OV}*\left(\frac{N_a}{N_p}\right)-V_{clamp}*\frac{V_{out,OV}}{V_{ZCDmax}}*\left(\frac{N_a}{N_s}\right)}{Iclamp_{\max}}\right)$$

where

$V_{in,OV}$ is the input overvolage threshold
$V_{out,OV}$ is the output overvoltage threshold
V_clamp : 0.2 V (refer to the IC datasheet)
V_{ZCDmax} : 2.66 V (refer to the IC datasheet)
$Iclamp_{\max}$: 3.2 mA (refer to the IC datasheet)

$$R_{ZCD1} > \left(\frac{\sqrt{2}*305*\left(\frac{17}{66}\right)-0.2*\frac{50}{2.66}*\left(\frac{17}{17}\right)}{3.2*10^{-3}}\right)\ \Omega$$

$$R_{ZCD1} > 33.1\ \text{k}\Omega$$

To have some margin, R_{ZCD1} = 56.2 kΩ was chosen.

$$R_{ZCD2} < \frac{R_{ZCD1}*V_{ZCDmax}*N_S}{Vo_{peak}*N_A-V_{ZCDmax}*N_S}$$

$$R_{ZCD2} < \frac{56200*2.66*17}{50*17-2.66*17}$$

$$R_{ZCD2} < 3.2\ \text{k}\Omega$$

Again, to have sufficient margin, R_{ZCD2} = 2.0 kΩ was chosen.

2.12 Selecting the Zero Crossing Detection (ZCD) Capacitor

As seen in **Figure 10**, C5 is required to filter noise on the ZCD pin. Please note that the capacitance of such ceramic capacitors varies with temperature. For good performance, it is recommended to use a C0G/NP0 ceramic capacitor.

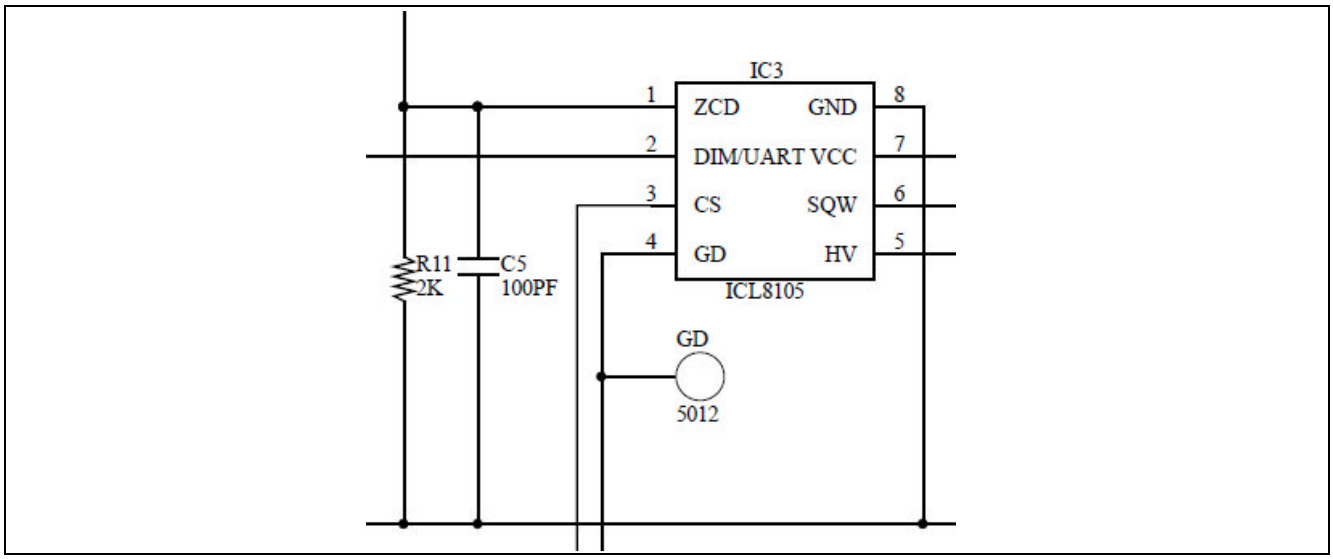


Figure 10 ZCD Capacitor

2.13 Dimensioning the Vcc Regulator Circuit for Wide Output Voltage Range

For applications that use a wide output voltage range exceeding a factor of two, a linear regulator for V_{CC} is required. This regulator ensures that the voltage at the V_{CC} pin is less than the Vcc overvoltage threshold.

The recommended range for ZD1 is 12 V to 18 V. The Vcc capacitor, C8, must be large enough to provide power during startup until self-supply becomes available.

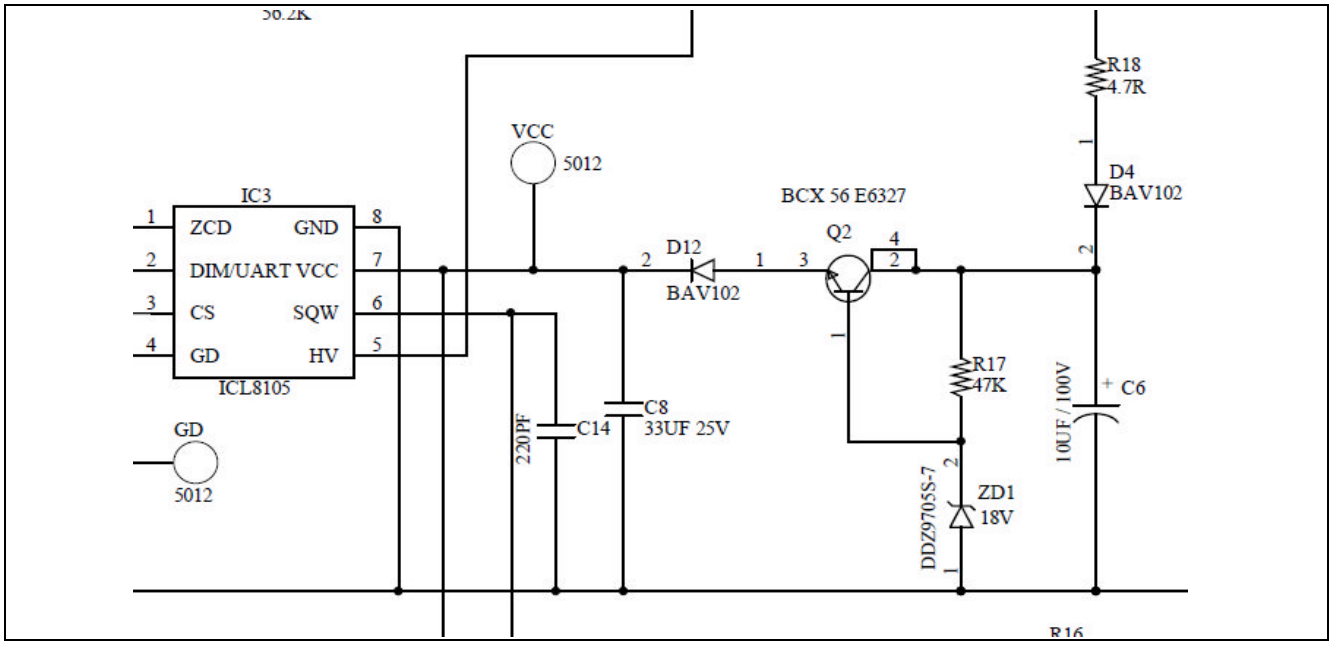


Figure 11 Vcc Regulator Circuit for Wide Output Voltage Range

2.14 Designing an Isolated 0 – 10 V Dimming Circuit

Isolated dimming control is implemented using the 0 - 10 V dimming circuit as shown in **Figure 12**. The SQW pin generates a square wave signal with 160 KHz, 7.5 V and a 50% duty cycle for the primary side of the dimming circuit. Dimming voltage inserted on the secondary side will effectively change the voltage on the primary side. A diode peak detector circuit on the primary side stores this dimming voltage information on the 1 nF capacitor for use as a dimming voltage.

The pull-up circuit on the right of **Figure 12** provides power to a current-sink dimmer while limiting the source current. It also ensures that the system provides full light output if no dimmer is connected. This circuitry is not required if a voltage source is delivering the dimming voltage.

Please note that D5 and D10 are necessary for temperature compensation on the voltage drop causes by the PNP Darlington transistor, Q5 (BCV46).

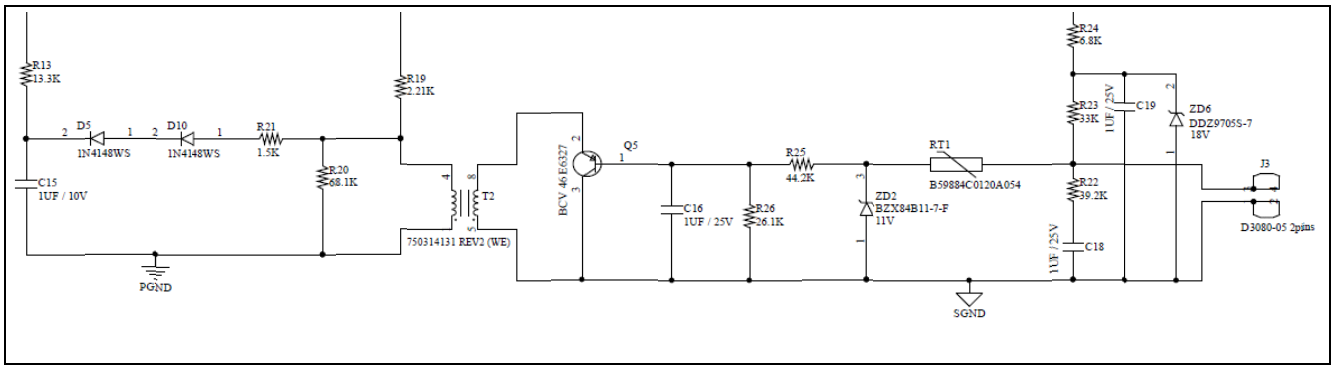


Figure 12 0-10 V Dimming Circuit

2.15 Designing the Pulse Transformer for 0 – 10 V Dimming Circuit

For pulse transformer design, it is recommended to use high permeability material. In our application, we have chosen to use A062 toroid core, which has an initial permeability of 6000 +/- 25% @25°C

	Symbol	Unit	Measuring Conditions			Telecom High Permeability Material
			Freq.	Flux den.	Temp.	A062
Initial Permeability	μ_i		≤ 10kHz	0.25mT	25°C	6000 ± 25%
Relative Loss Factor	tanδ/μ_i	10^{-6}	10kHz	< 0.25mT	25°C	< 10
			100kHz		25°C	< 30
Saturation Flux Density	Bms	mT	10kHz	H = 1200A/m	25°C	460
					100°C	320
Remanence	Brms	mT	10kHz	H = 1200A/m	25°C	100
					100°C	80
Temperature Factor of Permeability	αF	10^{-6}/°C	10kHz	< 0.25 mT	0 ~ 20°C	1 ~ 3
					20 ~ 70°C	-1 ~ 1
Hysteresis Material Constant	ηB	10^{-6}/mT	10kHz	1.5-3.0mT	25°C	< 0.5
Disaccommodation Factor	DF	10^{-6}	10kHz	< 0.25 mT	25°C	< 2
Curie Temperature	Tc	°C				160
Resistivity	ρ	Ωm				0.20
Density	d	g/cm³				4.85

Note: Material characteristics are typical for a toroid core.
Product specification will differ from these data due to the influence of geometry and size.

Figure 13 A062 toroid core specification

Hardware Design

To have highest permeability and least winding, it is suggested to operate around the knee point of the curve @ 200 KHz.

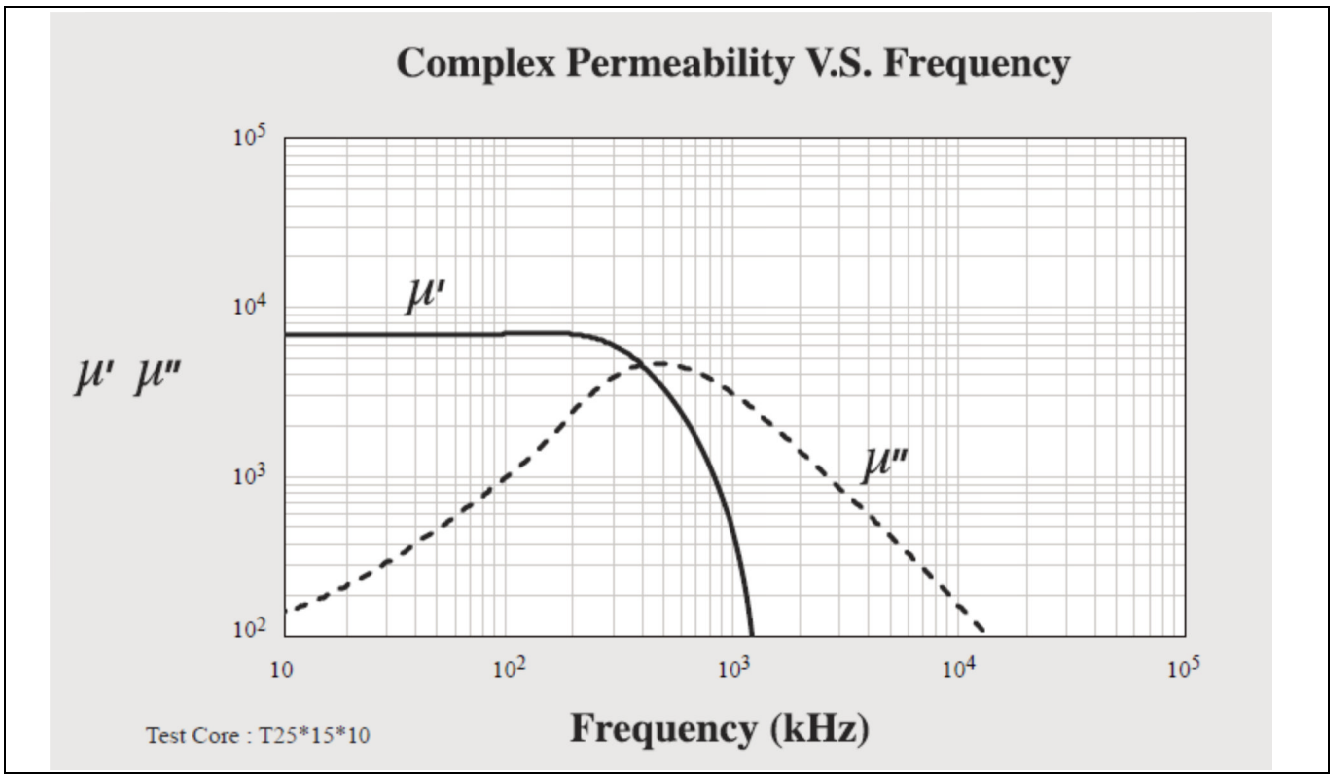


Figure 14 Complex Permeability VS Frequency

Next step is to calculate the minimum inductance required for our application.

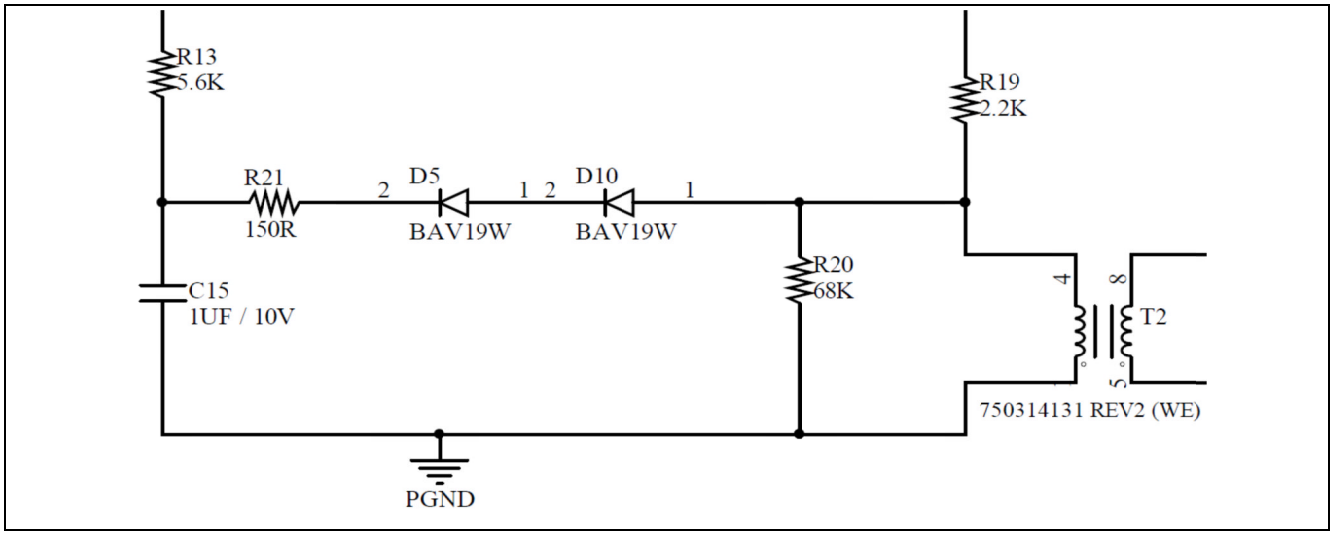


Figure 15 0-10 V Dimming Circuit

Hardware Design

Pulse signal information: Frequency = 200 KHz, 50% duty cycle, V_{max} = 7.5 V

Current flowing into pulse transformer, T2 is limited by R19 and can be computed as:

$$i = \frac{7.5 - V_{R20}}{R19}$$

Voltage across R20, $V_{R20} \cong V_{C15} + V_{D5} + V_{D10}$

Where

V_{C15} is the voltage at dimming pin, which is 1.8 V

V_{D5} is the voltage drop across D5 which is 0.7 V

V_{D10} is the voltage drop across D10 which is 0.7 V

So, $V_{R20} \approx 3\ V$

$$i = \frac{7.5 - 3}{2200}$$

i = 2.05 mA

$$L * i = V * t$$

Where t=2.5 µs, this is the t_{on} of the 200 KHz, 50% duty cycle

$$L = \frac{V * t}{i}$$

$$L = \frac{3 * 2.5 * 10^{-6}}{2.05 * 10^{-3}}$$

$L = 3.66$ mH

Noted that the permeability drops when temperature decreases, we need to consider this factor to ensure proper operation at low temperature.

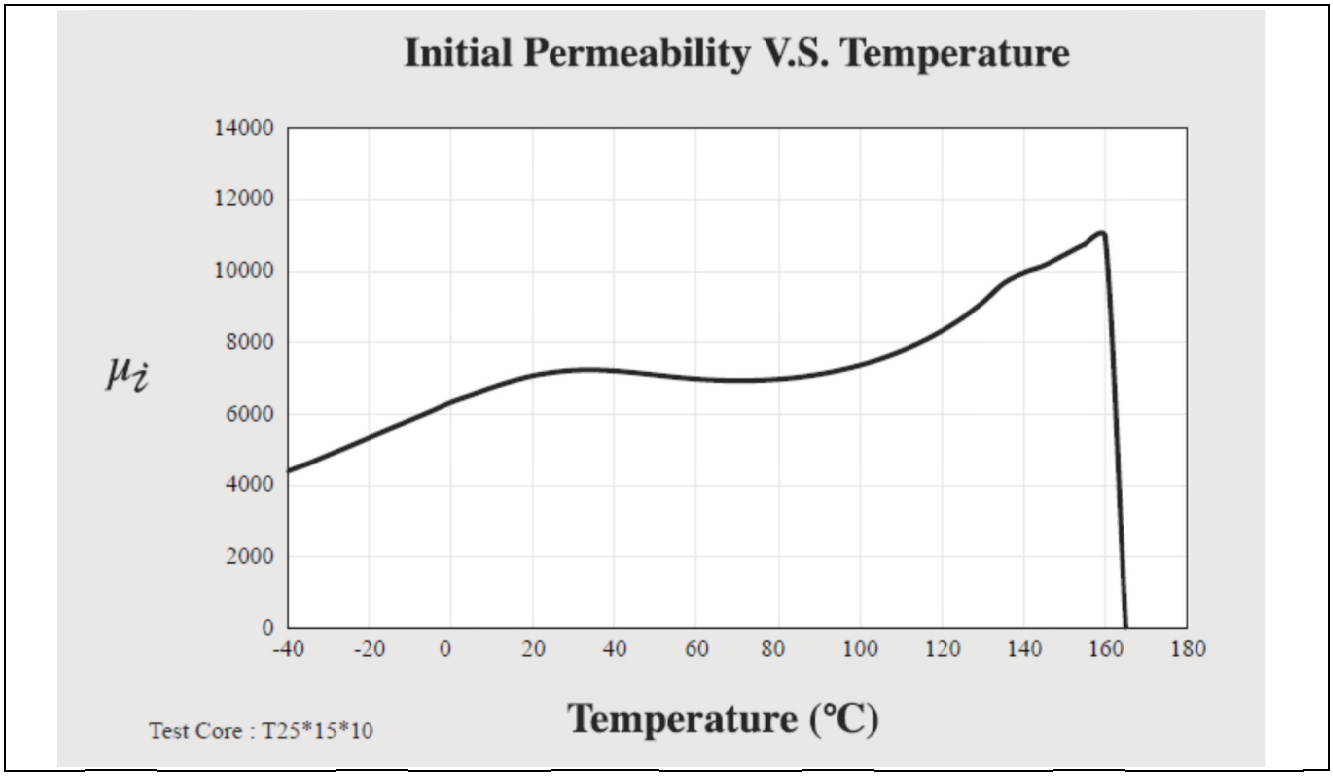


Figure 16 Permeability VS Temperature

From above curve, for low temperature compensation we need to add 35% margin to the computed inductance. The other factor we need to compensate is the tolerance of +/- 25%, so for worst case we need to add another 25% to the computed inductance.

, thus, $L = 3.66 * \frac{1}{0.65} * \frac{1}{0.75}$ mH

$L \cong 7.15$ mH

The AL value of A062 toroid core is 4000 nH/T^2

$$N = \sqrt{\frac{L}{AL}}$$

$$N = \sqrt{\frac{7.51 * 10^{-3}}{4000 * 10^{-9}}}$$

$N \cong 44$ turns

With N = Npri =Nsec = 1:1 = 44:44

2.16 Designing a PWM to Analog Conversion Circuit

In some cases where the dimming control circuitry is on the primary side and it is using PWM control, the circuit shown below is a typical PWM to analog conversion circuit. This circuit will convert the PWM dimming information to an analog dimming voltage that is used by the DIM/UART pin for the required dimming.

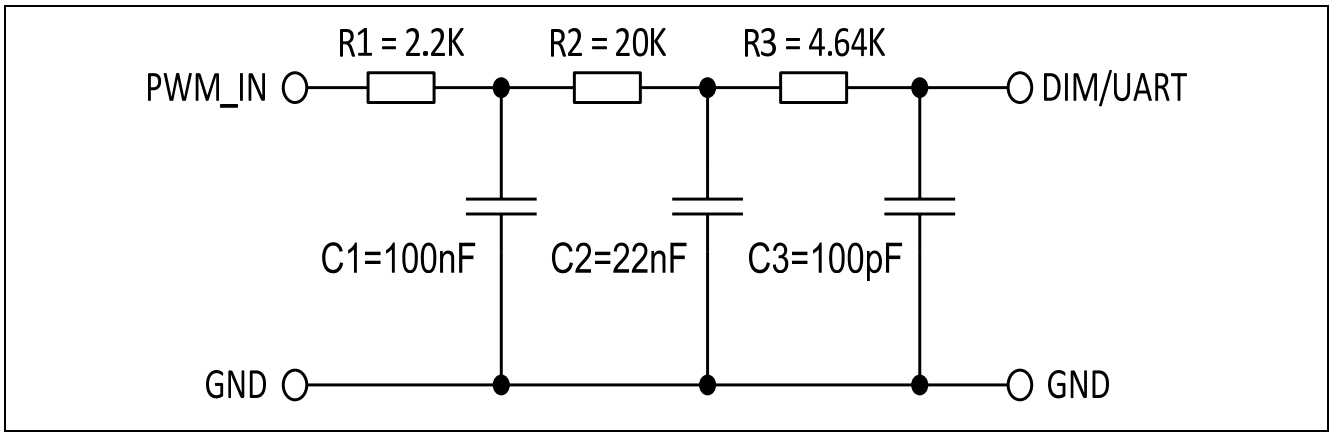


Figure 17 PWM to Analog Conversion Circuit

2.17 Designing an Active Bleeder Circuit

To discharge the extra electric charge stored in the output capacitor when the LEDs are disconnected, output bleeder circuitry is designed. The active bleeder circuit is used here although it has more components, but the resistor to discharge the extra charges is only on when needed and it does not require manual switching.

Note: This circuitry is required if output voltage needs to be maintained without light output (e.g. Dim-to-Off or for open load).

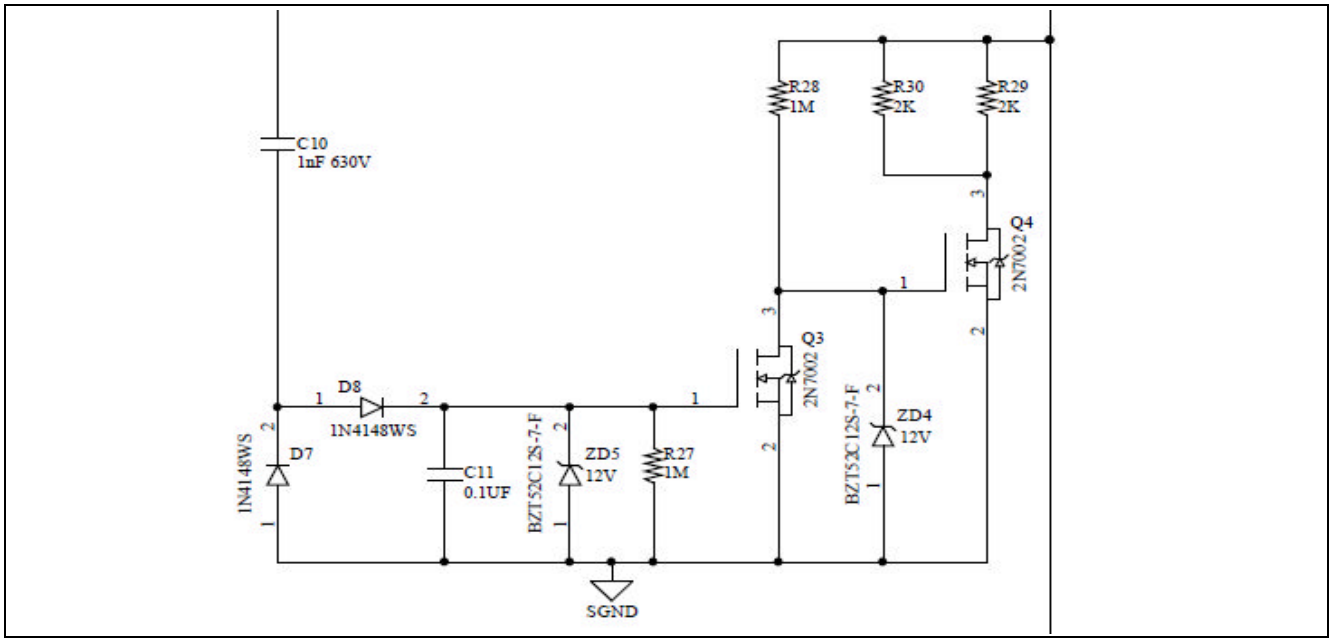


Figure 18 Active Bleeder Circuit

2.18 Components for Safety and Protection

Attention: ***To protect against failures of components, the circuit must be protected by a fuse.***

Attention: ***For surge protection, usage of a varistor at the input as well as high-voltage diodes behind the bridge for transient voltage suppression is recommended to absorb the surge.***

2.19 PCB Layout Guidelines

In power supply systems, PCB layout is a key point for a successful design. Following are some suggestions for this.

- Minimize the loop with pulse share current or voltage: Examples are the loop formed by the bus voltage source, primary winding, main switch and current sensing resistor or the loop consisting of secondary winding, output diode and output capacitor, or the loop of VCC power supply.
- Good grounding of ICL8105: As ICL8105 sees every signal to the reference point of the ICL8105 ground which is also the ground of the VCC power supply, it is advisable that the ground of the ICL8105 is connected to the bus voltage ground through a short and thick PCB track in a star structure. Note that ground of ICL8105 is treated as small signal ground and the RCS resistor ground and primary ground of auxiliary winding of the transformer are treated as power loop ground. It needs to be separated before connected to the bulk capacitor ground.
- Good grounding of other parts/functions: This includes the ICL8105 ground, DIM/UART loop ground, ZCD loop ground and the VCC loop ground. It is advisable that all the above grounds connected to the ICL8105 ground and then connected to the bus voltage ground using a star-structure.
- The high voltage pins are connected to bus voltage in typical applications. During lightning surge test, the noise on bus voltage is high. It is suggested that the track to HV pin shall be kept away from other small signal tracks. The distance is better to be more than 3mm.
- Please also keep distance of small signal tracks from MOSFET drain trace of at least 4mm

3 Parameter Handling / Recommendations

After finishing calculations of the hardware components in **Chapter 2**, the user has to determine the configuration for the ICL8105 ICs. This is achieved by entering the hardware configuration and the customer's requirements into the .dp vision tool. Based on this data, the .dp vision tool will automatically calculate all relevant parameters. The tool also allows the user to test the ICs with the parameters and finally to burn the parameters to the ICs.

A complete list of available parameters in ICL8105 can be found in the ICL8105 Target Datasheet (see [1]). Relevant information on using the .dp vision tool is available in the ICL8105 Universal Evaluation Board Application Note (see [2]) and in the .dp vision User Guide (see [3]).

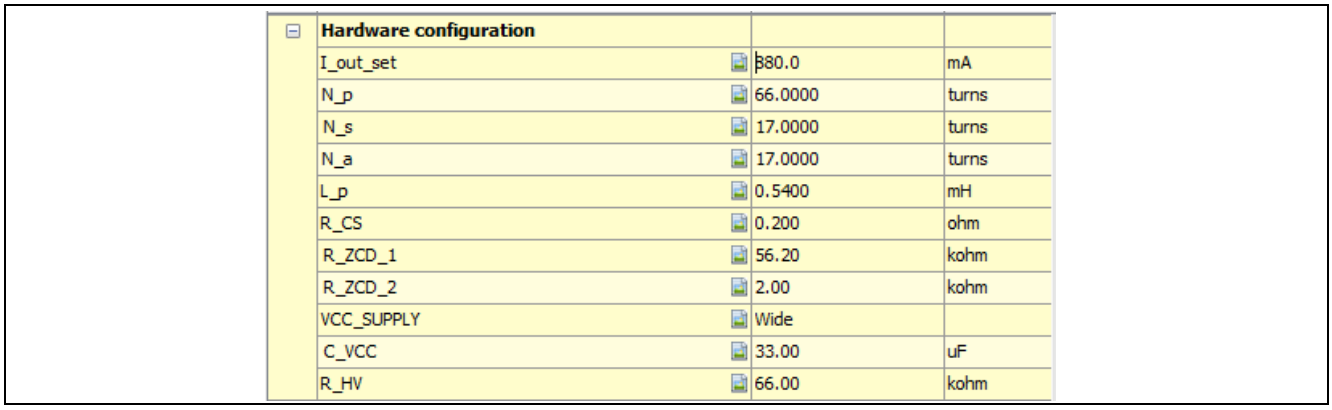
In the following subsections, a few examples on how to set up an ICL8105 configuration file are described. Additionally, the process of testing and burning parameters is described.

3.1 Design Parameters

After opening an existing configuration file, it is necessary to enter the appropriate values calculated previously in the design parameters box table. Available parameters are presented in the following subsections.

3.1.1 Hardware Configurations

Hardware configurations represent hardware component values that are calculated and assembled on the specified application board. According to calculations in the previous chapter, the parameters are entered accordingly (**Figure 19**).



Hardware configuration		
I_out_set	380.0	mA
N_p	66.0000	turns
N_s	17.0000	turns
N_a	17.0000	turns
L_p	0.5400	mH
R_CS	0.200	ohm
R_ZCD_1	56.20	kohm
R_ZCD_2	2.00	kohm
VCC_SUPPLY	Wide	
C_VCC	33.00	uF
R_HV	66.00	kohm

Figure 19 Hardware Configuration

In addition to the parameters determined by the formulas in the previous chapter, a few other items of hardware information is required:

VCC_ext and VCC_reg: Depending on the following cases, the user will need to configure these two parameters accordingly.

a. Narrow or fixed output voltage range
   i. VCC_ext: Self-supply
   ii. VCC_reg: Direct
b. Wide output voltage range
   i. VCC_ext: Self-supply
   ii. VCC_reg: With regulator
c. External supply
   i. VCC_ext: External
   ii. VCC_reg: Anything (this setting has no effect in this case)

3.1.2 Protections

Protection (**Figure 20**) parameters[1] represent chip-specific hardware features that can be configured by the user to adjust them for the custom application.

Protections		
t_start_max	15.0	ms
Speed_OVP_Vout	Slow	
V_outOV	50.0	V
V_out_dim_min	15.0	V
V_out_start	14.0	V
EN_UVP_Vout	Enabled	
V_outUV	5.0	V
EN_Iout_max_avg	Enabled	
I_out_max_avg	1200.0	mA
EN_Iout_max_peak	Enabled	
I_out_max_peak	2000.0	mA
V_in_type	AC	
EN_UVP_In	Enabled	
EN_OVP_In	Enabled	
V_inOV	305.0	V
V_in_start_min	72.0	V
V_inUV	65.0	V

Figure 20 Protections

[1] A more detailed description of these parameters can be found in the ICL8105 Target Datasheet.

Parameter Handling / Recommendations

Table 3 Protection Parameters

Parameter	Description
t_start_max	Timeout for a short at startup. This time has to be selected to be shorter than the minimum time the VCC voltage can be kept over the V_UVOFF threshold. Otherwise, the system will auto-restart due to loss of VCC.
Speed_OVP_Vout	Speed of auto-restart for output overvoltage reaction. Can be selected to be either slow (using t_auto_restart) or fast (using t_auto_restart_fast).
V_outOV	Output overvoltage threshold, refer to **Figure 21**.
V_out_dim_min	Minimum output voltage when fully dimmed. This must be higher than V_out_start, refer to **Figure 21**.
V_out_start	Output voltage to start constant current control loop. During dim-to-off with output voltage, this output voltage is maintained to power a current-sink dimmer (refer to **Figure 21**).
EN_UVP_Vout	Enable or disable for output undervoltage protection.
V_outUV	Output undervoltage threshold, refer to **Figure 21**.
EN_Iout_max_avg	Enable or disable for maximum average output current protection over one line half cycle.
I_out_max_avg	Maximum average output current (over one half line cycle) protection threshold. This threshold has to be higher than the nominal output current I_out_set.
EN_Iout_max_peak	Enable or disable for maximum peak output current protection.
I_out_max_peak	Maximum peak output current protection threshold. This threshold has to be higher than the nominal output current I_out_set.
V_in_type	Input voltage type. Please select either AC or DC. This is required to calculate the correct protection thresholds for the input voltages.
EN_UVP_In	Enable for Input undervoltage protection
EN_OVP_In	Enable for Input overvoltage protection.
V_inOV	Maximum input voltage for startup (RMS in the case of AC); refer to **Figure 23**.
V_iN_start_min	Minimum input voltage for startup (RMS in the case of AC). "Brown-in voltage", refer to **Figure 23**.
V_inUV	Minimum input voltage for shut-off (RMS in the case of AC). "Brown-out voltage", refer to **Figure 23**.

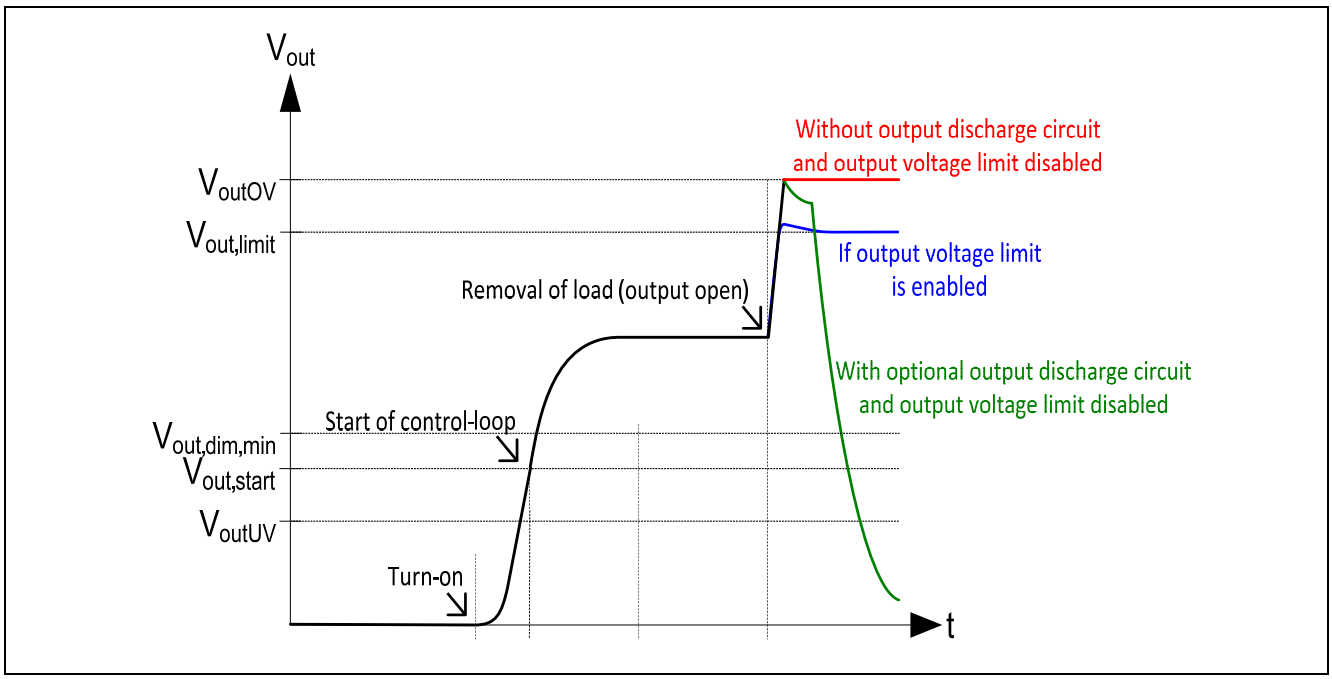


Figure 21 Output Voltage Limits

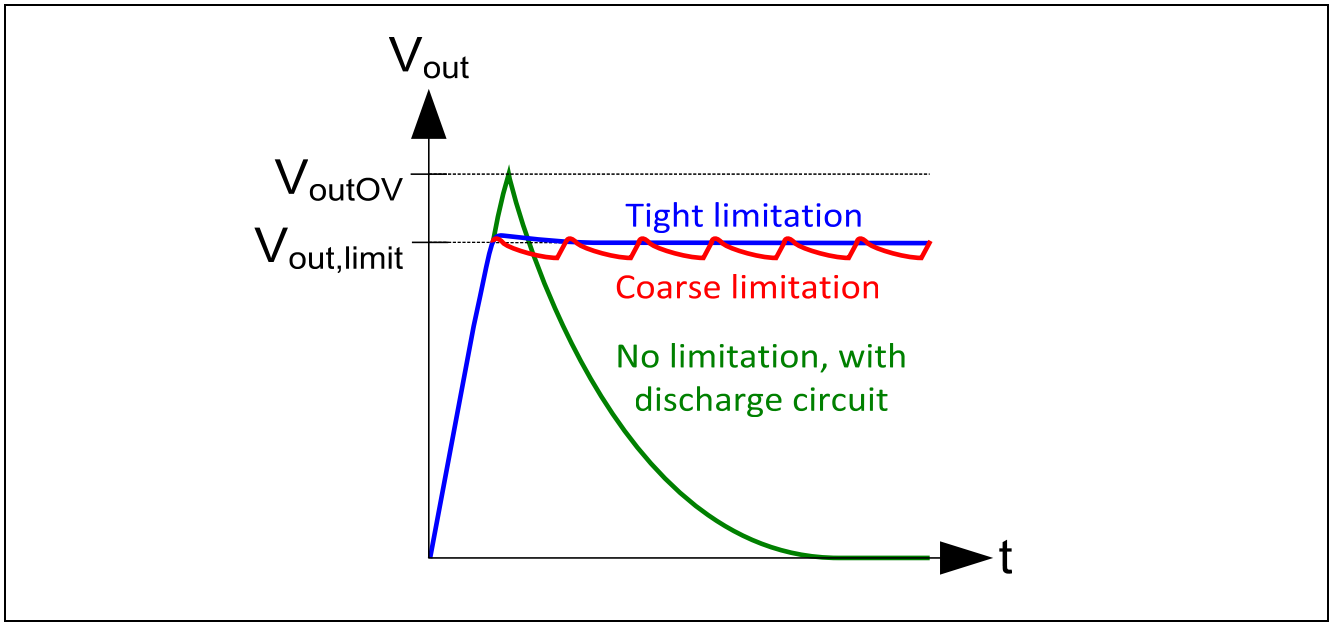


Figure 22 Vout Limitation

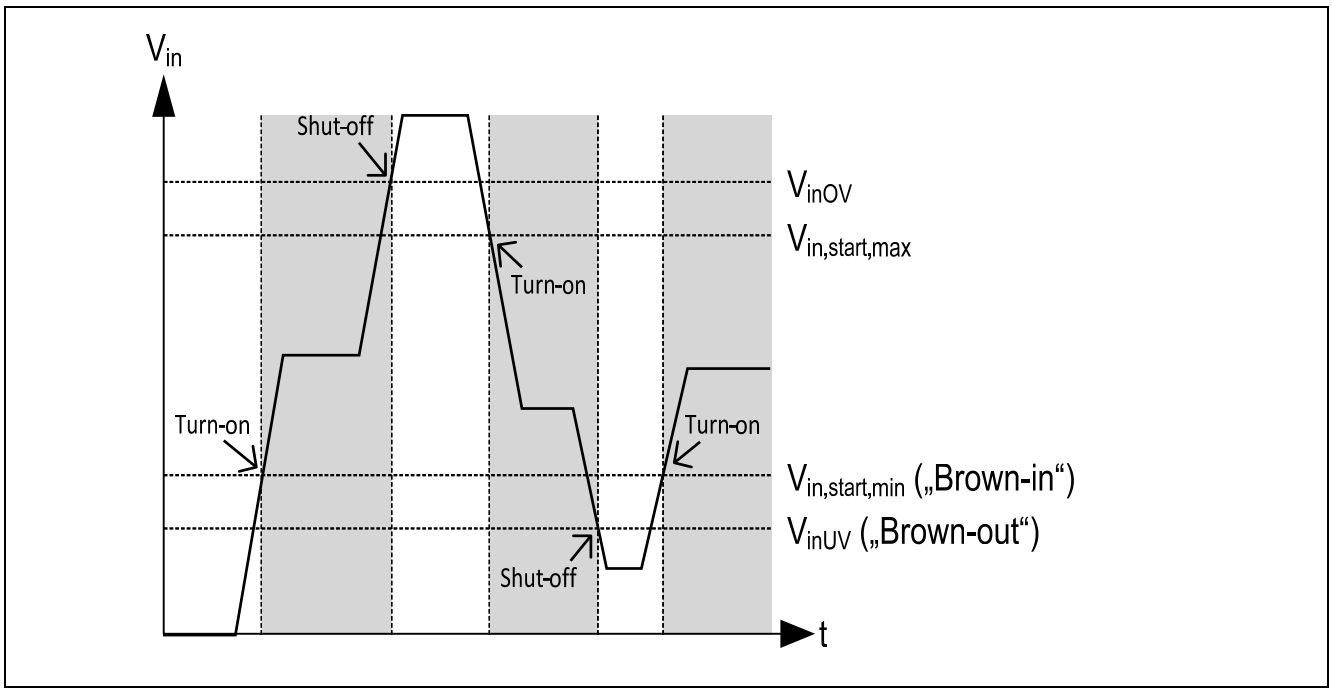


Figure 23 Vin Protections

3.1.3 Temperature Guard

This section allows the user to set the value and reaction for temperature protection. It is necessary to enter the values of temperature thresholds that define the device's behavior regarding operating temperature conditions.

Temperature guard		
EN_TempP	Enabled	
T_critical	110	degreeC
EN_ITP	Enabled	
T_hot	100	degreeC
I_out_red	200.0	mA
t_step	1	s

Figure 24 Temperature Guard

Table 4 Conventional Temperature Protection Parameters

Parameter	Description
EN_TempP	Allows the user to enable or disable the overtemperature protection. By default, when overtemperature protection is activated, the IC will go into latch mode.
T_critical	Junction temperature threshold for overtemperature protection ("Critical Temperature").

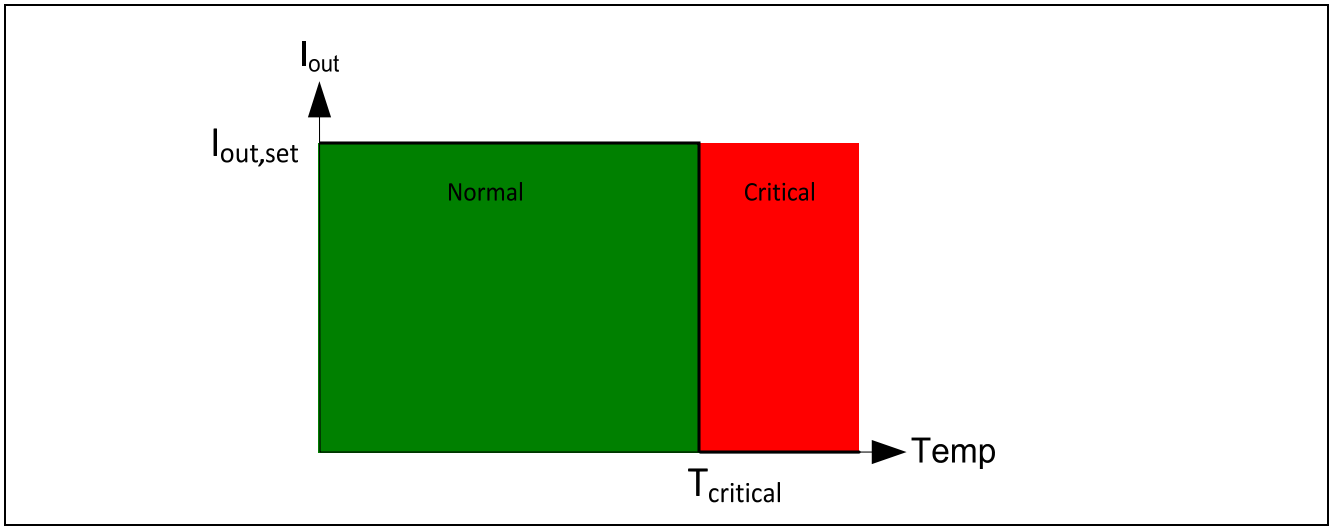


Figure 25 Overtemperature Protection

Parameter Handling / Recommendations

In addition to the conventional temperature protection, the ICL8105 also features an advanced internal temperature guard. The parameters of this feature are given in **Table 5** and depicted in **Figure 26** and **Figure 27**.

Table 5 Advanced Temperature Protection Parameters

Parameter	Description
EN_ITP	Allows the user to enable or disable the advanced internal temperature guard.
T_hot	If the junction temperature exceeds this threshold, the controller will start derating the output current. The derating will either stop if the temperature stabilizes at T_hot or if the minimum output current **I_out_red** is reached (**Figure 26**).
I_out_red	Minimum output current for internal temperature protection derating
t_step	Internal temperature protection derating time for the output current

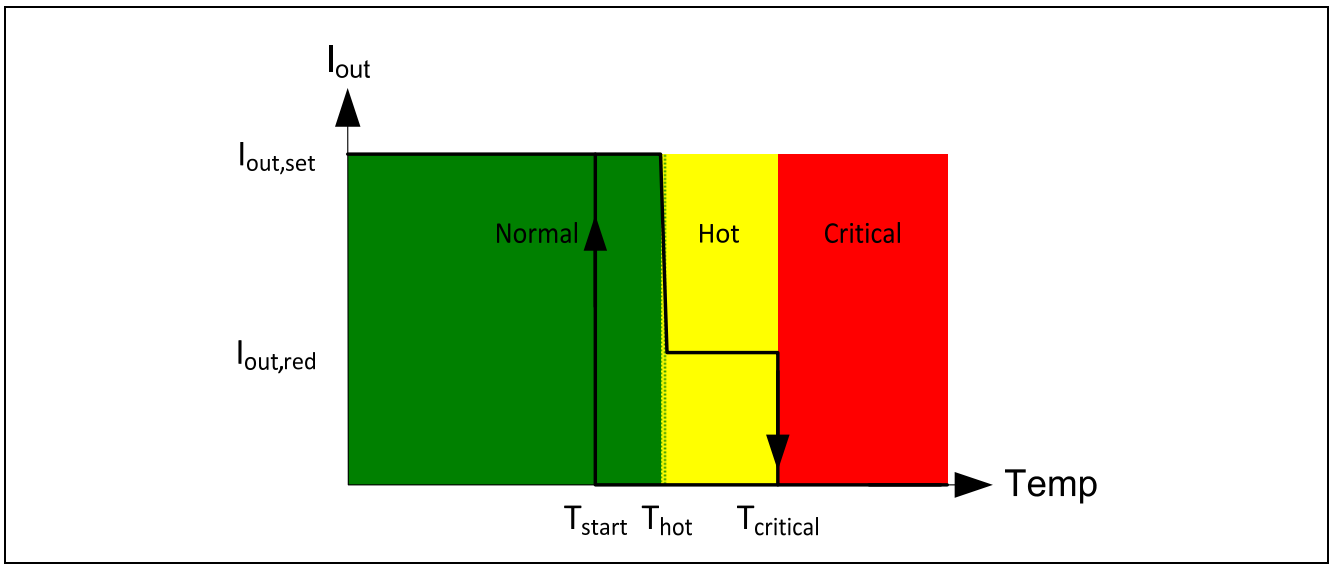


Figure 26 Internal Temperature Protection

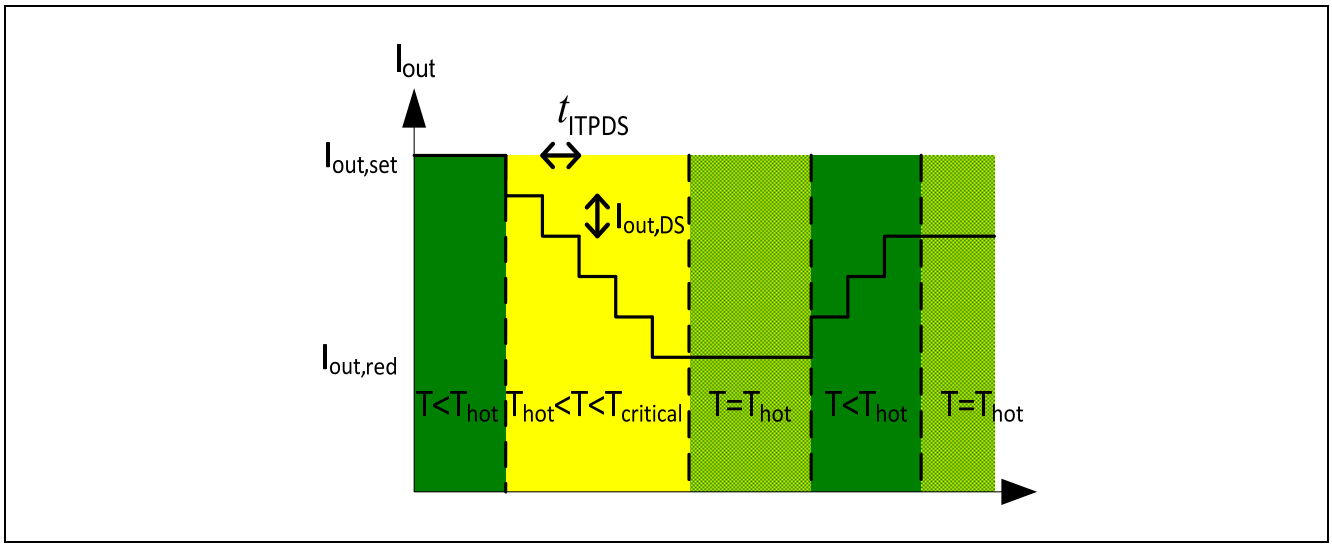


Figure 27 Output Current Derating Step

3.1.4 Startup & Shutdown

For startup and shutdown only one parameter is available, as shown in **Figure 28**. The **t_ss** defines the time per soft-start step.

Startup & shutdown		
t_ss	0.50	ms

Figure 28 Startup & Shutdown

Figure 29 shows the sequence of startup if the output was fully discharged. By default, a number of $n_{ss} = 4$ steps are used. If the output is still charged above $V_{out,start}$ at startup time (e.g. because of a previous operation), the startup will be skipped and the system enters regulated mode immediately.

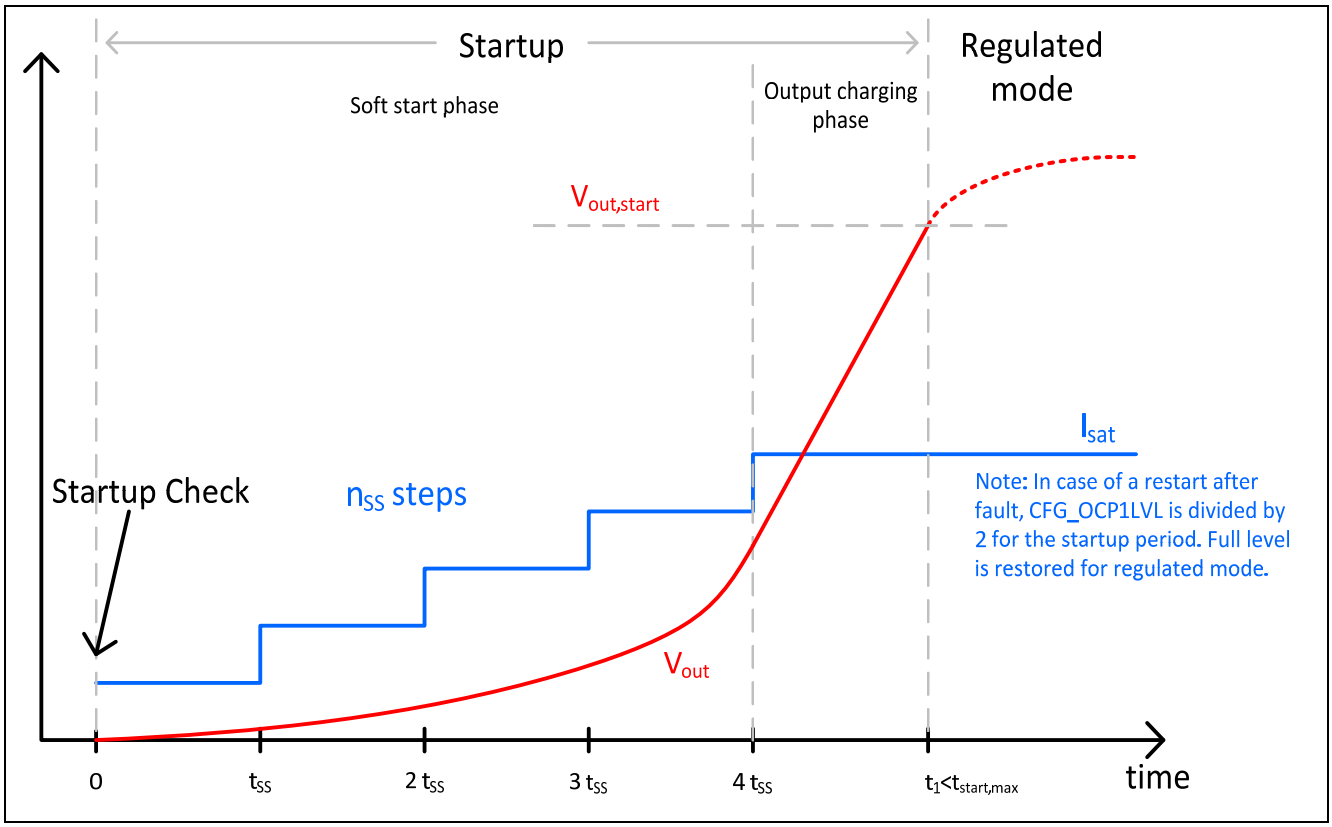


Figure 29 Startup & Shutdown

3.1.5 Dimming

This section allows users to define the parameters related to the dimming function. If the feature is enabled, the ICL8105 will sense the voltage level at the DIM/UART pin and change the output current accordingly (see **Figure 30**).

The human eye is subject to the logarithm of the light power (Weber-Fechner law). As a consequence, the quadratic dimming curve on the right of **Figure 30** creates a more equally dimming experience to the human eye. It is therefore recommended to be used in combination with, for example, 0 – 10 V wall dimmers. If the dimming voltage is provided by an external source (e.g. a microcontroller for DALI), the linear curve on the left of **Figure 30** can also be selected.

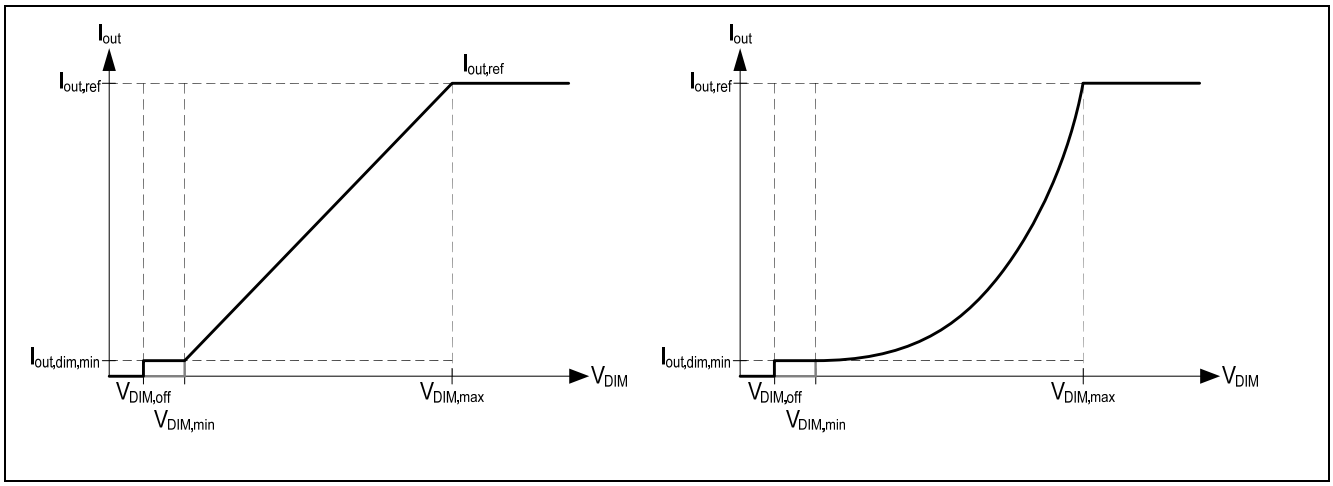


Figure 30 Relation of Dimming Voltage and Output Current

For applications which require an isolated dimming input, the ICL8105 can provide a square wave voltage signal to transfer the dimming voltage from an isolated input. If enabled, the SQW pin will output a 50% duty cycle square wave signal with 160 KHz and 7.5 V while the IC is not in auto-restart or latch mode.

Table 6 Dimming Parameters

Parameter	Description
EN_DIM	Allows the user to enable or disable the dimming via the DIM/UART pin.
I_out_dim_min	Minimum output current (at full dimming level). The lowest achievable output current may be limited due to operating conditions. The minimum output current must be at least 10 mA or 1 % of the nominal output current.
C_DIM	Allows the user to select either the linear or quadratic dimming curve.
EN_SQW	Allows the user to enable or disable the square wave output signal at the SQW pin.

Parameter Handling / Recommendations

For applications in which no hard wall switch is available to turn off the light completely, the ICL8105 provides a dim-to-off feature. If enabled, the ICL8105 will turn off the output current if a dimming voltage of lower than $V_{DIM,off}$ is sensed. The output current will be turned on again if the dimming voltage exceeds $V_{DIM,min}$ again.

Note: Turning on with a low secondary side current will charge the output caps rather slowly. This typically causes an increased time-to-light for dimmed operation.

In some applications, the dimmer is supplied by the output of the driver (e.g. current-sink dimmer). This requires keeping a minimum output voltage to provide power to the dimmer. The ICL8105 includes a feature which can maintain an output voltage of $V_{out,start}$ while the driver is in the dim-to-off state (see **Figure 31**). The driver will recharge the output to this voltage level every 400 ms.

Note: The Dim-to-Off feature with maintenance of output voltage requires an active bleeder circuit (see Chapter 2.17).

Note: The minimum LED voltage with out light has to be sufficiently larger than the resulting Dim-to-Off voltage at worst case conditions (highest input voltage and highest input frequency).

In applications where the dimming voltage is provided to the ICL8105 by a voltage source; maintenance of a minimum output voltage is not required. The feature can be disabled to reduce power consumption.

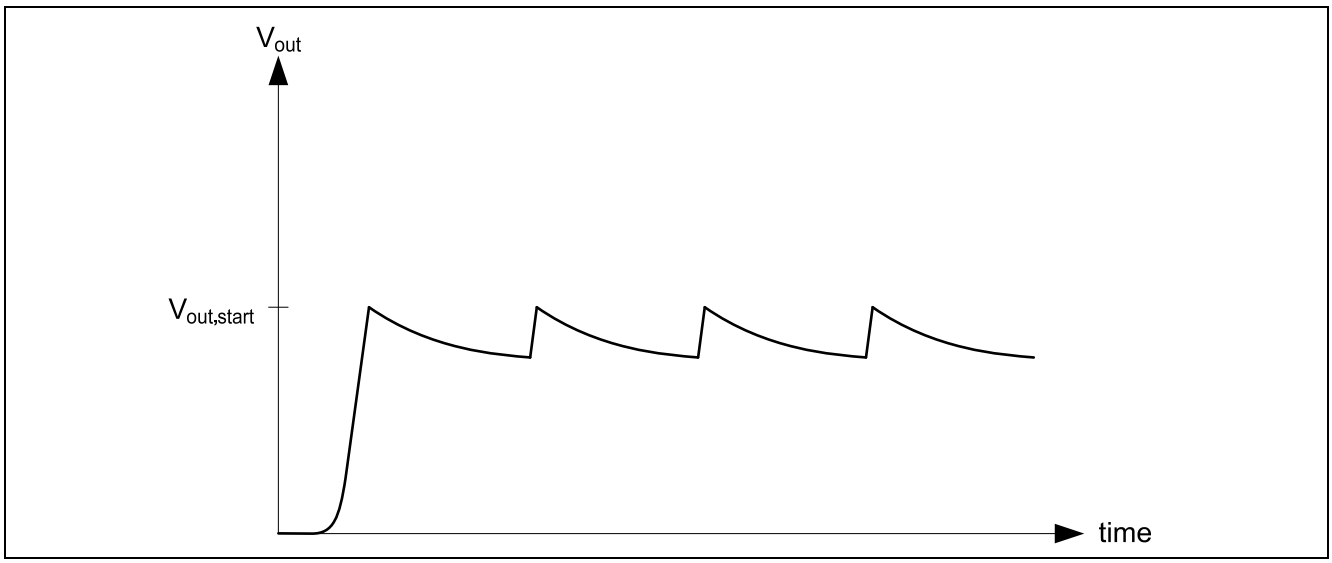
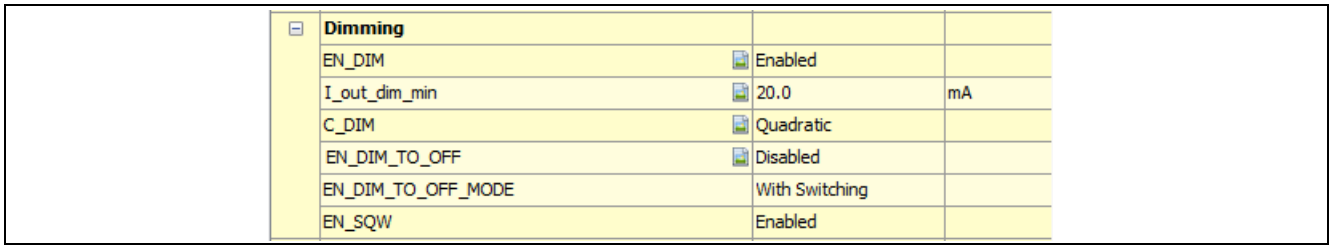


Figure 31 Output Voltage in Dim-to-Off to Maintain a Supply for a Current-Sink Dimmer

Table 7 Dimming Parameters for Dim-to-Off

Parameter	Description
EN_DIM_TO_OFF	Allows the user to enable or disable the dim-to-off feature.
EN_DIM_TO_OFF_MODE	Allows the user to enable or disable a minimum output voltage during the dim-to-off state.

Figure 32 shows a summary of exemplary settings of dimming parameters in .dp vision as used on the ICL8105 form factor board.

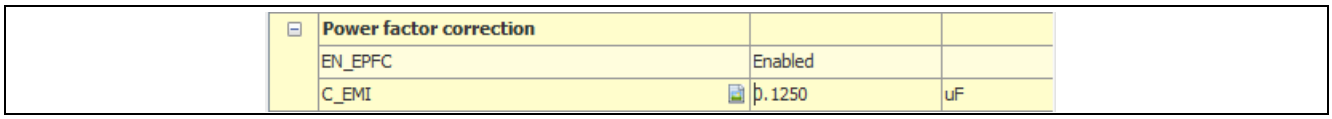


Dimming		
EN_DIM	Enabled	
I_out_dim_min	20.0	mA
C_DIM	Quadratic	
EN_DIM_TO_OFF	Disabled	
EN_DIM_TO_OFF_MODE	With Switching	
EN_SQW	Enabled	

Figure 32 Dimming Parameters in .dp vision

3.1.6 Power Factor Correction

As mentioned in Section Figure 4, an enhanced PFC (EPFC) scheme can be enabled to compensate for the penalty of the input filter cap on power factor and THD and thus improve them. Figure 33 and Table 8 show the parameters for this feature.



Power factor correction		
EN_EPFC	Enabled	
C_EMI	0.1250	uF

Figure 33 Power Factor Correction

Table 8 Enhanced PFC Parameters

Parameter	Description
EN_EPFC	Allows the user to enable the enhanced PFC feature. This feature improves the power factor for high output power only (when the controller is in QRM).
C_EMI	Capacitance after the rectifier. The enhanced PFC compensates the impact of C_EMI on power factor and THD. The value can be adjusted to optimize for either power factor and/or THD. As a consequence, the optimum value can differ from the actually used C_EMI.

The parameter C_EMI can be optimized using the following steps:

1. Switch off “Enhanced Power Factor Correction” by setting C_EMI = 0.
2. Set the input voltage to a high value close to the maximum value and select an operation point with medium high power (e.g. 80 % output power).
   a. To optimize for power factor: Change C_EMI while measuring reactive power.
      i. If reactive power decreases when C_EMI is increased, keep increasing C_EMI further.
      ii. If reactive power increases when C_EMI is increased, decrease C_EMI.
   b. To optimize for THD: Change C_EMI while measuring THD.
      i. If THD decreases when C_EMI is increased, keep increasing C_EMI further.
      ii. If THD increases when C_EMI is increased, decrease C_EMI.
3. Depending on your application requirements, choose either the result from 2a) or from 2b) or a value inbetween for a trade-off between PF and THD optimization.

3.1.7 Fine-tuning

The parameters in **Figure 34** and **Table 9** compensate for parasitic elements of the hardware. They allow better performance to be achieved for the target application.

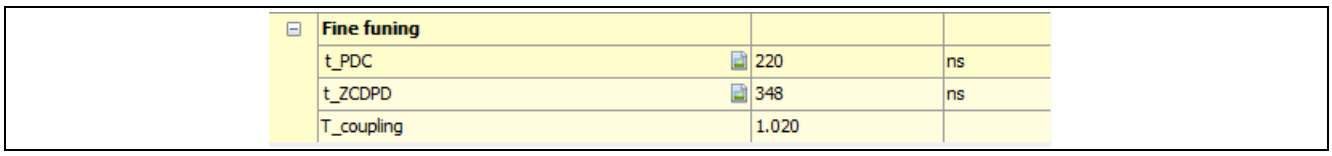


Figure 34 Fine-tuning

Table 9 Fine-tuning Parameters

Parameter	Description
t_PDC	Propagation delay compensation. Due to the capacitances of the MOSFET, the drain current will still rise after the gate has turned off. This value therefore affects line and load regulation. A good starting point for optimization is t_PDC [ns] = 5 * C_{oss} [pf] using C_{oss} at V_DS = 100 V.
t_ZCDPD	Compensation for valley switching. This parameter compensates for internal and external delays at the ZCD and GD pins, e.g. from external capacitors. This parameter affects line regulation accuracy.
T_coupling	Transformer coupling. Use this to fine-tune the output current set-point. Typically, the value needs to be slightly smaller than 1. The parameter has no effect on line or load regulation.

Optimization of these parameters is discussed as follows and should be performed in the following order:

1) **Optimization of the Zero-Crossing-Detection delay (t_ZCDPD)**
   This parameter influences the correct turn-on of the main switch in QRM. The parameter also affects current regulation. To optimize this parameter, please use DC input voltage, disable DCM switching frequency modulation and probe the aux winding signal.
   a. Choose a setpoint in which you expect the system to operate in QRM (e.g. maximum output power at minimum input voltage).
      Note: Please ensure that the frequency and on-time limits permit switching in QRM in this point of operation!
   b. Set the parameter t_ZCDPD to 0. The controller will switch too late after the valley occured. By increasing the parameter, the turn-on time can be moved to an earlier point of time.

   The parameter is correctly set if the turn-on of the gate happens exactly in the 1st valley.

2) **Optimization of propagation delay compensation (t_PDC)**
   a. Measure the output current over line voltage:
      i. If the output current drops while increasing voltage, reduce the parameter t_PDC.
      ii. If the output current increases while increasing voltage, increase the parameter t_PDC.

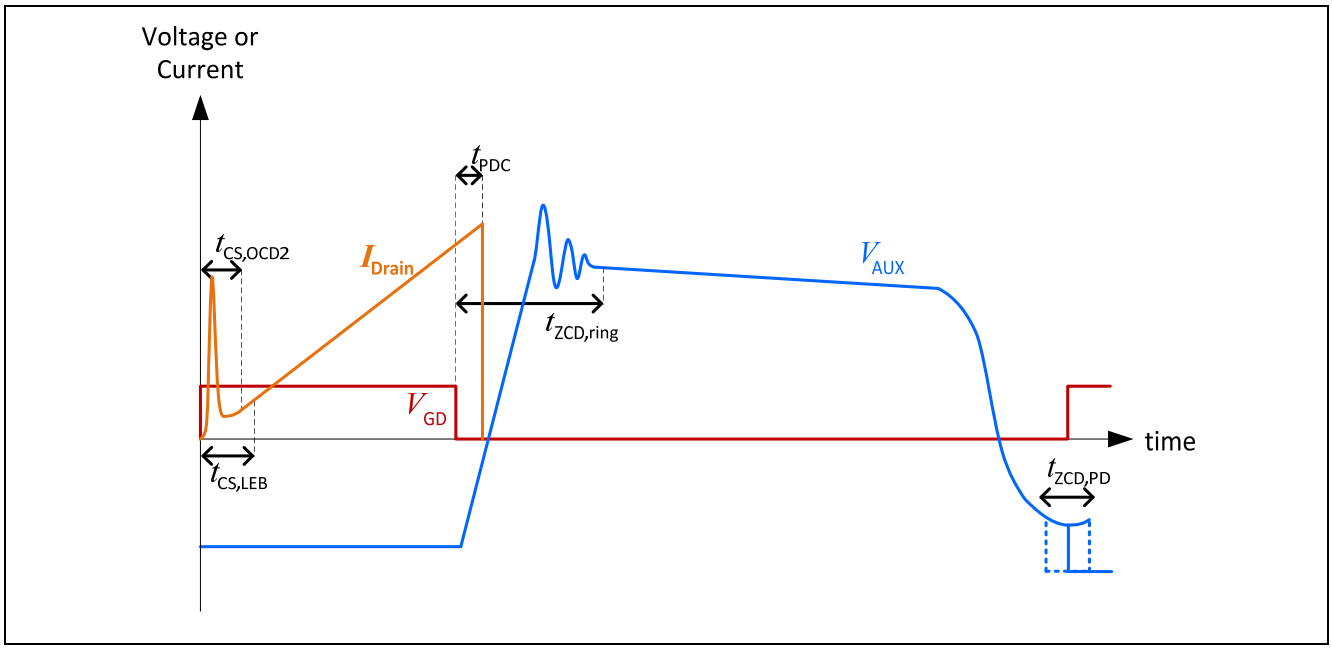


Figure 35 MOSFET and Transformer Voltage and Current Waveforms

3.2 Testing

After all parameters are set, it is necessary to test the application by loading parameters to RAM. Press tab “Functions -> Test Configuration Set” as shown in **Figure 36**. The new parameter values will be automatically loaded to RAM (see **Figure 37**).

Please note that the VCC has to be supplied by an external source (e.g. the interface board) to ensure the parameters are maintained in RAM. If VCC drops below UVOFF or if the IC latches, the parameters in RAM will be lost and need to be reloaded.

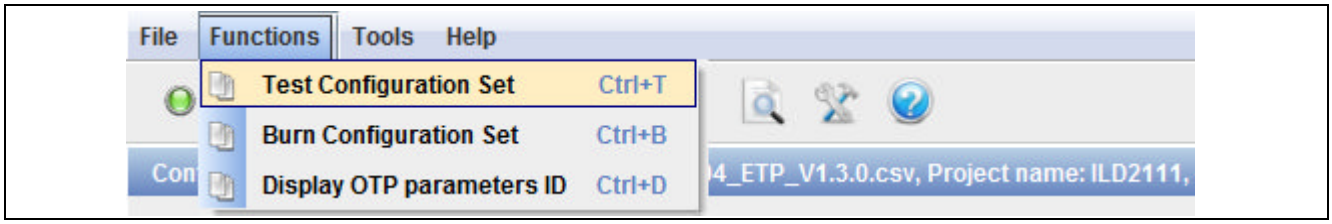


Figure 36 Test Configuration

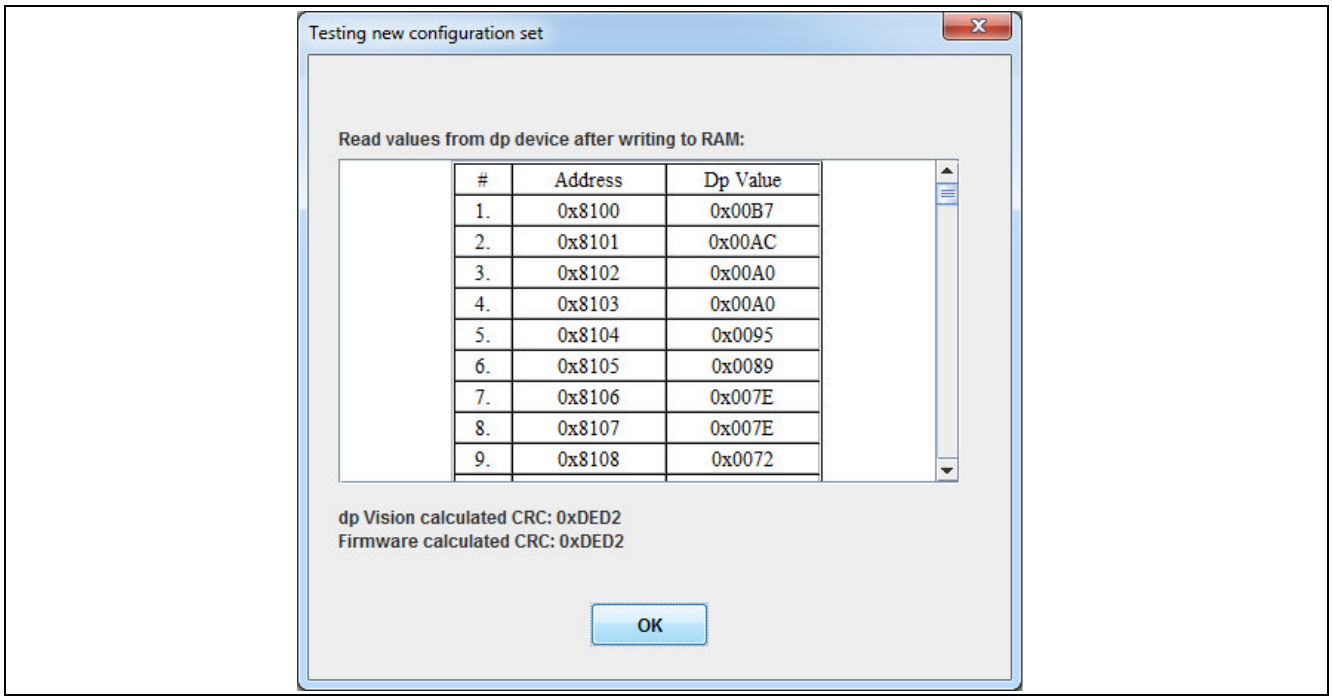


Figure 37 Testing New Configuration Set – Parameters are Downloaded to RAM

After completing these steps, the application can be tested in a real environment. If the behavior of the device meets the previously specified requirements, it is necessary to save a new configuration file (see **Figure 38**) and then burn it to the OTP memory of the chip.

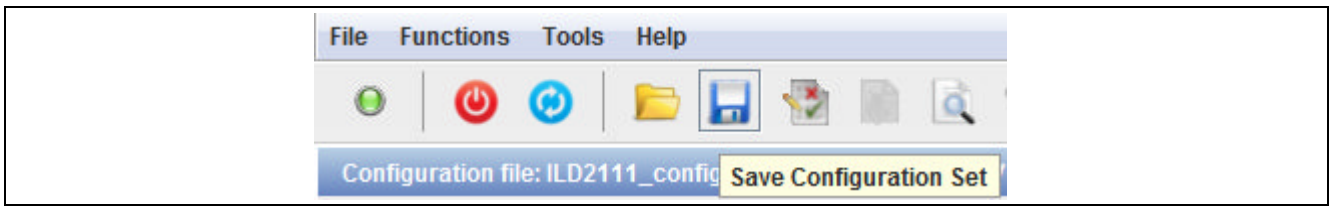


Figure 38 Saving a New Configuration Set

3.3 Burning

The burning procedure is performed using several steps, as shown below:

1. Select “Functions -> Burn Configuration Set” – see **Figure 39**. The differences between values from the chip and current configuration set will be displayed in the appropriate window – see **Figure 40**.
2. Press the “Yes” button to continue. The new configuration will be successfully downloaded to RAM – see **Figure 41**.
3. Press the “Continue burning” button to burn the parameter block to OTP. After successful burning, the appropriate message will appear – see **Figure 42**.
4. For attempts at reburning, the message shown in **Figure 43** will appear.

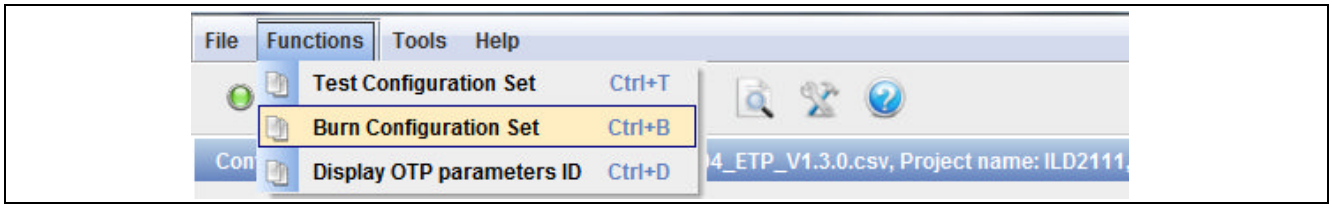


Figure 39 Burning a New Configuration Parameter Set

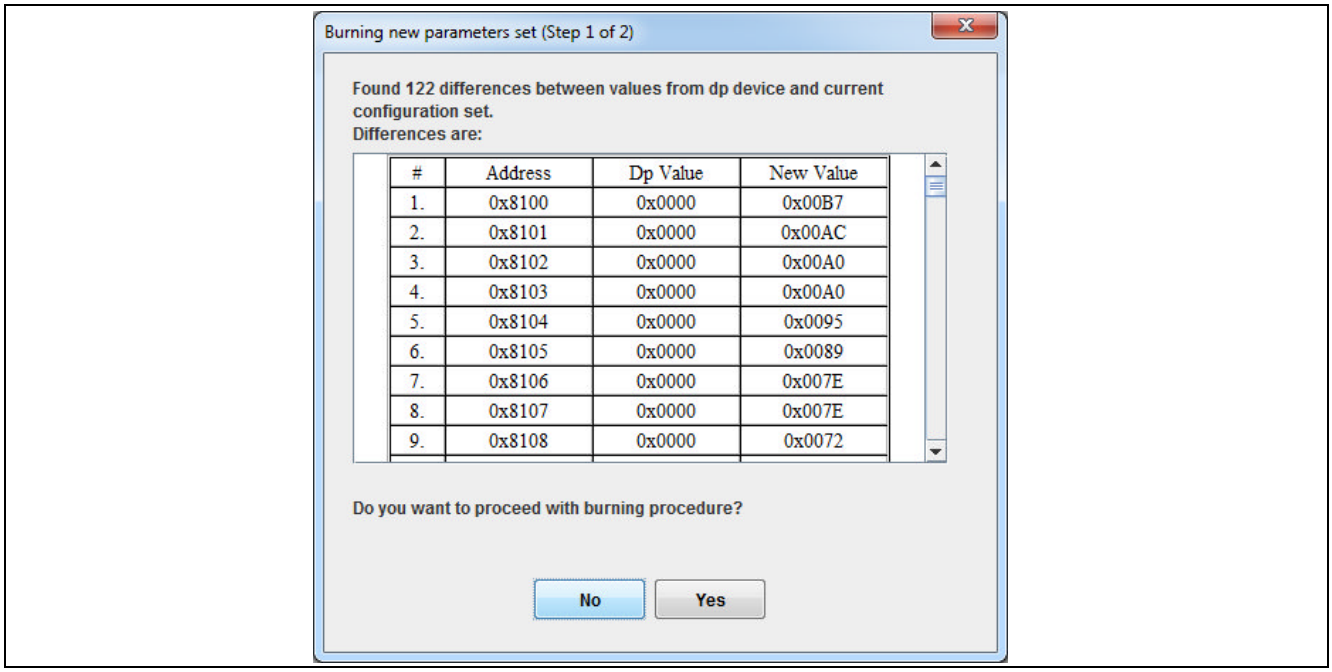


Figure 40 Burning a New Parameter Set – Step 1

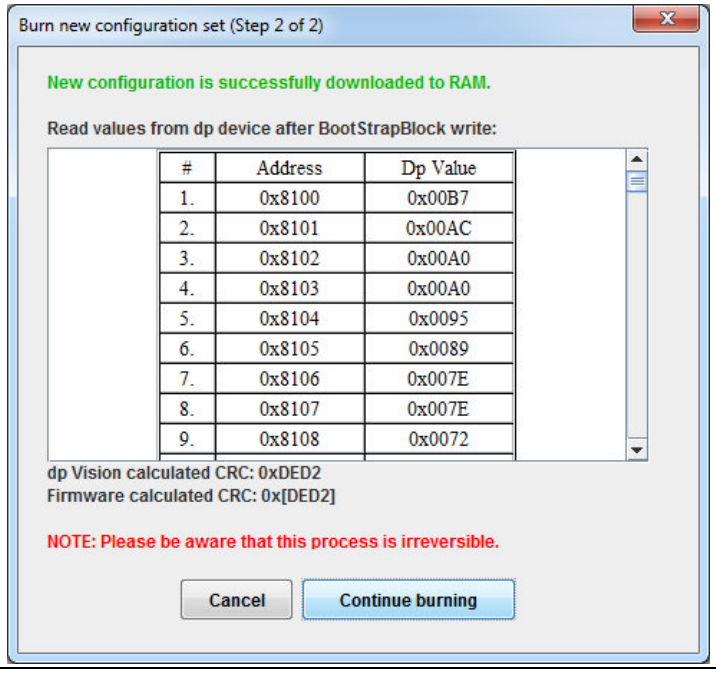


Figure 41 Burning a New Parameter Set – Step 2

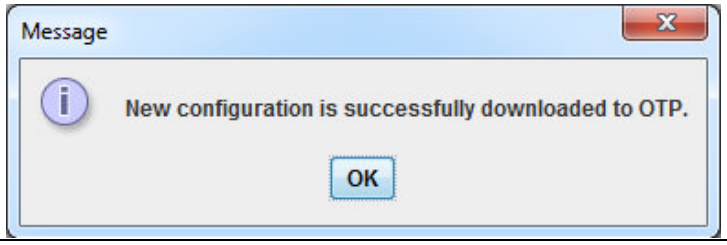


Figure 42 Burning a New Parameter Set – Message

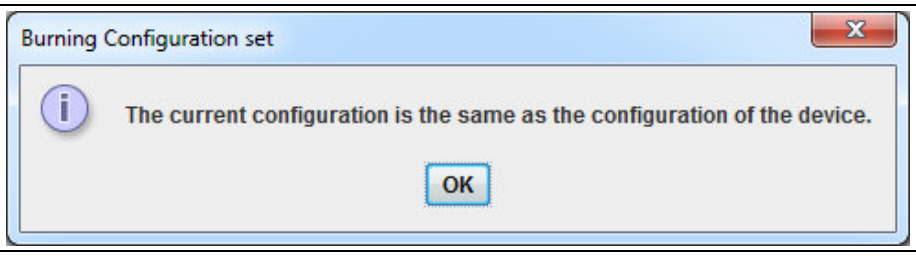


Figure 43 Reburning Configuration Set Attempt Message

3.4 Patching

If the user is not satisfied with the behavior of the device with previously burned parameters (or if the user accidentally made a mistake), or if an error occurred during the burning procedure, there is an option to perform patching. The patching procedure is performed in several steps.

1. Select or change the parameter's value to be patched. In this example, the external temperature protection will be disabled – see **Figure 44**.
2. Save the new configuration set with the changed parameter's value – see **Figure 45** (the configuration set could be saved with a different name). The user can decide if either the existing csv file is to be rewritten or if a new csv file is to be stored with another name – see **Figure 47**. The new configuration file will be saved in the directory whose path is shown in the window message – see **Figure 47**.
3. Select "Functions -> Burn Configuration Set" to burn the appropriate patch – see **Figure 48**. The complete patch structure will be displayed as shown in **Figure 49**. In this figure, the two structures that represent examples of one or two patches can be seen.
4. Press "Continue patching". After this action, the user will be informed that the patching was successful – see **Figure 50**. A list of parameters can also be seen in the same window, including the parameters that were patched in the previous step.
5. If attempting to repatch, the message shown in **Figure 51** will appear.

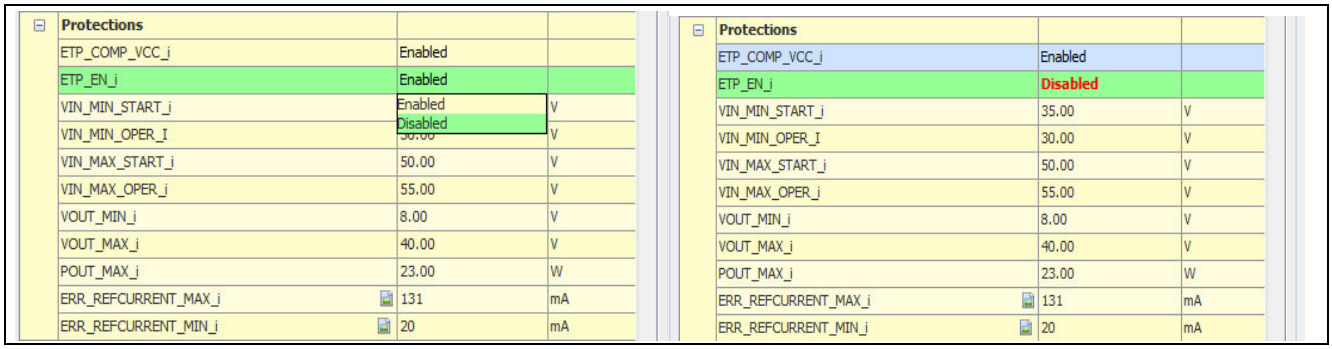


Figure 44 Changing a Parameter's Value

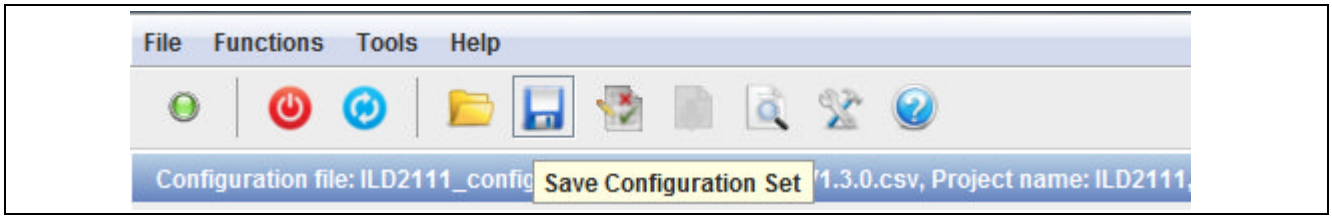


Figure 45 Save New Configuration Set with Changed Parameter's Value

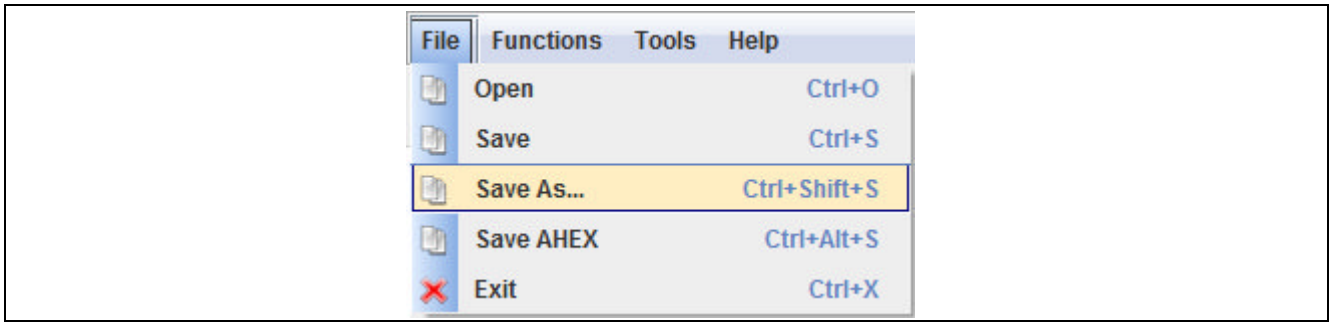


Figure 46 Save New Configuration Set with a Different Name

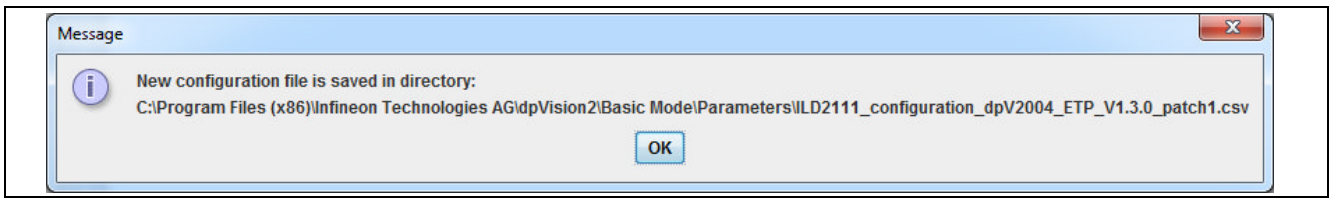


Figure 47 New csv Directory Path

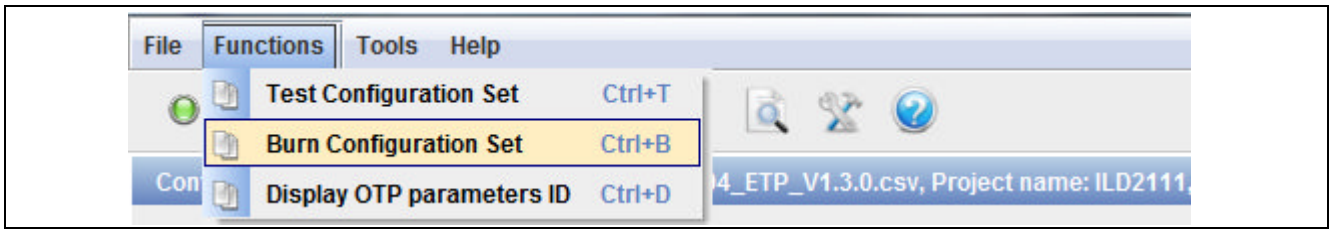


Figure 48 Burning a New Parameter Patch

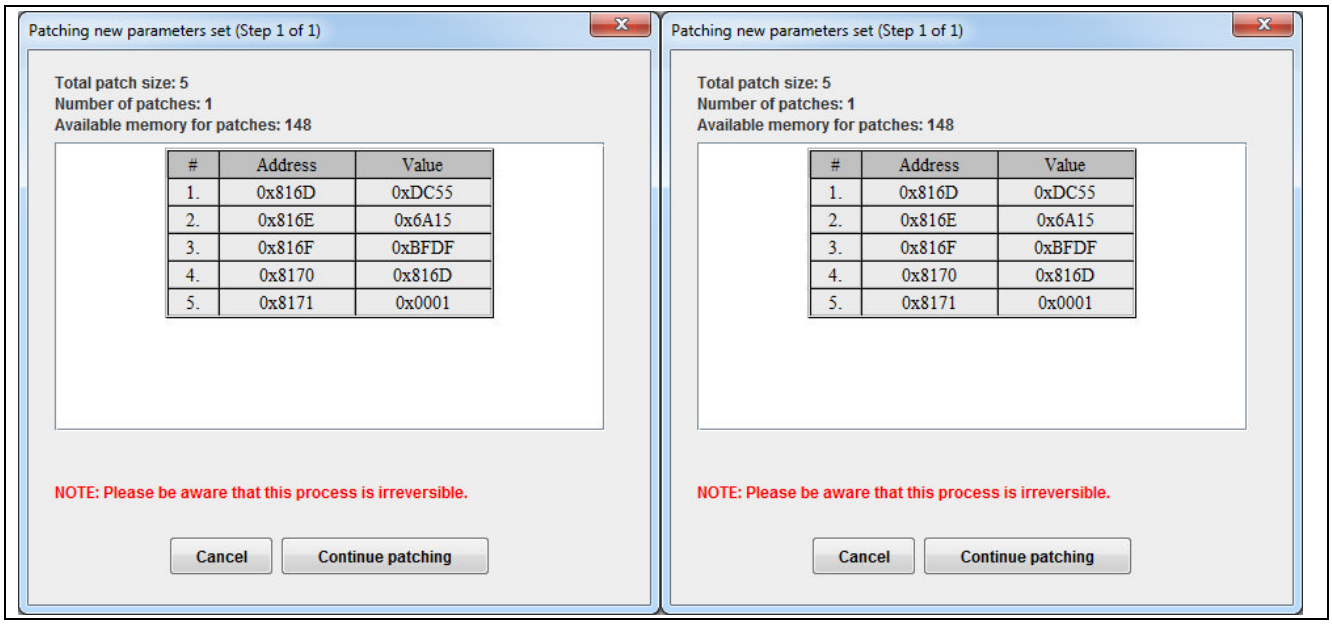


Figure 49 Patch Structure

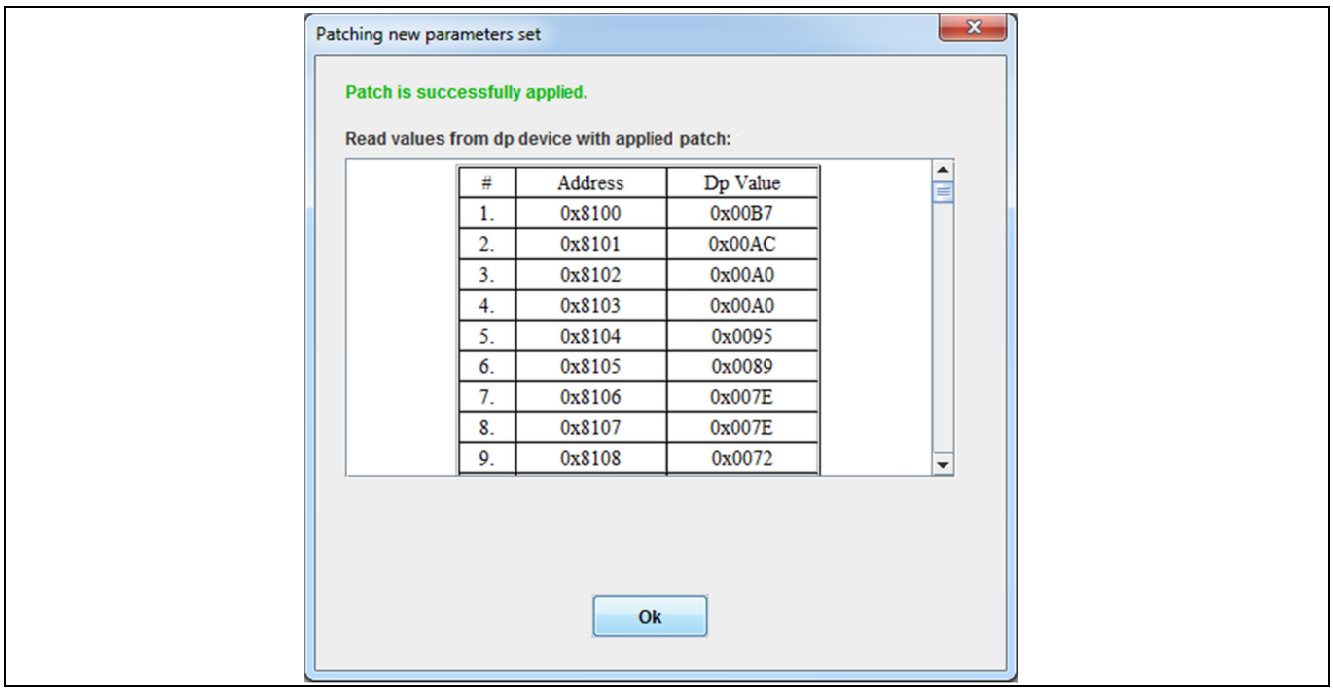


Figure 50 List of Parameter Values with Applied Patch/Patches

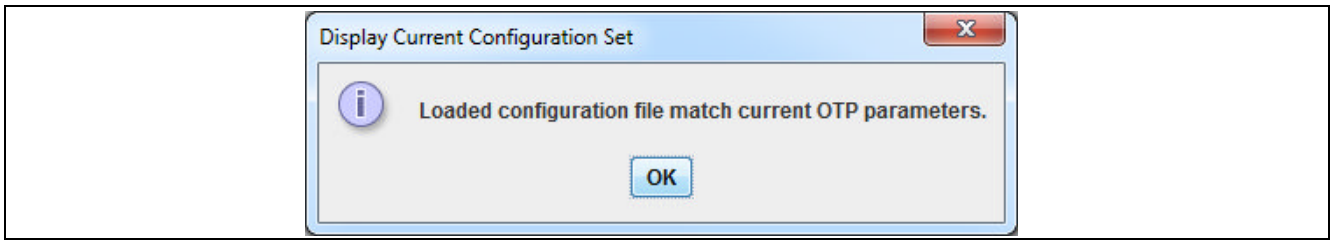


Figure 51 Repatching Configuration Set Attempt Message

4 Frequently Asked Questions

The controller is not switching at the valley, but is expected to be in QRM. What could be the root cause?

A few reasons could cause the MOSFET to not switch on at the valley (intentionally or unintentionally):

1) The output power at the present input voltage would require a smaller on-time than the minimum on-time, thus the controller enters DCM. Please note that the minimum on-time depends on input and output voltage.
2) The output power at the present input voltage would require a higher frequency than allowed for QRM as configured using the GUI, thus the controller enters DCM.
3) The ZCD delay parameter t_ZCDPD is set incorrectly and has to be corrected in the GUI. Please note that this will also cause an offset in the output current.

What can be done if the output current has an overall offset?

The transformer coupling (including the effect of leakage inductance) causes not all energy to be transferred from primary side to secondary side. Parameters T_coupling and L_p_lk can are used in the GUI to determine the correct set point, so the output current is correctly regulated.

Although not being physically possible for the circuit, parameter T_coupling can still be set to a value >1 if desired.

How can the power factor be optimized?

The power factor of a power converter describes how good input voltage and input current is “in sync”. Power factor correction (PFC) in ICL8105 consists of multiple features which contribute to improve the PF:

- Slow control loop:
  The IC regulates the average current over an AC halfwave. The averaging filter makes the control loop rather slow to ignore the halfwave ripple.
- Constant on-time switching:
  Without “enhanced PFC” the ICL8105 will use a quasi-constant on-time during the halfwave. This will ensure a relatively good power factor when the power transfer of the flyback is dominant, e.g. for the following conditions:
    - Low input voltage, and/or
    - High output power

  However, the capacitance behind the bridge rectifier contributes to a capacitative impedence of the full application which is more visible at high input voltage and medium to low output power.
- Enhanced PFC:
  When enabled, the “enhanced PFC” will modulate the on-time in sync with the line frequency. This modulation can compensate the capacitance behind the bridge rectifier. As a result, the power factor is typically improved by a few percent.
  This effect is most visible when operation at rather high input voltage with medium load.
- Modulation of Switching Frequency:
  For AC input voltage when operating under high load in QRM, the application will automatically modulate the switching frequency in sync with the AC frequency due to the quasi-constant on-time. The additional frequency modulation feature in ICL8105 can provide a similar, AC-sync’ed modulation also when operating under low load in DCM. As this shapes the input current of the system, this feature also improves slightly both power factor and THD for low loads.

How can THD be optimized?

The Total Harmonic Distortion (THD) describes the shape of the input current. It is best for a pure sinusoidal shape with only AC frequency. Distorted, non-sinusoidal shapes contain additional higher harmonic frequencies. Typically, power factor and THD are related in most cases, but this is not a must. E.g. a phase shift between a sinusoidal input current and sinusoidal input voltage will have a perfect THD while PF is bad. In another case, a rectangular input current and sinusoidal voltage may be in perfect sync (perfect power factor), but the THD is bad.

The switching element in the flyback can be used to shape the input current while ensuring the required power transfer in average. However, as power can only be transferred from primary to secondary side, there are limits to the current shaping.

In ICL8105, the current can be shaped by two features:

- Enhanced PFC (on-time modulation)
- Switching frequency modulation

By tuning the gain of both features, the improvement of power factor and THD can be traded-off. Often, both cannot be optimized completely at the same time.

Experience from the ICL8105 Evaluation System is:

- THD optimization: Only use a low on-time modulation.
- PF optimization: Use higher on-time modulation.

Note: Too high modulation gain may cause visible flicker!

How to avoid audible noise?

Audible noise can have multiple root-causes:

- Avoid moving parts, e.g. the transformer core, windings.
  ➔ Use a varnished transformer, pot the complete application.
- No not use low-frequency DCM as it uses switching frequencies in the audible range.
  ➔ Use active burst mode.
- The enhanced PFC and switching period modulation are working in sync with the AC frequency. As a consequence, they may cause audible noise with double AC frequency.
  ➔ Disable one or both features or change the gain of the features.
- To enhance brown-in accuracy, the product features a discharge pulse in auto-restart. This can cause a clicking noise in Dim-to-off.
  ➔ Reduce t_pw or set to zero.
- For wide output voltage range applications:
  If the diode between VCC capacitor and VCC regulator is omitted, a bipolar VCC linear regulator may enter reverse-conduction mode during startup. This can cause a chirping noise during auto-restart (e.g. dim-to-off, brownout, etc.).
  ➔ Use a diode to decouple the VCC regulator from the IC’s VCC.

5 References

[1] ICL8105 Datasheet

[2] ICL8105 Universal Evaluation Board Application Note

[3] .dp vision – Basic Mode User Manual

[4] Power Management Selectionguide:
http://www.infineon.com/powermanagement-selectionguide

Revision History

Major changes since the last revision

Page or Reference	Description of change

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Published by

Infineon Technologies AG

81726 Munich, Germany

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AN_201410_PL21_001

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