30 W power supply using CoolSET™ SiP ICE183LM

REF_30W1_ZVS_183LM

About this document

Scope and purpose

This application note describes a switched mode power supply (SMPS) using Infineon's latest CoolSET™ System in Package (SiP) ICE183LM. The power supply is designed for a universal line AC input and an isolated 12 V output.

Intended audience

This document is intended for power supply design, application engineers, or others who want to design efficient and reliable auxiliary power supplies.

Keypoints

- Overall high efficiency to meet energy efficiency requirements
- Zero voltage switching (ZVS) technology to boost efficiency performance and lower the electro-magnetic interference (EMI)
- Ultra-low standby-power consumption (<30 mW)
- Simplified circuitry with high-level integration of power control and protection features
- Auto-restart protection scheme to minimize interruption and enhance the end user experience

About this product family

Product family

Infineon's CoolSET™ AC-DC integrated power stages in fixed frequency and quasi-resonant switching schemes offer increased robustness and outstanding performance. This family offers superior energy efficiency, comprehensive protective features, and reduced system costs. The CoolSET™ controllers are ideally suited for auxiliary power supply applications.

Target applications

- SMPS
- Home appliances
- Server power supply units
- Telecom AC-DC power conversion

Table of contents

1 Introduction

This document describes a 12 V/2.50 A SMPS using Infineon's latest CoolSET™ SiP ICE183LM. This reference design demonstrates high power efficiency, low power consumption, and cost-effectiveness, made possible by the high-level integration capabilities of CoolSET™ SiP.

Table 1 lists the general system requirement for a power supply and the Infineon solution using ICE183LM.

Table 1   **General system requirement and reference design solution**

S.No.	General system requirement	Reference design solution – ICE183LM
1	High efficiency to meet energy efficiency requirements	Primary zero voltage switching and secondary optimal synchronous rectifier (SR) control
2	Low standby power consumption to comply to latest energy conservation standards	Optimized low supply currents for hysteretic mode operation to reach lowest stand-by power < 30 mW
3	Simplified circuitry with high-level integration	Integrated primary 800 V MOSFET, primary and secondary controller, and communication in a DSO-27 package
4	Minimize interruption to enhance end user experience	All protections are defined to enter auto-restart mode

2 Reference board

This document provides complete design details including power supply specifications, schematics, bill of materials, PCB layout, transformer specification, and performance data.

Top side of the board

Bottom side of the board
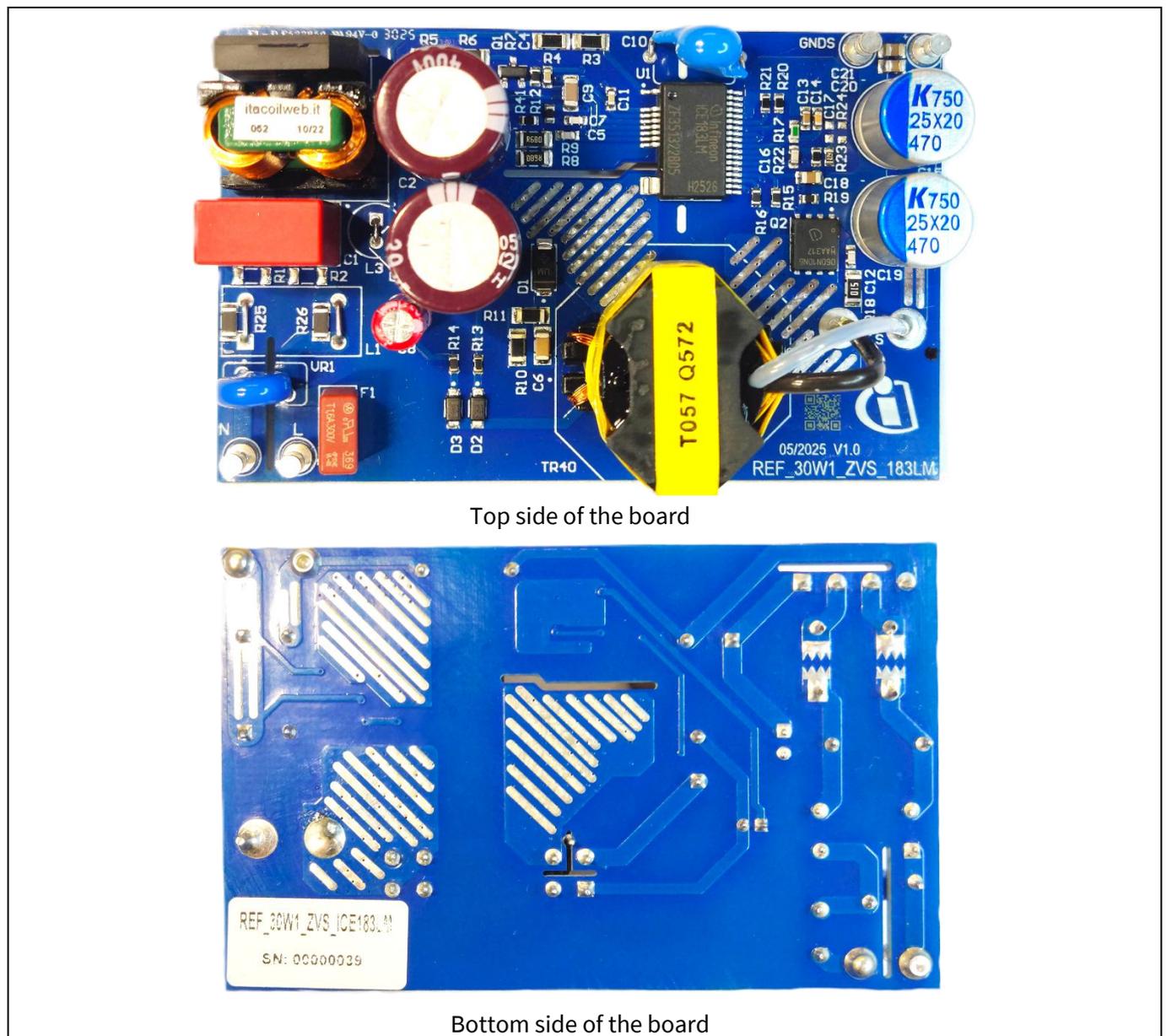
Figure 1   Reference board REF_30W1_ZVS_183LM

3 Power supply specifications

The following table represents the minimum acceptance performance of the design. The actual performance is listed in the Measurement data and graphs section.

Table 2 Specifications of REF_30W1_ZVS_183LM

Description	Symbol	Min.	Typ.	Max.	Units	Comments
Input						
Voltage	V_{IN}	90	–	264	V AC	Live (L) and Neutral (N) (no PE)
Frequency	f_{LINE}	47	50	64	Hz	–
Line overvoltage	V_{IN_OVP}	–	268	–	V AC	–
Output						
Output voltage	V_{OUT}	–	12	–	V	±1 percent (isolated)
Output current	I_{OUT}	–	2.50	–	A	–
Output voltage ripple	V_{RIPPLE}	–	–	240	mV	Peak to peak
Overcurrent protection	I_{OCP}	–	–	3.6	A	Measured at 230 V AC
Total output power	P_{OUT}	–	30	–	W	–
Efficiency						
Maximum load efficiency	η	–	92.7	–	%	Measured at 230 V AC
Environmental						
Conducted EMI	–	6			dB	Margin, CISPR 14
ESD						EN 61000-4-2
Contact discharge	–	±8			kV	–
Air discharge	–	±15			kV	–
Surge immunity						EN 61000-4-5
Differential mode	–	±2			kV	–
Common mode	–	±4			kV	–
PCB size	–	80 x 50			mm^2	L x W
Ambient temperature	Ta	–	–	50	°C	Convection cooling

4 Circuit diagram

Figure 2   Schematic of REF_30W1_ZVS_183LM

5 Circuit description

This section briefly describes the reference design circuit by different functional blocks. For more information on the design procedure and component selection for the flyback circuitry, see the IC datasheet [1] and design guide [2].

5.1 EMI filtering and line rectification

- The input of the power supply is taken from the AC power grid, which is in the 90 V AC ~ 264 V AC range
- The F1 fuse is right at the AC input to protect the system in case of excess current entering the system circuit due to a fault
- Following is the varistor VR1, which is connected across L and N to protect the system in case of a line surge transient event
- Common mode (CM) chokes L1 (jumped via R25, R26), L4 and the X-capacitor C1 form a basic filter to reduce the differential mode (DM)- and common mode (CM)-conducted EMI noise
- The bridge rectifier BR1 rectifies the AC input into DC voltage, filtered by the π-filter composed of capacitors C2, C3, and inductor L3

5.2 CoolSET™ SiP power stage

The flyback converter power stage consists of:

- Power transformer
- Primary power MOSFET
- Secondary synchronous rectifier (SR) MOSFET
- Secondary output capacitors
- Filtering components

The primary side and secondary side power management are separated for isolated power supply domains (VCCP, GNDP) and (VCCS, GNDS). CoolSET™ SiP ICE183LM controller IC provides reinforced and safe isolated communication between the primary and secondary sides.

5.2.1 CoolSET™ SiP primary side

CoolSET™ SiP ICE183LM integrates a 950 V startup cell and 800 V power MOSFET together in the primary side. The IC is self-starting through the startup resistors (R3, R4) in series with the HV pin – to charge the VCCP pin capacitors (C8, C9, and C11) when AC is applied at the input of the board. The primary winding start-terminal of the transformer (TR40) is connected to the drain of the CoolMOS™ MOSFET inside ICE183LM (U1). When the integrated CoolMOS™ turns on, energy is stored in the transformer. When it turns off, the stored energy is released to the output capacitors and output loading through the output SR MOSFET Q2.

Resistors R5, R6, and R7 are used for the input overvoltage protection (OVP) of the system, at pin VINP of U1. An additional power MOSFET (Q1) is used for achieving ultra-low standby power consumption. Q1 is switched on for very short periods, only when the input voltage reading is done at the VINP pin. Shunt resistors R8 and R9 serve as ICE183LM primary current sensing, to limit the peak current cycle by cycle.

A low-cost RCD clamp consisting of the diode D1, the resistors R10, R11, and the capacitor C6 is implemented to suppress the drain voltage spike that appears when the integrated CoolMOS™ power switch is turned off. This passive snubber helps to dissipate the energy stored in the transformer leakage inductance.

5.2.2 CoolSET™ SiP secondary side

The secondary side of CoolSET™ SiP ICE183LM starts to take over the PWM control when output voltage reaches 95% of its regulation target. The ICE183LM PWM control is based on the voltage at the pin ZCDS and on the error amplifier output EA voltage. ICE183LM integrated PWM and SR control ensures that the timing of the SR power switch (Q2) and the primary side power switch is well-synchronized, which avoids the cross conduction of the two switches and provides reliable and efficient synchronous rectification.

In addition, the current injection function via the SR power switch Q2 enables zero voltage switching operation on the primary side.

- Two external resistors, R20 and R21 are used to configure the IC with the transformer turns ratio and the desired preset of operation parameters
- C13, C14, and R17 form compensation network to stabilize the output voltage regulation
- Output filtering capacitors C15 and C19 are dimensioned to keep the output voltage ripple in the specified limits, working together with the ceramic capacitors C20 and C21 that are used to reduce the high frequency output voltage ripple

6 PCB layout

The REF_30W1_ZVS_183LM consists of a standard 2-layer PCB with only top side placement. The PCB prints are shown in the following figures.
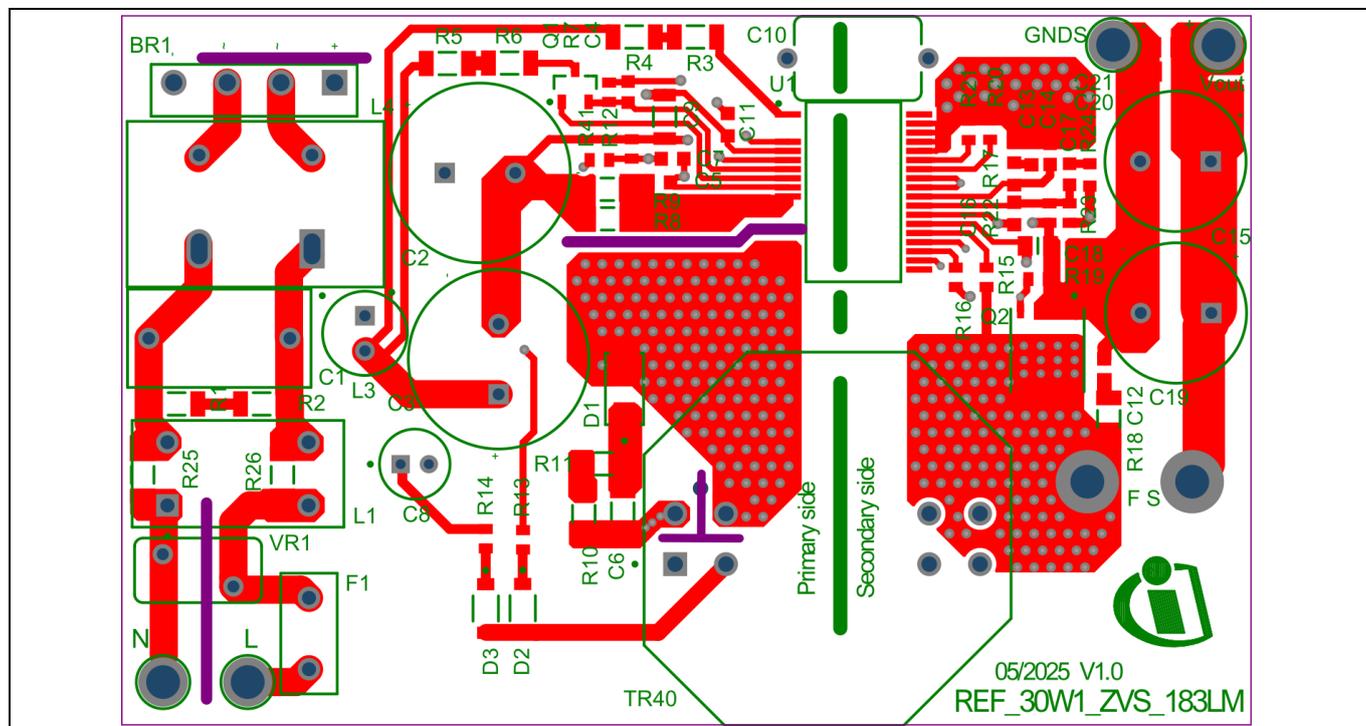
Figure 3   Top-side PCB
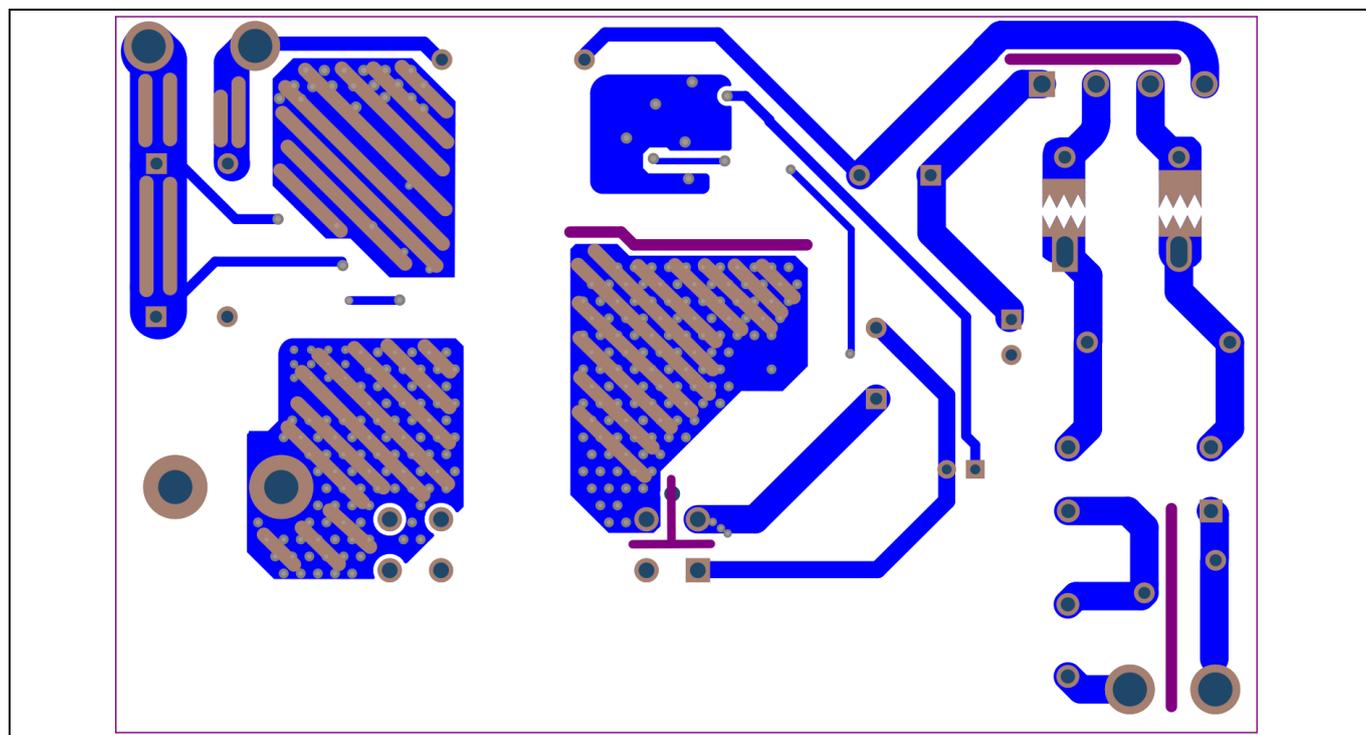
Figure 4   Bottom-side PCB

PCB layout

A good PCB layout is crucial for a successful design. Following are some recommendations:

1. Minimize the loop area with pulse shape current or voltage, such as the loop formed by the bus voltage source, primary winding, main power switch, and current sense resistor or the loop consisting of the secondary winding, SR switch, and output capacitor, or the loop of the V_{cc} power supply

2. **Star connection of the primary side ground (GNDP) at the bulk capacitor**: All primary grounds should be connected to the ground of the bulk capacitor C2 and C3 separately at one point. This can reduce the switching noise entering the sensitive pins of the CoolSET™ SiP device. The primary star ground can be split into four groups:
   – Combined signal (all small signal grounds connecting to the controller GNDP pin such as the filter capacitor C2, C3, and C9) and power ground (CS resistors R8 and R9)
   – V_{CCP} ground includes the V_{CCP} capacitor C9 ground and the auxiliary winding ground, pin 1 of the power transformer
   – EMI return ground includes the Y-capacitor C10 for isolated flyback application
   – DC ground from the bridge rectifier BR1
   – CoolSET™ SiP primary side GNDP pin 2 and pin 7 are recommended to be jointly connected to a PCB copper plane, and then star connected to the bulk capacitor ground
   – CoolSET™ SiP secondary side GNDS pin 11, pin 19 and pin 26 are recommended to be jointly connected to a PCB copper plane, and then star connected to the SR MOSFET source pin

3. **Place the filter capacitors at IC pins close to the controller ground (GNDP and GNDS)**: Filter capacitors should be placed as close to the controller ground and controller pin as possible to reduce the switching noise coupled into the controller

4. **High voltage (HV) trace clearance**: HV traces like startup, bulk capacitors + and primary switch drain traces should maintain sufficient spacing to the nearby traces – arcing may occur otherwise

5. Keep a minimum of 232 mm^2 copper area at both the primary drain pin and secondary GNDS for better thermal performance of the CoolSET™ SiP

6. SR switch Q2 drain copper plane surface area should be mentioned to a reasonable value for convection cooling capability

7 Bill of materials

Table 3 BOM

S.No.	Quantity	Designator	Description	Manufacturer	Part number
1	1	BR1	Dio 800 V/ / THT/ /	Taiwan Semiconductor	KBPF406G
2	1	C1	Cap 100 nF/ 630 V/ THT/Radial/ /10%	Würth Elektronik	890324023023CS
3	2	C2, C3	Cap 39 µF/ 400 V/ THT/Radial/ /20%	Nippon Chemi-Con	EKXN401ELL390MK20S
4	1	C4	Cap 1 nF/ 6.3 V/ 0603/ X5R/10%	–	–
5	3	C5, C12, C16	Cap 680 pF/ 50 V/ 0603/ X7R/5%	–	–
6	1	C6	Cap 1 nF/ 1 kV/ 1206/ X7R/10%	–	–
7	1	C7	Cap 33 pF/ 50 V/ 0603/ C0G/5%	–	–
8	1	C8	Cap 22 µF/ 50 V/ THT/Radial/ /20%	Würth Elektronik	860080672001
9	1	C9	Cap 10 µF/ 50 V/ 1206/ X5R/10%	–	–
10	1	C10	Cap 1 nF/ / THT/Radial/ Y5V/20%	–	–
11	1	C11	Cap 1 nF/ 50 V/ 0603/ X7R/5%	–	–
12	1	C13	Cap 68 nF/ 25 V/ 0603/ X7R/10%	–	–
13	1	C14	Cap 2.2 nF/ 25 V/ 0603/ X7R/10%	–	–
14	2	C15, C19	Cap 470 µF/ 25 V/ THT/Radial/ /20%	KEMET	A750MS477M1EAAE015
15	1	C18	Cap 4.7 µF/ 25 V/ 0805/ X7R/20%	–	–
16	2	C20, C21	Cap 2.2 µF/ 25 V/ 0805/ X7R/10%	–	–
17	1	D1	Dio S1M/ / DO-214AC (SMA)/ /	Taiwan Semiconductor	S1M
18	2	D2, D3	Dio 100 V/ / SMF (DO-219AB)/ /	Vishay	ES07B-GS08
19	1	F1	Pas 36911600000/ / Radial type/ /	Littelfuse	80713150000
20	4	GNDS, J1, J2, Vout	Con 1502-2/ / CON-THT-TP-1502-2/ /	Keystone Electronics Corp.	1502-2
21	1	L3	Ind 10 µH/ / THT/Radial/ /20%	Würth Elektronik	7447462100
22	1	L4	Ind 84 µH/ / THT/ /	ITACOIL	SCF1212052
23	1	Q1	Tra BSS127/ / PG-SOT23/ /	Infineon Technologies	BSS127
24	1	Q2	Tra ISC060N10NM6/ / PG-TDSON-8-36/ /	Infineon Technologies	ISC060N10NM6
25	2	R3, R4	Res 51k/ 200V/ 1206/ /1%	–	–
26	2	R5, R6	Res 5.1MEG/ 200V/ 1206/ /1%	–	–
27	1	R7	Res 75k/ 75V/ 0603/ /1%	–	–
28	2	R8, R9	Res 680mR/ / 1206/ /1%	–	–

Bill of materials

S.No.	Quantity	Designator	Description	Manufacturer	Part number
29	2	R10, R11	Res 180k/ 200V/ 1206/ /1%	–	–
30	1	R12	Res 2k/ 75V/ 0603/ /1%	–	–
31	1	R13	Res 0R/ 75V/ 0603/ /0%	–	–
32	2	R14, R16	Res 2.2R/ 75V/ 0603/ /1%	–	–
33	1	R15	Res 15k/ 75V/ 0603/ /1%	–	–
34	1	R17	Res 20k/ 75V/ 0603/ /0.1%	–	–
35	1	R18	Res 51R/ 200V/ 1206/ /1%	–	–
36	1	R19	Res 10k/ 75V/ 0603/ /1%	–	–
37	2	R20, R41	Res 18k/ 75V/ 0603/ /1%	–	–
38	1	R21	Res 3.9k/ 75V/ 0603/ /1%	–	–
39	1	R22	Res 30k/ 75V/ 0603/ /1%	–	–
40	1	R23	Res 270k/ 75V/ 0603/ /1%	–	–
41	2	R25, R26	Res 0R/ 200V/ 1206/ /0%	–	–
42	1	TR40	Tra 10344-T057/ / THT/ /	Sumida	10344-T057
43	1	U1	ICE184LM / / IFX-PG-DSO-27-1/ /	Infineon Technologies	ICE183LM-V001

8 Transformer specification

8.1 Electrical diagram and coil build

Manufacturer and part number: Sumida (10344-T057).
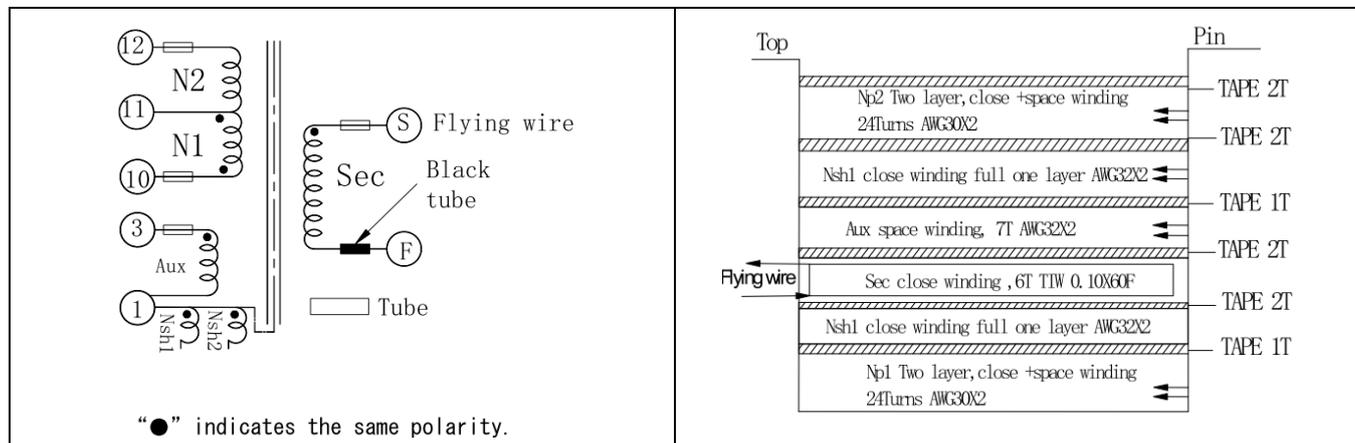
Figure 5   Schematic and winding area schematics 10344-T057

8.2 Electrical specifications

4. Electrical characteristics (at 25℃ unless otherwise specified)

Item	Specification	Measuring Condition
Inductance (10-12)	540μH±10%	100kHz, 1V
Leakage inductance (10-12)	8.5μH Max. (7.0μH Typ.)	100kHz, 1V (Tie:3+1+S+F)
D.C.R. (10-12)	420mΩ Max.	
D.C.R. (S-F)	16.0mΩ Max.	
Turns ratio (10-12):(3-1):(S-F)	8:1.167:1 (±3%)	100kHz, 1V
Hi-Pot (10, 11, 12, 3, 1-S, F)	AC 3000Vrms	50/60Hz, 2mA, 60S.
Hi-Pot (10, 11, 12)-(3, 1)	AC 1000Vrms	50/60Hz, 2mA, 60S.
Insulation impedance Coil-Core, Coil-Coil	100MΩ Min.	DC500V

Figure 6   Electrical characteristics 10344-T057

9 Measurement data and graphs

All performance data is measured at room temperature $T_a = 25°C$, unless otherwise specifically mentioned.

9.1 Efficiency result

Measurements were performed at 25%, 50%, 75%, and 100% of the nominal load after 5 minutes of burn-in time.

Table 4 **Efficiency and four-point average efficiency**

Input (V AC/Hz)	Load / %	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)	Average efficiency (%)
90 V AC/60 Hz	100	33.0	11.97	2.5	29.9	90.5	91.1
	75	24.6	11.98	1.9	22.5	91.4	
	50	16.3	11.98	1.2	15.0	91.6	
	25	8.1	11.98	0.6	7.4	91.1	
115 V AC/60 Hz	100	32.5	11.98	2.5	29.9	91.8	91.9
	75	24.4	11.98	1.9	22.5	92.2	
	50	16.2	11.98	1.2	15.0	92.2	
	25	8.1	11.98	0.6	7.4	91.3	
230 V AC/50 Hz	100	32.2	11.96	2.5	29.8	92.7	91.8
	75	24.3	11.97	1.9	22.5	92.6	
	50	16.3	11.98	1.2	14.9	91.7	
	25	8.2	11.98	0.6	7.4	90.1	
264 V AC/50 Hz	100	32.2	11.97	2.5	29.9	92.7	91.8
	75	24.3	11.97	1.9	22.5	92.6	
	50	16.3	11.98	1.2	15.0	91.8	
	25	8.2	11.98	0.6	7.4	89.9	
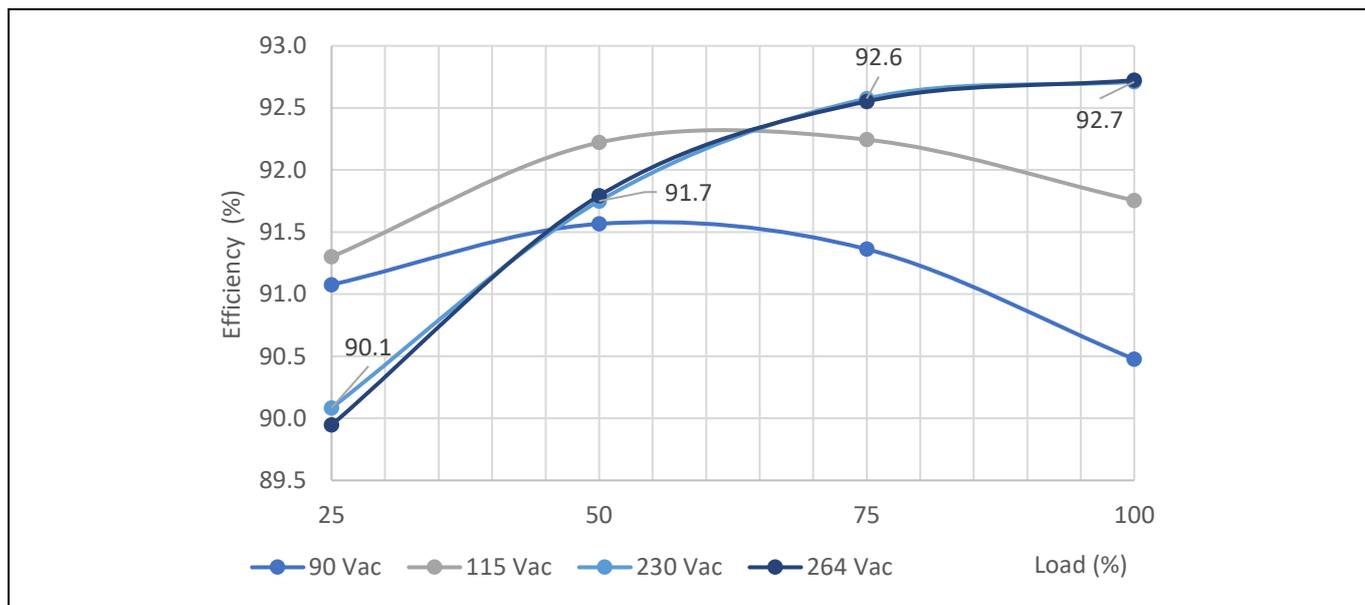
Figure 7   Efficiency vs. loading

9.2   Standby input power consumption

The standby input power consumption of the board was measured at different input voltages without any load attached, see Figure 8.
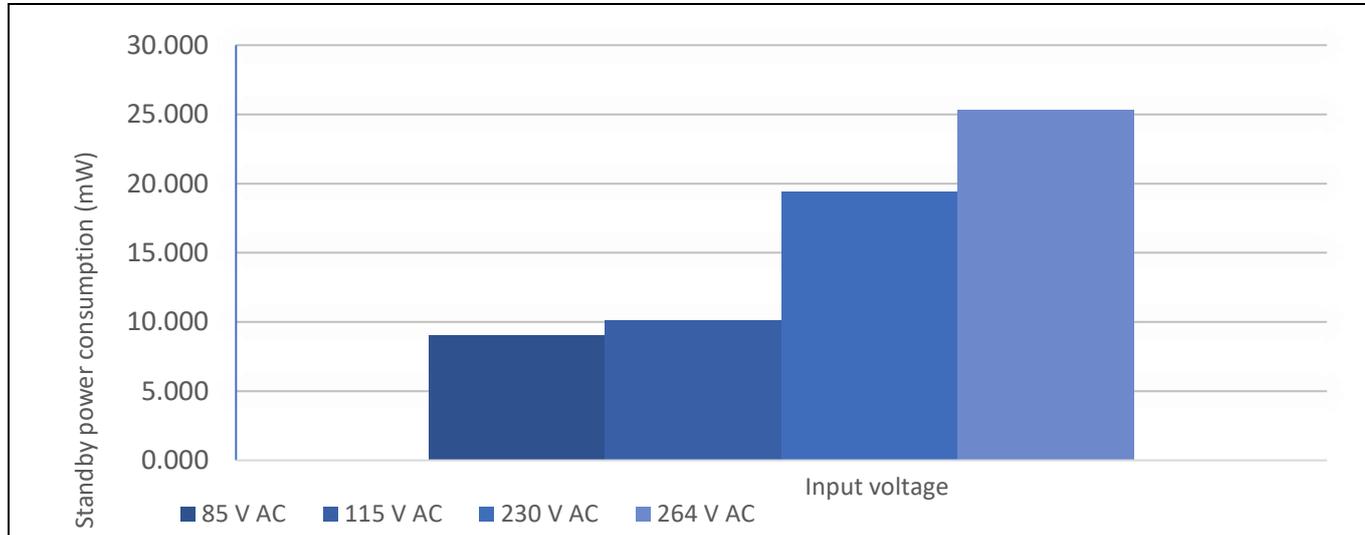
Figure 8   Standby input power consumption

9.3   ESD immunity (EN 61000-4-2)

The reference board was subjected to ESD testing according to EN 61000-4-2 level 3 (±8 kV contact and ±15 kV air discharge), as indicated in Table 5. It was tested at full load (resistive load). A test failure was defined as non-recoverable.

Measurement data and graphs

Table 5   System ESD test result

Description	ESD test	Level	Number of strikes		Test result
			V_{O1}	GNDS	
230 V AC, 30 W	Contact	±8 kV	10	10	Pass
	Air	±15 kV	10	10	Pass

9.4   Surge immunity (EN 61000-4-5)

The reference board was subjected to a surge immunity test according to EN 61000-4-5 level 4 (±2 kV DM and ±4 kV CM), as shown in Table 6. The test was conducted with the system running at full load and a resistive load was connected at the output. A test failure was defined as non-recoverable.

Note: Input line OVP was disabled to avoid protection triggering while testing ±4 kV CM.

Table 6   System lightning surge immunity test result

Description	Test	Level		Number of strikes				Test result
				0°	90°	180°	270°	
230 V AC, 30 W	DM	±2 kV	L → N	3	3	3	3	Pass
	CM	±4 kV	L → G	3	3	3	3	Pass
		±4 kV	N → G	3	3	3	3	Pass

9.5   Conducted emissions (EN 55014)

The conducted emissions test was performed at full output power following the test standard of EN 55014 (CISPR 14). The measurement was performed in phase and neutral configuration with a rated input voltage of 115 V AC/50 Hz and 230 V AC/50 Hz. The results reveal that there is sufficient margin, higher than the limit of 6 dB for both the average and quasi-peak scan, as shown in the plots of Figure 9 to Figure 12.

The measurement equipment used for this emissions test is Rohde & Schwarz HM6050-2 and Tektronix RSA503A. A variable wire wound power resistor adjusted to 4.8 Ω is used as a load.
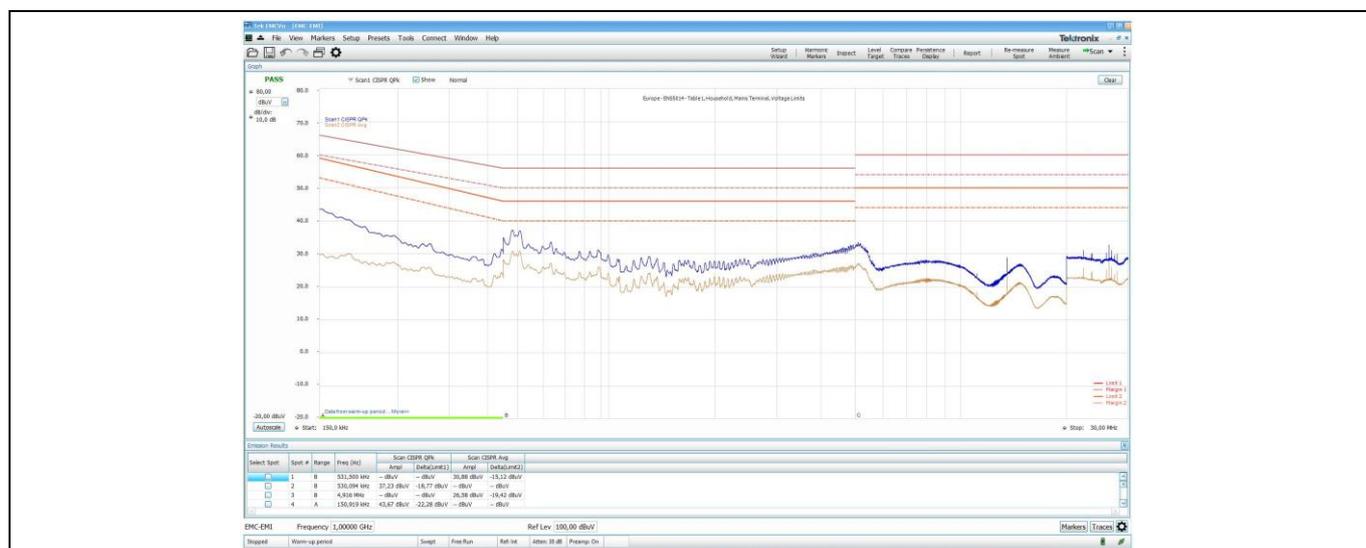
Figure 9   Conducted emissions – phase line (L) 230 V AC

Measurement data and graphs
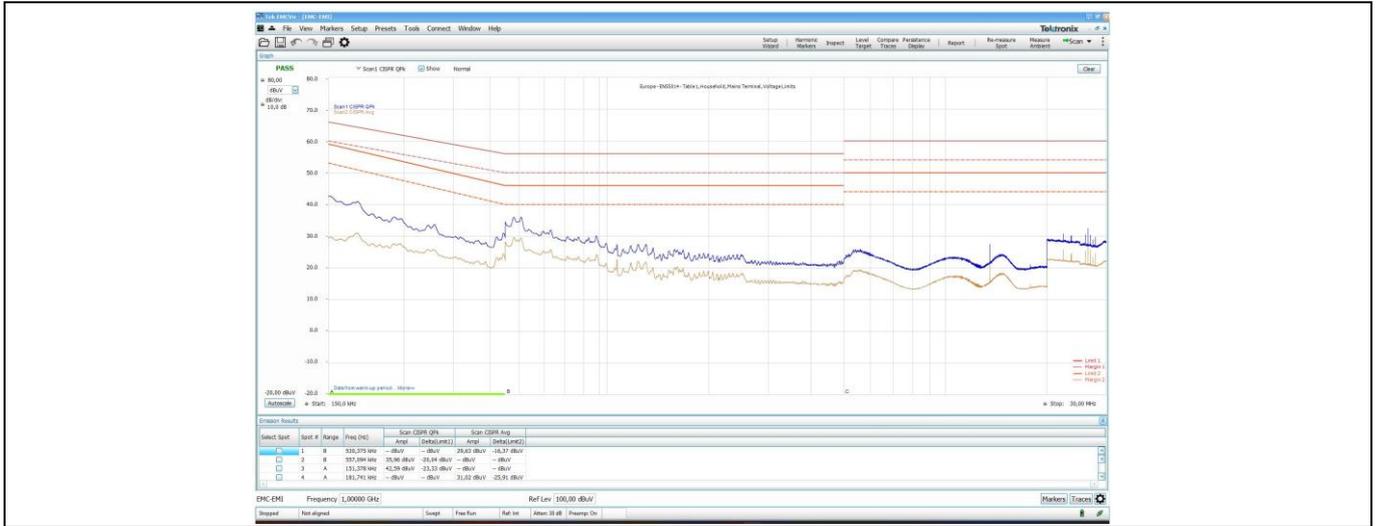
Figure 10   Conducted emissions – neutral line (N) 230 V AC
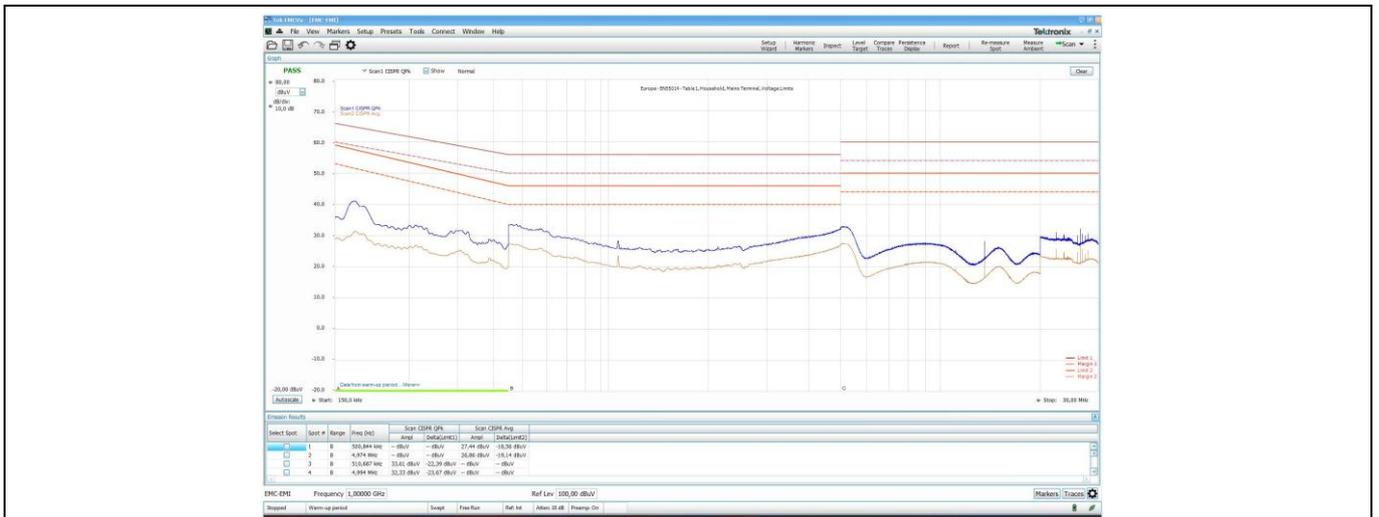
Figure 11   Conducted emissions – phase line (L) 115 V AC
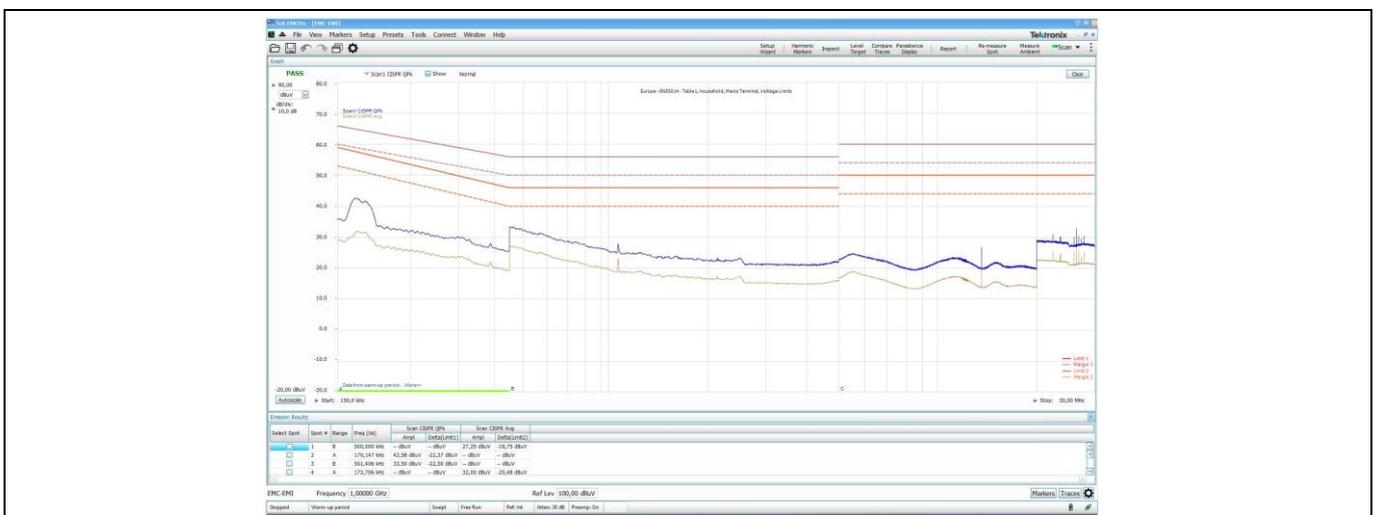
Figure 12   Conducted emissions – neutral line (N) 115 V AC

9.6 Thermal measurement

The thermal testing of the reference board was executed in open air without forced ventilation at an ambient temperature of 25°C. An infrared thermography camera (FLIR-T600) was used to capture the thermal reading of critical components. The measurements were taken at the maximum load of 30 W, running for one hour. The tested input voltages were 90 V AC and 264 V AC.

Table 7   Component temperature at full load under T$_a$ = 25°C

Circuit code	Major component	Input voltage 90 V AC	Input voltage 264 V AC
		Temperature (°C)	Temperature (°C)
TR40	Main transformer	60.8	63.6
BR1	Bridge diode	62.8	41.1
U1	ICE183LM	78.6	58.8
Q2	SR MOSFET	52.4	53.6
RCD	Primary side RCD snubber	66.9	59.6
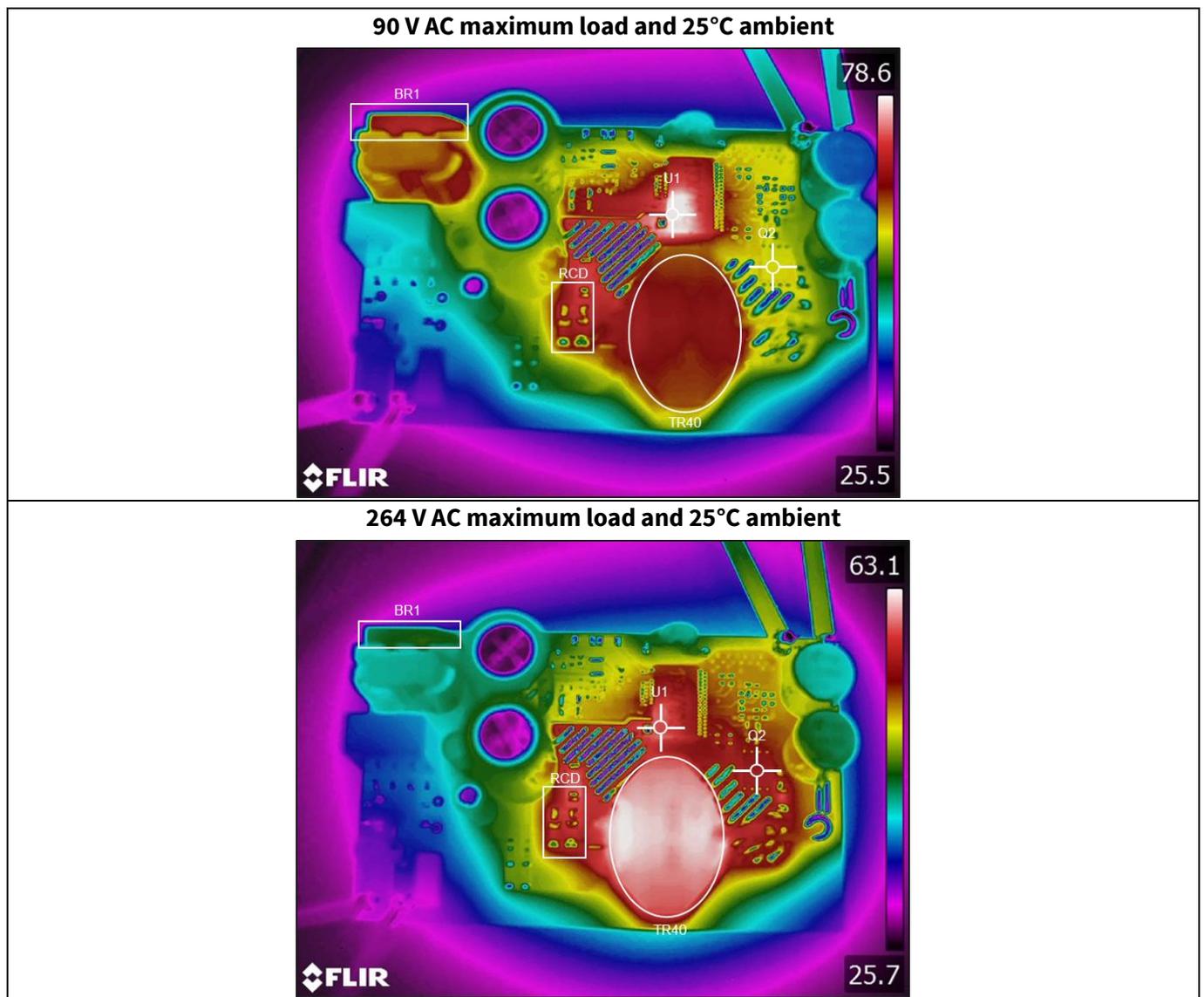
Figure 13   Thermal image of REF_30W1_ZVS_183LM

10 Waveforms and scope plots

The following waveforms and scope plots demonstrate the behavior of the reference board.

10.1 Startup at full load

C1 (yellow) : AC-line voltage	C1 (yellow) : AC-line voltage
C2 (purple) : +12 V output voltage	C2 (purple) : +12 V output voltage
C3 (blue) : +12 V output current	C3 (blue) : +12 V output current
90 V AC startup time at full load is around 704 ms	264 V AC startup time at full load is around 194 ms
The board can start up as expected over 90~264 V AC, output voltage smoothly rises and regulates at 12 V	
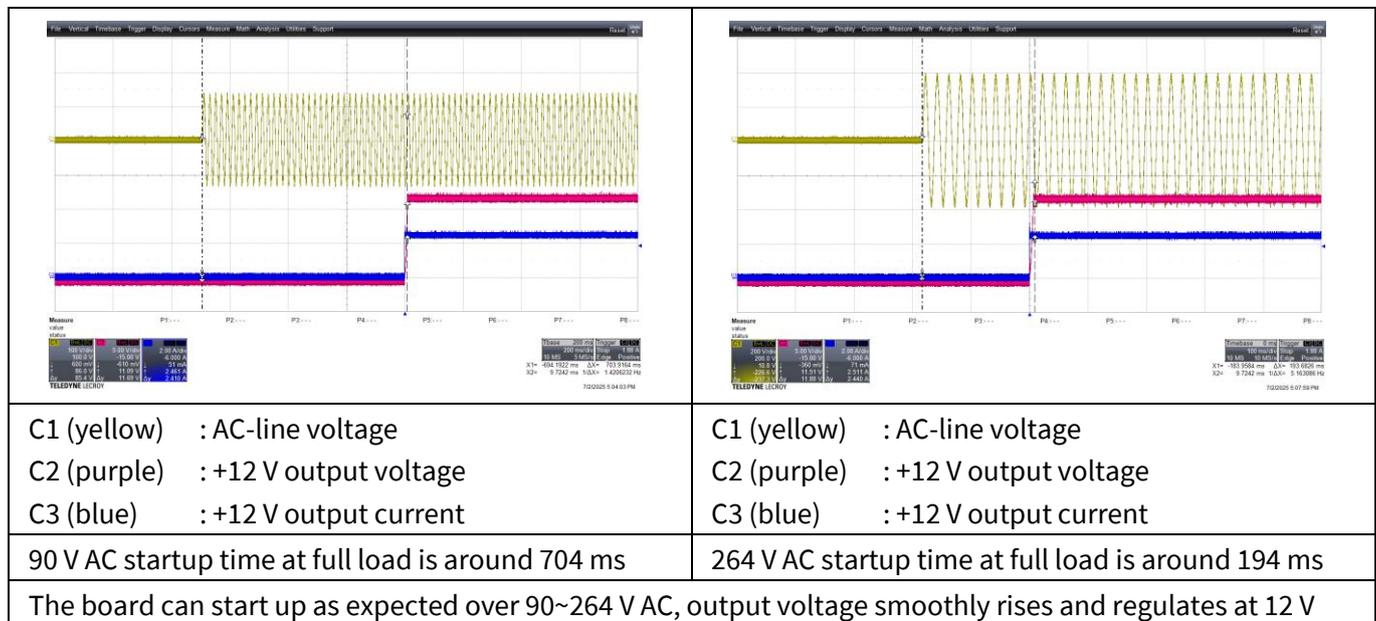
Figure 14 Startup at full load

10.2 Switching waveform at full load

C1 (yellow) : Drain voltage (V_{DS})	C1 (yellow) : Drain voltage (V_{DS})
C2 (purple) : CS voltage (V_{CS})	C2 (purple) : CS voltage (V_{CS})
C4 (green) : SR gate signal (V_{GDSR})	C4 (green) : SR gate signal (V_{GDSR})
V_{IN} = 90 V AC, full load; the first valley is measured (QR = 1 at low line)	V_{IN} = 264 V AC, full load; the third valley is measured (QR = 3 at high line with ZVS switching)
CoolSET™ SiP ICE183LM operates in quasi-resonant valley switching at low line and with zero voltage switching at high line	

Figure 15 Switching waveform at full load

10.3 SR FET voltage at full load

C4 (green) : SR Drain voltage(V_{SR_Drain})	C4 (green) : SR Drain voltage(V_{SR_Drain})
V_{IN} = 90 V AC, full load	V_{IN} = 264 V AC, full load
Maximum Drain voltage is around 31 V	Maximum Drain voltage is around 65 V
The measured SR MOSFET voltage stress at 264 Vac input is well below its voltage rating thanks to ZVS feature	
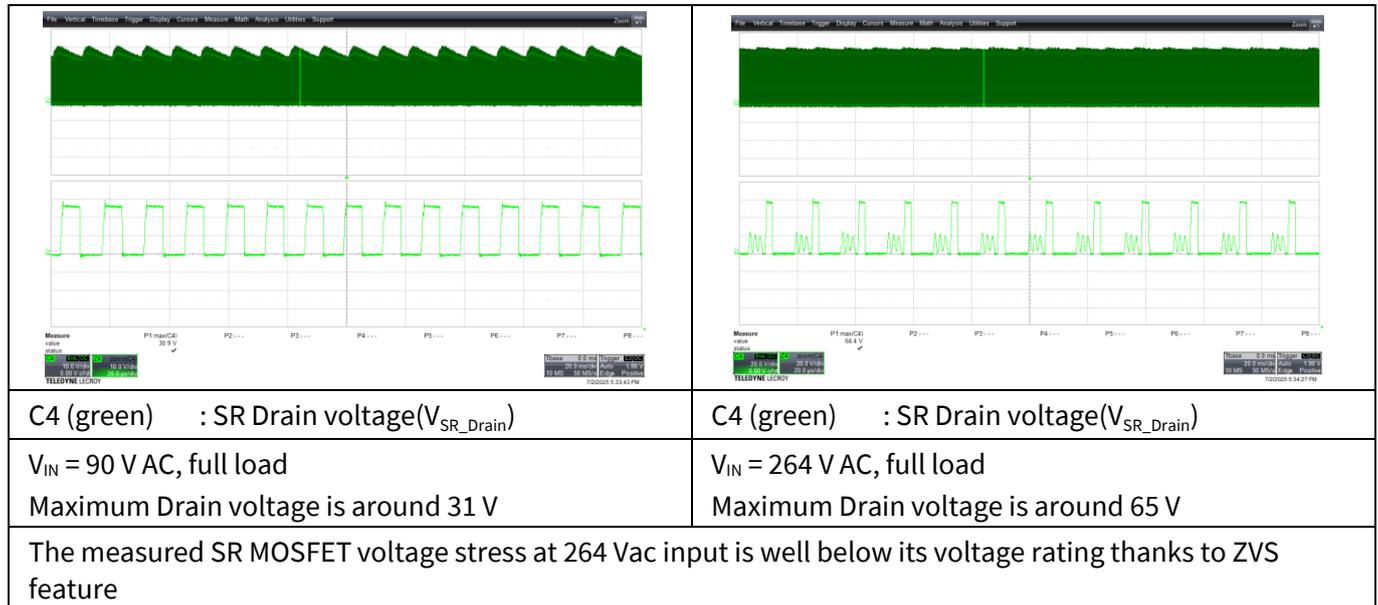
Figure 16   SR FET voltage

10.4 Output ripple voltage at full load

C4 (green) : +12 V output ripple voltage	C4 (green) : +12 V output ripple voltage
V_{IN} = 90 V AC, full load	V_{IN} = 264 V AC, full load
V_{ripple_pk} for +12 V output voltage: 166 mV	V_{ripple_pk} for +12 V output voltage: 193 mV
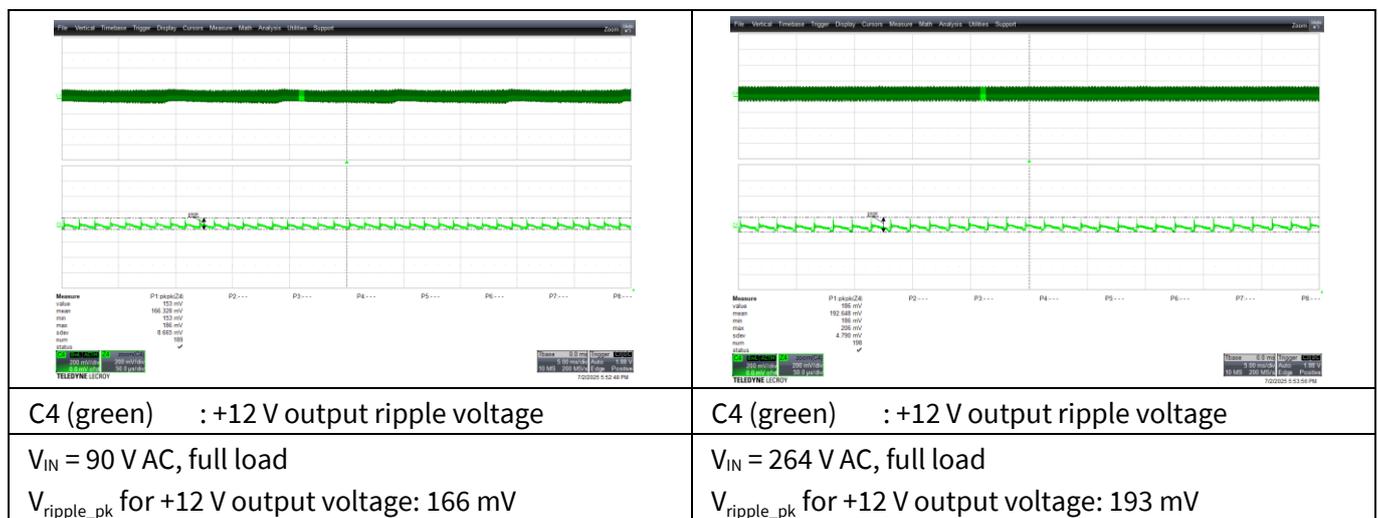
Figure 17   Output ripple voltage at full load (20 MHz bandwidth and 47 µF electrolytic capacitor in parallel with 0.1 µF ceramic capacitor)

Waveforms and scope plots

10.5   Load-transient response

The load-transient response of the system was tested at 90 VAC and 264 VAC input, as shown in Figure 18. The load-transient conditions are the following: +12 V output load change from 10% to 100% at 0.25 A/µs slew rate, 100 Hz. Oscilloscope probes were limited at 20 MHz bandwidth. A 47 µF electrolytic capacitor in parallel with 0.1 µF ceramic capacitor were placed on the output for the ripple voltage reading.

C3 (blue) : Load current C4 (green) : +12 V output ripple voltage	C3 (blue) : Load current C4 (green) : +12 V output ripple voltage
V_{IN} = 90 V AC V_{ripple_max} for +12 V output voltage: 237 mV V_{ripple_min} for +12 V output voltage: -232 mV	V_{IN} = 264 V AC V_{ripple_max} for +12 V output voltage: 235 mV V_{ripple_min} for +12 V output voltage: -252 mV
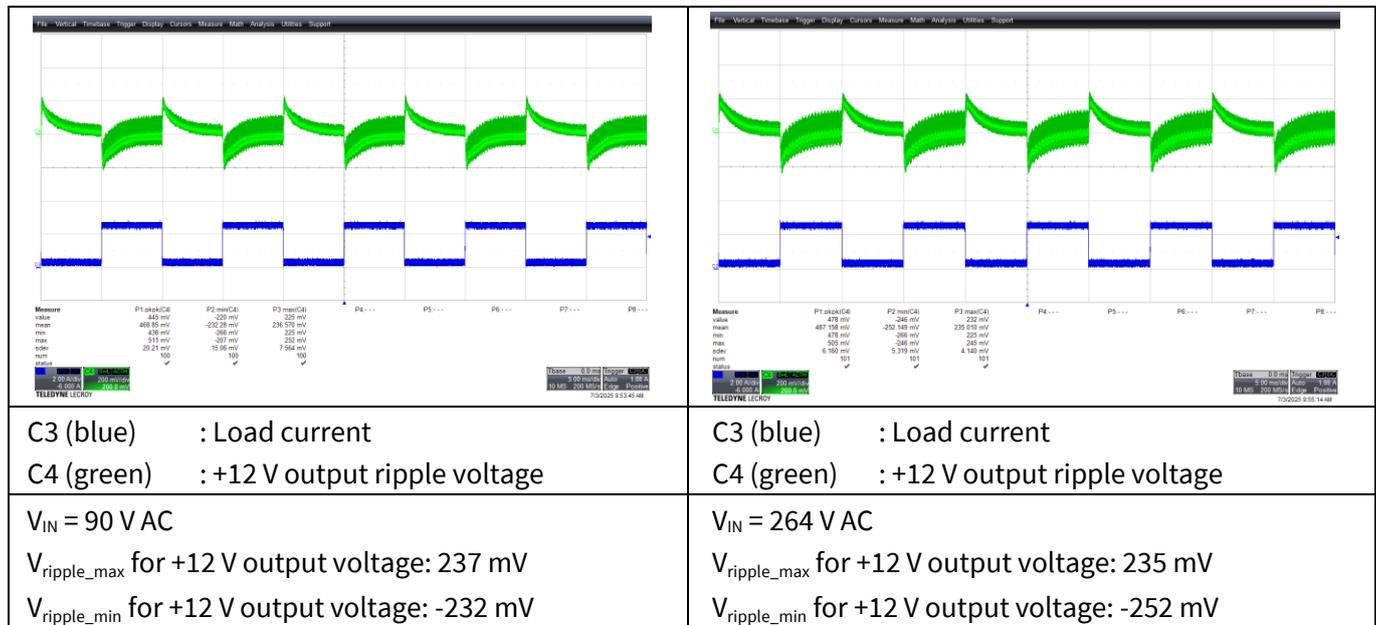
Figure 18   Load-transient response

11 Related resources

- AC-DC integrated power stage - CoolSET™
- Power Management ICs
- REF_30W1_ZVS_183LM

References

[1]   Infineon Technologies AG: Datasheet - CoolSET™ SiP G1 LM ICE183LM, Version 1.0, 2025; Available online

[2]   Infineon Technologies AG: Design guide for zero-voltage switching quasi-resonant flyback using CoolSET™ SiP; Available online

[3]   Infineon Technologies AG: Calculation tool: CoolSET™ SiP; Available online

Revision history

Document version	Date of release	Description of changes
V 1.0	2025-09-30	Initial release

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