100 V OptiMOS™ 8 power MOSFETs: Advancing trench technology performance

Setting a new industry standard with Infineon's latest trench MOSFET innovation

About this document

Scope and purpose

This document introduces Infineon's latest 100 V OptiMOS™ 8 family of MOSFETs based on Infineon's latest trench MOSFET technology, and provides an exceptionally low on-state resistance ($R_{DS(on)}$), a low $R_{DS(on)}$ temperature coefficient, and good switching performance. These features make the OptiMOS™ 8 MOSFET the ideal fit for $R_{DS(on)}$-driven applications that demand low conduction losses.

This application note demonstrates the performance improvement achieved over OptiMOS™ 5 MOSFET in applications, such as motor drives and battery protection units. A brief introduction to the technology highlighting its technical benefits is followed by an experimental evaluation comparing the 100 V OptiMOS™ 8 MOSFET with the OptiMOS™ 5 MOSFET. The final section of this application note highlights the system-level improvements contributed by 100 V OptiMOS™ 8 power MOSFETs to battery protection circuits in battery management systems.

Intended audience

The intended audiences for this document are design engineers, technicians, and developers of electronic systems.

Key points

- Demonstrates how the latest trench MOSFET technology improves performance in $R_{DS(on)}$-driven power applications
- Describes gate-drive design considerations when migrating from OptiMOS™ 5 to OptiMOS™ 8 for comparable di/dt, dv/dt, switching losses, and EMI performance
- Demonstrates measured loss, thermal, and current capability results to support informed device selection decisions
- Demonstrates device characteristics and their practical design benefits, such as higher efficiency, power density, and cost optimization

About this product family

Product family

Infineon's 100 V OptiMOS™ 8 power MOSFETs provide excellent performance with increase in efficiency, power density, and cost-effectiveness. Optimized for $R_{DS(on)}$-driven applications, they are ideally suited for a wide range of applications.

Setting a new industry standard with Infineon's latest trench MOSFET innovation

About this product family

Target applications

- Industrial drives
- Electric forklifts
- Battery management systems (BMS)
- Industrial and consumer BMS

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1 The latest 100 V OptiMOS™ 8 power MOSFET

1.1 Features and benefits

For low switching-frequency applications like motor drives, MOSFET losses are dominated by conduction losses. When MOSFETs are used as static switches in applications such as battery management systems, the total losses are determined solely by the on-state resistance ($R_{DS(on)}$). In these cases, decreasing $R_{DS(on)}$ significantly enhances system efficiency, enabling higher power density, lower losses, and reduced emissions. This is particularly important in modern applications, where energy efficiency is a key design requirement.

Infineon's latest trench MOSFET technology has enabled the development of the OptiMOS™ 8 MOSFET family, specifically optimized for applications requiring extremely low $R_{DS(on)}$.

With its superior $R_{DS(on)}$, the 100 V OptiMOS™ 8 power MOSFET delivers high efficiency, high power density, and high system reliability. As a result, in high-current applications like motor drives, it enables a potential reduction in the number of parallel-connected MOSFETs, simplifies thermal management, and supports extended system operating time.

1.2 Target applications

Applications that benefit from the new Infineon 100 V OptiMOS™ 8 power MOSFETs are shown in Figure 1.

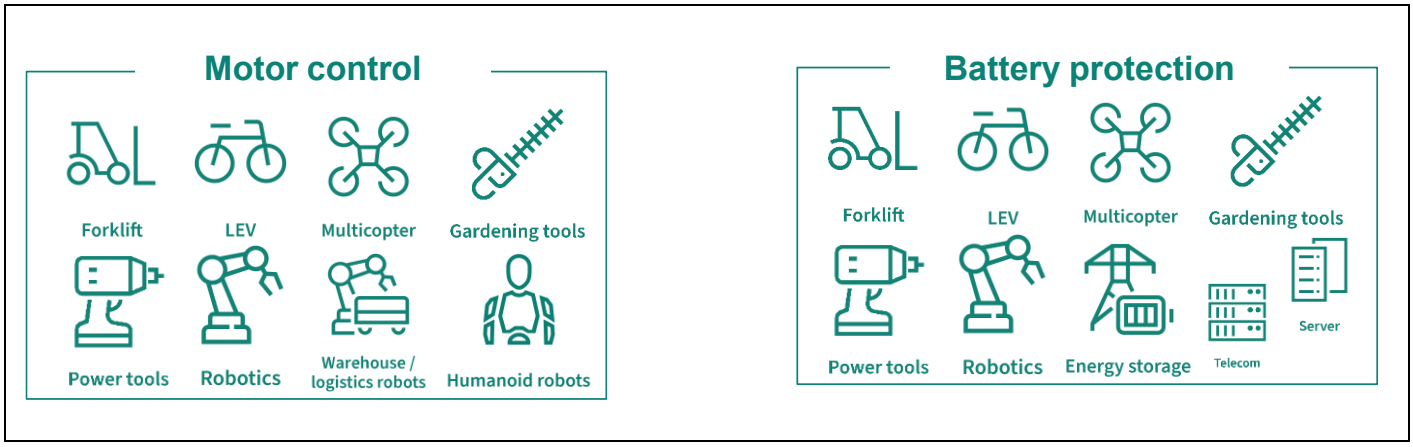


Figure 1 Key target applications of the 100 V OptiMOS™ 8 MOSFETs in motor control and battery protection systems

1.2.1 On-state resistance ($R_{DS(on)}$)

Figure 2 compares the $R_{DS(on)}$ values of the latest 100 V OptiMOS™ 8 power MOSFET technology with the previous-generation 100 V OptiMOS™ 5 power MOSFETs. A significant reduction in $R_{DS(on)}$ is observed, with improvements of 0.53 mΩ (35.3%) at T_C = 25°C and 1.1 mΩ (32.81%) at T_C = 25°C and T_C = 175°C, both specified at a gate-source voltage, V_{GS} = 10 V. This improvement highlights the enhanced performance of the OptiMOS™ 8 MOSFET family compared to the OptiMOS™ 5 MOSFET family.

The decreased $R_{DS(on)}$ provides system-level advantages in end applications, such as:

- Reduces conduction losses, improving battery lifetime and reducing thermal management complexity
- Potentially reduces the number of parallel-connected MOSFETs, leading to optimized cost, reduced PCB area, and increased power density
- Potentially enables the use of smaller package options without compromising the $R_{DS(on)}$ value
- Supports migration from IMS PCB to FR4 PCB in selected applications

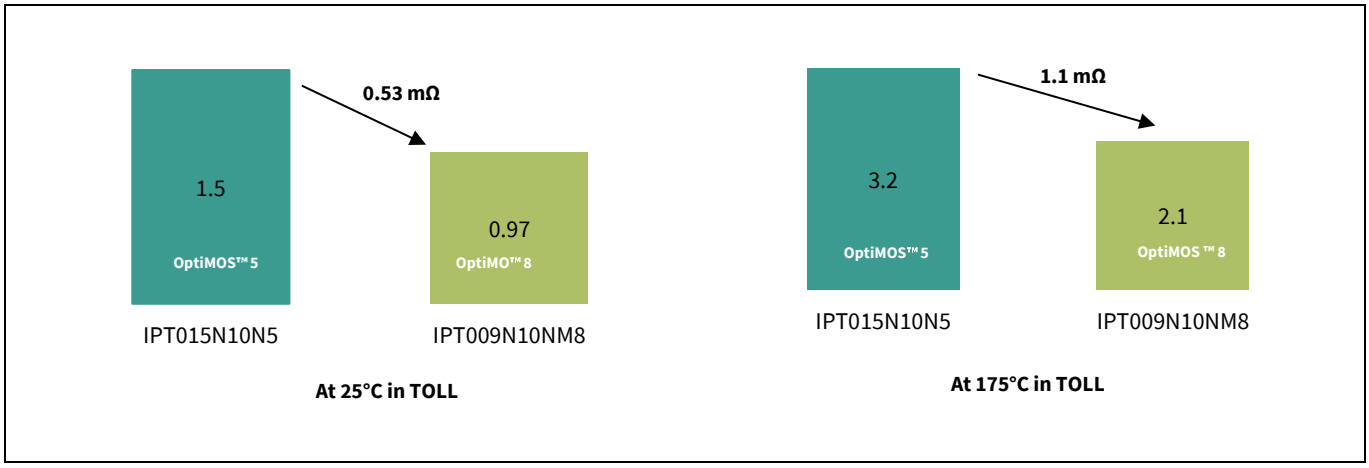


Figure 2 Comparison of maximum $R_{DS(on)}$ (mΩ) for 100 V MOSFETs in TOLL package at 25°C (left) and for 175°C (right)

When analysing the normalized $R_{DS(on)}$ versus temperature characteristics shown in the datasheet (see Figure 3), the OptiMOS™ 8 MOSFET initially displays a higher $R_{DS(on)}$ temperature dependency compared with OptiMOS™ 5 MOSFET because of the lower absolute $R_{DS(on)}$ reference value of OptiMOS™ 8 MOSFET. In absolute terms, the maximum variation in $R_{DS(on)}$ for OptiMOS™ 8 MOSFET is only 1.13 mΩ as the temperature increases from 25°C to 175°C, compared to 1.7 mΩ for OptiMOS™ 5 MOSFET under the same conditions.

When comparing the absolute $R_{DS(on)}$ variation over temperature, the OptiMOS™ 8 MOSFET remains closer to its 25°C $R_{DS(on)}$ reference value than the OptiMOS™ 5 MOSFET across the entire temperature range (see Figure 3).

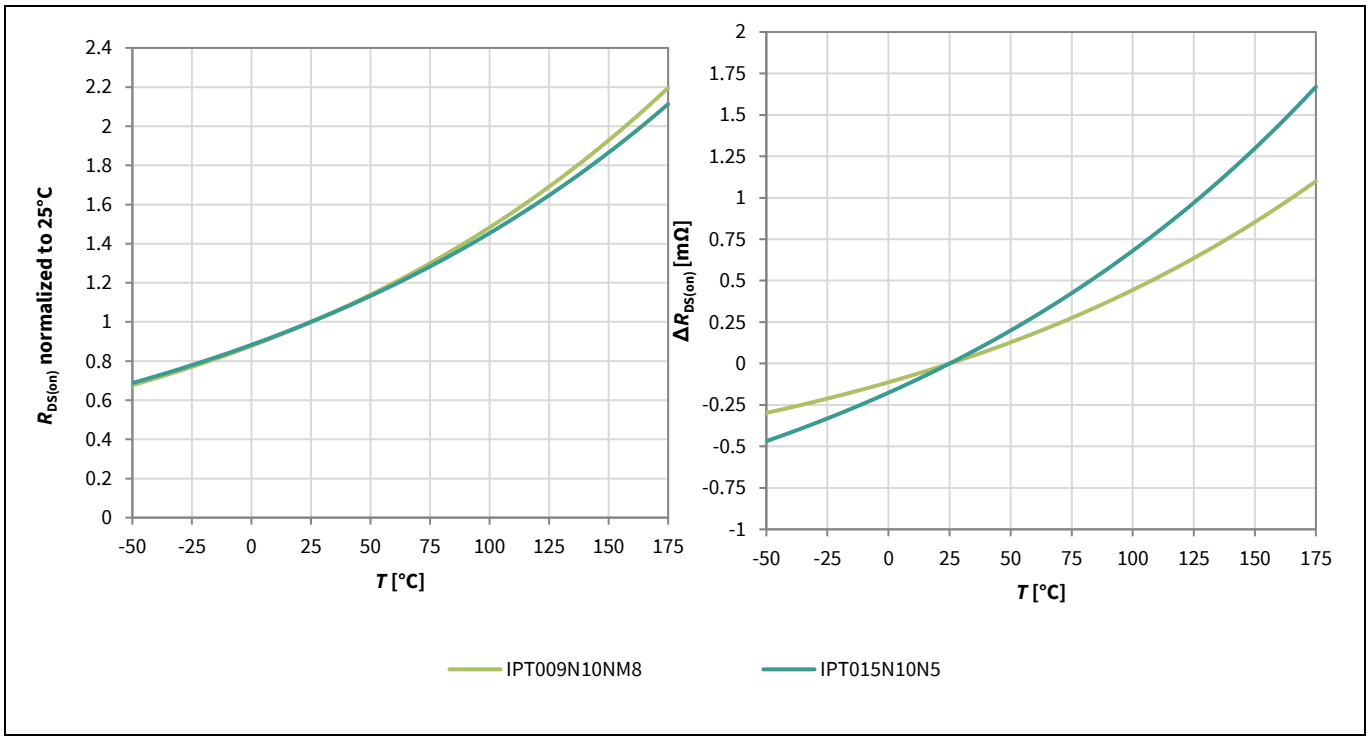


Figure 3 **Normalized $R_{DS(on)}$ to 25°C vs. junction temperature (left); absolute $R_{DS(on)}$ vs. temperature for OptiMOS™ 5 and OptiMOS™ 8 MOSFETs (right)**

In drive application development, engineers must continuously balance performance requirements with cost constraints. Table 1 presents the 100 V OptiMOS™ 8 product portfolio, which covers a wide range of $R_{DS(on)}$ values across multiple package types commonly used in drive applications. The 'Category' column indicates whether a device offers performance comparable to its OptiMOS™ 5 predecessor at a better price-to-performance ratio or supports higher motor drives inverter output power.

Table 1 **100 V OptiMOS™ 8 MOSFET family portfolio**

Package	Part number	$R_{DS(on),max}$ at V_{GS} = 15 V (mΩ)	Category
SSO8 5x6 PG-TDSON-8	ISC019N10NM8	1.93	Industry-leading
	ISC033N10NM8	3.33	Price/performance vs. BSC035N10NS5
	ISC040N10NM8	4.04	Price/performance vs. BSC040N10NS5
SSO8 5x6 PG-WSON-8	ISC019N10NM8SC	1.93	Industry-leading Double-side cooled package
TOLL PG-HSOF-8	IPT009N10NM8	0.93	Industry-leading
	IPT014N10NM8	1.38	Price/performance vs. IPT015N10N5
	IPT018N10NM8	1.84	Price/performance vs. IPT020N10N5

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The latest 100 V OptiMOS™ 8 power MOSFET

Package	Part number	$R_{DS(on),max}$ at V_{GS} = 15 V (mΩ)	Category
D^2Pak 7-pin PG-TO263-7	IPF009N10NM8	0.94	Industry-leading
	IPF014N10NM8	1.42	Price/performance vs. IPB017N10N5
	IPF019N10NM8	1.94	Price/performance vs. IPB024N10N5 IPB025N10N3
D^2PAK 3-pin PG-TO263-3	IPB013N10NM8	1.34	Industry-leading
	IPB018N10NM8	1.76	Price/performance vs. IPB020N10N5

2 Experimental results

The previous section focused on a technology comparison of the industry-leading devices, OptiMOS™ 5 IPT015N10N5 MOSFET and OptiMOS™ 8 IPT009N10NM8 MOSFET to highlight the performance advantages of the latest OptiMOS™ 8 MOSFETs. OptiMOS™ 5 IPB024N10N5 MOSFET is widely used in motor drive applications due to its excellent price performance ratio. Therefore, this section compares the 2.4 mΩ OptiMOS™ 5 IPB024N10N5 MOSFET with its OptiMOS™ 8 counterpart, the 1.9 mΩ IPF019N10NM8 MOSFET in a motor drives application.

2.1 Gate-drive circuitry considerations

At turn-on, the MOSFET gate behaves like an uncharged capacitor, C_{iss}, which is the sum of the gate-to-source capacitance (C_{GS}) and the gate-to-drain capacitance (C_{GD}):

$$C_{iss} = C_{GS} + C_{GD}$$

Equation 1 Input capacitance C_{iss}

In hard-switching applications, once the voltage across C_{GS} exceeds the gate-to-source threshold voltage $V_{GS(th)}$, a conductive channel forms under the gate, and the MOSFET begins to conduct current. As V_{GS} increases further, the drain current rises according to the transconductance g_{fs}, while the drain-to-source voltage remains approximately equal to the DC-link voltage. The resulting change in drain current can be approximated using the following relation:

$$\partial I_D = g_{fs} \times \partial V_{GS}$$

Equation 2 Drain current in the saturation region

Thus, a faster rise in V_{GS} results in a higher di/dt. Consequently, the RC element formed by R_G and C_{GS} can be used to control the di/dt. Due to the lower g_{fs} of the OptiMOS™ 8 MOSFET, a lower di/dt is expected for the same rate of change of V_{GS}.

When the MOSFET is fully turned on, the conducting channel connects the drain and source terminals of the MOSFET. Therefore, V_{DS} is almost zero and determined just by $R_{DS(on)}$ and the drain current I_D. For V_{DS} to decrease, the gate-to-drain capacitance (C_{GD}) and the drain-to-source capacitance (C_{DS}) must be discharged. At the beginning of the turn-on event, these capacitances are charged to V_{DC}. C_{DS} is discharged through the MOSFET channel, while C_{GD} is discharged by the gate driver. During the discharge of C_{GD} and C_{DS}, V_{DS} decreases and the entire gate-drive current is used to discharge C_{GD}, keeping V_{GS} constant. During this period, V_{GS} shows a plateau known as Miller plateau. For a smaller $C_{GD}R_G$ time constant, C_{GD} gets discharged faster, allowing the dv/dt to be controlled.

In summary, with the $C_{GS}R_G$ time constant, the di/dt can be controlled and the $C_{GD}R_G$ time constant can be used to control the dv/dt of the switching event. Since R_G is included in both time constants, any change in R_G affects both time constants.

In drive applications, usually an external C_{GS} is used to control the di/dt section. If the di/dt and dv/dt values of OptiMOS™ 5 MOSFET and OptiMOS™ 8 MOSFET are to be matched for comparable switching losses and EMI performance, dv/dt can be adjusted using the R_G value. Since OptiMOS™ 8 MOSFET shows a lower transconductance, C_{GS} can be reduced or even omitted to achieve the desired di/dt.

For gate drivers with a push-pull output stage, a common method to separate $R_{G,on}$ from $R_{G,off}$ is to use a diode, as shown in Figure 4. During turn-on, the diode is reverse-biased, so only $R_{G,on}$ is active. During turn-off, the diode becomes forward-biased, and the effective gate resistance is defined by the parallel combination of $R_{G,on}$ and $R_{G,off}$. All components located to the left of the red line in Figure 4 are placed on the gate-drive card, while those to the right are implemented on the power board (see Figure 5). The 10 Ω gate resistor on the power board is used to dampen ringing between the gate driver and the MOSFET, as both are located on separate PCBs.

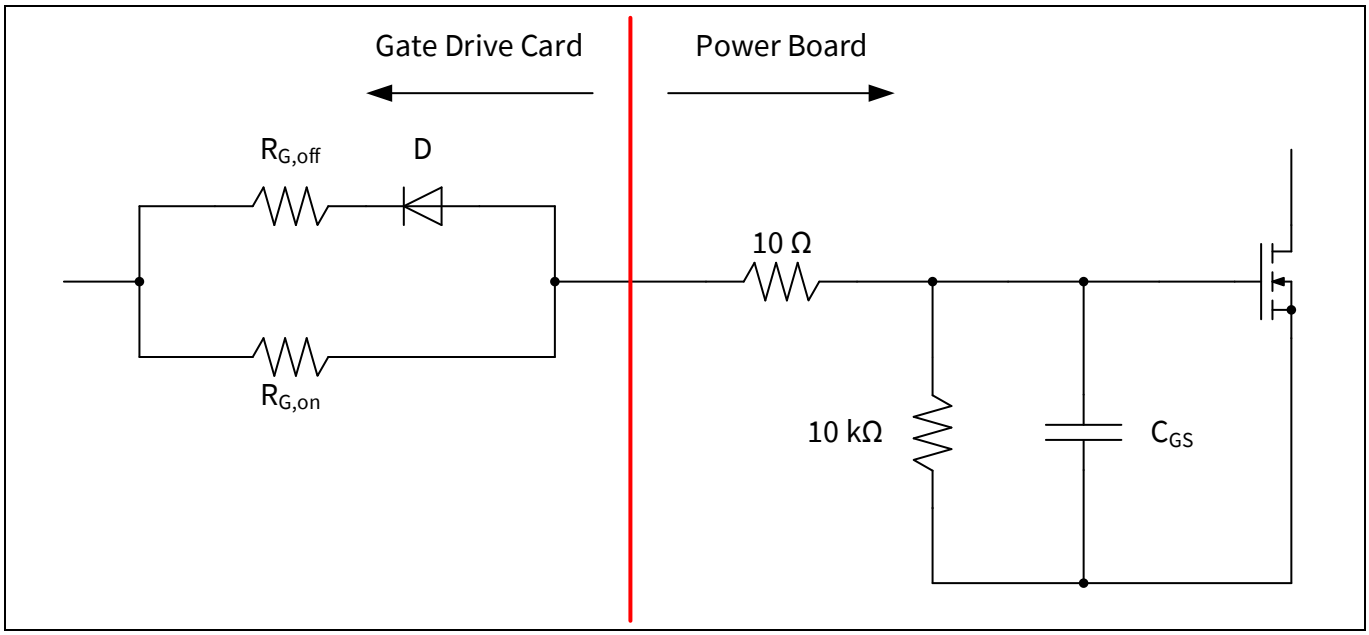


Figure 4 Gate-drive circuit

To match the waveforms for OptiMOS™ 5 IPB024N10N5 and OptiMOS™ 8 IPF019N10NM8 MOSFETs, the following values are used.

Table 2 Gate-drive circuit

Device	$R_{G,on}$	$R_{G,off}$	C_{GS}
	Ω	Ω	pF
OptiMOS™ 5 IPB024N10N5	150	120	470
OptiMOS™ 8 IPF019N10NM8	130	100	0

Due to the slightly higher charge values of the OptiMOS™ 8 MOSFET, slightly lower R_G values are applied. In addition, the $C_{GS}R_G$ time constant is further reduced by omitting C_{GS}. The resulting waveforms, with matched maximum di/dt and dv/dt values at a 100 A pulse, are shown in Figure 6 for turn-on and in Figure 7 for turn-off.

2.2 Bench test platform and conditions

For the bench test, the motor drive inverters with the devices under test (DUTs) are loaded with an induction motor (IM) operating at the same inverter conditions (input voltage, duty cycle, switching frequency, and synchronous speed of the IM). The motor load torque is adjusted to achieve a MOSFET case temperature of 100°C in a steady state condition. The output current of the inverter serves as an indicator of the performance of the investigated MOSFETs. A render of the test platform used is shown in Figure 5.

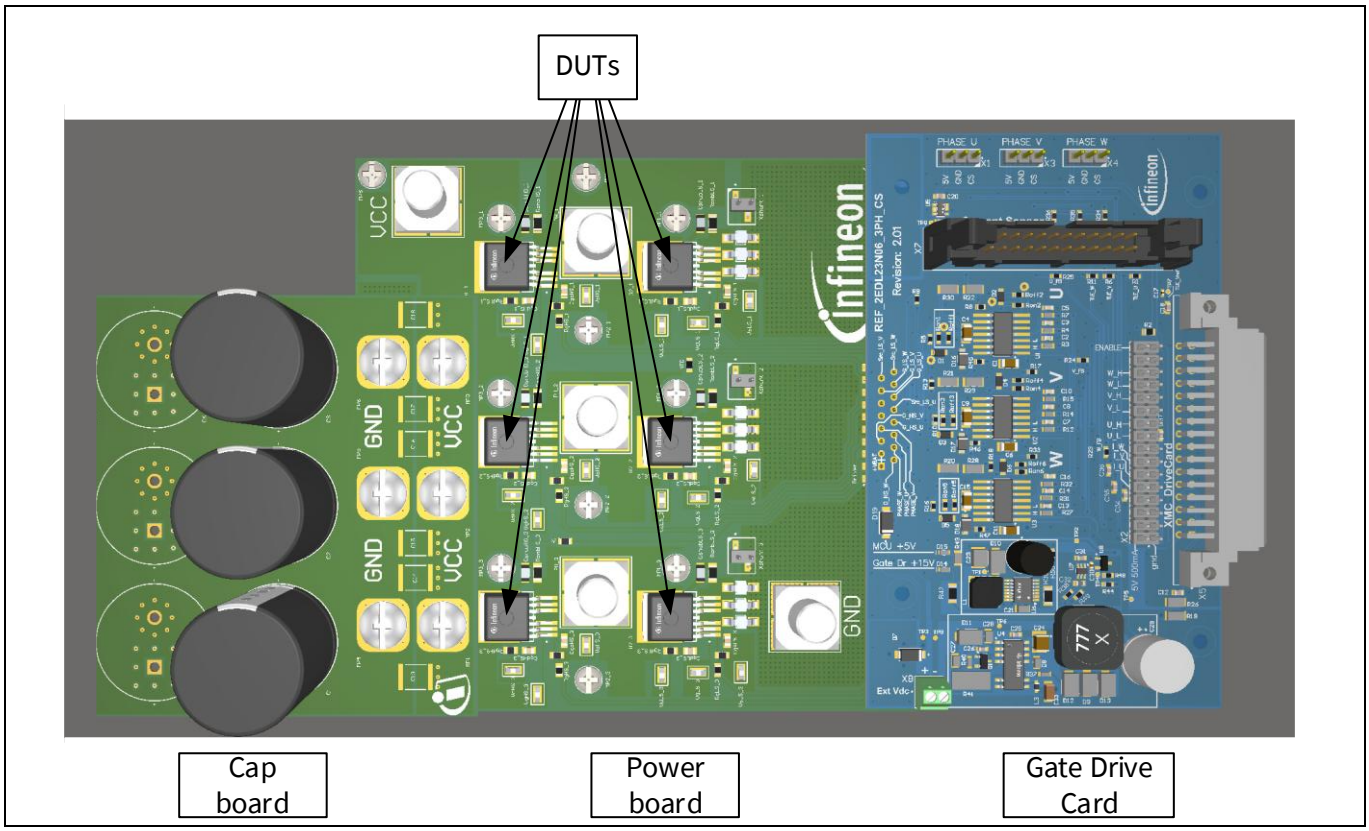


Figure 5 A render of the test platform

The following test conditions are applied:

- Topology: 3-phase inverter; 6 MOSFETs; single MOSFET per switch (no paralleling)
- PCB type: Double layer IMS with aluminum core
- DC bus voltage: 48 V
- Switching frequency: 10 kHz
- Modulation: Sinusoidal SVM
- Duty cycle: 83%
- Heat sink size: 123 mm×115 mm×40 mm (length×width×height)
- Load varied to reach 100°C at the MOSFET's case

2.3 Constant heatsink temperature test

The mechanical load of the induction motor (IM) is adjusted under the specified conditions to achieve a steady-state MOSFET case temperature of 100°C. The inverter output current is used as the key performance indicator.

2.3.1 Measurement results

The average of the measured $R_{DS(on)}$ for all six MOSFETs at 25°C is given in Table 3. As the temperature increases, $R_{DS(on)}$ also increases. The $R_{DS(on)}$ values are extrapolated to the corresponding junction temperature (T_j) using the temperature coefficient given in the datasheet, as shown in Figure 3. At a case temperature of 100°C, $R_{DS(on)}$ increases from 1.76 mΩ to 3.1 mΩ for the OptiMOS™ 5 IPB024N10N5 MOSFET and from 1.71 mΩ to 2.8 mΩ for the OptiMOS™ 8 IPF019N10NM8 MOSFET (see Table 3).

A comparison of the output current at a case temperature of 100°C shows that the OptiMOS™ 8 MOSFET achieves an approximately 4.3% higher output current capability than the OptiMOS™ 5 MOSFET.

Table 3 Measurement results

Device	25°C	100°C				
	$R_{DS(on)}$	T_{max}	T_{av}	$R_{DS(on)}$	I	ΔI
	mΩ	°C	°C	mΩ	A	%
OptiMOS™ 5 IPB024N10N5	1.76	100.5	99.1	3.1	78.2	Reference
OptiMOS™ 8 IPF019N10NM8	1.71	100.8	99.3	2.8	81.6	+ 4.3

The results of the thermal test show that the OptiMOS™ 8 MOSFET can support approximately 4.3% higher output current than its predecessor, while maintaining the same MOSFET case temperature.

With the lower cost of the replacement OptiMOS™ 8 device and its comparable performance, the solution achieves an improved price-to-performance ratio.

2.3.2 Static (conduction) losses

For motor-drive applications with relatively low switching frequencies, MOSFET losses are usually dominated by conduction losses. These losses can be determined easily using the $R_{DS(on)}$ and the RMS value of the inverter output current.

$$P_{con} = R_{DS(on)} I_{rms}^2$$

Equation 3 Conduction losses

At a MOSFET case temperature of 100°C, the analysis uses extrapolated $R_{DS(on)}$ values together with the measured inverter output currents (see Table 3). This results in conduction losses of 57.2 W for all six MOSFETs in the inverter using OptiMOS™ 5 IPB024N10N5 and 54.9 W using OptiMOS™ 8 IPF019N10NM8, as shown in Table 4.

Table 4 Conduction losses

Device	100°C
	P_{con}
	W
OptiMOS™ 5 IPB024N10N5	57.2
OptiMOS™ 8 IPF019N10NM8	54.9

2.3.3 Dynamic (switching) losses

In hard-switching topologies, such as the inverter used in the test platform, high voltages and currents occur simultaneously across the power switches. The MOSFETs must therefore withstand these high-power stress conditions. Unlike conduction losses, the switching losses are more difficult to predict and require measurement. In the following section, turn-on and turn-off losses are measured, and the total switching losses are quantified for both OptiMOS™ 5 and OptiMOS™ 8 MOSFETs.

Figure 6 shows the V_{DS}, I_D, and P_{sw} waveforms of the high-side switch for a turn-on event of the half-bridge and a positive output current of 100 A. When comparing OptiMOS™ 5 and OptiMOS™ 8 MOSFETs, it can be concluded that the switching energy to turn on an OptiMOS™ 5 MOSFET is slightly higher, indicated by the area under the power curve.

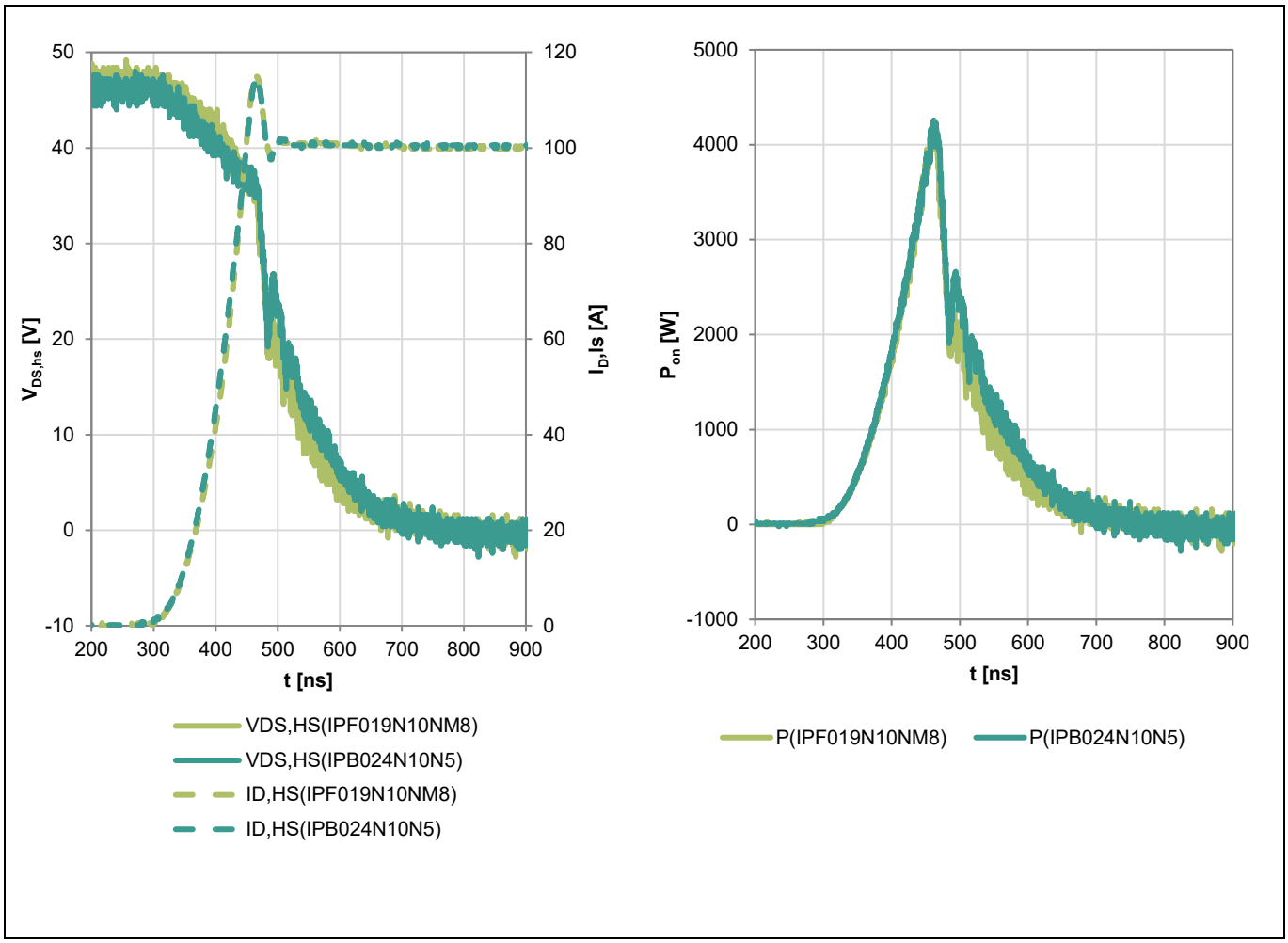


Figure 6 **Turn-on waveforms of OptiMOS™ 5 and OptiMOS™ 8 MOSFETs at I_D = 100 A; drain-source voltage and drain current (left) and instantaneous power (right)**

Figure 7 shows similar waveforms as Figure 6 for a turn-off event of the half-bridge. OptiMOS™ 8 MOSFET shows a faster rise of the V_{DS} voltage resulting in a slightly higher turn-off loss.

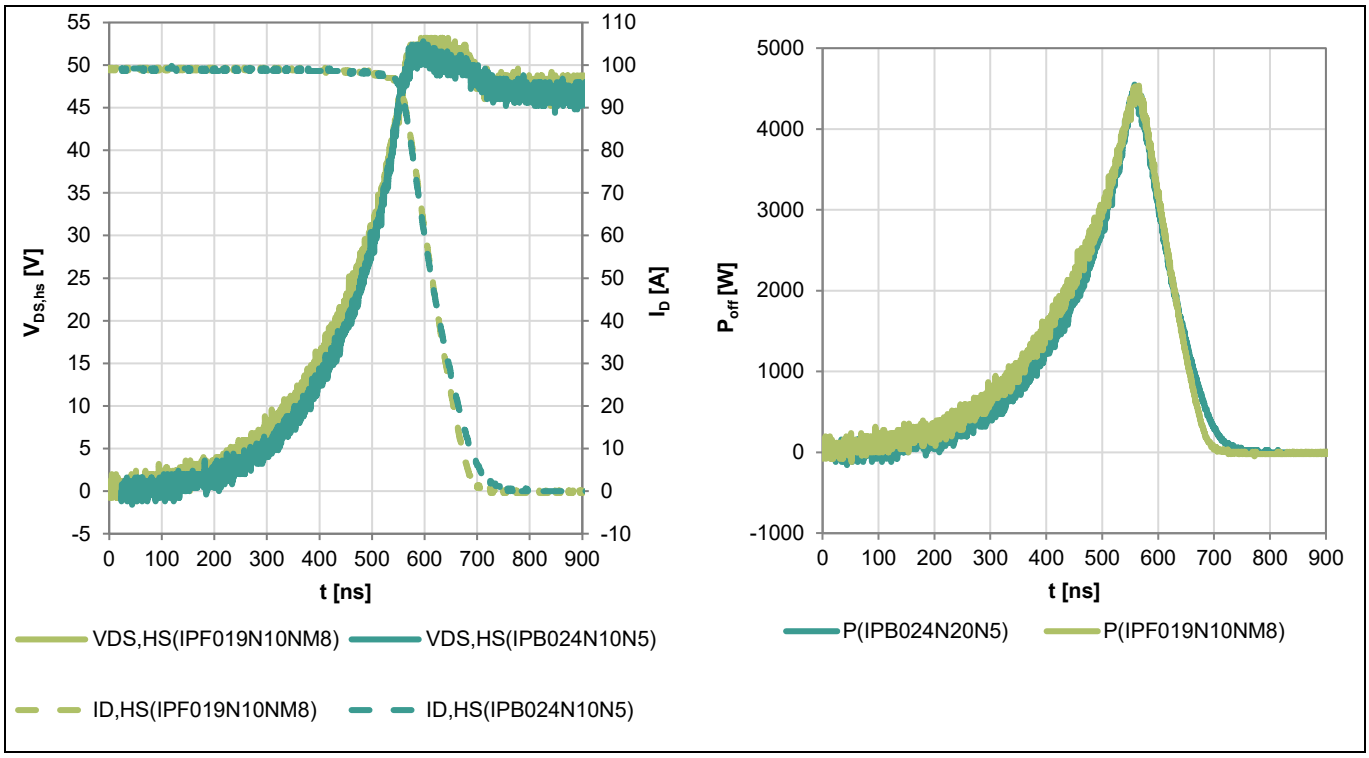


Figure 7 **Turn-off waveforms of OptiMOS™ 5 and OptiMOS™ 8 MOSFETs at I_D = 100 A; drain-source voltage and drain current (left) and instantaneous power (right)**

Table 5 summarizes the switching loss values for the high-side MOSFETs at an output current of 100 A.

Table 5 **Switching energies for the investigated MOSFETs at I_D = 100 A**

Device	Turn-on energy (48 V and 100 A)	Turn-off energy (48 V and 100 A)	Total switching energy
	µJ	µJ	µJ
OptiMOS™ 5 IPB024N10N5	513	837	1350
OptiMOS™ 8 IPF019N10NM8	465	899	1364

The gate drive circuits of both MOSFETs are adjusted to achieve comparable dv/dt and di/t values, resulting in similar total switching losses and similar voltage overshoot, oscillations, and EMI performance.

2.3.3.1 Total switching losses

Switching losses depend on the drain current (I_D). During one electrical period (T_{el}) of the IM, I_D varies continuously, leading to corresponding variations in switching losses. To determine the total switching losses of the MOSFETs for a given phase current, the analysis performs double-pulse tests for currents up to 200 A and calculates the switching losses for each current (see Figure 8).

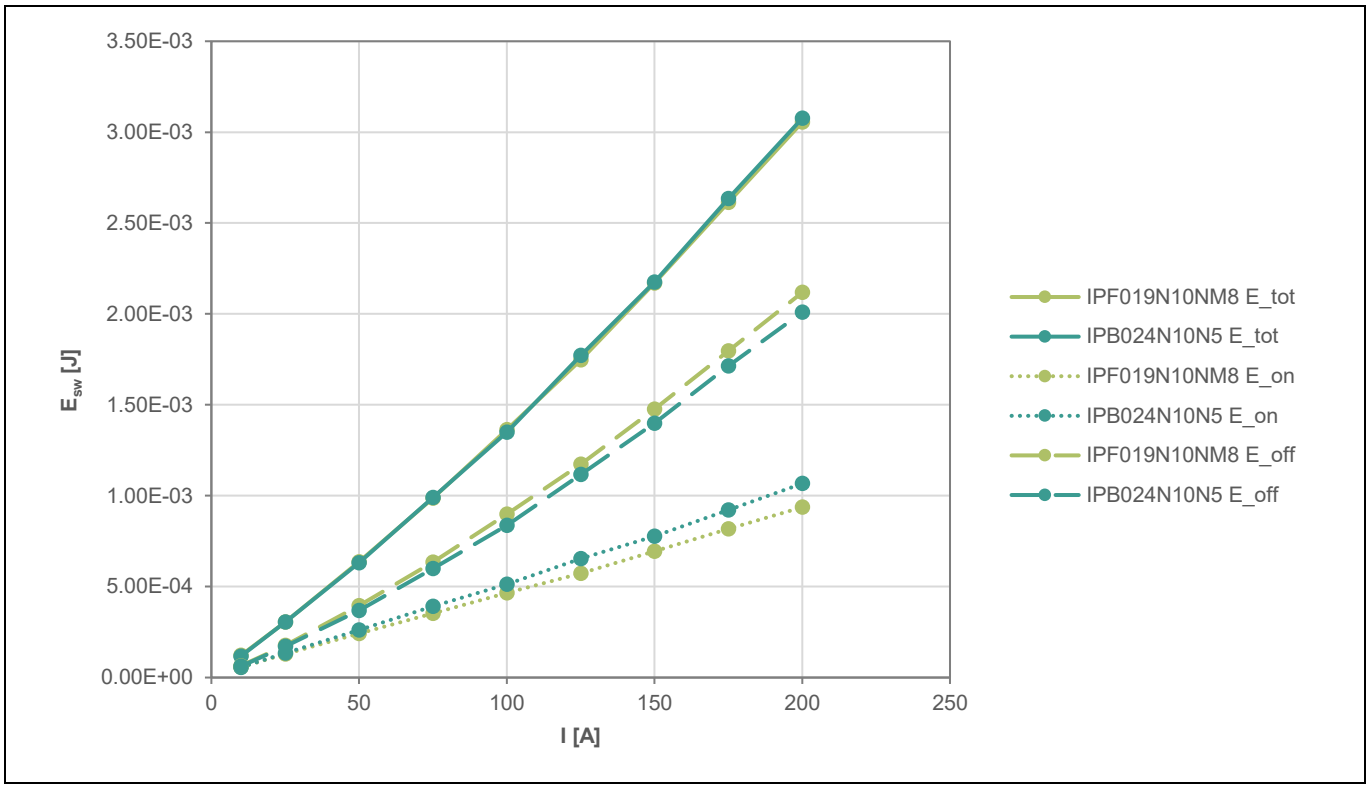


Figure 8 **Comparison of turn-on, turn-off, and total switching losses as a function of current for OptiMOS™ 5 and OptiMOS™ 8 MOSFETs**

During the free-wheeling intervals of the positive half-wave of the inverter output current, the current flows from source to drain of the low-side MOSFET. This condition forward-biases the body diode, and turning on the channel to reduces losses, results in soft switching. During turn-off, the current commutates back to the body diode, which also creates a soft-switching condition. As a result, only the high-side MOSFET undergoes hard switching during the positive half-wave of the phase current. During the negative half-wave, the current path reverses, and the low-side MOSFET becomes the hard-switching device. Therefore, only half of the electrical period needs to be considered when determining the switching losses.

The switching frequency ($T_{PWM} = 1/f_{PWM}$) defines the time between the two turn-on events and therefore, the position of the n^{th} switching event within the phase current waveform is defined. The amplitude of the drain current for the n^{th} switching event is given by:

$$\hat{I}_D(n) = \sqrt{2} I_{rms} \, sin\left(\frac{\pi}{n_{max}} n\right)$$

where n_{max} is defined by the ratio of the electrical frequency (T_{el}) and the switching period (T_{PWM})

$$n_{max} = \frac{T_{el}/_2}{T_{PWM}}$$

Equation 4 **Amplitude of the drain current for the n^{th} switching event**

The energy dissipated in the MOSFET ($E_{sw,n}$) for every single switching event is estimated by a quadratic interpolation of the measured switching losses. The switching loss is obtained by dividing the sum of the switching energies over one period of the drain current by T_{el}.

$$P_{sw} = \frac{\sum_{n}^{nmax} E_{sw,n}}{T_{el}}$$

Equation 5 Total switching losses

At an output current of 78.2 A, the OptiMOS™ 5 MOSFET shows switching losses of 28.2 W. The OptiMOS™ 8 MOSFET shows switching losses of 29.6 W at a higher output current of 81.6 A.

Table 6 Total switching losses for the investigated MOSFETs at 100°C

Device	100°C
	P_{sw}
	W
OptiMOS™ 5 IPB024N10N5	28.2 W at 78.2 A
OptiMOS™ 8 IPF019N10NM8	29.6 W at 81.6 A

2.3.4 Total losses

Figure 9 compares the conduction and switching losses of OptiMOS™ 5 and OptiMOS™ 8 MOSFETs at a case temperature of 100°C. Compared to the OptiMOS™ 5 MOSFET, the OptiMOS™ 8 MOSFET enables a 4.3% increase in inverter output current while maintaining the same MOSFET case temperature and achieving higher efficiency (see Figure 9).

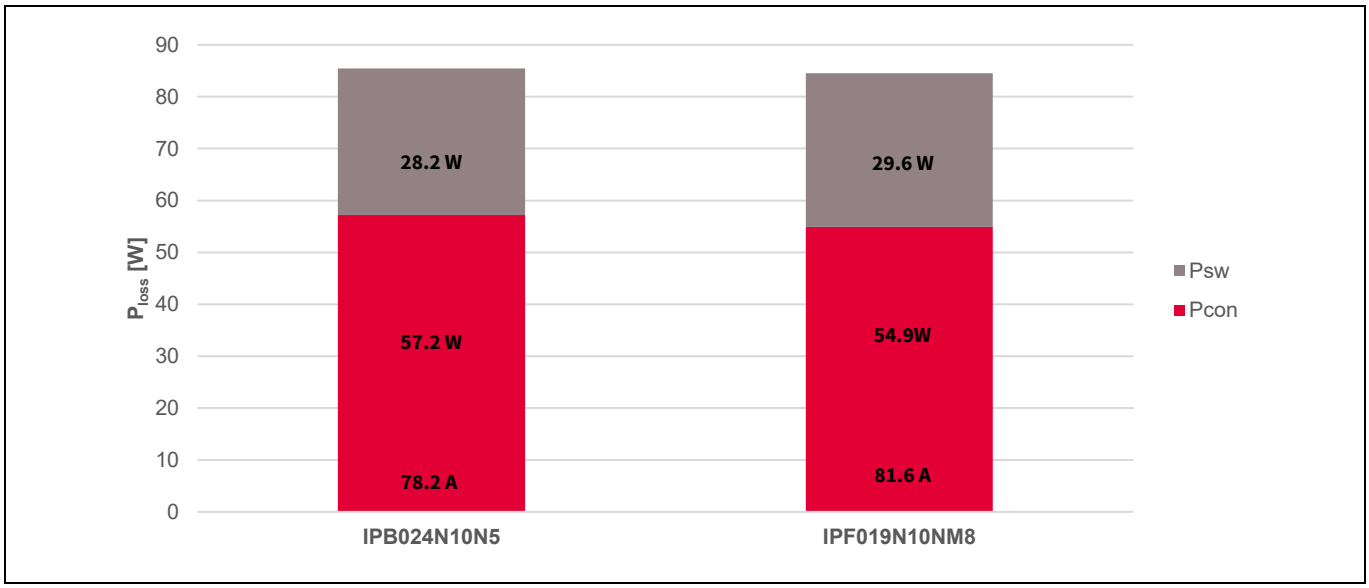


Figure 9 Comparison of the switching and conduction losses of OptiMOS™ 5 and OptiMOS™ 8 MOSFETs for a heatsink temperature of 100°C

As shown in Figure 8, the switching losses increase with increasing current. This increase limits the achievable rise in inverter output current to a value lower than that expected from the reduction in $R_{DS(on)}$.

2.4 Switching loss – gate charge considerations

As discussed in Section 2.1, the MOSFET gate exhibits capacitive behavior during the turn-on and turn-off events. At each turn-off event, the gate-drive circuit dissipates the energy stored in the gate capacitance, which is proportional to the total gate charge (Q_g) and the gate-drive voltage (V_g).

$$E_g = \frac{1}{2} Q_g V_g$$

Equation 6 Energy stored in the gate capacitance of a MOSFET

Extending the above equation by incorporating the switching frequency f_{sw} gives the total power loss resulting from charging and discharging the gate capacitance.

$$P_g = \frac{1}{2} Q_g V_g f_{sw}$$

Equation 7 Gate-drive power losses

Comparing the two investigated MOSFETs, Q_g increases by 11.6% from 138 nC for OptiMOS™ 5 MOSFET to 154 nC for OptiMOS™ 8 MOSFET at V_{GS} = 10 V. Since P_g scales linearly with Q_g, the gate-drive losses also increase by 11.6% for OptiMOS™ 8 MOSFET. At first glance, this increase appears unfavorable. However, when comparing the absolute values of the gate-drive losses with the other loss components discussed above, they can be considered negligible. For example, at V_g = 10 V and f_{sw} of 10 kHz, the gate-drive losses increase from 6.9 mW for OptiMOS™ 5 MOSFET to 7.7 mW for OptiMOS™ 8 MOSFET per device, and from 41.4 mW to 46.2 mW for the whole inverter, respectively. In comparison, the total MOSFET losses due to switching and conduction are 85.5 W for OptiMOS™ 5 MOSFET at an inverter output current of 78.2 A and 84.5 W for OptiMOS™ 8 MOSFET at an inverter output current of 81.6 A. Therefore, the $R_{DS(on)}$ reduction of the new OptiMOS™ 8 technology outweighs the increase of the gate drive losses by far.

2.5 Peak power

So far, the MOSFETs have only been compared under thermal steady-state condition. However, for motor drives in general, the peak power of the inverter is also an important performance parameter. Accelerating, lifting heavy loads, or driving uphill are typical examples of peak-power events. During such peak-power or overload events, much higher losses than those under steady state conditions are dissipated in the MOSFET. Consequently, the MOSFET will heat up further, and the duration of this event must be limited to avoid MOSFET overstress. The allowable peak-power duration depends on the system's thermal impedance, the starting conditions, and the losses dissipated in the MOSFET.

To evaluate the peak-power capability of the investigated MOSFETs, the inverter operates at currents exceeding the nominal value, and the resulting increase in MOSFET case temperature over time ($\Delta T/\Delta t$) is used as the performance parameter. Figure 10 compares the peak-power capability of the two investigated MOSFETs.

The lower ΔT/Δt indicates that the OptiMOS™ 8 MOSFET outperforms OptiMOS™ 5 MOSFET under all investigated overload conditions. A lower ΔT/Δt at a constant phase current enables a longer allowable overload duration.

Thus, for the same maximum case temperature, the system can either extend the overload duration or support a higher output current for the same duration. Note that as for the steady state tests, the absolute values depend on the cooling system, for example, the heatsink size.

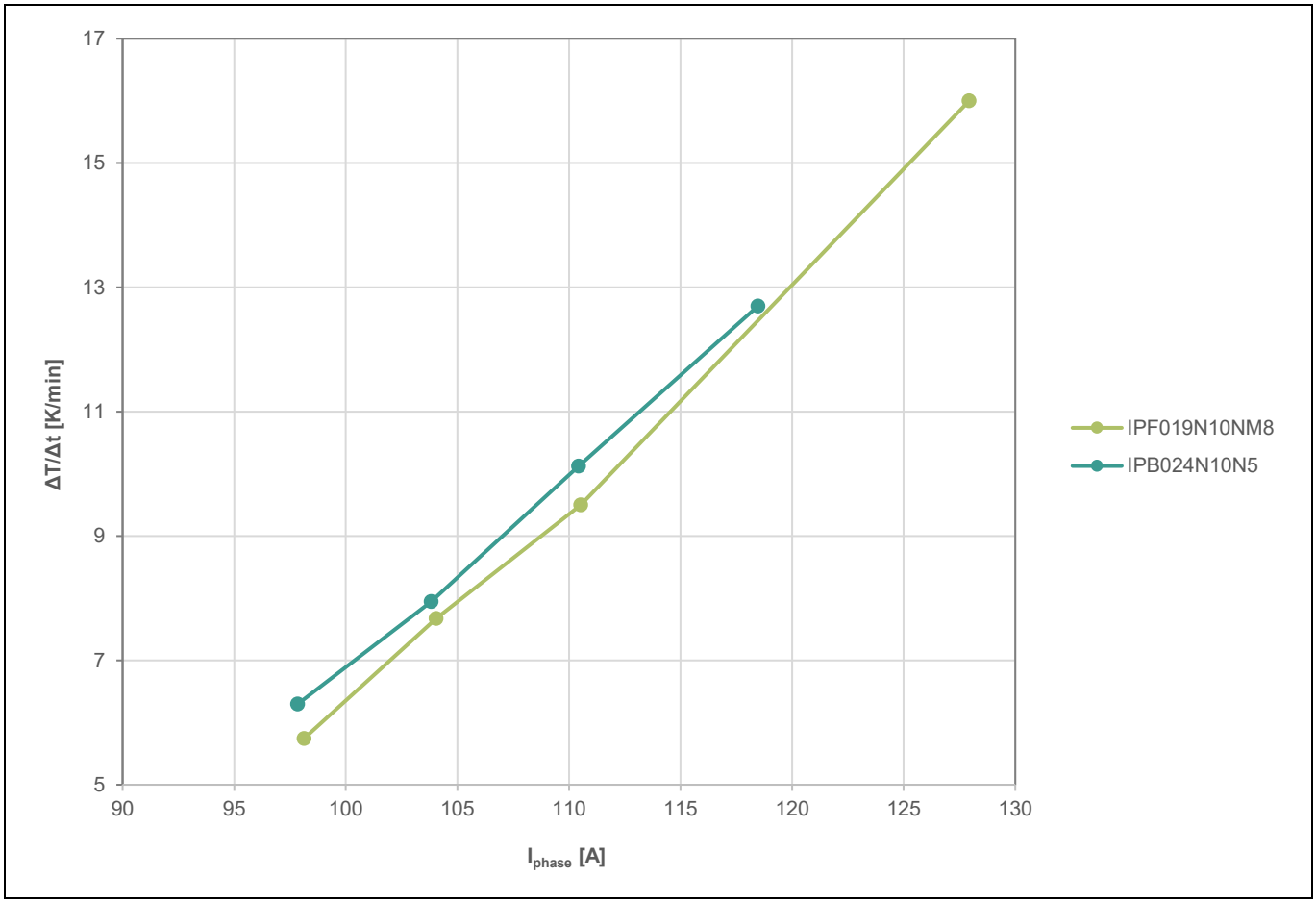


Figure 10 Temperature rise over time as a function of phase current

A comparison of the curvature of the OptiMOS™ 5 and OptiMOS™ 8 MOSFET characteristics suggests a potential intersection point, where the OptiMOS™ 5 MOSFET could exhibit a lower ΔT/Δt. However, this assumption relies on a linear interpretation and neglects the quadratic increase in conduction losses. In practice, the OptiMOS™ 5 MOSFET cannot achieve the same overload current as the OptiMOS™ 8 MOSFET. Thus, thermal limitations require stopping the tests for the OptiMOS™ 5 MOSFET at a lower current than for the OptiMOS™ 8 MOSFET.

3 Battery protection unit

The introduction of lithium-based batteries has significantly increased runtimes and output power, making battery-powered solutions highly attractive across a wide range of applications. These performance improvements have made such systems fully competitive with gasoline-powered equipment and have enabled new use cases, including light electric vehicles (LEVs). As a result, the number of batteries in use has grown steadily in recent years, further accelerated by the ongoing transition from gasoline-powered to battery-powered devices.

To protect these batteries from damage caused by overload or short-circuit conditions, designers use dedicated battery protection units (BPU). The BPU typically forms part of the battery management system (BMS), which monitors and controls battery parameters, such as state of charge, voltage, and temperature. During a fault event, the BPU disconnects the battery from the load to prevent damage. This is typically implemented using power MOSFETs connected in a back-to-back configuration, as shown in Figure 11. To maximize runtime and minimize temperature rise caused by conduction losses, the MOSFET must provide the lowest possible $R_{DS(on)}$. For higher-power battery systems, multiple MOSFETs are connected in parallel to further reduce the effective on-state resistance. In these applications, the new OptiMOS™ 8 MOSFET delivers excellent performance due to its exceptionally low $R_{DS(on)}$.

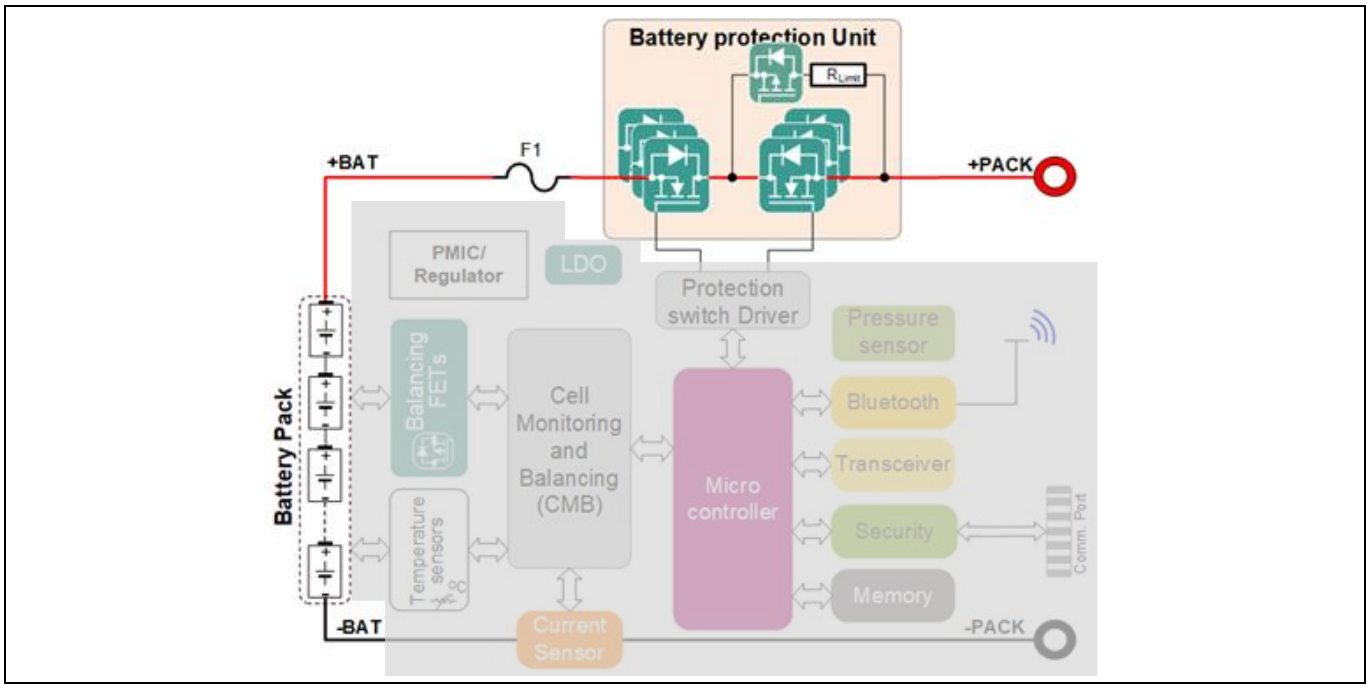


Figure 11 Typical battery management system with the back-to-back protection MOSFETs as a part of the BPU

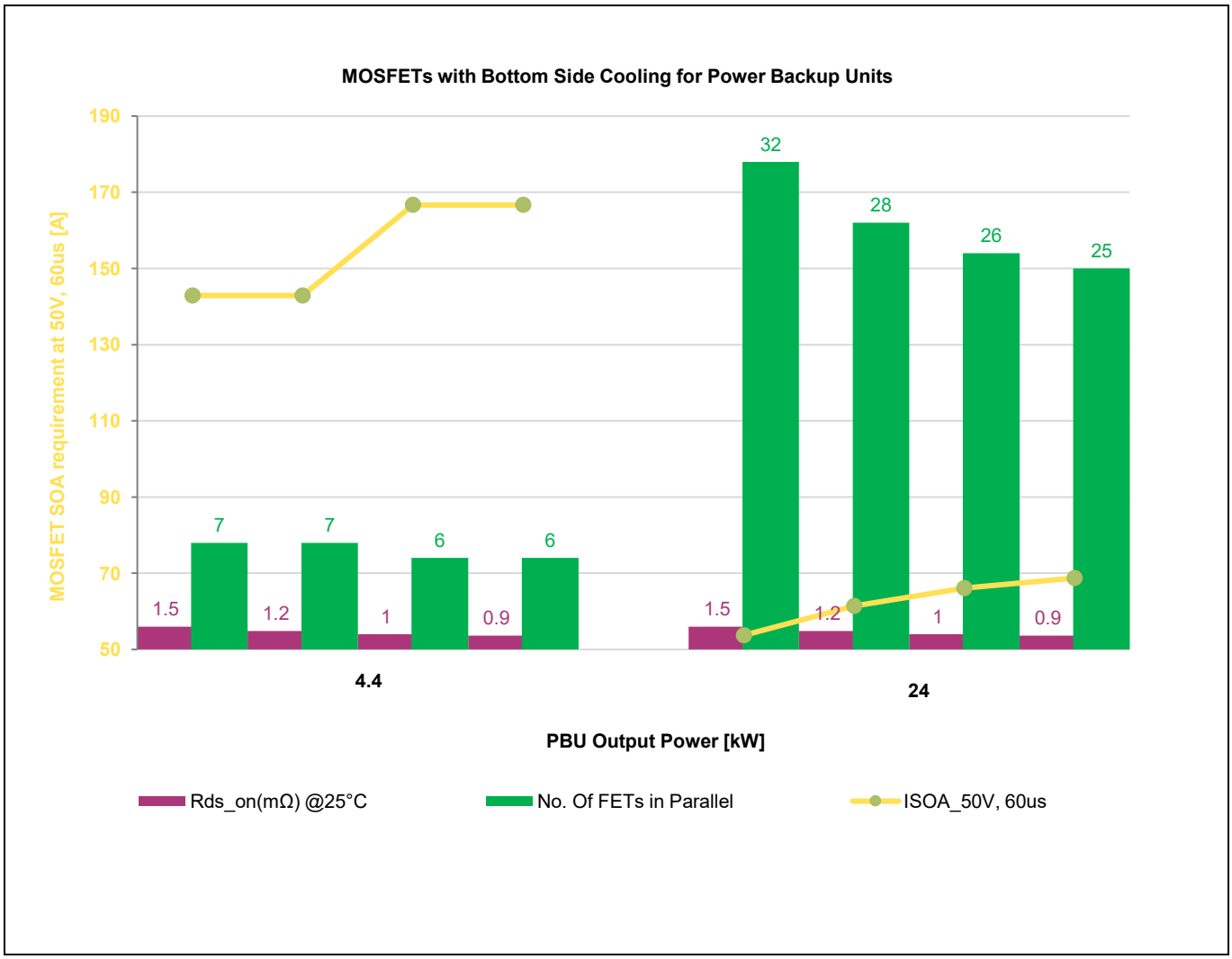


Figure 12 $R_{DS(on)}$ - SOA dependency for BPU systems with 4.4 kW and 24 kW output power

Increasing the battery output power while maintaining a constant voltage increases the output current that the BPU must handle. Figure 12 compares the number of paralleled MOSFETs required for different $R_{DS(on)}$ values and power levels, as well as resulting safe operating area (SOA) requirement per MOSFET. As indicated by the green bars, for a constant $R_{DS(on)}$, the required number of paralleled MOSFETs increases with the increasing output power. As a result, the current carried by each individual MOSFET decreases. Thus, the SOA requirement for each MOSFET is reduced.

To maintain acceptable system losses, the design increases the number of paralleled MOSFETs as the power level rises, which in turn reduces the SOA requirement per device. A comparison of SOA demand per MOSFET at power levels of 4.4 kW and 24 kW, using 0.9 mΩ MOSFETs, shows that the required SOA current decreases from 167 A per device to approximately 69 A per device. This observation indicates that MOSFET paralleling in high power BPUs primarily serves to achieve low $R_{DS(on)}$ rather than high short circuit handling capability.

Setting a new industry standard with Infineon's latest trench MOSFET innovation

Battery protection unit

As indicated by Figure 12 , increasing power demands in modern battery systems require very low $R_{DS(on)}$ values to minimize conduction losses and maximize runtime. The new OptiMOS™ 8 MOSFET, with its industry-leading $R_{DS(on)}$, addresses these requirements effectively. A key advantage of low $R_{DS(on)}$ MOSFETs in high-power BPUs lies in their ability to reduce system losses without compromising reliability or performance. This reduction improves battery lifetime and simplifies thermal management. By using these benefits of low $R_{DS(on)}$ MOSFETs, designers can develop BPUs that meet the demanding requirements of modern batteries and support the broader adoption of battery-powered technologies.

4 Conclusion

This application note introduces the 100 V OptiMOS™ 8 power MOSFET family, designed using Infineon's advanced trench MOSFET technology. The redesigned MOSFET cell provides industry-leading $R_{DS(on)}$, making the 100 V OptiMOS™ 8 power MOSFET well suited for applications where conduction losses dominate and high efficiency is critical, such as motor drives and battery protection solutions. By significantly reducing power losses, the device enables higher usable output power in motor control applications and extends runtime in battery-powered systems, directly translating electrical efficiency into tangible system-level benefits.

Beyond improving efficiency, the very low $R_{DS(on)}$ simplifies system design by reducing the number of paralleled MOSFETs, easing thermal management, and enabling more compact and cost-effective implementations. The resulting reduction in heat generation and current-sharing requirements can also enable migration from an IMS PCB to an FR4 PCB, supporting simpler manufacturing and an improved overall price-to-performance ratio.

Combined with a broad range of $R_{DS(on)}$ classes and package options, the 100 V OptiMOS™ 8 power MOSFET provides a straightforward upgrade path from previous-generation MOSFETs. This enables designers to maintain output power while improving the overall price-to-performance ratio or to achieve additional performance headroom at comparable cost. In summary, the 100 V OptiMOS™ 8 power MOSFET enables the development of more efficient, robust, and cost-competitive end products, not only in motor drive and battery protection applications, but also in any application dominated by conduction losses.

5 Related resources

- 100 V OptiMOS™ 8 power MOSFETs
- Developer Community

References

[1] Infineon Technologies AG: *100 V OptiMOS™ 8* power *MOSFETs*; Available online

[2] Infineon Technologies AG: *Paralleling power MOSFETs*; Available online

[3] Infineon Technologies AG: *Industrial and consumer BMS*; Available online

Revision history

Document revision	Date	Description of changes
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