5.5 kW three-phase interleaved LLC converter with 650 V CoolSiC™ TOLT

EVAL_5K5W_3PH_LLC_SIC2

About this document

Scope and purpose

This document introduces the design and performance of a high-efficiency and high-density LLC converter for server and datacenter applications. The EVAL_5K5W_3PH_LLC_SIC2 Evaluation Board (Figure 1) is a 5.5 kW three-phase interleaved LLC converter. The output voltage is regulated at 50 V. The input voltage ranges from 380 V to 420 V DC in normal operation. It can be operated down to 360 V for short time to support the hold-up time requirement when the design is part of a full PSU. The board achieves a peak efficiency of almost 99 percent and a power density of 170 W/in^3, enabled by the outstanding performance of Infineon semiconductor devices.

The evaluation board uses 650 V CoolSiC™ G2 MOSFETs on the primary side, which offer significantly better figures of merit than the silicon counterparts, increasing both efficiency and power density. The top-side cooled package decouples heat transfer from the PCB, allowing to optimize both electrical path and thermal path. 80 V OptiMOS™ 6 MOSFETs are used as synchronous rectifiers. The superior performance of OptiMOS™ 6 thin-wafer technology results in very low conduction losses and driving losses, leading to high efficiency.

The Infineon components used in the EVAL_5K5W_3PH_LLC_SIC2 are:

- CoolSiC™ 650 V, 50 mΩ TOLT (IMLT65R050M2H), and EiceDRIVER™ 2EDR9259X on primary side
- OptiMOS™ 80 V, 1.8 mΩ SuperSO8 (ISC018N08NM6), and EiceDRIVER™ 2EDF5215F on secondary side
- XMC4400-F100K256 microcontroller for the implementation of LLC control
- CoolSET™ Integrated power management IC (ICE5QR2280BG-1) for auxiliary power supply

Intended audience

The document and related EVAL_5K5W_3PH_LLC_SIC2 hardware are intended for power supply design engineers, and Infineon customers who want to evaluate the performance of Infineon products.

Compact and highly efficient 5.5 kW three-phase interleaved LLC converter

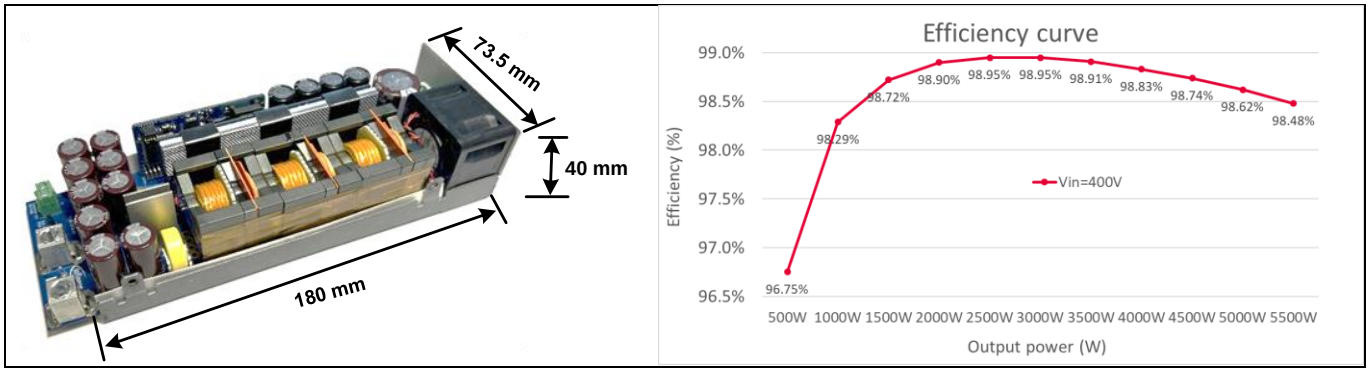

Figure 1 5.5 kW three-phase interleaved LLC converter: picture and efficiency curve

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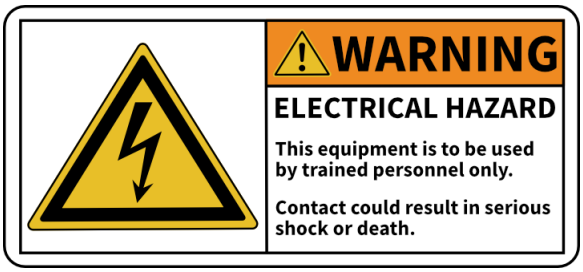
Safety information

Please read this document carefully before starting up the device.



Important notice

Evaluation boards, demonstration boards, reference boards and kits are electronic devices typically provided as an open-frame and unenclosed printed circuit board (PCB) assembly. Each board is functionally qualified by electrical engineers and strictly intended for use in development laboratory environments. Any other use and/or application is strictly prohibited. Our boards and kits are solely for qualified and professional users who have training, expertise, and knowledge of electrical safety risks in the development and application of high-voltage electrical circuits. Please note that evaluation boards, demonstration boards, reference boards and kits are provided “as is” (i.e., without warranty of any kind). Infineon is not responsible for any damage resulting from the use of its evaluation boards, demonstration boards, reference boards or kits. To make our boards as versatile as possible, and to give you (the user) opportunity for the greatest degree of customization, the virtual design data may contain different component values than those specified in the bill of materials (BOM). In this specific case, the BOM data has been used for production. Before operating the board (i.e. applying a power source), please read the application note/user guide carefully and follow the safety instructions. Please check the board for any physical damage, which may have occurred during transport. If you find damaged components or defects on the board, do not connect it to a power source. Contact your supplier for further support. If no damage or defects are found, start the board up as described in the user guide or test report. If you observe unusual operating behavior during the evaluation process, immediately shut off the power supply to the board and consult your supplier for support.

Operating instructions

Do not touch the device during operation, keep a safe distance. Do not touch the device after disconnecting the power supply, as several components may still store electrical voltage and can discharge through physical contact. Several parts, like heatsinks and transformers, may still be very hot. Allow the components to discharge and cool before touching or servicing. All work such as construction, verification, commissioning, operation, measurements, adaptations, and other work on the device (applicable national accident prevention rules must be observed) must be done by trained personnel. The electrical installation must be completed in accordance with the appropriate safety requirements.

Safety precautions

Note: *Please note the following warnings regarding the hazards associated with development systems.*

Table 1 **Safety precautions**

	**Warning:** *The evaluation or reference board contains DC bus capacitors, which take time to discharge after removal of the main supply. Before working on the converter system, wait five minutes for capacitors to discharge to safe voltage levels. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Warning:** *The evaluation or reference board is connected to the AC input during testing. Hence, high-voltage differential probes must be used when measuring voltage waveforms by oscilloscope. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Warning:** *Remove or disconnect power from the converter before you disconnect or reconnect wires, or perform maintenance work. Wait five minutes after removing power to discharge the bus capacitors. Do not attempt to service the drive until the bus capacitors have discharged to zero. Failure to do so may result in personal injury or death.*
	**Caution:** *The heatsink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.*
	**Caution:** *Only personnel familiar with the converter, power electronics and associated equipment should plan, install, commission, and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.*
	**Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	**Caution:** *A converter that is incorrectly applied or installed can lead to component damage or reduction in product lifetime. Wiring or application errors such as undersizing the cabling, supplying an incorrect or inadequate AC supply, or excessive ambient temperatures may result in system malfunction.*

1 System overview

1.1 Background

With the rapid evolution of artificial intelligence (AI), new and powerful AI processors are consuming very high current at very low voltages, pushing the power demand of server rack growing substantially. The power of each power supply unit (PSU) in the server rack has been increased from 3 kW to 5.5 kW. High efficiency is a key requirement for the PSU, which not only minimizes heat dissipation, but also reduces lifetime operating costs. High power density is also required as the space of the rack is limited.

LLC converter has been widely used in server PSU for voltage step down and Galvanic isolation. Single LLC converter is typically designed for 3 kW output power. To further increase the power level, three-phase interleaved LLC converter [1] can be employed. The three-phase interleaved LLC converter has improved current sharing due to coupled operation among the phases. It also greatly reduces the output ripple by interleaved operation. This document introduces the superior performance of a 5.5 kW three-phase interleaved LLC board enabled by Infineon semiconductor devices.

1.2 Functional description

Figure 2 shows a block diagram of the three-phase interleaved LLC. It consists of three half-bridges on the primary, three full-bridge rectifiers on the secondary, resonant capacitors in delta connection, and integrated magnetics including three resonant inductors and three transformers. The capacitors in delta connection have only 1/3 of the capacitance compared to Y connection, which reduces PCB space. The capacitor RMS current in delta connection is also smaller ($I_{Cr\_\Delta} = I_{Cr\_Y}/\sqrt{3}$). The capacitor AC voltage is larger ($V_{CrAC\_\Delta} = V_{CrAC\_Y} \cdot \sqrt{3}$), but there is zero DC offset (in contrast to Vin/2 offset in Y connection), which makes the overall capacitor voltage stress smaller in delta connection.

The output voltage of the converter is regulated at 50 V. The input voltage ranges from 380 V to 420 V DC in normal operation. It can be operated down to 360 V for short time to support hold-up time requirement when the design is part of a full PSU. The resonant frequency of this design is 200 kHz. The switching frequency varies from 130 kHz to 360 kHz. 650 V CoolSiC™ G2 IMLT65R050M2H is used on the primary and 80 V OptiMOS™ 6 ISC018N08NM6 is used on the secondary as synchronous rectifiers. The very low Qoss of CoolSiC™ G2 reduces the required magnetizing current or shortens the dead-time, which results in reduced conduction losses or the possibility of higher frequency design to improve power density. The low Rds(on) and Qg of OptiMOS™ 6 enables easier thermal design and less paralleling, leading to high system-efficiency. Reinforced isolated gate driver 2EDR9259X is used to drive the primary switches across the isolation boundary as the controller is located on the secondary side. 2EDF5215F is used to drive the low-voltage synchronous rectifiers. Quasi-Resonant integrated power IC ICE5QR2280BG-1 is used to generate the primary 18 V and secondary 12 V gate driving voltage.

The control is implemented with XMC4400 microcontroller, which includes voltage regulation functionality, burst mode operation, over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), soft-start, SR control, and adaptive dead-times (primary bridge and SRs).

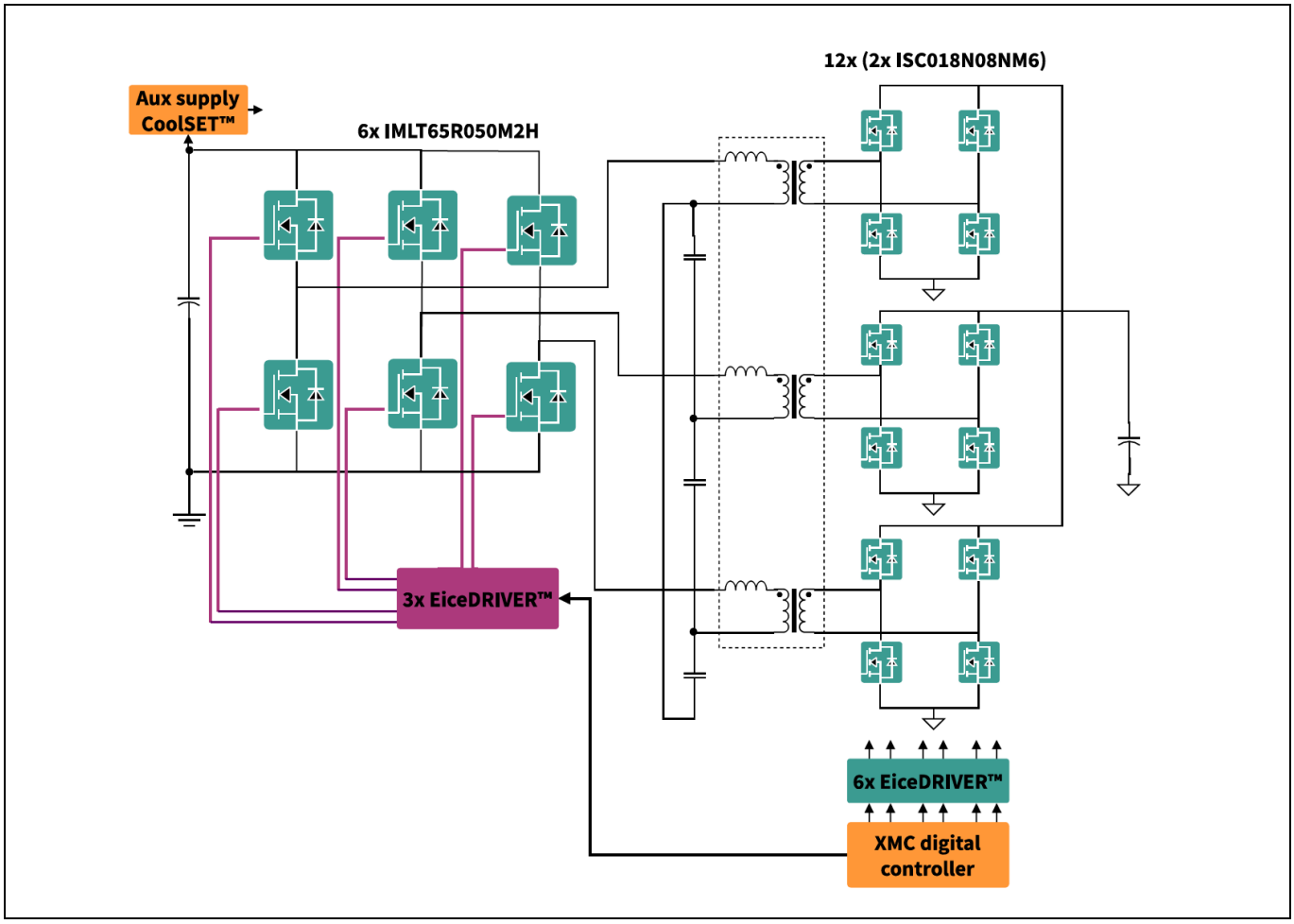


Figure 2 Block diagram of the 5.5 kW three-phase interleaved LLC

1.3 Operation at resonance

Multi-phase interleaved operation is typically employed for high-power applications. For multi-phase LLC converter simply connected in parallel, each phase is independent, and current sharing is highly sensitive to the tolerance of resonant components. This is because the gain of LLC is determined by frequency as well as load. When multiple phases are connected in parallel, they have the same gain. The tolerance of resonant components causes different resonant frequencies, leading to different load current. The further away from the resonant point, the worse of current unbalance.

In the three-phase LLC with Y or delta connection, the neutral line is removed, and each phase is not independent anymore. Figure 3 shows the equivalent circuit and the operation at resonance. In half cycle, each phase has three operation modes at the resonant point. As can be seen in Figure 3, for phase A, it is not just Lr, and Cr in phase A doing resonance. Lr and Cr in other phases are also involved. For phase B and C, similar coupled resonant operation can be seen. Due to coupling of the resonant components among the phases, the tolerance of resonant components becomes not so sensitive, which greatly improves current sharing capability.

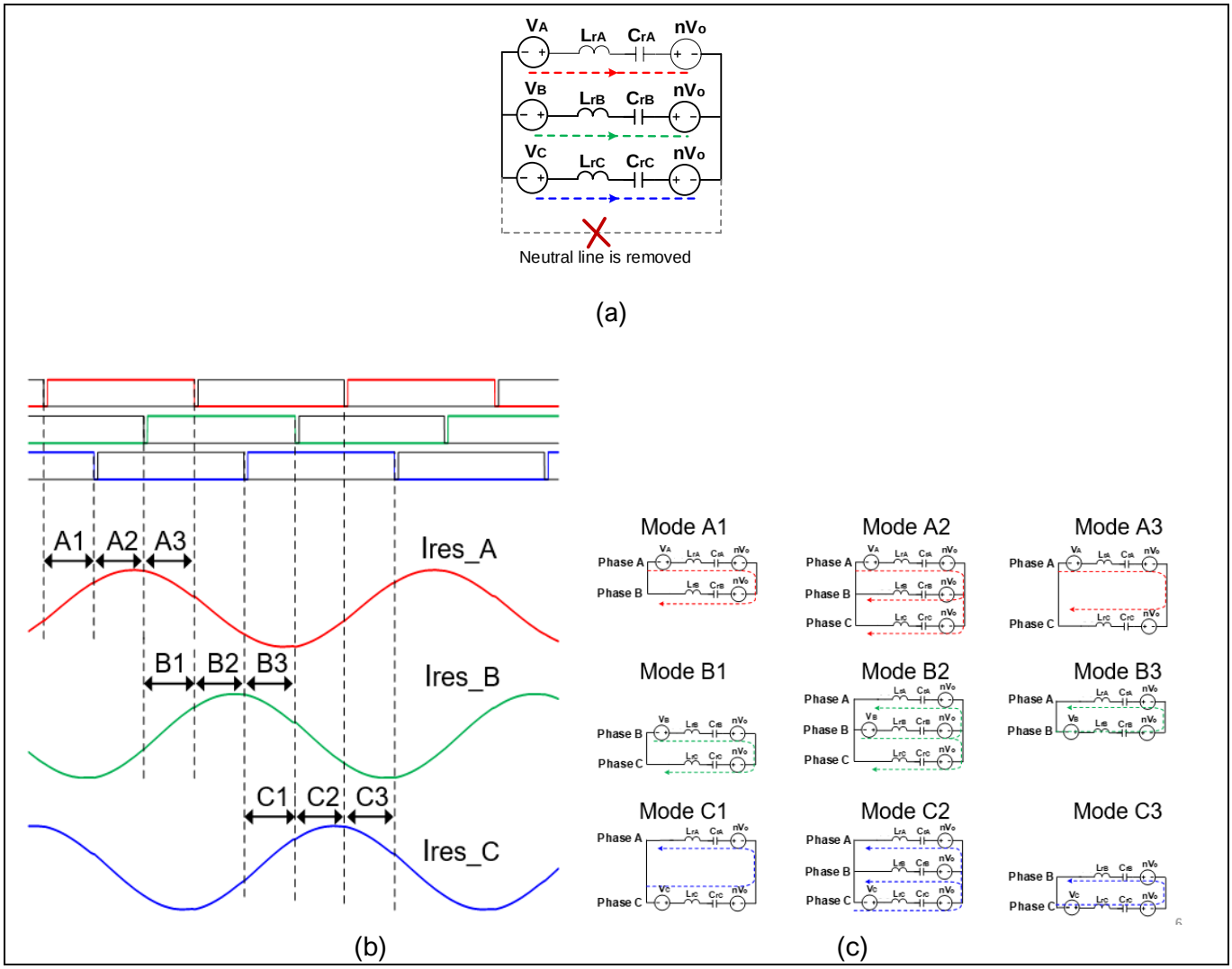


Figure 3 **Three-phase interleaved LLC at resonant point: (a) equivalent circuit; (b) waveforms; (c) operation modes**

1.4 Resonant tank design considerations

The design of resonant tank in three-phase LLC is the same as in single LLC converter. The design goal is to meet the regulation range while achieving best efficiency. Smaller inductance ratio (Ln=Lm/Lr) can achieve wider regulation range, but smaller Ln typically leads to smaller Lm, which causes high conduction losses since the rms currents in primary FETs, secondary FETs and magnetic windings are all related to Lm. Larger Ln makes it hard to regulate at high line (buck mode) light load, though burst mode control can be used to maintain the output voltage. Larger Ln also leads to wider frequency variation: at low line full load, the lower frequency results in higher rms currents, causing more thermal stress; at high line light load, the higher frequency results in less magnetizing current, which makes it hard to fully charge/discharge Coss to achieve ZVS as inductive energy could be less than capacitive energy. Therefore, a trade-off of Ln needs to be made between efficiency and operation range.

Once Ln is selected, Q can be found by the peak gain requirement. Note that the attainable peak gain obtained in First Harmonic Approximation (FHA) method is underestimated. The real LLC peak gain is higher than FHA predicts. For more accurate and optimal results, peak gain curves generated from circuit simulation could be used. A few iterations are needed to reach an optimized design. On this board, resonant frequency is 200 kHz. Magnetizing inductance is 63 µH. Resonant inductance (including transformer leakage) is 7.1 µH.

The equivalent resonant capacitance in single phase is 90 nF. In three-phase Cr delta connection, the capacitance becomes one-third, which is 30 nF.

1.5 CoolSiC™ features

CoolSiC™ MOSFETs offer significantly better figures of merit than the Silicon counterparts, allowing to increase both efficiency and power density. The characteristics comparison of IMLT65R050M2H, IPW65R060CM8, and IPT65R060CFD7 is shown in Figure 4. All of them have similar Rdson (typ. ~50 mOhm and max. ~60 mOhm). Firstly, CoolSiC™ Gen 2 has a linear and much lower output charge. It either reduces the needed circulating current or shortens the dead-time in LLC converter, which results in reduced power losses or the possibility of higher frequency design to improve power density. Secondly, CoolSiC™ Gen 2 has smaller temperature dependency of on-resistance, leading to lower conduction losses, which makes it the prime choice for high-current applications. Thirdly, the low gate charge and fast switching of CoolSiC™ Gen 2 help reduce gate driving loss and turn-off loss in LLC converter, further improving efficiency. Finally, CoolSiC™ Gen 2 has significantly lower reverse recovery charge. It reduces the risk of device failure in LLC converter due to hard commutation that may occur during startup, overload, or short-circuit conditions, thus improving system reliability. More details of CoolSiC™ can be found in [2].

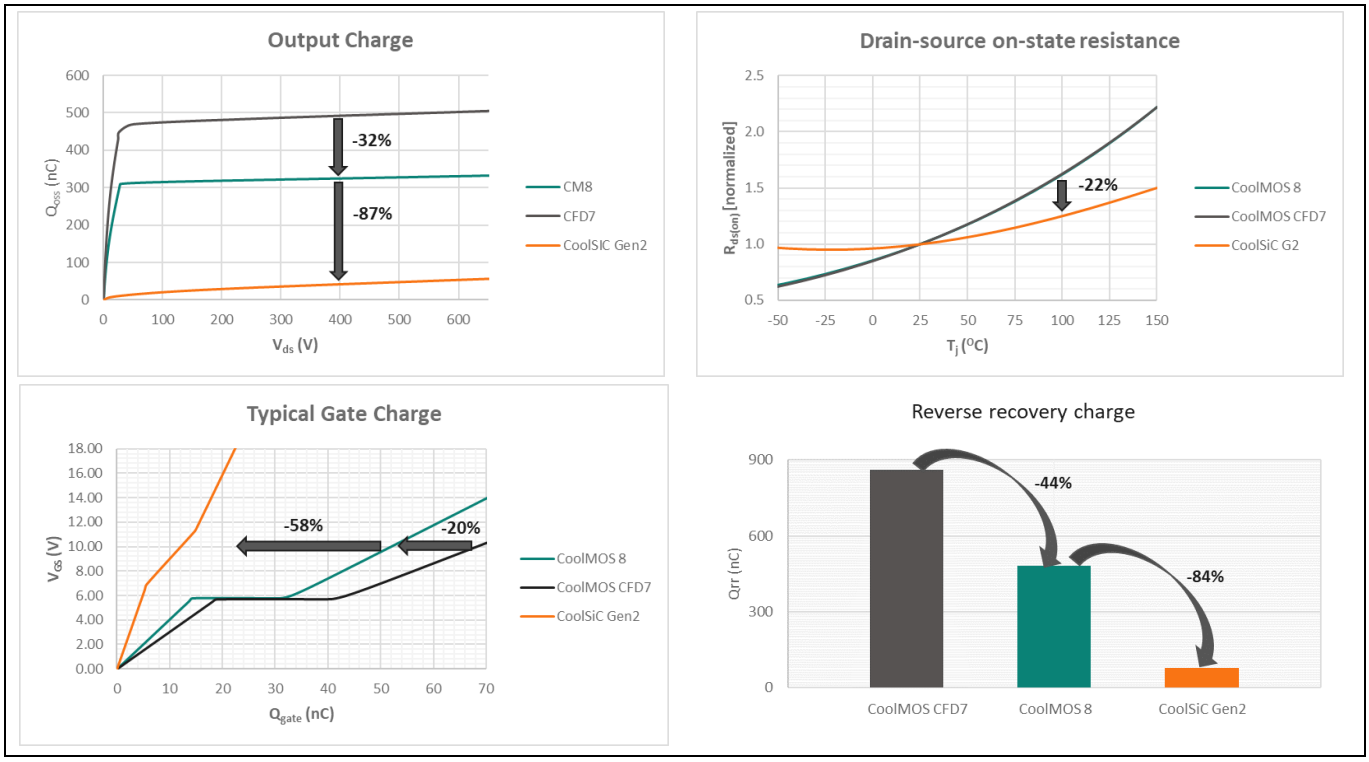


Figure 4 Comparison of CoolSiC™ Gen 2, CoolMOS™ 8, and CoolMOS™ CFD7

1.6 Top-side cooling package

Figure 5 shows a comparison of heat transfer in bottom-side cooling and top-side cooling. For bottom-side cooling packaged devices (like TOLL), thermal vias need to be placed on PCB, so that heat generated by the device can be transferred through thermal vias to the heatsink. Total thermal resistance depends on the size and number of the vias as well as PCB thickness. As PCB is involved in the thermal path, PCB typically has high temperature.

In contrast, for top-side cooling packaged devices (like TOLT), heat directly flows into heatsink from the top side. As PCB is decoupled from the thermal path, total thermal resistance can be lower, which means it allows either higher power dissipation or smaller heatsink. System lifetime can also be improved due to reduced PCB temperature. More details of top-side cooled devices can be found in [3].

Top-side cooling also separates electrical path from thermal path. From PCB layout point of view, as thermal vias are not needed, the return path can be placed directly under the devices, as seen in Figure 6, which minimizes the loop inductance [4]. Unlike bottom-side cooling, where components are placed only on one side of PCB and the other side are occupied by heatsink, top-side cooling allows components placed on both sides of PCB, which means more assembly areas and more layout flexibility.

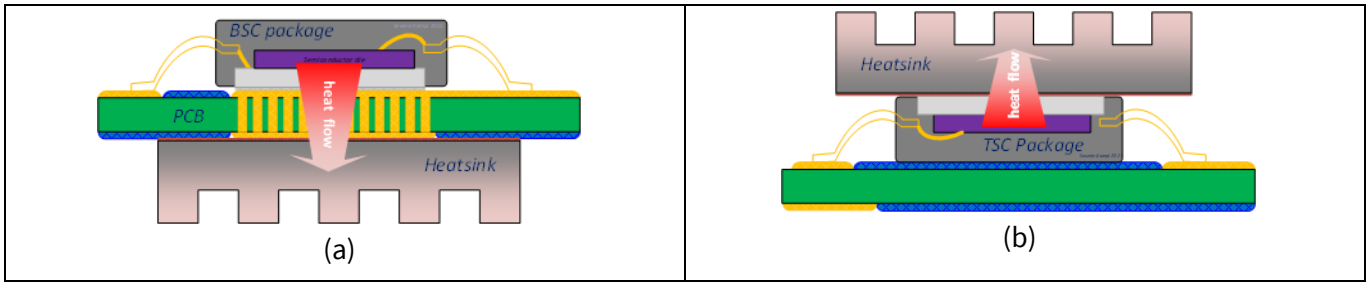


Figure 5 Heat transfer in (a) bottom-side cooling and (b) top-side cooling

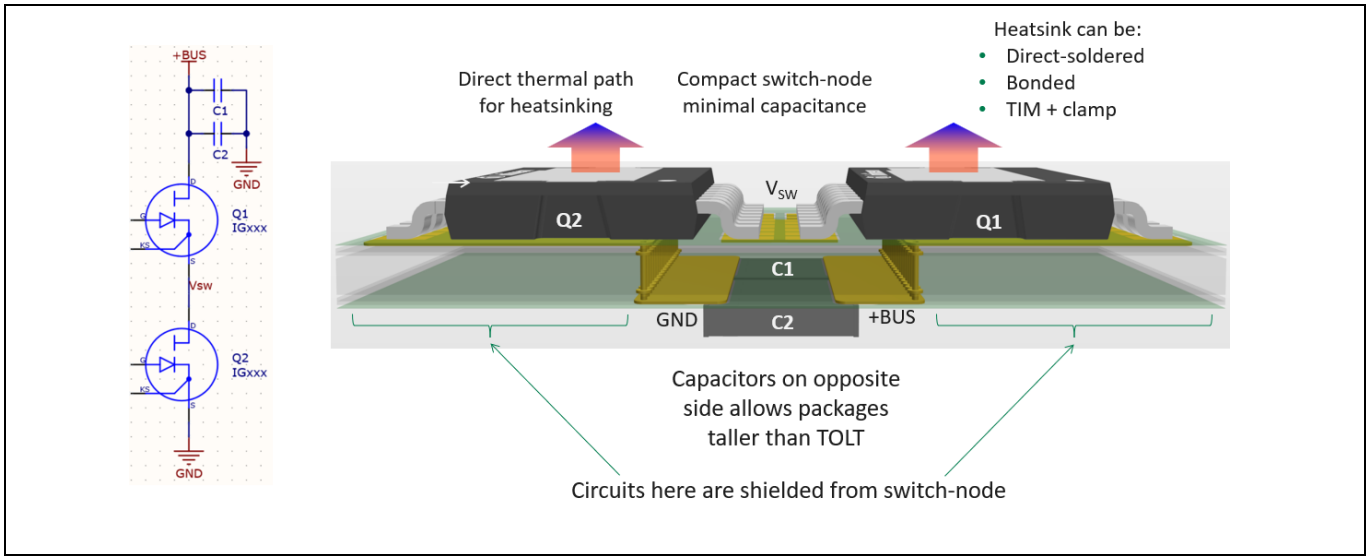


Figure 6 Top-side cooling allowing electrical layout optimization

1.7 LLC control and startup

Figure 7 shows the digital control of the LLC converter. The PID controller outputs a delta period, which is appended to the minimum period, resulting in the final LLC period for control. This period value is fed to the timer of digital controller and generates PWMs. Compared to frequency modulation typically used in analogue control (where PWMs are generated by frequency-related signal), the period modulation in digital control achieves better control performance across the line range. This is because the modulator gain in period modulation is non-linear, which can partially compensate the gain variation of LLC small signal model when line voltage changes, as seen in Figure 8.

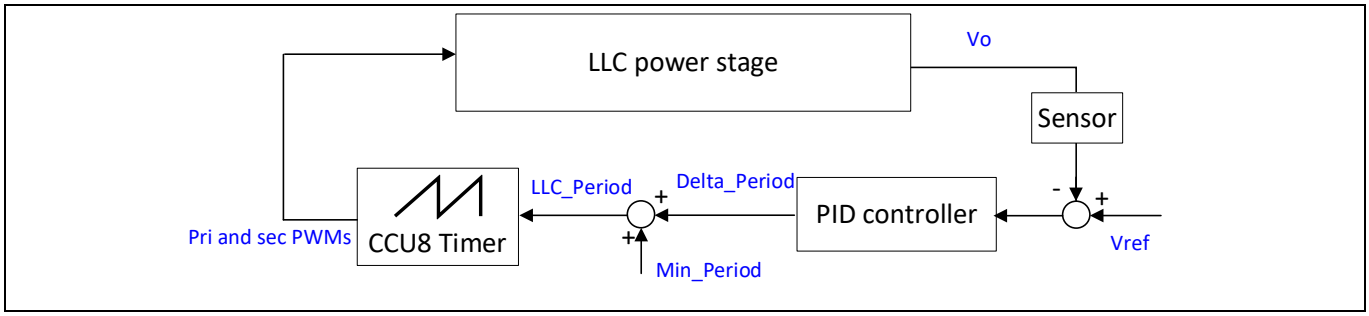


Figure 7 Control-block diagram

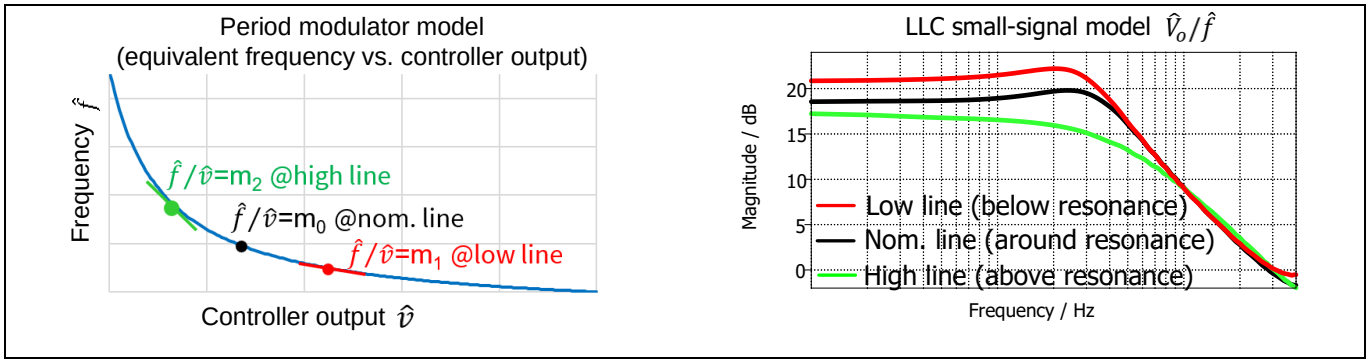


Figure 8 Small signal models of period modulator and LLC power stage

Soft start is needed to establish the output voltage progressively to prevent high inrush current and high-voltage stress. Figure 9 shows the startup sequence. Firstly, only the bottom PWMs are enabled to pre-charge the bootstrap circuits of top-side drivers. When the pre-charge is done, both top and bottom PWMs are enabled, and frequency sweep is initiated to limit the high inrush current. The switching frequency gradually sweeps from an initial high value 500 kHz down to 360 kHz, which is the maximum frequency used for close-loop control. Then, close-loop control with a slow PI controller takes over. The reference voltage starts ramping from the measured Vout at this moment to the nominal Vref. Note that only primary PWMs are turned on and secondary SR PWMS are still off. When the measured Vout rises close to the nominal output voltage (like 97 percent), a soft start of SR PWM happens. SR on time gradually ramps from zero to the maximum value, which is half the resonance period when below resonance or half the switching period when above resonance (with some delays). After that, the slow PID controller during startup is transitioned to a fast PID controller to improve transient performance at normal operation.

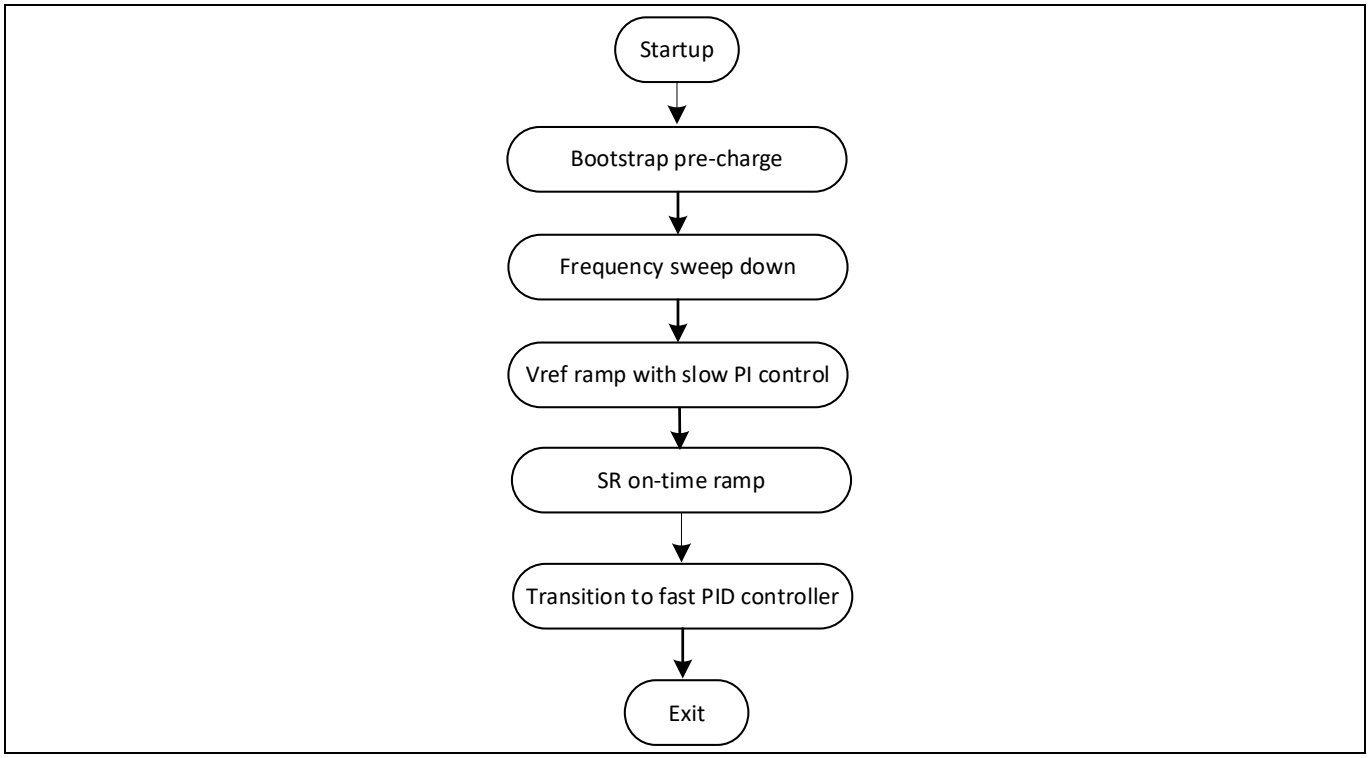


Figure 9 Start-up sequence

2 Board description

2.1 Specifications

Table 1 shows the specification of the EVAL_5K5W_3PH_LLC_SIC2 .

Table 1 Specifications

Parameter	Specification
Input voltage range	380 V_{DC} to 420 V_{DC} for normal operation, minimum 360 V_{DC} for short time operation to support hold up time requirement
Output voltage	50 V_{DC} nominal
Output power	5500 W
Output current	110 A
Resonant frequency	200 kHz
Switching frequency	130 kHz to 360 kHz for close loop operation, 500 kHz max for startup
Efficiency test	98.95 percent at Vin = 400 V half load (without fan loss)
	98.48 percent at Vin = 400 V full load (without fan loss)
Output voltage ripple	<150 mV p-p
Vin turn on threshold	370 V_{DC}
Input UVP	350 V_{DC}
Input OVP	430 V_{DC}
Output UVP	47 V_{DC}
Output OVP	54 V_{DC}
OCP	~130 A at nominal condition

2.2 Main board

The schematic of the main board is shown in Figure 10. The main board is mounted over a metallic frame and covered by a plastic enclosure to ensure proper airflow and cooling. The overall dimensions are 180 mm × 73.5 mm × 40 mm (excluding the output connector). The PCB is fabricated from a 4-layer board with 3 oz Copper thickness. Figure 11 shows the placement of different components. There are two sections of SR FETs connected in parallel. One section is on the bottom side of the main board and the other section is on the top side under the magnetics. The magnetics has a standoff height of 6 mm for proper airflow and clearance. Bus bars are added on the bottom to carry high output current. Copper plates are used as heatsink for SR FETs and transformer windings in the third phase, which are located farthest from the cooling fan.

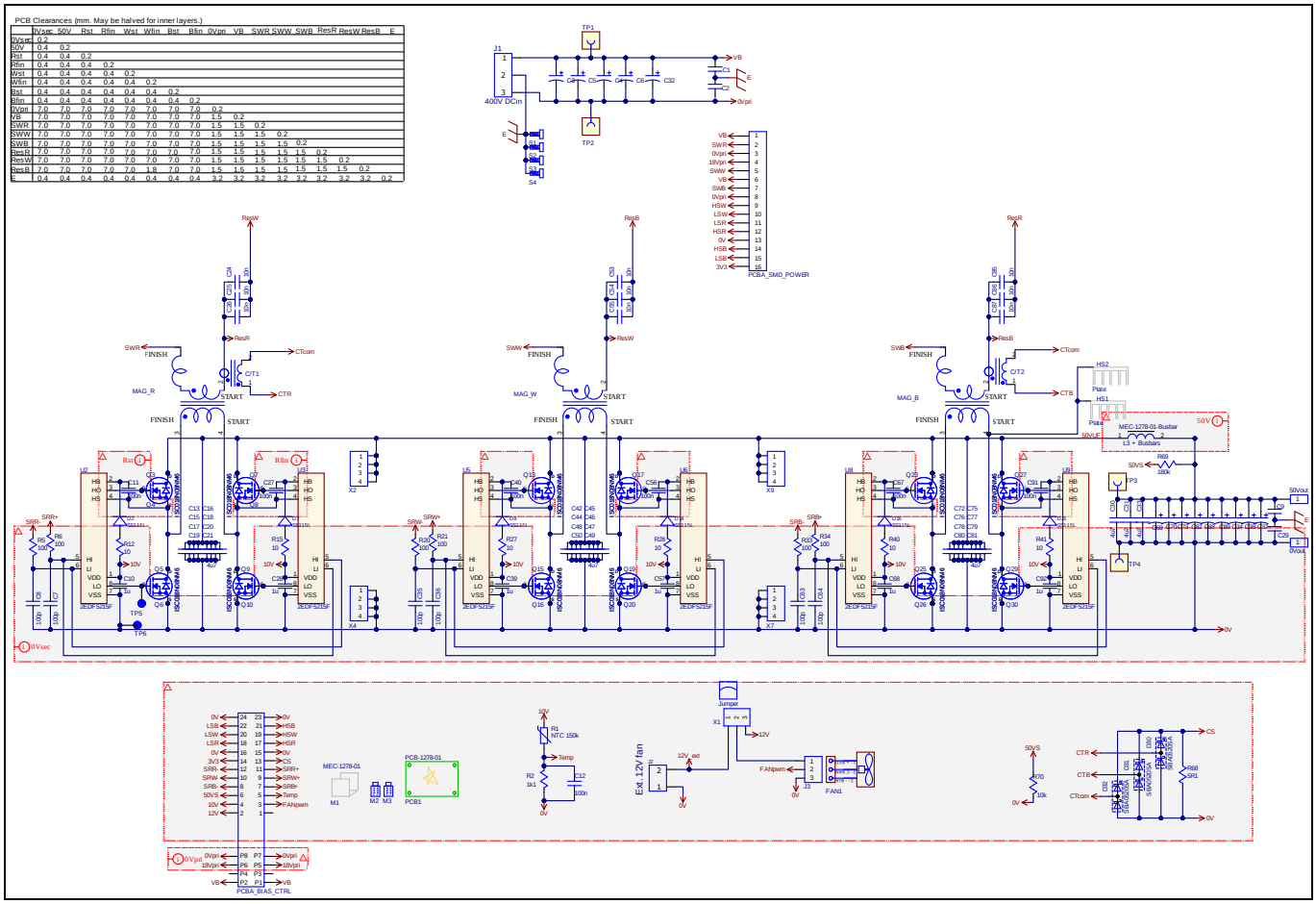
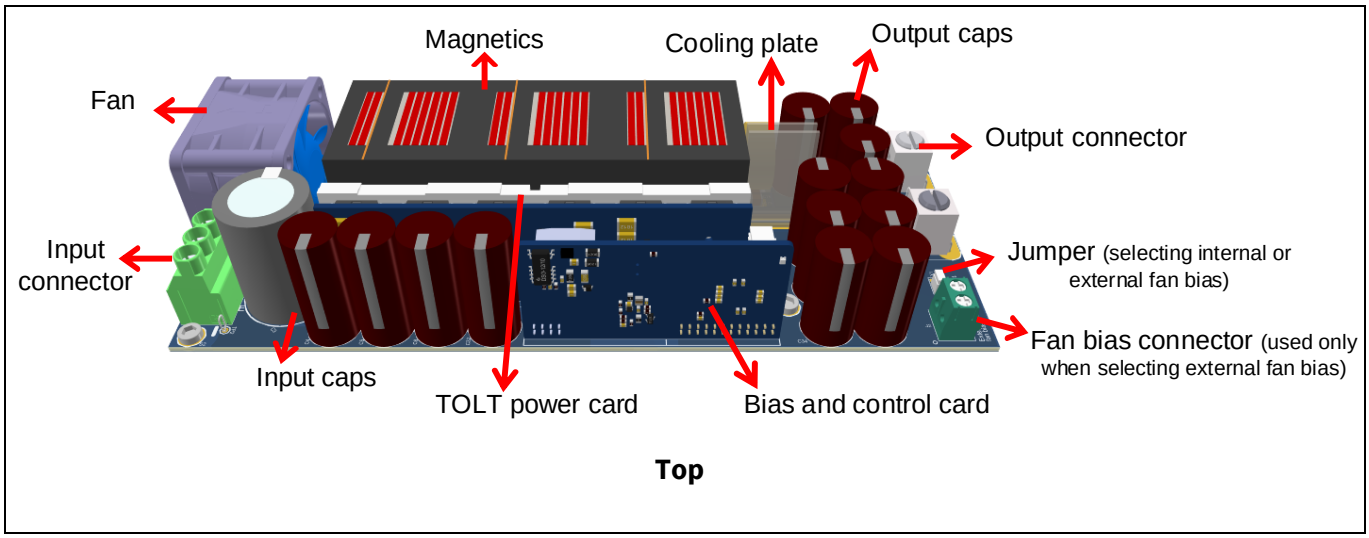


Figure 10 Schematics of main board



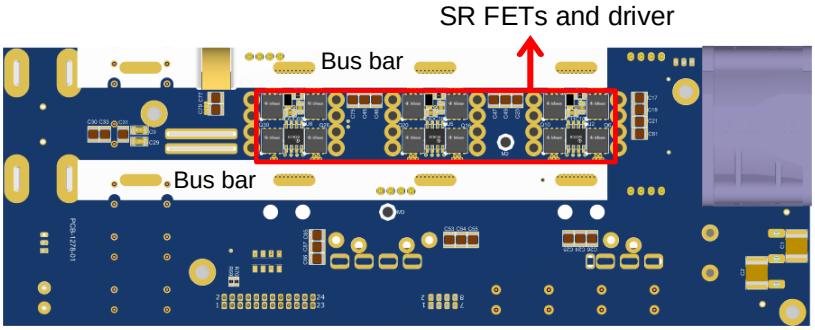


Figure 11 Placement of different sections on main board

2.3 TOLT power card

To achieve high power density, a tri-dimensional mechanical assembly is necessary, and multiple daughterboards are assembled on the main board. The three primary half bridges and the drivers are located in a daughtercard. The schematic is shown in Figure 12. Since top-side cooled packages are used, the components like bypass capacitor or gate drivers can be conveniently placed on either side of the PCB, which gives more assembly area. The heatsink is attached to the board using clips. Placement of the components on TOLT power card is shown in Figure 13.

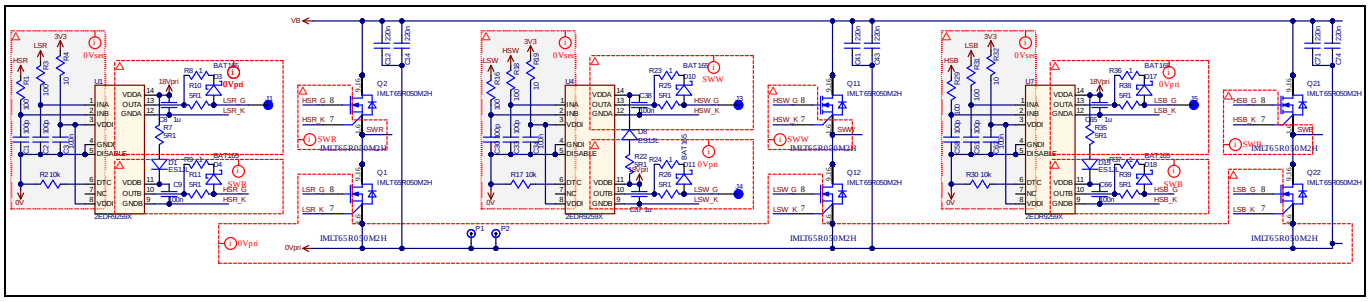


Figure 12 Schematics of TOLT power card

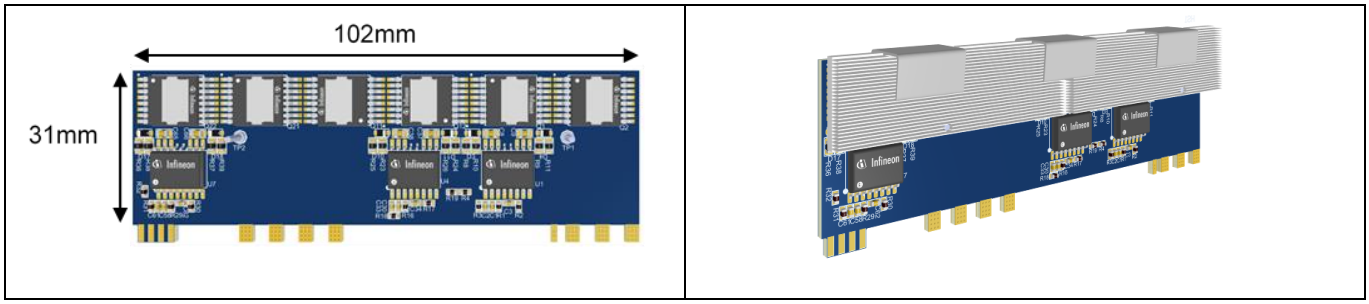


Figure 13 Placement of components on TOLT power card

2.4 Bias and control card

The flyback auxiliary power supply and XMC4400 digital control circuits are also located in a daughtercard. The schematics is shown in Figure 14. Placement of the components is shown in Figure 15. In each phase, one CCU8 timer slice is used to generate two complementary PWMs for the primary side (Pri_HS & Pri_LS). The rising and falling of ST1 triggers another CCU8 timer slice to generate secondary PWM SEC, as seen in Figure 16. Then the two SR PWMs are obtained by AND operation (SEC & Pri_HS, SEC & Pri_LS), which are implemented with

hardware logic gates. Three sets of the PWM signals are generated and phase shifted by 120 degrees for the three phases. The PWM pin map is shown in Figure 17.

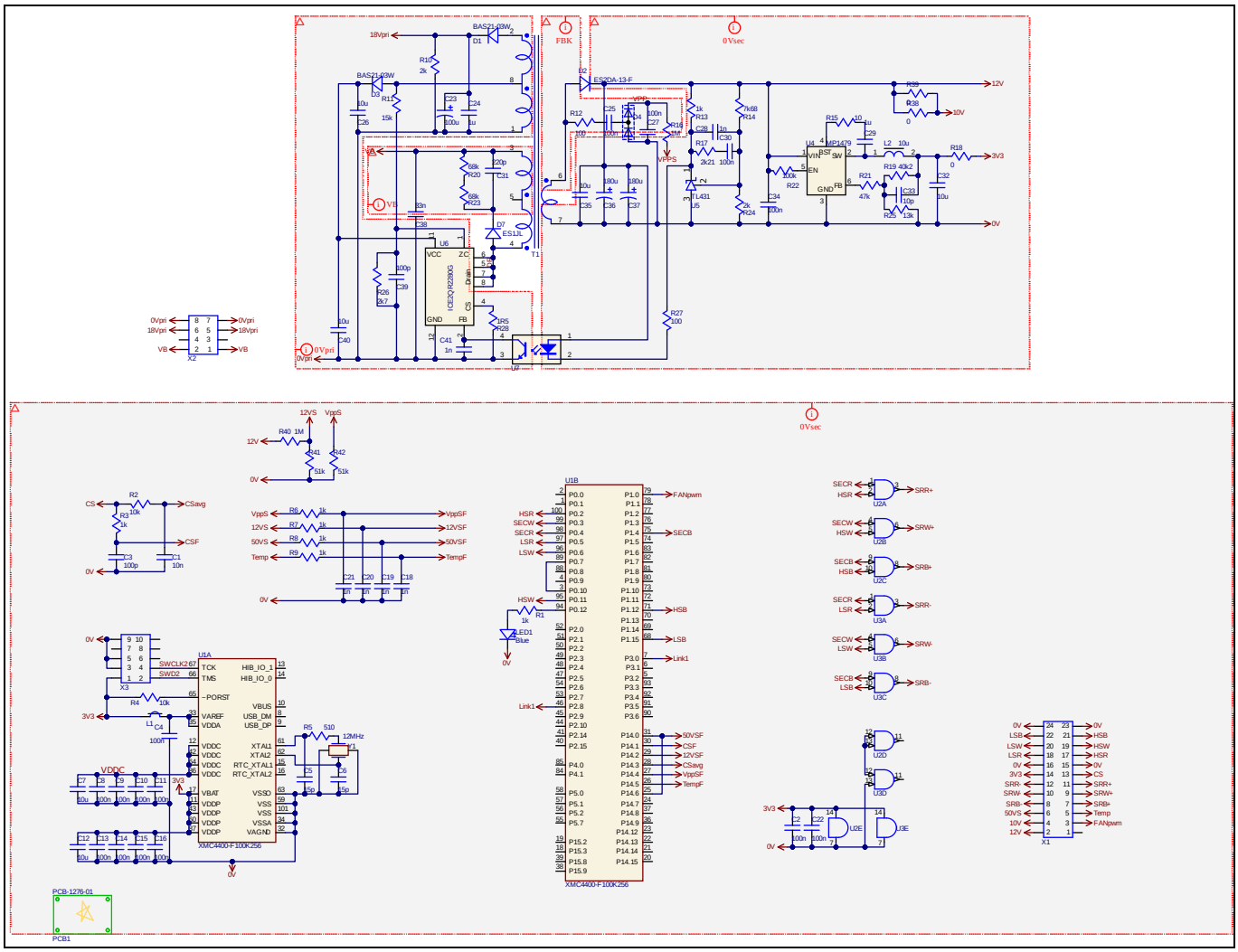


Figure 14 Schematics of bias and control card

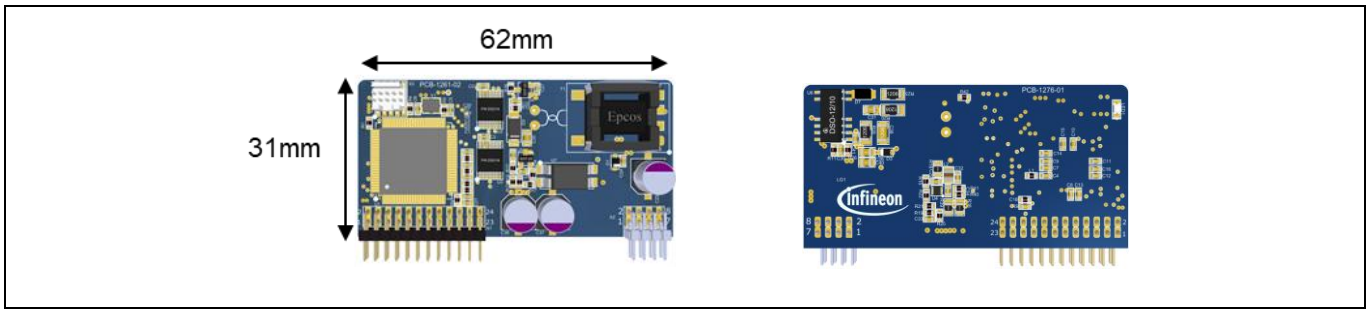


Figure 15 Placement of components on bias and control card

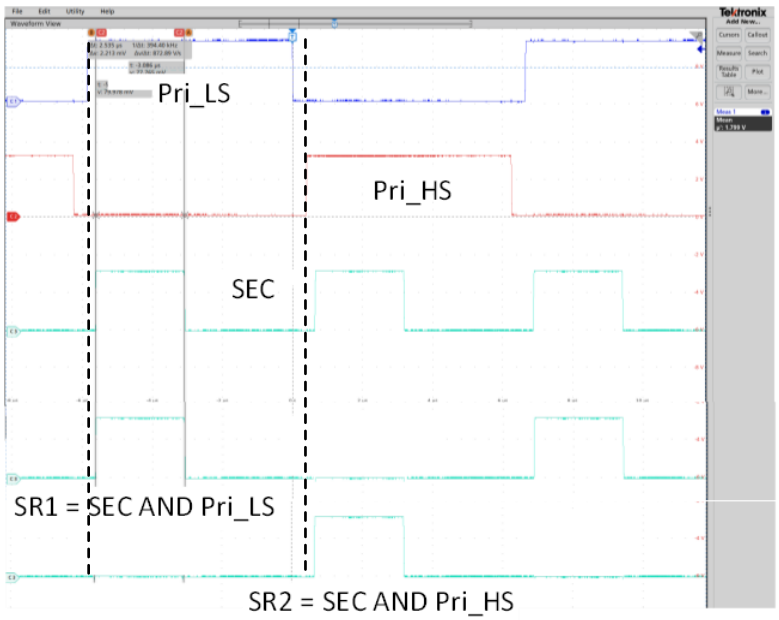


Figure 16 PWM generation in one phase

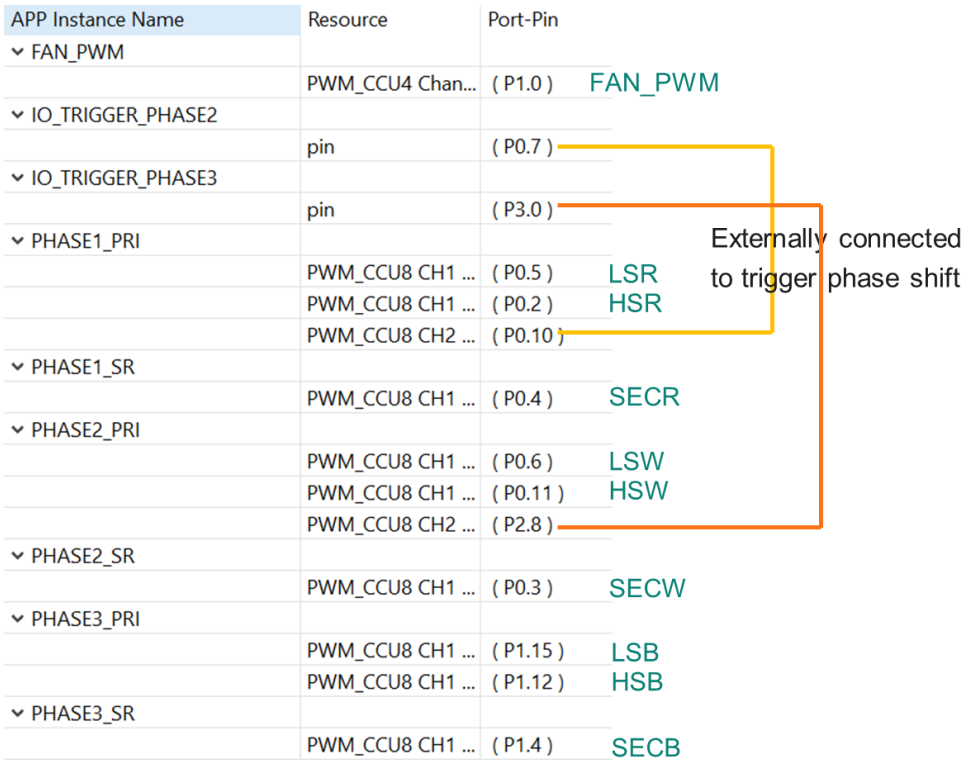


Figure 17 PWM pin map

2.5 Magnetics

The magnetics and Ansys simulation result are shown in Figure 18. There are three individual sections for the three phases, which are combined to save the space on PCB. Each section contains a resonant inductor and a 12:3 transformer with integrated magnetizing inductance. Each section is realized by half of a PQ35/20 core, a

plate and half of a PQ35/35 core with 3C95 material from YAGEO Ferroxcube. Triple-insulated Litz wire made of 405 strands x 0.05 mm diameter is used for the windings.

The primary windings have been interleaved with the secondary windings for minimum leakage inductance and proximity losses.

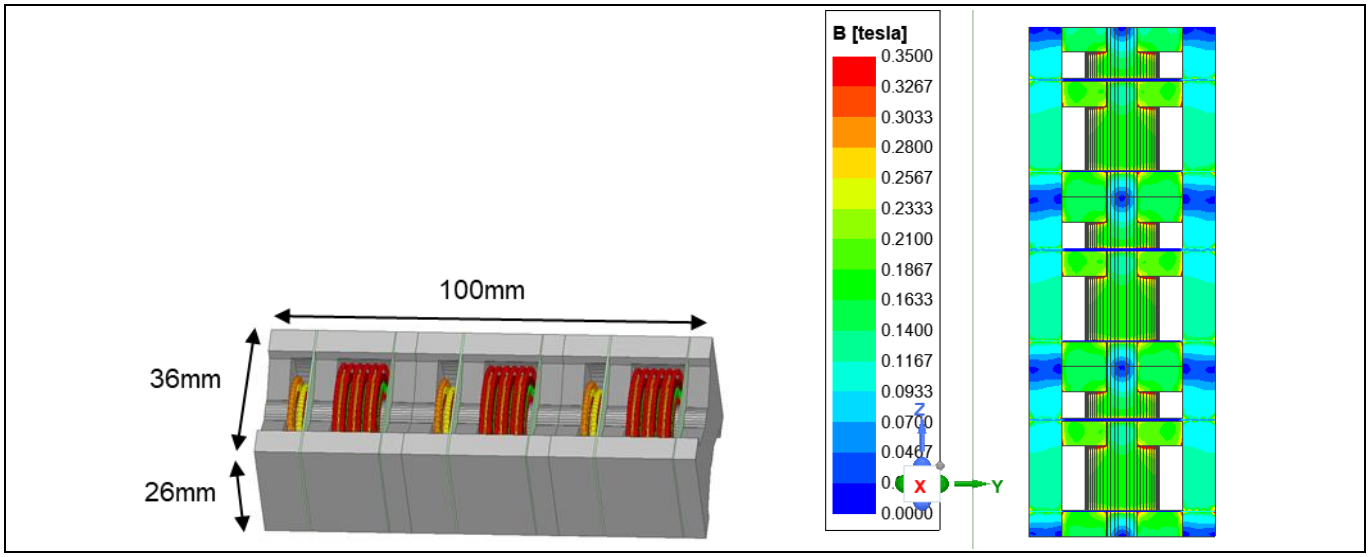


Figure 18 Three-phase magnetics and Ansys simulation

2.6 Test setup

For operation of the board, the necessary equipment includes:

- DC voltage supply capable of ~>420 V and at least 5500 W (when testing up to full load)
- Electronic load (0 to 60 V) with high current (greater than 110A), in constant current mode or constant resistance mode
- Low voltage power supply (12 V, greater than 1 A) to power the fan, used only when external fan bias is selected by the jumper
- Power analyzer for efficiency measurement

Figure 19 shows the test setup. For electrical safety and cooling reasons, it is recommended not to operate the board without enclosure or chassis.

The fan can be powered either from external power supply or from internal 12 V bias, to evaluate the board excluding or including fan power consumption. In both cases, the fan speed varies with the load, which is controlled by the microcontroller. The fan speed versus load is shown in Figure 20.

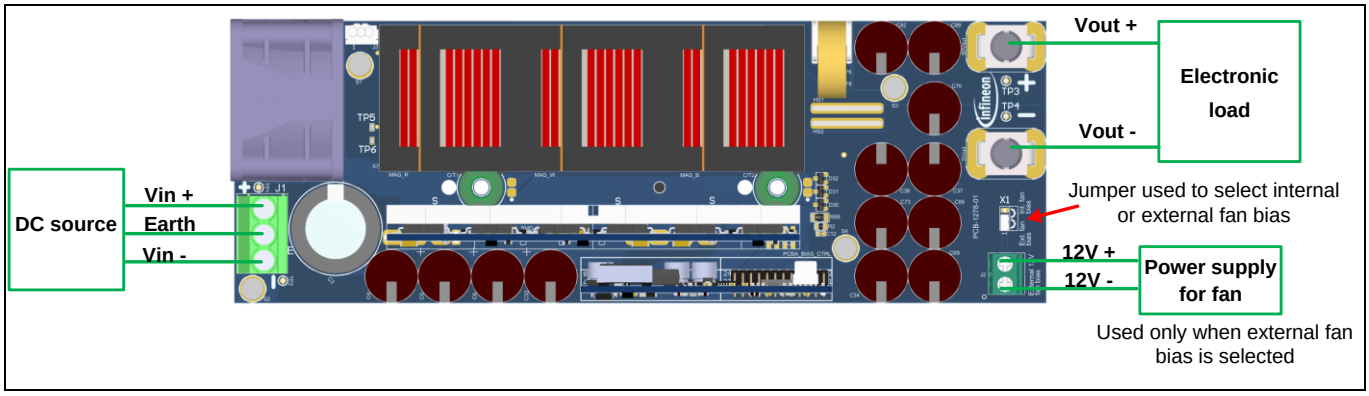


Figure 19 Test setup

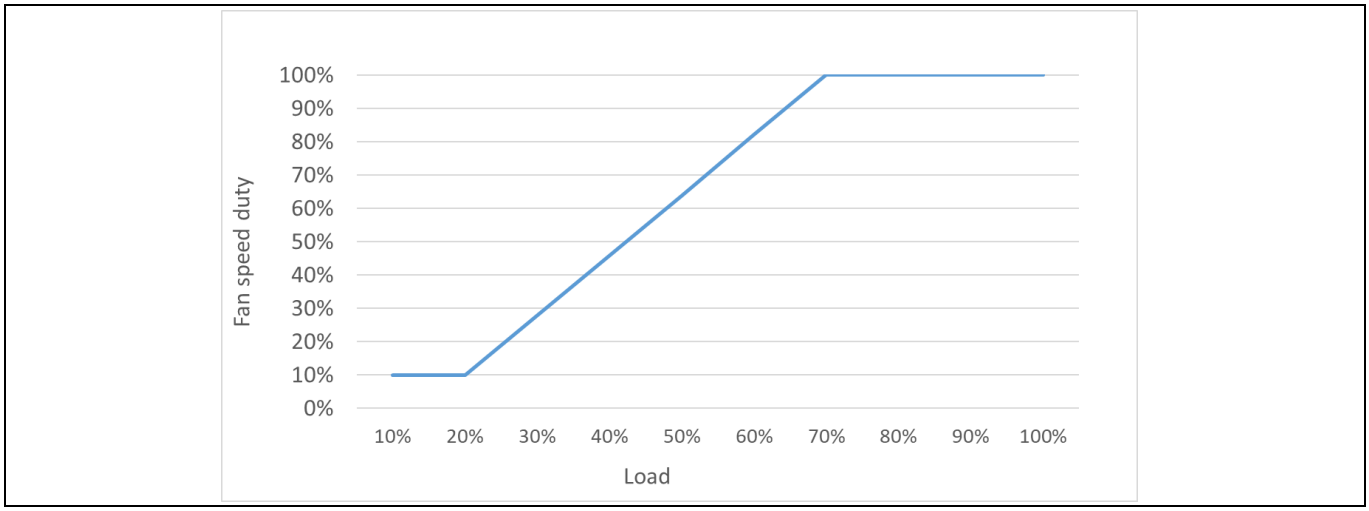


Figure 20 Fan speed versus load

3 Experimental results

3.1 Efficiency and losses

Figure 21 shows the measured efficiency over the line and load range. Here, an external 12 V power supply is connected to J2 to power the fan, so the fan loss is not included. Figure 22 shows the measured efficiency including fan loss, where the fan is powered from the internal 12 V bias supply. The efficiency measurements are obtained with a WT5000 power analyzer. The loss breakdown at Vin=400 V full load is shown in Figure 23. The loss calculations are given in Figure 24.

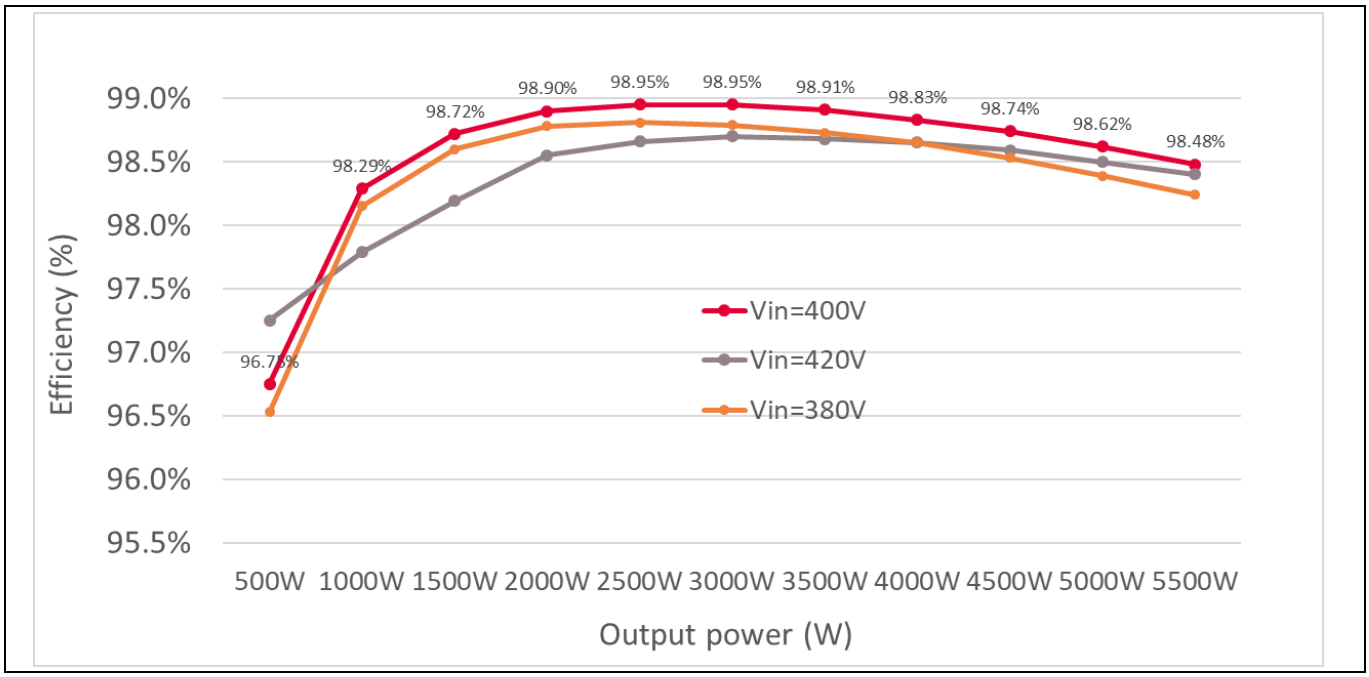


Figure 21 Measured efficiency without fan loss

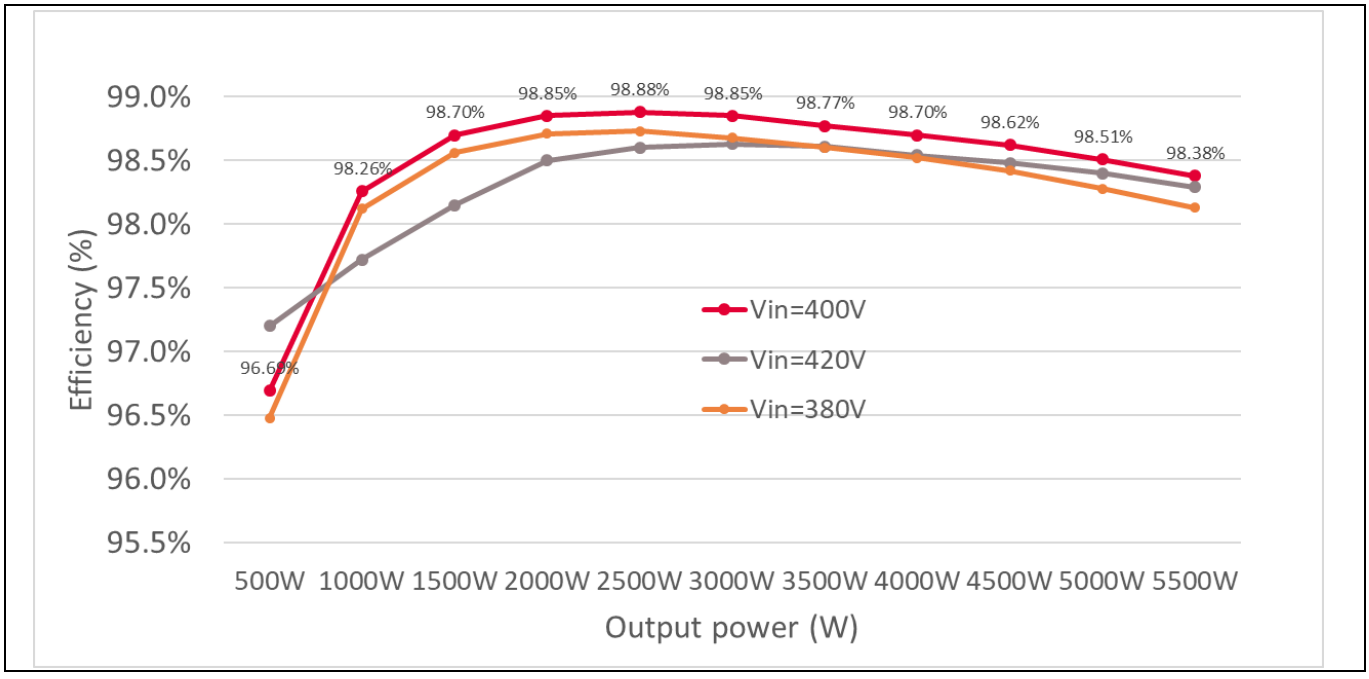


Figure 22 Measured efficiency including fan loss

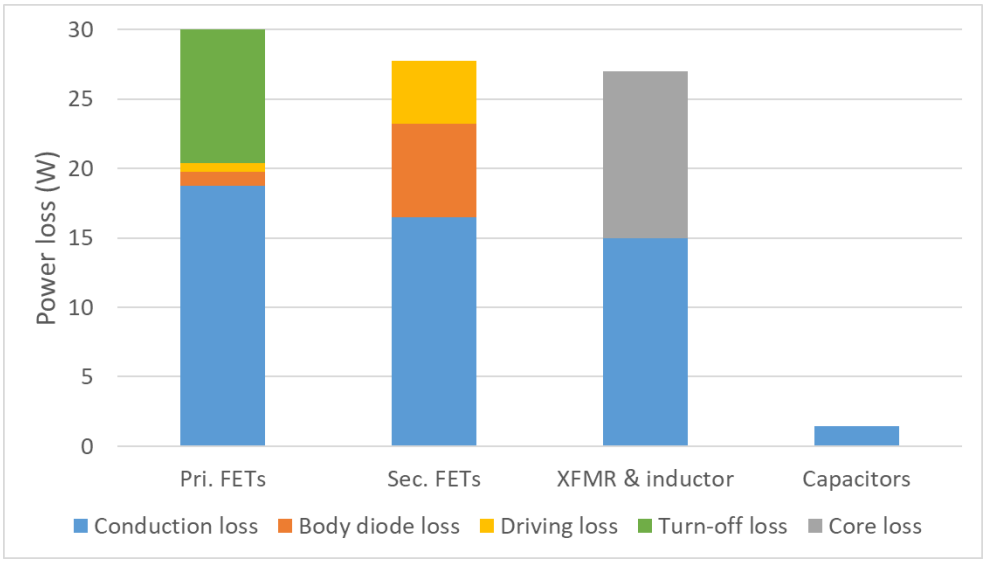


Figure 23 Loss breakdown at Vin = 400 V full load

Loss calculation of one phase

$Vin := 400\ V$ $Vo := 50\ V$ $P := \frac{5500\ W}{3} = (1.833 \cdot 10^3)\ W$ $fsw := 200\ kHz$

$IpriFET\_rms := 7.6\ A$ $IsecFET\_rms := 32\ A$

1. Loss of primary FETs

Conduction loss

$Rds\_pri := 50 \cdot 10^{-3} \cdot \Omega \cdot 1.08 = 0.054\ \Omega$ ← at Tj = 70C

$PpriFET\_cond := IpriFET\_rms^2 \cdot Rds\_pri \cdot 2 = 6.238\ W$

Body diode conduction loss

$Iturnoff := 4\ A$ $Vf := 4.3\ V$ $Tdeadtime := 50\ ns$

$Ppri\_bodydiode := Iturnoff \cdot Vf \cdot Tdeadtime \cdot fsw \cdot 2 = 0.344\ W$

Turn off loss

Eoff = $(9 \cdot 10^{-6})\ J$ from datasheet

$Ppri\_turnoff := (9 \cdot 10^{-6})\ J \cdot fsw \cdot 2 = 3.6\ W$

Driving loss

$Qg\_pri := 22 \cdot 10^{-9} \cdot C$ ← $Vdrv\_pri := 18 \cdot V$ ←

$Ppri\_driving := Qg\_pri \cdot Vdrv\_pri \cdot fsw \cdot 2 = 0.158\ W$

Total primary FET loss

$Ppri\ FET := PpriFET\ cond + Ppri\ bodydiode + Ppri\ turnoff + Ppri\ driving = 10.34\ W$

2. Loss of secondary FETs

Conduction loss

$Rds\_sec := 1.8 \cdot 10^{-3} \cdot \Omega \cdot 1.5 = 0.003\ \Omega$ ←

$PsecFET\_cond := IsecFET\_rms^2 \cdot \frac{Rds\_sec}{2} \cdot 4 = 5.53\ W$

Body diode conduction loss

$Ion\_SR := \frac{8}{2} A = 4\ A$ $Ioff\_SR := \frac{24}{2} A = 12\ A$

from simulation and experimental waveforms

$Vf\_sec := 1\ V$ $Td\_on := 100\ ns$ $Td\_off := 200\ ns$

$Psec\_bodydiode := (Ion\_SR \cdot Vf\_sec \cdot Td\_on + Ioff\_SR \cdot Vf\_sec \cdot Td\_off) \cdot fsw \cdot 4 = 2.24\ W$

Driving loss

$Qg\_sec := 76 \cdot 10^{-9} \cdot C$ ← $Vdrv\_sec := 12 \cdot V$ ←

$Psec\_driving := Qg\_sec \cdot Vdrv\_sec \cdot fsw \cdot 8 = 1.459\ W$

Total secondary FET loss

$Psec\_FET := PsecFET\_cond + Psec\_bodydiode + Psec\_driving = 9.229\ W$

3. Loss of magnetics

The magnetic losses come from ANSYS simulation

Core loss = 4.1W
winding loss = 5W per phase

4. Loss of capacitors

Resonant capacitor

$ICr\_rms := 6\ A$ $ESR\_Cr := \frac{10 \cdot 10^{-3} \cdot \Omega}{3} = 0.003\ \Omega$

$PCr := ICr\_rms^2 \cdot ESR\_Cr \cdot 2 = 0.24\ W$

Output capacitor

$ICo\_rms := 10\ A$ $ESR\_Co := \frac{20 \cdot 10^{-3} \cdot \Omega}{9} = 0.002\ \Omega$

$PCo := ICo\_rms^2 \cdot ESR\_Co = 0.222\ W$

Figure 24 Loss calculations

3.2 Thermal

Figure 25 shows the thermal performance of the main components at full load, operating within the enclosure at 25°C ambient temperature. The enclosure provides proper cooling as it conveys the airflow through the high-temperature components. The data are taken with thermocouples. The temperatures are well below the maximum limits of the components.

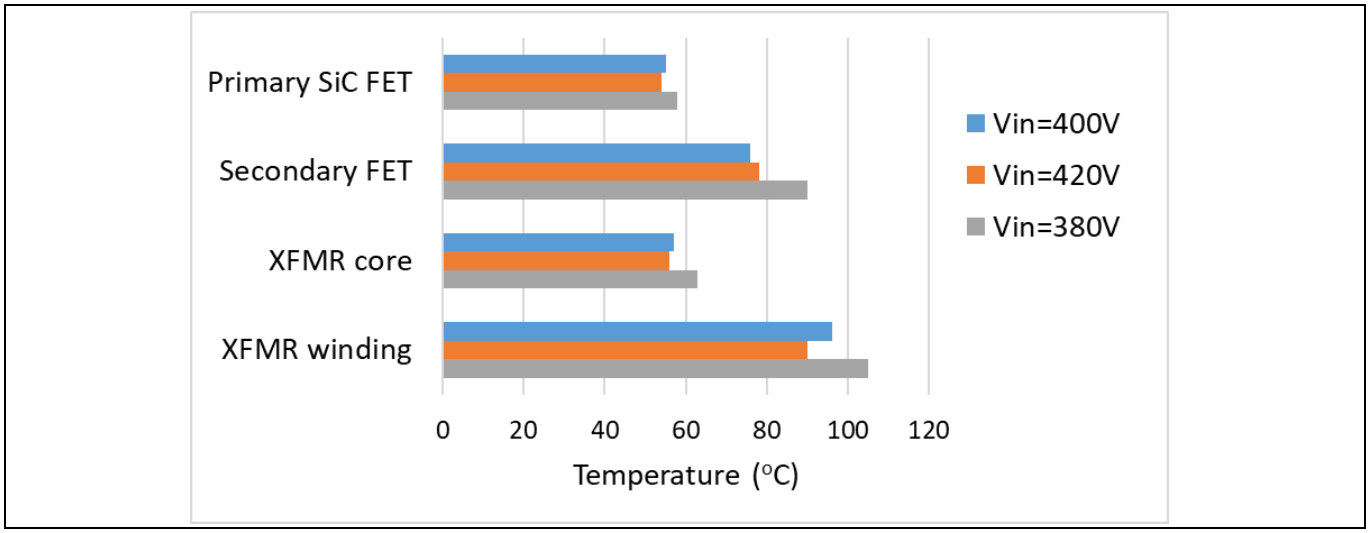


Figure 25 Thermal measurements within the enclosure

3.3 Steady state waveforms

Figure 26 to Figure 28 show the steady state waveforms across the line range. ZVS is achieved in the primary FETs. A relatively large SR turn off delay (~200 ns) is used to accommodate the tolerance of resonant components.

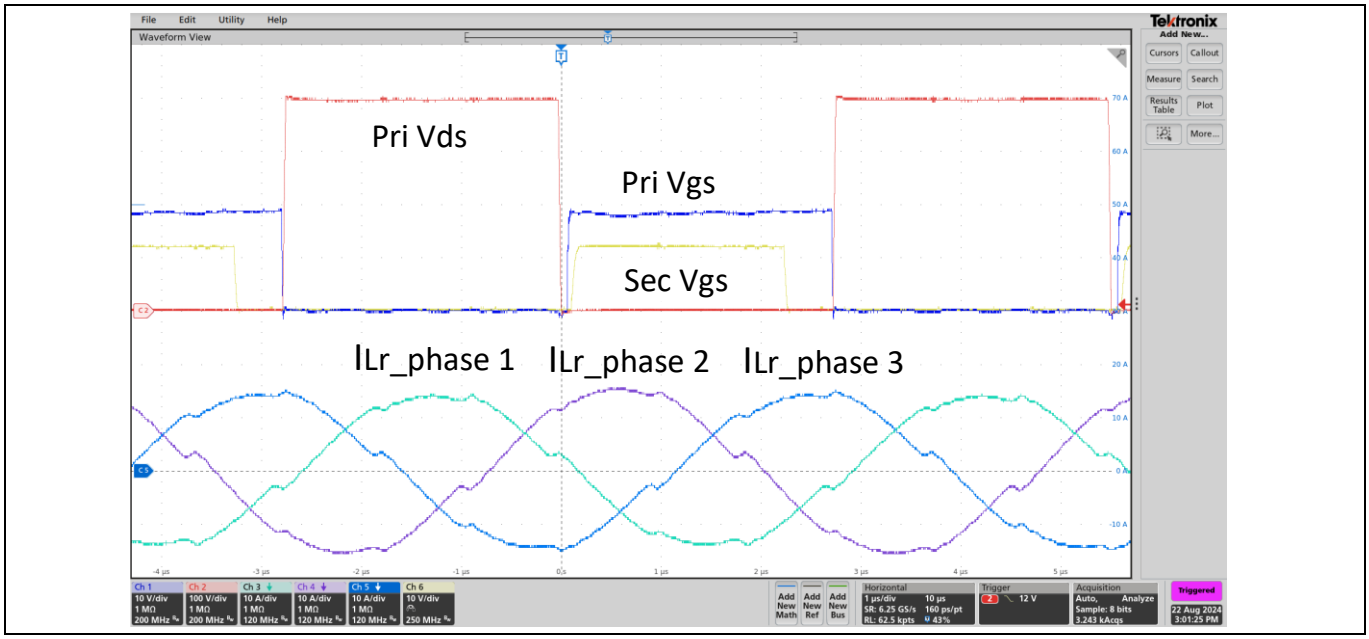


Figure 26 Waveform at Vin = 400 V full load

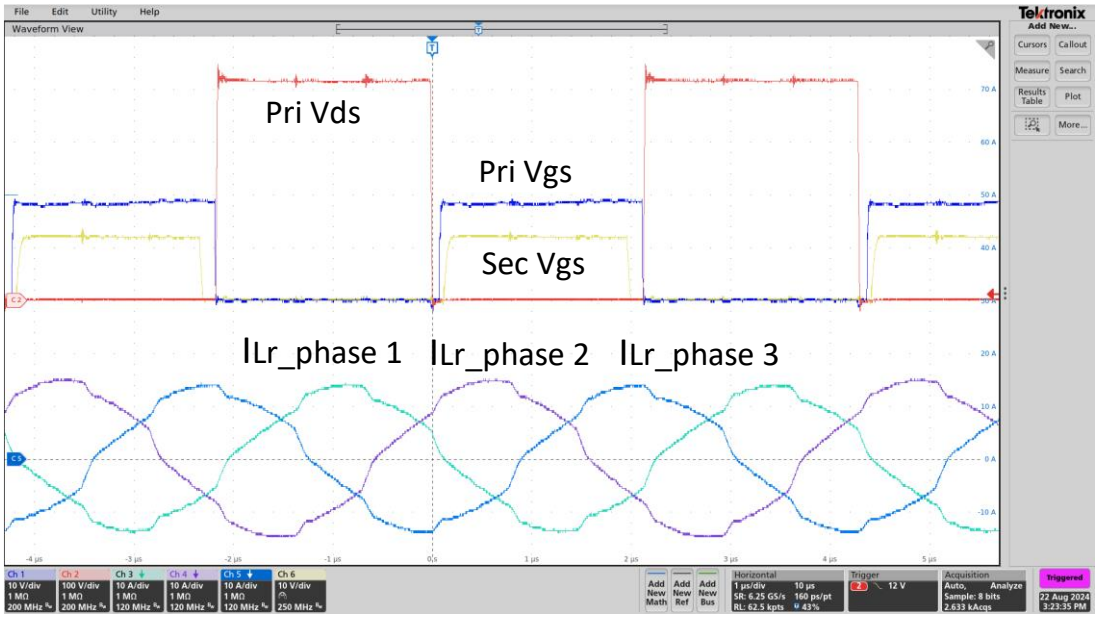


Figure 27 Waveform at Vin = 420 V full load

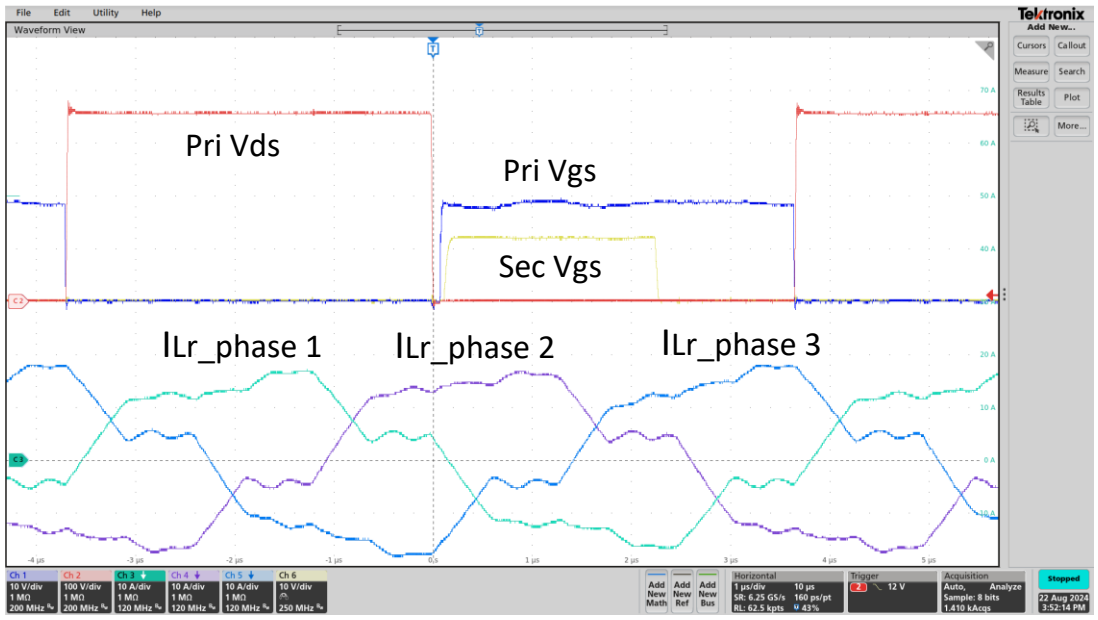


Figure 28 Waveform at Vin = 360 V full load for holdup time requirement

3.4 Startup waveforms

Figure 29 to Figure 32 show the startup waveforms at different line voltages and load. It can be seen that the inrush current is small and the drain-source voltage overshoot of the primary FETs is well under the maximum voltage limits. At no load, the converter enters burst mode after startup.

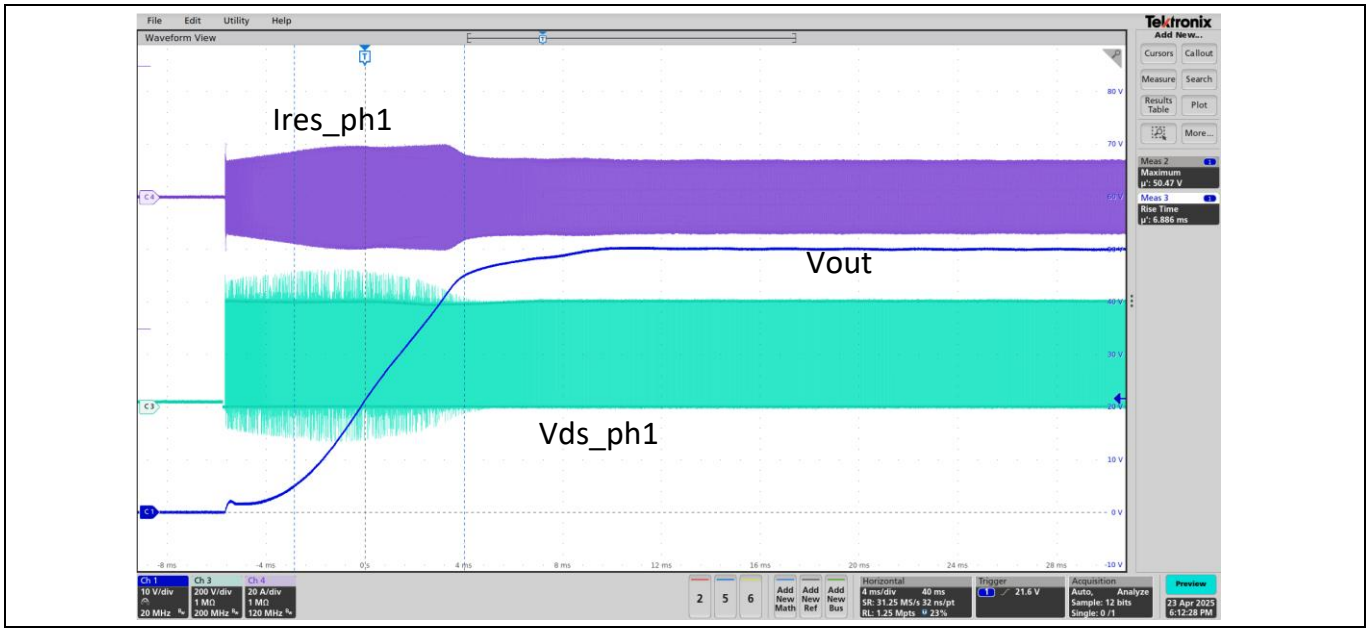


Figure 29 Startup waveform at Vin = 400 V full load

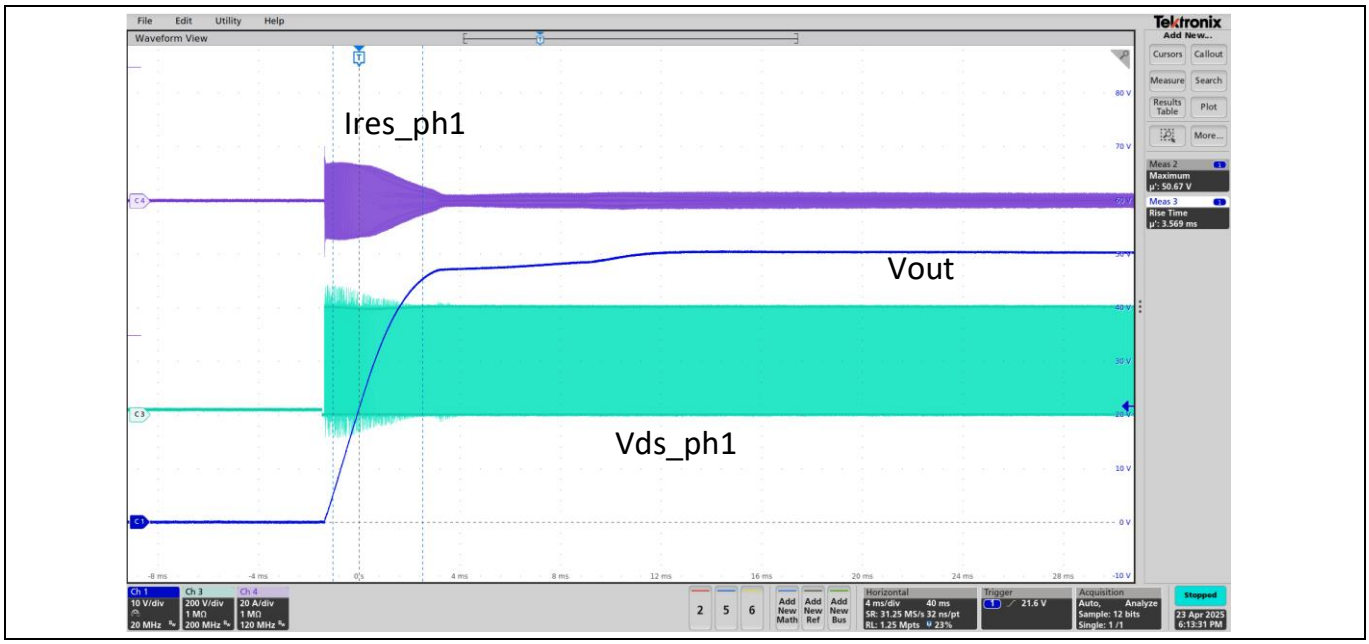


Figure 30 Startup waveform at Vin = 400 V, 10-percent load

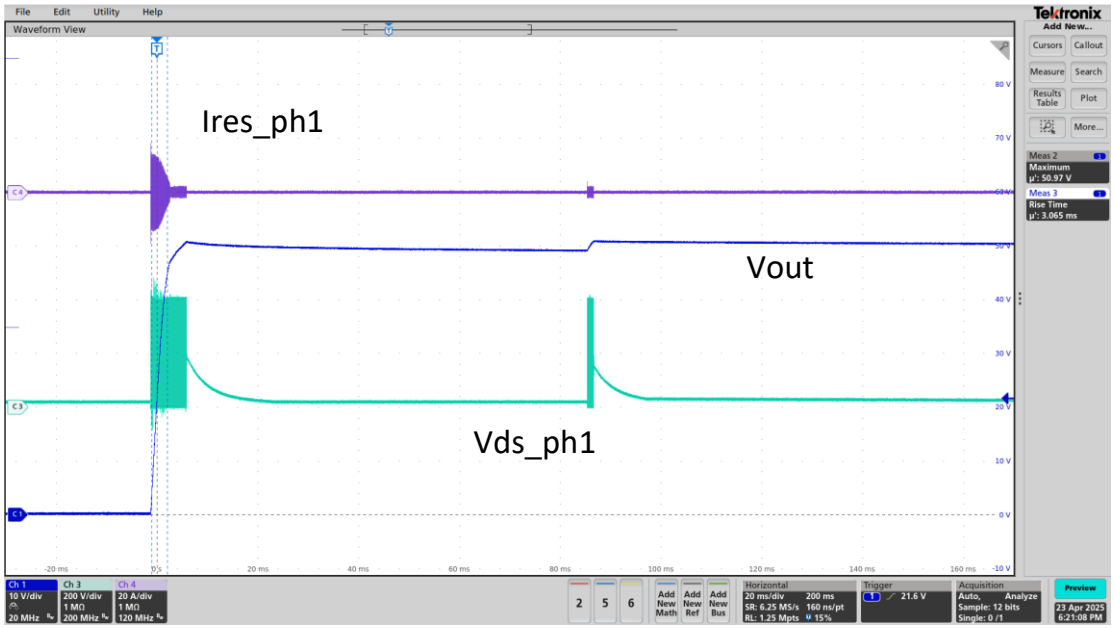


Figure 30 Startup waveform at Vin = 400 V, no load

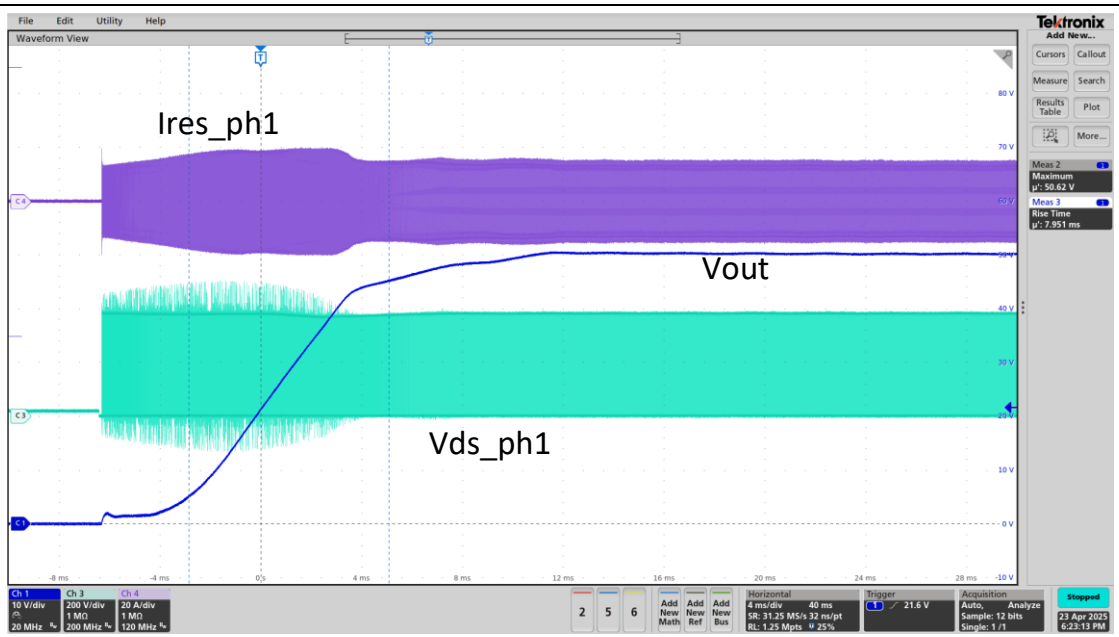


Figure 31 Startup waveform at Vin = 380 V, full load

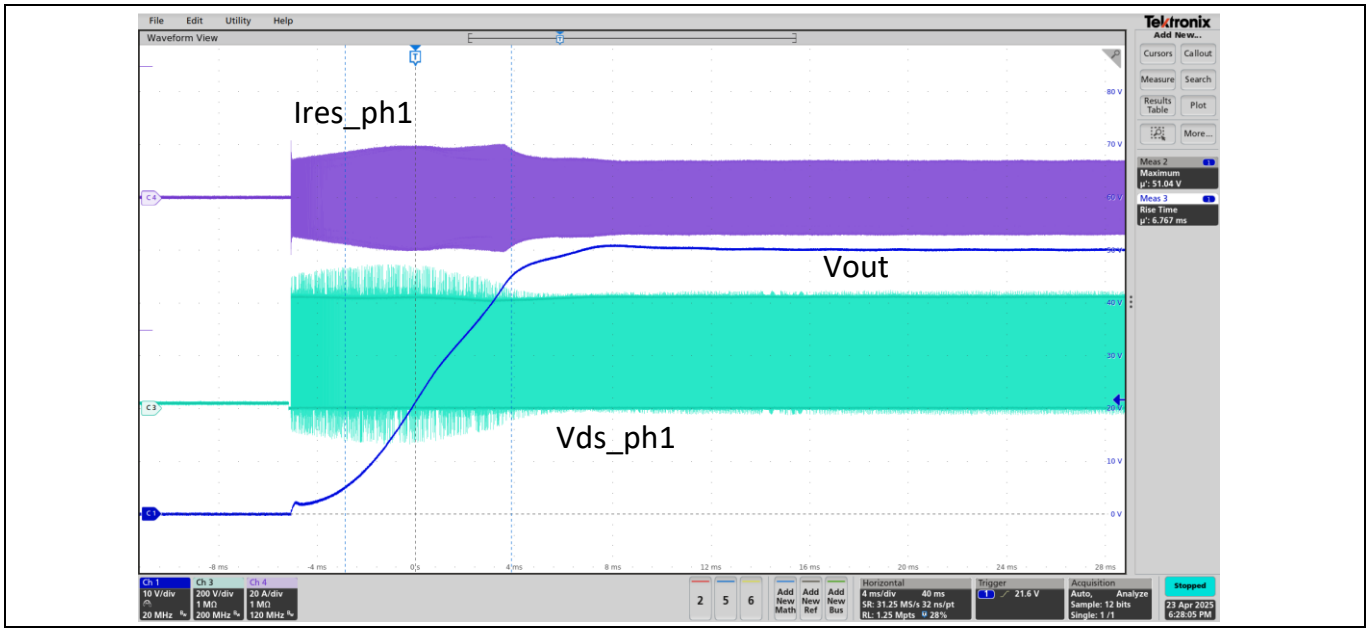


Figure 32 Startup waveform at Vin = 420 V, full load

3.5 Burst mode operation

The converter enters burst mode at no load or high-line light load for output regulation and efficiency improvement. The frequency is limited to a maximum frequency (360 kHz) during burst. Figure 33 gives the burst mode waveform at Vin=420 V and 10-percent load.

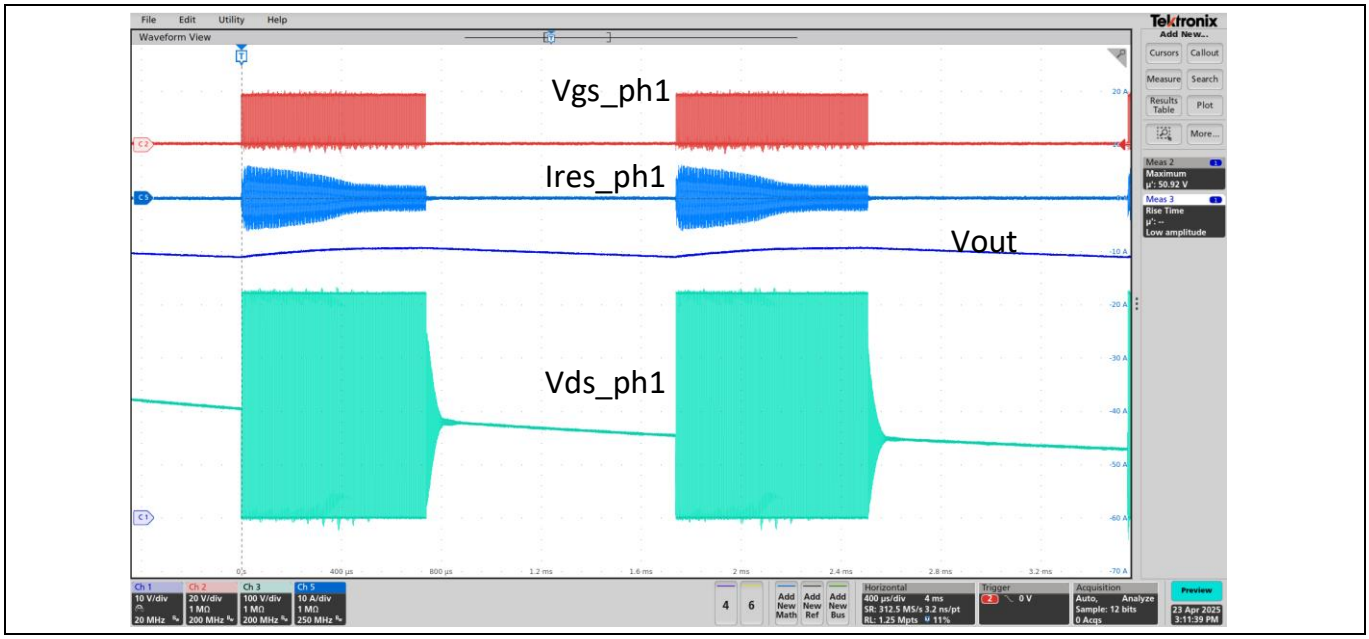


Figure 33 Burst mode waveform at Vin = 420 V and 10 percent load

3.6 Output voltage ripple

Figure 34 shows the output voltage ripple waveform. The typical voltage ripple is 90 mV at Vin = 400 V at full load.

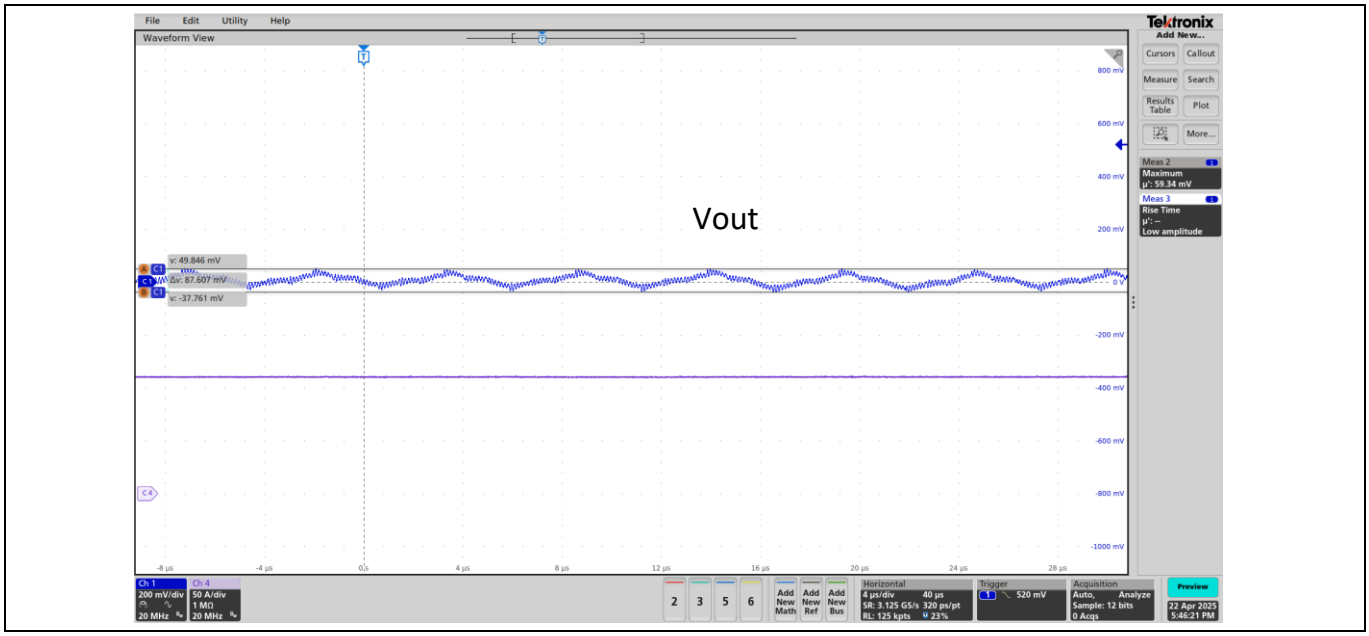


Figure 34 Output voltage ripple at Vin = 400 V full load

3.7 Load transient

Figure 35 to Figure 36 show the load transient waveforms. The controller is well within the stability criteria requirement. The overshoot and undershoot is within 3 percent of the nominal output voltage for 50 percent of load jump. In LLC converter, the small signal model depends strongly on the load and line voltage. An adaptive controller can be implemented to further improve the transient performance.

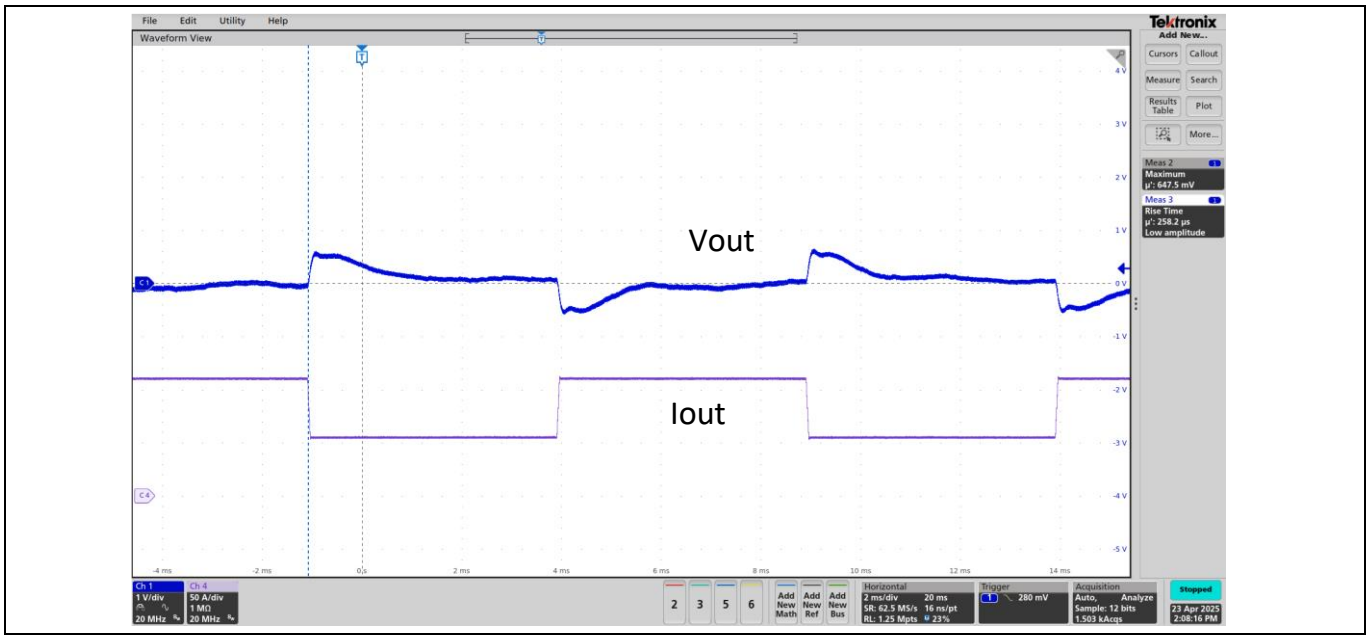


Figure 35 Transient at Vin = 400 V from half load to full load

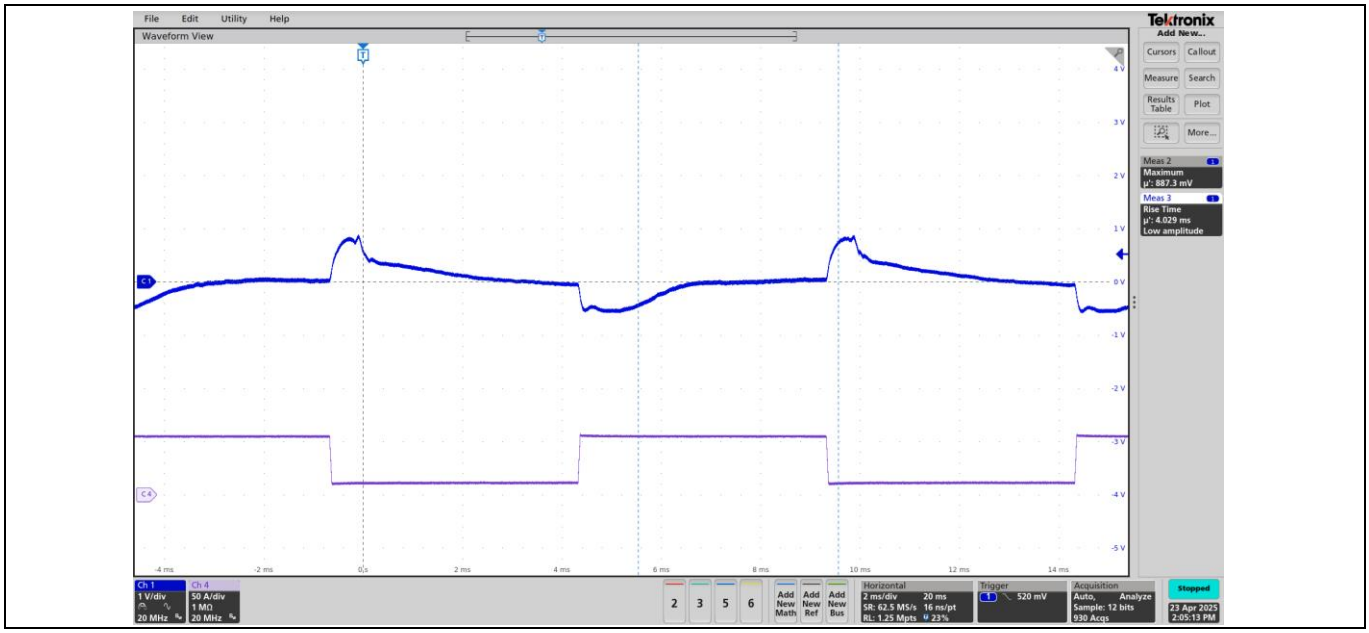


Figure 36 Transient at Vin = 400 V from 10 percent load to half load

4 Summary

This document described a 5.5 kW three-phase interleaved LLC converter designed for server and data center applications. It converts 380 V to 420 V DC input voltage to a regulated 50 V output, achieving a peak efficiency of almost 99 percent and a power density of 170 W/in^3.

The board utilizes 650 V CoolSiC™ MOSFETs, which features very low Qoss and Qg as well as small Rdson dependence over temperature, allowing to increase both efficiency and power density. By using top-side cooled packages, heat transfer can be decoupled from the PCB, allowing to optimize both electrical path and thermal path. 80 V OptiMOS™ 6 MOSFETs are used as synchronous rectifiers, leading to very low conduction losses and driving losses.

References

[1] C. Fei, R. Gadelrab, Q. Li and F. C. Lee, "High-Frequency Three-Phase Interleaved LLC Resonant Converter With GaN Devices and Integrated Planar Magnetics," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 7, no. 2, pp. 653-663, June 2019.

[2] Infineon Technologies AG: CoolSiC™ 650 V G2 MOSFET application note; Available online

[3] S. Kampl and S. Mollov, "Optimization of thermal performance of top-side cooled discrete power semiconductors," PCIM Europe 2022; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany, 2022, pp. 1-6, doi: 10.30420/565822126

[4] Infineon Technologies AG: Optimizing PCB layout for HV CoolGaN™ power transistors application note; Available online

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