100 W power supply using CoolSET™ SiP ICE180LM

EVAL_100W1_ZVS_180LM

About this document

This engineering report describes the EVAL_100W1_ZVS_180LM Evaluation Board for a flyback converter with an isolated 12 V, 8.33 A output using the latest Infineon CoolSET™ ICE180LM System in Package (SiP) zero-voltage switching (ZVS) flyback integrated solution with CoolSiC™ MOSFET. This 100 W evaluation board serves the purpose of understanding the technical features and capabilities of the CoolSET™ ICE180LM. For detailed features and power delivery capability, see the device datasheet [1].

Highlights of this power supply:

- Overall high efficiency to meet energy efficiency requirement
- Simplified circuitry with high-level integration of power control and protection features
- Auto-restart protection scheme to minimize interruption and enhance the user experience
- Zero-voltage switching (ZVS) technology to boost efficiency
- CoolSiC™ MOSFET to enable higher output power

Intended audience

This document is intended for power supply design, application engineers, or others who want to design efficient and reliable auxiliary power supplies.

CoolSET™

Infineon's CoolSET™ AC-DC integrated power stages in fixed frequency and quasi-resonant switching schemes offer increased robustness and outstanding performance. This family offers superior energy efficiency, comprehensive protective features, and reduced system costs and is ideally suited for auxiliary power supply applications in a wide variety of potential applications such as:

- SMPS
- Home appliances
- Server power supply units (PSU)
- Telecom

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1 Introduction

This engineering report describes the EVAL_100W1_ZVS_180LM Evaluation Board designed in a zero-voltage switching (ZVS) quasi-resonant (QR) flyback converter using CoolSET™ ICE180LM System in Package (SiP) from Infineon's first fully integrated controller. The evaluation board provides 100 W output at 12 V and 8.33 A, with an input range of 90 VAC to 264 VAC. The evaluation board can achieve 93.7% peak efficiency.

The CoolSET™ ICE180LM is ideally targeted for auxiliary power supplies for SMPS, home appliances, servers, and telecom applications. The SiP integration includes an 800 V CoolSiC™ MOSFET, primary and a secondary controller, and isolated communication. An advanced PWM switching pattern forces a zero-voltage switching (ZVS) quasi-resonant (QR) operation, reducing the turn-on switching losses and optimizing the EMI signature. A comprehensive set of protection features supports ease of design-in.

Table 1 lists the general system requirements for a power supply and the corresponding Infineon solution using ICE180LM.

Table 1 General system requirement and proposed design solution

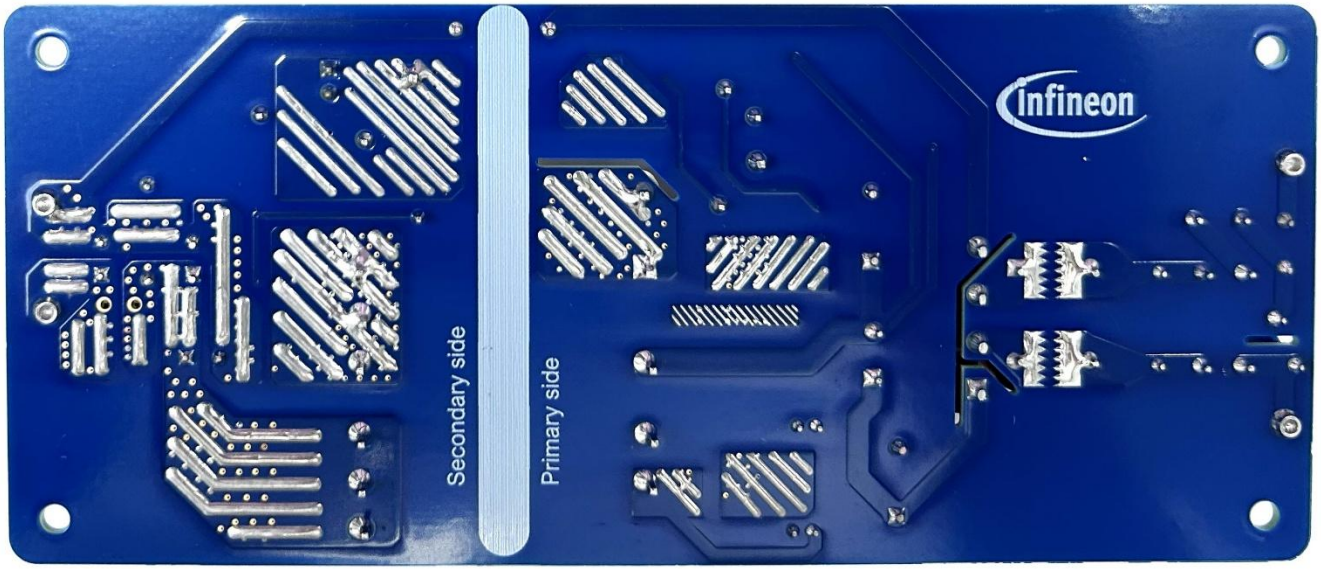
	General system requirements	Proposed design solution – ICE180LM
1	High efficiency to meet energy efficiency requirements	Primary zero-voltage switching and secondary optimal synchronous rectifier (SR) control
2	Simplified circuitry with high-level integration	Primary 800 V CoolSiC™ MOSFET, primary and secondary controller, and communication integrated in a DSO-27 package
3	Minimize interruption to enhance user experience	All protections are defined to enter auto-restart mode

2 EVAL_100W1_ZVS_180LM Evaluation Board

This document contains the list of features, power supply specifications, schematics, bill of materials (BOM), and performance data. Typical operating characteristics, such as performance curve and scope waveforms are shown at the later sections of this document.



Top view



Bottom view

Figure 1 EVAL_100W1_ZVS_180LM Evaluation Board

3 Specifications of evaluation board

Table 2 Specifications of EVAL_100W1_ZVS_180LM

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions/notes
Input						
Voltage	V_{IN}	90	–	264	VAC	2-wire (no P.E.)
Frequency	f_{LINE}	47	50/60	64	Hz	–
Output						
Voltage	V_{OUT}	12			V	–
Current	I_{OUT}	8.33			A	–
Output power	P_{OUT}	100			W	–
Ripple	V_{pk-pk}	150			mV	–
Overcurrent protection	I_{OCP}	10			A	–
Environmental						
Conducted EMI	–	6			dB	EN55022, Class B
Surge immunity – Differential mode (DM)	–	±2			kV	EN 61000-4-2
Surge immunity – Common mode (CM)	–	±4			kV	
ESD – Contact discharge	–	±8			kV	EN 61000-4-5
ESD – Air discharge	–	±15			kV	
Ambient temperature	T_{amb}	–20	–	50	°C	Free convection, sea level
Size	–	140 × 60 × 38.5			mm	L × W × H

Note: The table above represents the minimum acceptable performance of the design. Actual measurement results are listed in the Test results section.

4 Schematic

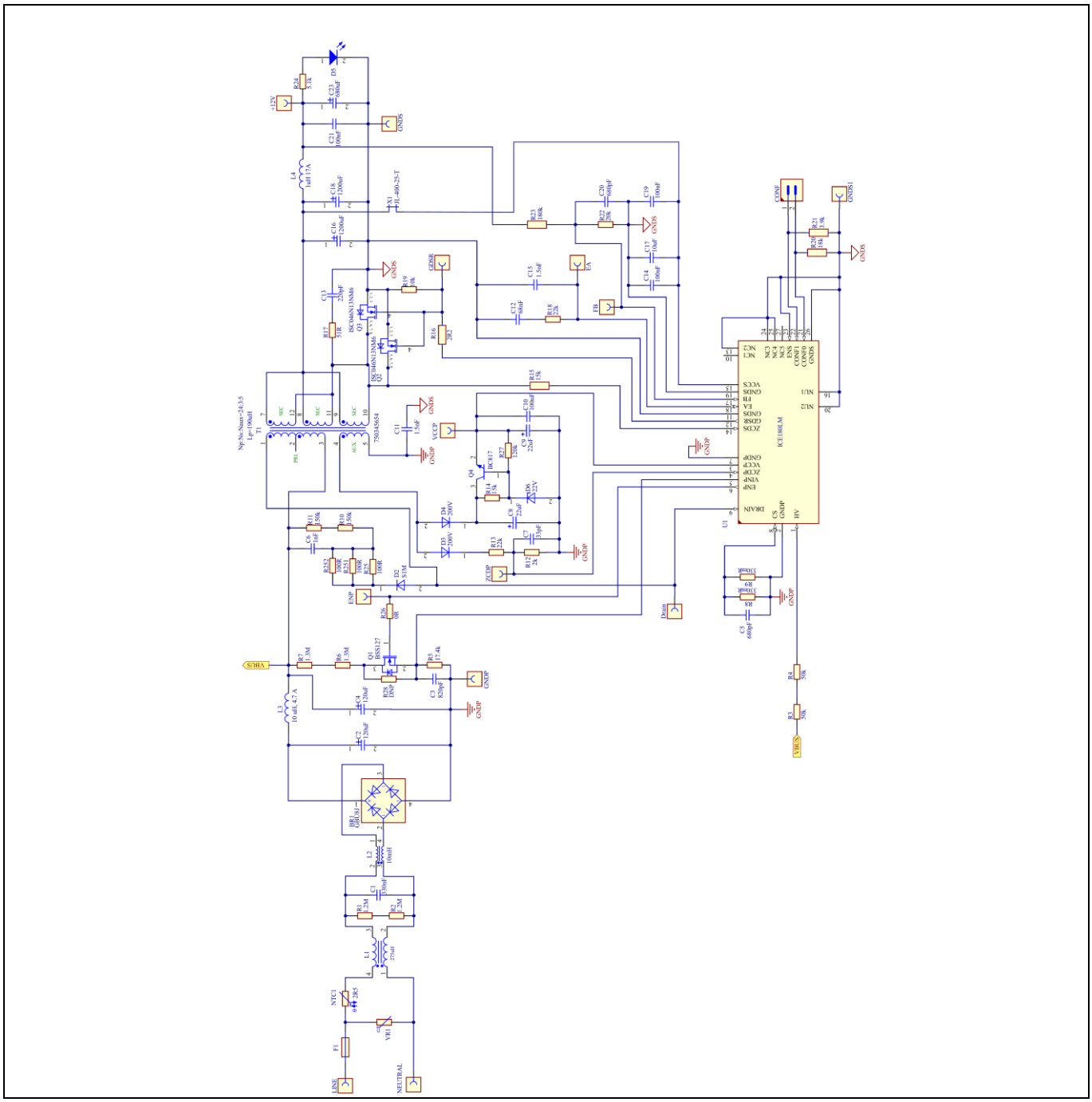


Figure 2 Schematic of EVAL_100W1_ZVS_180LM

5 Circuit description

This section briefly describes the proposed design circuit by different functional blocks. For details of the design procedure and component selection for the flyback circuitry, see the IC datasheet [1] and design guide [2].

5.1 EMI filtering and line rectification

The input of the power supply is taken from the AC power grid, which is in the 90 V AC ~ 264 VAC range. The fuse (F1) is at the input to protect the system in case of excess current entering the system circuit due to a fault. Following is the varistor (VR1), which is connected across L and N to absorb the line surge transient.

Common mode choke L1, L2, and the X-capacitor C1 form a basic filter to reduce the EMI noise. The bridge rectifier (BR1) rectifies the AC input into DC voltage, filtered by the π filter (C2, C4, and L3). R1 and R2 resistors discharge C1 when the power supply is disconnected from the AC mains. NTC1 is used to suppress the inrush current when the AC is connected to the board.

5.2 CoolSET™ SiP power stage

The flyback converter power stage consists of a power transformer, primary power MOSFET, secondary synchronous rectifier (SR) MOSFET, secondary output capacitors, and so on.

Primary and secondary sides power management are separated for isolated power supply domains (VCCP, GNDP, and VCCS, GNDS). ICE180LM provides reinforced isolation and safe communication between primary and secondary sides.

5.2.1 CoolSET™ SiP primary side

The CoolSET™ ICE180LM SiP integrates a 950 V startup cell at the primary side. The IC self-starts through the startup resistors (R3 and R4) in series with this startup cell to charge the VCCP pin capacitors (C9, C10) when DC supply is applied. These startup resistors, together with ZCDP pin external configuration resistor R_{ZCDPL} (R12), determine the brown-in and brown-out protection, as shown in Table 3.

Table 3 Primary-side configuration options

Option	$R_{ZCDPL(min)}$; $R_{ZCDPL(max)}$	Brown-in current threshold I_{HV_BI}	Brown-out current threshold I_{HV_BO}	Internal shunt resistor $R_{HVshunt}$
1	[1.00 kΩ; 1.05 kΩ]	2.00 mA	1.40 mA	0.5 kΩ
2	[1.87 kΩ; 2.70 kΩ]	1.00 mA	0.70 mA	1.0 kΩ
3	[4.30 kΩ; 5.00 kΩ]	0.67 mA	0.47 mA	1.5 kΩ
4	[9.20 kΩ; 9.50 kΩ]	0.50 mA	0.35 mA	2.0 kΩ

Option 2 is selected with R_{ZCDPL} (R12) = 2 kΩ, the brown-in voltage can be estimated as:

$$V_{BI} = (R_{HV} + R_{HVshunt}) \times I_{HV_BI} = (100\ \text{k}\Omega + 1\ \text{k}\Omega) \times 1\ mA = 101\ V$$

Equation 1

And the brown-out voltage can be estimated as:

$$V_{BO} = (R_{HV} + R_{HVshunt}) \times I_{HV_BO} = (100\ \text{k}\Omega + 1\ \text{k}\Omega) \times 0.7\ mA = 70.7\ V$$

Equation 2

Moreover, R12 and R13 resistors offer zero-crossing detection during the soft-start period and primary-sensed output overvoltage protection.

$$V_{OUT_OVP} = \left(\frac{(R_{ZCDPH} + R_{ZCDPL}) \times V_{ZCDP_OVP_min}}{R_{ZCDPL}} + V_{Daux}\right) \times \frac{N_{SEC}}{N_{AUX}} - V_{Dsec}$$
$$= \left(\frac{(22\ k\Omega + 2\ k\Omega) \times 2.05\ V}{2\ k\Omega} + 0.3\ V\right) \times \frac{3}{5} - 0.1\ V \approx 14.84\ V$$

Equation 3

Where,

N_{SEC}: Number of secondary turns

N_{AUX}: Number of auxiliary turns

V_{Daux}: Diode forward voltage drop at auxiliary winding

V_{Dsec}: Voltage drop across SR MOSFET

$V_{ZCDP_OVP_min}$: Minimum voltage of the output overvoltage threshold

V_{OUT_OVP}: User-defined output overvoltage level

C7 is chosen to adjust the delay time, which starts when the drain-source voltage falls below the bus voltage until the ZCDP voltage falls to $V_{ZCDPthr}$ (100 mV, Typ.). Therefore, the power switch can be turned on at the valley point of the drain-source voltage.

A total 44 µF capacitor for C8, C9 is selected to ensure stable system operation and enough break time for auto-restart protection. The VCCP linear regulator (R14, R27, D6, and Q4) is placed to avoid the VCCP voltage exceeding the pin voltage rating (32 V) in case of severe voltage spike coupling from the transformer during the surge test.

DC line overvoltage protection is detected by sensing the bus capacitor voltage through the VINP pin via the divider resistor R5. Once the VINP pin voltage is higher than the line overvoltage threshold V_{VINP_LOVP}, the controller enters the line overvoltage protection and releases the protection mode when the VINP pin voltage falls below V_{VINP_LOVP}.

Typical LOVP voltage is calculated as follows:

$$V_{BUS_OVP} = V_{VINP_LOVP} \times \frac{R6+R7+R5}{R5} = 2.80\ V \times \frac{1.3\text{M}\Omega+1.3\text{M}\Omega+17.4\ \text{k}\Omega}{17.4k\Omega} = 421\ V$$

Equation 4

The primary overcurrent protection is sensed by the R8 and R9 resistor through the CS pin. The V_{CSOCP1} is 0.76 V and V_{CSOCP2} is 1.1 V. The R8 and R9 are selected to ensure the system will not enter the overcurrent protection before the targeted OCP level is hit.

A low-cost RCD clamp consisting of the D2 diode, R25, R251, R252 resistor, and the C6 capacitor is implemented to suppress the peak drain voltage when turning off the power switch inside ICE180LM. This passive snubber helps dissipate the energy stored in the transformer leakage inductance.

5.2.2 CoolSET™ SiP secondary side

The secondary side of CoolSET™ ICE180LM SiP starts to take over the PWM control when the output voltage reaches 95% of its regulation target. The ICE180LM PWM control is based on sensing the reflected voltage from the primary side via the ZCDS pin and the error amplifier (EA) output voltage. ICE180LM integrated PWM and SR control ensures that the timing of the SR power switch (Q2 and Q3) and the primary-side power switch is well synchronized, which avoids the cross conduction of the two switches and provides reliable synchronous rectification. In addition, the current injection function via the SR power switch (Q2 and Q3) enables zero-voltage switching operation on the primary side.

R20 is connected to CONF0 and serves as R_{SET0}. The value of R20 is determined by the transformer turns ratio, which is a critical parameter in the design. According to Table 4, the transformer turns ratio is specified as 8. Based on this value, R20 is set as 18 kΩ.

Table 4 Resistance for R_{SET0}

Turns ratio N_{MAIN}/N_{SEC}	R_{SET0}
5	3.9 kΩ
6	6.8 kΩ
7	12.0 kΩ
8	18.0 kΩ
9	27.0 kΩ
10	39.0 kΩ

R21 is connected to CONF1 and acts as R_{SET1}, defining the parameters for Hysteretic-mode operation. Choose options between 1 to 3 to fine-tune amount of loading for which the system stays in Hysteretic mode. For this board, 3.9 kΩ (option 1 in Table 5) is chosen to keep the smallest power range operating in Hysteretic mode. For details, see the design guide [2].

Table 5 Resistance for R_{SET1}

Symbol / Parameter	Option	1	2	3	4	5	6
	R_{SET1}	3.9 kΩ	6.8 kΩ	12.0 kΩ	18.0 kΩ	27.0 kΩ	39.0 kΩ
EA voltage for wakeup in Hysteretic mode	V_{EA_HMOn}	1.25 V	1.20 V	1.10 V	1.25 V	1.20 V	1.10 V
EA voltage for off-phase in Hysteretic mode	V_{EA_HMOff}	0.95 V	0.9 V	0.8 V	0.95 V	0.9 V	0.8 V
EA voltage Hysteretic mode exit threshold	V_{EA_LHM}	1.4 V	1.4 V	1.4 V	1.6 V	1.6 V	1.6 V

The output voltage feedback is through the sense resistors R22 and R23 to the FB pin. The FB reference voltage is 1.2 V. A compensation network consisting of C12, C15, and R18 is implemented to stabilize the output voltage regulation. This network is carefully designed to ensure that the power supply's output voltage remains stable and within the desired range. For a detailed understanding of the compensation network's calculation, see the design guide [2].

To minimize output voltage ripple, the choice of output capacitors is crucial. The output capacitors C16, C18 are recommended to have low equivalent series resistance (ESR) type capacitor. A low pass filter L4 and C23 are added to further filter the output ripple. And a ceramic capacitor C21 is added to suppress the high frequency noise.

6 PCB layout

6.1 Top-side layout

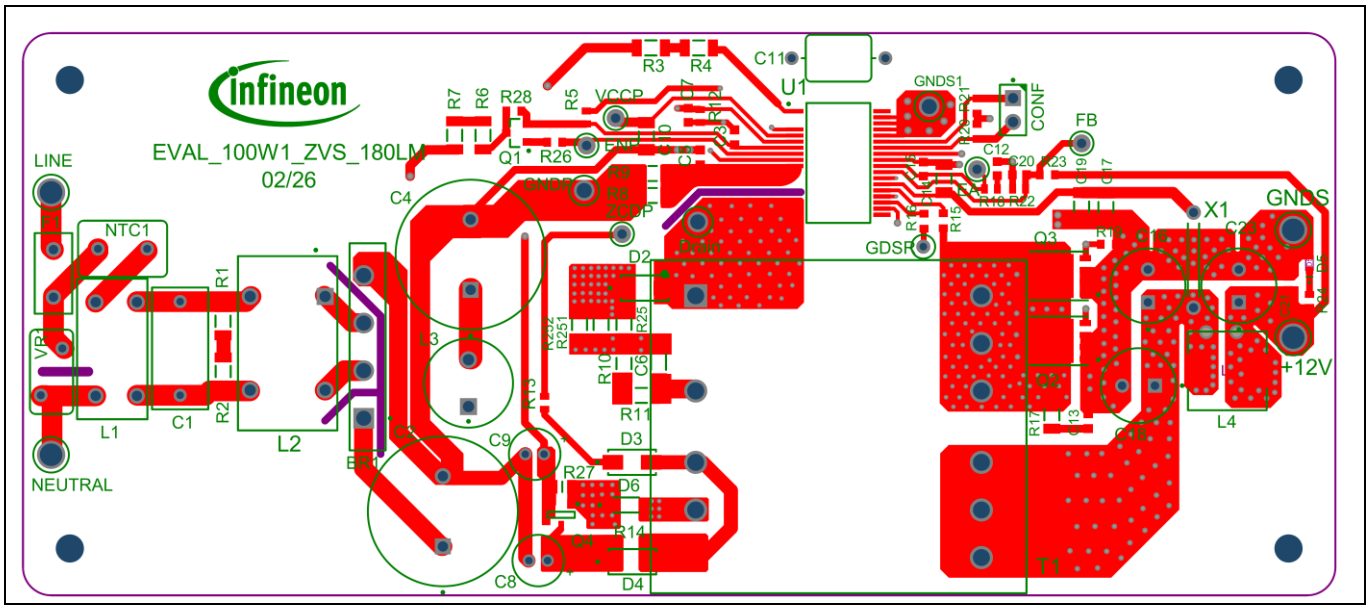


Figure 3 Top-side layout (view from top side)

6.2 Bottom-side layout

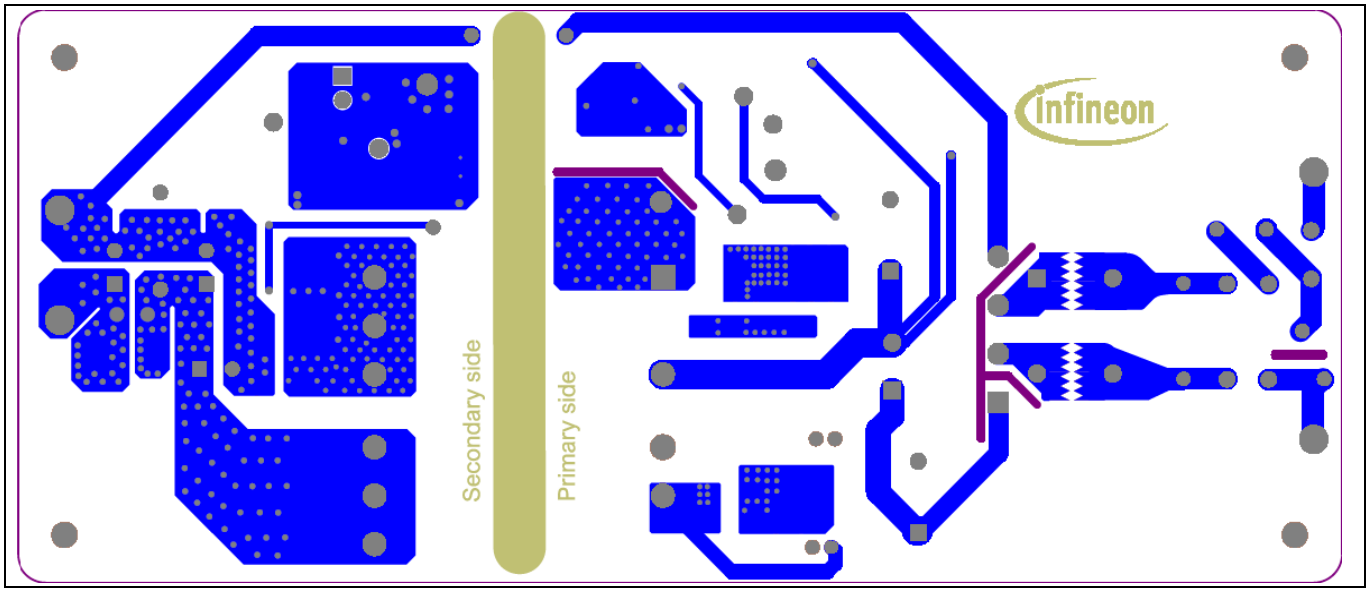


Figure 4 Bottom-side layout (view from bottom side)

7 Bill of materials

Table 6 BOM

No.	Designator	Description	Manufacturer	Part number	Qty
1	BR1	Bridge rectifier 1 phase 600 V 8 A GBU	onsemi	GBU8J	1
2	C1	Safety capacitors 310 VAC 0.33 µF 20%	DGCX	X2334K/310V/P=10	1
3	C13	MLCC - SMD/SMT 100 Volts 220 pF X7R 10% 0603	–	–	2
4	C3	MLCC - SMD/SMT 100 Volts 820 pF C0G/NP0 1% 0603	–	–	1
5	C5, C20	MLCC - SMD/SMT 50 Volts 680 pF X7R 10% 0603	–	–	2
6	C6	MLCC - SMD/SMT 1000 pF 1 kV 10% 1206	–	–	1
7	C7	MLCC - SMD/SMT 50 Volts 33 pF X7R 10% 0603	–	–	1
8	C8, C9	Aluminum electrolytic capacitors - Radial leaded 22 µF 35 V	BERYL	RG035M220LO5*11TA-1A1E	2
9	C10	MLCC - SMD/SMT 100 nF 50 VDC 10% 1206 X7T	–	–	1
10	C11	Safety capacitors 1500 pF 310 V 20%	KEMET	C741U152MSWDCA7317	1
11	C12	MLCC - SMD/SMT 50 Volts 68 nF X7R 10% 0603	–	–	1
12	C14, C19	MLCC - SMD/SMT 100 nF 50 V 10% 1206	–	–	2
13	C15	MLCC - SMD/SMT 50 Volts 1.5 nF X7R 10% 0603	–	–	1
14	C16, C18	CAP ALUM POLY 1200 uF 20% 16 V T/H	Nichicon	RNL1C122MDS1KX	2
15	C17	MLCC - SMD/SMT 10 uF 50 V 10% 1206	–	–	1
16	C21	MLCC - SMD/SMT 100 nF 50 V 10% 0603	–	–	1
17	D2	Surface mount rectifier 1.0 A/1000 V	onsemi	S1M	1
18	D3, D4	Diode Schottky 200 V 1 A DO214AC	Micro Commercial Co	SS1200-LTP	2
19	D5	Chip LED Waterclear, size 0603, blue	Würth Elektronik	150060BS75003	1
20	D6	Zener Diode 22 V 500 mW ±2% surface mount SOD-123	Vishay	MMSZ5251C-E3-08	1
21	Drain, GNDP, GNDS1	Test point THT, white	Keystone Electronics Corp.	5012	3

7 Bill of materials

No.	Designator	Description	Manufacturer	Part number	Qty
22	EA, ENP, FB, GDSR, VCCP, ZCDP	Test point THT, white	Keystone Electronics Corp.	5002	6
23	F1	Time lag fuse, 300 V, 3.15 A	Littelfuse	36913150000	1
24	GNDS, +12V, LINE, NEUTRAL	Solder terminal, double turret, .109 long	Keystone Electronics Corp.	1502-2	4
25	L1	Inductor common mode standard polarization core 4 pins, 275 µH	Endela Electronics	L-13-0100	1
26	L2	Inductor common mode standard polarization core 4 pins, 10 mH	Tenda	TD1515-10MH 0.2*1.5	1
27	L3	Radial leaded wire wound inductor WE-TI, 10 µH 4.70 A	Würth Elektronik	7447452100	1
28	L4	SMD WE-HCC HCur Cube8070 1µH 17A 2.95mΩ	Würth Elektronik	7443340100	1
29	NTC1	Power NTC 2.5Ω Y kink bulk	Bourns	BN-LG08Y2R5MYB	1
30	Q1	SIPMOS small-signal-transistor	Infineon Technologies	BSS127H6327XTSA2	1
31	Q4	Bipolar transistors - SOT-23, 45 V, 800 mA, NPN	Diotec	BC817-25	1
32	R1, R2	Thick film resistors - SMD 1/4 Watt 1.2 MΩ 1206 5%	–	–	2
33	R3, R4	Thick film resistors - SMD 50 kΩ 250 mW 1206 1%	–	–	2
34	R5	Thick film resistors - SMD 17.4 kΩ 100 mW 0603 1%	–	–	1
35	R6, R7	Thick film resistors - SMD 1/4 Watt 1.3 MΩ 1206 1%, 500 V rating	–	–	2
36	R10, R11	Thick film resistors - SMD 1/4 Watt 150 kΩ 1206 1%	–	–	2
37	R12	Thick film resistors - SMD 2 kΩ 1% 0603	–	–	2
38	R13, R18	Thick film resistors - SMD 22 kΩ 1% 0603	–	–	2
39	R14, R15	Thick film resistors - SMD 15 kΩ 100 mW 0603 1%	–	–	1
40	R16	Thick film resistors - SMD 0603 2.2 Ω 1%	–	–	1
41	R17	Thick film resistors - SMD 1/4 Watt 51 Ω 1206 5%	–	–	2
42	R19	Thick film resistors - SMD 10 kΩ 100 mW 0603 1%	–	–	1
43	R20	Thick film resistors - SMD 18 kΩ 1% 0603	–	–	1
44	R21	Thick film resistors - SMD 3.9 kΩ 1% 0603	–	–	1

7 Bill of materials

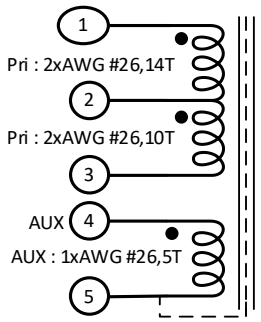
No.	Designator	Description	Manufacturer	Part number	Qty
45	R22	Thick film resistors - SMD 20 kΩ 100 mW 0603 1%	–	–	1
46	R23	Thick film resistors - SMD 180 kΩ 0603 1%	–	–	1
47	R24	Thick film resistors - SMD 5.1 kΩ 100 mW 0603 1%	-–	–	1
48	R25, R251, R252	Thick film resistors - SMD 1/4 Watt 100 Ω 1206 1%	–	–	3
49	R26	Thick film resistors - SMD 0 Ω 0603	–	–	1
50	R27	Thick film resistors - SMD 120 kΩ 0805	–	–	1
51	R28	Thick film resistors - SMD 0 Ω 0603	–	–	DNP
52	VR1	Varistors 275 VAC 10% 7 mm	Bourns	CV275K7BL1	1
53	X1	Through hole jumper, 10.16 mm pitch, 2 pins	Samtec	JL-400-25-T	1
54	CONF	Connector header through hole 2 position 0.100" (2.54 mm)	Samtec	TSW-102-08-G-S	1
55	C2, C4	Aluminium electrolytic capacitors - Radial leaded 120 µF 420 V	Ymin	KCMI2502T121MF	2
56	C23	CAP ALUM POLY 680 µF 20% 16 V T/H	AVX	RPF0811681M016K	1
57	Q2, Q3	Power-transistor, optimized for high performance SMPS	Infineon Technologies	ISC046N13NM6ATMA1	2
58	U1	CoolSET™ SiP	Infineon Technologies	ICE180LM	1
59	L4	SMD WE-HCC HCur Cube8070 1 µH 17 A 2.95 mΩ	Würth Elektronik	7443340100	1
60	T1	100 W transformer 750345654 Rev01	Würth Elektronik	750345654	1
61	R8, R9	Thick film resistors - SMD 1206 0.33 Ω 1%	Bourns	CRL1206-FW-R330ELF	2

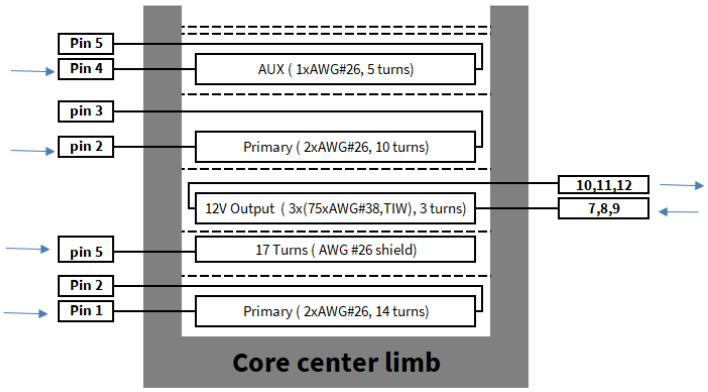
8 Transformer specifications

8.1 Electrical diagram and coil build

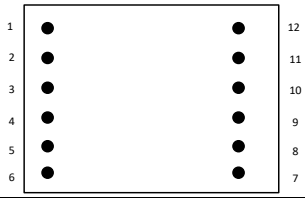
- Manufacturer and part number: Würth Electronik (750345654 Rev 01)

Core: PQ3220, Lp=190 µH, 24T: 3T: 5T (Np: Ns1: Naux)





Top view (PQ3220)



Wire size requirement :

Start	Stop	No. of turns	Wire size	Layer
1	2	14	2 x AWG#26	1/2 Primary
5		17	1 x AWG#26	SHIELD
7,8,9	10,11,12	3	3x(75xAWG#38 ,TIW)	Secondary
2	3	10	2 x AWG#26	1/2 Primary
4	5	5	1 x AWG#26	AUX

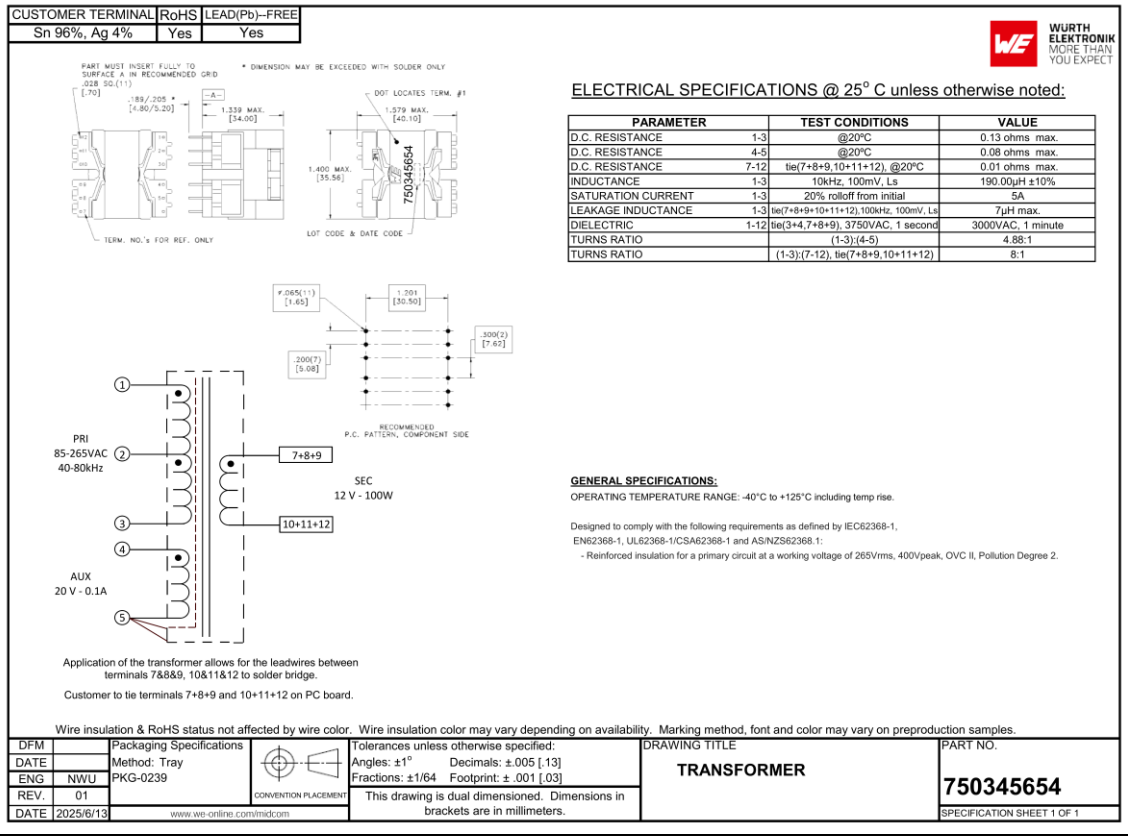


Figure 5 Electrical diagram and coil structure

9 Test results

All performance data is measured at room temperature T_A = 25°C unless otherwise specifically mentioned.

9.1 Efficiency

Efficiency data has been taken under +12 V load condition with NTC1 shorted and LED D5 removed. The standby power measured at 230 VAC is 77 mW.

Table 7 Efficiency

Input (VAC/Hz)	Load percentage (%)	PIN (W)	VOUT (VDC)	IOUT (A)	POUT (W)	Efficiency η (%)	Average η (%)
90/60	No load	0.02	11.99	0.00			
	10	10.96	12.00	0.84	10.04	91.61	
	25	26.59	11.99	2.06	24.75	93.06	91.96
	50	53.45	11.97	4.14	49.54	92.70	
	75	81.05	11.95	6.21	74.21	91.57	
	100	109.22	11.94	8.28	98.86	90.52	
115/60	No load	0.02	11.99	0.00			
	10	11.03	12.00	0.84	10.04	91.07	
	25	26.51	11.99	2.06	24.75	93.35	92.94
	50	52.86	11.98	4.12	49.41	93.47	
	75	80.14	11.94	6.24	74.47	92.93	
	100	106.88	11.90	8.27	98.35	92.02	
230/50	No load	0.08	11.99	0.00			
	10	11.23	11.99	0.84	10.05	89.52	
	25	26.67	11.98	2.06	24.72	92.68	93.32
	50	53.34	11.95	4.18	49.95	93.65	
	75	79.62	11.90	6.26	74.49	93.56	
	100	104.70	11.85	8.25	97.78	93.39	
264/50	No load	0.11	11.99	0.00			
	10	11.31	11.99	0.84	10.04	88.72	
	25	26.81	11.97	2.06	24.70	92.16	93.25
	50	53.42	11.95	4.18	49.96	93.52	
	75	79.69	11.92	6.27	74.71	93.76	
	100	104.85	11.87	8.26	98.09	93.56	

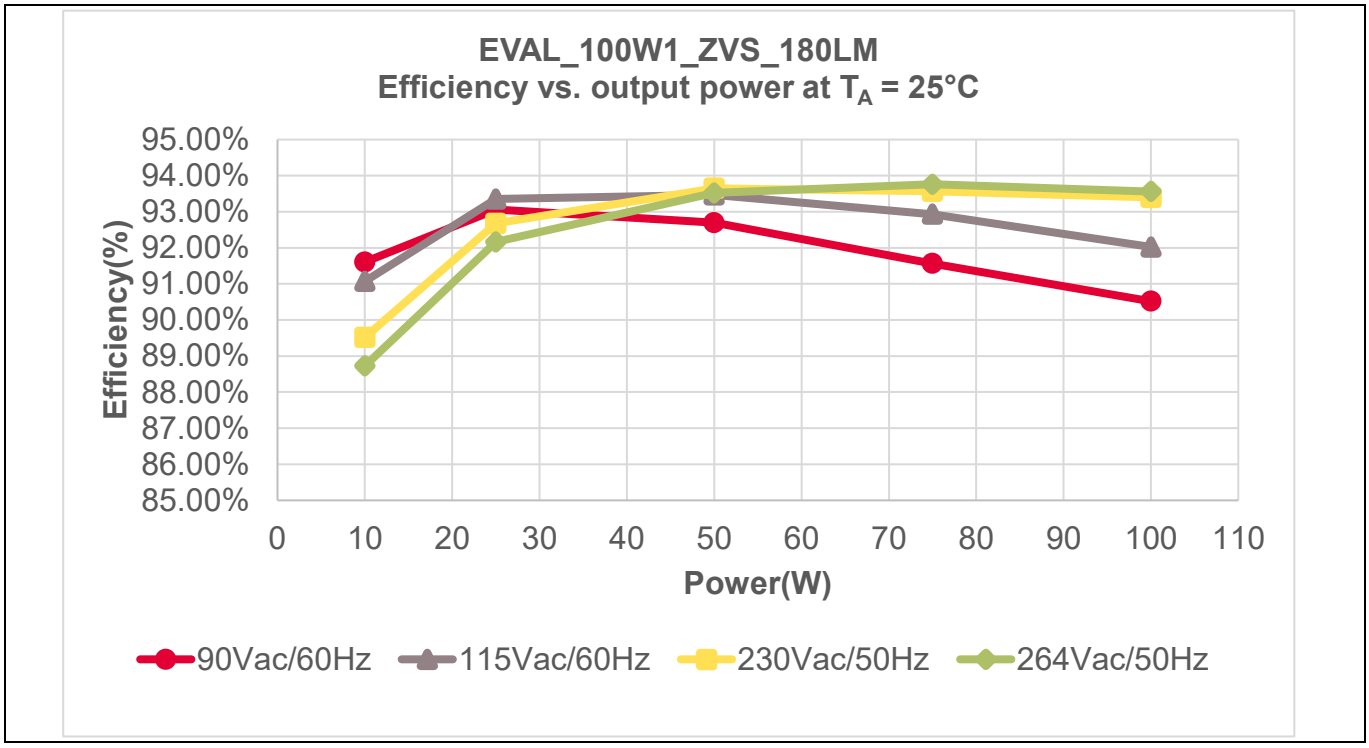


Figure 6 Efficiency vs. output power (W)

9.2 ESD immunity (EN 61000-4-2)

The evaluation board was subjected to ESD testing according to EN 61000-4-2 level 3 (±8 kV contact and ±15 kV air discharge). It was tested at full load (resistive load) and meets criteria A (normal performance within the specification limits).

Table 8 ESD immunity test result

Description	ESD test	Level	Number of strikes				Test result
			Vout	GNDS	Line	Neutral	
230 VAC, 100 W	Contact	±8 kV	10	10	10	10	Pass
	Air	±15 kV	10	10	10	10	Pass

9.3 Surge immunity (EN 61000-4-5)

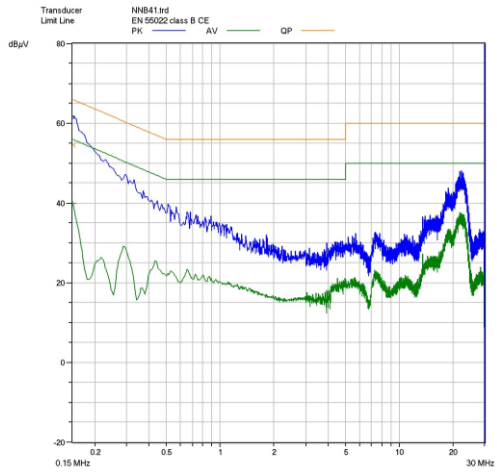
The evaluation board was subjected to a surge immunity test according to EN 61000-4-5 level 4 (±2 kV Differential mode and ±4 kV Common mode). It was tested at full load (resistive load) and meets criteria A (normal performance within the specification limits).

Table 9 Surge immunity test result

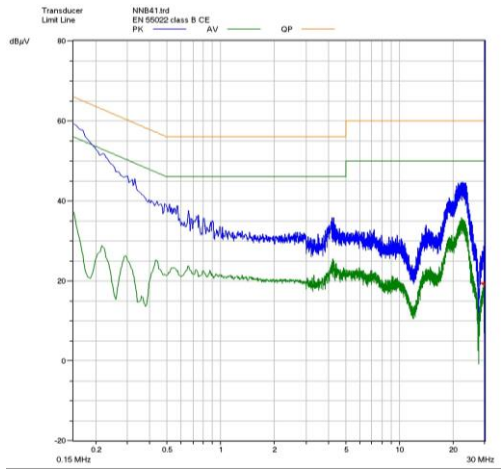
Description	Test	Level		Number of strikes				Test result
				0°	90°	180°	270°	
230 VAC, 100 W	Differential mode	±2 kV	L → N	3	3	3	3	Pass
	Common mode	±4 kV	L → G	3	3	3	3	Pass
		±4 kV	N → G	3	3	3	3	Pass

9.4 Conducted emissions (EN 55022 Class B)

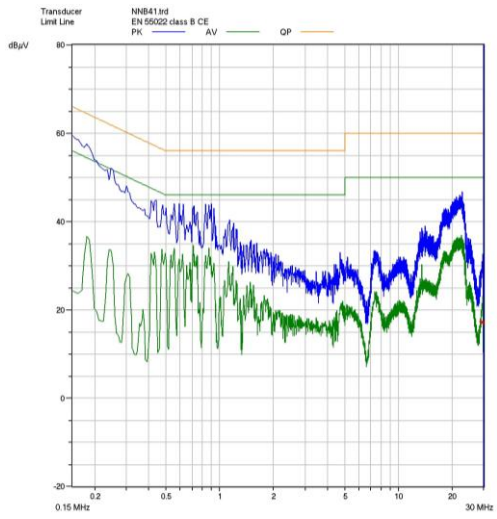
Conducted EMI was measured by Schaffner (SMR4503) and followed the test standard of EN 55022 (CISPR 22) Class B. The evaluation board was tested at full load (resistive load) at input voltages of 115 V AC and 230 VAC.



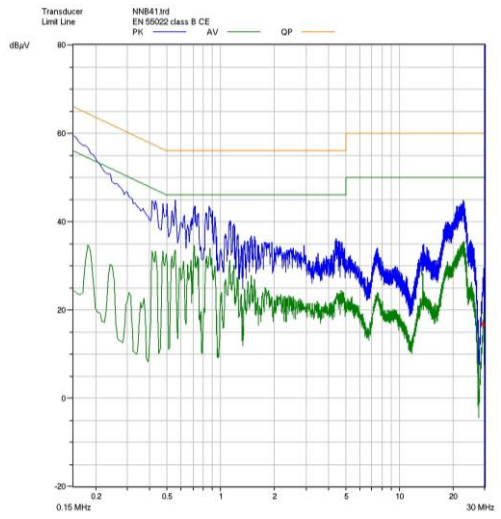
Conducted emission at 115 VAC line



Conducted emission at 115 VAC neutral



Conducted emission at 230 VAC line



Conducted emission at 230 VAC neutral

Figure 7 Conducted emissions

9.5 Thermal measurement

The thermal testing of the evaluation board was executed in open air without forced ventilation at an ambient temperature of 25°C. An infrared thermography camera (FLIR-T62101) was used to capture the thermal reading of critical components. The measurements were taken at the maximum load running for one hour with NTC1 shorted. The tested input voltages were 90 V AC and 264 V AC.

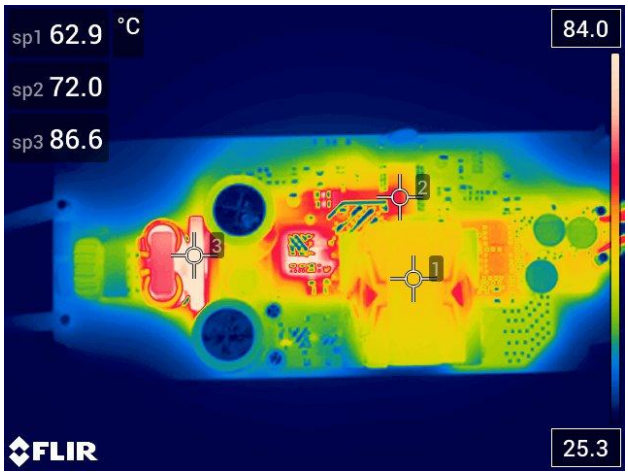
Table 10 Component temperature at full load under T_A = 25°C

Reference designator	Major component	90 VAC (°C)	264 VAC (°C)
R25, R251, R252	Primary side RCD snubber resistor	90.4	70.5
IC1	ICE180LM	72	60.1

9 Test results

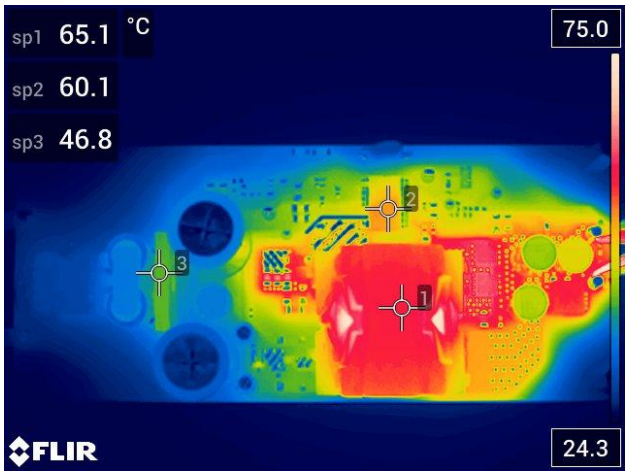
Reference designator	Major component	90 VAC (°C)	264 VAC (°C)
Q2	SR MOSFET	67.6	69.1
BR1	Bridge diode	86.6	46.8
T1	Main transformer core	62.9	65.1
T1	Main transformer winding	72.8	74.0

90 VAC full load and 25°C ambient

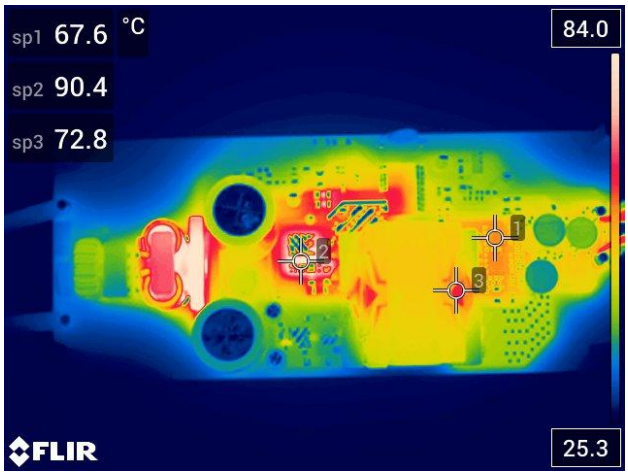


Top side

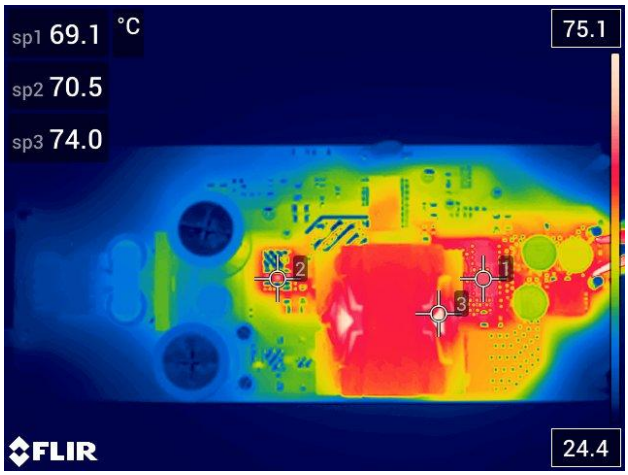
264 VAC full load and 25°C ambient



Top side



Top side



Top side

Figure 8 Infrared thermal image of EVAL_100W1_ZVS_180LM

10 Waveforms and scope plots

All waveforms and scope plots were recorded with a Teledyne LeCroy HDO4034 oscilloscope.

10.1 Start-up with maximum load

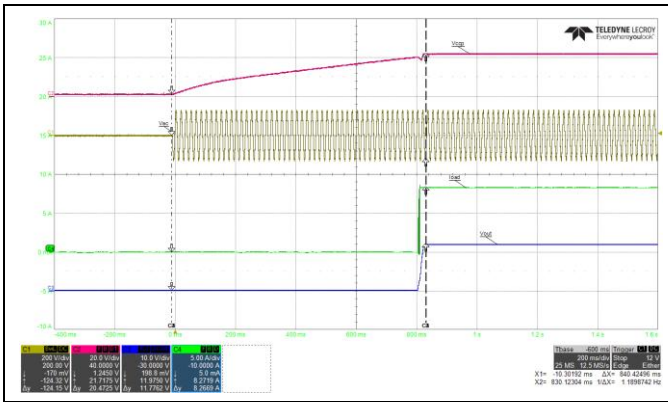
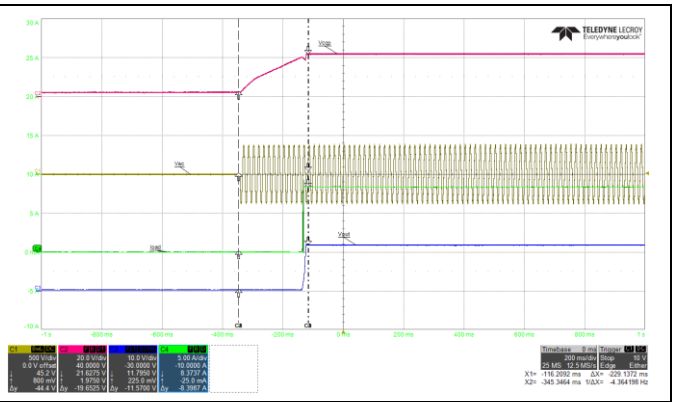
	
C1 : AC line voltage (V_{AC}) C2 : VCCP voltage (V_{VCCP}) C3 : Output voltage (V_{OUT}) C4 : Output current (I_{OUT})	C1 : AC line voltage (V_{AC}) C2 : VCCP voltage (V_{VCCP}) C3 : Output voltage (V_{OUT}) C4 : Output current (I_{OUT})
Start-up time at 90 VAC and maximum load ≈ 840 ms	Start-up time at 264 VAC and maximum load ≈ 230 ms
The board can startup as expected over 90 ~ 264 VAC, output voltage rises smoothly and regulates at 12 V.	

Figure 9 Start-up

10.2 Soft-start

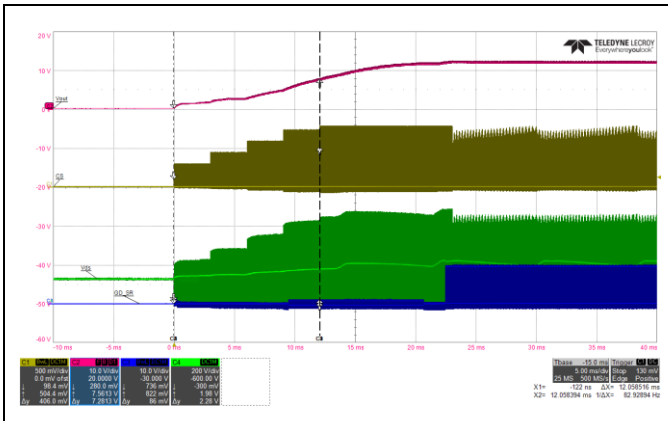
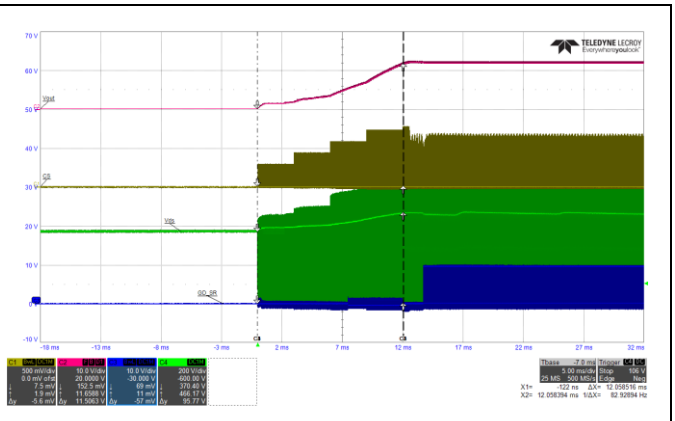
	
C1 : CS voltage (V_{CS}) C2 : Output voltage (V_{OUT}) C3 : Output voltage SR gate (V_{GDSR}) C4 : Drain voltage (V_{DRAIN})	C1 : CS voltage (V_{CS}) C2 : Output voltage (V_{OUT}) C3 : Output voltage SR gate (V_{GDSR}) C4 : Drain voltage (V_{DRAIN})
Soft-start time at 90 VAC and maximum load ≈ 12 ms	Soft-start time at 264V AC and maximum load ≈ 12 ms
Stepped soft-start from V_{SS1}(typ. 0.3V) to V_{CSOCP1}(typ. 0.8 V).	

Figure 10 Soft-start

10.3 Switching waveform at full load

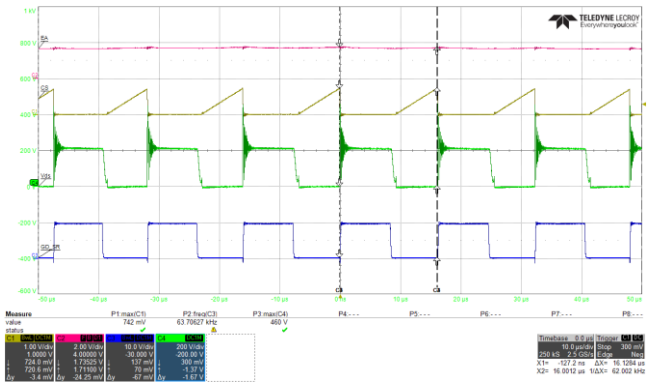
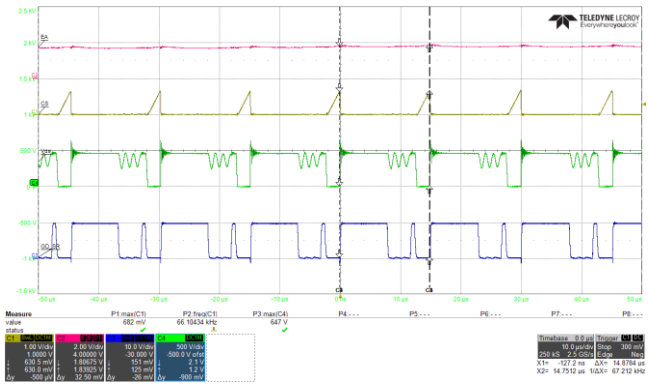
	
C1 : CS voltage (V_{CS}) C2 : EA output (V_{EA}) C3 : Output voltage SR gate (V_{GDSR}) C4 : Drain voltage (V_{DRAIN})	C1 : CS voltage (V_{CS}) C2 : EA output (V_{EA}) C3 : Output voltage SR gate (V_{GDSR}) C4 : Drain voltage (V_{DRAIN})
V_{IN} = 90 VAC, full load; the first valley is measured (QR = 1 at low line). V_{DS_MAX} = 460 V, $f_{switching}$ = 63.7 kHz	V_{IN} = 264 VAC, full load; the third valley is measured (QR = 3 at high line with ZVS switching). V_{DS_MAX} = 647 V, $f_{switching}$ = 66 kHz
ICE180LM operates quasi-resonant valley switching at low line and together with zero voltage switching at high line.	

Figure 11 Drain and CS voltage at maximum load

10.4 SR FET voltage at full load

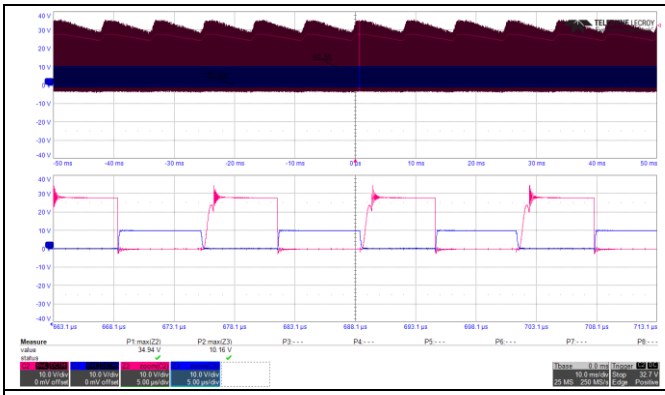
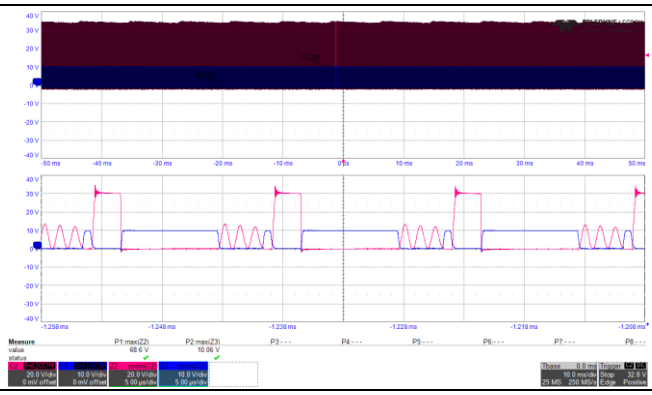
	
C2 : SR drain voltage (V_{SR_DRAIN}) C3 : Output voltage SR gate (V_{GDSR})	C2 : SR drain voltage (V_{SR_DRAIN}) C3 : Output voltage SR gate (V_{GDSR})
V_{IN} = 90 VAC, full load. Maximum drain voltage is around 34.94 V	V_{IN} = 264 V AC, full load. Maximum drain voltage is around 65.0 V
The measured SR MOSFET voltage stress at 264 VAC input is well below its voltage rating (100 V).	

Figure 12 SR FET voltage

10.5 Output ripple voltage at maximum load

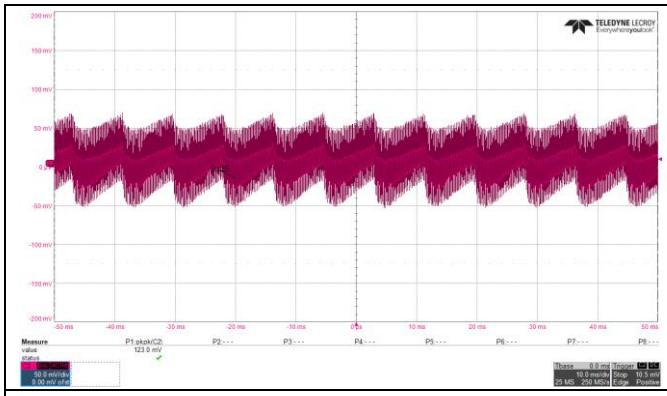
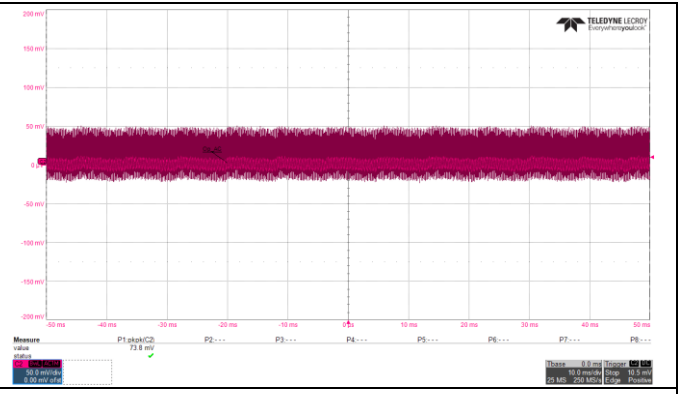
	
C2 : Output voltage, AC coupled (V_{OUT})	C2 : Output voltage, AC coupled (V_{OUT})
V_{IN} = 90 VAC, full load. Vripple_pk for +12 V output voltage: 120 mV	V_{IN} = 264 VAC, full load. Vripple_pk for +12 V output voltage: 73.8 mV
The measured output ripple is around 1% of the output voltage.	

Figure 13 Output ripple voltage at full load (20 MHz bandwidth and 10 µF electrolytic capacitor in parallel with 0.1 µF ceramic capacitor)

10.6 Hysteretic mode operation

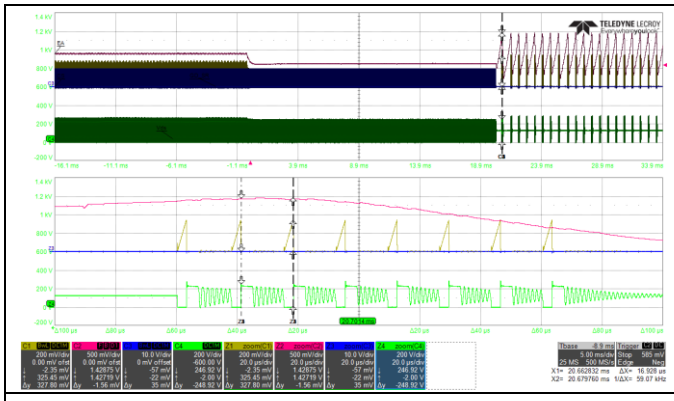
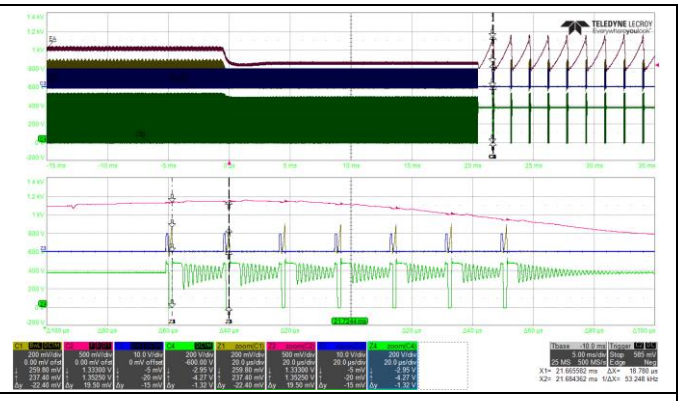
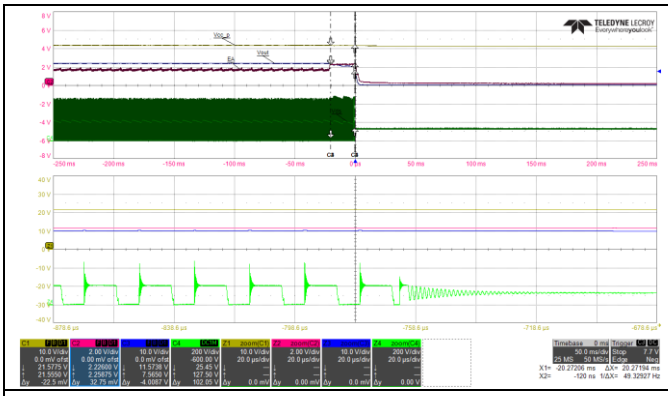
	
C1 : CS voltage (V_{CS}) C2 : EA output (V_{EA}) C3 : Output voltage SR gate (V_{GDSR}) C4 : Drain voltage (V_{DRAIN})	C1 : CS voltage (V_{CS}) C2 : EA output (V_{EA}) C3 : Output voltage SR gate (V_{GDSR}) C4 : Drain voltage (V_{DRAIN})
• 90 VAC, 10 W to 3.6 W load • Operation at f_{osc_ABM} = 59.07 kHz	• 264 VAC, 10 W to 1.2 W load • Operation at f_{osc_ABM} = 53.9 kHz
At light loads, the system enters the hysteretic mode to reduce the power loss.	

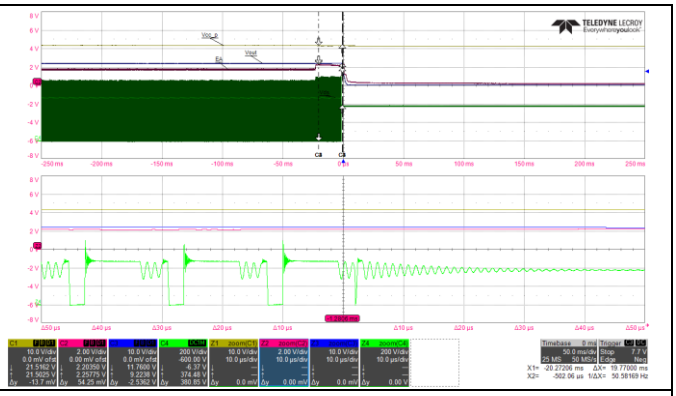
Figure 14 Hysteretic mode operation

10.7 Overload protection



C1 : VCC primary voltage (V_{VCCP})
C2 : EA output (V_{EA})
C3 : Output voltage (V_{OUT})
C4 : Drain voltage (V_{DRAIN})

At 90 VAC, 100 W, load stepped to 120 W. System enters overload protection(auto-restart) when V_{EA} >2.1 V and blanking time ~20 ms



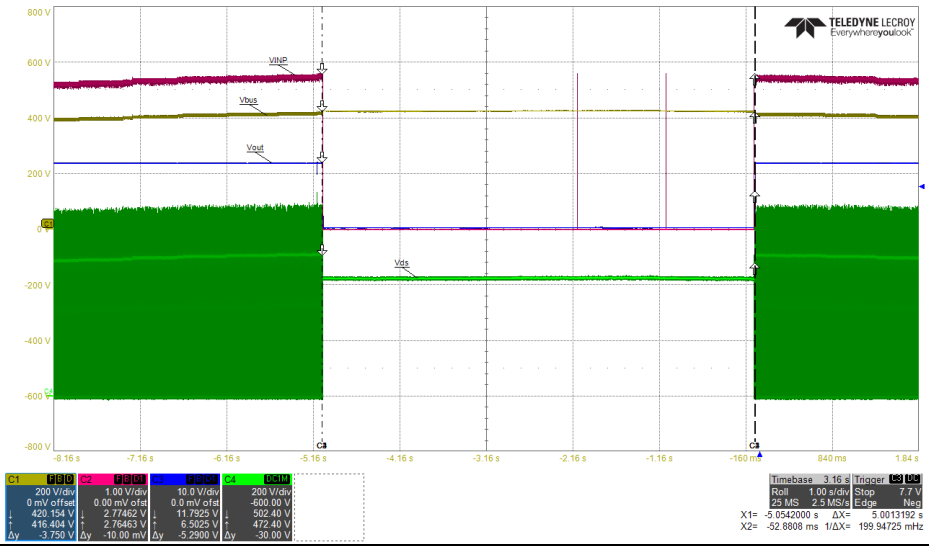
C1 : VCC primary voltage (V_{VCCP})
C2 : EA output (V_{EA})
C3 : Output voltage (V_{OUT})
C4 : Drain voltage (V_{DRAIN})

At 264 VAC, 100 W, load stepped to 120 W. System enters overload protection when V_{EA} > 2.1 V and blanking time ~20 ms

System enters overload protection at ~20% higher than rated load.

Figure 15 Overload protection

10.8 Line OVP

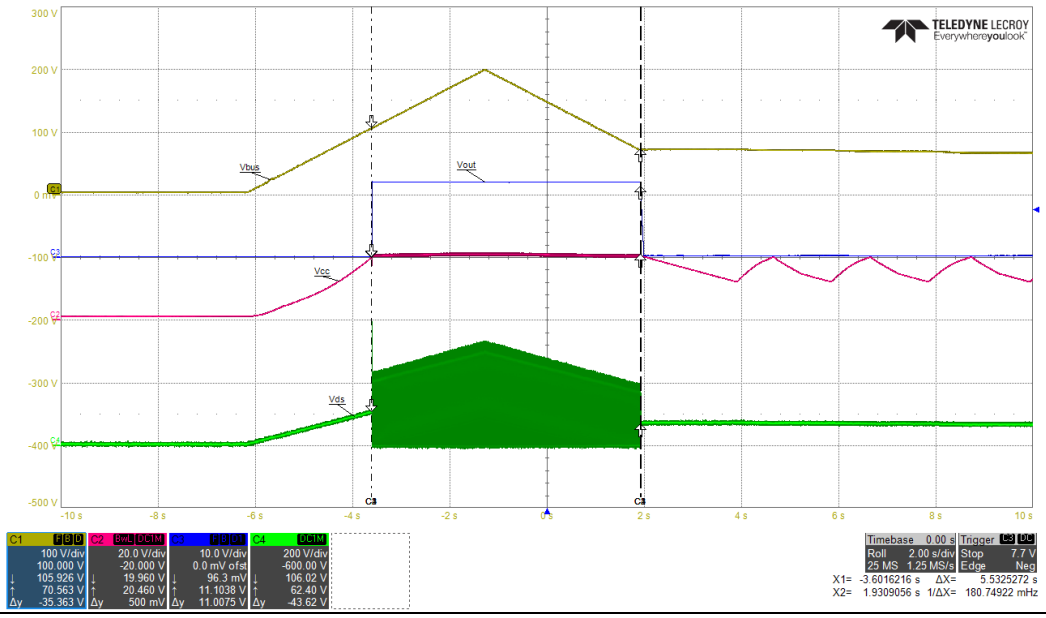


C1 : DC bus voltage (V_{BUS})
C2 : VINP (V_{VINP})
C3 : Output voltage (V_{OUT})
C4 : Drain voltage (V_{DRAIN})

Increase the input from 270 VAC to 300 VAC and decrease back to 270 VAC. System detects and enters line OVP at V_{BUS} > 420 VDC when the V_{VINP} >2.8 V. System enters non switch auto restart protection. The switching resumes when V_{BUS} < 416 VDC.

Figure 16 Line OVP

10.9 Brown-in and brown-out



C1 : DC bus (V_{BUS})
C2 : VCC primary (V_{VCCP})
C3 : Output voltage (V_{OUT})
C4 : Drain voltage (V_{DRAIN})

Increase the input voltage from 0 VAC to 140 VAC and decrease back to 0 VAC. Brown-in is measured at V_{BUS} >105 VDC and brown-out is measured at V_{BUS} < 70 VDC. When the bulk capacitor voltage drops below brown-out, non-switch auto restart is triggered.

System enters brown-in and brown-out protection as expected.

Figure 17 Brown-in and brown-out

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References

[1] Infineon Technologies AG: *CoolSET™ SiP ICE180LM datasheet*; Available online

[2] Infineon Technologies AG: *Design guide for ZVS QR flyback using CoolSET™ SiP*; Available online

Revision history

Document revision	Date	Description of changes
V 1.0	2026-06-02	Initial release
V 1.1	2026-10-29	Updated Section 4, Section 7, Section 8.1

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