60 W 12 V 5 V SMPS demo board with ICE5QSAG and IPA80R600P7

DEMO_5QSAG_60W1

About this document

Scope and purpose

This document is an engineering report for a 60 W dual-output SMPS with the latest fifth-generation Infineon QR controller ICE5QSAG and CoolMOS™ IPA80R600P7. The power supply is designed with a universal input compatible with most geographic regions and dual isolated outputs (+12 V/4.58 A and +5 V/1 A), as typically employed in most home appliances.

Highlights of the demo board:

- High efficiency under light-load conditions to meet ENERGY STAR requirements
- Single-layer PCB design for compatibility with wave-soldering process and low-cost manufacturing
- Auto-restart protection scheme to minimize interruption to enhance end-user experience

Intended audience

This document is intended for power supply design/application engineers, students, etc. who wish to design low-cost and highly reliable systems for off-line SMPS, either auxiliary power supplies for white goods, PCs, servers and TVs, or enclosed adapters for Blu-ray players, set-top boxes, games consoles, etc.

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1 Abstract

This engineering report is a 60 W 12 V and 5 V demo board designed in a QR Flyback converter topology using the fifth-generation QR controller ICE5QSAG and a P7 series of HV CoolMOS™ IPA80R600P7. The target applications of ICE5QSAG are either auxiliary power supplies for white goods, PCs, servers and TVs, or enclosed adapters for Blu-ray players, set-top boxes, games consoles, etc. The new improved digital frequency reduction with proprietary QR operation offers lower EMI and higher efficiency for a wide AC range by reducing the switching frequency difference between low- and high-line. The enhanced Active Burst Mode (ABM) power enables flexibility in standby power operation range selection and QR operation during ABM. As a result, the system efficiency, over the entire load range, is significantly improved compared to conventional free-running QR converters implemented with only maximum switching frequency limitation at light load. In addition, numerous adjustable protection functions have been implemented in ICE5QSAG to protect the system and customize the IC for the chosen application. In case of failure modes like brown-out or line Over Voltage (OV), V_{CC} OV/Under Voltage (UV), open control-loop or over-load, output OV, over-temperature, V_{CC} short-to-GND and CS short-to-GND, the device enters protection mode. By means of the cycle-by-cycle Peak Current Limitation, the dimensions of the transformer and the current rating of the secondary diode can both be optimized. In this way, a cost-effective solution can easily be achieved.

2 Demonstrator board

This document provides complete design details including specifications, schematics, Bill of Materials (BOM), and PCB layout and transformer design and construction information. This information includes performance results pertaining to line/load regulation, efficiency, transient load, thermal conditions, conducted EMI scans, etc.

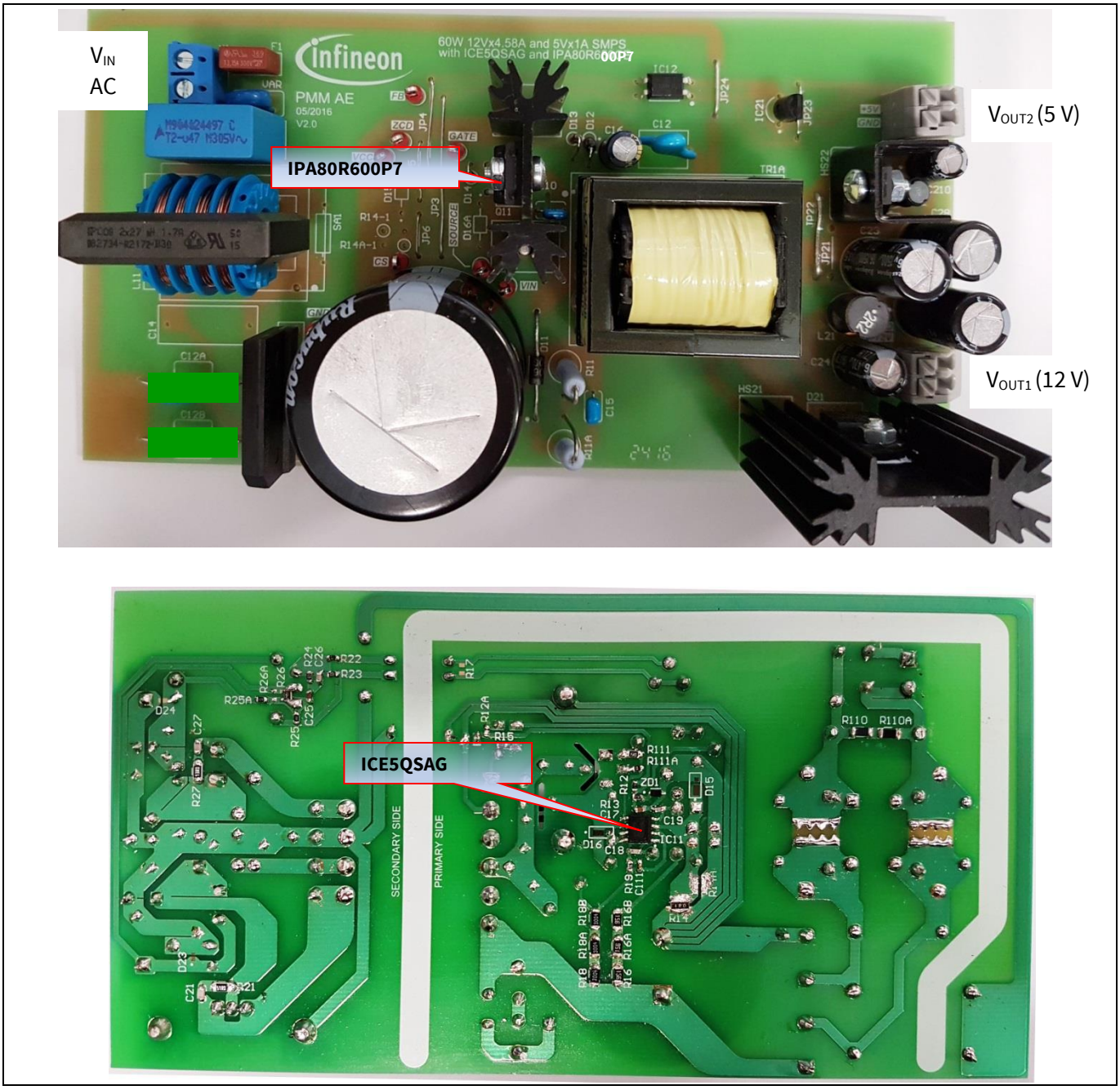


Figure 1 DEMO_5QSAG_60W1

3 Power supply specifications

The table below represents the minimum acceptance performance of the design. Actual performance is listed in the measurements section.

Table 1 Specifications of DEMO_5QSAG_60W1

Description	Symbol	Min.	Typ.	Max.	Units	Comments
Input						
Voltage	V_{IN}	85	–	300	V AC	Two wires (no P.E.)
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load input power	P_{stby_NL}	–	–	0.09	W	230 V AC
40 mW load input power	P_{stby_ML}	–	–	0.20	W	230 V AC
Output						
Output voltage 1	V_{OUT1}	–	12	–	V	±5 %
Output current 1	I_{OUT1}	0.001	2.29	4.58	A	
Output voltage ripple 1	$V_{RIPPLE1}$	–	–	100	mV	20 MHz BW
Output voltage 2	V_{OUT2}	–	5	–	V	±5 percent
Output current 2	I_{OUT2}	0.006	0.5	1	A	
Output voltage ripple 2	$V_{RIPPLE2}$	–	–	100	mV	20 MHz BW
Max. power output	P_{OUT_Max}	–	–	60	W	
Efficiency						
Max. load	η	–	83	–	%	115 V AC/230 V AC
Average efficiency at 25 percent, 50 percent, 75 percent and 100 percent of P_{OUT_Max}	η_{avg}	84	–	–	%	115 V AC/230 V AC
Environmental						
Conducted EMI		6	–	–	dB	Margin, CISPR 22 class B
ESD		10	–	–	kV	EN 61000-4-2
Surge immunity						EN 61000-4-5
Differential Mode (DM)		2	–	–	kV	
Common Mode (CM)		4	–	–	kV	
Ambient temperature	T_{amb}	0	–	50	°C	Free conviction, sea level
Form factor		160 × 83 × 43			mm^3	L × W × H

Note: *"The demo board is designed for dual-output with cross-regulated loop feedback (FB). It may not regulate properly if loading is applied only to single-output. If the user wants to evaluate for single-output (12 V only) conditions, the following changes are necessary on the board.*

1. Remove D22, L22, C28, C210, R25A (to disable 5 V output).
2. Change R26 to 10 kΩ and R25 to 38 kΩ (to disable 5 V FB and enable 100 percent weighted factor on 12 V output).

Since the board (especially the transformer) is designed for dual-output with optimized cross-regulation, single-output efficiency might not be optimized. It is only for IC functional evaluation under single output conditions."

4 Circuit diagram

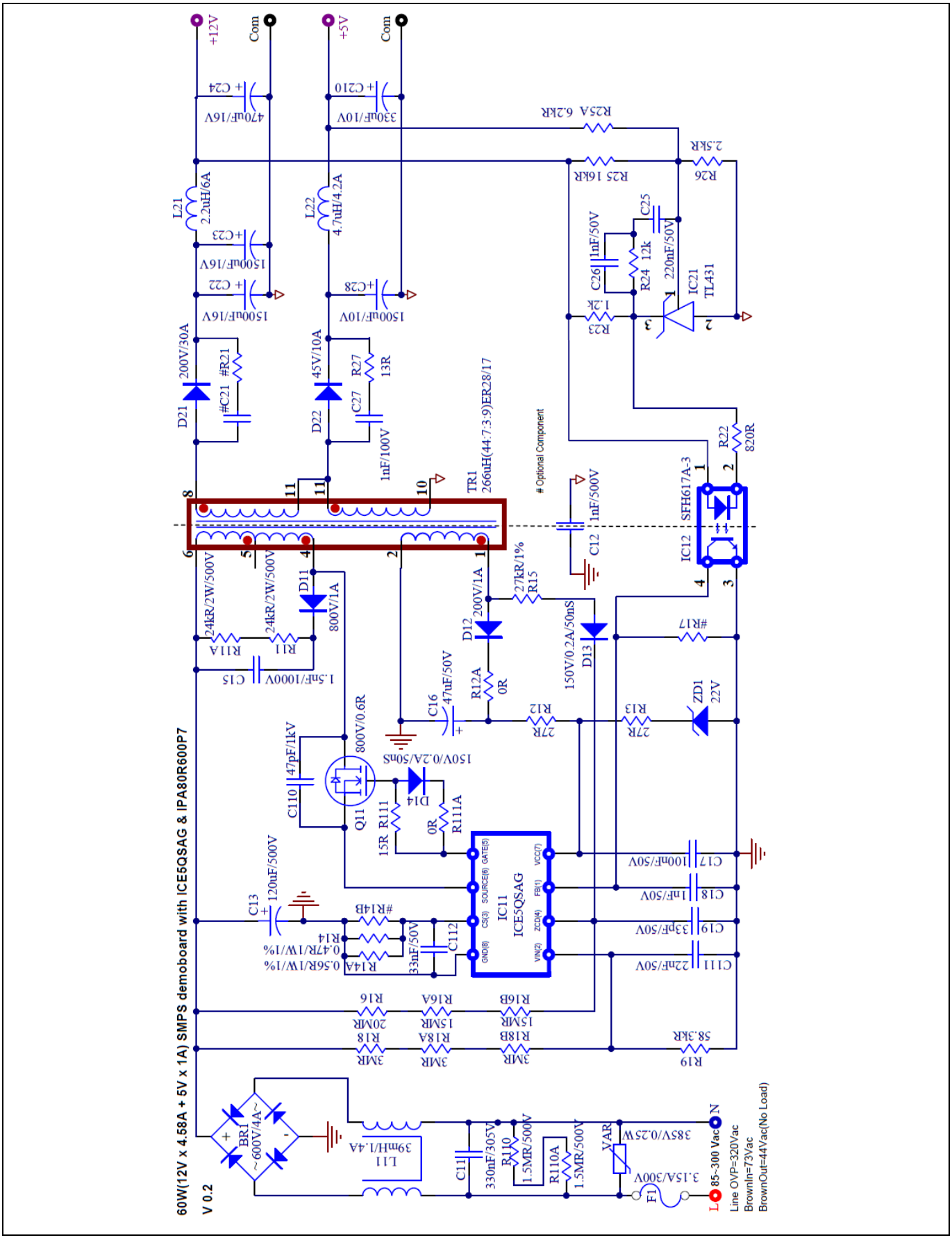


Figure 2 Schematic of DEMO_5QSAG_60W1

5 Circuit description

In this section, the design circuit for the SMPS unit will be briefly described by the different functional blocks. For details of the design procedure and component selection for the Flyback circuitry please refer to the IC design guide [3] and calculation tool [4].

5.1 EMI filtering and line rectification

The input of the PSU is taken from the AC power grid, which is in the range of 85 V AC~300 V AC. The fuse F1 is right at the entrance to protect the system in case of excess current entering the system circuit due to any fault. Following is the varistor VAR, which is connected across L and N to absorb the line surge transient. Inductors L11 and C11 form a filter to attenuate the DM and CM conducted EMI noise. C11 must be X-capacitor grade. There are optional spark-gap devices SA1 and SA2 to absorb further higher surge level transient if required by the system. Resistors R110 and R110A are used to discharge the X-capacitor when the AC is off in order to fulfill the IEC61010-1 and UL1950 safety requirements. The bridge rectifier BR1 rectifies the AC input into DC voltage, filtered by the bulk capacitor, C13.

5.2 Flyback converter power stage

The Flyback converter power stage consists of C13, transformer TR1, a primary HV MOSFET (CoolMOS™ IPA80R600P7), secondary rectification diodes D21 and D22, secondary output capacitors and filtering (C22, C23, L21 and C24 for V_{OUT1} and C28, L22 and C210 for V_{OUT2}).

When the primary HV MOSFET turns on, some energy is stored in the transformer. When it turns off, the stored energy is released to the output capacitors and the output loading through the output diode D21 and D22.

A sandwich winding structure for the transformer TR1 is used to reduce the leakage inductance, reducing the loss in the clamper circuit. TR1 has two output windings: one for the V_{OUT1} (12 V) and the other for the V_{OUT2} (5 V). The output rectification of V_{OUT1} is provided by the diode D21 through the filtering of C22, C23, L21 and C24. The output rectification of V_{OUT2} is provided by diode D22 through the filtering of C28, L22 and C210. All the secondary capacitors must be the low-ESR type, which can effectively reduce the switching ripple. Together with the Y-capacitor C12, C12A and C12B across the primary and secondary side, the EMI noise can be further reduced to comply with CISPR 22 specifications.

5.3 Control of Flyback converter through fifth-generation QR controller ICE5QSAG

5.3.1 PWM control and switching MOSFET

The PWM pulse is generated by the fifth-generation QR PWM current-mode controller ICE5QSAG, and this PWM pulse drives the HV power MOSFET IPA80R600P7. The CoolMOS™ provides all the benefits of a fast-switching superjunction (SJ) MOSFET, while not sacrificing ease of use. It achieves extremely low conduction and switching losses, and can make switching applications more efficient, more compact, lighter and cooler. The PWM switch-on is determined by the zero-crossing input signal and the value of the up/down counter. The PWM switch-off is determined by the FB signal V_{FB} and the Current Sensing (CS) signal V_{CS}. ICE5QSAG also performs all necessary protection functions in Flyback converters. More details are provided in the product datasheet.

5.3.2 Current sensing

The ICE5QSAG is a current mode controller. The peak current is controlled cycle-by-cycle through the CS resistors R14 and R14A in the CS pin (pin 3), so transformer saturation can be avoided and the system is more robust and reliable.

5.3.3 FB and compensation network

Resistors R25 and R25A are used to sense the V_{OUT1} and V_{OUT2} through the shared current regulation method and FB to the demo pin (pin 1) of error amplifier IC21 with demo to the voltage at resistor R26 and R26A. A type 2 compensation network C25, C26 and R24 is connected between the output pin (pin 3) and the demo pin (pin 2) of the IC21 to stabilize the system. The IC21 further connects to pin 2 of the optocoupler, and IC12 with a series resistor R22 to convert the control signal to the primary side through the connection of pin 4 of the IC12 to ICE5QSAG FB pin (pin 1) and complete the control loop. Both the optocoupler IC12 and the error amplifier IC21 are biased by V_{OUT1}; IC12 is a direct connection while IC21 is through an R23 resistor.

The FB pin of ICE5QSAG is a multi-function pin, which is used to select the entry burst power level (there are two levels available) through R17 and also the burst-on/burst-off sense input during ABM.

5.4 Unique features of the fifth-generation QR controller

5.4.1 Fast self-start-up and sustaining of V_{CC}

The IC start-up uses the cascode structure integrated into the package to charge up the V_{CC} capacitor during the start-up stage [3]. The Zero Crossing Detection (ZCD) pin (pin 4) is a multi-function pin and it serves as the start-up pin with the connection of pull-up resistors R16, R16A and R16B, which has the other end connecting to the bus voltage during the start-up phase. The device is implemented with two steps of charging current: the smaller current 0.2 mA (V_{VCC_typ} = 0 V~1.1 V) and the larger current 3.2 mA (V_{VCC_typ} = 1.1 V~16 V). The start-up time consists of the addition of those two charging times. With V_{CC} capacitor C16 at 47 µF, the start-up time is shortened to around 0.35 s.

After start-up, the IC V_{CC} supply is sustained by the auxiliary winding of transformer TR1, which needs to support the V_{CC} to be above Under Voltage Lockout (UVLO) voltage (10 V typ.) through the rectifier circuit D12, R12, R12A and C17.

5.4.2 QR switching with valley sensing

ICE5QSAG is a QR Flyback controller, which always turns on at the lowest valley point of the drain voltage. The IC senses the valley point through the ZCD pin (pin 4), which monitors the auxiliary winding voltage by R15, D13 and C19 to the ZCD pin (pin 4) together with the internal resistor R_{ZCD}. The IC detects the valley crossing signal. When the ZCD voltage drops below 100 mV (typ.), the CoolMOS™ is allowed to switch on. With QR switching, the lowest switching losses can be achieved for good efficiency.

5.4.3 System robustness and reliability through protection features

5.4.3.1 Input voltage monitoring and protection

To avoid system damage due to the high AC input transient, the SMPS unit requires the input line Over Voltage Protection (OVP) to stop the Flyback converter switching whenever the V_{Bus} voltage exceeds the operating range. The IC has a V_{IN} pin (pin 2), which can sense V_{Bus} voltage through voltage dividers R18, R18A, R18B and R19. When the V_{IN} pin exceeds the protection threshold 2.9 V (typ.), the IC stops switching. With the same V_{IN} sensing, ICE5QSAG also implements input Under Voltage Protection (UVP) (brown-in/brown-out) to prevent the Over Current (OC) stress of the power-stage components when the input voltage is too low.

5.4.3.2 Other protections with auto restart

Besides input OVP and UVP, ICE5QSAG has more comprehensive system protection features, such as V_{CC} OV, V_{CC} UV, over-load, output short-circuit, open-loop protection, output OV, over-temperature, CS short-to-GND, V_{CC} short-to-GND, etc.

5.5 Clamper circuit

A clamper network D11, C15, R11 and R11A is used to reduce the switching spikes for the drain pin, which are generated from the leakage inductance of the transformer TR1. This is a dissipative circuit, and the selection of the R11 and R11A needs to be fine-tuned.

5.6 PCB design tips

For a good PCB design layout, there are several points to note.

- The power loop needs to be as small as possible (see Figure 3). There are three power loops in the demo design; one from the primary side and two from the secondary side. For the primary side, it starts from the bulk capacitor (C13) positive to the bulk capacitor negative. The power loop components include C13, the main primary transformer winding (pin 6 and pin 4 of TR1), the power MOSFET (Q11) and the CS pin of the controller IC11 and CS resistors R14 and R14A. For the secondary side, the 12 V output starts from the secondary transformer windings (pin 8 of TR1), output diode D21 and output capacitors C22 and C23, while the 5 V output starts from the secondary transformer windings (pins 11 of TR1), output diode D22 and output capacitor C28.
- A star-ground concept should be used to avoid unexpected HF noise coupling, which can affect control. The ground of the small-signal components, e.g. C111, C17, C18, C19 and R19, and the emitter of optocoupler (pin 3 of IC12) etc. should connect directly to the IC ground (pin 8 of IC11). Then it connects to the negative terminal of the C13 capacitor directly.

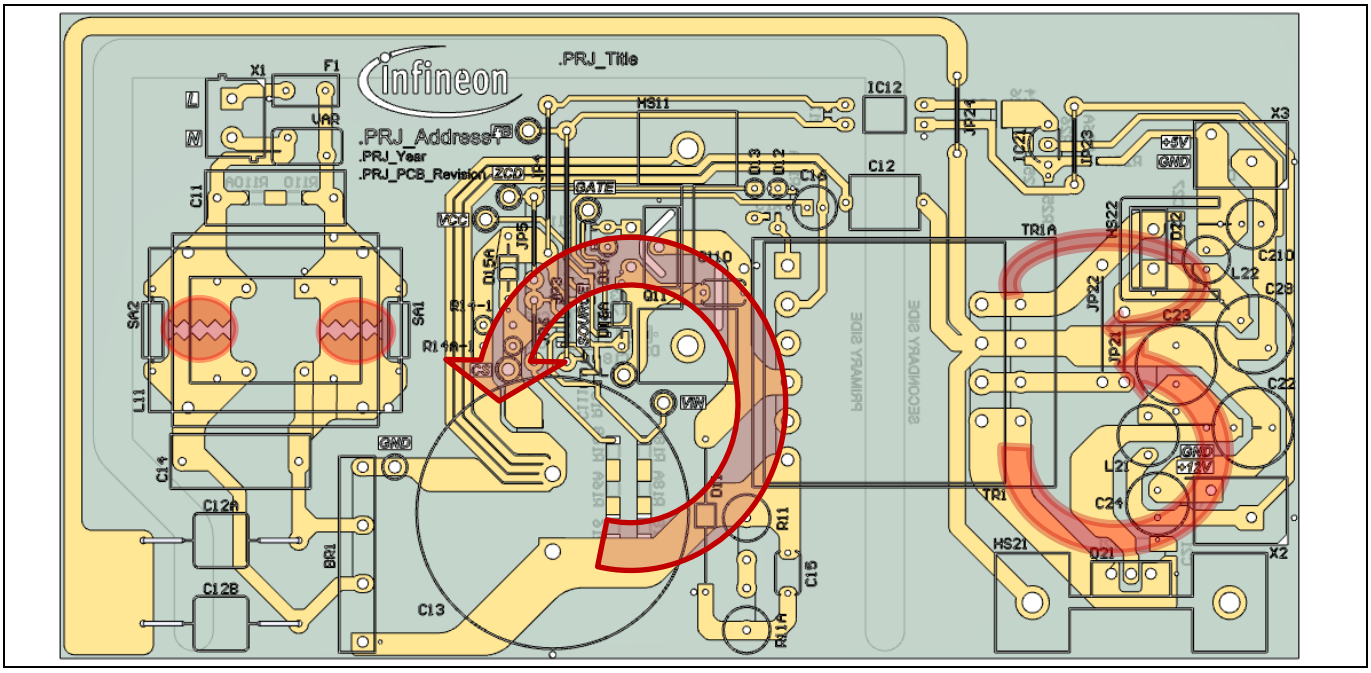


Figure 3 PCB layout tips

- Adding the spark-gap (PCB saw-tooth, 0.5 mm separation) pattern under the input CM choke L11 can increase the system input-line surge capability.
- Separating the HV and LV components e.g. clamper circuit D11, R11, R11A and C15 at the lower part of the PCB (see Figure 3) and the other LV components at the top part of the PCB can reduce the spark-over chance of the high energy surge during ESD or a lightning surge test.

5.7 EMI reduction tips

EMI compliance is always a challenge for the power supply designer. There are several critical points to consider in order to achieve satisfactory EMI performance.

Circuit description

- Good transformer winding coupling is very important. Without this there would be high leakage inductance and a lot of switching spike and HF noise. The most effective method is to adopt sandwich winding (see Figure 8), where the secondary winding is in the middle of the winding and covered by the primary winding on the bottom and top layer. Shielding the transformer can reduce the HF noise. The outermost shield wrapped around the transformer cores with copper foil can help to reduce leakage flux and reduce the noise coupling to nearby components. The inner shield (copper foil or copper wire winding) between the transformer windings can help to reduce the parasitic capacitance and reduce the HF noise coupling. Both shields need to tie to the negative of C13 to achieve the best performance, but note that the inner shield approach would result in more energy loss.
- Use short power-loop design in the PCB (as described in section 5.6) and terminate to the low-ESR capacitor such as C13 for the primary-side loop and C22, C23 and C28 for the secondary-side loops. This can help to reduce the switching ripple, which comes out to the input terminals V_{IN}. In addition, adding a low-ESR ceramic capacitor in parallel to C13/C22/C23/C28 can help to reduce the switching ripple further.
- Sufficient input LC (L11 and C11) filter design is important to pass the EMI requirement. Note that the most effective capacitor is C11, which has the best filtering capability for the switching ripple.
- The Y-capacitor C12 has a function to return the HF noise to the source (negative of C13) and reduce the overall HF noise going out to the input terminals. The larger capacitance is more effective. However, a larger value could introduce a larger leakage current and may fail the safety requirements.

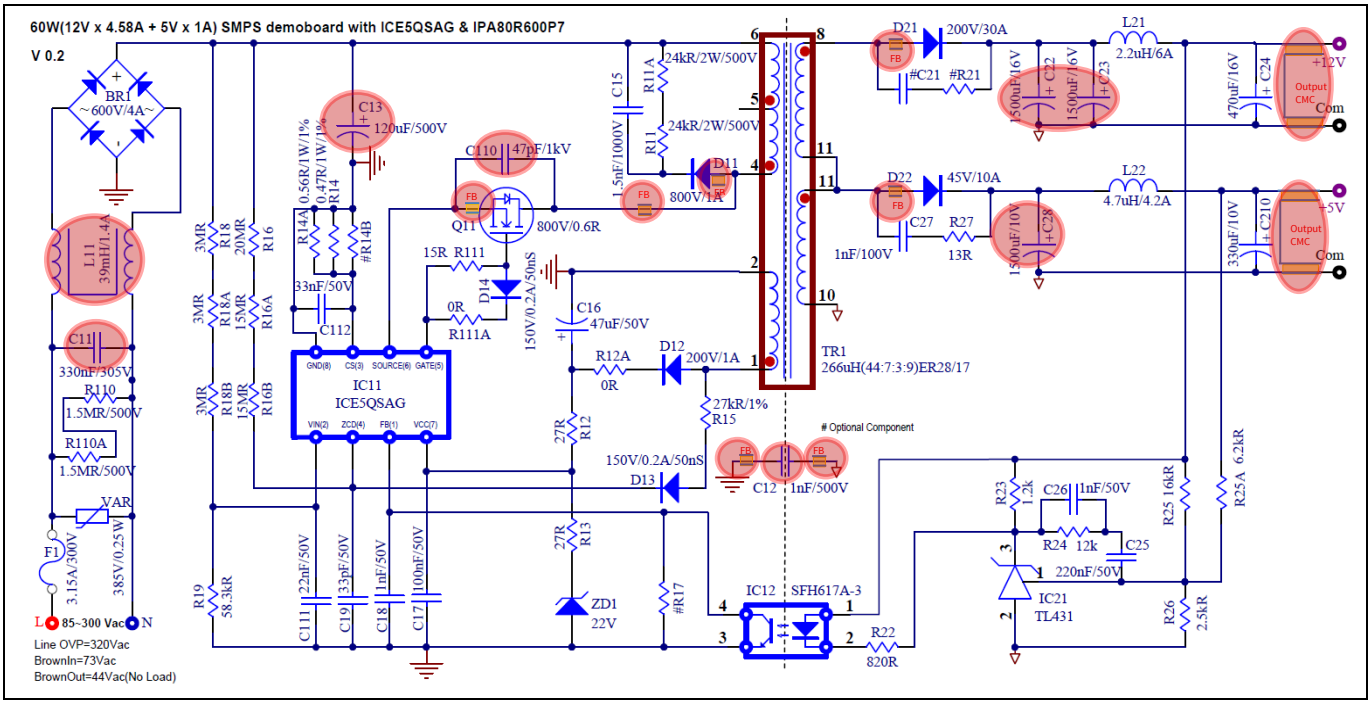


Figure 4 EMI reduction tips

- Adding drain to the CS capacitor C110 for the MOSFET can reduce the high switching noise. However, it also reduces efficiency.
- Adding a ferrite bead to the critical nodes of the circuit can help to reduce the HF noise, such as the connecting path between the transformer and the drain pin, HV MOSFET source pin (Q11), clamper diode D11, output diodes (D21 and D22), Y-capacitor C12, etc.
- Adding an output CM choke can also help to reduce the HF noise.

6 PCB layout

6.1 Top side

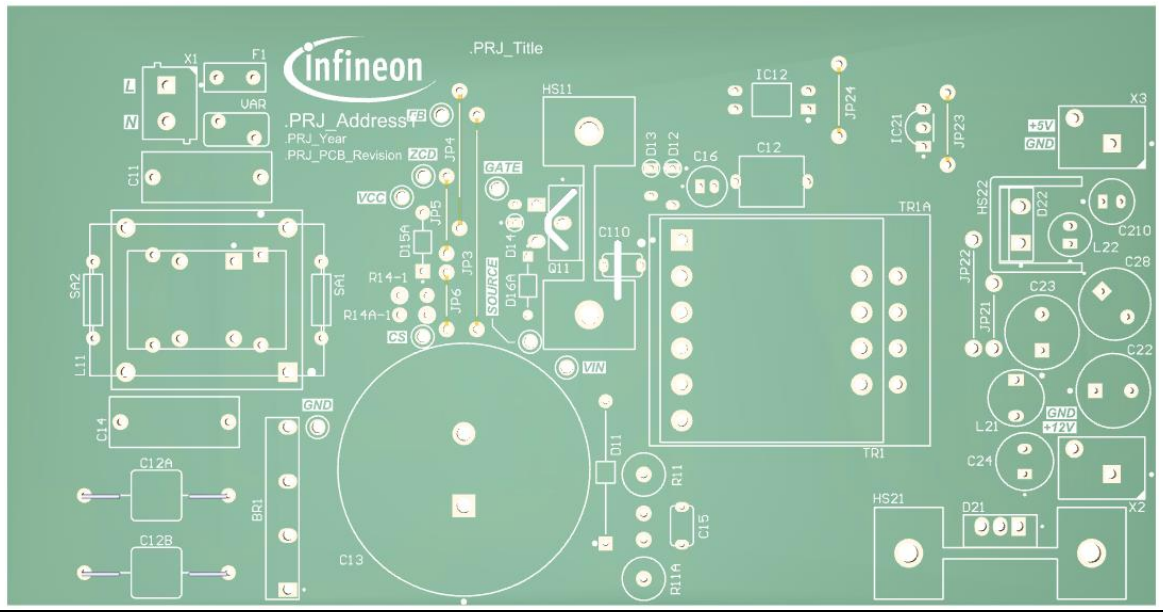


Figure 5 Top-side component legend

6.2 Bottom side

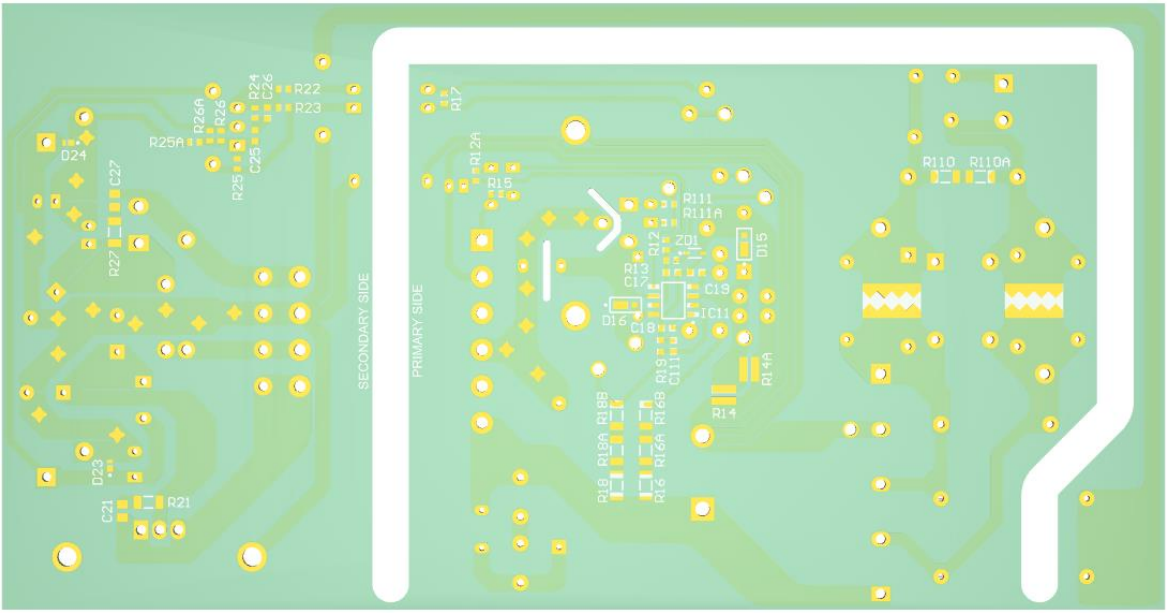


Figure 6 Bottom-side copper and component legend

7 BOM

Table 2 BOM (V 0.2)

No.	Designator	Description	Part number	Manufacturer	Quantity
1	BR1	600 V/4 A	D4SB60L	Shindengen	1
2	C11	0.33 µF/305 V	B32922C3334M000	Epcos	1
3	C12	1 nF/500 V	DE1E3RA102MA4BQ	Murata	1
4	C13	120 µF/500 V	LGN2H121MELB30		1
5	C15	1.5 nF/1000 V	RDE7U3A152J3K1H03	Murata	1
6	C16	47 µF/50 V	35PX47MEFC5X11	Rubycon	1
7	C17	100 nF/50 V	GRM188R71H104KA93D	Murata	1
8	C18, C26	1 nF/50 V	GRM1885C1H102GA01D	Murata	2
9	C19	33 pF/50 V	GRM1885C1H330GA01D	Murata	1
10	C110	47 pF/1000 V	RDE7U3A470J2K1H03	Murata	1
11	C111	22 nF/50 V	GCM188R71H223KA37D	Murata	1
12	C112	33 nF/50 V	GRM188R71H333KA61D	Murata	1
13	C22, C23	1500 uF/16 V	16ZLH1500MEFC10X20	Rubycon	2
14	C24	470 uF/16 V	16ZLH470MEFC8X11.5	Rubycon	1
15	C25	220 nF/50 V	GRM188R71H224KAC4D	Murata	1
16	C27	1 nF/100 V	GRM2162C2A102JA01#	Murata	1
17	C28	1500 uF/10 V	10ZLH1500MEFC10X16	Rubycon	1
18	C210	330 uF/10 V	10ZLH330MEFC6.3X11	Rubycon	1
19	D11	1 A/800 V	UF4006		1
20	D12	1 A/200 V	1N4003-E3/54		1
21	D13, D14	0.2 A/150 V/50 ns	FDH400		1
22	D21	30 A/200 V	VF30200C-E3/4W		1
23	D22	10 A/45 V	VFT1045BP		1
24	F1	3.15 A/300 V	36913150000		1
25	HS11, HS21	Heatsink	513102B02500G		2
26	HS22	Heatsink	577202B00000G		1
27	IC11	ICE5QSAG	ICE5QSAG	Infineon	1
28	IC12	Optocoupler	SFH617A-3		1
29	IC21	Shunt regulator	TL431BVLPG		1
30	JP3, JP4, JP5, JP6, JP23	Jumper			5
31	L11	39 mH/1.4 A	B82734R2142B030	Epcos	1
32	L21	2.2 uH/6 A	744772022	Wurth Electronics	1
33	L22	4.7 uH/4.2 A	7447462047	Wurth Electronics	1
34	Q11	800 V/600 mΩ	IPA80R600P7	Infineon	1
35	R11, R11A	24 kR/2 W/500 V	PR02000202402JR500		2
36	R12, R13	27 Ω	0603 resistor		2
37	R12A, R111A	0 Ω	0603 resistor		2
38	R14	0.47 R/0.75 W/±1 percent	ERJ-B2BFR47V		1
39	R14A	0.56 R/0.75 W/±1 percent	ERJ-B2BFR56V		1
40	R15	27 kΩ/±1 percent	0603 resistor		1
41	R16	20 MR	1206 resistor		1
42	R16A, R16B	15 MR	1206 resistor		2
43	R18, R18A, R18B	3 MR	1206 resistor		3

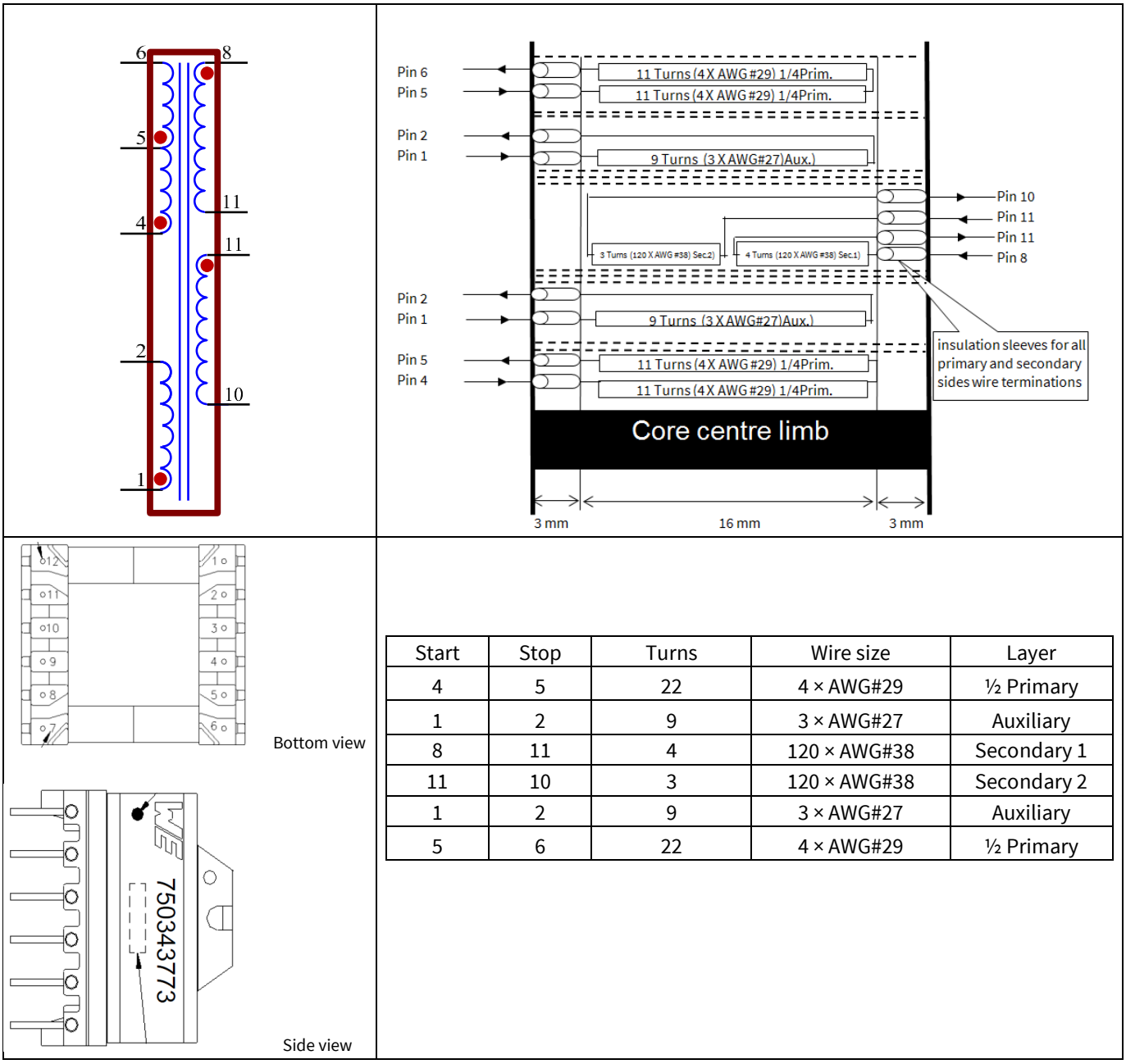
BOM

44	R19	58.3 kR/0.1 W/0.5 percent	RT0603DRE0758K3L		1
45	R110, R110A	1.5 MΩ/500 V	1206 resistor		2
46	R111	15 Ω	0603 resistor		1
47	R22	820 Ω	0603 resistor		1
48	R23	1.2 kΩ	0603 resistor		1
49	R24	12 kΩ	0603 resistor		1
50	R25	16 kΩ	0603 resistor		1
51	R25A	6.2 kΩ	0603 resistor		1
52	R26	2.5 kΩ	0603 resistor		1
53	R27	13 R	1206 resistor		1
54	TR1	266 µH	750343773 (Rev. 02)	Wurth Electronics	1
55	FB, V_{IN}, CS, ZCD, GATE, SOURCE, V_{CC}, GND	Test point	5010		8
56	VAR	0.25 W/385 V	B72207S0381K101	Epcos	1
57	ZD1	22 V	DZ2J220M0L		1
58	Con (L N)	Connector	691102710002	Wurth Electronics	1
59	Con (+12 V com), Con (+5 V com)	Connector	691 412 120 002B	Wurth Electronics	2

8 Transformer specification

(Refer to Appendix A for transformer design and Appendix B for WE transformer specification.)

- Core and materials: ER28/17, TP4A (TDG)
- Bobbin: 070-5652 (12-pin, THT, horizontal version)
- Primary inductance: L_p = 266 µH (±10 percent), measured between pin 4 and pin 6
- Manufacturer and part number: Wurth Electronics Midcom (750343773) Rev 0.2



Start	Stop	Turns	Wire size	Layer
4	5	22	4 × AWG#29	½ Primary
1	2	9	3 × AWG#27	Auxiliary
8	11	4	120 × AWG#38	Secondary 1
11	10	3	120 × AWG#38	Secondary 2
1	2	9	3 × AWG#27	Auxiliary
5	6	22	4 × AWG#29	½ Primary

Figure 7 Transformer structure

9 Measurement data and graphs

Table 3 Measurement data

Input (V AC/Hz)	Description	P_{IN} (W)	V_{OUT2} (V DC)	I_{OUT2} (A)	V_{OUT1} (V DC)	I_{OUT1} (A)	P_{OUT} (W)	η (percent)	η_{avg} (percent)	P_{IN_OLP} (W)	I_{OUT1_OLP} (A) (Fixed 5 V at 1 A)
85/60	No load	0.05	4.96	0.000	12.04	0.000				85.00	5.30
	Min. load	0.10	4.79	0.006	12.50	0.001	0.04	44.42			
	1/20 load	3.60	4.97	0.050	12.04	0.228	2.99	83.16			
	1/10 load	7.16	4.97	0.100	12.03	0.458	6.00	83.86			
	1/4 load	17.90	4.97	0.250	12.03	1.148	15.05	84.06	82.45		
	Typ. load	36.23	4.96	0.500	12.04	2.297	30.13	83.17			
	3/4 load	54.69	4.96	0.750	12.03	3.435	45.04	82.36			
	Max. load	75.00	4.96	1.000	12.05	4.580	60.15	80.20			
115/60	No load	0.06	4.97	0.000	12.03	0.000				95.60	6.23
	Min. load	0.11	4.79	0.006	12.49	0.001	0.04	38.82			
	1/20 load	3.59	4.97	0.050	12.03	0.228	2.99	83.32			
	1/10 load	7.15	4.97	0.100	12.03	0.458	6.00	83.98			
	1/4 load	17.74	4.97	0.250	12.02	1.148	15.04	84.75	84.27		
	Typ. load	35.61	4.96	0.500	12.03	2.297	30.11	84.56			
	3/4 load	53.29	4.96	0.750	12.02	3.435	45.01	84.46			
	Max. load	72.16	4.96	1.000	12.04	4.580	60.10	83.29			
230/50	No load	0.08	4.97	0.000	12.02	0.000				100.20	6.60
	Min. load	0.14	4.79	0.006	12.49	0.001	0.04	30.10			
	1/20 load	3.71	4.97	0.050	12.02	0.228	2.99	80.57			
	1/10 load	7.33	4.97	0.100	12.02	0.458	6.00	81.85			
	1/4 load	17.97	4.97	0.250	12.01	1.148	15.02	83.61	84.81		
	Typ. load	35.37	4.97	0.500	12.01	2.297	30.07	85.01			
	3/4 load	52.65	4.97	0.750	12.01	3.435	44.98	85.44			
	Max. load	70.44	4.96	1.000	12.02	4.580	60.01	85.20			
265/50	No load	0.10	4.97	0.000	12.02	0.000				103.00	6.90
	Min. load	0.15	4.79	0.006	12.49	0.001	0.04	27.42			
	1/20 load	3.75	4.97	0.050	12.02	0.228	2.99	79.71			
	1/10 load	7.41	4.97	0.100	12.02	0.458	6.00	80.97			
	1/4 load	18.15	4.97	0.250	12.01	1.148	15.02	82.78	84.46		
	Typ. load	35.52	4.97	0.500	12.01	2.297	30.07	84.66			
	3/4 load	52.81	4.97	0.750	12.01	3.435	44.98	85.18			
	Max. load	70.42	4.96	1.000	12.02	4.580	60.01	85.22			
300/50	No load	0.11	4.97	0.000	12.02	0.000				105.00	7.10
	Min. load	0.17	4.79	0.006	12.49	0.001	0.04	24.22			
	1/20 load	3.82	4.97	0.050	12.02	0.228	2.99	78.25			
	1/10 load	7.50	4.97	0.100	12.01	0.458	6.00	79.94			
	1/4 load	18.35	4.97	0.250	12.01	1.148	15.02	81.87	83.98		
	Typ. load	35.71	4.97	0.500	12.01	2.297	30.07	84.20			
	3/4 load	53.03	4.97	0.750	12.01	3.435	44.98	84.82			
	Max. load	70.54	4.97	1.000	12.01	4.580	59.98	85.02			

Measurement data and graphs

- No-load condition (no load) : 5 V at 0 A and 12 V at 0 A
- Minimum load condition (min. load) : 5 V at 6 mA and 12 V at 1m A
- 1/20 load condition (1/20 load) : 5 V at 50 mA and 12 V at 229 mA
- 1/10 load condition (1/10 load) : 5 V at 100 mA and 12 V at 458 mA
- 1/4 load condition (1/4 load) : 5 V at 250 mA and 12 V at 1.145 A
- Typical load condition (typ. load) : 5 V at 500 mA and 12 V at 2.290 A
- 3/4 load condition (3/4 load) : 5 V at 750 mA and 12 V at 3.435 A
- Maximum load condition (max. load) : 5 V at 1000 mA and 12 V at 4.58 A

9.1 Load regulation

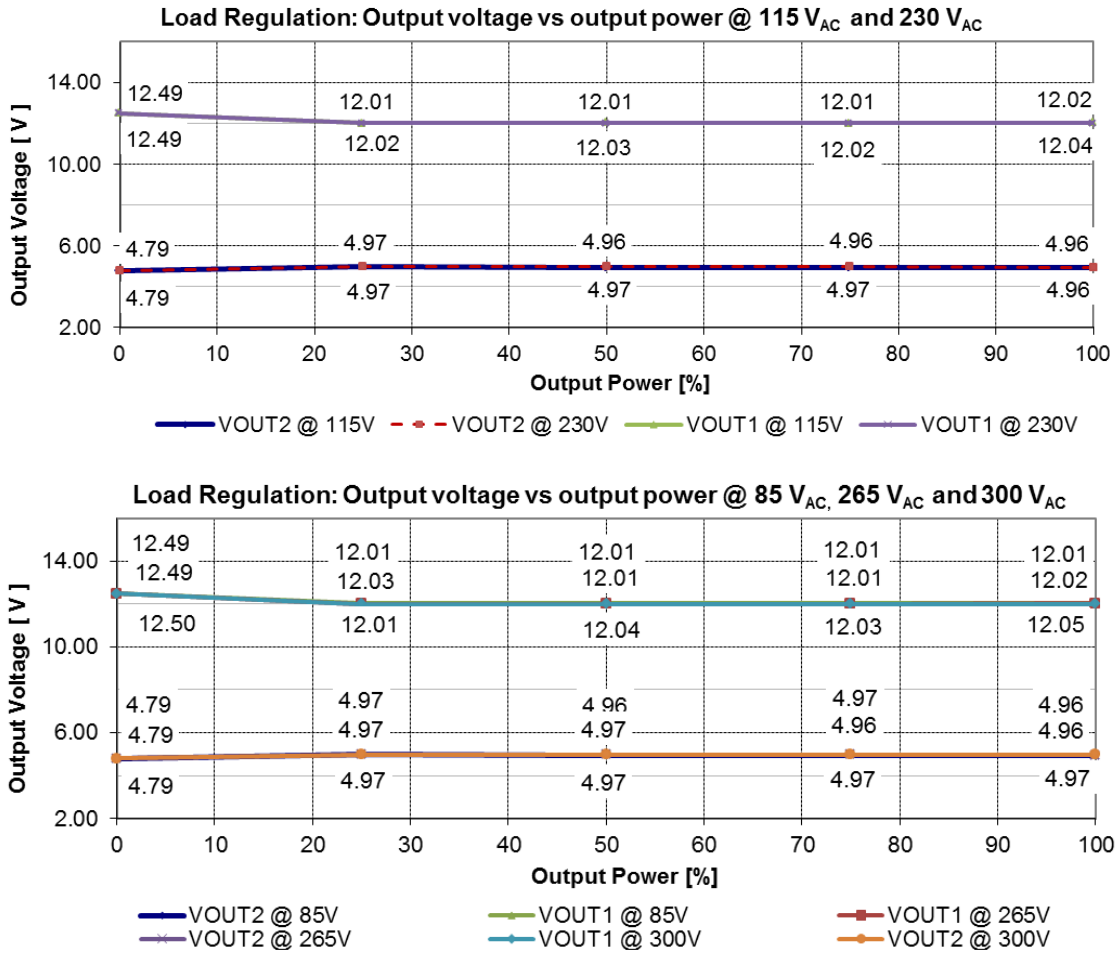


Figure 8 Load regulation V_{OUT} vs output power

9.2 Line regulation

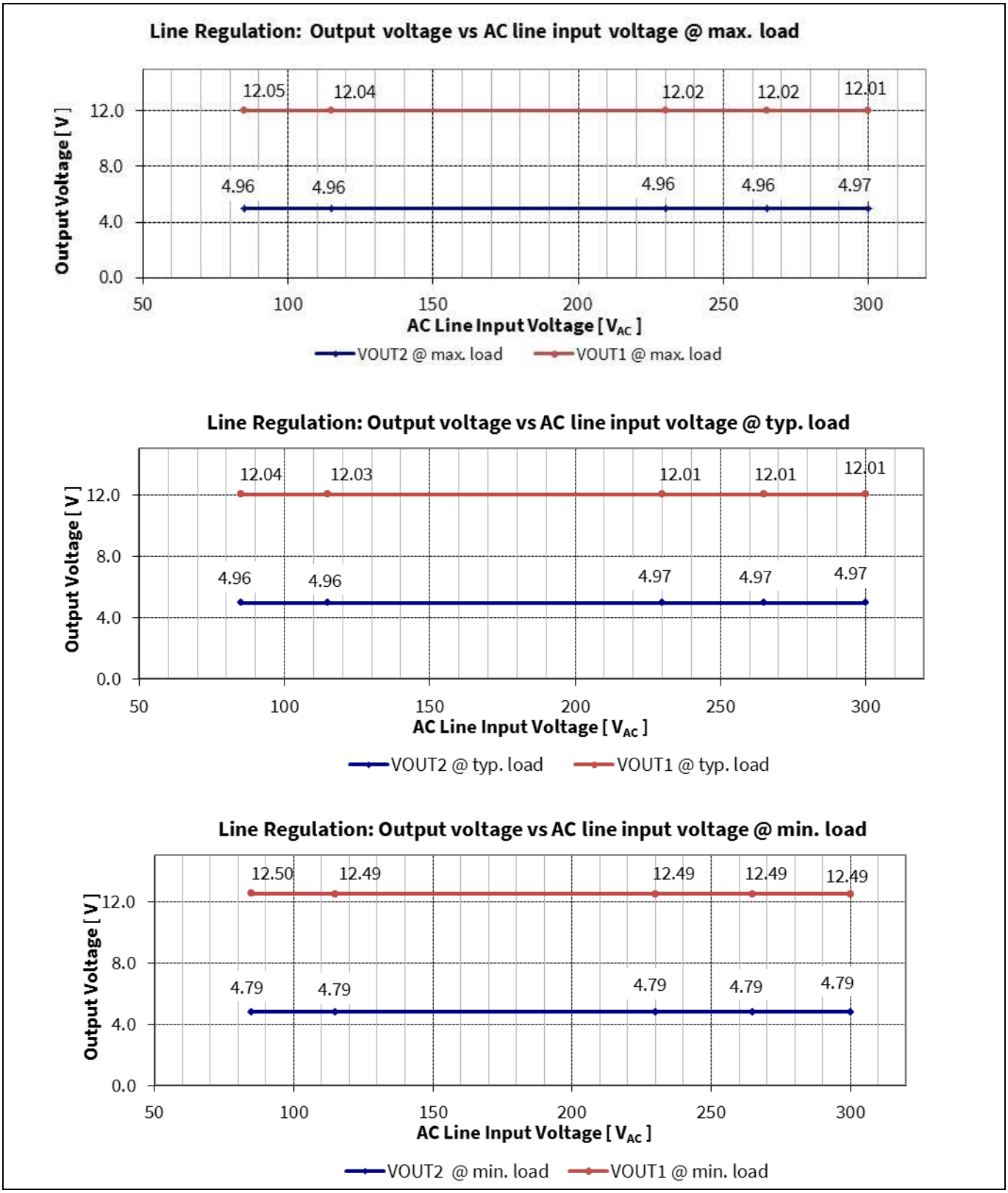


Figure 9 Line regulation: V_{OUT} vs AC-line input voltage

9.3 Efficiency vs AC-line input voltage

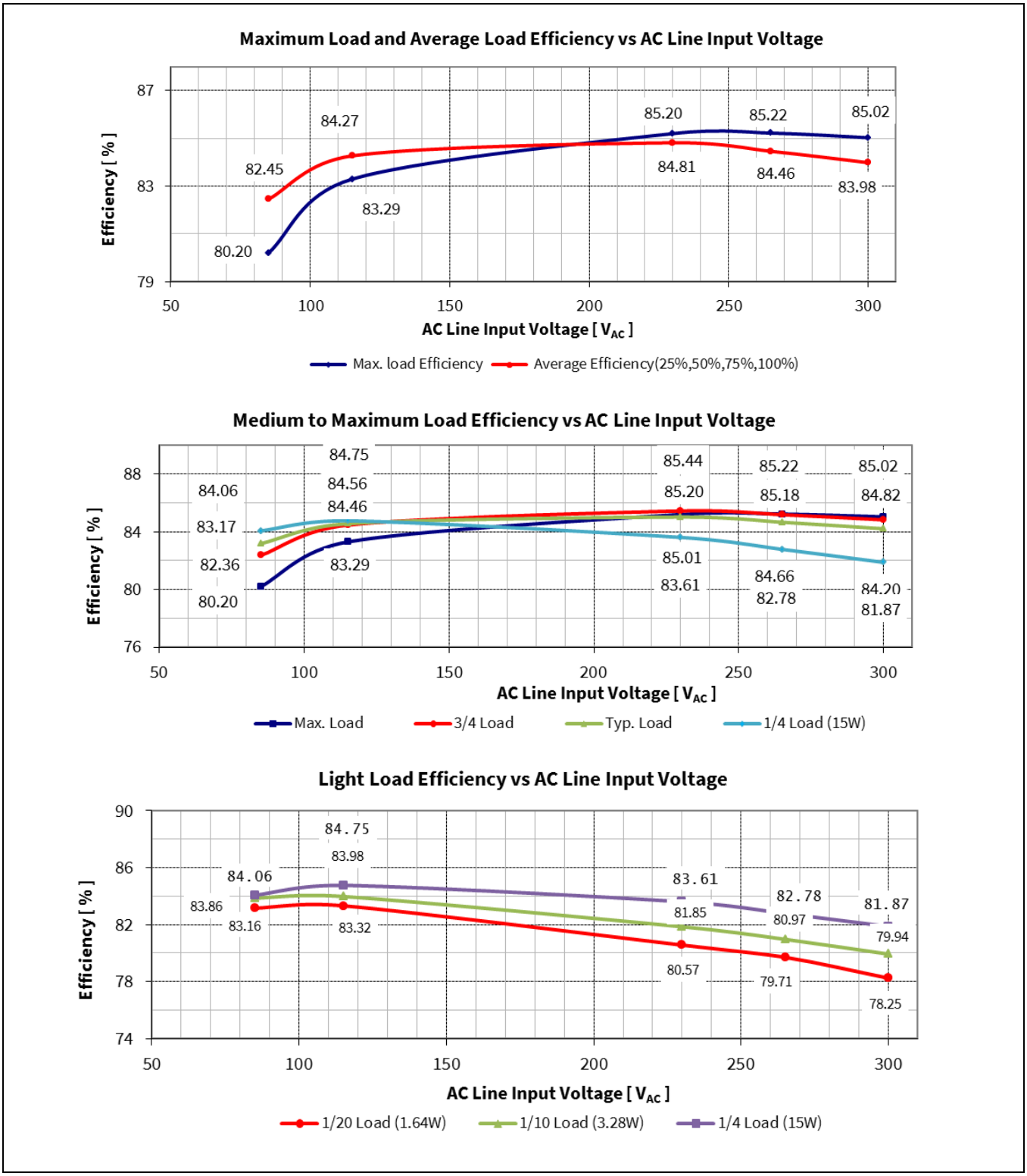


Figure 10 Efficiency vs AC-line input voltage

9.4 Standby power

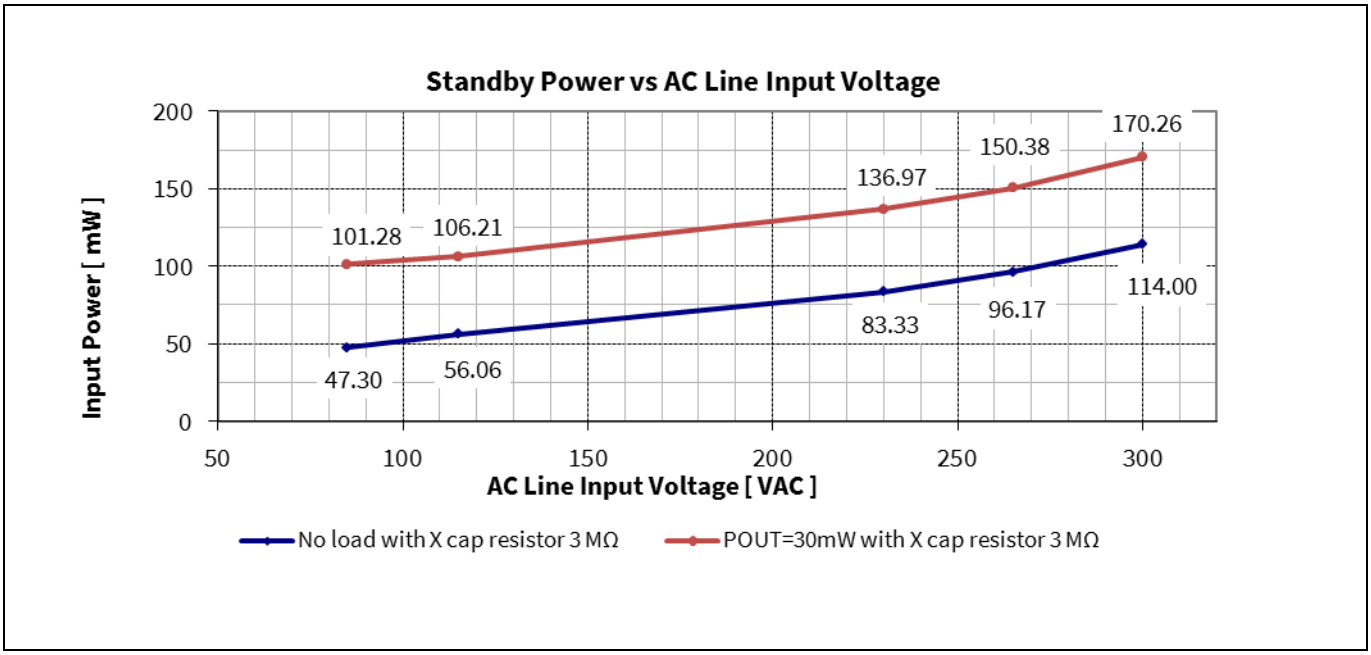


Figure 11 **Standby power at no load (P_{stby_NL}) and 30 mW load (P_{stby_ML}) vs AC-line input voltage (measured by Yokogawa WT210 power meter – integration mode)**

9.5 Maximum input power

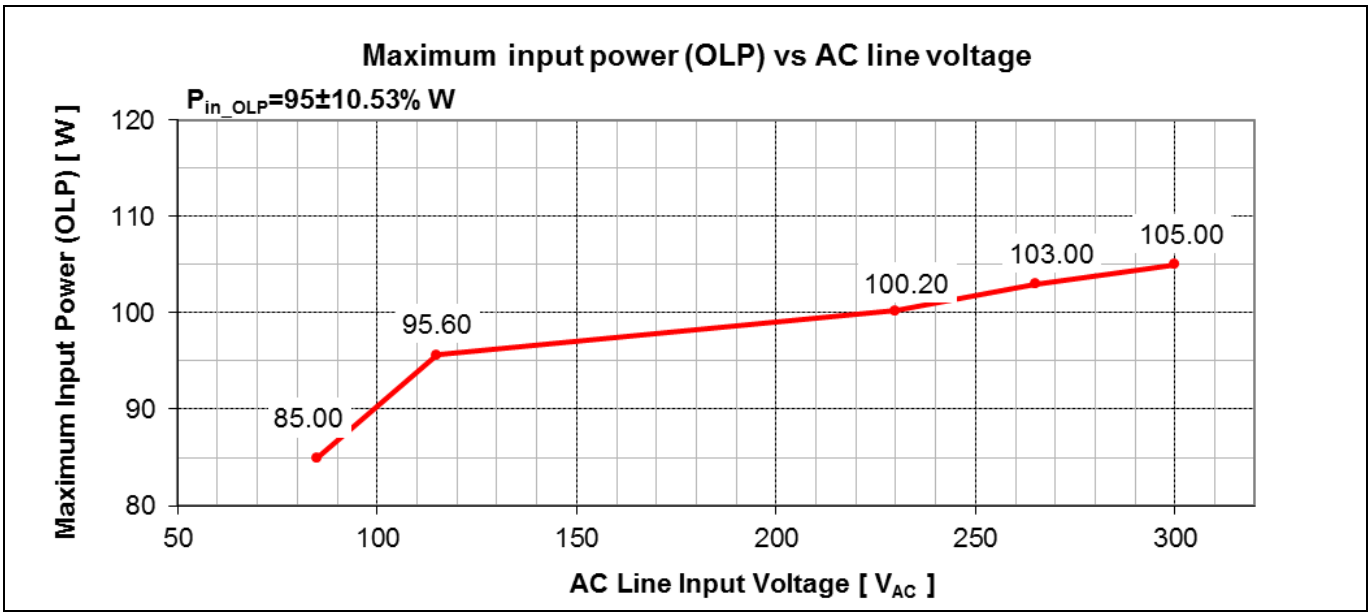


Figure 12 **Maximum input power (before over-load protection) vs AC-line input voltage**

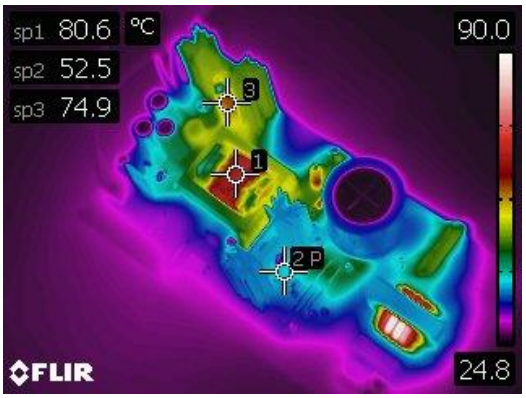
10 Thermal measurement

The thermal testing of the demo board was done in the open air without forced ventilation, at an ambient temperature of 25°C. An infrared thermography camera (FLIR-T62101) was used to capture the thermal reading of particular components. The measurements were taken at the maximum load running for one hour. The tested input voltage was 85 V AC and 300 V AC.

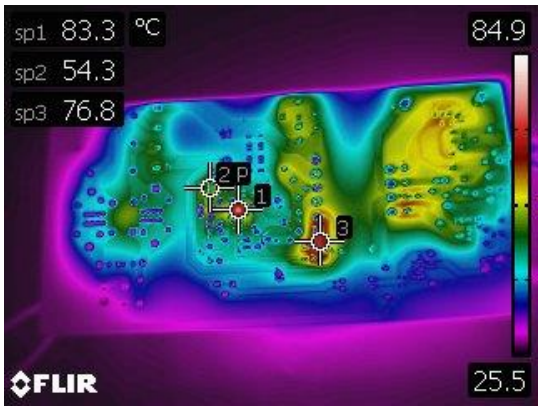
Table 4 Component temperature at full load (12 V at 4.58 A and 5 V at 1 A) under T_{amb} = 25°C

Circuit code	Major component	85 V AC (°C)	300 V AC (°C)
IC11	ICE5QSAG	83.3	47.2
Q11	IPA80R600P7	52.5	52.7
R14	CS resistor	54.3	38.2
TR1	Transformer	80.6	82.2
BR1	Bridge diode	64.2	32.2
R11	Clamper resistor	72.4	71.5
L11	Input CM choke	90.0	39.9
D21	+12 V output diode	74.9	80.3
D22	+5 V output diode	51.9	53.3
	Ambient	25.0	25.0

85 V AC maximum load and 25°C ambient

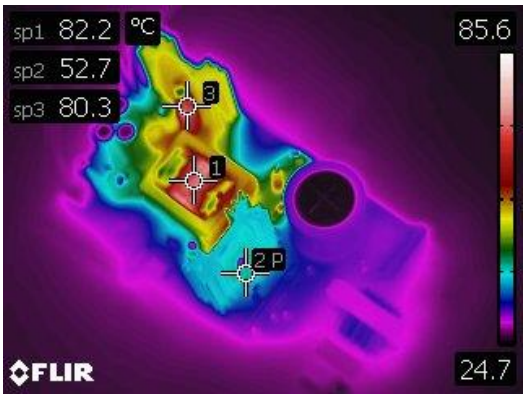


Top side

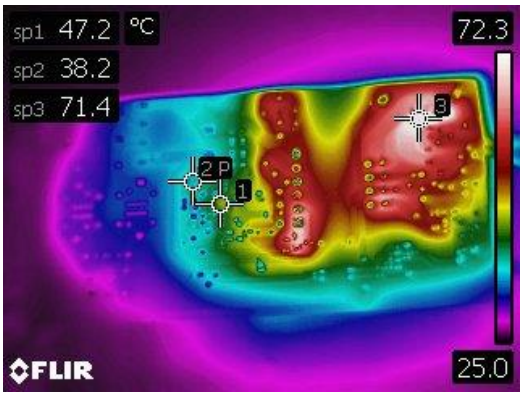


Bottom side

300 V AC maximum load and 25°C ambient



Top side



Bottom side

Figure 13 Infrared thermal image of DEMO_5QSAG_60W1

11 Waveforms

All waveforms and scope plots were recorded with a Teledyne LeCroy 606Zi oscilloscope.

11.1 Start-up at low/high AC-line input voltage with maximum load

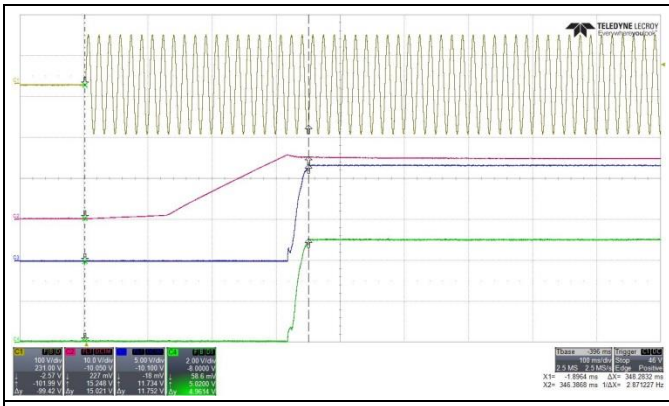
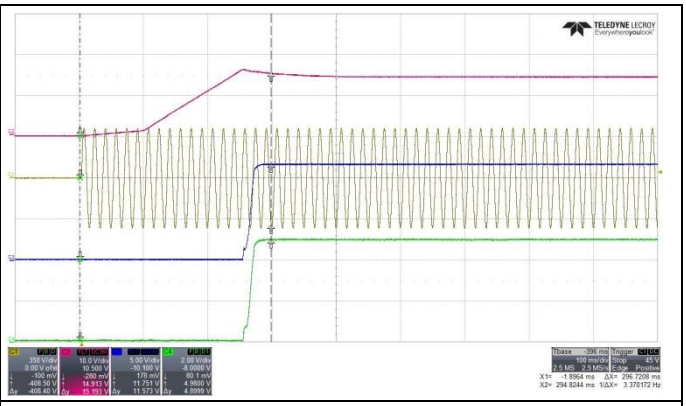
	
C1 (yellow): V AC; C2 (purple): V_{VCC}; C3 (blue): V_{OUT1} (12 V); C4 (green): V_{OUT2} (5 V)	C1 (yellow): V AC; C2 (purple): V_{VCC}; C3 (blue): V_{OUT1} (12 V); C4 (green): V_{OUT2} (5 V)
V_{IN} = 85 V AC, max. load; start-up time: ≈350 ms	V_{IN} = 300 V AC, max. load; start-up time: ≈300 ms

Figure 14 Start-up

11.2 Soft-start

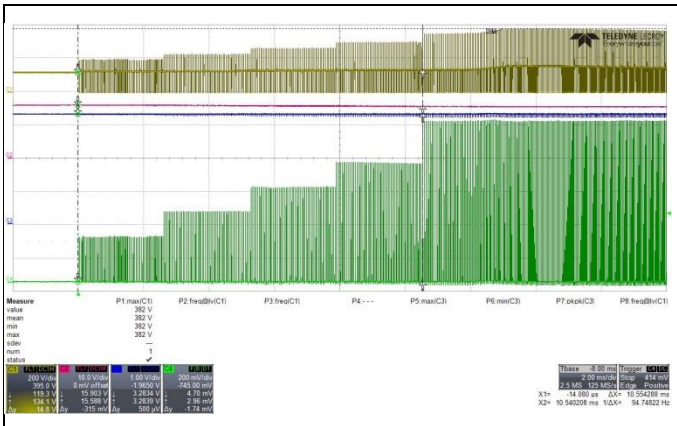
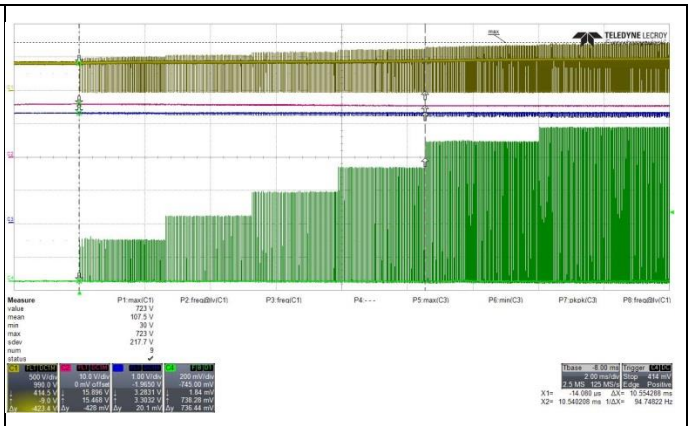
	
C1 (yellow): V_{Drain}; C2 (purple): V_{VCC}; C3 (blue): V_{FB}; C4 (green): V_{CS}	C1 (yellow): V_{Drain}; C2 (purple): V_{VCC}; C3 (blue): V_{FB}; C4 (green): V_{CS}
V_{IN} = 85 V AC, max. load; soft-start time: ≈11 ms	V_{IN} = 300 V AC, max. load; soft-start time: ≈11 ms

Figure 15 Soft-start

11.3 Switching waveform at maximum load

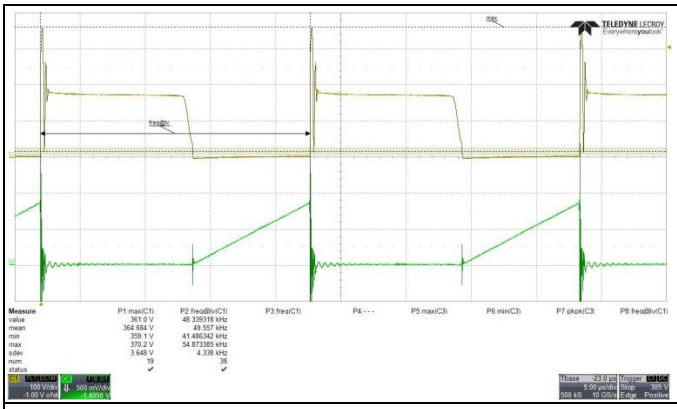
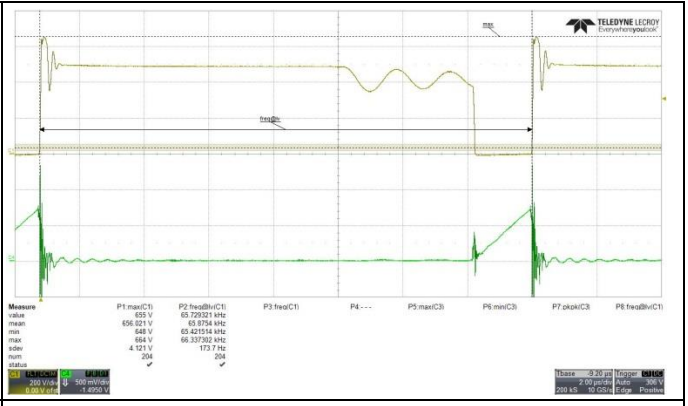
	
C1 (yellow): V_{Drain}; C4 (green): V_{CS}	C1 (yellow): V_{Drain}; C4 (green): V_{CS}
V_{IN} = 85 V AC, max. load; V_{Drain_peak}: 370 V DC and f_{S_Min}: 41 kHz; first ZC is measured	V_{IN} = 300 V AC, max. load; V_{Drain_peak}: 664 V DC and f_{S_Min}: 65 kHz; third ZC is measured

Figure 16 Drain and CS voltage at maximum load

11.4 Switching waveform at 25 percent load

- 25 percent load (5 V at 0.25 A and 12 V at 1.145 A)

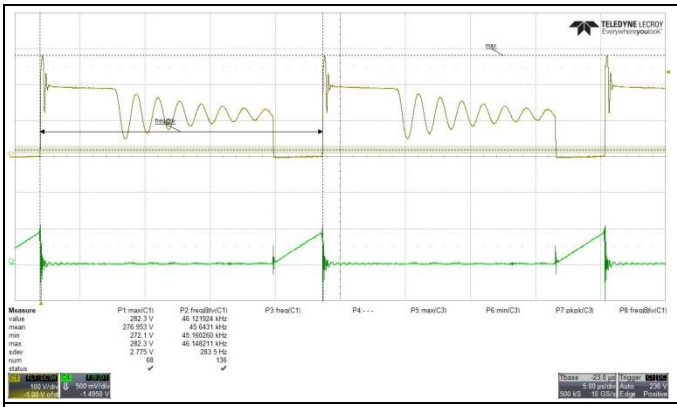
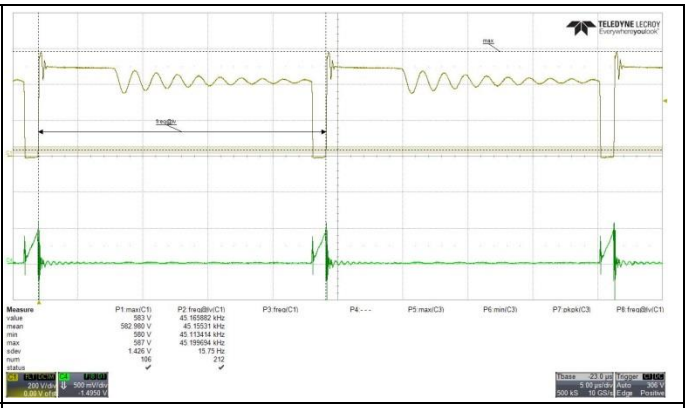
	
C1 (yellow): V_{Drain}; C4 (green): V_{CS}	C1 (yellow): V_{Drain}; C4 (green): V_{CS}
V_{IN} = 85 V AC, 25 percent load; eighth ZC is measured (highest ZC at low-line)	V_{IN} = 300 V AC, 25 percent load; tenth ZC is measured (highest ZC at high-line)

Figure 17 Drain and CS voltage at 25 percent load

11.5 Output ripple voltage at maximum load

- Probe terminal end with decoupling capacitor of 0.1 µF (ceramic) and 1 µF (electrolytic), 20 MHz BW

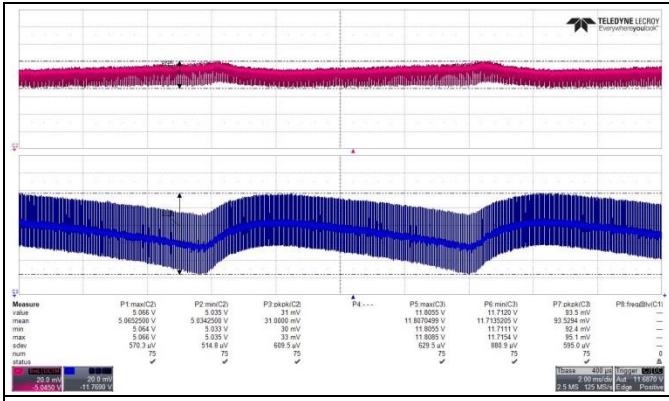
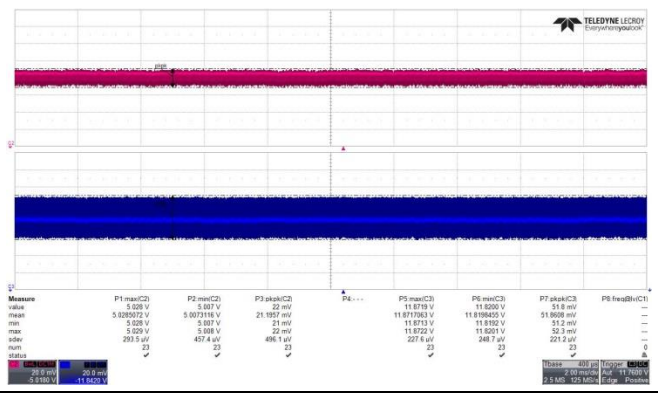
	
C2 (purple): $V_{RIPPLE2}$ (5 V); C3 (blue): $V_{RIPPLE1}$ (12 V)	C2 (purple): $V_{RIPPLE2}$ (5 V); C3 (blue): $V_{RIPPLE1}$ (12 V)
V_{IN} = 85 V AC, max. load; $V_{RIPPLE2}$ (5 V): 33 mV; $V_{RIPPLE2}$ (12 V): 96 mV	V_{IN} = 300 V AC, max. load; $V_{RIPPLE2}$ (5 V): 22 mV; $V_{RIPPLE2}$ (12 V): 53 mV

Figure 18 Output ripple voltage at maximum load

11.6 Output ripple voltage in ABM 1 W load

- Probe terminal end with decoupling capacitor of 0.1 µF (ceramic) and 1 µF (electrolytic), 20 MHz BW
- Load: 1 W (5 V at 6 mA and 12 V at 80 mA)

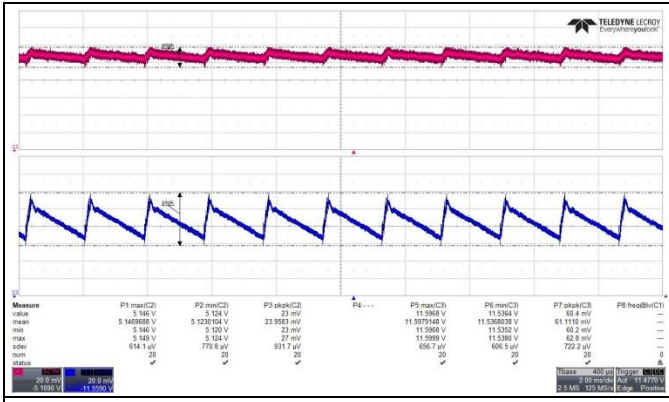
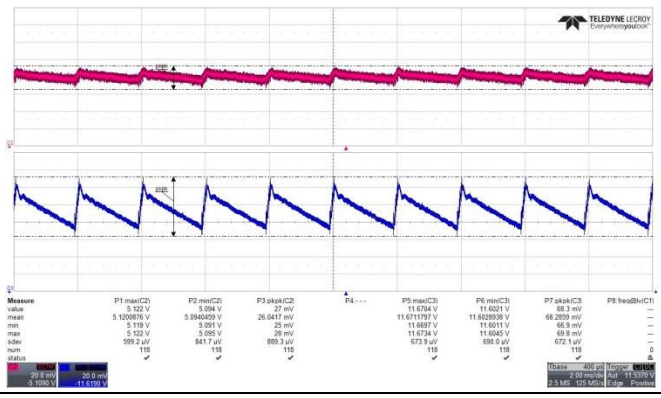
	
C2 (purple): $V_{RIPPLE2}$ (5 V); C3 (blue): $V_{RIPPLE1}$ (12 V)	C2 (purple): $V_{RIPPLE2}$ (5 V); C3 (blue): $V_{RIPPLE1}$ (12 V)
V_{IN} = 85 V AC, 1 W load; $V_{RIPPLE2}$ (5 V): 27 mV; $V_{RIPPLE2}$ (12 V): 63 mV	V_{IN} = 300 V AC, 1 W load; $V_{RIPPLE2}$ (5 V): 28 mV; $V_{RIPPLE2}$ (12 V): 70 mV

Figure 19 Output ripple voltage in ABM 1 W load

11.7 Load transient response (dynamic load from 10 percent to 100 percent)

- Probe terminal end with decoupling capacitor of 0.1 µF (ceramic) and 1 µF (electrolytic), 20 MHz BW
- 12 V load change from 10 percent to 100 percent and 5 V at 200 mA load, 100 Hz, 0.4 A/µs slew rate

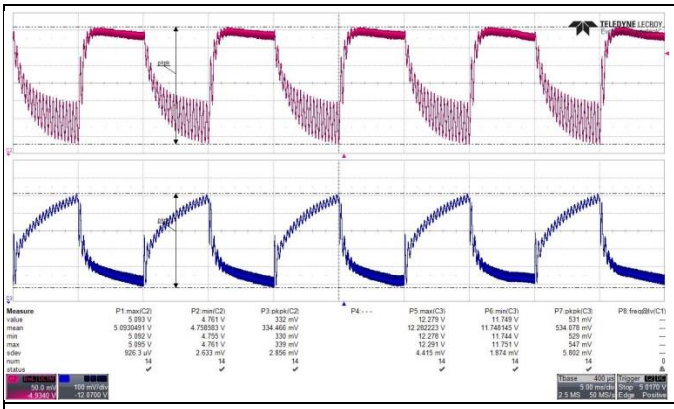
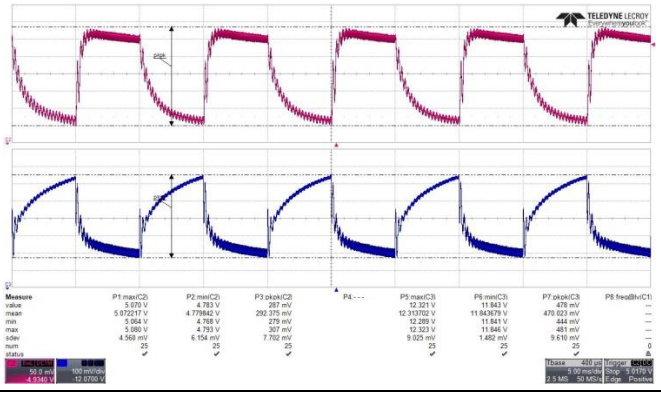
	
C2 (purple): $V_{RIPPLE2}$ (5 V); C3 (blue): $V_{RIPPLE1}$ (12 V)	C2 (purple): $V_{RIPPLE2}$ (5 V); C3 (blue): $V_{RIPPLE1}$ (12 V)
V_{IN} = 85 V AC, 10 percent to 100 percent load; $V_{RIPPLE2}$ (5 V): 340 mV; $V_{RIPPLE2}$ (12 V): 550 mV	V_{IN} = 300 V AC, 10 percent to 100 percent load; $V_{RIPPLE2}$ (5 V); 310 mV; $V_{RIPPLE2}$ (12 V): 450 mV

Figure 20 Load transient response

11.8 Entering ABM

- Load change from 11.5 W (5 V at 60 mA and 12 V at 0.9375 A) to 1.5 W (5 V at 60 mA and 12 V at 0.1 A)

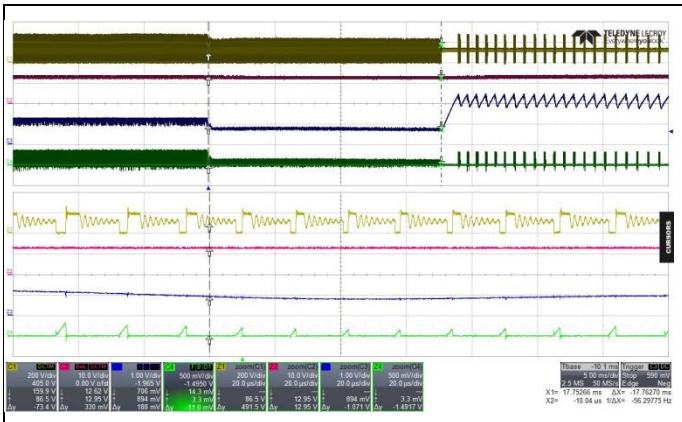
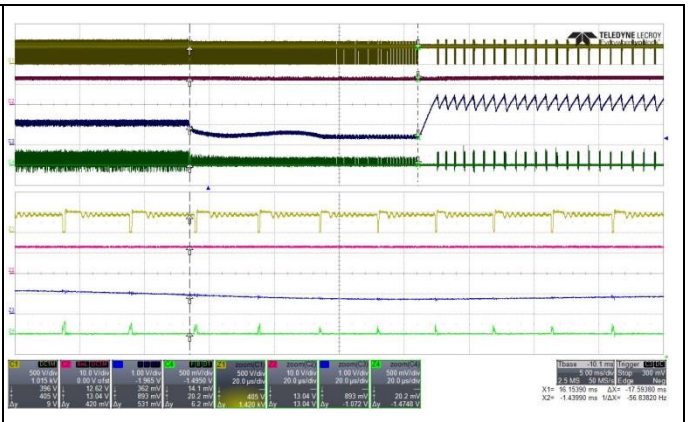
	
C1 (yellow): V_{Drain}; C2 (purple): V_{VCC}; C3 (blue): V_{FB}; C4 (green): V_{CS}	C1 (yellow): V_{Drain}; C2 (purple): V_{VCC}; C3 (blue): V_{FB}; C4 (green): V_{CS}
V_{IN} = 85 V AC; system enters burst mode level 1: V_{FB} < 0.9 V, N_{ZC} = 8 and $t_{blanking}$ = 20 ms	V_{IN} = 85 V AC; system enters burst mode level 1: V_{FB} < 0.9 V, N_{ZC} = 10 and $t_{blanking}$ = 20 ms

Figure 21 Entering ABM

11.9 During ABM

- Load: 1.5 W (5 V at 60 mA and 12 V at 0.1 A)

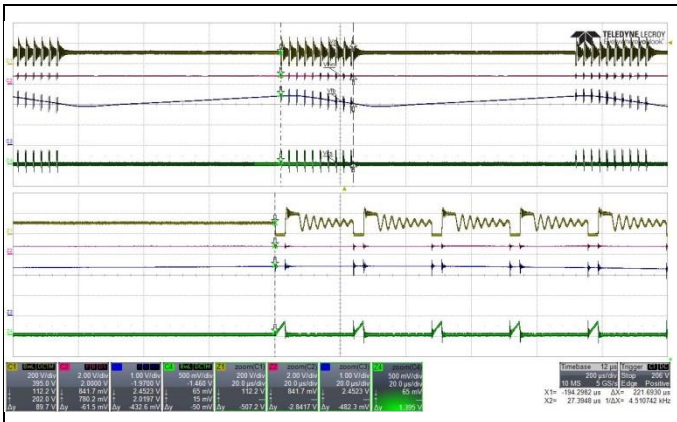
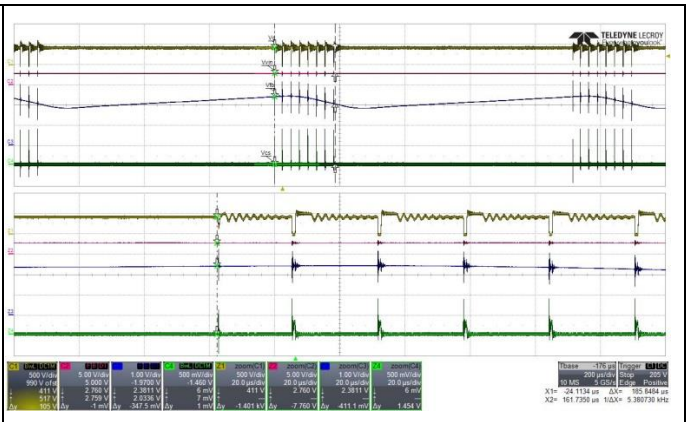
	
C1 (yellow): V_{Drain}; C2 (purple): V_{VCC}; C3 (blue): V_{FB}; C4 (green): V_{CS}	C1 (yellow): V_{Drain}; C2 (purple): V_{VCC}; C3 (blue): V_{FB}; C4 (green): V_{CS}
V_{IN} = 85 V AC; burst mode level 1: V_{FB_BOn} = 2.4 V, V_{FB_BOff} = 2.0 V, V_{CSBLP} = 0.31 V, N_{ZC} = 8	V_{IN} = 300 V AC; burst mode level 1: V_{FB_BOn} =2.4 V, V_{FB_BOff} = 2.0 V, V_{CSBLP} = 0.31 V, N_{ZC} = 10

Figure 22 During ABM

11.10 Leaving ABM

- Load change from 1.5 W (5 V at 60 mA and 12 V at 0.1 A) at 85 V AC to full load

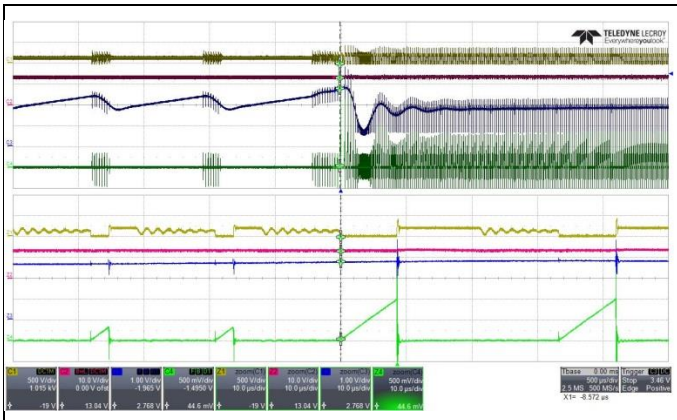
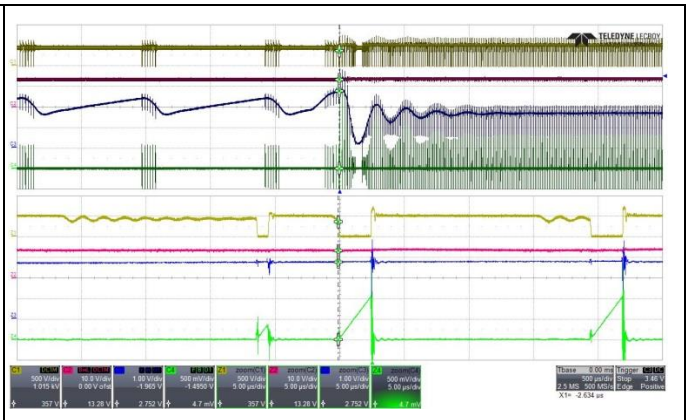
	
C1 (yellow): V_{Drain}; C2 (purple): V_{VCC}; C3 (blue): V_{FB}; C4 (green): V_{CS}	C1 (yellow): V_{Drain}; C2 (purple): V_{VCC}; C3 (blue): V_{FB}; C4 (green): V_{CS}
V_{IN} = 85 V AC; system leaves burst mode: V_{FB} > 2.75 V	V_{IN} = 300 V AC; system leaves burst mode: V_{FB} > 2.75 V

Figure 23 Leaving ABM

11.11 Line OVP (non-switch auto restart)

- Increase AC-line voltage gradually at maximum load until line OVP is detected and then decrease the AC-line until line OVP reset detected

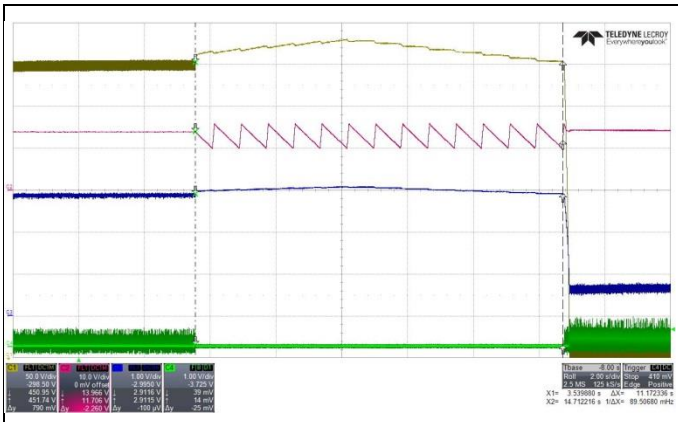
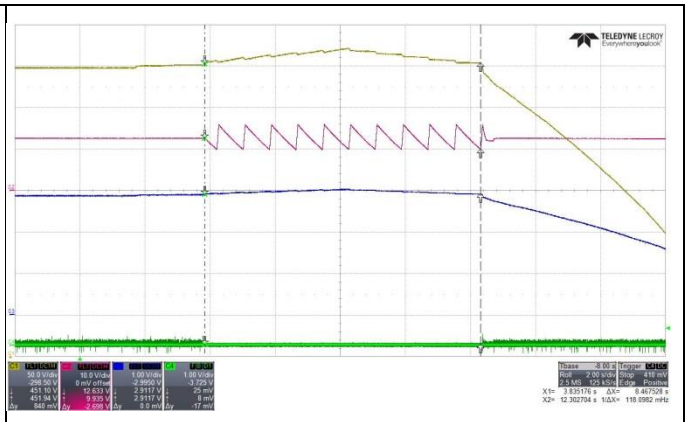
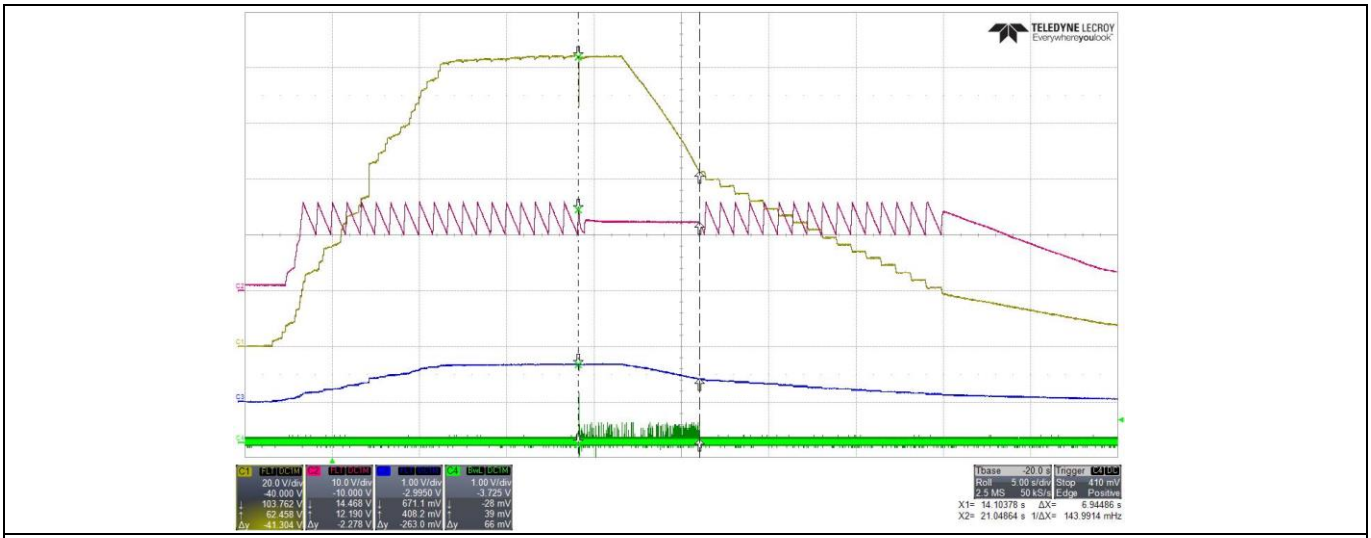
	
C1 (yellow): V_{Bus}; C2 (purple): V_{VCC}; C3 (blue): V_{VIN}; C4 (green): V_{CS}	C1 (yellow): V_{Bus}; C2 (purple): V_{VCC}; C3 (blue): V_{VIN}; C4 (green): V_{CS}
Max. load; line OVP triggered: 320 V AC (V_{Bus} > 451 V DC or V_{VIN} > 2.9 V); line OVP reset: 320 V AC (V_{Bus} < 451 V DC or V_{VIN} < 2.9 V)	1 W load; line OVP triggered: 320 V AC (V_{Bus} > 451 V DC or V_{VIN} > 2.9 V); line OVP reset: 320 V AC (V_{Bus} < 451 V DC or V_{VIN} < 2.9 V)

Figure 24 Line OVP

11.12 Brown-in/brown-out protection (non-switch auto restart)

- Increase AC-line voltage gradually at 1 W load (5 V at 6 mA) until the system starts up (brown-in) and then reduce the AC-line until the system shut-down (brown-out)



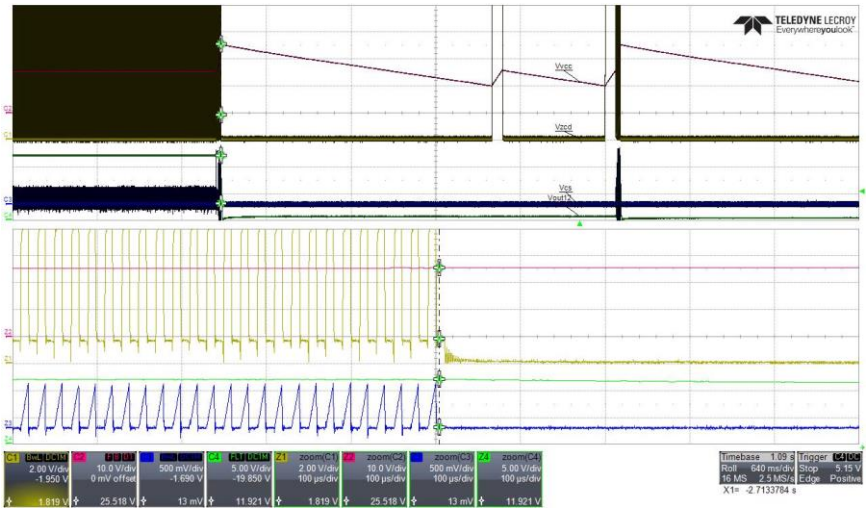
C1 (yellow): V_{Bus}; C2 (purple): V_{VCC}; C3 (blue): V_{VIN}; C4 (green): V_{CS}

30 mW load; brown-in: 73 V AC (V_{Bus} > 103 V DC or V_{VIN} > 0.66 V); brown-out: 44 V AC (V_{Bus} < 62 V DC or V_{VIN} < 0.4 V)

Figure 25 Brown-in/brown-out protection

11.13 V_{CC} OVP (odd-skip auto restart)

- Change D13 to 1N485B and short R26 resistor during system operation at no load



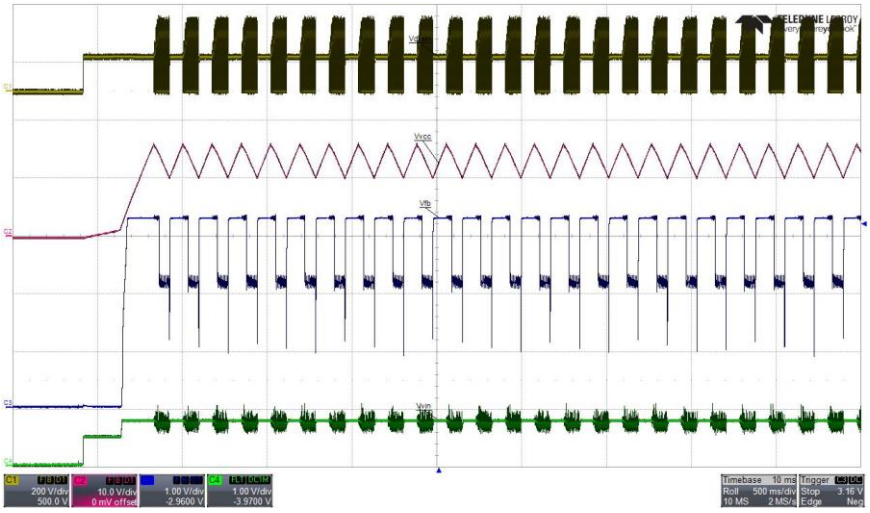
C1 (yellow): V_{ZCD}; C2 (purple): V_{VCC}; C3 (blue): V_{OUT1} (12 V); C4 (green): V_{CS}

V_{IN} = 85 V AC; system enters V_{CC} OVP: V_{CC} > 25.5 V

Figure 26 V_{CC} OVP

11.14 V_{CC} UVP (auto restart)

- Remove R12A and power on the system with full load



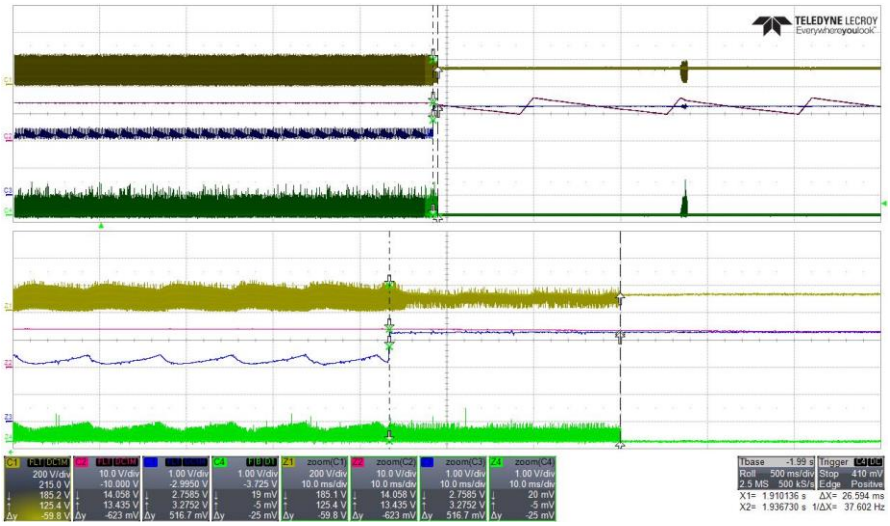
C1 (yellow): V_{Drain}; C2 (purple): V_{VCC}; C3 (blue): V_{FB}; C4 (green): V_{CS}

V_{IN} = 85 V AC; system enters V_{CC} UV protection: V_{CC} < 10 V

Figure 27 V_{CC} UVP

11.15 Over-load protection (odd-skip auto restart)

- V_{OUT1} (12 V) short-to-GND at 85 V AC



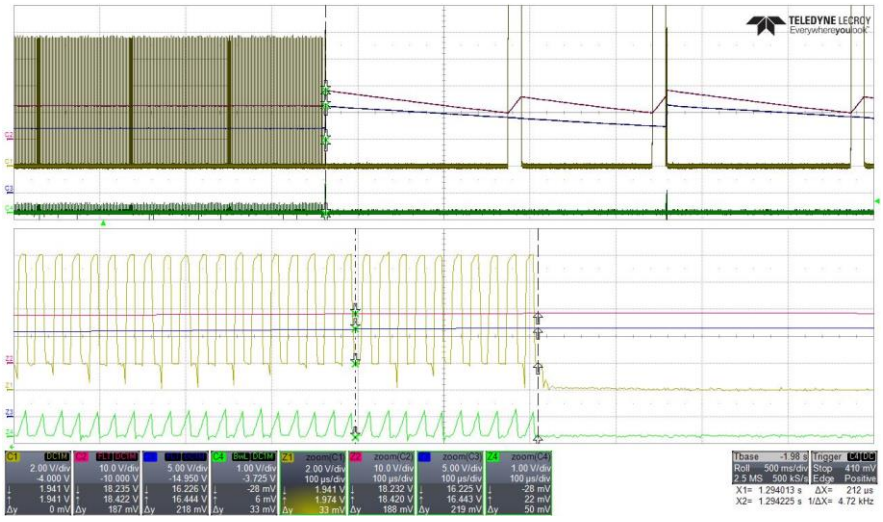
C1 (yellow): V_{Drain}; C2 (purple): V_{VCC}; C3 (blue): V_{FB}; C4 (green): V_{CS}

V_{IN} = 85 V AC; system enters OLP: V_{FB} > 2.75 V and last for ≈27 ms blanking time

Figure 28 Over-load protection (OLP)

11.16 Output OVP (odd-skip auto restart)

- Short resistor R26 during system operation at 30 mW load



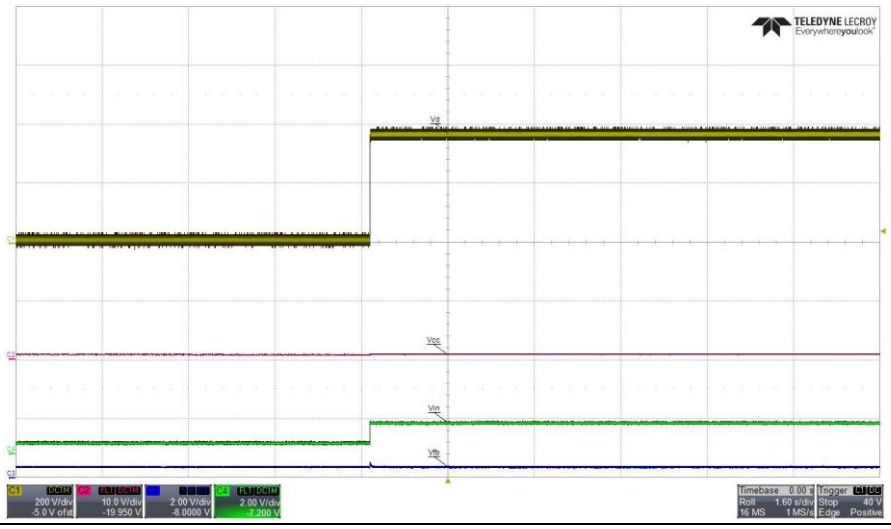
C1 (yellow): V_{ZCD}; C2 (purple): V_{VCC}; C3 (blue): V_{OUT1} (12 V); C4 (green): V_{CS}

V_{IN} = 85 V AC; system enters output OV: V_{ZCD} > 2 V and lasts for 10 consecutive pulses

Figure 29 Output OVP

11.17 V_{CC} short-to-GND protection

- Short V_{CC} pin-to-GND before system start-up



C1 (yellow): V_{Drain}; C2 (purple): V_{VCC}; C3 (blue): V_{FB}; C4 (green): V_{VIN}

V_{IN} = 300 V AC; system enters V_{CC} short-to-GND: $V_{CC} < V_{VCC_SCP}$ → I_{VCC} = 513 µA (input power is ≈ 350 mW)

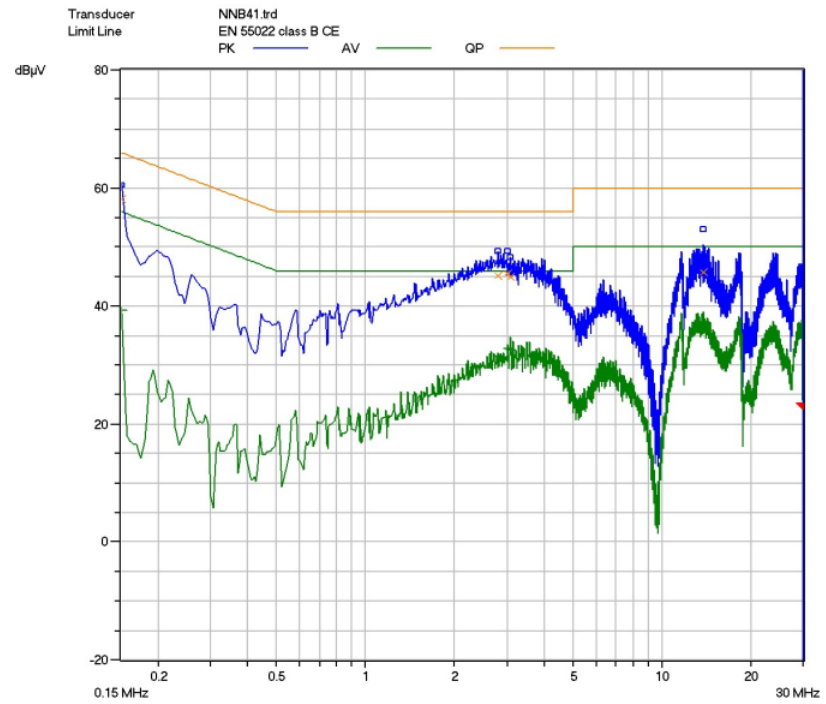
Figure 30 V_{CC} short-to-GND protection

11.18 Conducted emissions (EN 55022 class B)

Equipment: Schaffner SMR4503 (receiver); standard: EN 55022 (CISPR 22) class B; test conditions: V_{IN} = 115 V AC and 230 V AC, load: 60 W (12 V at 2.61 Ω and 5 V at 5 Ω).

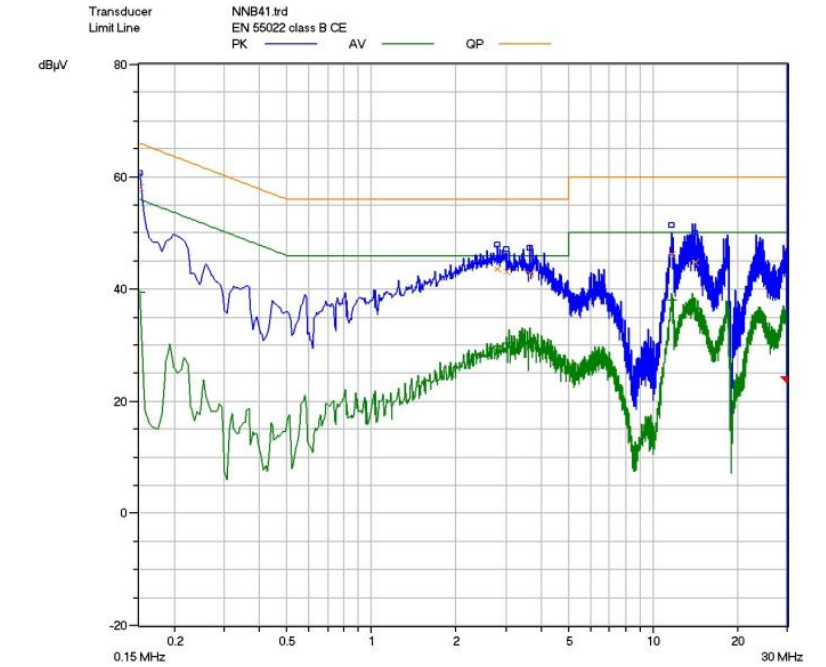
- Pass conducted emissions EN 55022 (CISPR 22) class B with greater than 7 dB margin for quasi-peak measurement at low-line (115 V AC) and approximately 6 dB margin for average measurement at high-line (230 V AC).

Waveforms



Frequency		Level Pk		Level AV		Level QP	Limit AV	Limit QP
0.1500	L	60.5	L	39.3	L	58.1	56.0	66.0
2.7900	L	49.4	L	31.5	L	45.2	46.0	56.0
3.0000	L	49.4	L	32.8	L	45.5	46.0	56.0
3.0720	L	48.3	L	32.5	L	45.0	46.0	56.0
13.8080	L	53.0	L	37.2	L	45.8	50.0	60.0

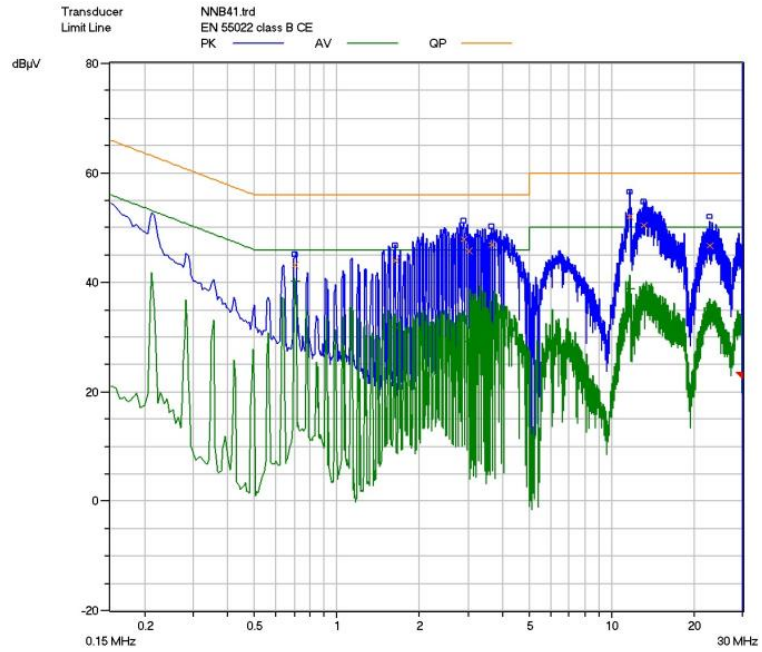
Figure 31 Conducted emissions at 115 V AC-line and 60 W load – > 7 dB margin



Frequency		Level Pk		Level AV		Level QP	Limit AV	Limit QP
0.1500	N	60.7	N	39.5	N	58.1	56.0	66.0
2.7900	N	48.0	N	29.8	N	43.7	46.0	56.0
3.0000	N	47.2	N	30.4	N	43.3	46.0	56.0
3.6640	N	47.4	N	30.4	N	42.8	46.0	56.0
11.6880	N	51.5	N	38.0	N	46.2	50.0	60.0
14.0240	N	50.1	N	36.5	N	44.7	50.0	60.0

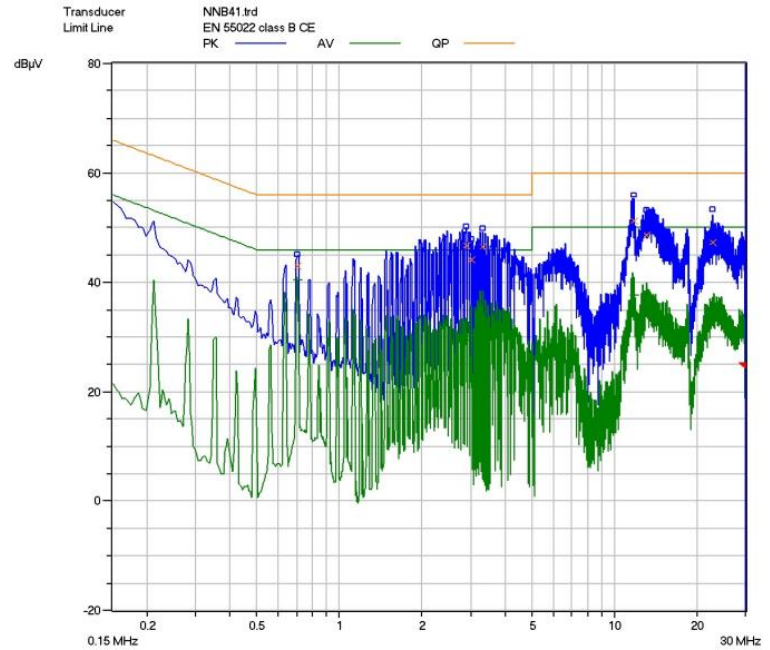
Figure 32 Conducted emissions at 115 V AC neutral and 60 W load – > 7 dB margin

Waveforms



Frequency		Level Pk		Level AV		Level QP	Limit AV	Limit QP
0.7020	L	45.1	L	40.0	L	43.2	46.0	56.0
1.6260	L	46.8	L	31.7	L	44.0	46.0	56.0
2.8980	L	51.2	L	33.6	L	47.9	46.0	56.0
3.0000	L	48.1	L	29.2	L	45.8	46.0	56.0
3.6560	L	50.3	L	32.3	L	47.0	46.0	56.0
11.6640	L	56.5	L	38.9	L	52.0	50.0	60.0
13.0720	L	54.8	L	36.7	L	50.4	50.0	60.0
22.8160	L	52.1	L	35.3	L	46.8	50.0	60.0

Figure 33 Conducted emissions at 230 V AC-line and 60 W load – ≈ 6 dB margin



Frequency		Level Pk		Level AV		Level QP	Limit AV	Limit QP
0.7020	N	45.2	N	40.0	N	43.1	46.0	56.0
2.8980	N	50.2	N	29.4	N	46.8	46.0	56.0
3.0000	N	47.9	N	30.2	N	44.3	46.0	56.0
3.3120	N	50.0	N	32.6	N	46.4	46.0	56.0
11.7360	N	55.9	N	37.7	N	51.3	50.0	60.0
13.0480	N	53.2	N	36.1	N	48.7	50.0	60.0
22.8080	N	53.4	N	34.8	N	47.4	50.0	60.0

Figure 34 Conducted emissions at 230 V AC neutral and 60 W load – ≈ 6 dB margin

11.19 ESD immunity (EN 61000-4-2)

This system was subjected to a ±10 kV ESD test according to EN 61000-4-2 for both contact and air discharge. A test failure was defined as non-recoverable.

- Air discharge: pass ±10 kV; contact discharge: pass ± 10 kV

Table 5 System ESD test result

Description	ESD test	Level	Number of strikes				Test result
			$+V_{OUT1}$	$-V_{OUT1}$	$+V_{OUT2}$	$-V_{OUT2}$	
115 V AC at 60 W (12 V at 2.61 Ω and 5 V at 5 Ω)	Contact	+10 kV	10	10	10	10	PASS
		-10 kV	10	10	10	10	PASS
	Air	+10 kV	10	10	10	10	PASS
		-10 kV	10	10	10	10	PASS
230 V AC at 60 W (12 V at 2.61 Ω and 5 V at 5 Ω)	Contact	+10 kV	10	10	10	10	PASS
		-10 kV	10	10	10	10	PASS
	Air	+10 kV	10	10	10	10	PASS
		-10 kV	10	10	10	10	PASS

11.20 Surge immunity (EN 61000-4-5)

This system was subjected to a surge immunity test (±2 kV DM and ±4 kV CM) according to EN 61000-4-5. A test failure was defined as a non-recoverable.

- DM: pass ±2 kV; CM: pass ±4 kV

Table 6 System surge immunity test result

Description	Surge test	Level		Number of strikes				Test result
				0°	90°	180°	270°	
115 V AC at 60 W (12 V at 2.61 Ω and 5 V at 5 Ω)	DM	+2 kV	L → N	3	3	3	3	PASS[1]
		-2 kV	L → N	3	3	3	3	PASS[1]
	CM	+4 kV	L → G	3	3	3	3	PASS[1]
		+4 kV	N → G	3	3	3	3	PASS[1]
		-4 kV	L → G	3	3	3	3	PASS[1]
		-4 kV	N → G	3	3	3	3	PASS[1]
230 V AC at 60 W (12 V at 2.61 Ω and 5 V at 5 Ω)	DM	+2 kV	L → N	3	3	3	3	PASS[1]
		-2 kV	L → N	3	3	3	3	PASS[1]
	CM	+4 kV	L → G	3	3	3	3	PASS[1]
		+4 kV	N → G	3	3	3	3	PASS[1]
		-4 kV	L → G	3	3	3	3	PASS[1]
		-4 kV	N → G	3	3	3	3	PASS[1]

[1] PCB spark-gap distance needs to reduce to 0.5 mm.

12 Appendix: WE transformer specification

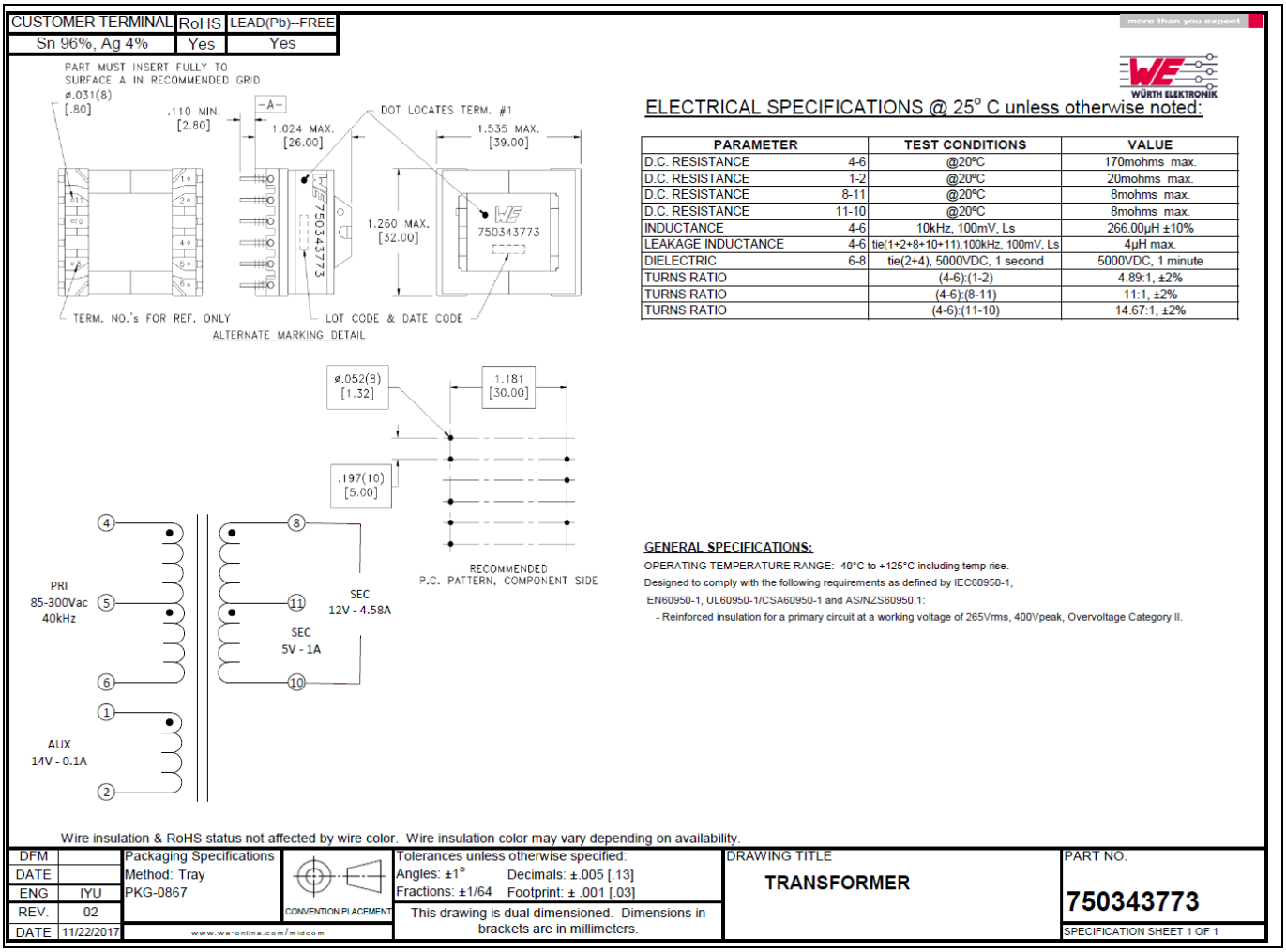


Figure 35 WE transformer specification

13 References

[1] ICE5QSAG datasheet, Infineon Technologies AG

[2] IPA80R600P7 datasheet, Infineon Technologies AG

[3] AN-201609_PL83_026-5th-Generation Quasi-Resonant Design Guide

[4] Calculation Tool Quasi-Resonant CoolSET™ Generation 5

Revision history

Document version	Date of release	Description of changes
V1.0	16 November 2017	First release

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