Energy buffer circuit for hold-up extension and grid current shaping in AI data centers and servers

REF_12KW_HFHD_PSU (Energy Buffer)

About this document

Scope and purpose

This document introduces a solution of an auxiliary circuit, also called an energy buffer (EB), which is part of a power supply unit (PSU) (see Figure 1) addressing AI data center and server applications. This circuit could be considered independent of the power supply, as it can be connected to the DC bus of any converter with similar purpose. The topology of this auxiliary circuit, and more specifically the operation and the configuration for the AI data centers and server applications, is patented by Infineon Technologies under the patents [1] and [2]

Intended audience

The document is intended for R&D engineers, hardware designers, and developers of power electronic systems. Figure 1 shows the complete reference design REF_12KW_HFHD_PSU of the PSU [3].

Figure 1 Reference design of the REF_12KW_HFHD_PSU power supply unit

Key points

- Explains an auxiliary energy buffer circuit for hold-up extension and grid-current shaping in AI data center PSUs
- Describes bidirectional buck-boost topology enabling energy storage and release during transient events like line cycle drop-out (LCDO)and load jumps
- Demonstrates reduced bulk capacitance and improved PSU power density by minimizing electrolytic capacitors
- Provides control scheme ensuring stable DC-link voltage and reliable operation under startup, voltage sag, and overload conditions
- Highlights benefits of grid slew-rate limitation and enhanced transient response for AI workload profiles

About this product family

Product family

Infineon's 12 kW high-density PSU reference design combines Si, SiC, and GaN technologies to deliver exceptional efficiency and power density. Ideal for AI data center and server power racks, it supports machine learning accelerators and compute-intensive applications.

Target applications

- AI data centers
- High-performance server power racks
- Compute-intensive workloads with rapid load transients
- Cloud infrastructure requiring grid-current shaping and hold-up compliance
- Large-scale GPU clusters for machine learning and training tasks

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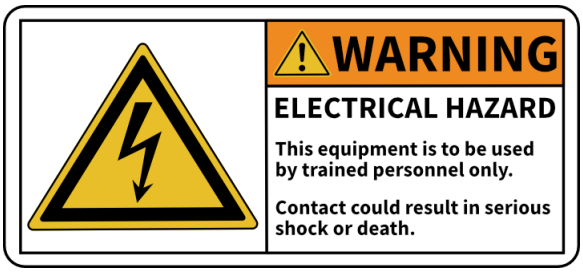
Safety information

Please read this document carefully before starting up the device.



Important notice

Evaluation boards, demonstration boards, reference boards and kits are electronic devices typically provided as an open-frame and unenclosed printed circuit board (PCB) assembly. Each board is functionally qualified by electrical engineers and strictly intended for use in development laboratory environments. Any other use and/or application is strictly prohibited. Our boards and kits are solely for qualified and professional users who have training, expertise, and knowledge of electrical safety risks in the development and application of high-voltage electrical circuits. Please note that evaluation boards, demonstration boards, reference boards and kits are provided “as is” (i.e., without warranty of any kind). Infineon is not responsible for any damage resulting from the use of its evaluation boards, demonstration boards, reference boards or kits. To make our boards as versatile as possible, and to give you (the user) opportunity for the greatest degree of customization, the virtual design data may contain different component values than those specified in the bill of materials (BOM). In this specific case, the BOM data has been used for production. Before operating the board (i.e. applying a power source), please read the application note/user guide carefully and follow the safety instructions. Please check the board for any physical damage, which may have occurred during transport. If you find damaged components or defects on the board, do not connect it to a power source. Contact your supplier for further support. If no damage or defects are found, start the board up as described in the user guide or test report. If you observe unusual operating behavior during the evaluation process, immediately shut off the power supply to the board and consult your supplier for support.

Operating instructions

Do not touch the device during operation, keep a safe distance. Do not touch the device after disconnecting the power supply, as several components may still store electric charge and can discharge through physical contact. Several parts, like heatsinks and transformers, may still be very hot. Allow the components to discharge and cool before touching or servicing. All work such as construction, verification, commissioning, operation, measurements, adaptations, and other work on the device (applicable national accident prevention rules must be observed) must be done by trained personnel. The electrical installation must be completed in accordance with the appropriate safety requirements.

Safety precautions

Note: *Please note the following warnings regarding the hazards associated with development systems.*

Table 1 Safety precautions

	**Warning:** *The evaluation or reference board contains DC bus capacitors, which take time to discharge after removal of the main supply. Before working on the converter system, wait five minutes for capacitors to discharge to safe voltage levels. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Warning:** *The evaluation or reference board is connected to the AC input during testing. Hence, high-voltage differential probes must be used when measuring voltage waveforms by oscilloscope. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Warning:** *Remove or disconnect power from the converter before you disconnect or reconnect wires or perform maintenance work. Wait five minutes after removing power to discharge the bus capacitors. Do not attempt to service the drive until the bus capacitors have discharged to zero. Failure to do so may result in personal injury or death.*
	**Caution:** *The heatsink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.*
	**Caution:** *Only personnel familiar with the converter, power electronics and associated equipment should plan, install, commission, and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.*
	**Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	**Caution:** *A converter that is incorrectly applied or installed can lead to component damage or reduction in product lifetime. Wiring or application errors such as under sizing the cabling, supplying an incorrect or inadequate AC supply, or excessive ambient temperatures may result in system malfunction.*

1 Background and specifications

1.1 Application background

The evolution of AI is more rapid than ever and the demand for more power is continuously growing. The power supply units (PSUs) need to be designed considering the AI-specific load transients of the graphics processing units (GPUs) clusters. AI workloads differ from conventional computing loads due to the machine learning process, where huge amounts of data are computed on request, resulting in sudden load changes [4].

The transient loads are expected to be reflected onto the grid supply as well, which is undesirable because sudden current changes will stress the grid and the generators [5]. Moreover, the whole AI infrastructure must be immune to grid shutdowns for the time period when the supply is switched over from one generator to another, or to the battery backup unit (BBU).

The REF_12KW_HFHD_PSU (Energy Buffer) solution from Infineon demonstrates a viable solution of an auxiliary circuit that addresses the above challenges and at the same time provides the benefit of increased power density of the PSU, as proven in the reference design REF_12KW_HFHD_PSU [3].

1.2 The OCP ORv3 and AI requirements

The Open Compute Project “Open Rack V3 5.5 kW PSU specification” [6] has been considered as the main guideline for the design and performance requirements of the PSU, and hence also for the transient events that the unit must comply with. Apart from this standard, in our proposed solution, Infineon has considered the input of other reliable sources in the market, like GPU vendors that are working on the edge of the AI technology and data center infrastructures.

Among the basic requirements and specifications posed by the OCP standard and the market are the efficiency, the power density, and the dimensions of the PSU; but also specific transient events that the PSU must comply with. These will be presented in detail in the following sections.

1.3 Key features of the 12 kW PSU

The main power circuit consists of an AC-DC and a DC-DC converter. The front-end interleaved 3-level flying capacitor totem-pole AC-DC converter provides power factor correction (PFC) and regulates the intermediate DC-link voltage. The back-end isolated DC-DC LLC converter provides isolated and regulated 49–50 V_{DC} nominal output voltage (following a droop control) from the high-voltage rail. More details about the whole PSU can be found in the corresponding application note [3].

The auxiliary circuit is connected in parallel to the DC-link between the two converters and this document is focused only on that part of the circuit. More specifically, a proposed converter and control solution is presented and described in detail that addresses the requirements for hold-up extension and current grid shaping, both of which are essential in AI data centers and server applications. The converter itself is a simple two-switch buck and boost bidirectional converter that acts as an energy buffer and is enabled during the transient events such as the startup period or the hold-up period when the grid is off (the typical value for a server PSU is 20 ms). During these events, the load jumps up to 140% of the nominal load and even the voltage sags. The auxiliary circuit has a dual purpose: one is to increase the power density of the PSU by minimizing the number of electrolytic capacitors, and the other is the grid-current shaping, meaning that the power supplied from the grid shouldn’t suffer from big overshoots and rapid changes.

Although this application note focuses on the auxiliary circuit which operates during the transient events, it is worth presenting the overall PSU features of the REF_12KW_HFHD_PSU (Figure 2), in which the auxiliary circuit is implemented:

- 12 kW maximum steady state output power
- 97.8% peak efficiency at 230 V_{AC}
- 96.5% efficiency at 230 V_{AC} and 100% output load
- 40 mm × 68 mm × 640 mm (including the chassis)
- 113 W/in^3 power density
- 20 ms hold-up time extension at 100% output load
- Power/current grid-shaping function
- Inrush current limiting circuit with no electromechanical relays
- Overcurrent protections on LLC primary and output currents (5 retries before latching)
- AC input voltage brown-out protection
- UVP and OVP protections on output voltage (5 retries before latching)
- UVP and OVP protections on bulk voltage

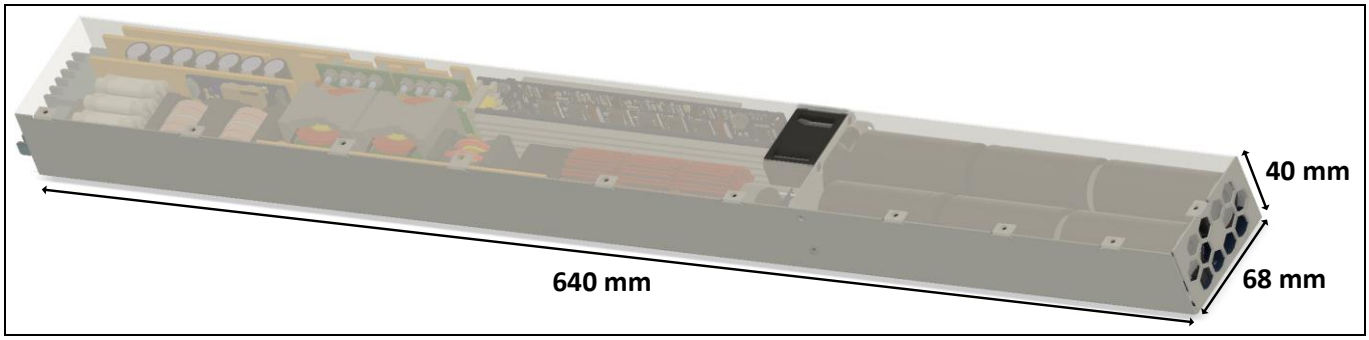


Figure 2 Dimensions of the 12 kW power supply REF_12KW_HFHD_PSU

2 System overview and description

2.1 System overview

The overall PSU consists of two main power converters and an auxiliary circuit as depicted in Figure 3. The first stage is an AC-DC three-level flying capacitor interleaved power factor correction (3L_IL_PFC) converter, which feeds a DC-DC LLC converter. The auxiliary circuit consists of a two-switch buck and boost bidirectional converter.

This auxiliary unit essentially operates as an energy buffer (EB) which stores energy in the electrolytic capacitor bank at the output of the buck converter. The input of the buck converter is connected to the DC-link of the AC-DC and DC-DC converters, on which the amount of capacitance is much less (mainly film capacitors are connected). The stored energy is used during the transient events, and only then is the auxiliary converter operating. During the steady state operation of the PSU, the EB is off and the static switch (IPT60R016CM8) is on, connecting the electrolytic capacitor bank to the DC-link.

The topology of the buck and boost bidirectional converter was selected considering the need of a simple and low volume circuit, with low control complexity and the capability of bidirectional power flow.

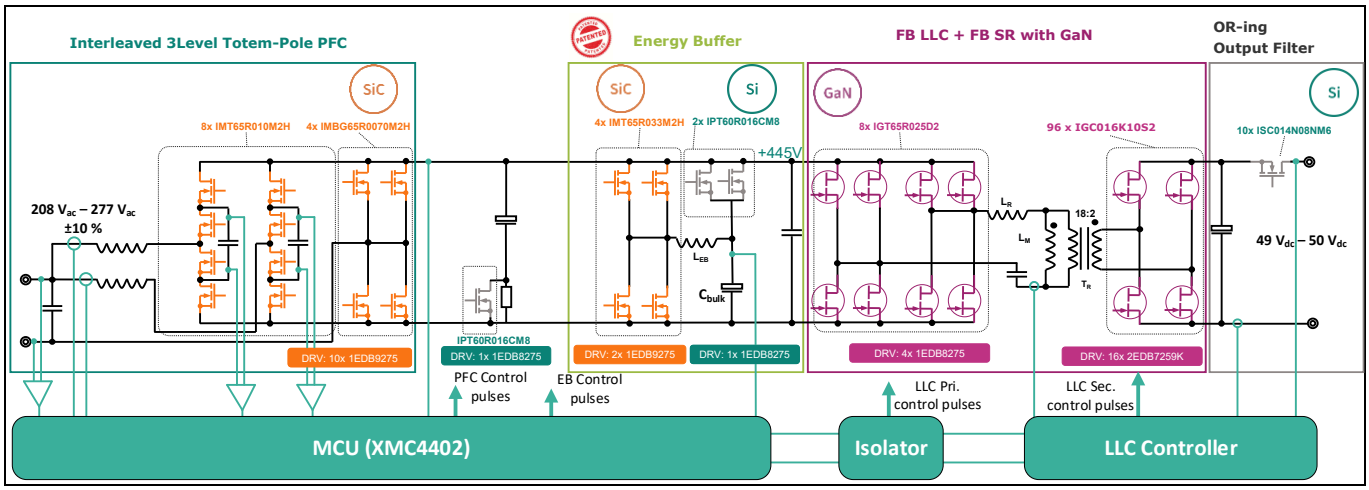


Figure 3 Simplified schematic of REF_12KW_HFHD_PSU with the auxiliary circuit/energy buffer highlighted

2.2 Hardware implementation

The complete hardware implementation of the PSU is shown in Figure 4 with main components and circuit sections highlighted. The EB circuit is located on the same card as the LLC full-bridge (FB) and the controller that is referred to the primary-side potential, which directly controls the PFC and the EB converters. The energy buffer consists of 4 devices (two each in parallel) and some decoupling capacitors, as shown in Figure 5. The inductor of the buck-boost converter lies between the two PFC inductors (Figure 4).

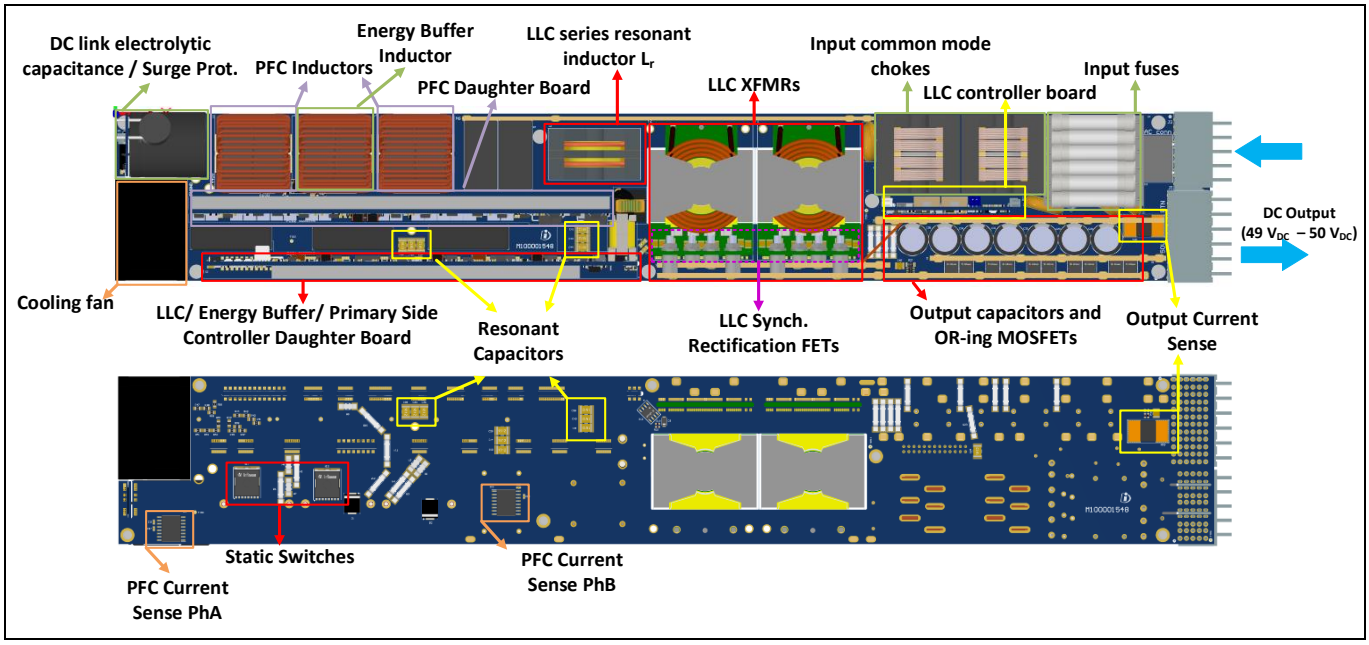


Figure 4 Hardware implementation of REF_12KW_HFHD_PSU (top and bottom)

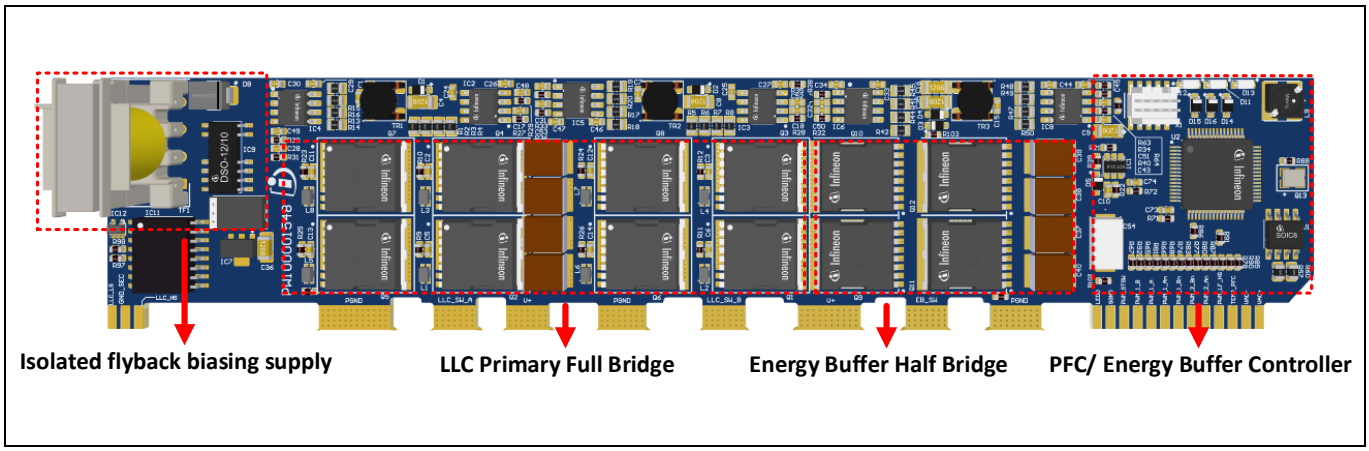


Figure 5 Hardware implementation of the daughter card containing the LLC, the EB, and primary-side controller (top side)

The overall footprint of the EB is quite small compared to the rest of the circuit, but its contribution is significant during the transient events. Moreover, a reduction of the total converter volume is achieved, thanks to the elimination of the additional capacitance that would have been needed for the transient events.

A detailed description for the overall PSU circuit can be found in the application note [3].

3 Topology and operation principles

The functional purpose of the EB is to operate as an auxiliary circuit during transient events, like the line cycle drop-out (LCDO), load jumps, and of course the startup.

A special characteristic of the AI workloads is the periodic load jumps that occur during the data loading and the training of the system [4], [7]. It should be noted that these rapid load changes are naturally reflected onto the grid, creating possible harmful disturbances in the generators, the transformers, and the grid network in general. Therefore, another feature of the EB is to limit the transients seen from the grid-side, but to still be supporting the fast load changes that the AI workloads require. As a result, the need for such an auxiliary circuit is considered essential and crucial for the performance of the PSU.

3.1 Capacitor sizing and AI-workload profiles

In order to calculate the required capacitance of the capacitor bank, the energy that needs to be stored must be derived, and also the transient time intervals must be defined.

Regarding the hold-up requirement, the energy can be easily calculated for the nominal operation with Equation 1, where P_{nom} is the nominal output power of the converter (for simplicity the DC-DC converter efficiency is neglected) and t_{hold_up} is the LCDO time event.

$$E_{hold\_up} = P_{nom} * t_{hold\_up}$$

Equation 1 Energy calculation for nominal operation

Note: An even worse case would be if the LCDO happens at the same time during a transient load higher than 100% of the load.

If no auxiliary circuit is used, then the required capacitance to support the output load during hold-up is calculated using Equation 2, where V_{nom} is the voltage during steady state and V_{min} is the minimum allowed voltage of the DC bus at which the LLC converter can operate. The ripple voltage is neglected for simplicity here, otherwise it can also be subtracted from the average value of V_{nom}.

$$C_{hold\_up} = \frac{2*E_{hold\_up}}{{V_{nom}}^2 - {V_{min}}^2}$$

Equation 2 Capacitance for hold-up

If an auxiliary converter is implemented as the interface between the capacitor bank and the DC bus, then Equation 2 can be modified in the form of Equation 3, where η is the efficiency of the auxiliary converter and $V_{min,aux}$ is the new minimum voltage of the capacitor bank. This value can be much lower than V_{min}, as the auxiliary converter can boost the voltage and keep the DC bus at the nominal value.

$${C_{hold\_up}}' = \frac{2*E_{hold_{up}}/\eta}{{V_{nom}}^2 - {V_{min,aux}}^2}$$

Equation 3 Modified equation for hold-up capacitance

By combining Equation 2 and Equation 3, the relation of the capacitor banks with and without the energy buffer circuit can be derived as Equation 4 (considering only the hold-up requirement at this point). The auxiliary converter can be designed to be quite efficient (η>98% weighted efficiency), therefore η≈1.

$$\frac{C_{hold\_up}{}'}{C_{hold\_up}} = \frac{V_{nom}{}^2 - V_{min}{}^2}{V_{nom}{}^2 - V_{min,aux}{}^2}$$

Equation 4 Relation of capacitor banks

For example, without the energy buffer, the minimum value of V_{min} could be set to 360 V, which is still a value that would stress the LLC converter, by forcing lower operating frequency and higher currents. By using the energy buffer, the value of $V_{min,aux}$ can go down to 200 V, and still due to the boosting feature the DC-link voltage V_{nom} can be at 445 V. Considering the above numbers in this example, there is a reduction of around 57% in bulk capacitance, which directly corresponds to volume reduction in the PSU.

Additionally, the benefit of using the energy buffer is not limited to the bulk capacitance value. As mentioned, the DC bus voltage is kept to the nominal value, while in the case of a standalone capacitor bank the voltage would drop lower. As a result, the design of the LLC converter would be much more challenging, requiring wider regulation range due to the big variation of the input voltage, and moreover, the transformer design would be also affected by the lower operating frequency and higher currents that would lead to bigger core size to avoid saturation.

The LCDO is only one of the transient events that the PSU should be able to sustain. The other main requirement refers to loads jumping higher than 100% of the nominal load. Considering that the power from the grid cannot exceed 110% of its rated value, the remaining amount must be covered by the capacitor bank. In Figure 6, an example of a load jump pattern is presented (red line) with corresponding time intervals for some worst case scenarios: 175% of the nominal load for $t_{175\%}$ = 2 ms[1], 140% for $t_{140\%}$ = 50 ms[1], 100% for $t_{100\%}$ = 50 ms and 10% for $t_{10\%}$ = 25 ms. The average power supplied to the load during this time is still 100% of the nominal power and shouldn't be higher. The graph below is valid regardless of the existence of an auxiliary circuit or not.

[1]These are the maximum expected values based on [7].

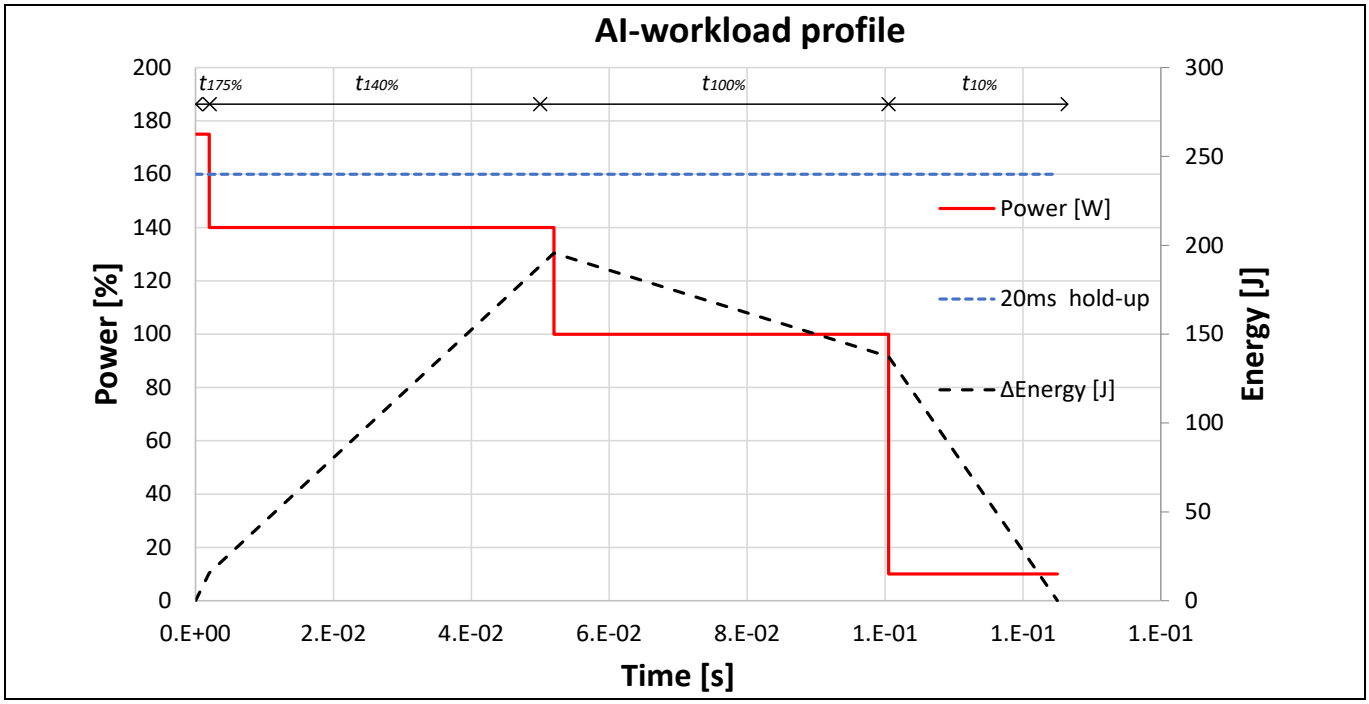


Figure 6 **A worst-case example of load jump profile of an AI-workload depicted with the output power (red), the required energy from the capacitor bank (black) and the hold-up time required energy for a 12kW converter and 20 ms LCDO**

The energy required from the capacitor bank is depicted with the dashed black line and can be calculated with Equation 5.

$$E_{add} = \left(P_{load} - P_{grid}\right) * t$$

Equation 5 **Energy required from the capacitor bank during worst-case scenarios**

It can be easily noted that, when the power of the load exceeds the maximum allowed power from the grid, the capacitor bank is discharged (energy is rising), while when the load drops below 110% then the capacitor bank can be charged, hence the required energy is decreasing. The maximum value of the energy defines the capacitor sizes (Equation 2 and Equation 3 can be generalized). Based on Figure 6, the LCDO requires more energy than the load jumps and it should be considered for the sizing of the capacitor bank.

It should be noted that, if no auxiliary circuit is used, then the minimum voltage, which represents the input voltage of the LLC, might need to be higher than in the case of the LCDO. The reason is that the LLC must not only operate with a lower input voltage but at the same time must deliver more power than the nominal amount, a consequence that magnifies the design concerns that are mentioned previously. In this case, the energies of both events should be considered when calculating the required capacitance.

3.1.1 Energy buffer waveforms

In Figure 7, the average power per grid cycle for the grid, the load, and the auxiliary converter are shown, following similar patterns as in the previous example. In the case of the energy buffer, positive power signifies charging of the capacitor bank and negative power indicates its discharging. Similarly, in Figure 8, the energy fluctuation is shown, where the y-axis indicates the difference from the initial stored energy. The positive slope indicates charging and the negative discharging of the capacitor bank.

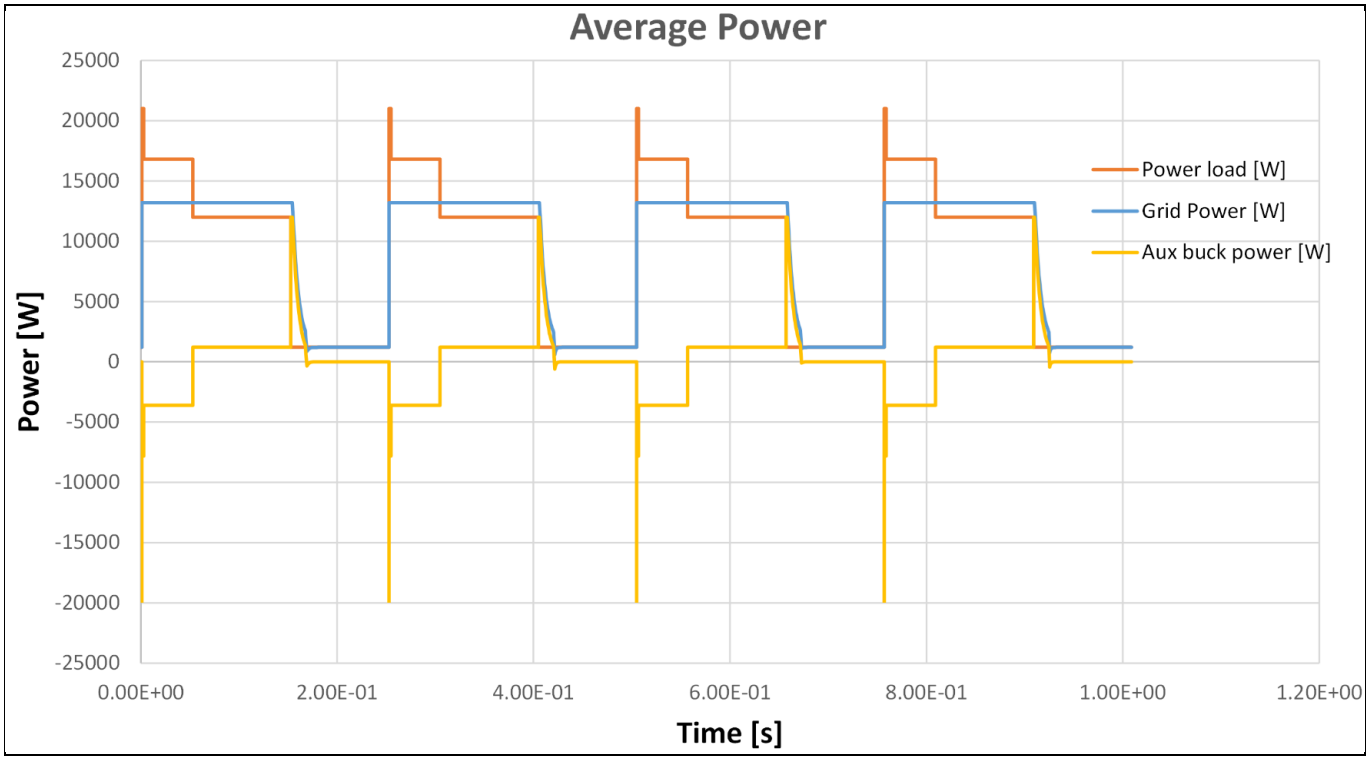


Figure 7 **An example of a periodic sequence of load jumps depicted with the output power (orange), the grid power (blue), and the auxiliary converter power (yellow), with immediate grid response**

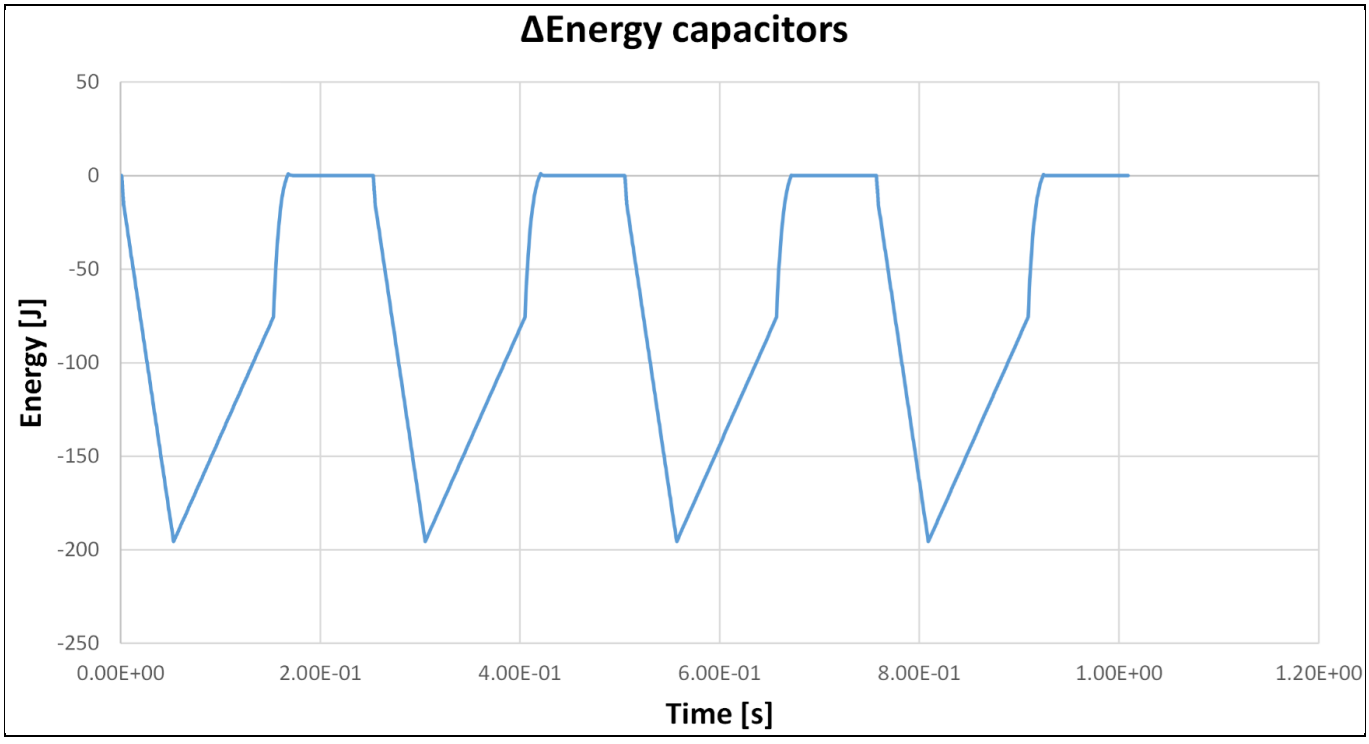


Figure 8 **An example of a periodic sequence of load jumps depicted with the energy difference of the capacitor bank, with immediate grid response**

It is evident that the difference between the grid power and the auxiliary power results in the load power, while the EB is managing the excess power between the load and the grid.

The example in Figure 7 and Figure 8 refers to an ideal case, in which the grid responds immediately. However, within the data center requirements, there is also the limitation of the slew rate of the power supplied from the grid. If this restriction is applied to 660 W/ms (based on 110 % of the nominal power that can be supplied in a grid period of 20 ms) then the above figures are modified to Figure 9 and Figure 10.

The rise and falling edges of the grid are essentially delayed, extending the operation of the auxiliary circuit that needs to manage the difference in power between the grid and the load.

During the 175% and 140% of overload, the capacitor bank discharges even faster than in the ideal case, because the grid cannot respond fast enough, therefore the energy required from the capacitor bank is higher. Moreover, during the negative load step (load decreasing below 110%) the capacitor bank must be overcharged in order to maintain the maximum slew rate of the power coming from the grid.

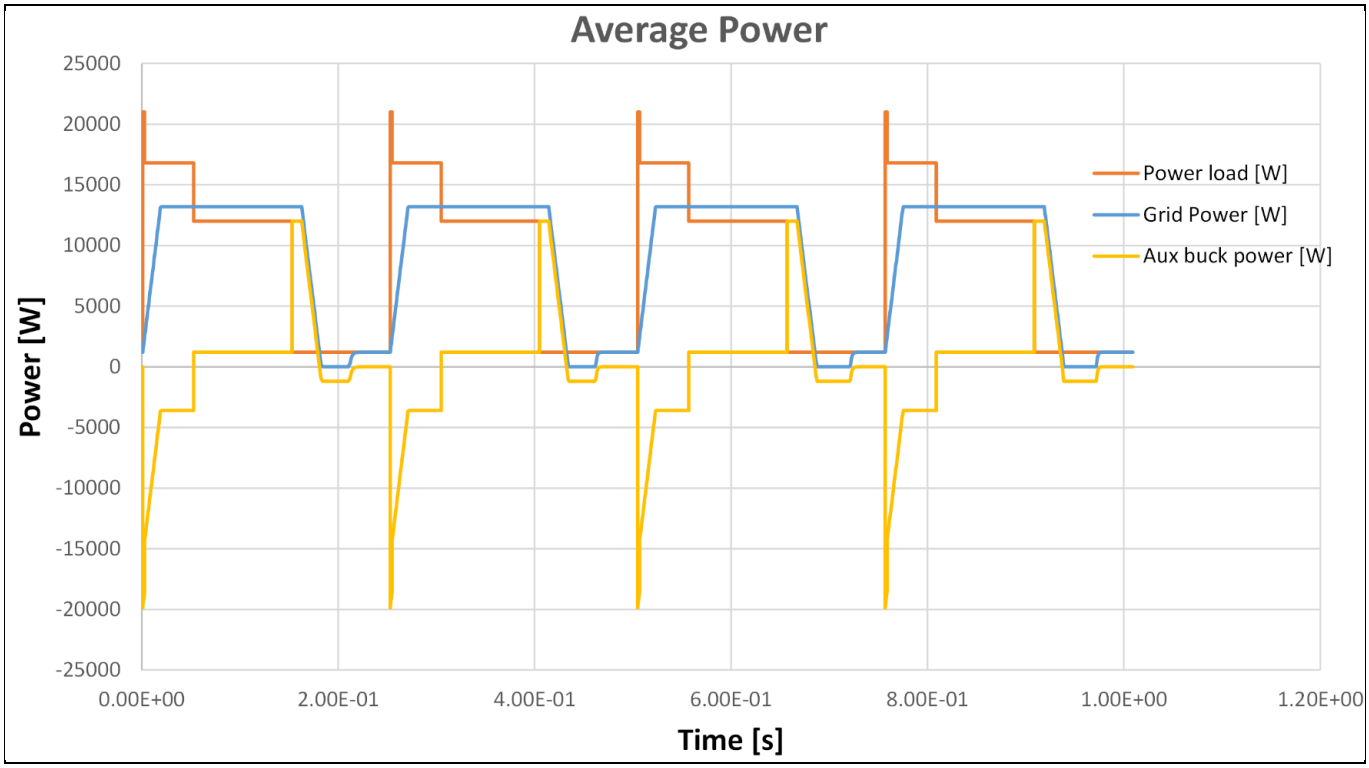


Figure 9 **An example of a periodic sequence of load jumps depicted with the output power (orange), the grid power (blue), and the auxiliary converter power (yellow), with 660 W/ms of grid response**

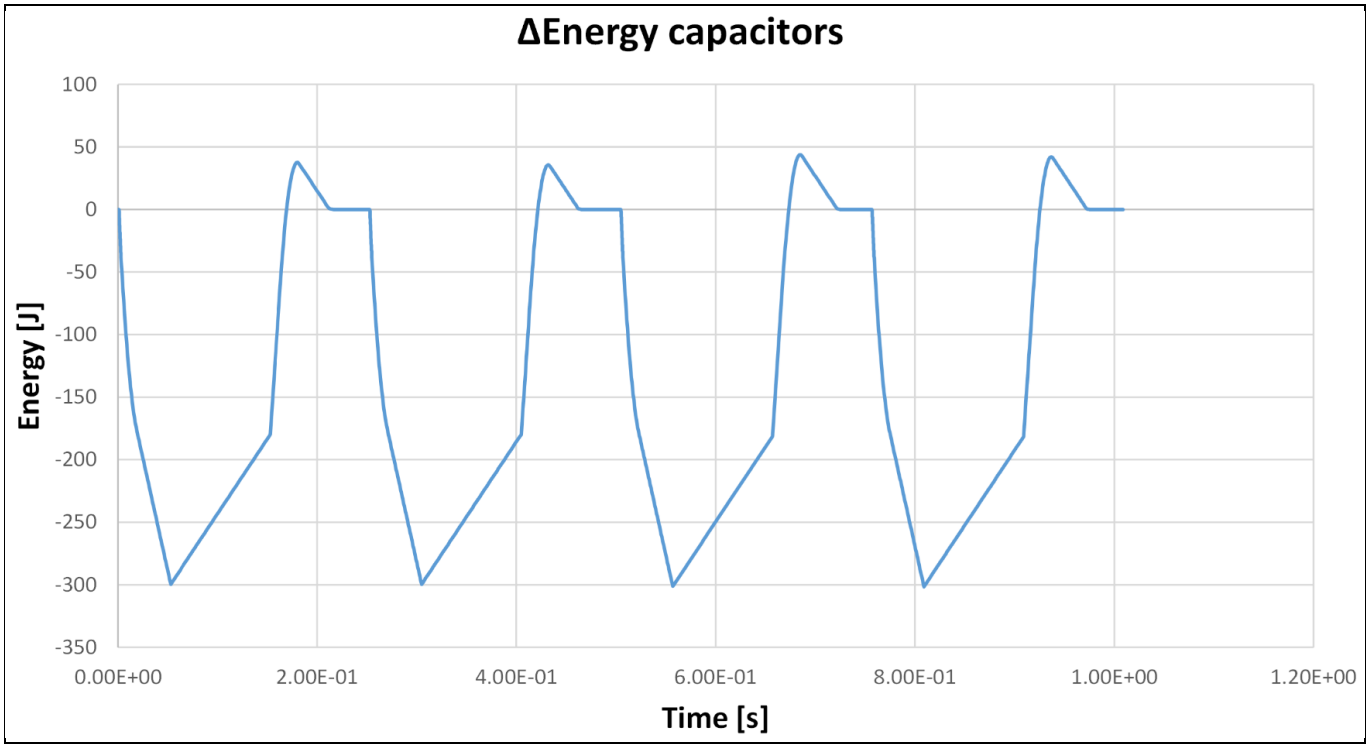


Figure 10 An example of a periodic sequence of load jumps depicted with the energy difference of the capacitor bank, with 660 W/ms of grid response

To conclude, when calculating the capacitance of the capacitor bank, all system requirements should be defined carefully, as they have a direct impact on the necessary energy that needs to be stored for transient events.

3.2 Bidirectional buck-boost topology

In Figure 11, a simplified schematic of the PSU is shown, focusing on the connection of the EB circuit in the system and omitting any other details about the rest of the unit. The PFC and LLC stages are represented as simple blocks connected to the same DC-link.

The main DC bus consists mainly of film capacitors but there is also an electrolytic capacitor, which is placed mainly for limiting the voltage overshoot during a surge event, when the static-switch is off. This additional capacitance from the electrolytic provides better filtering and stability during the transient events as well, but it will be disregarded for the sake of the explanation and only film capacitors are depicted in Figure 11.

During steady state, the static-switch $Q_{St.Sw}$ is conducting and connects the DC-link with the capacitor bank C_{bulk}, as shown in Figure 12. Therefore, the electrolytic capacitors provide sufficient filtering for the double line frequency (100/120 Hz) ripple that comes from the grid. In this state, the EB circuit has no contribution to the operation and the losses of the unit. The voltage class of the static switch depends on the DC-link voltage, while the on-resistance of the device doesn't depend on the main current flowing between the two main converters, as the switch is not placed in series, and therefore doesn't act as a bypass switch. It is $Q_{St.Sw}$ that conducts the AC current ripple that the electrolytic bank filters from the DC bus. Moreover, it should be able to sustain the power dissipated on it during a surge event.

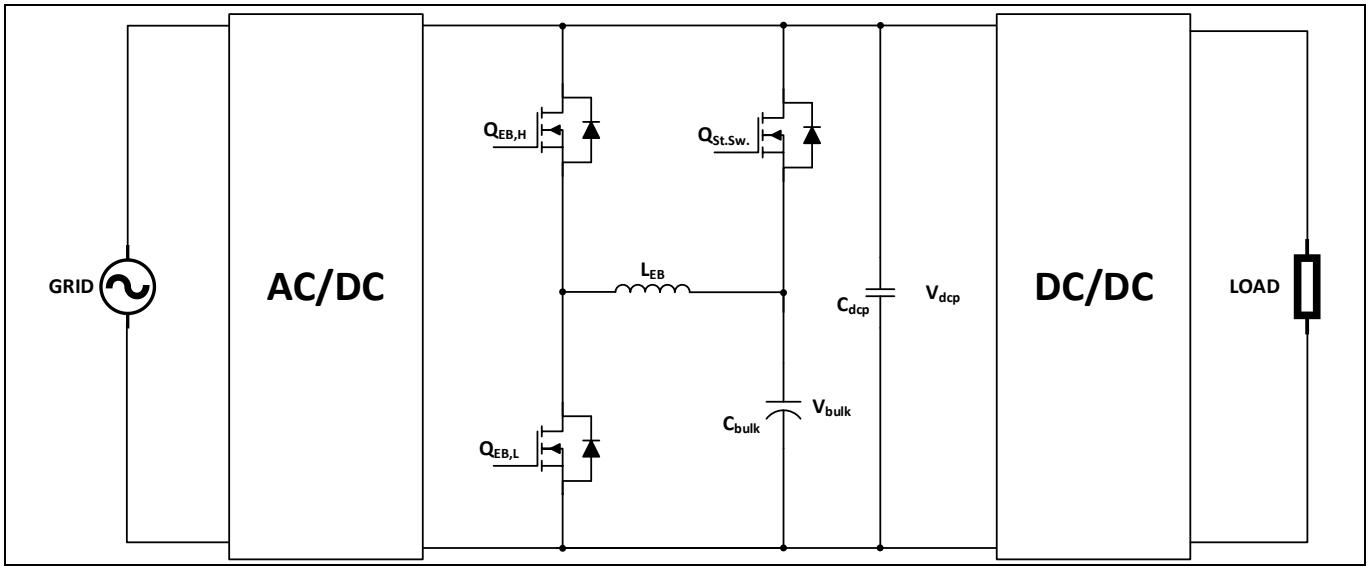


Figure 11 **Simplified schematic of the auxiliary circuit in the design of REF_12KW_HFHD_PSU**

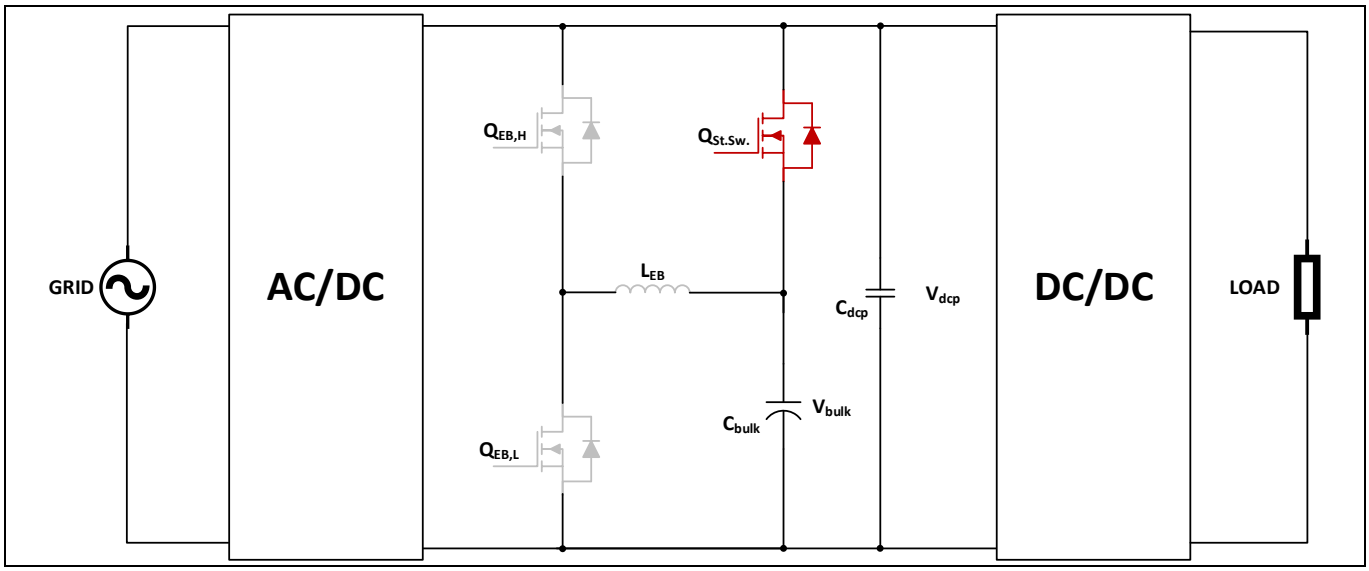


Figure 12 **Simplified schematic of the auxiliary circuit in the design of REF_12KW_HFHD_PSU, during steady state operation**

As already mentioned, the purpose of the energy buffer circuit is to provide additional energy to the circuit, in the event that it cannot be supplied from the grid. This could be either because the grid has been shut down (line cycle drop-out – LCDO) or because it cannot provide the required power at the required rate, which means that there is a limit to how fast the grid power can increase. Therefore, the EB must be able to discharge and charge the capacitor bank, hence bidirectional power flow is required.

The bidirectional buck-boost topology in our proposed solution is theoretically analyzed for the case of a 12 kW PSU. The LCDO is one of the most stressful operating conditions for the EB, as it handles the entire energy that needs to be supplied to the output. Therefore, a detailed loss analysis is performed isolating the LCDO event for 20 ms plus 80 ms of additional operating time until the capacitor bank is brought back close to the nominal value after the grid returns. The theoretical efficiency and overall losses of the auxiliary converter are depicted in Figure 13. The highest stress occurs at the end of 20 ms, where the bulk voltage is at the minimum value, as expected. Despite that, the overall efficiency of the converter is considerably high, and the losses are

constrained within acceptable levels even if the LCDO would be a frequent and repetitive event, which is not usually the case.

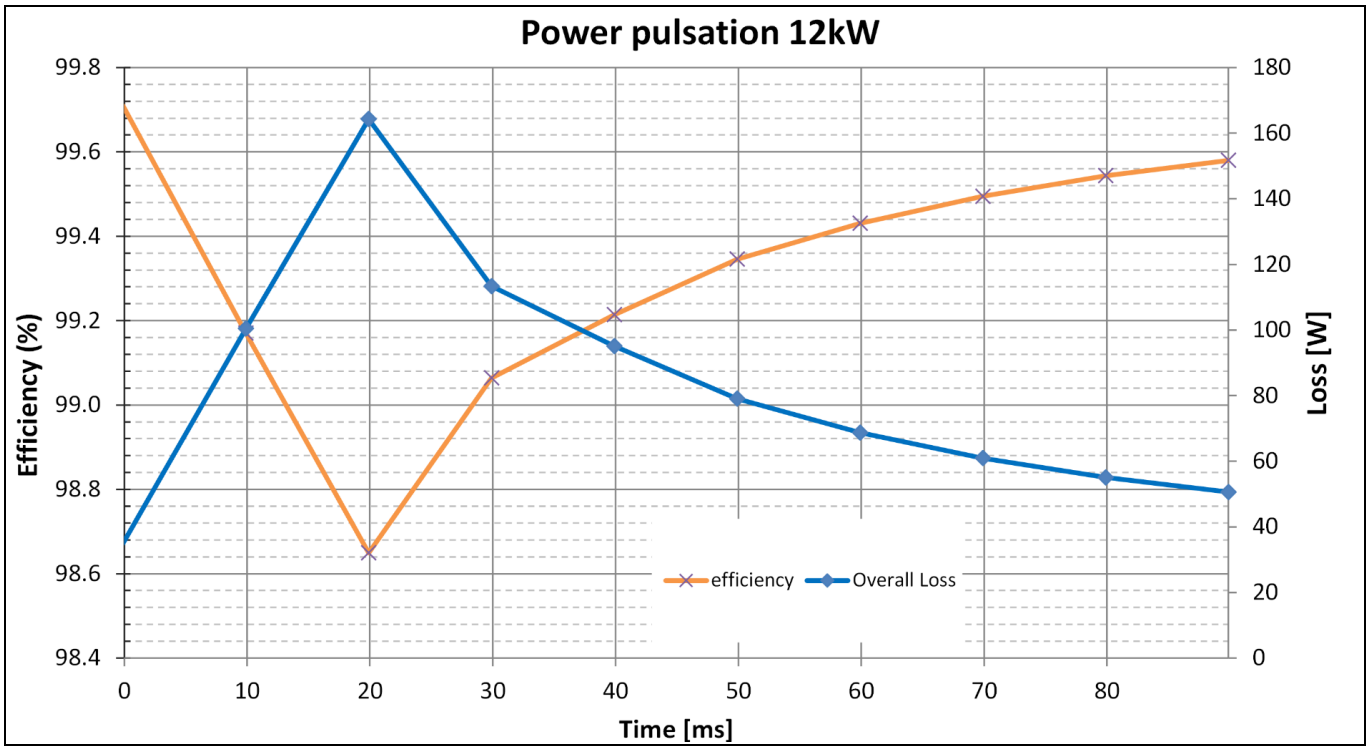


Figure 13 Theoretical efficiency and loss analysis results during an LCDO event

3.2.1 Buck operation: storing energy

The auxiliary circuit of the EB operates as a buck converter when the capacitor bank needs to be charged, stepping down the voltage of the DC-link to a value very close to it. Therefore, the range of the voltage gain must be wide, as during the startup of the unit the electrolytic capacitors are totally discharged. $Q_{EB,H}$ operates as the main switch and $Q_{EB,L}$ operates as a synchronous switch (diode mode). The power flow is shown with green arrows in Figure 14, resulting in charging the electrolytic bank from the grid.

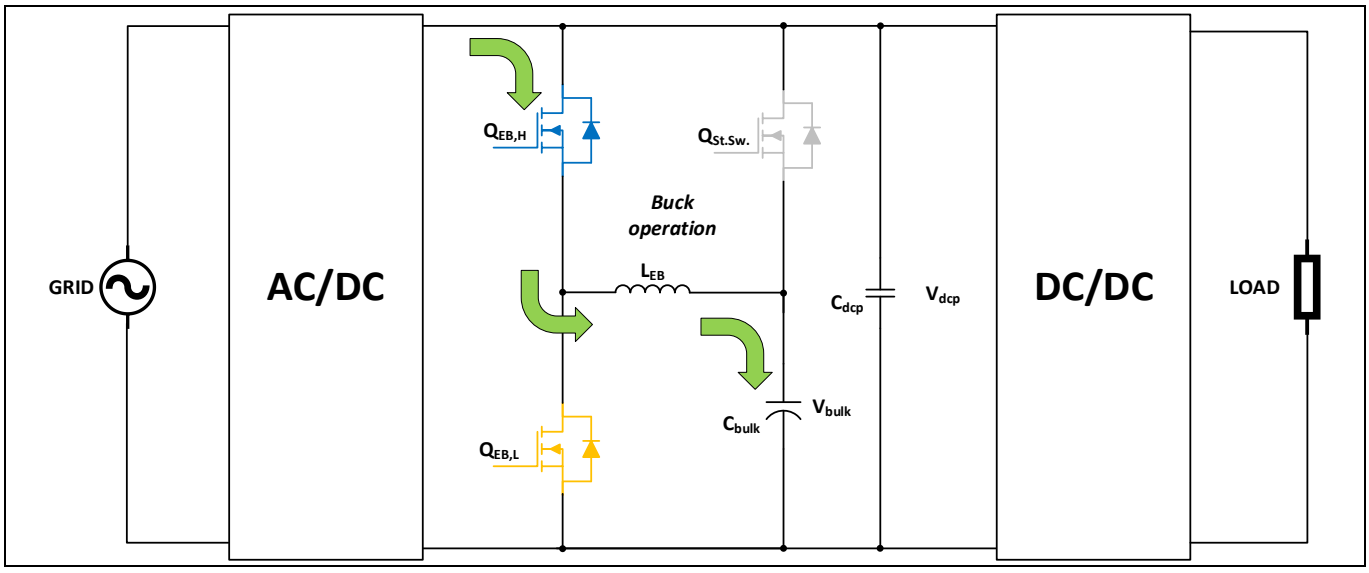


Figure 14 Simplified schematic of the auxiliary circuit in the design of REF_12KW_HFHD_PSU, during buck operation

3.2.2 Boost operation: releasing energy

When additional energy is needed to support the load, but cannot be drawn from the grid (LCDO or power limit) the auxiliary circuit operates as a boost converter with $Q_{EB,L}$ operating as the main switch and $Q_{EB,H}$ operating as a synchronous switch (diode mode). The power flow is shown with green arrows in Figure 15, resulting in discharging of the electrolytic bank through the load.

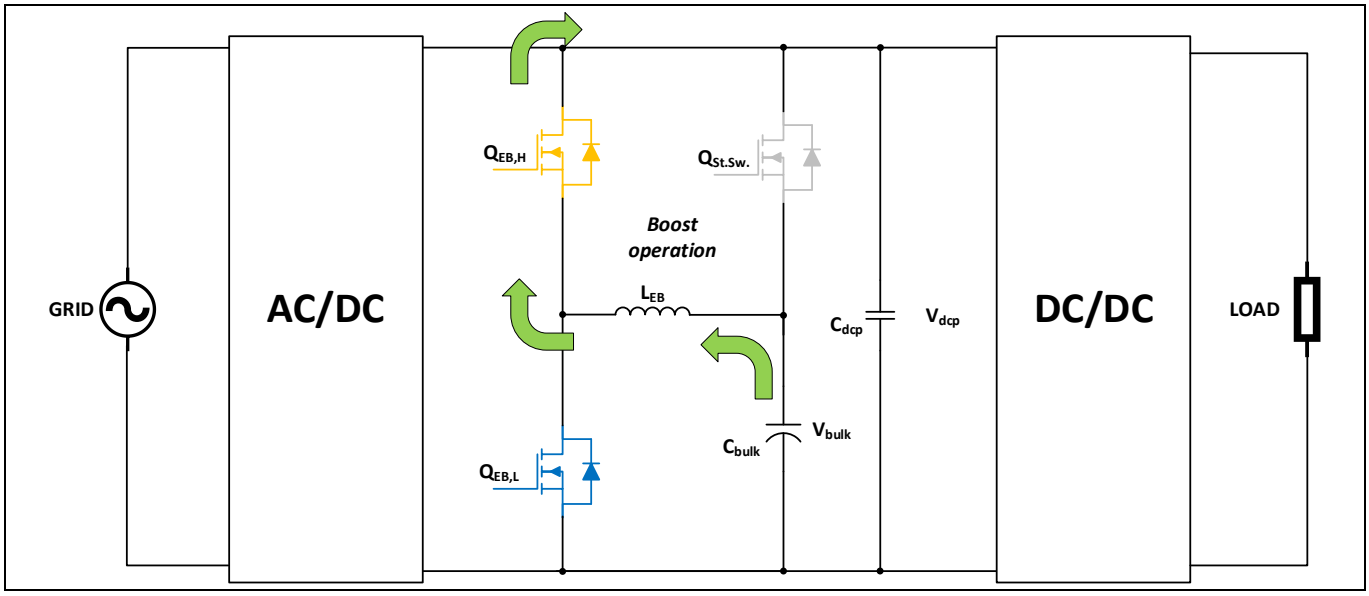


Figure 15 Simplified schematic of the auxiliary circuit in the design of REF_12KW_HFHD_PSU, during boost operation

3.3 Transient events

As discussed above, the EB operates during transient events, but the requirements are not only to support the load but also to maintain the DC-link voltage (V_{dcP}) at its nominal value, regardless of the input voltage and the load demand. From the perspective of the DC-DC converter, it is irrelevant whether the auxiliary circuit operates, as long as V_{dcP} voltage is kept to the nominal value. The LLC is responsible for controlling the required power that needs to be provided to the load. It should be noted that the operation of the PFC and the EB are coupled, as their voltage control refers to the same DC-link voltage. More details about the control loops and dependencies will be presented in Section 4 with explanatory block diagrams.

To better understand the following subsections, it is essential to point out that the auxiliary converter controls the DC-link and the electrolytic bank voltages, not the output load. Also, the block diagrams and experimental results are used to describe the operating sequences of the EB in different transient events.

3.3.1 Startup

The simplest transient event is the startup of the converter. In Figure 16, a sequence of events is shown. The red color indicates that the corresponding part of the circuit is disabled. At first, only the PFC operates, and it is charging the DC-link capacitance (Figure 16 (a)). Then follows the charging of the electrolytic capacitor bank by enabling the auxiliary circuit, while still the LLC converter is disabled (Figure 16 (b)). Finally, the two buses are connected via the static switch and the LLC starts transferring power to the load (Figure 16 (c)), while the electrolytic bank provides sufficient filtering of the 100/120 Hz ripple voltage.

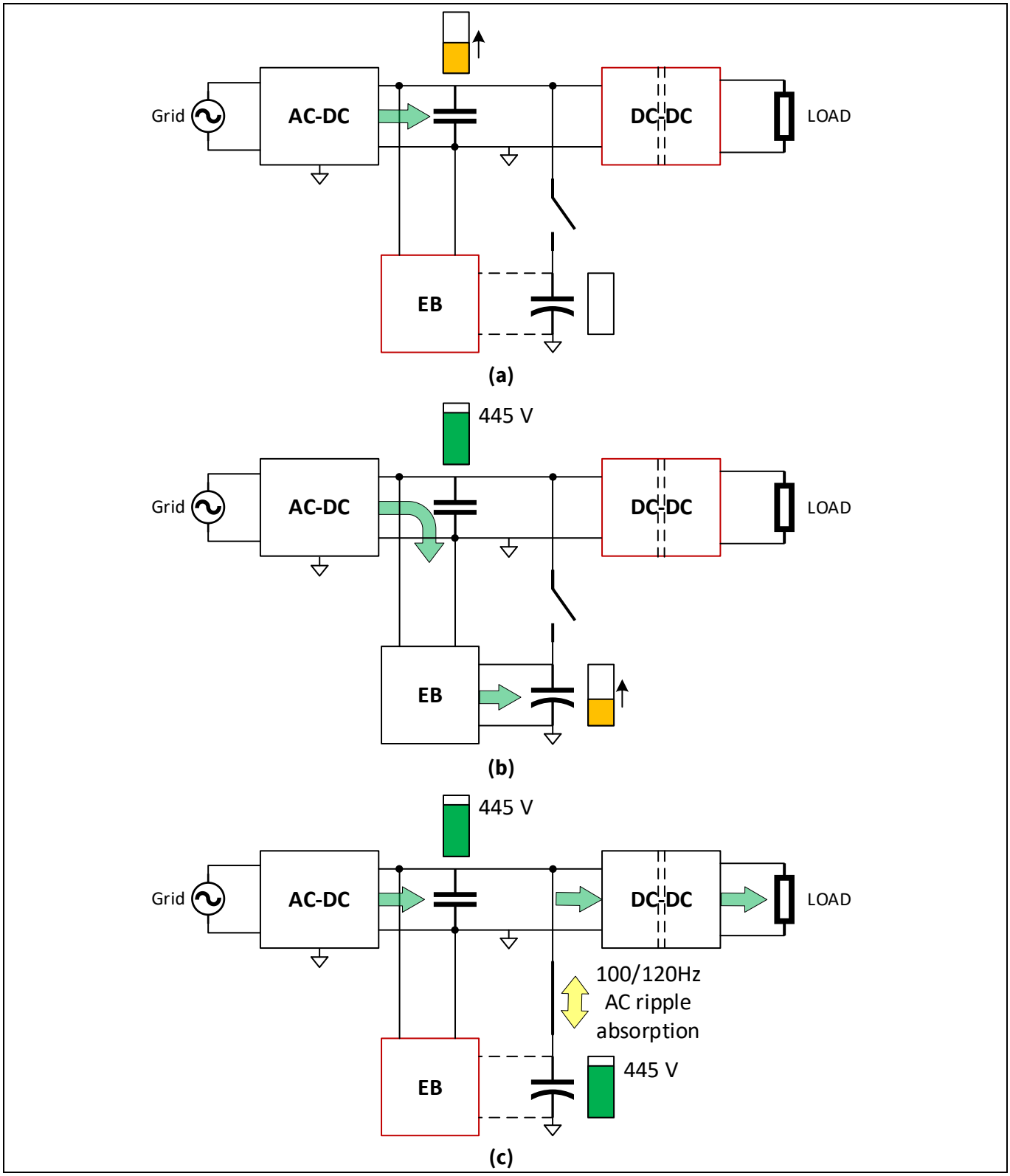


Figure 16 **Block diagram of the operation stages during startup: (a) charge of the DC-link capacitance, (b) charge of the electrolytic capacitor bank, and (c) enabling of the static-switch**

The above sequence can be seen experimentally in Figure 17. The converter is initially off and the input voltage from the grid is applied under full-load conditions.

Point 1-2: The DC-link capacitance starts charging through the PFC operation (V_{DC} rises).

Point 2-3: The EB starts operating in buck mode, charging the electrolytic bank from the grid through the PFC (V_{bulk} rises).

Point 3: The voltage difference between the DC-link (V_{DC}) and the V_{bulk} is close to 5 V (adjustable value), the EB turns-off, and the static switch connecting the two banks is turned-on.

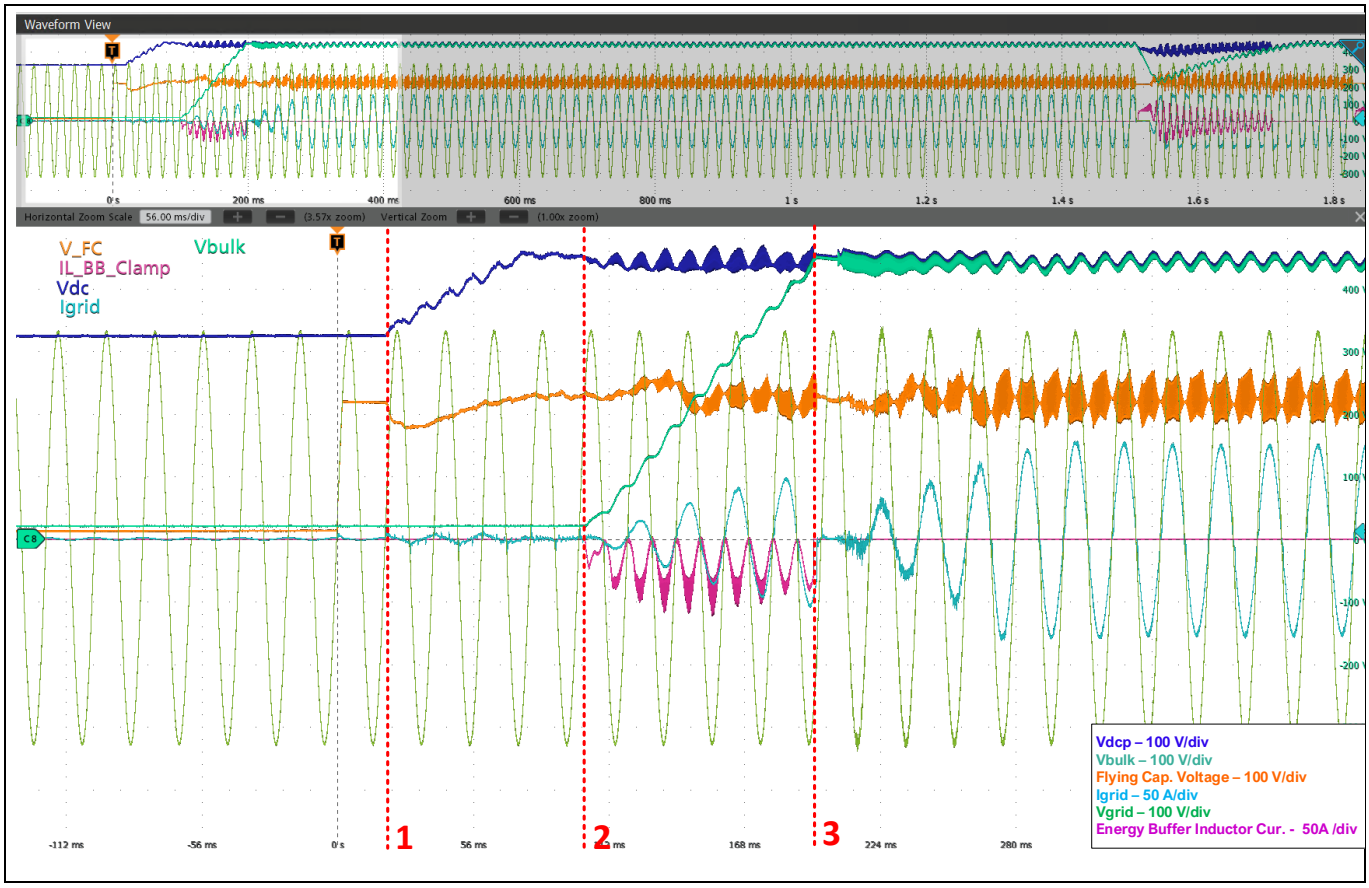


Figure 17 Experimental results during the startup of the PSU under full load conditions

3.3.2 Line cycle drop-out (LCDO)

One of the most important requirements in data centers is for the PSU to sustain the maximum power transfer to the load, for a maximum of 20 ms, while the grid voltage is zero. This event can be divided into two main sections, as shown in Figure 18.

First, when the grid is off, the EB starts providing the required energy to the load by discharging the electrolytic capacitor bank, while at the same time maintaining the DC-link voltage at the nominal value of 445 V (Figure 18 (a)).

After the grid power returns, it continues supplying the load, while at the same time charging the electrolytic capacitor bank through the PFC and the auxiliary converter. The power flow in the EB is bidirectional but the average current is positive, in the sense that it is charging the electrolytic bank. This will be better described with the experimental waveforms that follow in Figure 19.

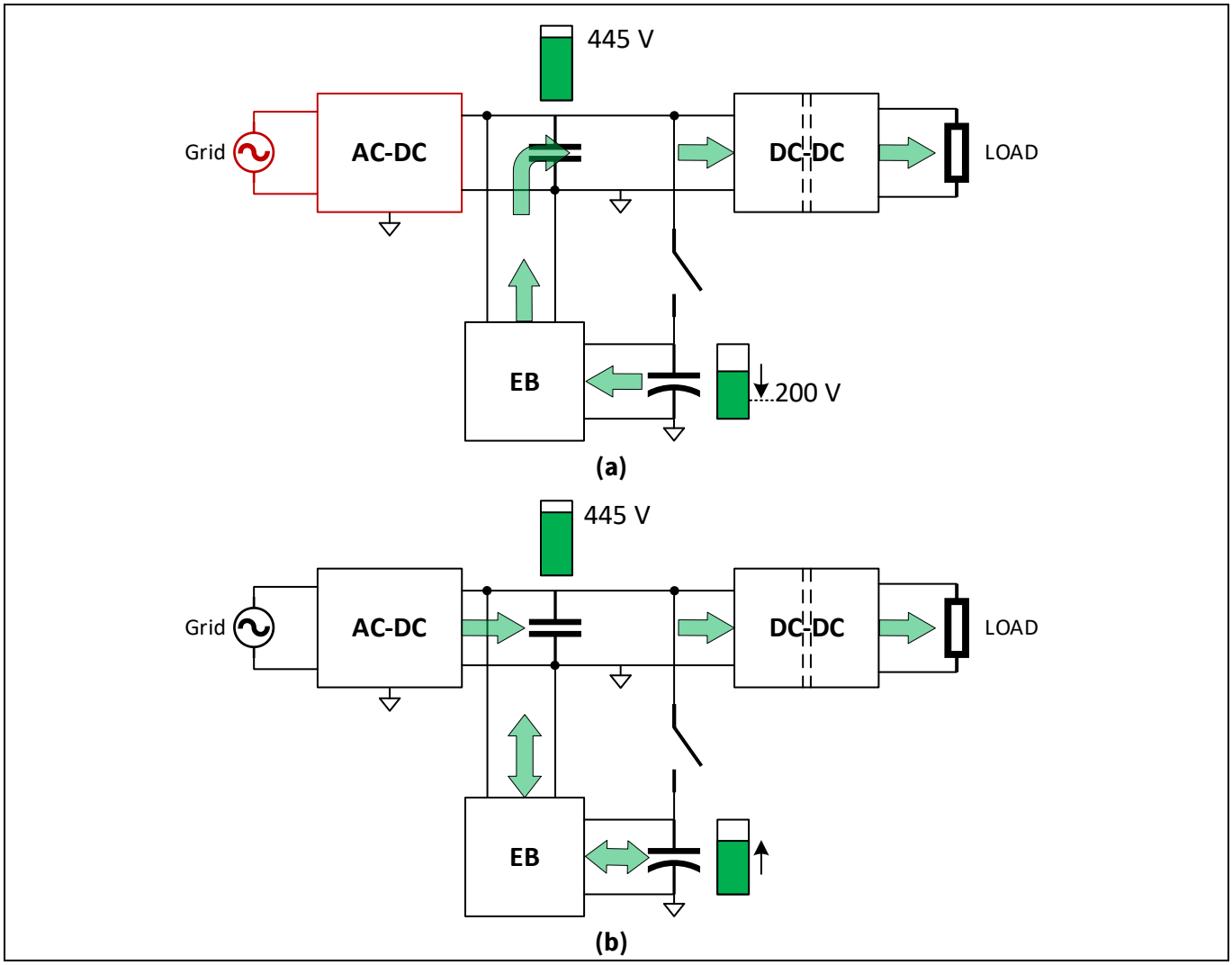


Figure 18 **Block diagram of the operation stages during LCDO: (a) discharge of the capacitor bank and (b) recharge of the capacitor bank**

Point 1: While the converter operates in steady state at full load, the grid voltage drops to zero (LCDO) for 20 ms.

Point 1-2: During the time that the grid is off, the EB operates in boost mode, discharging the capacitor bank to keep the DC-link voltage close to the nominal value, so that the LLC keeps supplying the output load.

Point 2: The grid voltage returns. The PFC must now supply the load power plus the energy that was lost from the big capacitor bank.

Point 2-3: However, the grid power cannot exceed 110% of the rated power. The EB operates in both directions, in buck and boost modes, alternatively. More specifically, close to the peak of the grid voltage, the grid provides energy for both the DC-link and the big capacitor bank (charging it), hence the EB operates in buck mode. While closer to the zero-crossing of the grid voltage, the capacitor bank provides the energy needed to support the DC-link and the power drawn from the load, hence the EB operates in boost mode.

Point 3: After the continuously exchanging power flow, the average energy supplied to the electrolytic capacitor bank has been positive thanks to the synergy of the control loops of the PFC and the EB converters. Thus, the V_{bulk} voltage is able to reach close to the value of the DC-link voltage V_{dcP}, therefore the EB stops

operating and the two buses are connected via the static switch. The converter continues to operate in steady state. The nominal load of the PSU has been continuously supplied despite the LCDO.

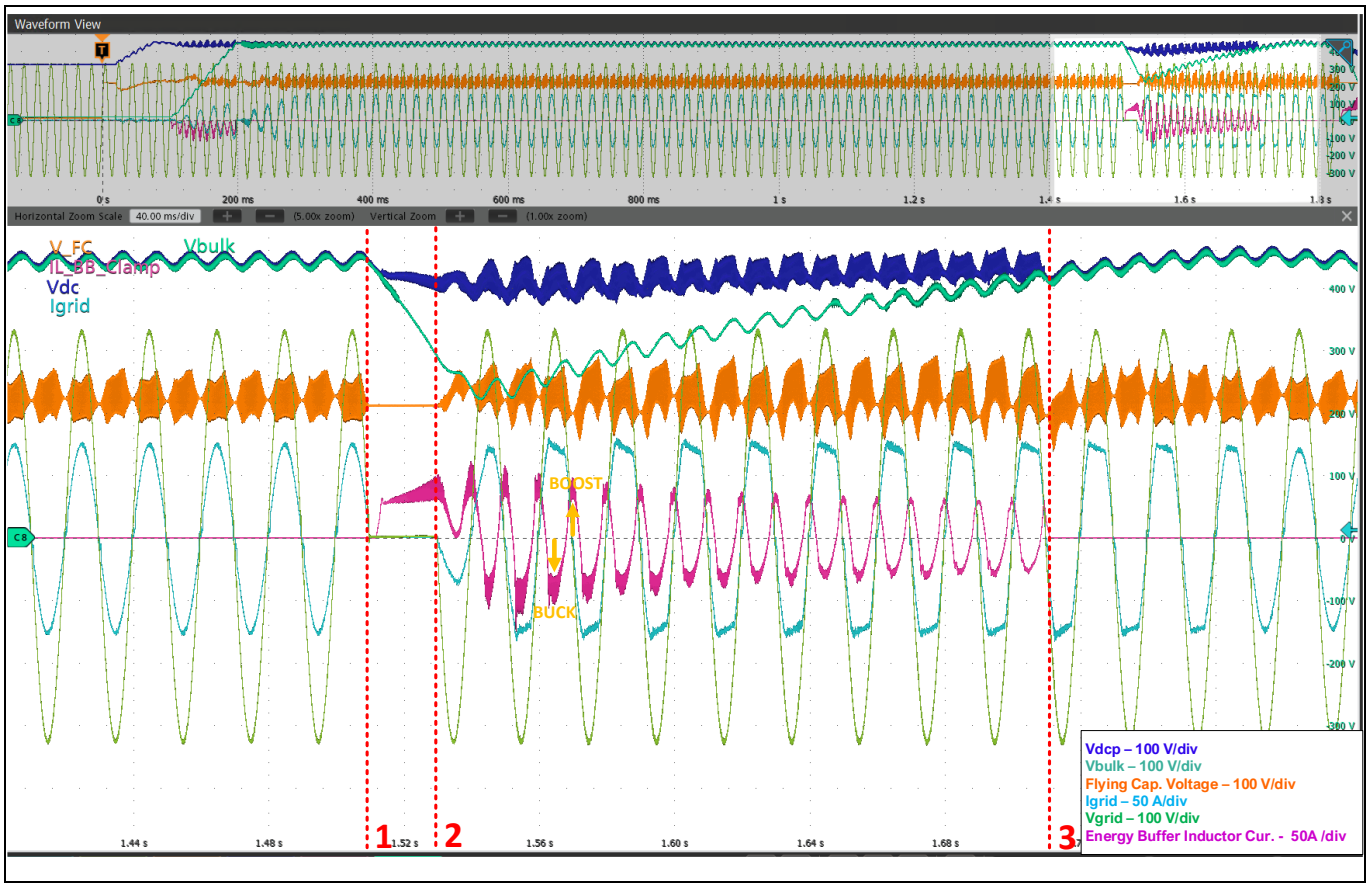


Figure 19 Experimental results during the LCDO under full-load conditions

3.3.3 Load jumps

As already mentioned, load jumps are considered normal transients for the AI workloads and they can even be periodic events with the peak power more than 100% of the nominal power. In the following experimental example, a transition from 10% to 100% will be considered, but the same principle holds for any kind of load step.

In this case, the auxiliary circuit serves as a “damping factor” for the grid, in the sense that the step response of the grid power should be limited to a maximum of 660 W/ms. This number is derived from an existing customer’s requirements but is not according to any standard at this point; that is why this value is configurable in the firmware. The EB supplies the extra power that is not “permitted” from the grid (see Figure 20). A rapid change of the grid power should be avoided (grid-shaping) in order to minimize the stress on the grid network, the generators, and the other loads “hanging” from it.

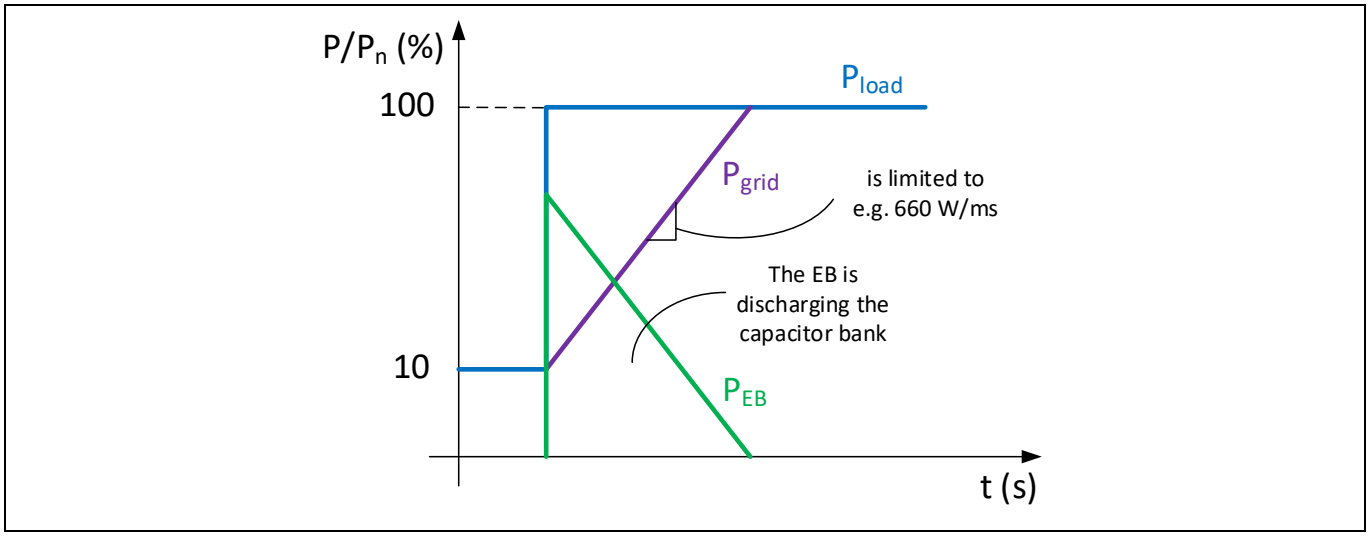
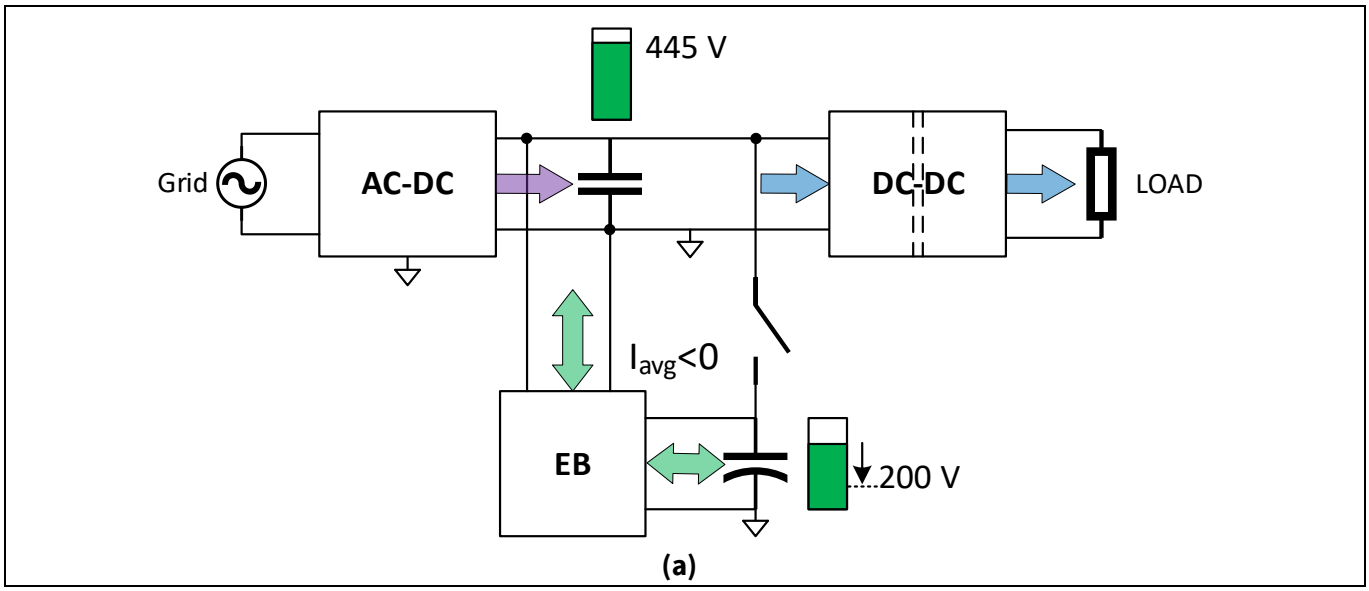


Figure 20 Indicative graph of the relation of power from the grid, the EB, and the load during a positive load-jump transition

In Figure 21, the sequence of the operating conditions is presented, from the moment that a load jump is detected. First, the power from the grid starts rising towards the power that the load requires after the step change. This slew rate of the power increase is limited by the EB operation, which covers the difference in power between the load and the grid (see Figure 20).

There is bidirectional power flow between the DC-link and the capacitor bank, so that the DC-link voltage is maintained to the nominal value. On average the capacitor bank is discharged during the transient time interval (Figure 21 (a)) and is charged again when the conditions permit it (Figure 21 (b)), a procedure that is automatically implemented via the control structure.



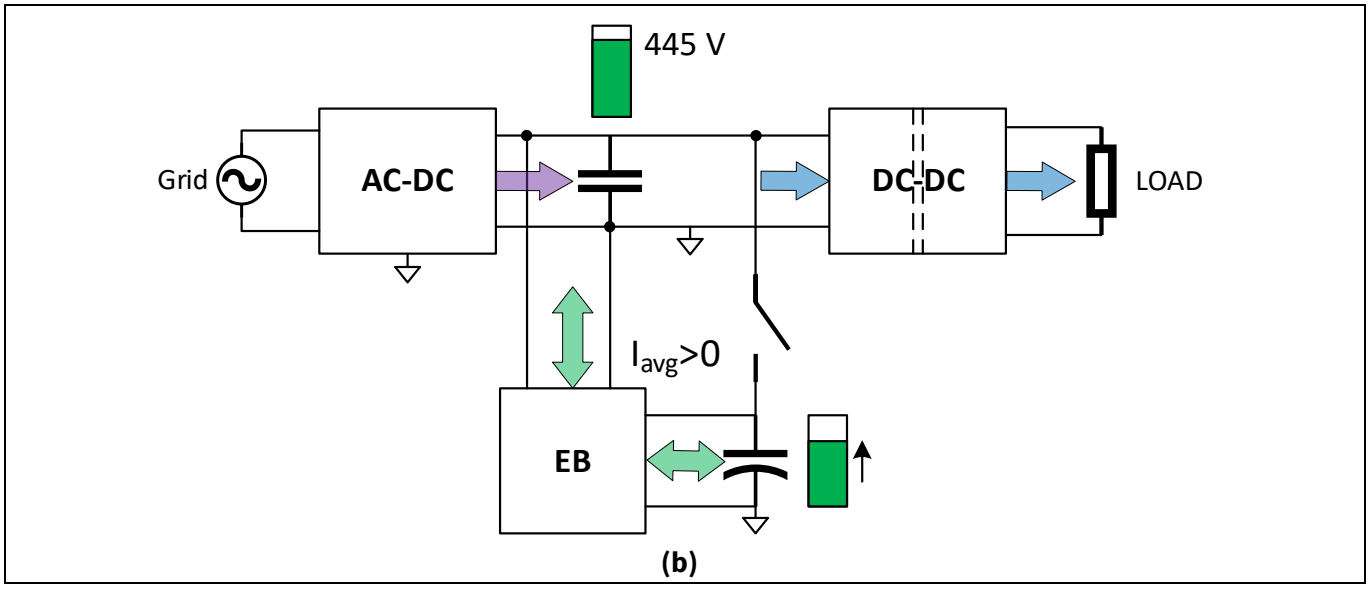


Figure 21 **Block diagram of the operation stages during a load jump: (a) discharge of the capacitor bank and (b) recharge of the capacitor bank**

In Figure 22, the experimental results of a load jump are presented, followed by an explanation of the waveforms.

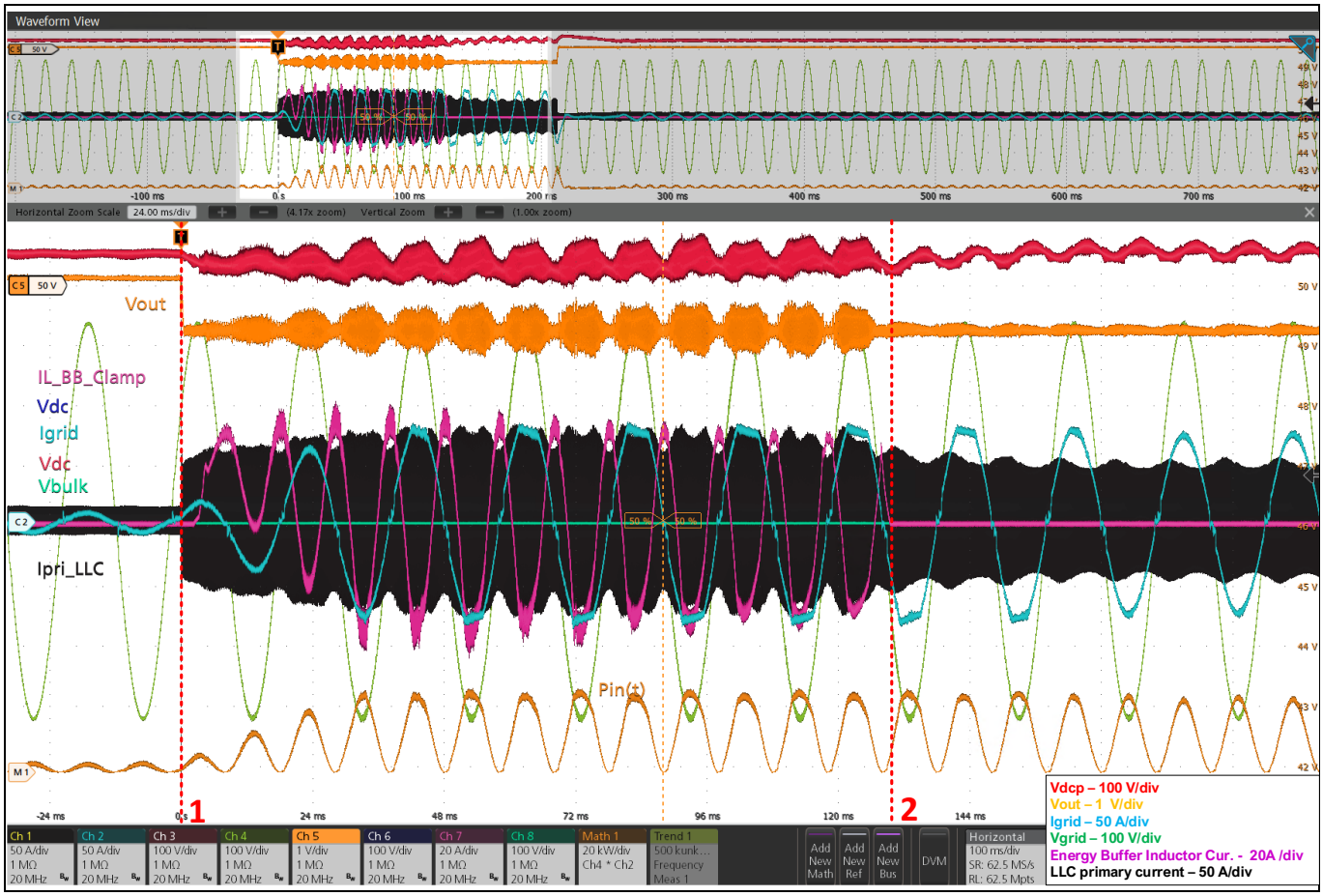


Figure 22 **Experimental results during load jump from 10% to 100% of the nominal load**

Point 1: The output load jumps from 10% to 100% with 5 A/µs slope.

Point 1-2: In order to limit the response of the grid and not have a rapid current change at the input, the EB is enabled and provides a portion of the energy required by the load, so that the grid doesn't have to take over completely. This maintains a smooth increase of the grid power as can be seen in the orange waveform at the bottom of Figure 22. At the same time, the DC-link voltage is kept to the regulated value, therefore energy is transferred back and forth between the DC-link and the electrolytic capacitor bank.

Point 2: As in the LCDO event, the condition for the EB to be turned off is the same as in the previous case; the voltage of the capacitor bank must again be close to the DC-link voltage.

Similarly, in Figure 23 a series of load jumps is tested with 10 Hz of repetition frequency.

Point 1-2: The output load jumps from 10 A to 240 A and as soon as the DC-link voltage drops below the threshold value set, the EB starts operating in boost and buck mode to provide the required energy. As explained before, there is bidirectional power flow.

Point 2-3: The output load steps down from 240 A to 10 A. The load is so small that the DC-link starts rising (considering that there are electrolytic capacitors at the DC output rail as well) and the EB starts charging the large capacitor bank until the two voltages are equalized again.

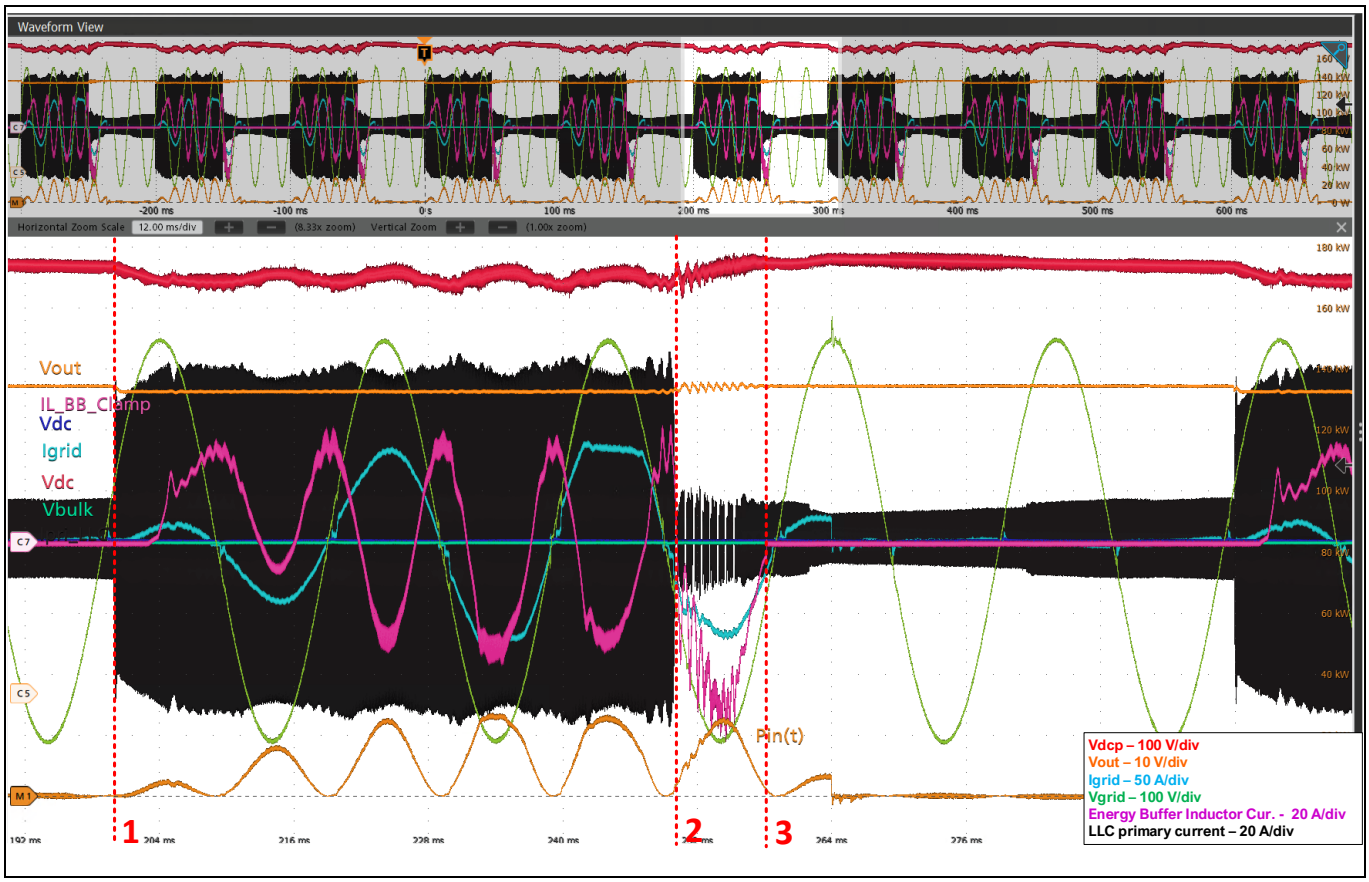


Figure 23 Experimental results during repetitive load jumps from 10 A to 240 A

Another set of results for the same operating condition is presented in Figure 24, but in this case the slew rate of the grid power is increased in the firmware of the microcontroller, resulting in a smaller duration of the EB operation.

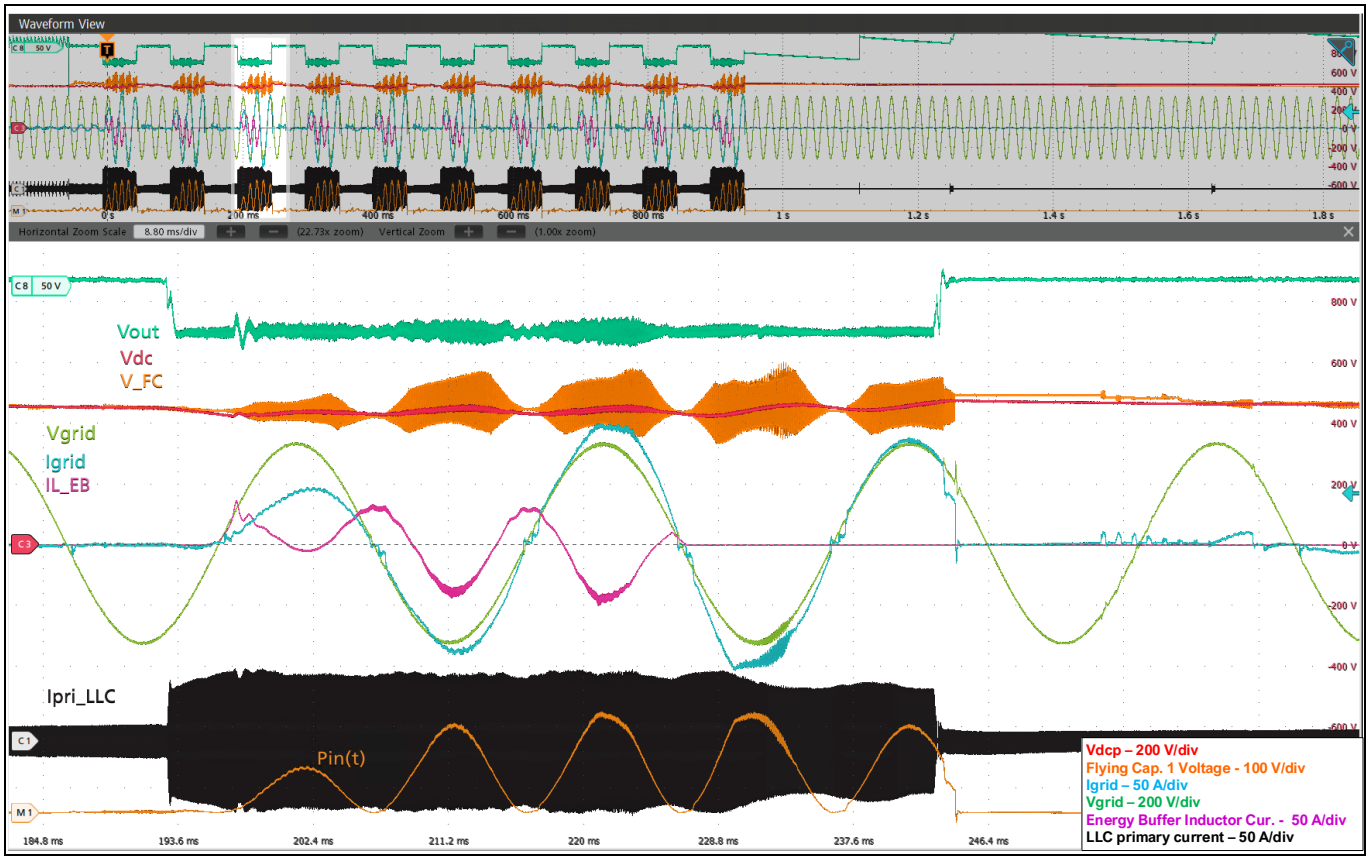


Figure 24 Experimental results during repetitive load jumps from 10 A to 240 A with higher permissible slew rate of the power from the grid

In Figure 25 a load jump from 24 A to 350 A (5 A/µs) is tested as well, for the cases where the step load increases over the nominal load for 50 ms.

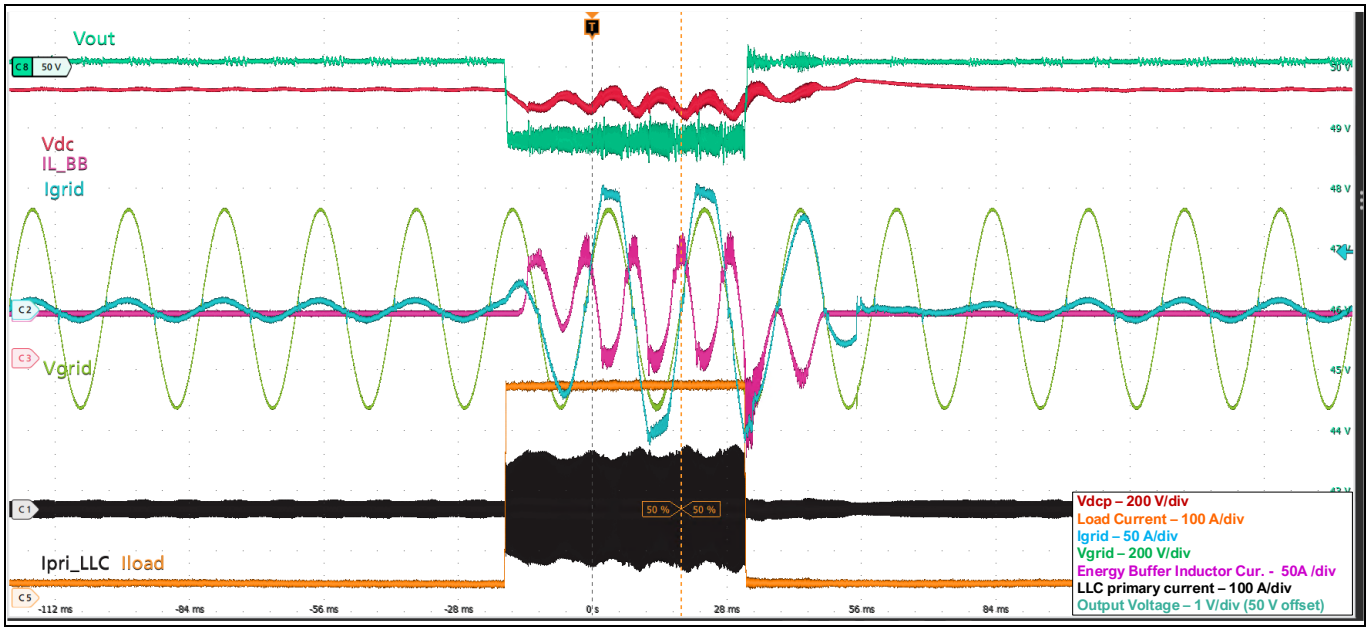


Figure 25 Experimental results during load jump from 10% to 140% of the nominal load

The output voltage follows the droop control reference and the overshoot and undershoot are minimum.

3.3.4 Voltage sag

In the case of a voltage sag down to 160 V, the input current increases rapidly. Similarly, to limit the maximum slope of the power supplied from the grid, the EB is automatically enabled during the voltage sag and provides the missing energy to the load. An example of a voltage sag for 500 ms is shown in Figure 26 for an output load equal to 220 A and in Figure 27 for an output load equal to 240 A. In the second case, where the load is higher, the EB operates for a longer time to support the limited current allowed from the grid.

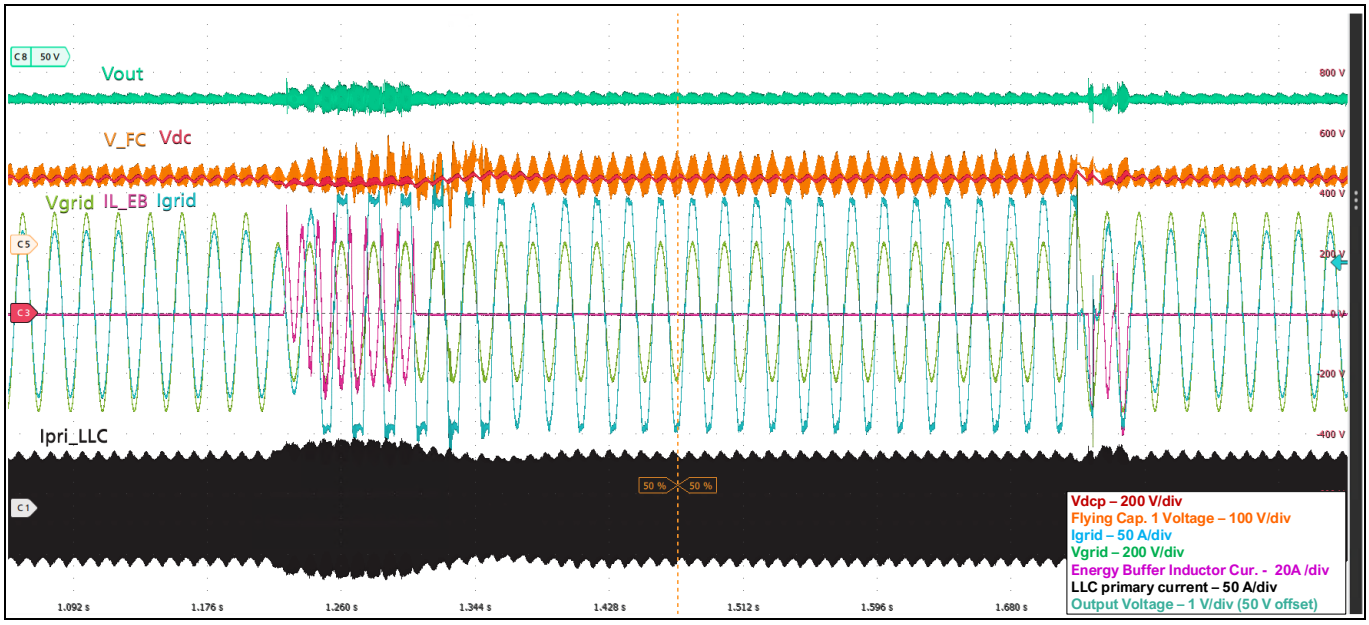


Figure 26 Experimental results during voltage sag down to 160 V input voltage for 500 ms under 220 A load

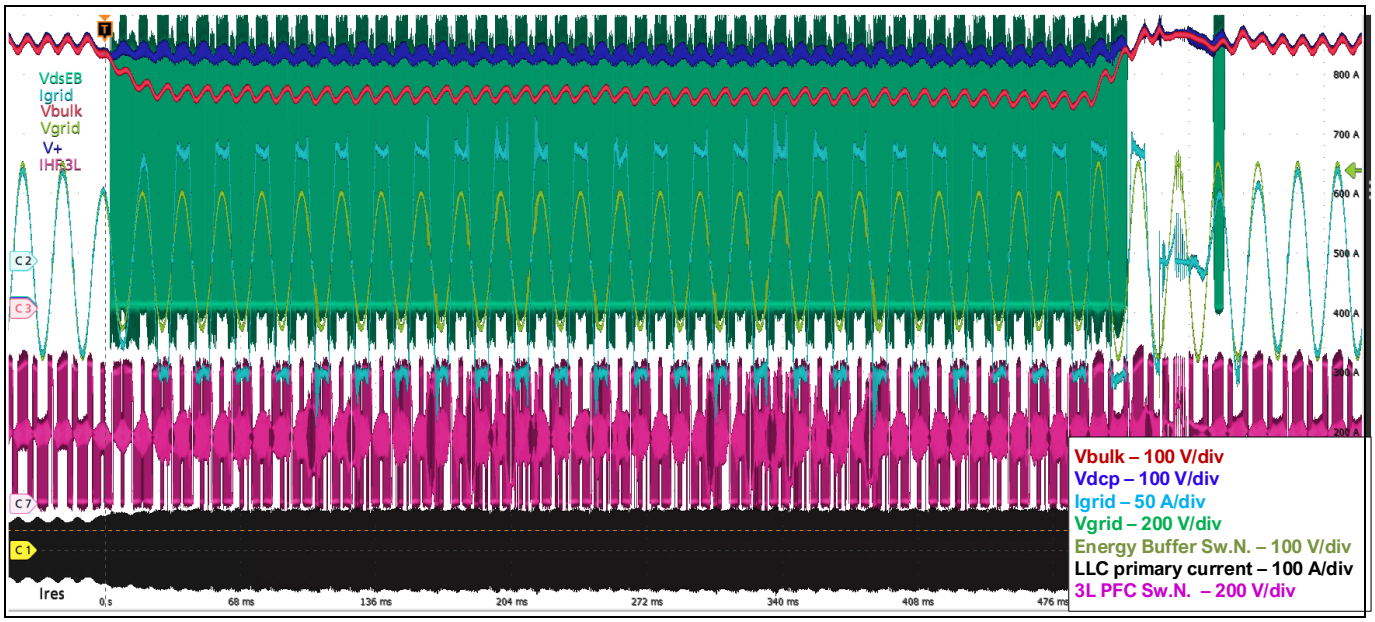


Figure 27 Experimental results during voltage sag down to 160 V input voltage for 500 ms under 240 A load

4 Control scheme

The energy buffer circuit controls the voltages on either side of the buck-boost converter, meaning the DC-link voltage as well as the electrolytic bank voltages. The PFC control scheme includes both the control of the DC-link voltage as well as the current on the two PFC chokes. The speed of the current loop is faster (inner loop), while that of the voltage loop is slower (outer loop), as shown in Figure 28. More details about the PFC control logic are explained in the application note of the reference design REF_12KW_HFHD_PSU [3].

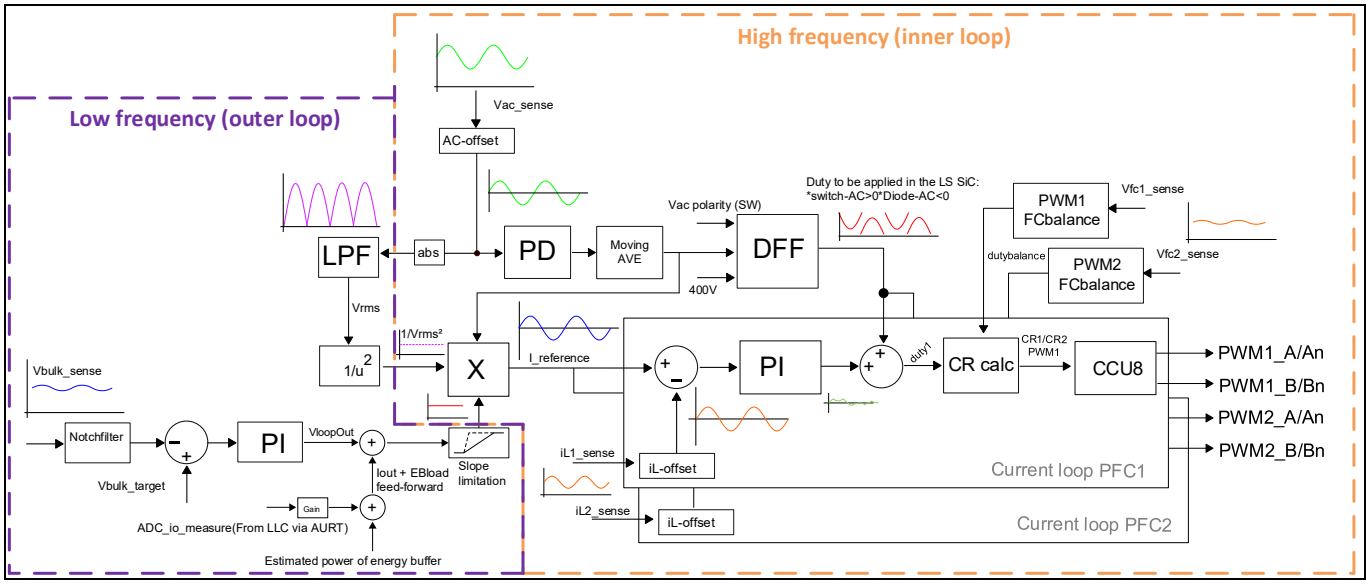


Figure 28 Control scheme of the PFC converter, including the current and voltage loops

As can be seen from Figure 28, the only effect that the EB has on the PFC control loop is through the feed-forward term that corresponds to the energy transferred from/to the EB together with the output load on the LLC side. The estimated power of the EB is dependent on the voltage level of the capacitor bank.

Moving to the control of the EB itself, a relative diagram is given in Figure 29.

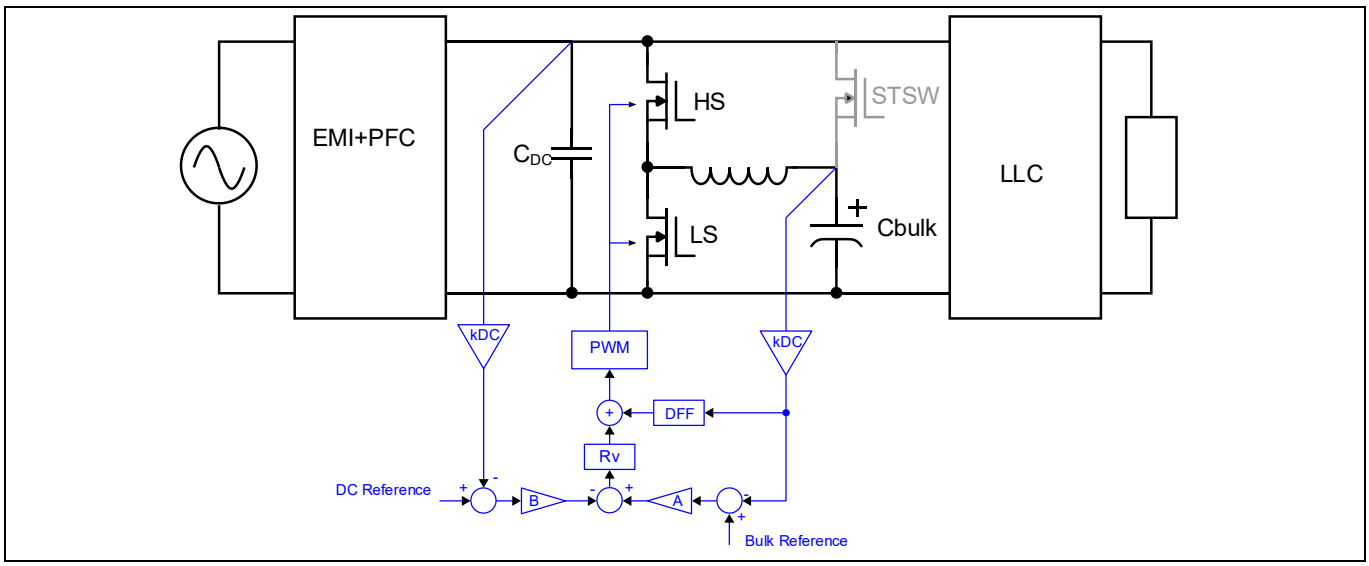


Figure 29 Block diagram of the EB control loop with the weighted gains on the DC-link and bulk capacitance voltage errors

REF_12KW_HFHD_PSU (Energy Buffer)
Control scheme

The EB consists of a bidirectional buck-boost converter and both input and output rails are monitored, the DC-link and the bulk capacitor bank voltages. The error signals coming from the two voltage rails have different weights (A and B), assigning a higher gain on the DC-link voltage error. In the end, the direction of the power transfer is automatically decided depending on the theoretical values of the DC voltages that derive from the applied duty cycle and the actual voltages on the two rails, according to the weights that are given.

Both are combined to generate a single error signal for the control and the PWM generation signal. Moreover, a feed-forward term for the duty cycle of the converter is generated based on the bulk voltage measurement.

5 Summary

The auxiliary circuit of the energy buffer (EB) is verified and confirmed in a 12 kW power supply unit REF_12KW_HFHD_PSU for an AI data center application.

Multiple transient conditions are experimentally successfully tested without disturbing the PSU operation or damaging components, for example the startup, load jumps, line cycle drop-out (LCDO), and voltage sag events. The temperatures of the components of the auxiliary circuit are also measured during periodic operations under nominal loads. In Figure 30, the thermal image of the energy buffer devices is depicted considering continuous 10% to 100% load jumps with a 10 Hz repetition. The maximum temperature recorded on the device case is 64°C with open chassis and airflow on top of the daughterboard, while the temperature of the inductor is also way below its rated limits.

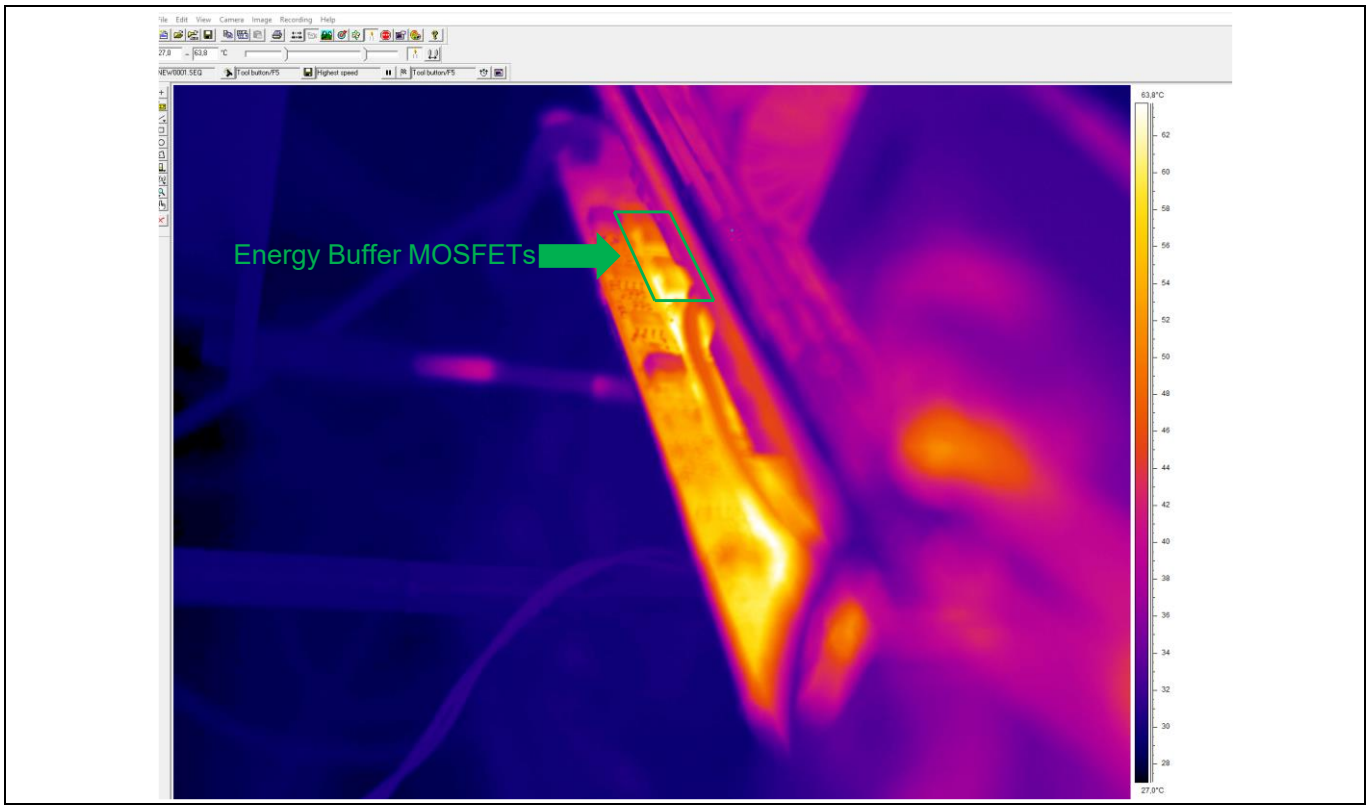


Figure 30 Thermal image of the energy buffer devices during the continuous 10 Hz load jumps from 10% to 100% load

Not only is the power density of the whole PSU increased by using this auxiliary circuit, but also grid-current shaping is achieved, keeping the grid power within acceptable limits and slowing down the slew rate during transient events.

The control of the EB circuit is simple and effective, allowing reliable operation of the converter, supporting LCDO, load step changes, voltage sag, and grid shaping functionality.

Overall, it is proven that the proposed and implemented solution provides great benefits to power supplies for data centers.

6 List of figures

References

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Acronyms/abbreviations

Table 2 Acronyms/abbreviations

Acronym	Description
AC/DC	alternating current to alternating current
BBU	battery backup unit
BOM	bill of materials
DC	direct current
DC/DC	direct current to direct current
EB	energy buffer
ESD	electrostatic discharge
FB	full-bridge
GaN	gallium nitride
GPU	graphic processing unit
LCDO	line cycle drop-out
LLC	LLC resonant converter
OCP	overcurrent protection
ORv3	open rack version 3
OVP	overvoltage protection
PCB	printed circuit board
PFC	power factor correction
PSU	power supply unit
Si	silicon
SiC	silicon carbide
SR	synchronous rectification
UVP	undervoltage protection
3L_IL_PFC	three level interleaved power factor correction

Revision history

Document revision	Date	Description of changes
V 1.0	2025-11-30	Initial release

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Edition 2025-11-30

Published by

Infineon Technologies AG

81726 Munich, Germany

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AN133109

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