Solution to abnormal high-side output (HO) pulse

2EDL8x2x timing requirement

About this document

Scope and purpose

This document describes the timing requirement needed from the time the high-side boot voltage (HB-HS) has reached undervoltage lockout (UVLO) rising threshold to the first high-side input (HI) pulse in order to avoid occurrence of the abnormal HO pulse in a full-bridge configuration with diagonal driving scheme using the **2EDL8x2x** gate driver.

Intended audience

Power supply designers using the 2EDL8x2x gate driver

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1 Occurrence of abnormal HO pulse

When the falling edge of the first HI pulse comes close to the internal UVLO release, a glitch or abnormal HO pulse can be observed as shown in the simulation result below.

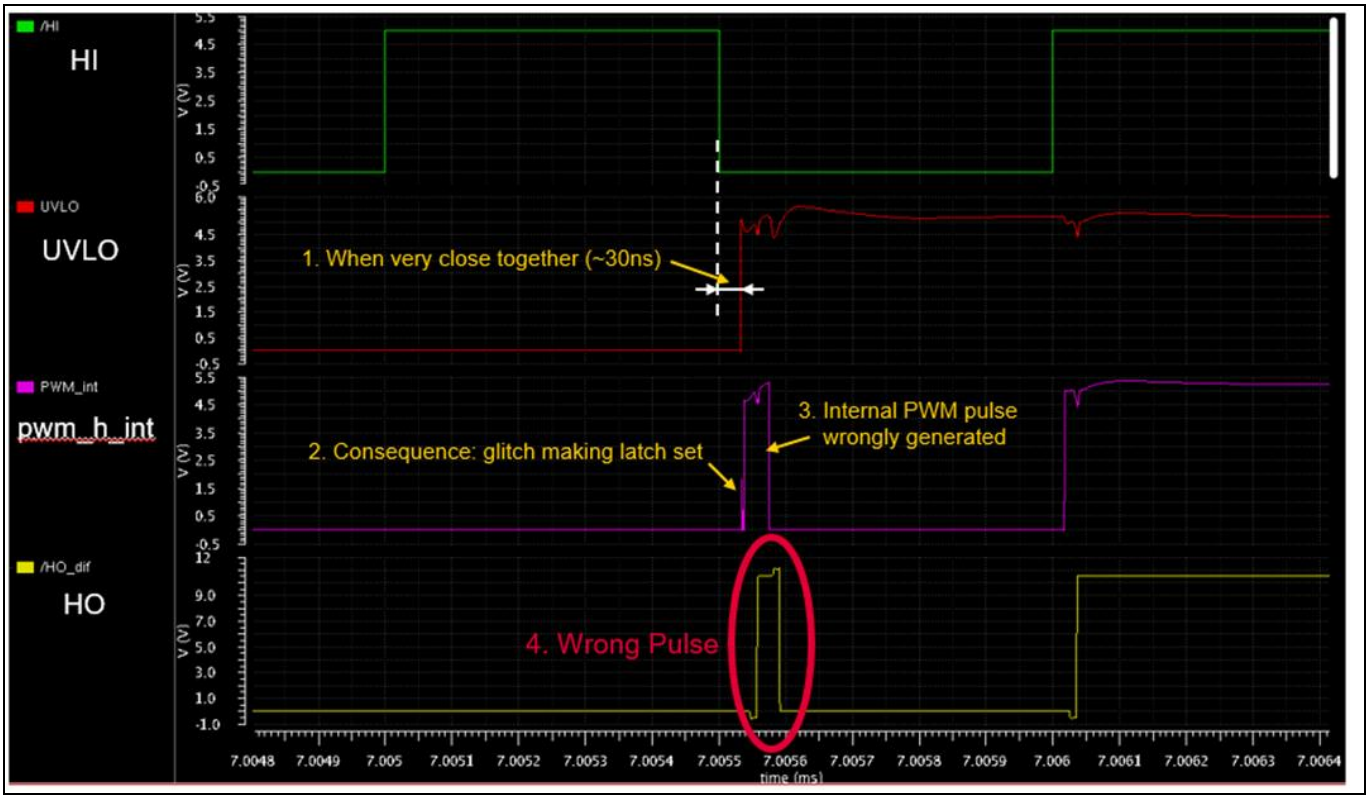


Figure 1 Simulation of abnormal HO pulse

2 Minimum timing requirement for the application

The first HI pulse should come after the overall delay time of the internal UVLO, which is dictated by the internal supplies start-up time plus the RC constant deglitching time. The internal UVLO delay time variation considering all process corners and temperature can be seen in **Figure 2**. It is recommended to give the first HI pulse 10 µs after the high-side boot-cap voltage (HB-HS) has reached the UVLO rising threshold to ensure that it is not within the UVLO release time, as shown in **Figure 3**.

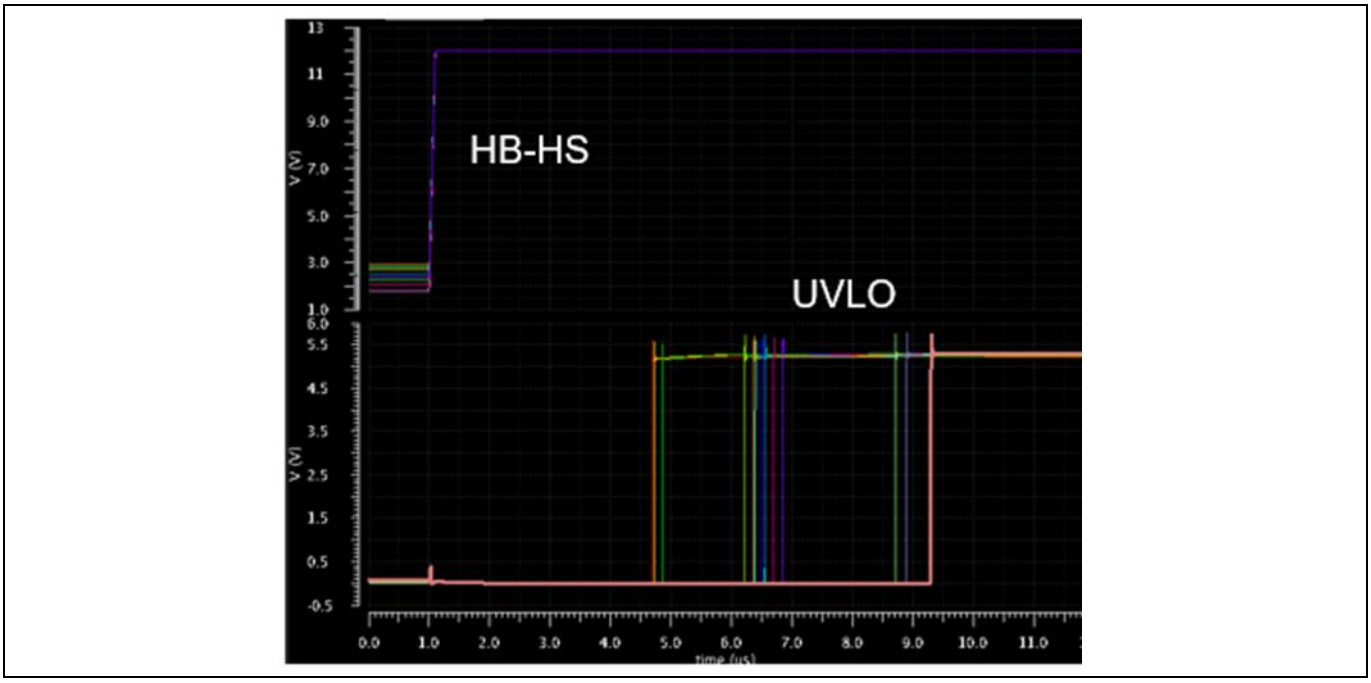


Figure 2 UVLO delay time variation

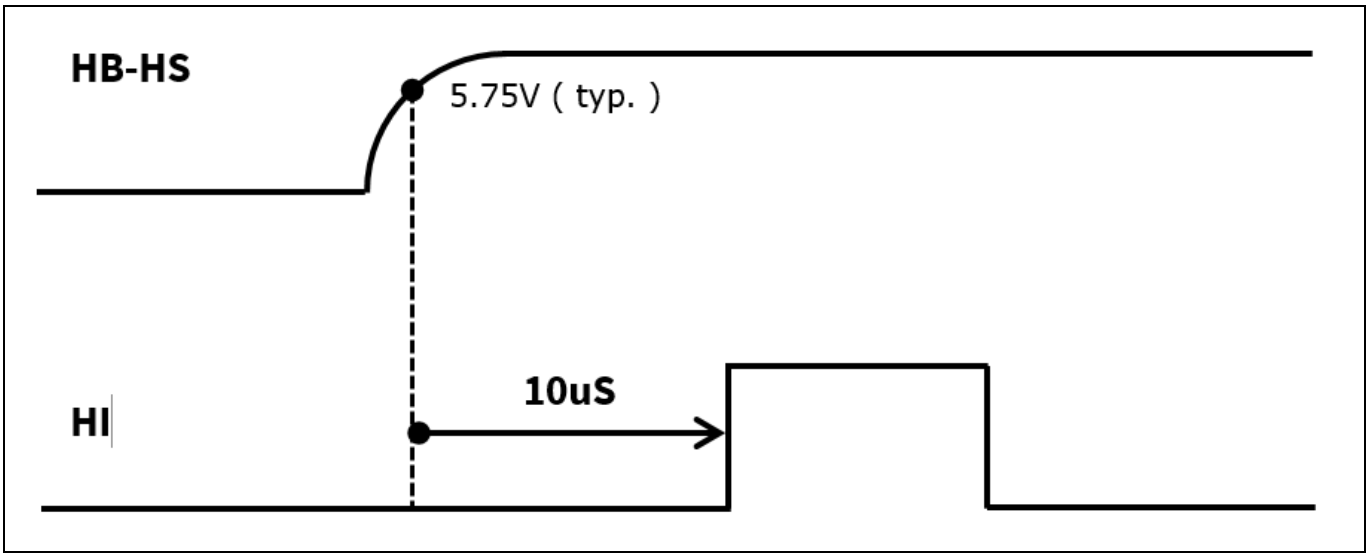


Figure 3 First HI pulse timing requirement

Revision history

Document version	Date of release	Description of changes
V 1.0	2022-06-29	Initial release

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Edition 2022-06-29

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference
AN_2001_PL88_2002_165704

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